TMCS1126-Q1 AEC-Q100、 高精度 500kHz ホール効果電流センサ、強化動作電圧、過電流検出、周囲磁界除去機能搭載

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - 温度グレード 1:-40℃～125℃、T_A
- 機能安全対応
  - 機能安全システム設計に役立つ資料を利用可能
- 高い連続電流能力:$80A_{RMS}$
- 堅牢な強化絶縁
- 高い精度
  - 感度誤差:±0.1%
  - 感度の温度ドリフト:±20ppm/℃
  - 感度の寿命ドリフト:±0.2%
  - オフセット誤差:±0.2mV
  - オフセット温度ドリフト:±2μV/℃
  - オフセット寿命ドリフト:±0.2mV
  - 非線形性:±0.1%
- 外部の磁界に対する高い耐性
- 高精度ゼロ電流リファレンス出力
- 高速応答
  - 信号帯域幅:500kHz
  - 応答時間:250ns
  - 伝搬遅延:60ns
  - 過電流検出応答:100ns
- 動作電源電圧範囲:3V～5.5V
- 双方向および単方向の電流センシング
- 複数の感度オプション:
  - 15mV/A～150mV/A の範囲
- 安全関連認証 (予定)
  - UL 1577 部品認定プログラム
  - IEC/CB 62368-1

2 アプリケーション

- オンボード チャージャ
- DC/DC コンバータ
- 回転子励起
- HVAC 向けコンプレッサ
- 高電圧 PDU
- EV (電気自動車) 充電

3 概要

TMCS1126-Q1 は、業界をリードする絶縁性と精度を備えたガルバニック絶縁ホール効果電流センサです。入力電流に比例する出力電圧により、優れた直線性と、あらゆる感度オプションで低ドリフトを実現しています。ドリフト補償を内蔵した高精度のシグナル コンディショニング回路は、温度範囲と寿命全体にわたって、システム レベルのキャリブレーションを必要としない 1.4% 未満の最大感度誤差を達成しており、寿命と温度ドリフトの両方を含む 1 回限りの室温キャリブレーションで、0.9% 未満の最大感度誤差を達成しています。

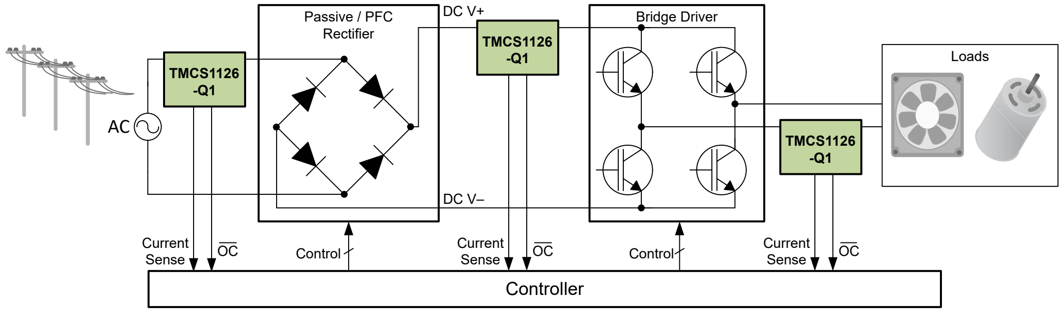
AC または DC 入力電流は内部導体を流れ、そこで発生する磁界を、内蔵のオンチップ ホール効果センサで測定します。コアレス構造のため、磁気コンセントレータは不要です。差動ホール センサは、外部の浮遊磁界による干渉を排除します。導体抵抗が小さいと、測定可能な電流範囲が最大 ±103A まで拡大すると同時に、電力損失を最小化し、放熱要件を緩和できます。$5kV_{RMS}$ に耐える絶縁と、最小 8mm の沿面距離および空間距離により、高いレベルの信頼性の高い寿命の強化動作電圧を実現します。内蔵シールドにより、優れた同相除去と過渡耐性を実現しています。

固定感度とすることで、デバイスは 3V～5.5V の単一電源で動作でき、レシオメトリック誤差をなくし、電源ノイズ除去を向上させています。テキサス・インスツルメンツは、低コスト オプションとして TMCS1126xxB-Q1 を提供しています。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
TMCS1126-Q1	DVG (SOIC、10)	10.3mm × 10.3mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



代表的なアプリケーション

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4 Device Comparison

表 4-1. Device Comparison

PRODUCT[3]	SENSITIVITY	ZERO CURRENT OUTPUT VOLTAGE	I_{IN} LINEAR MEASUREMENT RANGE[1]	
			V_S = 5V	V_S = 3.3V
TMCS1126ADx-Q1	20mV/A	2.5V	±120A[2]	–120A to 35A[2]
TMCS1126A1x-Q1	25mV/A		±96A[2]	–96A to 28A[2]
TMCS1126A7x-Q1	30mV/A		±80A[2]	–80A to 23.3A[2]
TMCS1126A8x-Q1	40mV/A		±60A[2]	–60A to 17.5A[2]
TMCS1126A2x-Q1	50mV/A		±48A[2]	–48A to 14A[2]
TMCS1126A3x-Q1	75mV/A		±32A	–32A to 9.3A
TMCS1126A4x-Q1	100mV/A		±24A	–24A to 7A
TMCS1126A5x-Q1	150mV/A		±16A	–16A to 4.7A
TMCS1126B6x-Q1	15mV/A	1.65V	–103.3A to 216.7A[2]	±103.3A[2]
TMCS1126BDx-Q1	20mV/A		–77.5A to 162.5A[2]	±77.5A[2]
TMCS1126B1x-Q1	25mV/A		–62A to 130A[2]	±62A[2]
TMCS1126BCx-Q1	26.4mV/A		–58.7A to 123A[2]	±58.7A[2]
TMCS1126B9x-Q1	33mV/A		–46.9A to 98.5A[2]	±46.9A[2]
TMCS1126BBx-Q1	39.6mV/A		–39.1A to 82A[2]	±39.1A[2]
TMCS1126B8x-Q1	40mV/A		–38.7A to 81.2A[2]	±38.7A[2]
TMCS1126B2x-Q1	50mV/A		–31A to 65A[2]	±31A
TMCS1126BAx-Q1	66mV/A		–23.5A to 49.2A[2]	±23.5A
TMCS1126B3x-Q1	75mV/A		–20.7A to 43.3A[2]	±20.7A
TMCS1126B4x-Q1	100mV/A		–15.5A to 32.5A	±15.5A
TMCS1126BEx-Q1	132mV/A		–11.7A to 24.6A	±11.7A
TMCS1126B5x-Q1	150mV/A		–10.3A to 21.7A	±10.3A
TMCS1126C1x-Q1	25mV/A	0.33V	–9.2A to 183A[2]	–9.2A to 115A[2]
TMCS1126C2x-Q1	50mV/A		–4.6A to 91.4A[2]	–4.6A to 57.4A[2]
TMCS1126C3x-Q1	75mV/A		–3.1A to 60.9A[2]	–3.1A to 38.3A[2]
TMCS1126C4x-Q1	100mV/A		–2.3A to 45.7A[2]	–2.3A to 28.7A
TMCS1126C5x-Q1	150mV/A		–1.5A to 30.5A	–1.5A to 19.1A

(1) Linear range limited by the maximum output swing to power supply (3V to 5.5V) and ground, not by thermal limitations.
(2) Current levels must remain below both allowable continuous DC/RMS and transient peak current safe operating areas to not exceed device thermal limits. See the *Safe Operating Area* section.
(3) For more information on the device name and device options, see the *Device Nomenclature* section.

5 Pin Configuration and Functions

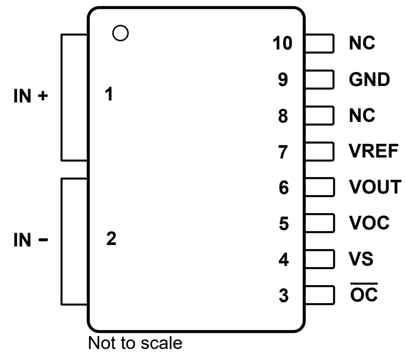


図 5-1. DVG Package 10-Pin SOIC Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN+	Analog Input	Input current positive pin
2	IN–	Analog Input	Input current negative pin
3	$\overline{OC}$	Digital Output	Overcurrent output, open-drain active low. Connect pin to GND if not used.
4	VS	Analog	Power supply
5	VOC	Analog Input	Overcurrent threshold. Sets overcurrent threshold. Connect pin to VS if not used.
6	VOUT	Analog Output	Output voltage
7	VREF	Analog Output	Zero current output voltage reference
8	NC	-	Reserved. Pin can be connected to GND or left floating.
9	GND	Analog	Ground
10	NC	-	Reserved. Pin can be connected to GND or left floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage	V_S		GND – 0.3	6	V
Analog input		VOC	GND – 0.3	(V_S) + 0.3	V
Analog output		VOUT, VREF			
Digital output		$\overline{OC}$			
No Connect		NC			
Junction temperature	T_J		–65	165	°C
Storage temperature	T_{stg}		–65	165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Operating supply voltage	3	5	5.5	V
T_A [1]	Operating free-air temperature	–40		125	°C

(1) Input current safe operating area is constrained by junction temperature. Recommended condition based on use with the *TMCS1126xEVM*. Input current rating is derated for elevated ambient temperatures.

6.4 Thermal Information

THERMAL METRIC[1]		TMCS1126[2] DVG (SOIC-W-10) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	10.1	
Ψ_{JT}	Junction-to-top characterization parameter	4.4	
Ψ_{JB}	Junction-to-board characterization parameter	8.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Applies when device is mounted on the *TMCS1126xEVM*. For more details, see the *Safe Operating Area* section.

6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[(1)]	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage[(1)]	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
CTI	Comparative tracking index	DIN EN 60112; IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ $600V_{RMS}$	I-IV	
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1344	V_{PK}
V_{IOWM}	Maximum reinforced isolation working voltage	AC voltage (sine wave)	600	V_{RMS}
			849	V_{DC}
	Maximum basic isolation working voltage	AC voltage (sine wave)	950	V_{RMS}
			1344	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = \sqrt{2} \times V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[(2)]	Test method per IEC 62368-1, 1.2/50µs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	10000	V_{PK}
q_{pd}	Apparent charge[(3)]	Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	pC
C_{IO}	Barrier capacitance, input to output[(4)]	V_{IO} = 0.4 sin (2πft), f = 1MHz	0.6	pF
R_{IO}	Isolation resistance, input to output[(4)]	V_{IO} = 500V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	Ω
		V_{IO} = 500V at T_S = 150°C	$> 10^{9}$	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Take care to maintain the creepage and clearance distance of the board design to make sure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device.

6.6 Electrical Characteristics

at T_A = 25°C, V_S = 5V on TMCS1126Axx-Q1, V_S = 3.3V on TMCS1126Bxx-Q1 and TMCS1126Cxx-Q1 (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
R_{IN}	Input Conductor Resistance	IN+ to IN–		0.7		mΩ
R_{IN}	Input Conductor Resistance Temperature Drift	T_A= –40ºC to 125ºC		2.1		µΩ/°C
$I_{IN,MAX}$	Maximum Continuous Input Current[(1)]	T_A= 25ºC		80		A_{RMS}
		T_A= 125ºC		44		
OUTPUT						
S	Sensitivity	TMCS1126x6x-Q1		15		mV/A
		TMCS1126xDx-Q1		20		
		TMCS1126x1x-Q1		25		
		TMCS1126xCx-Q1		26.4		
		TMCS1126x7x-Q1		30		
		TMCS1126x9x-Q1		33		
		TMCS1126xBx-Q1		39.6		
		TMCS1126x8x-Q1		40		
		TMCS1126x2x-Q1		50		
		TMCS1126xAx-Q1		66		
		TMCS1126x3x-Q1		75		
		TMCS1126x4x-Q1		100		
		TMCS1126xEx-Q1		132		
		TMCS1126x5x-Q1		150		
e_S	Sensitivity Error: Grade A	TMCS1126xxA-Q1, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V		±0.1	±0.4	%
	Sensitivity Error: Grade B	TMCS1126xxB-Q1, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V		±0.3	±1	
$S_{drift,therm}$	Sensitivity Thermal Drift: Grade A	TMCS1126xxA-Q1, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V, T_A = −40°C to 125°C		±20	±50	ppm/°C
	Sensitivity Thermal Drift: Grade B	TMCS1126xxB-Q1, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V, T_A = −40°C to 125°C		±40	±100	
$S_{drift, life}$	Sensitivity Lifetime Drift[(2)]	0.05V ≤ V_{OUT} ≤ V_S − 0.2V		±0.2	±0.5	%
e_{NL}	Nonlinearity Error: Grade A	TMCS1126xxA-Q1, V_{OUT} = 0.1V to V_S – 0.1V		±0.1		%
	Nonlinearity Error: Grade B	TMCS1126xxB-Q1, V_{OUT} = 0.1V to V_S – 0.1V		±0.2		
$V_{OUT,0A}$	Zero Current Output Voltage	TMCS1126Axx-Q1, I_{IN} = 0A		2.5		V
		TMCS1126Bxx-Q1, I_{IN} = 0A		1.65		
		TMCS1126Cxx-Q1, I_{IN} = 0A		0.33		

at T_A = 25°C, V_S = 5V on TMCS1126Axx-Q1, V_S = 3.3V on TMCS1126Bxx-Q1 and TMCS1126Cxx-Q1 (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OE}	Output Voltage Offset Error: Grade A	TMCS1126x6A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.1	±0.8	mV
		TMCS1126xDA-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.2	±1	
		TMCS1126x1A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.2	±1	
		TMCS1126xCA-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.2	±1	
		TMCS1126x7A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.2	±1	
		TMCS1126x9A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.2	±1	
		TMCS1126xBA-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.3	±1.5	
		TMCS1126x8A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.3	±1.5	
		TMCS1126x2A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.3	±1.5	
		TMCS1126xAA-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.4	±2	
		TMCS1126x3A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.4	±2	
		TMCS1126x4A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.5	±2.5	
		TMCS1126xEA-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.6	±3	
		TMCS1126x5A-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.6	±3	
	Output Voltage Offset Error: Grade B	TMCS1126x6B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.4	±1.5	
		TMCS1126xDB-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.7	±2	
		TMCS1126x1B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.7	±2	
		TMCS1126xCB-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.7	±2	
		TMCS1126x7B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.7	±2	
		TMCS1126x9B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.7	±2	
		TMCS1126xBB-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.8	±2.5	
		TMCS1126x8B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.8	±2.5	
		TMCS1126x2B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±0.8	±2.5	
		TMCS1126xAB-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±1	±3	
		TMCS1126x3B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±1	±3	
		TMCS1126x4B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±1.5	±4.5	
		TMCS1126xEB-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±2	±6	
		TMCS1126x5B-Q1, $V_{OUT,0A} - V_{REF}$, I_{IN} = 0A		±2	±6	

at T_A = 25°C, V_S = 5V on TMCS1126Axx-Q1, V_S = 3.3V on TMCS1126Bxx-Q1 and TMCS1126Cxx-Q1 (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OE, drift, therm}$	Output Voltage Offset Thermal Drift	TMCS1126x6x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±10	±30	µV/°C
		TMCS1126xDx-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±10	±30	
		TMCS1126x1x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±10	±30	
		TMCS1126xCx-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±15	±40	
		TMCS1126x7x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±15	±40	
		TMCS1126x9x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±15	±40	
		TMCS1126xBx-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±15	±40	
		TMCS1126x8x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±15	±40	
		TMCS1126x2x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±15	±40	
		TMCS1126xAx-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±20	±50	
		TMCS1126x3x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±20	±70	
		TMCS1126x4x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±30	±80	
		TMCS1126xEx-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±40	±100	
		TMCS1126x5x-Q1, $V_{OUT,0A}$ − V_{REF}, I_{IN} = 0A, T_A = −40°C to 125°C		±40	±100	
$I_{OS, drift, life}$	Offset Lifetime Drift[2]	Input Referred, ($V_{OUT,0A}$ − V_{REF}) / S, I_{IN} = 0A		±8	±16	mA
PSRR	Power Supply Rejection Ratio: Grade A	TMCS1126xxA-Q1, Input Referred, V_S = 3V to 5.5V, T_A= –40ºC to 125ºC		±10	±45	mA/V
	Power Supply Rejection Ratio: Grade B	TMCS1126xxB-Q1, Input Referred, V_S = 3V to 5.5V, T_A= –40ºC to 125ºC		±40	±80	
CMTI	Common Mode Transient Immunity[3]	V_{CM} = 1000V, ΔV_{OUT} < 200mV, 1µs		150		kV/µs
CMRR	Common Mode Rejection Ratio	Input Referred, DC to 60Hz		5		µA/V
CMFR	Common Mode Field Rejection	Uniform External Magnetic Field, Input Referred, DC to 1kHz			10	mA/mT
	Input Noise Density	Input Referred, Full Bandwidth		150		µA/√Hz
$C_{L,MAX}$	Maximum Capacitive Load	VOUT to GND		4.7		nF
	Short Circuit Output Current	VOUT short to GND, short to V_S		50		mA
$Swing_{VS}$	Swing to V_S Power Supply Rail	R_L = 10kΩ to GND, T_A= –40ºC to 125ºC		V_S – 0.02	V_S – 0.05	V
$Swing_{GND}$	Swing to GND			5	10	mV
BANDWIDTH & RESPONSE						
BW	Analog Bandwidth	- 3dB Gain		550		kHz
SR	Slew Rate[4]	Output rate of change between reaching 10% and 90% of final value as shown in *Figure 7-2* with a 100ns input step		6		V/µs
t_r	Response Time[4]	Time between input and output reaching 90% of final values, as shown in *Figure 7-2* with a 100ns input step and a 1V output transition		250		ns
t_{pd}	Propagation Delay[4]	Time between input and output reaching 10% of final values as shown in *Figure 7-2* with a 100ns input step and a 1V output transition		60		ns
	Current Overload Recovery Time			300		ns

at T_A = 25°C, V_S = 5V on TMCS1126Axx-Q1, V_S = 3.3V on TMCS1126Bxx-Q1 and TMCS1126Cxx-Q1 (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTEGRATED REFERENCE						
V_{REF}	Reference Output Voltage: Grade A	TMCS1126AxA-Q1	2.496	2.5	2.504	V
		TMCS1126BxA-Q1	1.647	1.65	1.653	
		TMCS1126CxA-Q1	0.329	0.33	0.331	
	Reference Output Thermal Drift: Grade A	TMCS1126AxA-Q1		20	50	µV/°C
		TMCS1126BxA-Q1		15	33	
		TMCS1126CxA-Q1		3	7	
	Reference Output Lifetime Drift: Grade A	TMCS1126AxA-Q1		±1.3	±2.5	mV
		TMCS1126BxA-Q1		±0.9	±1.7	
		TMCS1126CxA-Q1		±0.3	±0.5	
V_{REF}	Reference Output Voltage: Grade B	TMCS1126AxB-Q1	2.49	2.5	2.51	V
		TMCS1126BxB-Q1	1.64	1.65	1.66	
		TMCS1126CxB-Q1	0.32	0.33	0.34	
	Reference Output Thermal Drift: Grade B	TMCS1126AxA-Q1		40	100	µV/°C
		TMCS1126BxA-Q1		25	65	
		TMCS1126CxA-Q1		5	15	
	Reference Output Lifetime Drift: Grade B	TMCS1126AxB-Q1		±3	±5	mV
		TMCS1126BxB-Q1		±2	±3.5	
		TMCS1126CxB-Q1		±0.6	±1	
	Reference Output Voltage PSRR	V_S = 3V to 5.5V		80	150	µV/V
	Maximum Reference Output Capacitive Load			20		nF
	Reference Output Voltage Load Regulation	V_{REF} load = -5mA, 0mA, 5mA		0.25		mV/mA

at T_A = 25°C, V_S = 5V on TMCS1126Axx-Q1, V_S = 3.3V on TMCS1126Bxx-Q1 and TMCS1126Cxx-Q1 (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVER CURRENT DETECTION						
V_{OC}	Over Current Detection Threshold Voltage	V_{OC} = S x I_{OC} / 2.5	0.3		V_S	V
R_{OC}	Over Current Input Impedance		120			kΩ
	Over Current Hysteresis	TMCS1126x6x-Q1		8.4		A
		TMCS1126xDx-Q1		8.4		
		TMCS1126x1x-Q1		4.5		
		TMCS1126xCx-Q1		4.5		
		TMCS1126x7x-Q1		3.6		
		TMCS1126x9x-Q1		3.4		
		TMCS1126xBx-Q1		4.7		
		TMCS1126x8x-Q1		4.7		
		TMCS1126x2x-Q1		3.5		
		TMCS1126xAx-Q1		2.5		
		TMCS1126x3x-Q1		2.2		
		TMCS1126x4x-Q1		1.4		
		TMCS1126xEx-Q1		2.7		
		TMCS1126x5x-Q1		2.7		
	I_{OC} Error	T_A = –40°C to 125°C		±2	±10	%
	Over Current Detection Response Time	I_{IN} step = 120% of I_{OC}		100	250	ns
$\overline{OC}_{,OL}$	$\overline{OC}$ Pin Pull-down Voltage	I_{OL} = 3mA. T_A = –40°C to 125°C	GND	0.07	0.2	V
POWER SUPPLY						
V_S	Supply Voltage	T_A = –40ºC to 125ºC	3.0		5.5	V
I_Q	Quiescent Current	T_A = 25ºC		11	14	mA
		T_A = –40ºC to 125ºC			14.5	mA
	Power On Time	Time from V_S > 3V to valid output		34		ms

(1) Thermally limited by junction temperature, see *Absolute Maximum Ratings*. Applies when device mounted on *TMCS1126xEVM*. For more details, see the *Safe Operating Area* section.
(2) Lifetime and environmental drift specifications based on three lot AEC-Q100 qualification stress test results. Typical values are population mean+1σ from worst case stress test condition. Min/max are tested device population mean±6σ; devices tested in AEC-Q100 qualification stayed within min/max limits for all stress conditions. See *Lifetime and Environmental Stability* section for more details.
(3) Refer to the *Common-Mode Transient Immunity* section for details on common-mode transient response.
(4) Refer to the *Transient Response Parameters* section for details on transient response of the device.

6.7 Typical Characteristics

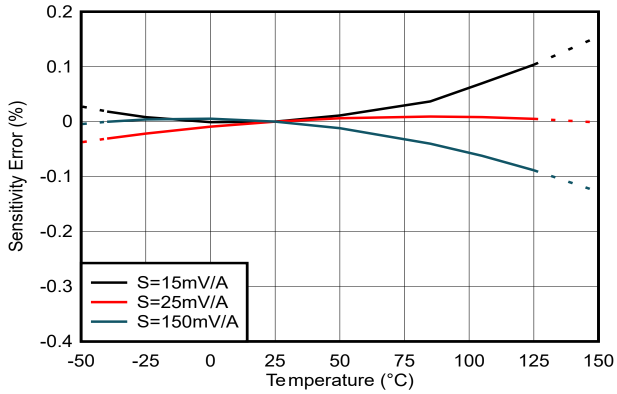


図 6-1. Sensitivity Error vs Temperature

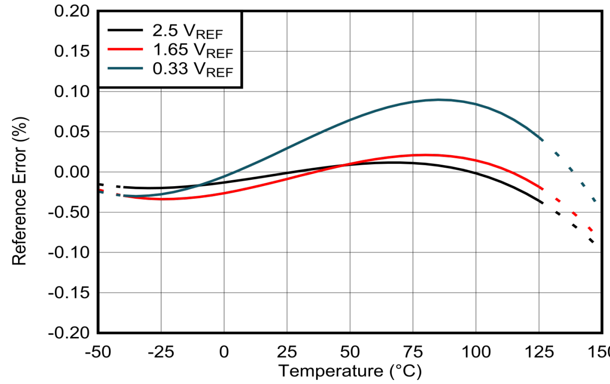


図 6-2. Reference Error vs Temperature

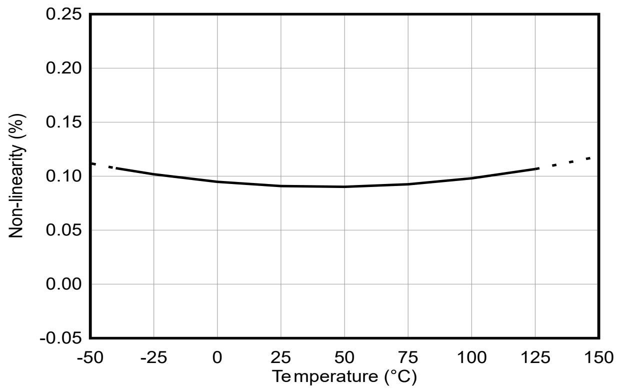


図 6-3. Non-Linearity vs Temperature

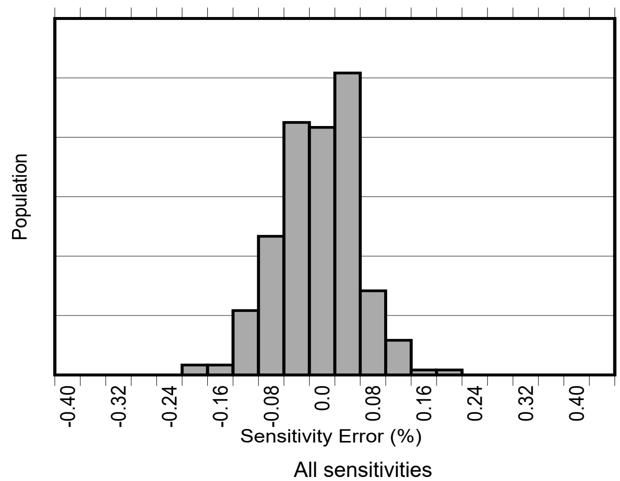


図 6-4. Sensitivity Error Production Distribution: Grade A

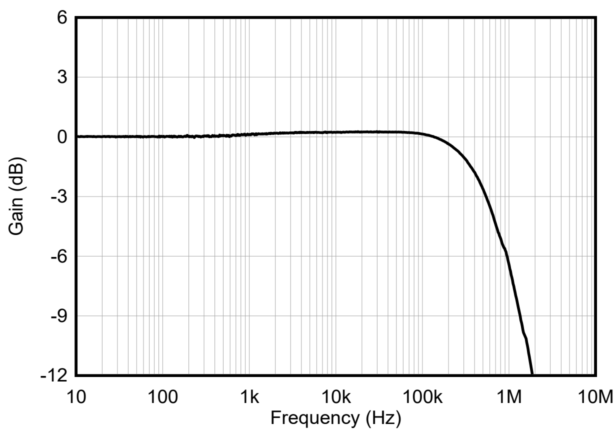


図 6-5. Sensitivity vs Frequency, All Gains Normalized to 1Hz

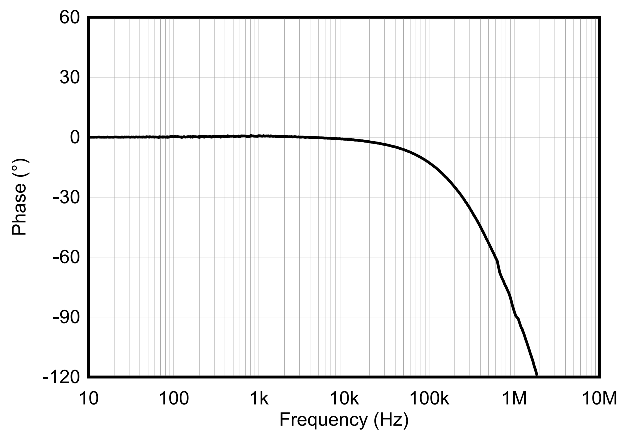


図 6-6. Phase vs Frequency, All Gains

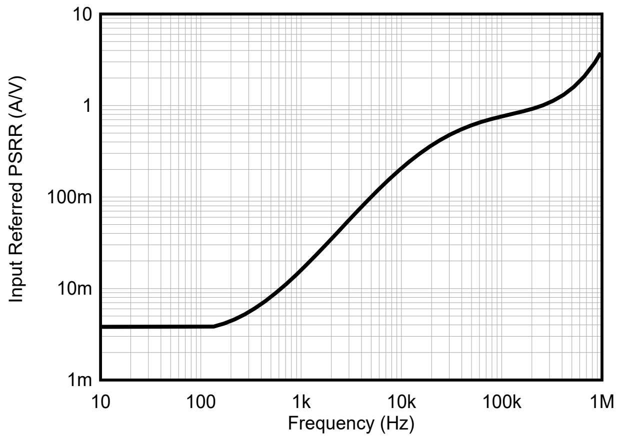


図 6-7. PSRR vs Frequency

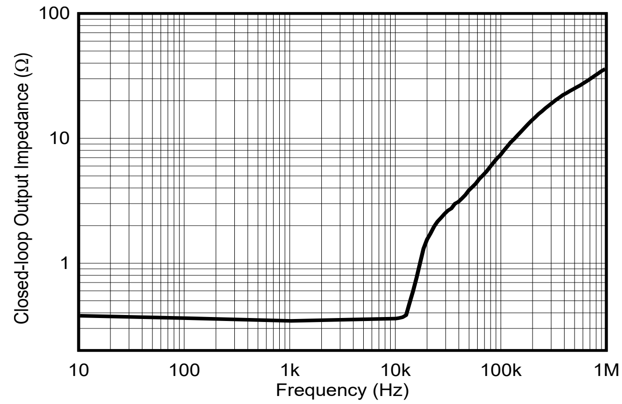


図 6-8. Output Impedance vs Frequency

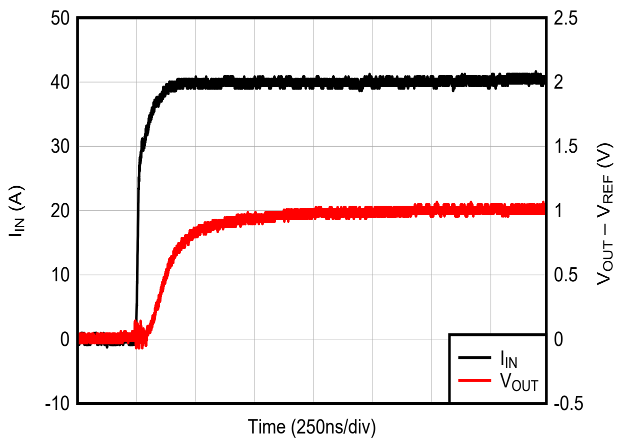


図 6-9. Voltage Output Step Response, Rising

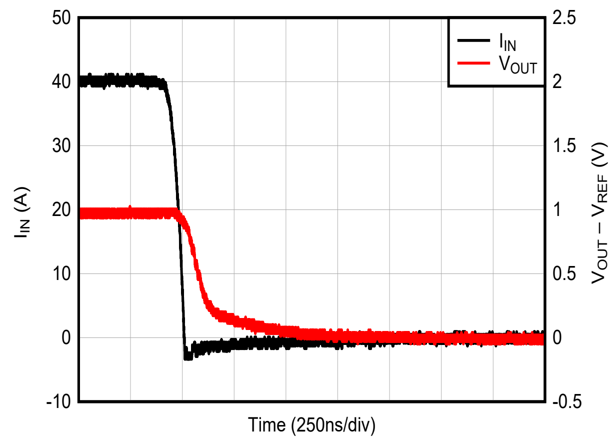


図 6-10. Voltage Output Step Response, Falling

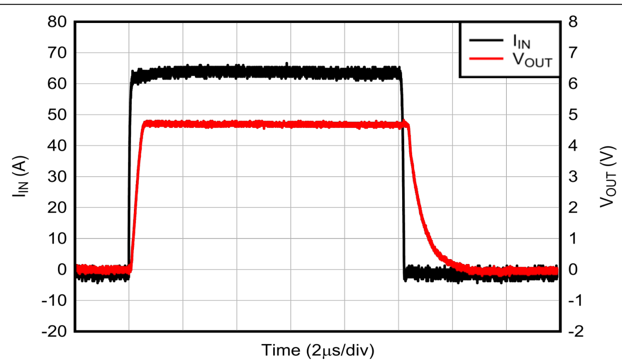


図 6-11. Current Overload Response

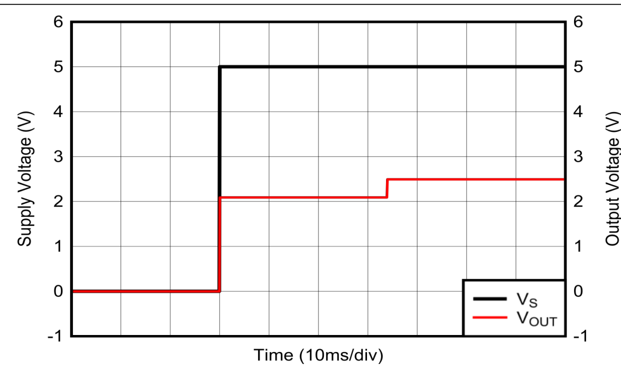


図 6-12. Startup Transient Response

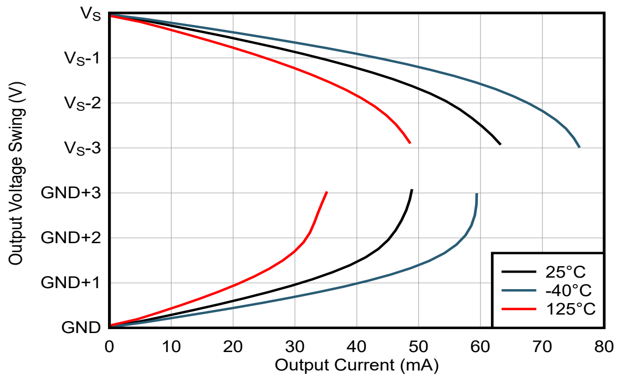


図 6-13. Output Swing vs Output Current

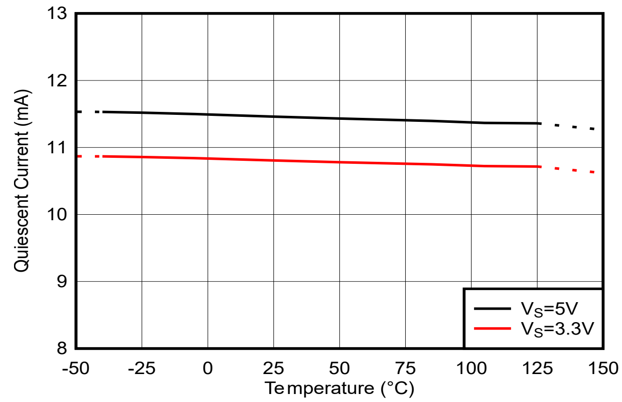


図 6-14. Quiescent Current vs Temperature

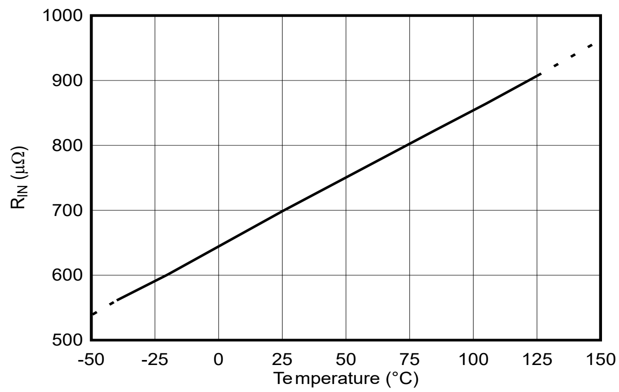


図 6-15. Input Conductor Resistance vs Temperature

7 Parameter Measurement Information

7.1 Accuracy Parameters

The ideal first-order transfer function of the TMCS1126-Q1 is given by 式 1, where the output voltage is a linear function of input current. The accuracy of the device is quantified both by the error terms in the transfer function parameters, as well as by nonidealities that introduce additional error terms not in the simplified linear model. See *Total Error Calculation Examples* for example calculations of total error, including all device error terms.

$$V_{OUT} = (I_{IN} \times S) + V_{REF} \tag{1}$$

where

- V_{OUT} is the analog output voltage.
- I_{IN} is the isolated input current.
- S is the sensitivity of the device.
- V_{REF} is the zero current reference output voltage for the device variant.

7.1.1 Sensitivity Error

Sensitivity is the proportional change in the sensor output voltage due to a change in the input conductor current. This sensitivity is the slope of the first-order transfer function of the sensor (see 図 7-1). The sensitivity of the TMCS1126-Q1 is tested and calibrated at the factory for high accuracy.

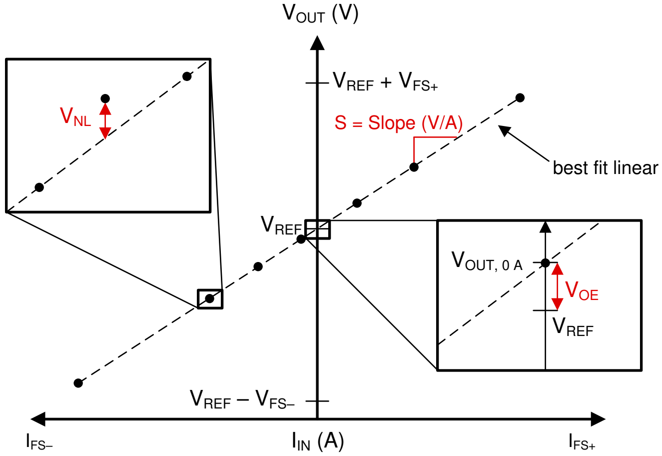


図 7-1. Sensitivity, Offset, and Nonlinearity Error

Sensitivity error e_S is the deviation from ideal sensitivity and is defined in 式 2 as the variation of the best-fit measured sensitivity from the ideal sensitivity.

$$e_S = \frac{(S_{fit} - S_{ideal})}{S_{ideal}} \tag{2}$$

where

- e_S is the sensitivity error.
- S_{fit} is the best fit sensitivity.
- S_{Ideal} is the ideal sensitivity.

Sensitivity thermal drift $S_{drift,therm}$ is the change in sensitivity with temperature and is reported in ppm/°C. To calculate sensitivity error at any given temperature T use 式 3 to multiply the sensitivity thermal drift by the change in temperature from 25°C and add that value to the sensitivity error at 25°C.

$$e_{S,\Delta T} = e_{S,25°C} + \left(S_{drift,therm} \times \Delta T\right) \tag{3}$$

where

- $S_{drift,therm}$ is the sensitivity drift over temperature in ppm/°C.
- ΔT is the change in device temperature from 25°C.

Sensitivity lifetime drift $S_{drift,life}$ is the change in sensitivity due to operational and environmental stresses over the entire lifetime of the device, and is reported as a worst-case percentage change in sensitivity over lifetime at 25°C.

7.1.2 Offset Error and Offset Error Drift

Offset error is the deviation from the ideal output with zero input current and most often limits measurement accuracy at low input current levels. Offset error can be referred to the output as offset voltage error or referred to the input as offset current error. When divided by device sensitivity, S, output voltage offset error V_{OE} is input referred as input current offset error I_{OS} (see 式 4). Offset error referred to the input (RTI) allows for more direct comparisons or offset error with input current. Regardless of whether offset error is referred to the input as current offset error I_{OS}, or to the output as voltage offset error V_{OE}, offset error is a single error source and must only be included once in either input-referred or output-referred error calculations.

$$I_{OS} = \frac{V_{OE}}{S} \quad (4)$$

As shown in 図 7-1, the output voltage offset error V_{OE} of the TMCS1126-Q1 is the difference between the zero current output voltage $V_{OUT,0A}$ and the zero current output reference voltage V_{REF} (see 式 5).

$$V_{OE} = V_{OUT,\,0A} - V_{REF} \quad (5)$$

The output offset error V_{OE} includes magnetic offset error in the Hall sensor and offset voltage error in the signal chain. The internal zero current output reference voltage is brought out to pin VREF so that errors in the internal reference voltage as well as errors introduced at the system level can be removed.

Offset drift is the change in the offset as a function of temperature T. Output offset drift is reported in μV/°C. To calculate offset error at any given temperature, multiply the offset drift by the change in temperature and add that value to the offset error at 25°C (see 式 6).

$$V_{OE,\,\Delta T} = V_{OE,\,25°C} + \left(V_{OE,\,drift} \times \Delta T\right) \quad (6)$$

where

- $V_{OE,drift}$ is the output voltage offset drift with temperature in μV/°C.
- ΔT is the change in device temperature from 25°C.

7.1.3 Nonlinearity Error

Nonlinearity is the deviation of the output voltage from a linear relationship to the input current. Nonlinearity voltage, as shown in 図 7-1, is the maximum voltage deviation from the best-fit line based on measured parameters (see 式 7).

$$V_{NL} = V_{OUT,\,meas} - \left[\left(I_{meas} \times S_{fit}\right) + V_{OUT,\,0A}\right] \quad (7)$$

where

- $V_{OUT,meas}$ is the voltage output at maximum deviation from best fit.
- I_{meas} is the input current at maximum deviation from best fit.
- S_{fit} is the best-fit sensitivity of the device.
- $V_{OUT,0A}$ is the device zero current output voltage.

Nonlinearity error for the TMCS1126-Q1 is specified as a percentage of the full-scale output range, V_{FS} (see 式 8).

$$e_{NL} = \frac{V_{NL}}{V_{FS}} \tag{8}$$

7.1.4 Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is the change in device offset due to variations in supply voltage. Use 式 9 to calculate input referred offset errors caused by supply variations on TMCS1126Axx-Q1 variants. Use 式 10 to calculate input referred offset errors caused by supply variations on TMCS1126Bxx-Q1 and TMCS1126Cxx-Q1 variants.

$$e_{PSRR,\,A} = PSRR \times (V_S - 5V) \tag{9}$$

$$e_{PSRR,\,B} = e_{PSRR,\,C} = PSRR \times (V_S - 3.3V) \tag{10}$$

where

- PSRR is the input referred power supply rejection ratio in mA/V.
- V_S is the operational supply voltage.

7.1.5 Common-Mode Rejection Ratio

Common-mode rejection ratio (CMRR) quantifies the effective input current error due to varying voltage on the isolated input of the device. Due to magnetic coupling and galvanic isolation of the current signal, the TMCS1126-Q1 has very high rejection of input common-mode voltage. Use 式 11 to calculate the error contribution from the input common-mode voltage V_{CM}.

$$e_{CMRR} = CMRR \times V_{CM} \tag{11}$$

where

- CMRR is the input-referred common-mode rejection in µA/V.
- V_{CM} is the operational AC or DC voltage on the input of the device.

7.1.6 External Magnetic Field Errors

The TMCS1126-Q1 suppresses interference from external magnetic fields generated by adjacent high-current carrying conductors, nearby motors, magnets, or any other sources of stray magnetic fields. Common-mode field rejection (CMFR) quantifies the effective input-referred error caused by stray magnetic fields. Use 式 12 to calculate error contributions from stray external magnetic fields B_{EXT}.

$$e_{Bext} = B_{EXT} \times CMFR \tag{12}$$

where

- B_{EXT} is the intensity of the external magnetic field in mT.
- CMRF is the common-mode field rejection in mA/mT.

7.2 Transient Response Parameters

Critical TMCS1126-Q1 transient step response parameters are shown in 図 7-2. Propagation delay, t_{pd}, is the time period between the input current waveform reaching 10% of the final value and the output voltage, V_{OUT}, reaching 10% of the final value. Response time, t_r, is the time period between the input current reaching 90% of the final value and the output voltage reaching 90% of the final value, for an input current step sufficient to cause a 1V change in the output voltage. Slew rate, SR, is defined as the rate of change between the output voltage reaching 10% and 90% of the final value during the sufficiently fast input current step.

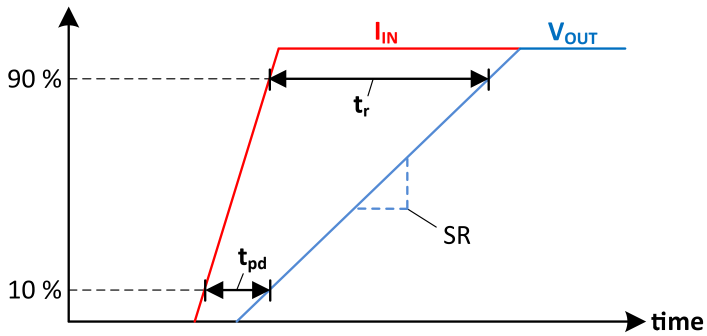


図 7-2. Transient Step Response

7.2.1 CMTI, Common-Mode Transient Immunity

CMTI is the capability of the device to tolerate a rising or falling voltage step on the input without coupling significant disturbance on the output signal. The device is specified for the maximum common-mode transition rate when the output signal does not experience a disturbance greater than 200mV lasting longer than 1µs, as shown in 図 7-3 with a 150kV/µs common-mode input step. Higher edge rates than the specified CMTI can be supported with sufficient filtering or blanking time after common-mode transitions.

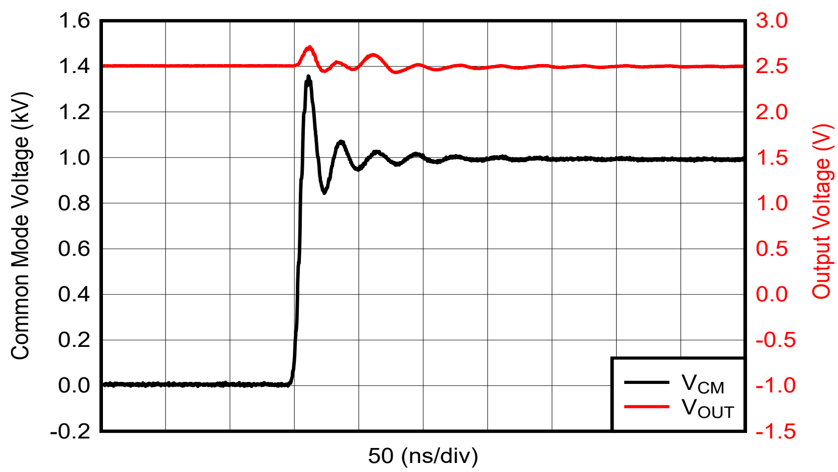


図 7-3. Common-Mode Transient Response

7.3 Safe Operating Area

The isolated input current safe operating area (SOA) of the TMCS1126-Q1 is constrained by self-heating due to power dissipation in the input conductor. Depending upon the use case, the SOA is constrained by multiple conditions, including exceeding maximum junction temperature, Joule heating in the leadframe, or leadframe fusing under extremely high currents. These mechanisms depend greatly on input current amplitude and duration, along with ambient thermal conditions.

Current SOA strongly depends on the thermal environment and design of the system-level printed circuit board (PCB). Multiple thermal variables control the transfer of heat from the device to the surrounding environment, including air flow, ambient temperature, and PCB construction and design. All ratings are for a single TMCS1126-Q1 device mounted on the *TMCS1126xEVM* , or equivalent PCB design with no air flow under specified ambient temperature conditions. Device use profiles must satisfy continuous current conduction SOA capabilities for the thermal environment planned for system operation.

7.3.1 Continuous DC or Sinusoidal AC Current

The longest thermal time constants of device packaging and PCBs are in the order of seconds; therefore, any continuous DC or sinusoidal AC periodic waveform with a frequency higher than 1Hz can be evaluated based on the RMS continuous-current levels. The continuous-current capability has a strong dependence upon the operating ambient temperature range expected in operation. 図 7-4 shows the maximum continuous current-handling capability of the device when mounted on the *TMCS1126xEVM* . Current capability falls off at higher ambient temperatures because of the reduced thermal transfer from junction-to-ambient and increased power dissipation in the leadframe. By improving the thermal design of an application, the SOA can be extended to higher currents at elevated temperatures. Using larger and heavier copper power planes, providing air flow over the board, or adding heat sinking structures to the area of the device can all improve thermal performance.

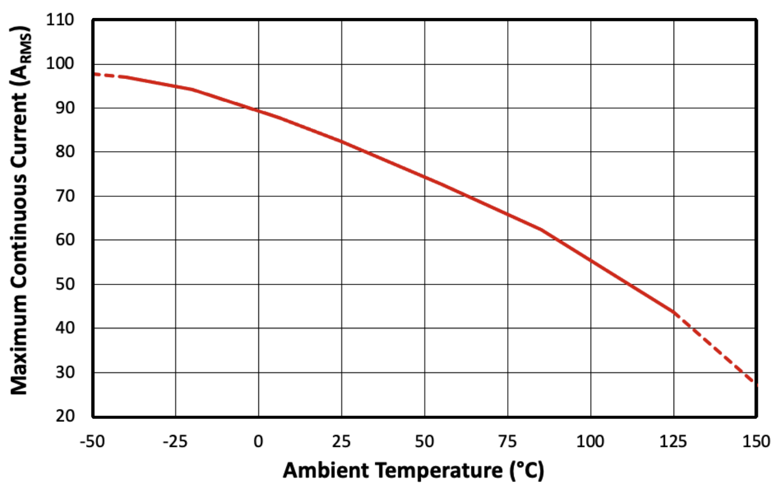


図 7-4. Maximum Continuous RMS Current vs Ambient Temperature

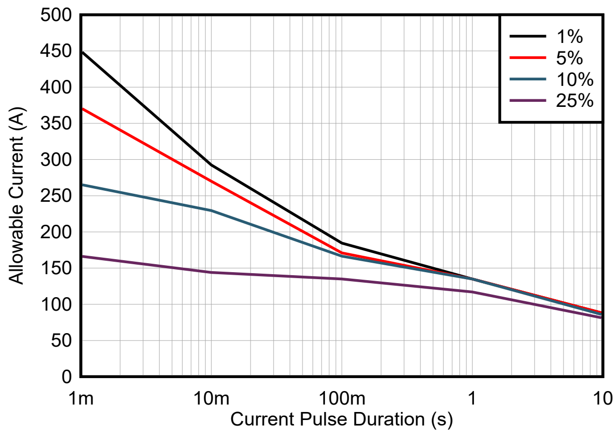
7.3.2 Repetitive Pulsed Current SOA

For applications where current is pulsed between a high current and no current, the allowable capabilities are limited by short-duration heating in the leadframe. The TMCS1126-Q1 can tolerate higher current ranges under some conditions, however, for repetitive pulsed events, the current levels must satisfy both the pulsed current SOA and the RMS continuous current constraint. Pulse duration, duty cycle, and ambient temperature all impact the SOA for repetitive pulsed events. 図 7-5, 図 7-6, 図 7-7, and 図 7-8 illustrate repetitive stress levels based on test results from the *TMCS1126xEVM* under which parametric performance and isolation integrity was not impacted post-stress for multiple ambient temperatures. At high duty cycles or long pulse durations, this limit approaches the continuous current SOA for a RMS value defined by 式 13.

$$I_{IN,\ RMS} = I_{IN,\ P} \times \sqrt{D} \quad (13)$$

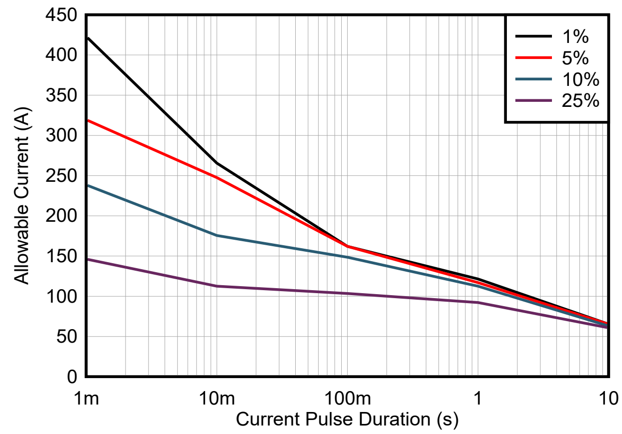
where

- $I_{IN,RMS}$ is the RMS input current level
- $I_{IN,P}$ is the pulse peak input current
- D is the pulse duty cycle



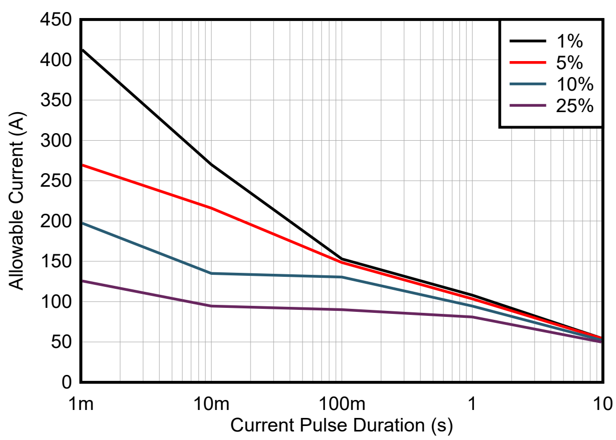
T_A = 25°C

図 7-5. Maximum Repetitive Pulsed Current vs. Pulse Duration



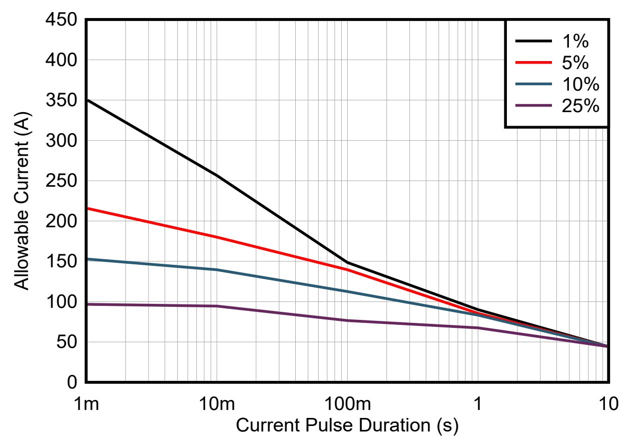
T_A = 85°C

図 7-6. Maximum Repetitive Pulsed Current vs. Pulse Duration



T_A = 105°C

図 7-7. Maximum Repetitive Pulsed Current vs. Pulse Duration



T_A = 125°C

図 7-8. Maximum Repetitive Pulsed Current vs. Pulse Duration

7.3.3 Single Event Current Capability

Single higher-current events that are shorter duration can be tolerated by the TMCS1126-Q1 , because the junction temperature does not reach thermal equilibrium within the pulse duration. 図 7-9 shows the short-circuit duration curve for the device for single current-pulse events, where the leadframe resistance changes after stress. This level is reached before a leadframe fusing event, but must be considered an upper limit for short duration SOA. For long-duration pulses, the current capability approaches the continuous RMS limit at the given ambient temperature.

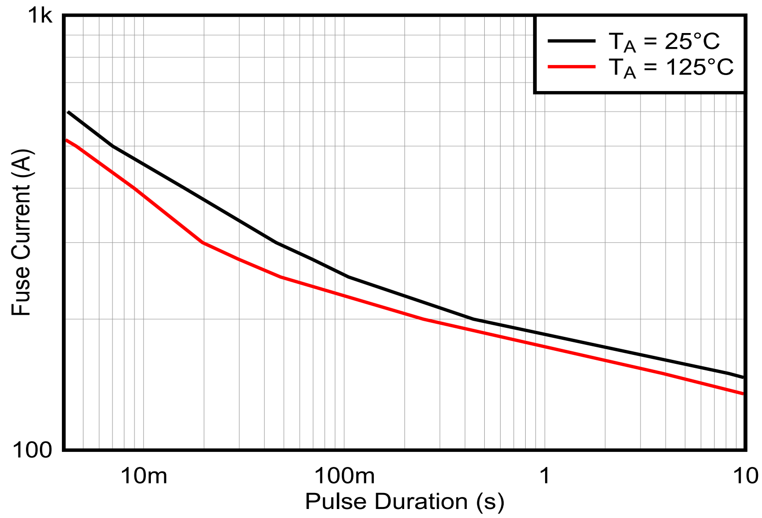


図 7-9. Single-Pulse Leadframe Capability

8 Detailed Description

8.1 Overview

The TMCS1126-Q1 is a precision Hall-effect current sensor, providing high levels of reliable reinforced isolation working voltage, ambient field rejection and high current carrying capability. A maximum total lifetime error of less than 1.4% can be achieved with no system level calibration, or less than 1% maximum total error can be achieved with a one-time room temperature calibration (including both temperature and lifetime drift). Numerous device options are provided for both unidirectional and bidirectional current measurements. The input current flows through a conductor between the isolated input current pins. The conductor has a 0.7mΩ resistance at room temperature and accommodates up to $44A_{RMS}$ of continuous current at 125°C ambient temperature when used with printed circuit boards of comparable thermal design, such as the *TMCS1126xEVM* . The low-ohmic leadframe path reduces power dissipation compared to alternative current measurement methodologies, and does not require any external passive components, isolated supplies, or control signals on the high-voltage side. The magnetic field generated by the input current is sensed by a Hall sensor and amplified by a precision signal chain. The device can be used for both AC and DC current measurements and has a bandwidth of 500kHz. There are multiple fixed-sensitivity device options to choose from, providing a wide variety of bidirectional linear current sensing ranges from ±10A to ±103A, as well as unidirectional linear current sensing ranges from 19A to 183A. The TMCS1126-Q1 can operate with a low voltage supply ranging from 3V to 5.5V, and is optimized for high accuracy and temperature stability, with both offset and sensitivity compensated across the entire operating temperature range.

8.2 Functional Block Diagram

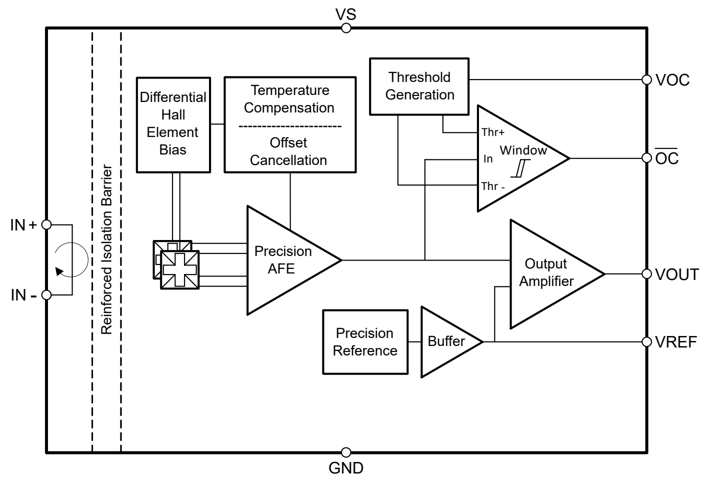


図 8-1. Function Block Diagram

8.3 Feature Description

8.3.1 Current Input

Input current to the TMCS1126-Q1 passes through the isolated high-voltage side of the package leadframe into and out of the IN+ and IN– pins. The current flowing through the package generates a magnetic field that is proportional to the input current, which is measured by an integrated on-chip galvanically-isolated, precision Hall sensor. As a result of the electrostatic shielding on the Hall sensor die, only the magnetic field generated by the input current is measured, thus limiting input voltage switching pass-through to the circuitry. This configuration allows for direct measurement of currents with high-voltage transients without signal distortion on the current-sensor output. The leadframe conductor has a low resistance and a positive temperature coefficient as defined in *Electrical Characteristics*.

8.3.2 Ambient Field Rejection

The TMCS1126-Q1 is designed to provide high levels of current measurement accuracy in harsh environments. Immunity to interference from stray magnetic fields allows for use in close proximity to high current carrying traces, motor windings, inductors, or any other erroneous source of stray magnetic fields. The TMCS1126-Q1 incorporates differential Hall sensors that are strategically located and configured to reject interference from stray external magnetic fields. Ambient Field Rejection (AFR) limited only by Hall element matching and package leadframe coupling reduces errors from stray magnetic fields.

8.3.3 High-Precision Signal Chain

The TMCS1126-Q1 uses a precision, low-drift signal chain with proprietary sensor linearization techniques to provide a highly accurate and stable current measurement across the full temperature range and lifetime of the device. The device is fully tested and calibrated at the factory to account for any variations in either silicon processing, assembly, or packaging of the device. The full signal chain provides a fixed sensitivity voltage output that is proportional to the current flowing through the leadframe of the isolated input.

8.3.3.1 Temperature Stability

The TMCS1126-Q1 includes a proprietary temperature compensation technique which results in significantly improved parametric drift across the full temperature range. This compensation technique accounts for changes in ambient temperature, self-heating, and package stress. A zero-drift signal chain architecture along with Hall sensor temperature compensation methods enable stable sensitivity while minimizing offset errors across temperature. System-level performance is drastically improved across required operating conditions.

8.3.3.2 Lifetime and Environmental Stability

In addition to large thermal drift, typical magnetic current sensors suffer an additional 2% to 3% drift in sensitivity due to aging over the lifetime of the device. The same proprietary compensation techniques used in the TMCS1126-Q1 to reduce temperature drift are also used to greatly reduce lifetime drift due to aging from stress and environmental conditions especially at high operating temperatures. As shown in the *Electrical Characteristics*, the TMCS1126-Q1 has industry leading lifetime sensitivity drift realized after Highly Accelerated Stress Tests (HAST) at 130°C and 85% relative humidity (RH) during standard three lot AEC-Q100 qualifications. Low sensitivity and offset drift within the bounds specified in the *Electrical Characteristics* are also observed after 1000 hour, 125°C high temperature operating life stress tests are performed as prescribed by AEC-Q100 qualifications. These tests mimic typical device lifetime operation, and show device performance variation due to aging is vastly improved compared with typical magnetic current sensors. 図 8-2 and 図 8-3 show the sensitivity and offset drift after a 1000 hour, 125°C high temperature operating life stress test as specified by AEC-Q100. Device operational performance varies over the lifetime of the device. This test mimics typical device lifetime operations and shows the likelihood of the device vastly improving performance compared to typical magnetic sensors.

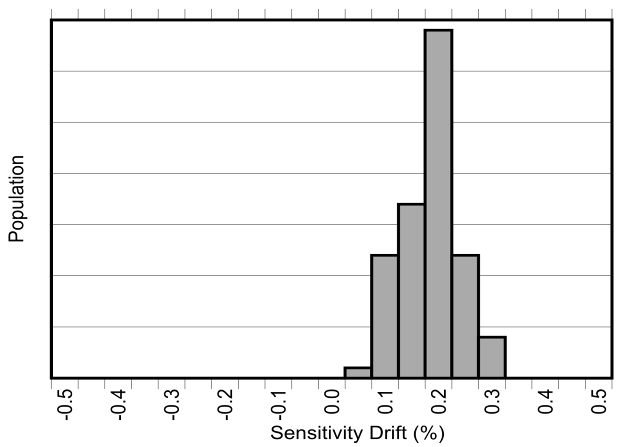


図 8-2. Sensitivity Error Drift After AEC-Q100 High Temperature Operating Life Stress Test

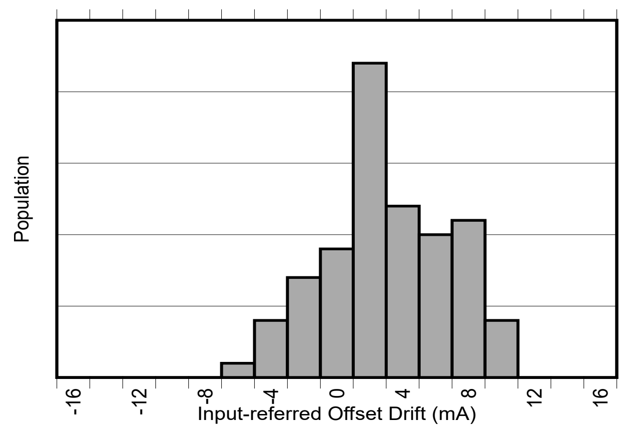


図 8-3. Input-Referred Offset Drift After AEC-Q100 High Temperature Operating Life Stress Test

8.3.4 Internal Reference Voltage

The TMCS1126-Q1 has a precision internal reference that determines the zero current output voltage, $V_{OUT,0A}$. Overall current sensing dynamic range can be optimized by choosing either of the three different zero current output voltage options listed in the *Device Comparison* table. These extremely low-drift precision zero current reference options are listed in 式 14, 式 15, and 式 16. These equations are for precise bidirectional or unidirectional current measurements using various supply voltages ranging between 3.0V to 5.5V.

$$\text{TMCS1126Axx-Q1} \rightarrow V_{OUT,0A} = V_{REF} = 2.5V \quad (14)$$

$$\text{TMCS1126Bxx-Q1} \rightarrow V_{OUT,0A} = V_{REF} = 1.65V \quad (15)$$

$$\text{TMCS1126Cxx-Q1} \rightarrow V_{OUT,0A} = V_{REF} = 0.33V \quad (16)$$

8.3.5 Current-Sensing Measurable Ranges

The zero current reference voltage, V_{REF}, along with device sensitivity, S, and supply voltage, V_S, determine the TMCS1126-Q1 linear input current measurement ranges listed in the *Device Comparison* table. The maximum linear output voltage, $V_{OUT,max}$, is limited to 100mV less than the supply voltage as shown in 式 17. The minimum linear output voltage, $V_{OUT,min}$, is limited to 100mV above ground as shown in 式 18.

$$V_{OUT,\,max} = V_S - 100mV \tag{17}$$

$$V_{OUT,\,min} = 100mV \tag{18}$$

Overall maximum dynamic range can be optimized with proper device selection by referring minimum and maximum linear output voltage swing to minimum and maximum linear input current range by dividing output voltage by sensitivity, S (see 式 19 and 式 20).

$$I_{IN,\ max+} = \frac{\left(V_{OUT,\,max} - V_{OUT,\,0A}\right)}{S} \tag{19}$$

$$I_{IN,\ max-} = \frac{\left(V_{OUT,\,0A} - V_{OUT,\,min}\right)}{S} \tag{20}$$

where

- $I_{IN,max+}$ is the maximum linear measurable positive input current.
- $I_{IN,max–}$ is the maximum linear measurable negative input current.
- S is the sensitivity of the device variant.
- $V_{OUT,0A}$ is the appropriate zero current output voltage.

As examples for determining linear input current measurement range, consider TMCS1126A2A-Q1, TMCS1126B2A-Q1 and TMCS1126C2A-Q1 devices, all with 50mV/A sensitivity as shown in the *Device Comparison* table. When used with a 5V supply, the TMCS1126A2A-Q1 has a balanced ±48A bidirectional linear current measurement range about the 2.5V zero current output reference voltage, V_{REF}, as shown in 図 8-4. When used with a 3.3V supply, the TMCS1126B2A-Q1 has a balanced ±31A bidirectional linear current measurement range about the 1.65V zero current output reference voltage. If used with a 5V supply, the linear current measurement range of the TMCS1126B2A-Q1 can be extended from –31A to 65A as shown in 図 8-4. The TMCS1126C2A-Q1 with a 0.33V zero current reference voltage is intended for measuring unidirectional currents. When used with a 3.3V supply the TMCS1126C2A-Q1 has a unidirectional linear current measurement range from –5A to 57A which can be extended from –5A to 91.4A when used with a 5V supply.

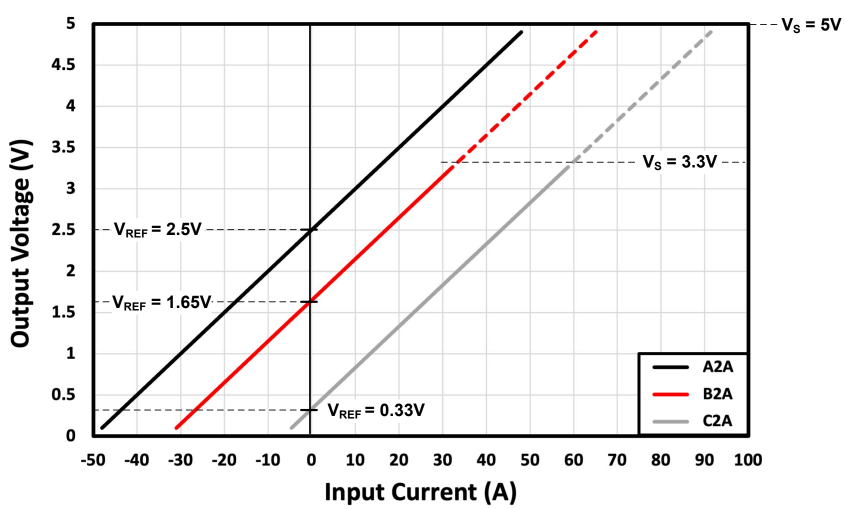


図 8-4. Output Voltage Relationship to Input Current for TMCS1126x2A-Q1

8.3.6 Overcurrent Detection

In addition to the precision analog signal, the TMCS1126-Q1 also offers a fast digital overcurrent detection response. The Overcurrent Detection (OCD) circuit provides an open-drain comparator output that can be used to trigger a warning or initiate a system shutdown to prevent damage from excessive current flow caused by short circuits, motor stalls, or other unintended system conditions. This fast digital response can be configured on both bidirectional and unidirectional devices to assert based on a signal that is anywhere from half to over twice the full-scale analog measurement range.

Use of this fast digital output $\overline{OC}$ instead of the precision analog output VOUT to detect overcurrent events outside the nominal operating current range allows for higher dynamic range with higher sensitivity optimized for the nominal operating current range. Use of this fast digital output $\overline{OC}$ also allows for lower overall signal noise from lower analog signal bandwidth than often needed when using the analog signal chain to detect fast overcurrent events.

8.3.6.1 Setting The User Configurable Overcurrent Threshold

The desired overcurrent threshold, I_{OC}, is set by applying an external voltage, V_{OC}, to the VOC pin according to 式 21.

$$V_{OC} = \frac{S \times I_{OC}}{2.5} \quad (21)$$

where

- S is the device sensitivity in mV/A.
- I_{OC} is the desired overcurrent threshold.
- V_{OC} is the voltage applied that sets the overcurrent threshold.

An example of how to set the desired overcurrent threshold, I_{OC}, is shown in セクション 8.3.6.1.3. Regardless of which TMCS1126-Q1 sensitivity variant is chosen or which zero current output voltage option is selected, 式 21 applies when calculating overcurrent thrshold voltage V_{OC}. A digital-to-analog converter (DAC) can be used to set the desired overcurrent threshold I_{OC}, or a simple external resistor divider circuit can be used as shown in セクション 8.3.6.1.1 or セクション 8.3.6.1.2.

8.3.6.1.1 Setting Overcurrent Threshold Using Power Supply Voltage

A simple external resistor divider driven from the power supply as shown in 図 8-5 can be used to generate the external overcurent voltage V_{OC} applied to the VOC pin to set the desired overcurrent threshold I_{OC} according to 式 21.

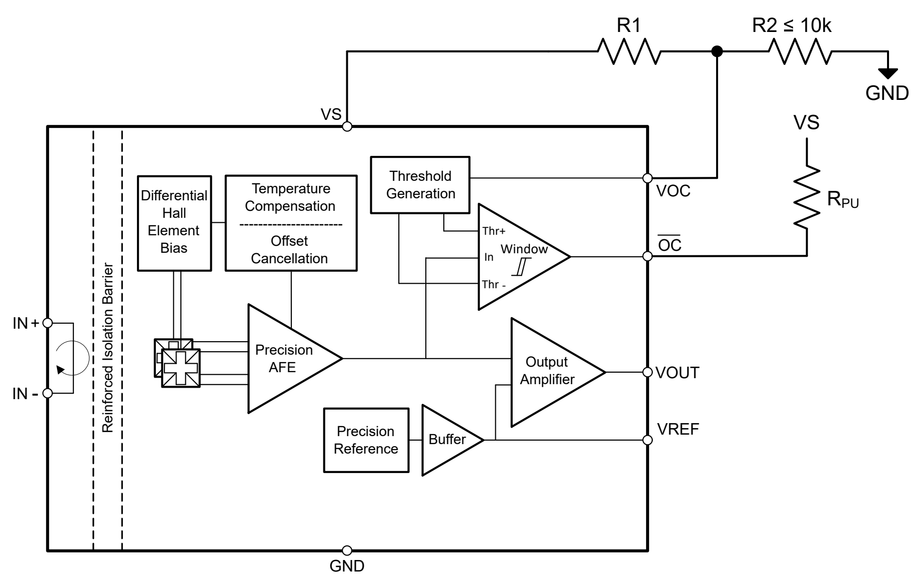


図 8-5. User Configurable Overcurrent Threshold Using Power Supply Voltage

When using a resistor divider as shown in 図 8-5, R2 must be less than 10kΩ to mitigate the impact of the VOC input impedance on overcurrent threshold accuracy.

8.3.6.1.2 Setting Overcurrent Threshold Using Internal Reference Voltage

Higher overcurrent threshold accuracy can be achieved by using the zero current output reference voltage VREF as shown in 図 8-6 to generate the external overcurrent voltage V_{OC} required to set the desired overcurrent threshold I_{OC} according to 式 21.

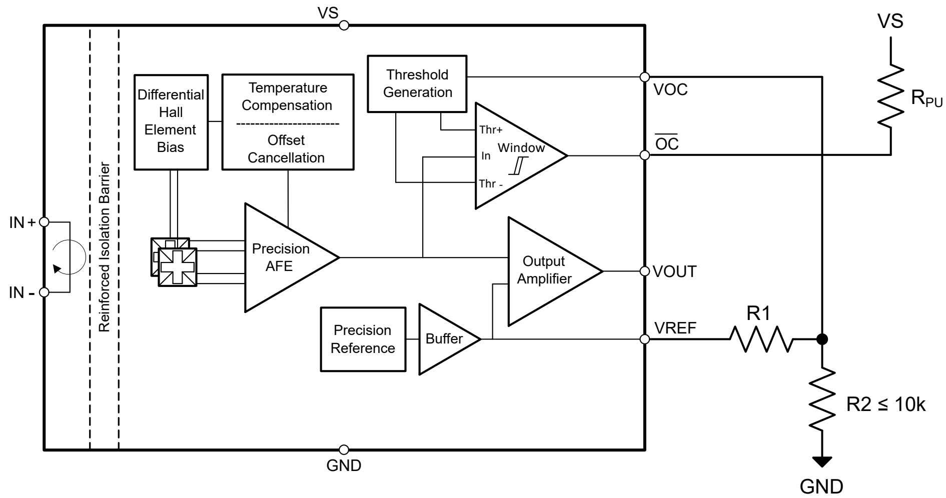


図 8-6. User Configurable Overcurrent Threshold Using Zero Current Output Reference Voltage

When using a resistor divider as shown in 図 8-6, R2 must be less than 10kΩ to mitigate the impact of the VOC input impedance on overcurrent threshold accuracy.

8.3.6.1.3 Setting Overcurrent Threshold Example

For example, to set a desired overcurrent threshold to I_{OC} = ±50A on bidirectional TMCS1126A3A-Q1 or TMCS1126B3A-Q1 devices with ±32A linear measurement range, as well as on the unidirectional TMCS1126C3A-Q1 device, size the resistors R1 and R2 to apply a voltage V_{OC} = 1.5V to the VOC pin according to 式 21.

with

- TMCS1126A3A-Q1, TMCS1126B3A-Q1 and TMCS1126B3A-Q1 device sensitivity, S = 75mV/A.
- Desired overcurrent threshold, I_{OC} = ±50A.
- Applied overcurrent threshold voltage V_{OC} = 1.5V.

8.3.6.2 Overcurrent Output Response

図 8-7 shows the active-low overcurrent digital output $\overline{OC}$ response to bidirectional overcurrent events. When the input current exceeds $|\pm I_{OC}|$ on a bidirectional device, the fast $\overline{OC}$ pin is pulled low. The input current must return to within $\pm I_{OC}$ by more than a hysteresis current I_{Hys} before the $\overline{OC}$ pin resets back to the normal high-state.

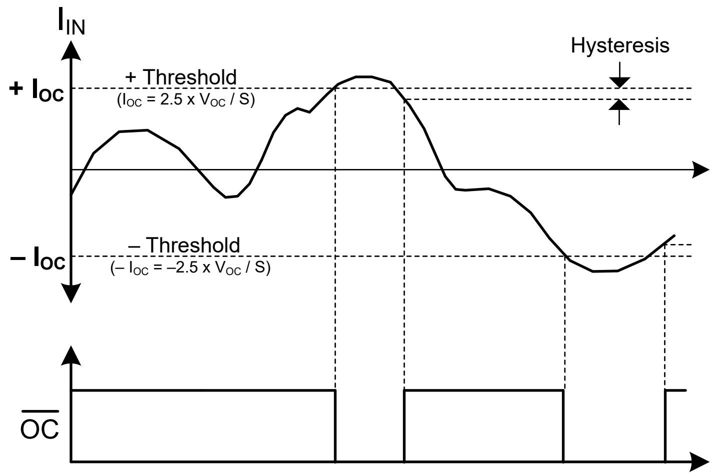


図 8-7. Overcurrent Output Response

8.4 Device Functional Modes

8.4.1 Power-Down Behavior

As a result of the inherent galvanic isolation of the device, very little consideration must be paid to powering down the device, as long as the limits in the *Absolute Maximum Ratings* table are not exceeded on any pins. The isolated current input and the low-voltage signal chain can be decoupled in operational behavior, as either can be energized with the other shutdown, as long as the isolation barrier capabilities are not exceeded. The low-voltage power supply can be powered down while the isolated input is still connected to an active high-voltage signal or system.

9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The key feature sets of the TMCS1126-Q1 provide significant advantages in any application where an isolated current measurement is required.

- Galvanic isolation provides a high isolated working voltage and excellent immunity to input voltage transients.
- Hall-based measurement simplifies system level designs without the need for a power supply on the high-voltage (HV) side.
- An input current path through the low impedance conductor minimizes power dissipation.
- Excellent accuracy and low temperature drift eliminate the need for multipoint calibrations without sacrificing system performance.
- A wide operating supply range enables a single device to function across a wide range of voltage levels.

These advantages increase system-level performance while minimizing complexity for any application where precision current measurements must be made on isolated currents. Specific examples and design requirements are detailed in the following section.

9.1.1 Total Error Calculation Examples

Users can calculate the total error for any arbitrary device condition and current level. Consider error sources like input-referred offset current (I_{OS}), Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio

(PSRR), sensitivity error, nonlinearity, as well as errors caused by any external magnetic fields (B_{EXT}). Compare each of these error sources in percentage terms, as some are significant drivers of error and some have inconsequential impact to current measurement error. Offset (式 22), CMRR (式 23), PSRR (式 24), and external magnetic field error (式 25) are all referred to the input, and so are divided by the actual input current I_{IN} to calculate percentage errors. For sensitivity error and nonlinearity error calculations, the percentage limits explicitly specified in the *Electrical Characteristics* table can be used.

$$e_{Ios} = \frac{I_{OS}}{I_{IN}} \times 100\% = \frac{V_{OE}}{S \times I_{IN}} \times 100\% \tag{22}$$

$$e_{CMRR} = \frac{CMRR \times V_{CM}}{I_{IN}} \times 100\% \tag{23}$$

$$e_{PSRR,\ A} = \frac{PSRR \times (V_S - 5V)}{I_{IN}} \times 100\%\ ;\ e_{PSRR,\ B} = e_{PSRR,\ C} = \frac{PSRR \times (V_S - 3.3V)}{I_{IN}} \times 100\% \tag{24}$$

$$e_{Bext} = \frac{B_{EXT} \times CMFR}{I_{IN}} \times 100\% \tag{25}$$

where

- V_{OE} is the output-referred offset voltage error.
- V_{CM} is the input common-mode voltage.
- $e_{PSRR,A}$ is the power supply rejection error for TMCS1126Axx-Q1 devices.
- $e_{PSRR,B}$ is the power supply rejection error for TMCS1126Bxx-Q1 devices.
- $e_{PSRR,C}$ is the power supply rejection error for TMCS1126Cxx-Q1 devices.
- V_S is the supply voltage.
- CMFR is the common-mode magnetic field rejection.

When calculating error contributions across temperature, only offset error and sensitivity error contributions vary significantly. To determine the offset error across temperature, use 式 26 to calculate total input-referred offset error current, I_{OS}, at any ambient temperature, T_A.

$$e_{Ios,\Delta T} = \frac{V_{OE,\ 25°C} + \left(V_{OE,\ drift} \times |\Delta T|\right)}{S \times I_{IN}} \times 100\% \tag{26}$$

where

- $V_{OE,25°C}$ is the output-referred offset error at 25°C.
- $V_{OE,drift}$ is the output-referred offset drift with temperature in μV/°C.
- ΔT is the change in temperature from 25°C.
- S is the sensitivity of the device variant.

Sensitivity error at 25°C is specified as $e_{S,25°C}$ in the *Electrical Characteristics* table along with sensitivity variation over temperature as sensitivity thermal drift $S_{drift,therm}$ in ppm/°C. To determine the sensitivity error across temperature, use 式 27 to calculate sensitivity error at any ambient temperature, T_A, over the given application operating ambient temperature range between –40°C and 125°C.

$$e_{S,\Delta T} = e_{S,\ 25°C} + \left(S_{drift,\ therm} \times |\Delta T| \times 100\%\right) \tag{27}$$

To accurately calculate the total expected error of the device, the contributions from each of the individual components above must be understood in reference to operating conditions. To account for the individual error sources that are statistically uncorrelated, use a root sum square (RSS) error calculation to calculate total error. For the TMCS1126-Q1 , only the input-referred offset current (I_{OS}), CMRR, and PSRR are statistically correlated. These error terms are lumped in an RSS calculation to reflect this nature, as shown in 式 28 for room temperature and in 式 29 across a given temperature range. The same methodology can be applied for calculating typical total error by using the appropriate error term specification.

$$e_{RSS} = \sqrt{\left(e_{Ios}+e_{PSRR}+e_{CMRR}\right)^2 + \left(e_{Bext}\right)^2 + \left(e_S\right)^2 + \left(e_{NL}\right)^2} \quad (28)$$

$$e_{RSS,\Delta T} = \sqrt{\left(e_{Ios,\Delta T}+e_{PSRR}+e_{CMRR}\right)^2 + \left(e_{Bext}\right)^2 + \left(e_{S,\Delta T}\right)^2 + \left(e_{NL}\right)^2} \quad (29)$$

The total error calculation has a strong dependence on the actual input current, therefore always calculate total error across the dynamic range that is required. These curves asymptotically approach the sensitivity and nonlinearity error at high current levels, and approach infinity at low current levels due to offset error terms with input current in the denominator. Key figures of merit for any current-measurement system include the total error percentage at full-scale current, as well as the dynamic range of input current over which the error remains below some key level. 図 9-1 shows the RSS maximum total error as a function of input current for a TMCS1126A2A-Q1 at room temperature and across the full temperature range with a 5.25V supply.

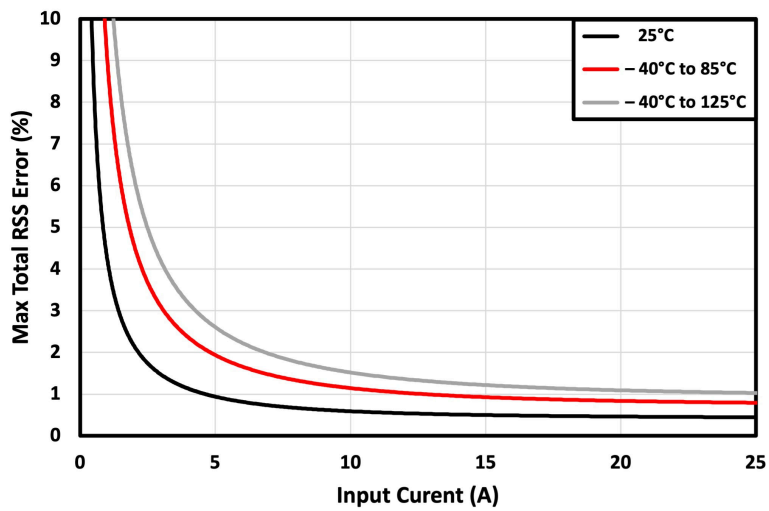

図 9-1. RSS Error vs Input Current

9.1.1.1 Room-Temperature Error Calculations

For room-temperature total error calculations, specifications across temperature and drift are ignored. As an example, consider a TMCS1126B2A-Q1 with a supply voltage (V_S) of 3.1V and a worst-case common-mode excursion of 600V to calculate operating-point-specific parameters. Consider a measurement error due to an external 400µT magnetic field generated by a $20A_{DC}$ current flowing through an adjacent trace or conductor that is 10mm away. The full-scale current range of the device in specified conditions is slightly greater than ±31A, as shown in the *Device Comparison* table. In this case, the calculating error at both 25A and 12.5A highlights error dependencies on the input-current level. 表 9-1 shows the individual error components and RSS maximum total error calculations at room temperature under the conditions specified. Relative to other errors, the additional errors from CMRR, external ambient magnetic fields B_{EXT} and nonlinearity are negligible, and can typically be excluded from total error calculations.

表 9-1. Total Error Calculation: Room Temperature Example

ERROR COMPONENT	SYMBOL	EQUATION	ERROR AT I_{IN} = 25A	ERROR AT I_{IN} = 12.5A
Input offset error	e_{Ios}	$e_{Ios} = \frac{I_{OS}}{I_{IN}} \times 100\% = \frac{V_{OE}}{S \times I_{IN}} \times 100\% = \frac{\pm 1.5mV}{50mV/A \times I_{IN}} \times 100\%$	±0.12%	±0.24%
PSRR error	e_{PSRR}	$e_{PSRR} = \frac{PSRR \times (V_S - 3.3)}{I_{IN}} \times 100\%$	±0.04%	±0.07%
CMRR error	e_{CMRR}	$e_{CMRR} = \frac{CMRR \times V_{CM}}{I_{IN}} \times 100\%$	±0.01%	±0.02%

表 9-1. Total Error Calculation: Room Temperature Example (続き)

ERROR COMPONENT	SYMBOL	EQUATION	ERROR AT I_{IN} = 25A	ERROR AT I_{IN} = 12.5A
External Field error	e_{Bext}	$e_{Bext} = \frac{B_{EXT} \times CMFR}{I_{IN}} \times 100\%$	±0.02%	±0.03%
Sensitivity error	e_S	Specified in *Electrical Characteristics*	±0.4%	±0.4%
Nonlinearity error	e_{NL}	Specified in *Electrical Characteristics*	±0.1%	±0.1%
RSS total error	e_{RSS}	$e_{RSS} = \sqrt{(e_{Ios}+e_{PSRR}+e_{CMRR})^2 + (e_{Bext})^2 + (e_S)^2 + (e_{NL})^2}$	0.45%	0.53%

9.1.1.2 Full-Temperature Range Error Calculations

To calculate total error across any specific temperature range, use 式 28 and 式 29 for RSS maximum total errors, similar to the example for room temperatures. Conditions from the example in *Room-Temperature Error Calculations* are replaced with the respective equations and error components for a –40°C to 85°C temperature range below in 表 9-2.

表 9-2. Total Error Calculation: –40°C to 85°C Example

ERROR COMPONENT	SYMBOL	EQUATION	ERROR AT I_{IN} = 25A	ERROR AT I_{IN} = 12.5A
Input offset error	$e_{Ios,\Delta T}$	$e_{Ios,\Delta T} = \frac{V_{OE,25°C} + (V_{OE,drift} \times \lvert\Delta T\rvert)}{S \times I_{IN}} \times 100\%$	±0.31%	±0.62%
PSRR error	e_{PSRR}	$e_{PSRR} = \frac{PSRR \times (V_S - 3.3)}{I_{IN}} \times 100\%$	±0.04%	±0.07%
CMRR error	e_{CMRR}	$e_{CMRR} = \frac{CMRR \times V_{CM}}{I_{IN}} \times 100\%$	±0.01%	±0.02%
External Field error	e_{Bext}	$e_{Bext} = \frac{B_{EXT} \times CMFR}{I_{IN}} \times 100\%$	±0.02%	±0.03%
Sensitivity error	$e_{S,\Delta T}$	$e_{S,\Delta T} = e_{S,25°C} + (S_{drift,therm} \times \lvert\Delta T\rvert \times 100\%)$	±0.70%	±0.70%
Nonlinearity error	e_{NL}	Specified in *Electrical Characteristics*	±0.1%	±0.1%
RSS total error	$e_{RSS,\Delta T}$	$e_{RSS,\Delta T} = \sqrt{(e_{Ios,\Delta T}+e_{PSRR}+e_{CMRR})^2+(e_{Bext})^2+(e_{S,\Delta T})^2+(e_{NL})^2}$	0.79%	1.01%

9.2 Typical Application

In many applications, power must be converted from AC sources for use in DC circuitry. Some type of controlled power factor correction (PFC) stage is usually needed to improve power transfer efficiency. Faster and faster power switches are being used in modern PFC stages to reduce overall size and to improve power transfer efficiency. Often, the PFC stage of AC to DC converters is connected directly to AC power grids. A primary challenge to sensing in PFC stages is that the current sensor is subjected to large voltage spikes coming from the high-voltage (HV) power grid along with large transients coming from high speed power switches during charge transfer. Inherent isolation in the TMCS1126-Q1 construction helps overcome these challenges by providing high levels of isolation between the HV current sensing nodes and low-voltage control circuitry, with high common-mode transient immunity (CMTI). 図 9-2 shows the use of the TMCS1126-Q1 measuring phase currents in a common AC to DC converter stage.

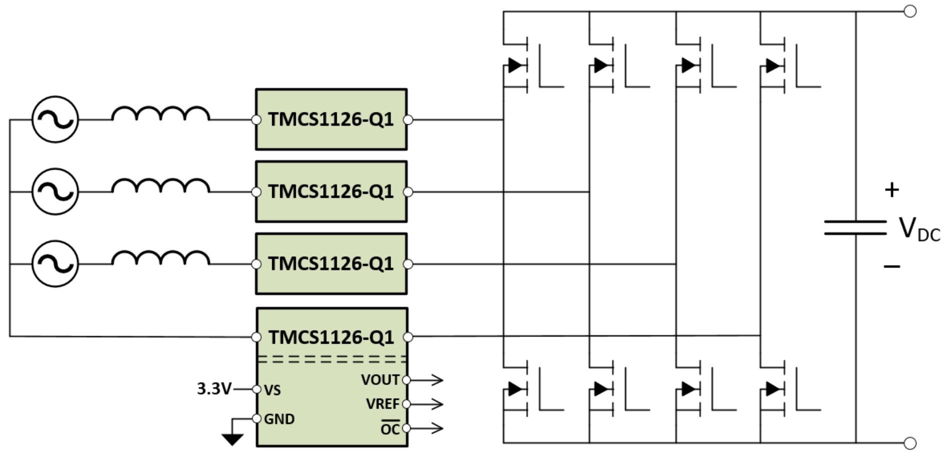

図 9-2. AC to DC Converter Current Sensing

9.2.1 Design Requirements

For a 3-phase current sensing application, make sure to provide linear sensing across the expected current range, and make sure that the device remains within working thermal constraints. A single TMCS1126-Q1 can be used to measure current in each phase if necessary. For this example, consider a nominal supply of 5V but a minimum of 4.9V to include for some supply variation. Maximum output swings are defined according to TMCS1126-Q1 specifications, and a full-scale current measurement of ±20A is required.

表 9-3. Example Application Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
$V_{S,nom}$	5V
$V_{S,min}$	4.9V
$I_{IN,FS}$	±20A

9.2.2 Detailed Design Procedure

The primary design parameter for using the TMCS1126-Q1 is the optimum sensitivity variant based on the required measured current levels and the selected supply voltage. Positive and negative currents are measured in this in-line phase current application example, therefore select a bidirectional variant. The TMCS1126-Q1 has a precision internal reference voltage that determines the zero current output voltage, $V_{OUT,0A}$.

The internal reference voltage on TMCS1126AxA-Q1 variants, with zero current output voltage $V_{OUT,0A}$ = 2.5V is intended for bidirectional current measurements when used with 5V power supplies. The internal reference voltage on TMCS1126BxA-Q1 variants, with zero current output voltage $V_{OUT,0A}$ = 1.65V is intended for bidirectional current measurements when used with 3.3V power supplies. Further consideration of noise and integration with an ADC can be explored, but is beyond the scope of this application design example. The TMCS1126-Q1 output voltage V_{OUT} is proportional to the input current I_{IN} as defined by 式 30 with output offset set by $V_{OUT,0A}$.

$$V_{OUT} = (I_{IN} \times S) + V_{OUT,0A} \quad (30)$$

Design of the sensing solution focuses on maximizing the sensitivity of the device while maintaining linear measurement over the expected current input range. The TMCS1126-Q1 has a linear measurable current range that is constrained by either the positive swing to supply or negative swing to ground. To account for the operating margin, consider the previously defined minimum possible supply voltage $V_{S,min}$ = 4.9V. With the previous parameters, the maximum linear output voltage $V_{OUT,max}$ is defined by 式 31 and the minimum linear output voltage $V_{OUT,min}$ is defined by 式 32.

$$V_{OUT,\ max} = V_{S,\ min} - 100mV \tag{31}$$

$$V_{OUT,\ min} = 100mV \tag{32}$$

Design parameters for this example application are shown in 表 9-4 along with the calculated output range.

表 9-4. Example Application Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{OUT,max}$	4.8V
$V_{OUT,0A}$	2.5V
$V_{OUT,max} – V_{OUT,0A}$	2.3V

These design parameters result in a maximum positive linear output voltage swing of ±2.3V about $V_{OUT,0A}$ = 2.5V. To determine which sensitivity variant of the TMCS1126-Q1 most fully uses this linear range, use 式 33 to calculate the maximum current range for a bidirectional current $\pm I_{IN,max}$.

$$I_{IN,\ max} = \frac{\left(V_{OUT,\ max} - V_{OUT,\ 0A}\right)}{S} \tag{33}$$

where

- S is the sensitivity of the relevant AxA variant.

表 9-5 shows the calculation for each gain variant of the TMCS1126-Q1 with the appropriate sensitivities.

表 9-5. Maximum Full-Scale Current Ranges With 2.3V Positive Output Swing

VARIANT	SENSITIVITY	$I_{IN,max}$
TMCS1126ADx-Q1	20mV/A	±115A
TMCS1126A1x-Q1	25mV/A	±92A
TMCS1126A7x-Q1	30mV/A	±76.6A
TMCS1126A8x-Q1	40mV/A	±57.5A
TMCS1126A2x-Q1	50mV/A	±46A
TMCS1126A3x-Q1	75mV/A	±30.6A
TMCS1126A4x-Q1	100mV/A	±23A
TMCS1126A5x-Q1	150mV/A	±15.3A

In general, the highest sensitivity variant is selected to provide the lowest maximum input current range that is larger than the desired full-scale current range. For the design parameters in this example, either the higher precision TMCS1126A4A-Q1 or the less accurate TMCS1126A4B-Q1 (both with sensitivity of 100mV/A is the proper selection because the maximum ±23A linear measurable range is larger than the desired ±20A full-scale current range.

9.2.3 Application Curve

To illustrate high levels of isolation achievable between noisy high-voltage current sensing nodes and low-voltage precision current measurement and control circuitry, 図 9-3 shows the output signal from the TMCS1126-Q1 in a noisy in-phase PWM motor control example. In this example with a large induction motor under no load, no PWM edge interference is seen on the current sensor output with high-voltage PWM switching on the current sensor input, as is often pronounced on many current sensors.

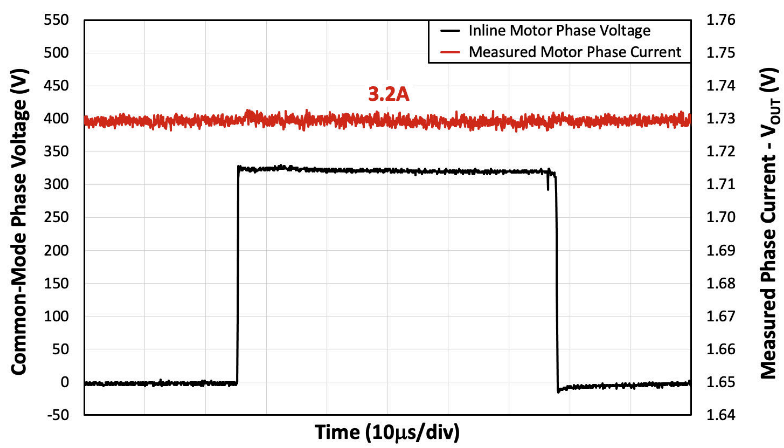

図 9-3. Inline Motor Current-Sense Input and Output Signals

9.3 Power Supply Recommendations

The TMCS1126-Q1 only requires a power supply (V_S) on the low-voltage isolated side, which powers the analog circuitry independent of the isolated current input. V_S determines the full-scale output range of the analog output V_{OUT}, and can be supplied with any voltage between 3V and 5.5V. To filter noise in the power-supply path, place a low-ESR decoupling capacitor of 0.1µF between V_S and GND pins as close as possible to the supply and ground pins of the device. More decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. When used in extremely noisy environments, ferrite beads can be added close to the supply pin as shown in 図 9-4 to target and suppress high-frequency noise coupled on to system supply.

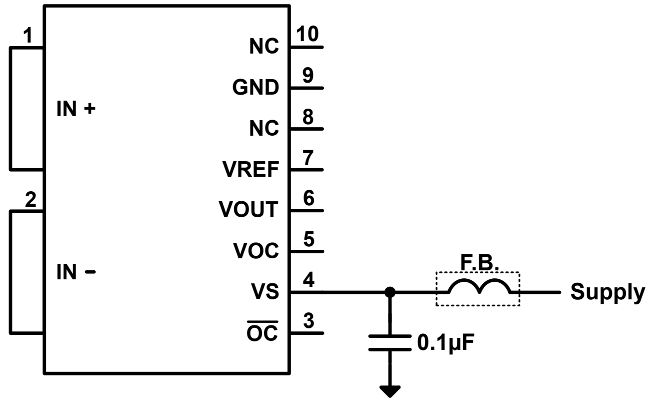

図 9-4. Power Supply Noise Filtering

The TMCS1126-Q1 power supply V_S can be sequenced independently of current flowing through the input. However, there is a power-on delay between V_S reaching the recommended operating voltage and the analog output validation. During this power-on time, the output voltage V_{OUT} can transition between GND and V_S as the output transfers from a high impedance reset state to the active drive state. If this behavior must be avoided, then provide a stable supply voltage V_S for longer than the power-on time prior to applying input current.

9.4 Layout

9.4.1 Layout Guidelines

The TMCS1126-Q1 is specified for a continuous current handling capability on the *TMCS1126xEVM* which uses 4oz copper planes. This current capability is fundamentally limited by the maximum device junction temperature and the thermal environment, primarily the PCB layout and design. To maximize current-handling capability and thermal stability of the device, take care with PCB layout and construction to optimize the thermal capability. Efforts to improve the thermal performance beyond the design and construction of the *TMCS1126xEVM* can result in increased continuous-current capability due to higher heat transfer to the ambient environment. Keys to improving thermal performance of the PCB include:

- Use large copper planes for both input current path and isolated power planes and signals.
- Use heavier copper PCB construction.
- Place thermal via *farms* around the isolated current input.
- Provide airflow across the surface of the PCB.

9.4.2 Layout Example

An example layout, shown in 図 9-5, is from the *TMCS1126xEVM User's Guide* . Device performance is targeted for thermal and magnetic characteristics of this layout, which provides optimal current flow from the terminal connectors to the device input pins while large copper planes enhance thermal performance.

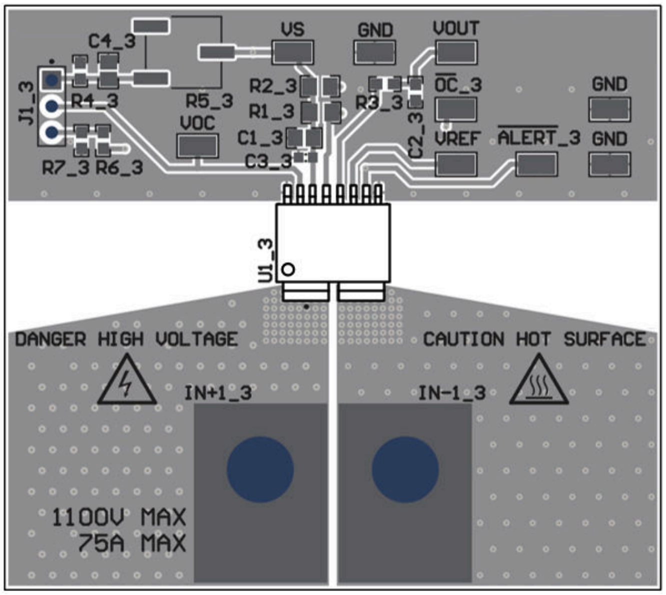

図 9-5. Recommended Board Layout

10 Device and Documentation Support

10.1 Device Nomenclature

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *DVG*), the temperature range, and the device speed range, in megahertz. 図 10-1 provides a legend for reading the complete device name for any *TMCS1126-Q1* device.

For orderable part numbers of *TMCS1126-Q1* devices in the *SOIC* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *Silicon Errata*.

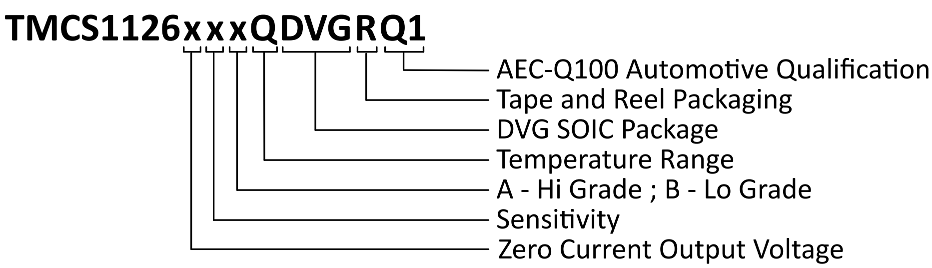

図 10-1. Part Number Naming Designators

10.2 Device Support

10.2.1 Development Support

For development tool support see the following:

- Texas Instruments, *TMCS1126xEVM*

10.3 Documentation Support

10.3.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMCS1126xEVM User's Guide*

- Texas Instruments, *Isolation Glossary*, application note

10.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.5 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.8 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2024) to Revision A (November 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新。...1
- Added the *Setting The User Configurable Overcurrent Threshold*, *Setting Overcurrent Threshold Using Power Supply Voltage*, *Setting Overcurrent Threshold Using Internal Reference Voltage*, *Setting Overcurrent Threshold Example*, and *Overcurrent Output Response sections* to the *Overcurrent Detection* section.........25

12 Mechanical, Packaging, and Orderable Information

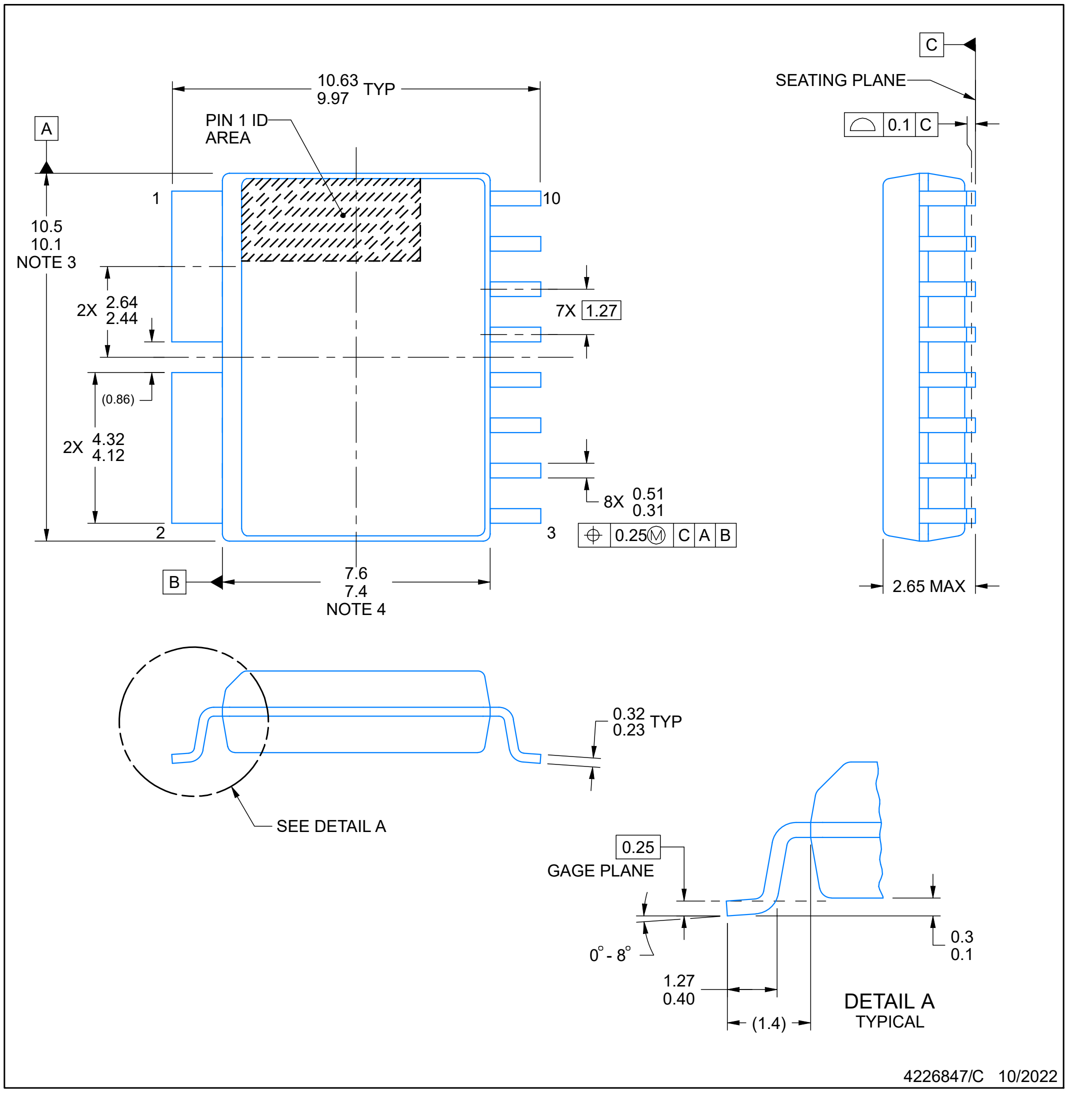
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DVG0010A

SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

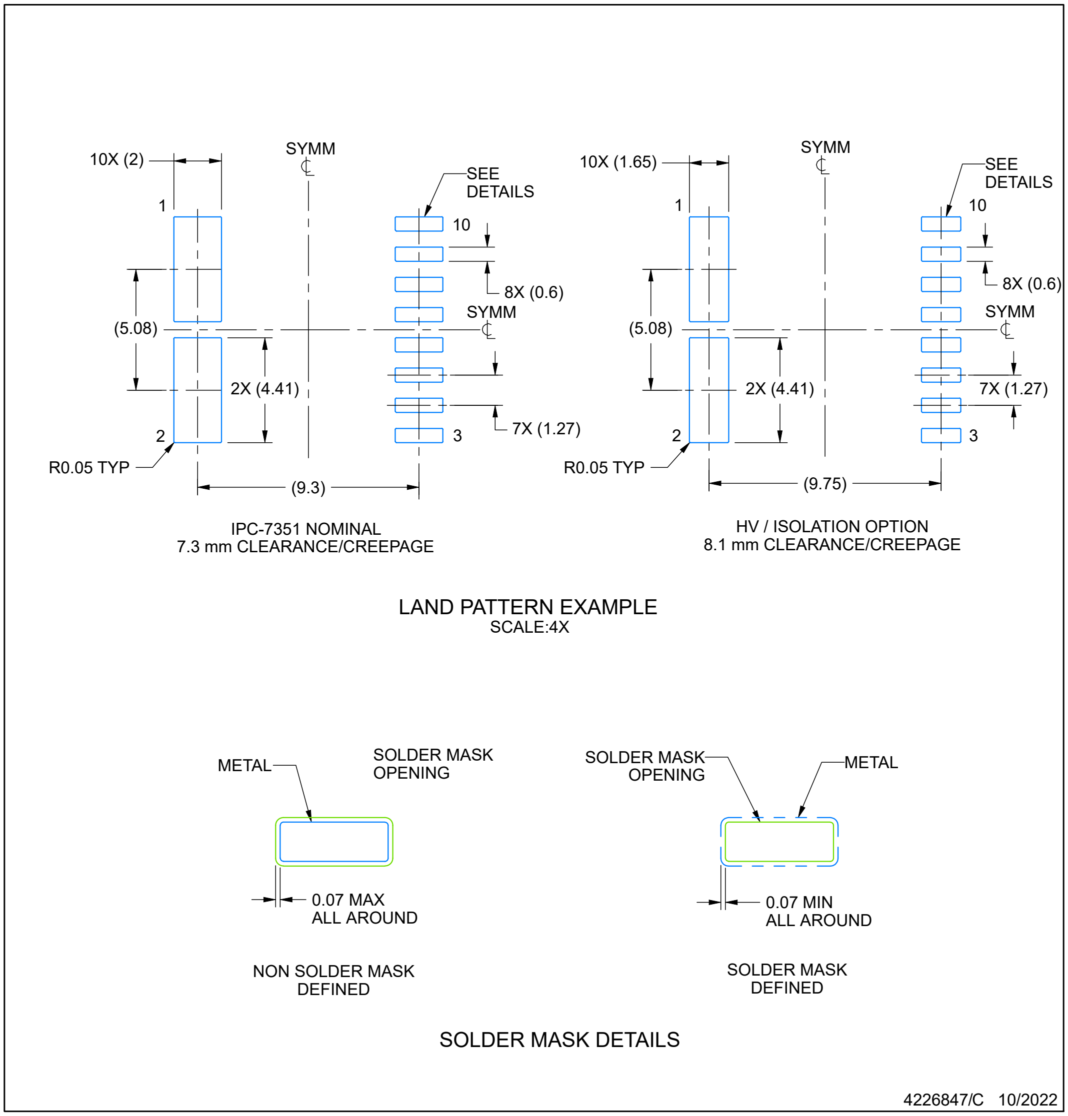
www.ti.com

EXAMPLE BOARD LAYOUT

DVG0010A

SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

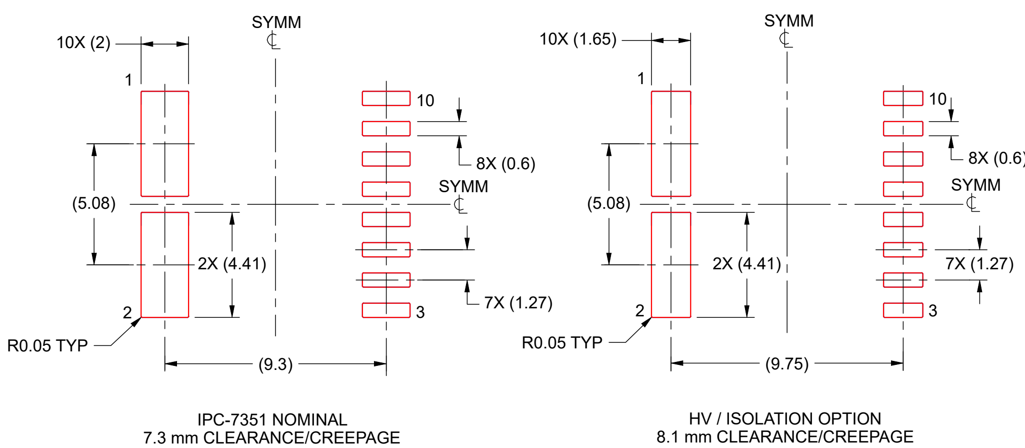
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DVG0010A

SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4226847/C 10/2022

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMCS1126A1AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126A1AQ1	Samples
TMCS1126A1BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126A1BQ1	Samples
TMCS1126A2AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126A2AQ1	Samples
TMCS1126A2BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126A2BQ1	Samples
TMCS1126A3BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126A3BQ1	Samples
TMCS1126A7AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126A7AQ1	Samples
TMCS1126A8AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126A8AQ1	Samples
TMCS1126A8BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126A8BQ1	Samples
TMCS1126B1AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B1AQ1	Samples
TMCS1126B1BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B1BQ1	Samples
TMCS1126B2AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B2AQ1	Samples
TMCS1126B4AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B4AQ1	Samples
TMCS1126B5AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B5AQ1	Samples
TMCS1126B6AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B6AQ1	Samples
TMCS1126B6BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B6BQ1	Samples
TMCS1126B8BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B8BQ1	Samples
TMCS1126B9AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B9AQ1	Samples
TMCS1126B9BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126B9BQ1	Samples
TMCS1126BBAQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126BBAQ1	Samples
TMCS1126BDAQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126BDAQ1	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMCS1126C4AQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126C4AQ1	Samples
TMCS1126C5BQDVGRQ1	ACTIVE	SOIC	DVG	10	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1126C5BQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TMCS1126-Q1 :

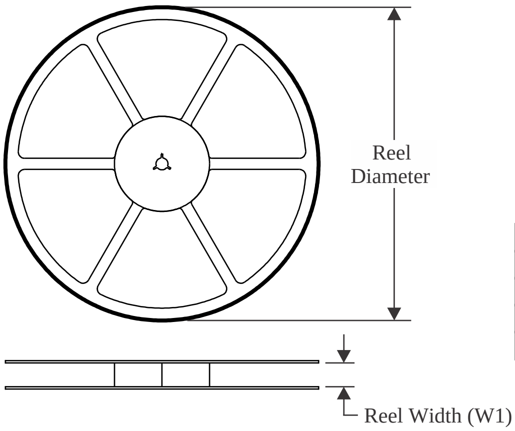
- Catalog : TMCS1126

NOTE: Qualified Version Definitions:

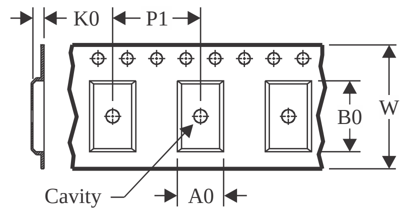
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

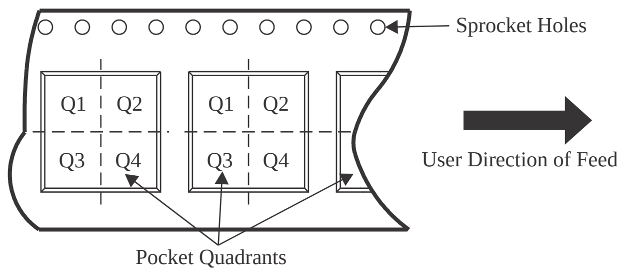


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

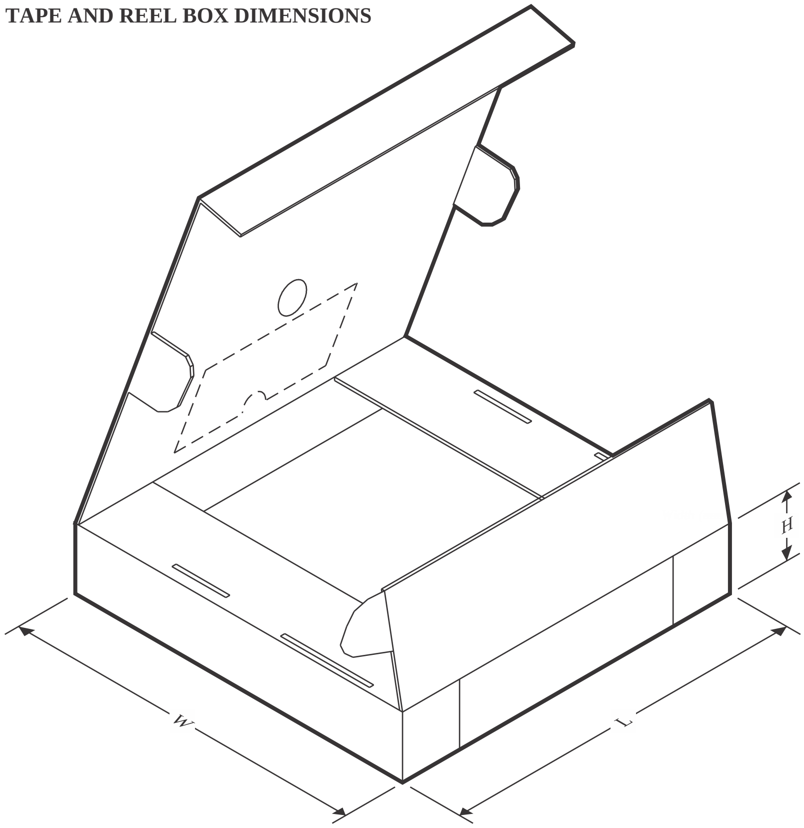


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMCS1126A1AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126A1BQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126A2AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126A2BQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126A7AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126A8AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126B1AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126B1BQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126B2AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126B4AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126B5AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126B6AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126B9AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126BBAQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126BDAQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1126C4AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

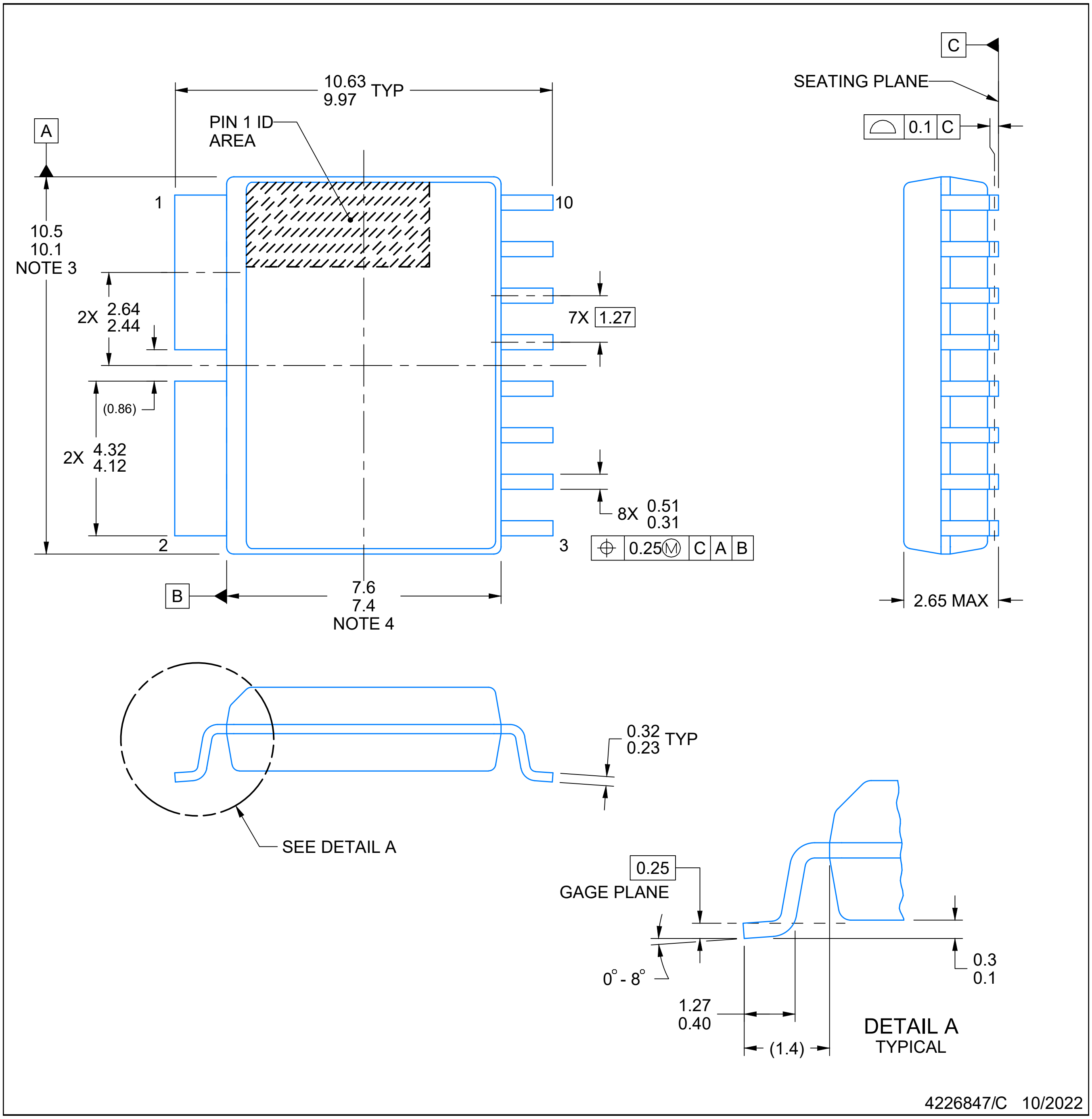
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMCS1126C5BQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



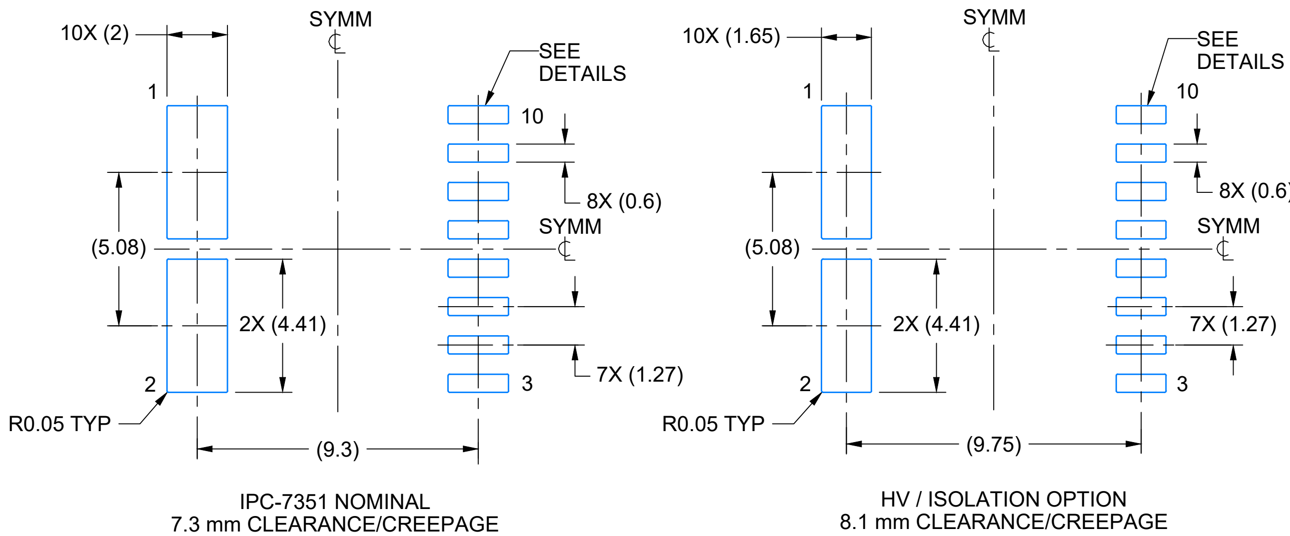
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMCS1126A1AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126A1BQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126A2AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126A2BQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126A7AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126A8AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126B1AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126B1BQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126B2AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126B4AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126B5AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126B6AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126B9AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126BBAQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126BDAQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126C4AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1126C5BQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0

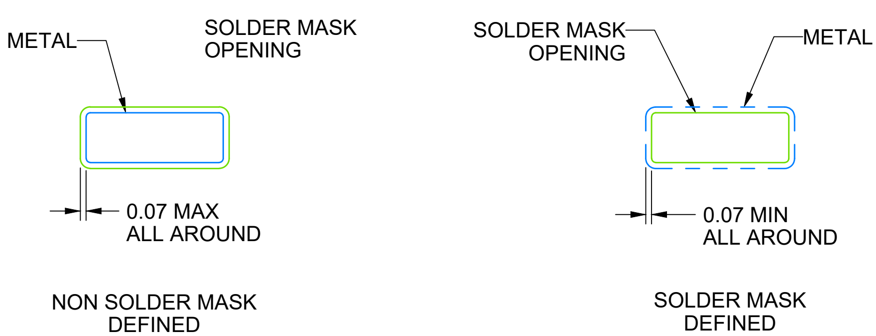


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

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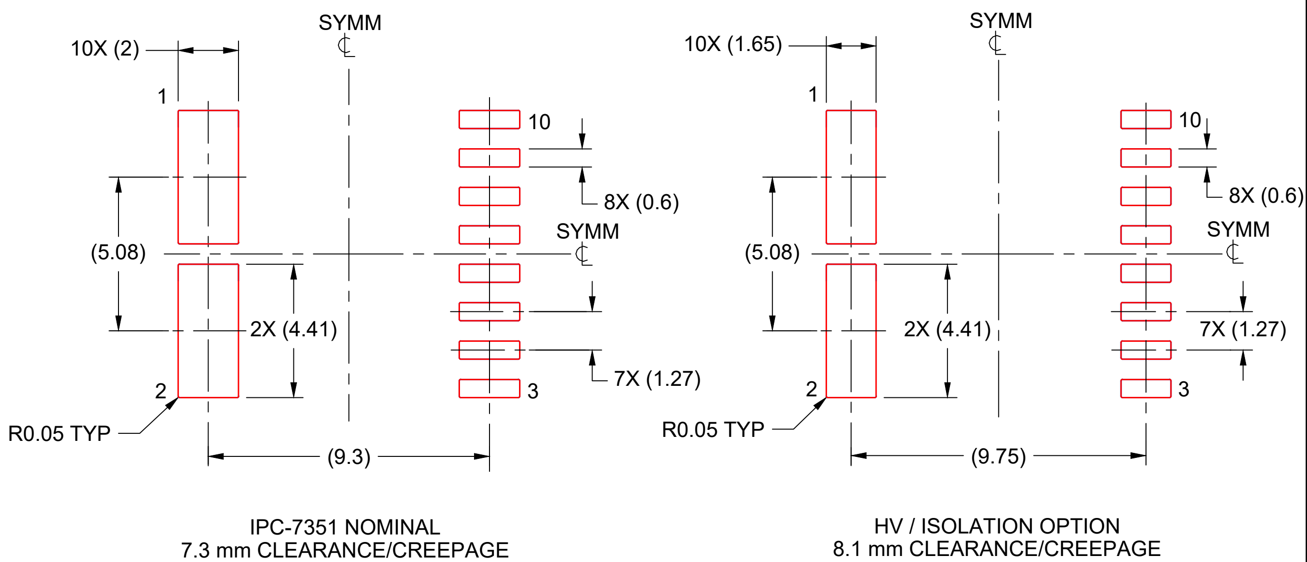
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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