TLV703x-Q1/TLV704x-Q1 レール・ツー・レール、低消費電力コンパレータ

1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C5
- 広い電源電圧範囲:1.6V～6.5V
- 静止消費電流:315nA
- 短い伝搬遅延:3µs
- 内部ヒステリシス:6.5mV
- レール・ツー・レールの同相入力電圧
- 既知の起動条件を確保するパワー・オン・リセット機能を内蔵
- オーバードライブ入力についても位相反転なし
- プッシュ・プル出力 (TLV703x-Q1)
- オープン・ドレイン出力 (TLV704x-Q1)
- –40℃～125℃の動作温度
- 機能安全に対応
  - 機能安全システムの設計に役立つ資料を利用可能 (TLV70x1-Q1)
  - 機能安全システムの設計に役立つ資料を利用可能 (TLV70x2-Q1)

2 アプリケーション

- テレマティクス eCall
- 車載用ヘッド・ユニット
- インストルメント・クラスタ
- オーディオ・アンプ
- オンボード・チャージャ (OBC) / ワイヤレス・チャージャ

3 概要

TLV703x-Q1/TLV704x-Q1 は、レール・ツー・レール入力を備えた低電圧ナノパワー・コンパレータです。これらのコンパレータは、インフォテインメント、テレマティクス、ヘッド・ユニット・アプリケーションなど、スペースに制約があり消費電力を重視した設計に適用できます。

TLV703x-Q1 と TLV704x-Q1 は低消費電力と高速応答を兼ね備えています。この高速な応答時間とナノパワーとの組み合わせから、電力の限られたシステムでも、フォルト状況を監視して迅速に応答できます。これらのコンパレータの動作電圧範囲は 1.6V～6.5V であり、1.8V、3V、5V のシステムと互換性があります。

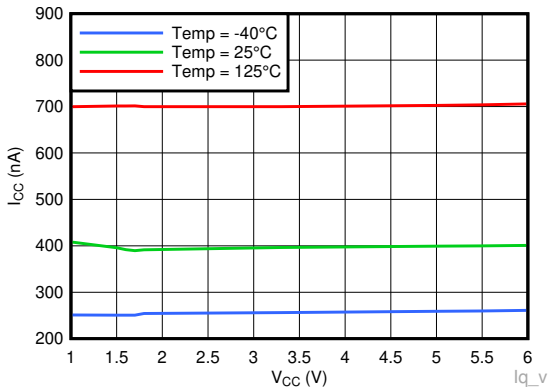
また、TLV703x-Q1 と TLV704x-Q1 は、オーバードライブ入力に対しても出力位相が反転しないことが保証されており、内部ヒステリシスが存在するため、緩やかに変動する入力信号をクリーンなデジタル出力に変換する必要があるノイズが多い過酷環境でも、高精度の電圧監視に使用できます。

TLV703x-Q1 は、数ミリアンペアの電流をシンクおよびソースできるプッシュプル出力段を備えています。TLV704x-Q1 は、V_{CC} を超えてプルできるオープン・ドレイン出力段を備えています。

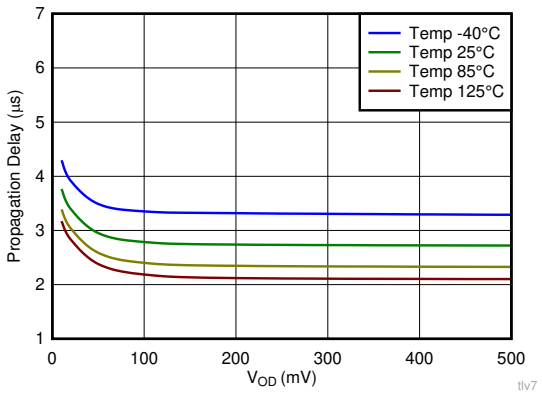
製品情報

部品番号	パッケージ (ピン数) (1)	本体サイズ (公称)
TLV7031-Q1、TLV7041-Q1	SC70 (5)	2.00mm × 1.25mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV7032-Q1、TLV7042-Q1	VSSOP (8)	3.00mm × 3.00mm
	SOT-23 (8)	2.90mm × 1.60mm
TLV7034-Q1、TLV7044-Q1	TSSOP (14)	4.40mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



I_{CC} と V_{CC} との関係



伝搬遅延と入力オーバードライブとの関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2021) to Revision D (February 2023) — **Page**

- TLV7032-Q1 および TLV7042-Q1 の SOT-23 (8) パッケージ・オプションからプレビュー注記を削除 ... 1

Changes from Revision B (February 2021) to Revision C (October 2021) — **Page**

- 「特長」セクションに新しい FIT 率レポートのリンクを追加 ... 1

Changes from Revision A (October 2020) to Revision B (February 2021) — **Page**

- 全体にわたってデュアルおよびクワッド・パッケージ・オプションを追加 ... 1

Changes from Revision * (May 2020) to Revision A (October 2020) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- APL から RTM へのリリース ... 1

5 Pin Configuration and Functions

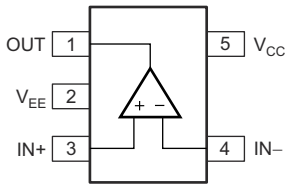


図 5-1. DBV, DCK Packages
5-Pin SOT-23, SC70
Top View

表 5-1. Pin Functions

PIN		I/O (1)	DESCRIPTION
SOT-23, SC70	NAME		
1	OUT	O	Output
5	V_{CC}	P	Positive (highest) power supply
2	V_{EE}	P	Negative (lowest) power supply
4	IN–	I	Inverting input
3	IN+	I	Noninverting input

(1) I = Input, O = Output, P = Power

Pin Functions: TLV7032/42

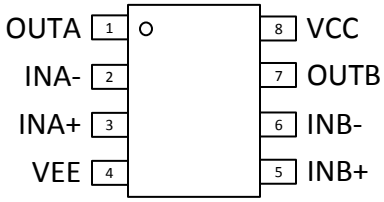


図 5-2. TLV7032/42 DGK, DDF Packages
8-Pin VSSOP, SOT-23
Top View

表 5-2. Pin Functions: TLV7032/42

PIN		I/O	DESCRIPTION
NAME	NO.		
INA–	2	I	Inverting input, channel A
INA+	3	I	Noninverting input, channel A
INB–	6	I	Inverting input, channel B
INB+	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
VEE	4	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	8	—	Positive (highest) supply

5.1 Pin Functions: TLV7034/44

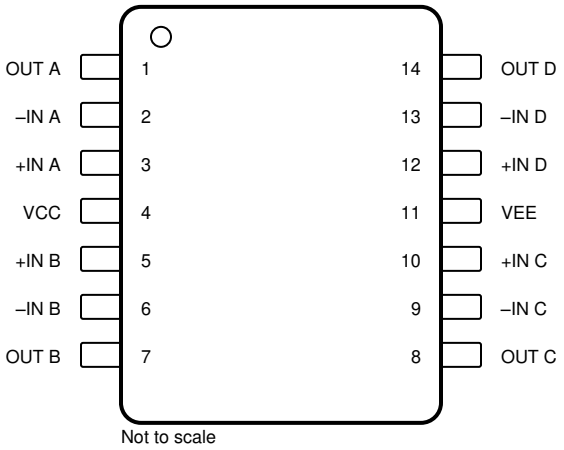


図 5-3. TLV7034/44 PW Packages
14-Pin TSSOP
Top View

表 5-3. Pin Functions: TLV7034/44

PIN		I/O	DESCRIPTION
NAME	TSSOP		
–IN1 A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
NC	—	—	No internal connection
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
VEE	11	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} – V_{EE}$	–0.3	7	V
Input pins (IN+, IN–) (2)	V_{EE} – 0.3	7	V
Output (OUT) (push-pull)(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Output (OUT) (open-drain)	V_{EE} – 0.3	7	V
Output short-circuit duration(4)		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to V_{EE}. Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less
(3) Output maximum is (V_{CC} + 0.3 V) or 7 V, whichever is less.
(4) Short-circuit to ground, one comparator per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} – V_{EE}$	1.6	6.5	V
Input voltage range	V_{EE} – 0.1	V_{CC} + 0.1	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information (Single)

THERMAL METRIC (1)		TLV7031/TLV7041		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	297.2	278.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	224.7	186.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	200.1	113.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	141.2	82.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	198.9	112.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information (Dual)

THERMAL METRIC (1)		TLV7032/TLV7042		UNIT
		DGK (VSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.7	212.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	127.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.5	129.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.3	25.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	131.7	129.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Thermal Information (Quad)

THERMAL METRIC (1)		TLV7034/44		UNIT
		RTE (QFN)	PW (TSSOP)	
		16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.4	131.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.2	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.5	74.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.6	12.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.5	73.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	24.1	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = V_S / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = V_S / 2, T_A = 25℃	2	6.5	17	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (push-pull only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Output leakage current (open-drain only)	V_S = 5 V, V_{ID} = +0.1 V (Output High), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	V_S = 5 V, sourcing (push-pull only)		35		mA
		V_S = 5 V, sinking		40		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		390	900	nA

6.8 Switching Characteristics

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; C_L = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ open-drain only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ open-drain only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (push-pull only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output will reflect the input..		200		µs

6.9 Electrical Characteristics (Dual)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (push-pull only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Output leakage current (open-drain only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing (push-pull only)		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		315	750	nA

6.10 Switching Characteristics (Dual)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ open-drain only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ open-drain only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (push-pull only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output will reflect the input..		200		µs

(1) The lower limit for RP is 650 Ω

6.11 Electrical Characteristics (Quad)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (push-pull only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Output leakage current (open-drain only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing (push-pull only)		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		315	750	nA

6.12 Switching Characteristics (Quad)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ open-drain only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ open-drain only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (push-pull only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for t_{ON} before the output will reflect the input..		400		µs

(1) The lower limit for RP is 650 Ω

6.13 Timing Diagrams

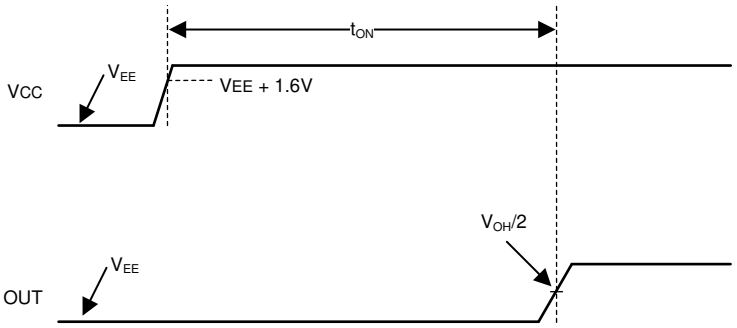


図 6-1. Start-Up Time Timing Diagram (IN+ > IN–)

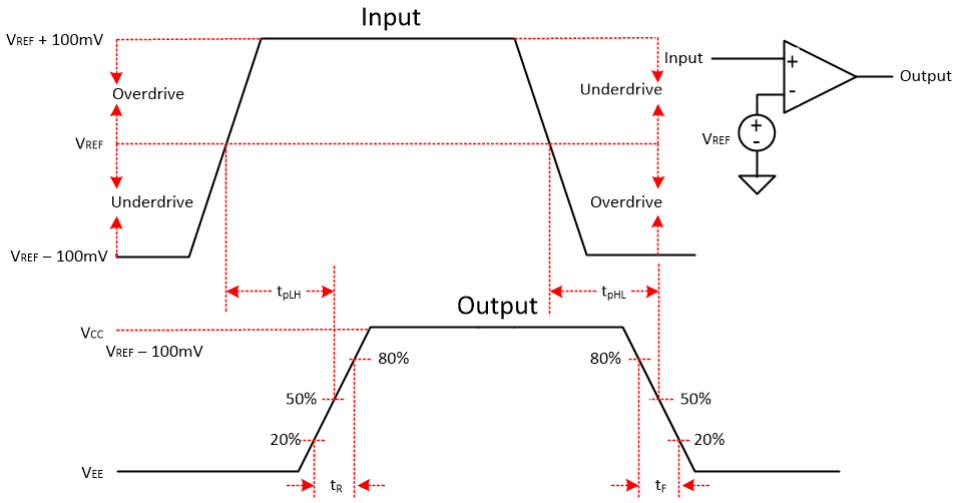


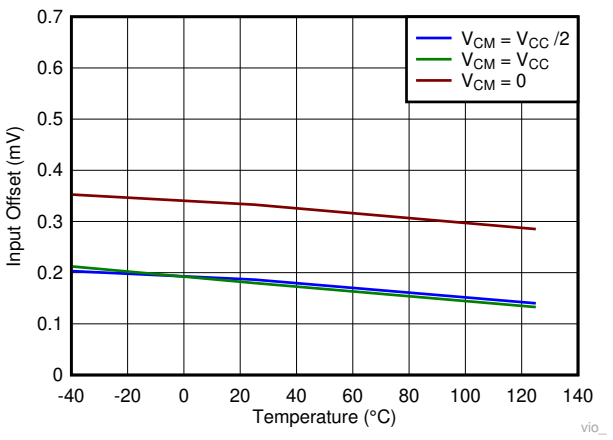
図 6-2. Propagation Delay Timing Diagram

注

The propagation delays t_{pLH} and t_{pHL} include the contribution of input offset and hysteresis.

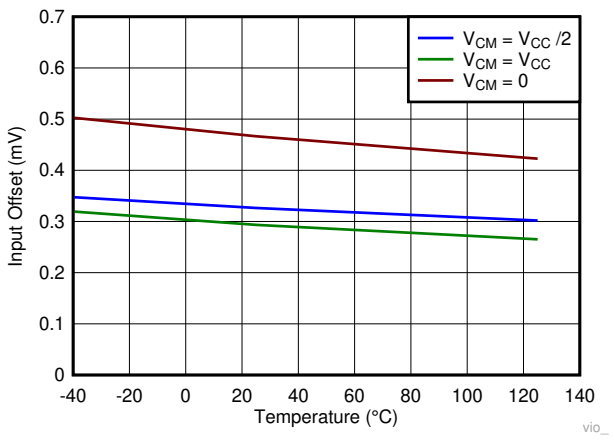
6.14 Typical Characteristics

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



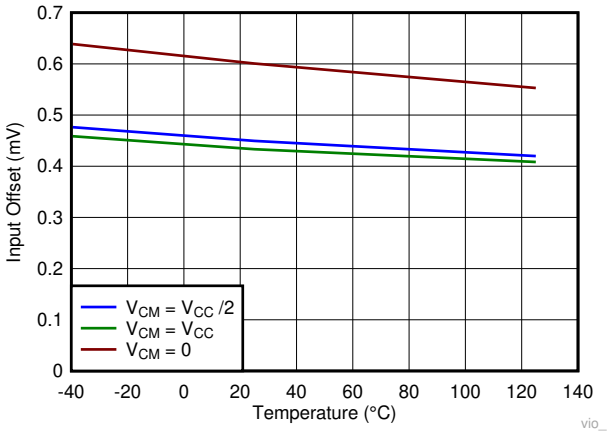
V_{CC} = 1.8 V

図 6-3. Input Offset vs Temperature



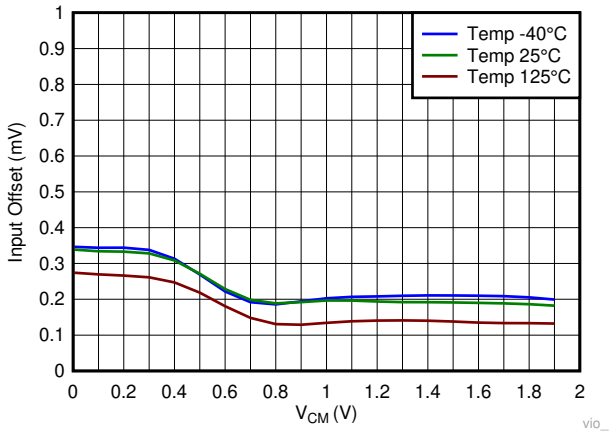
V_{CC} = 3.3 V

図 6-4. Input Offset vs Temperature



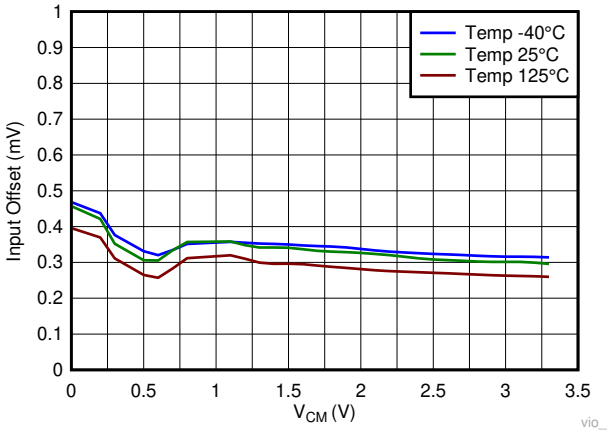
V_{CC} = 5 V

図 6-5. Input Offset vs Temperature



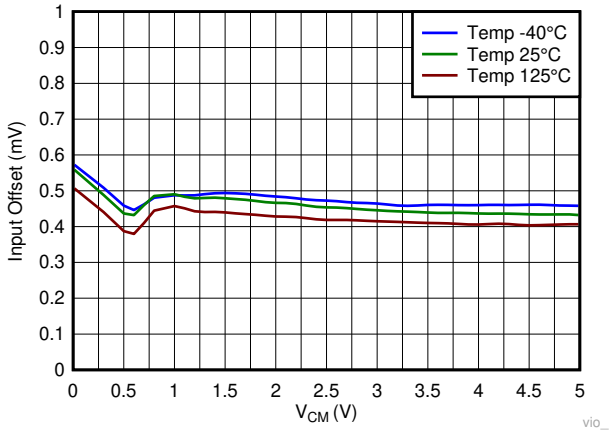
V_{CC} = 1.8 V

図 6-6. Input Offset Voltage vs V_{CM}



V_{CC} = 3.3 V

図 6-7. Input Offset Voltage vs V_{CM}

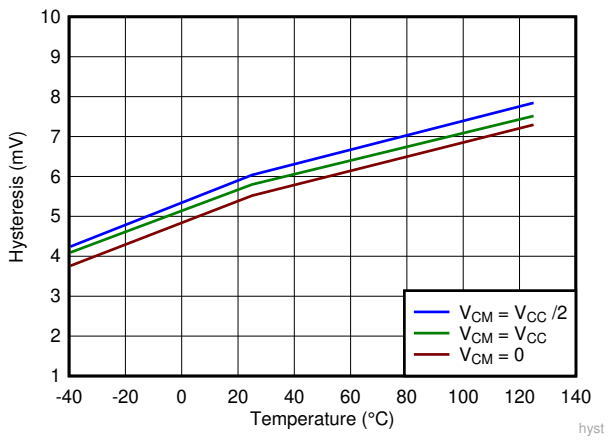


V_{CC} = 5 V

図 6-8. Input Offset Voltage vs V_{CM}

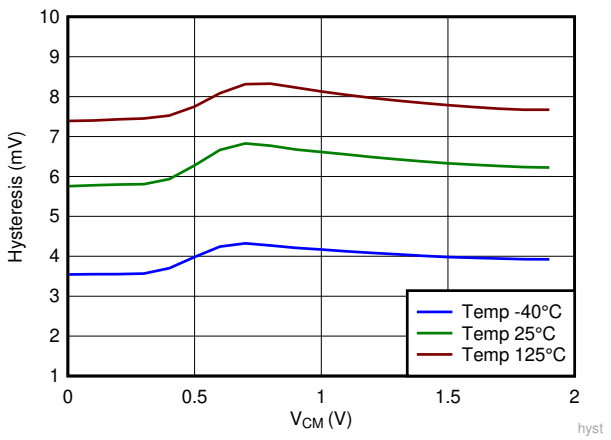
6.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



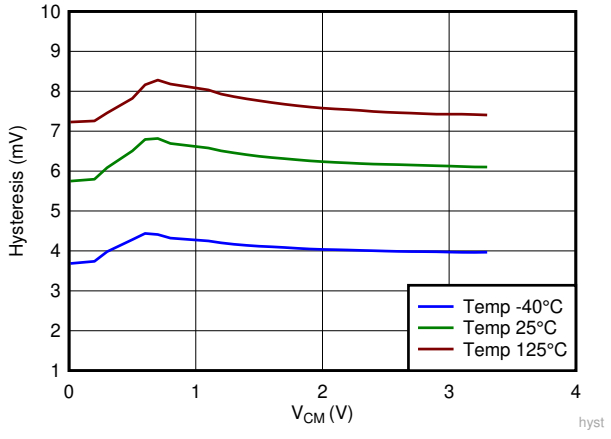
V_{CC} = 1.8 V to 5 V TLV70x1

図 6-9. Hysteresis vs Temperature



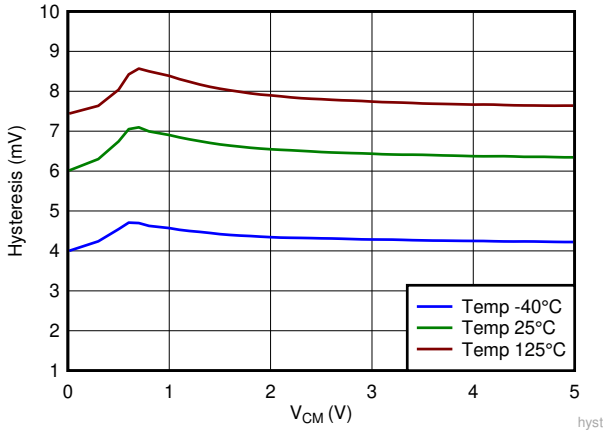
V_{CC} = 1.8 V TLV70x1

図 6-10. Hysteresis vs V_{CM}



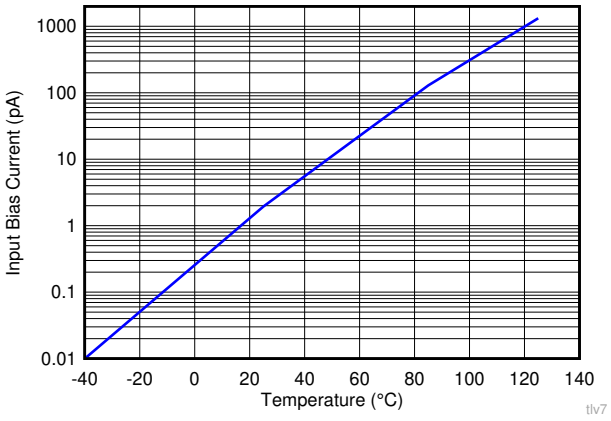
V_{CC} = 3.3 V TLV70x1

図 6-11. Hysteresis vs V_{CM}



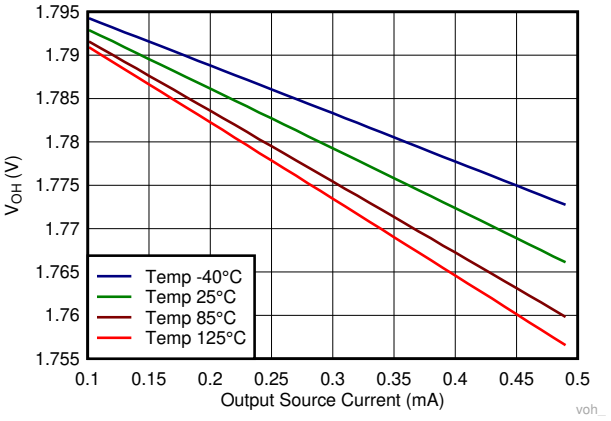
V_{CC} = 5 V TLV70x1

図 6-12. Hysteresis vs V_{CM}



A. V_{CC} = 5 V

図 6-13. Input Bias Current vs Temperature

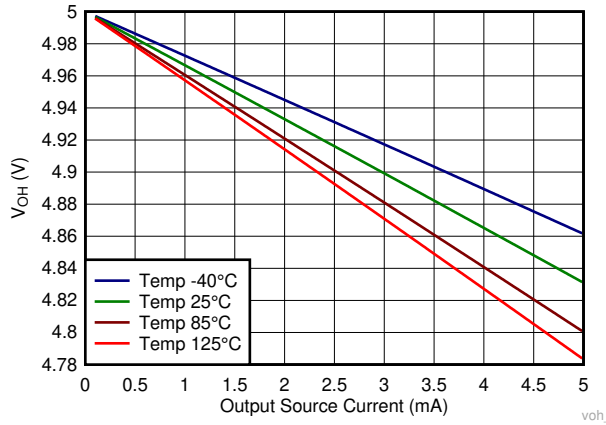


V_{CC} = 1.8 V TLV703x

図 6-14. Output Voltage High vs Output Source Current

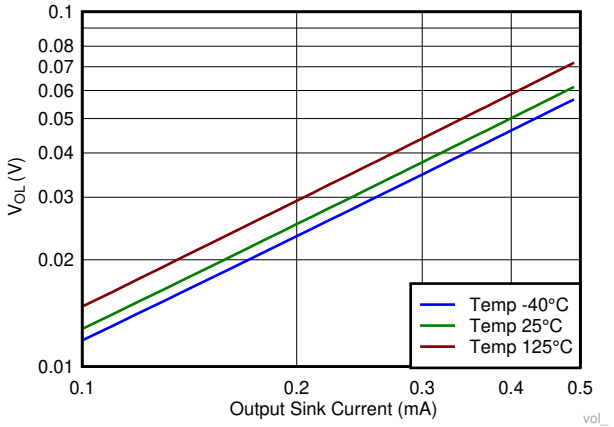
6.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



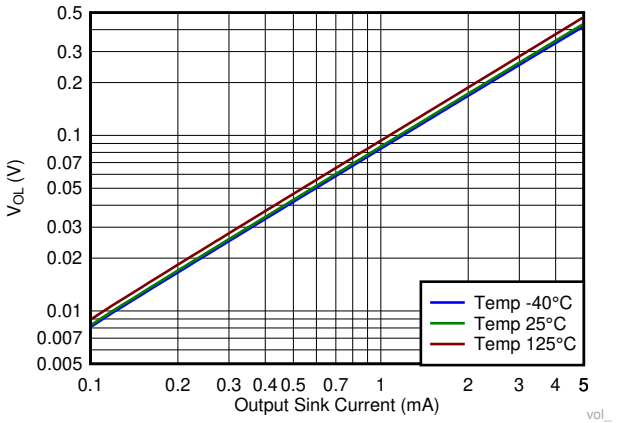
V_{CC} = 5 V TLV703x

図 6-15. Output Voltage High vs Output Source Current



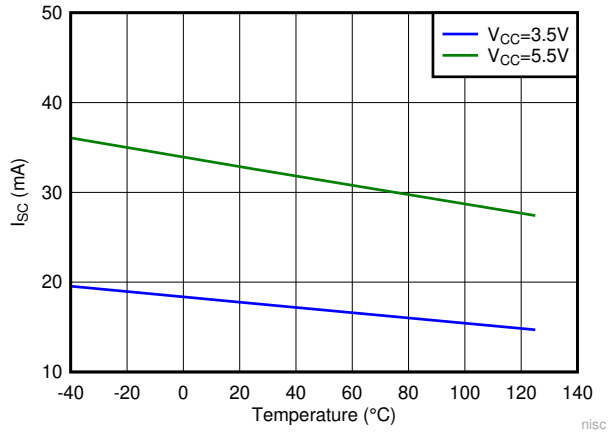
V_{CC} = 1.8 V

図 6-16. Output Voltage Low vs Output Sink Current



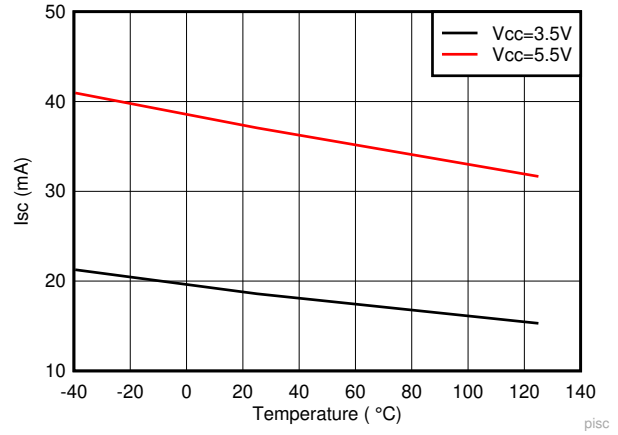
V_{CC} = 5 V

図 6-17. Output Voltage Low vs Output Sink Current



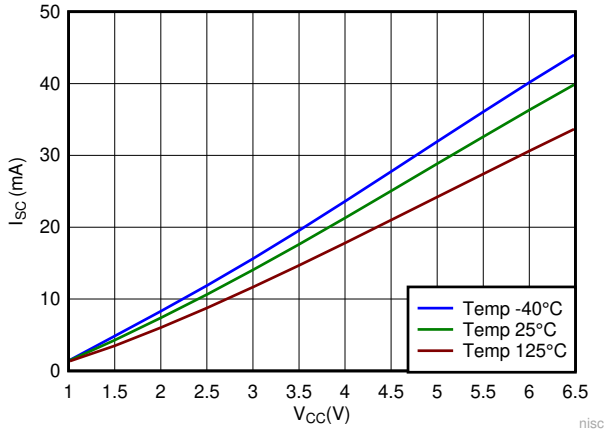
V_{CM} = V_{CC} / 2

図 6-18. Output Short-Circuit (Sink) Current vs Temperature



V_{CM} = V_{CC} / 2 TLV703x

図 6-19. Output Short-Circuit (Source) Current vs Temperature

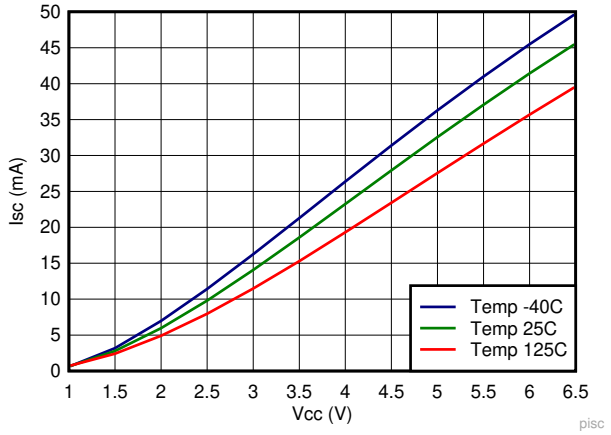


V_{CM} = V_{CC} / 2

図 6-20. Output Short Circuit (Sink) vs V_{CC}

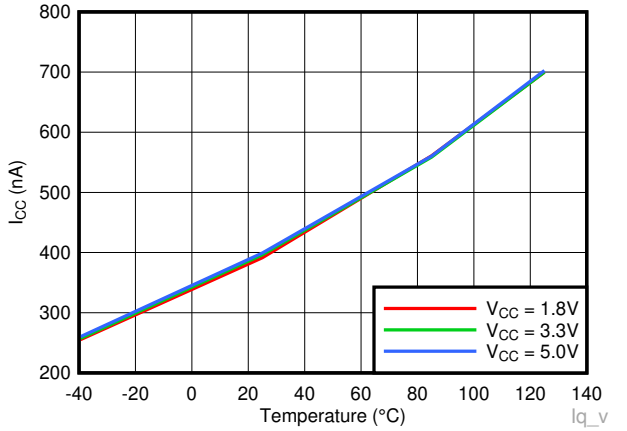
6.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



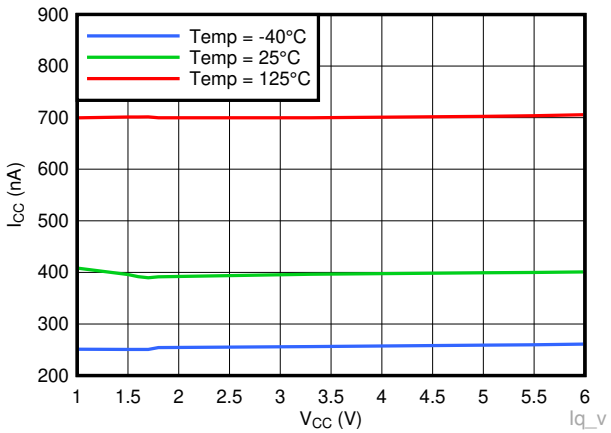
V_{CM} = V_{CC} / 2 TLV703x

図 6-21. Output Short Circuit (Source) vs V_{CC}



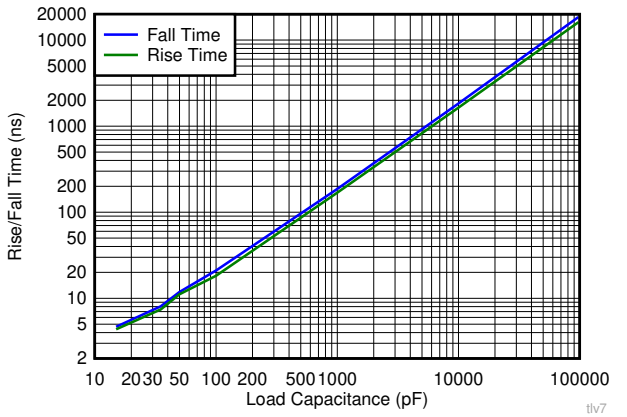
V_{CM} = V_{CC} / 2 TLV70x2

図 6-22. I_{CC} vs Temperature



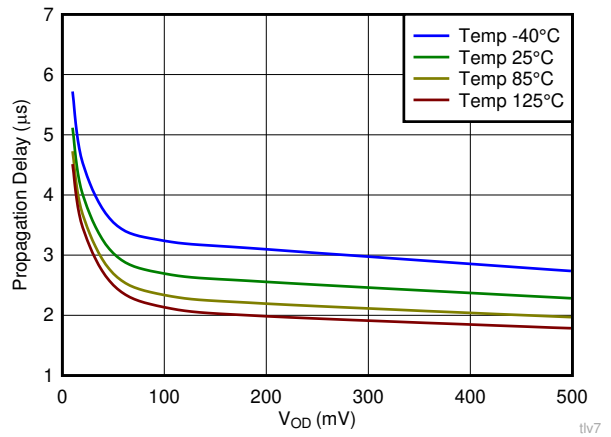
V_{CM} = V_{CC} / 2 TLV70x2

図 6-23. I_{CC} vs V_{CC}



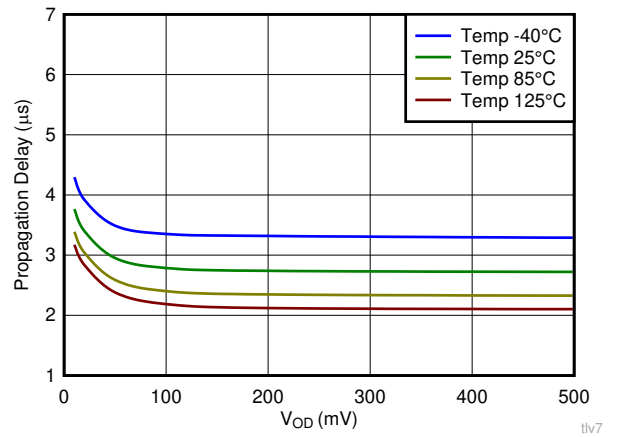
V_{OD} = 100 mV TLV703x Rise only

図 6-24. Rise/Fall Time vs Load Capacitance



V_{CC} = 3.3 V to 5 V TLV703x

図 6-25. Propagation Delay (L-H) vs Input Overdrive



V_{CC} = 3.3 V to 5 V

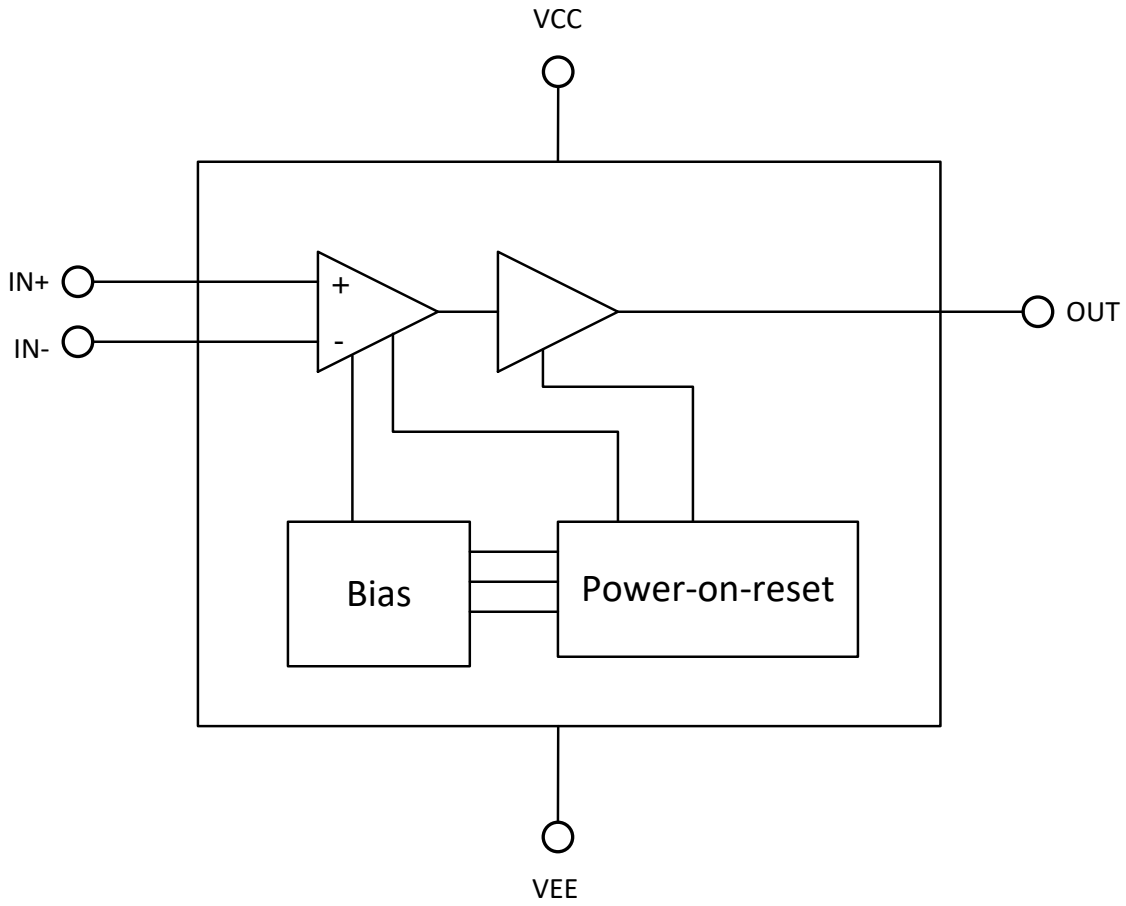
図 6-26. Propagation Delay (H-L) vs Input Overdrive

7 Detailed Description

7.1 Overview

The TLV703x-Q1 and TLV704x-Q1 devices are single-channel, nano-power comparators with push-pull and open-drain outputs. Operating from 1.6 V to 6.5 V and consuming only 315 nA, the TLV703x-Q1 and TLV704x-Q1 are designed for portable and industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV703x-Q1 and TLV704x-Q1 comparators are nanopower comparators that are capable of operating at low voltages. The TLV703x-Q1 and TLV704x-Q1 feature a rail-to-rail input stage capable of operating up to 100 mV beyond the V_{CC} power supply rail. The TLV703x-Q1 (push-pull) and TLV704x-Q1 (open-drain) also feature internal hysteresis.

7.4 Device Functional Modes

The TLV703x-Q1 and TLV704x-Q1 have a power-on-reset (POR) circuit. While the power supply (V_S) is less than the minimum supply voltage, either upon ramp-up or ramp-down, the POR circuitry is activated.

For the TLV703x-Q1, the POR circuit holds the output low (at V_{EE}) while activated.

For the TLV704x-Q1, the POR circuit keeps the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

7.4.1 Inputs

The TLV703x-Q1 and TLV704x-Q1 input common-mode extends from V_{EE} to 100 mV above V_{CC}. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase inversion of the comparator output occurs when the input pins exceed V_{CC} and V_{EE}.

The input of TLV703x-Q1 and TLV704x-Q1 is fault tolerant. It maintains the same high input impedance when V_{CC} is unpowered or ramping up. The input can be safely driven up to the specified maximum voltage (7 V) with V_{CC} = 0 V or any value up to the maximum specified. The V_{CC} is isolated from the input such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between V_{CC} and V_{EE}. The comparator inputs are protected from voltages below V_{EE} by internal diodes connected to V_{EE}. As the input voltage goes under V_{EE}, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles every 10°C temperature increases.

7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in 図 7-1. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (7 mV for both TLV703x-Q1 and TLV704x-Q1).

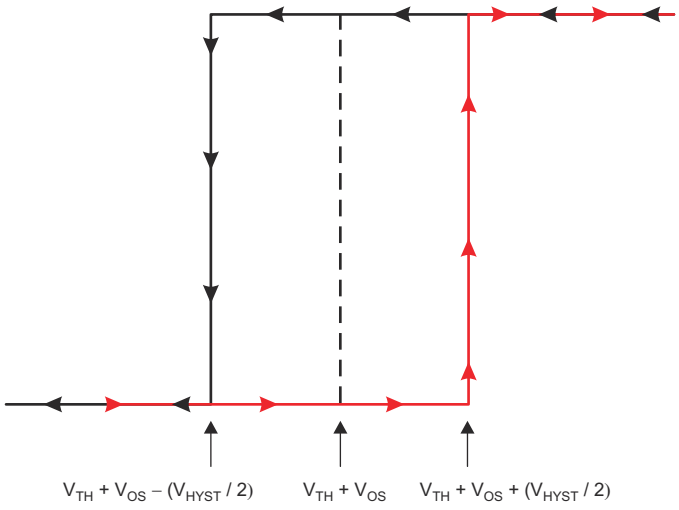


図 7-1. Hysteresis Transfer Curve

7.4.3 Output

The TLV703x-Q1 features a push-pull output stage eliminating the need for an external pullup resistor. On the other hand, the TLV704x-Q1 features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6.5 V independent of the supply voltage.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV703x-Q1 and TLV704x-Q1 are nano-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV703x-Q1 is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV704x-Q1 with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and small size of the TLV703x-Q1 and TLV704x-Q1 make these comparators excellent candidates for battery-operated and portable, handheld designs.

8.1.1 Inverting Comparator With Hysteresis for TLV703x-Q1

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 図 8-1. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. 式 1 defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use 式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

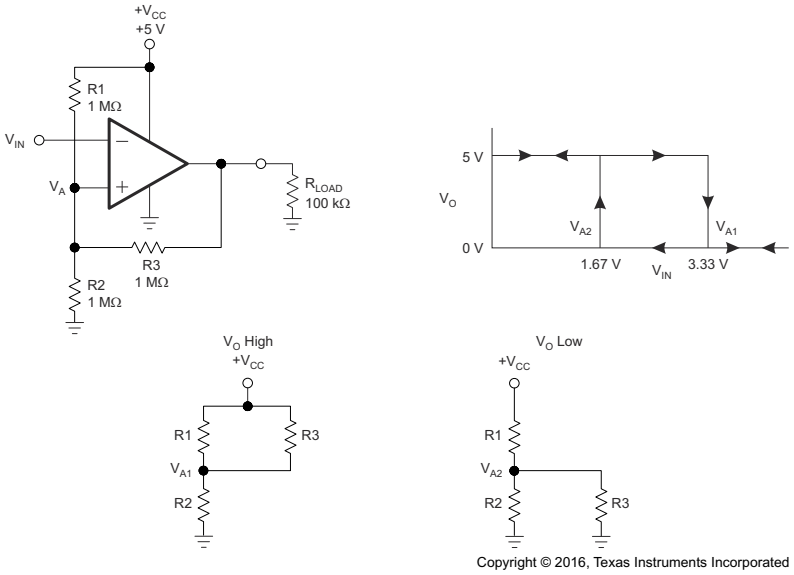


図 8-1. TLV703x-Q1 in an Inverting Configuration With Hysteresis

8.1.2 Noninverting Comparator With Hysteresis for TLV703x-Q1

A noninverting comparator with hysteresis requires a two-resistor network, as shown in 図 8-2, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. Use 式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF}. Use 式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

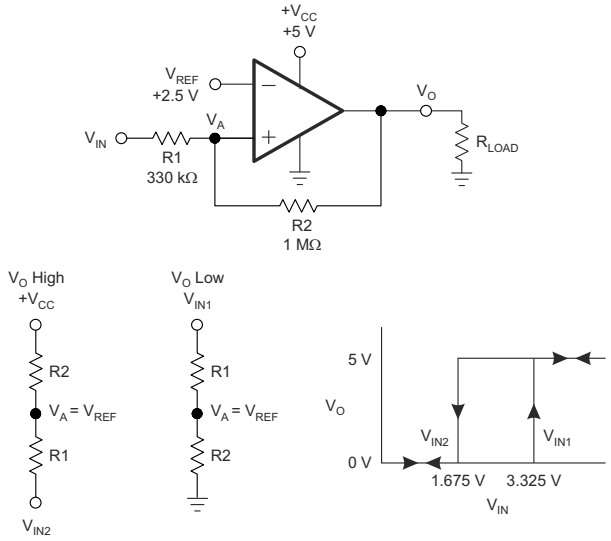


図 8-2. TLV703x-Q1 in a Noninverting Configuration With Hysteresis

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 図 8-3 shows a simple window comparator circuit.

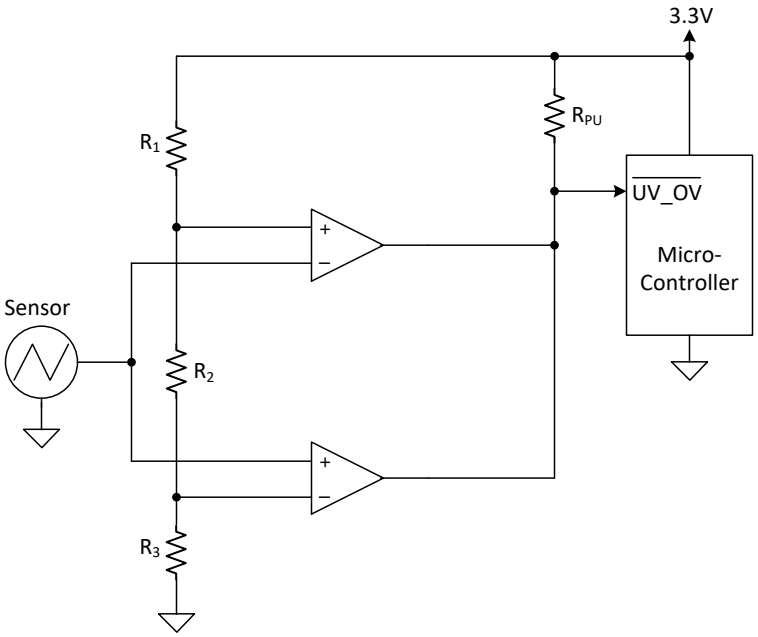


図 8-3. TLV704x-Q1-Based Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 8-3. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2, and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10 MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV704x-Q1 devices. The TLV704x-Q1 is used for its open-drain output configuration. Using the TLV704x-Q1 allows the two comparator outputs to be wire-ored together. The respective comparator outputs are low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} is high when the sensor is in the range of 1.1 V to 2.2 V.

8.2.1.3 Application Curve

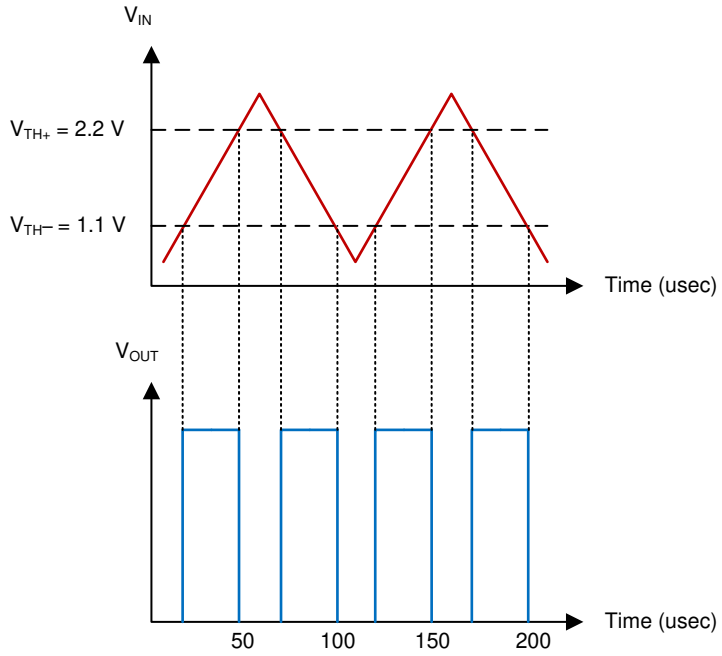


図 8-4. Window Comparator Results

8.2.2 IR Receiver Analog Front End

A single TLV703x-Q1 device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.

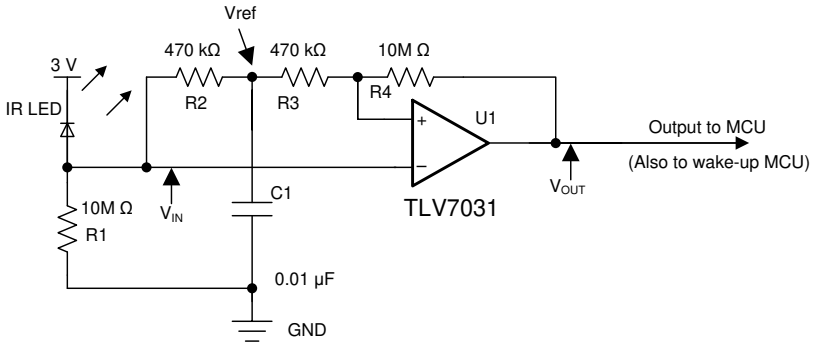


図 8-5. IR Receiver Analog Front End Using TLV703x-Q1

8.2.2.1 Design Requirements

For this design, follow these design requirements:

- Use a proper resistor (R_1) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current I_B (2 pA typical) ensures that a greater value of R1 to be used.
- The RC constant value (R_2 and C_1) must support the targeted data rate (that is, 9,600 bauds) in order to maintain a valid tripping threshold.
- The hysteresis introduced with R_3 and R_4 helps to avoid spurious output toggles.

8.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. R_1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. The RC network of R_2 and C_1 establishes a reference voltage V_{ref}, which tracks the mean amplitude of the IR signal. The noninverting input is directly connected to V_{ref} through R_3. R_3 and R_4 are used to produce a hysteresis to keep transitions free of spurious toggles. To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

More technical details are provided in the TI TechNote *Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters* (SNVA808).

8.2.2.3 Application Curve

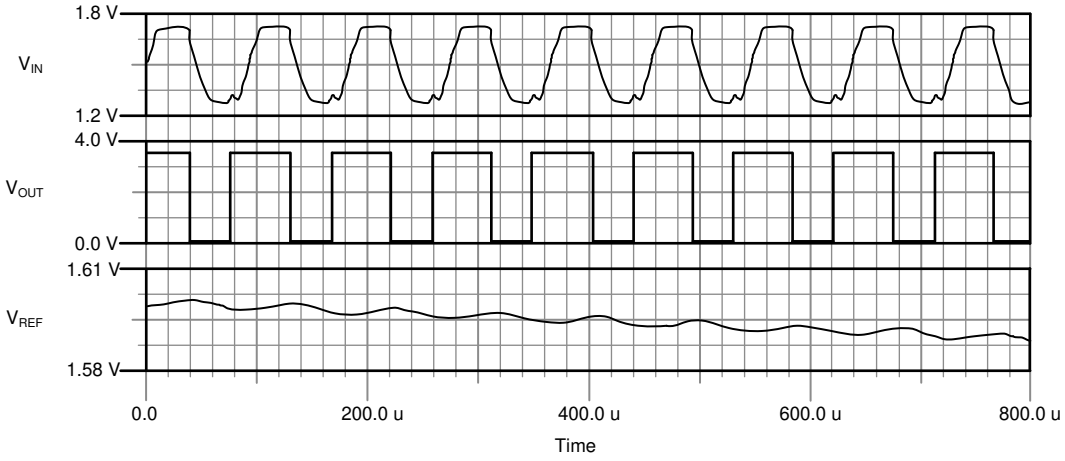


図 8-6. IR Receiver AFE Waveforms

8.2.3 Square-Wave Oscillator

A square-wave oscillator can be used as low-cost timing reference or system supervisory clock source.

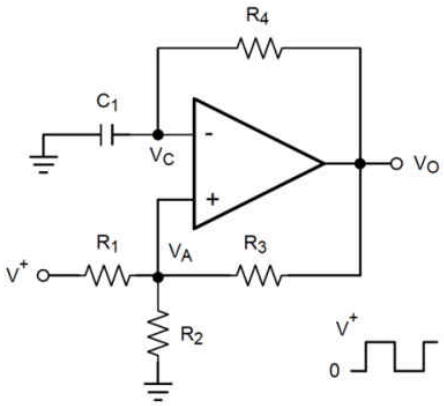


図 8-7. Square-Wave Oscillator

8.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by the propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help reduce BOM cost and board space.

8.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following section provides details to calculate these component values.

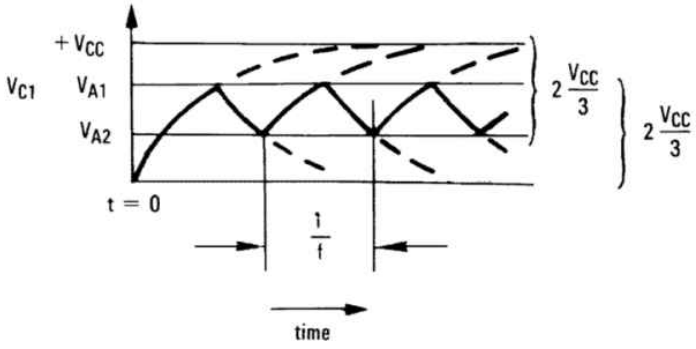


図 8-8. Square-Wave Oscillator Timing Thresholds

First consider the output of figure 図 8-7 is high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by 式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC}/\ 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by 式 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \tag{8}$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals the time duration from 2 V_{CC} / 3 to V_{CC} / 3 then back to 2 V_{CC} / 3, which is given by R_4C_1 × ln2 for each trip. Therefore, the total time duration is calculated as 2 R_4C_1 × ln2. The oscillation frequency can be obtained by 式 9:

$$f = 1/(2\ R4 \times C1 \times In2) \tag{9}$$

8.2.3.3 Application Curve

図 8-9 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100$ kΩ
- $C_1 = 100$ pF, $C_L = 20$ pF
- V+ = 5 V, V– = GND
- C_{stray} (not shown) from V_A to GND = 10 pF

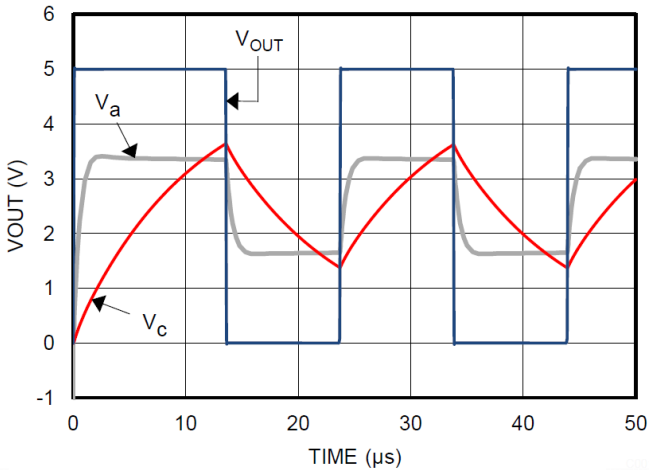


図 8-9. Square-Wave Oscillator Output Waveform

9 Power Supply Recommendations

The TLV703x-Q1 and TLV704x-Q1 have a recommended operating voltage range (V_S) of 1.6 V to 6.5 V. V_S is defined as V_{CC} – V_{EE}. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to V_{EE}.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

図 10-1 shows the typical connections for the TLV7031-Q1. To minimize supply noise, power supplies must be capacitively decoupled by a 0.1-µF ceramic capacitor in parallel with a 10-µF electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (the use of a ground plane) helps to maintain the specified performance of the TLV70x1-Q1 family.

For best results, maintain the following layout guidelines:

1. Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The top-side ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

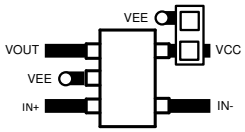


図 10-1. TLV7031-Q1 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV703x-Q1, TLV704x-Q1 device family. The DIP Adapter EVM can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7031QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7031	Samples
TLV7031QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GP	Samples
TLV7032QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2R4F	Samples
TLV7032QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7032	Samples
TLV7034QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7034Q	Samples
TLV7041QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7041	Samples
TLV7041QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GQ	Samples
TLV7042QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2R5F	Samples
TLV7042QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7042	Samples
TLV7044QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7044Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV7031-Q1, TLV7032-Q1, TLV7034-Q1, TLV7041-Q1, TLV7042-Q1, TLV7044-Q1 :

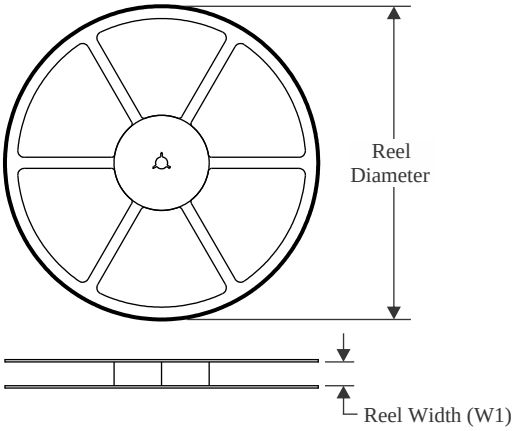
- Catalog : TLV7031, TLV7032, TLV7034, TLV7041, TLV7042, TLV7044

NOTE: Qualified Version Definitions:

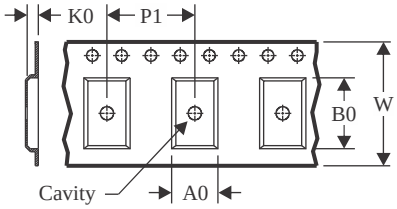
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

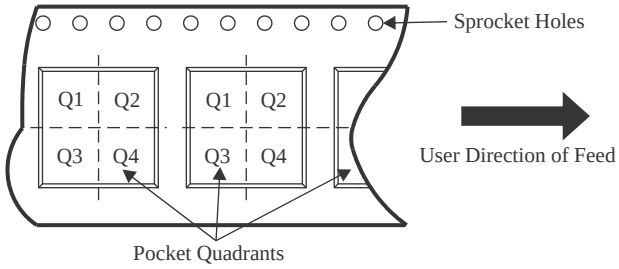


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

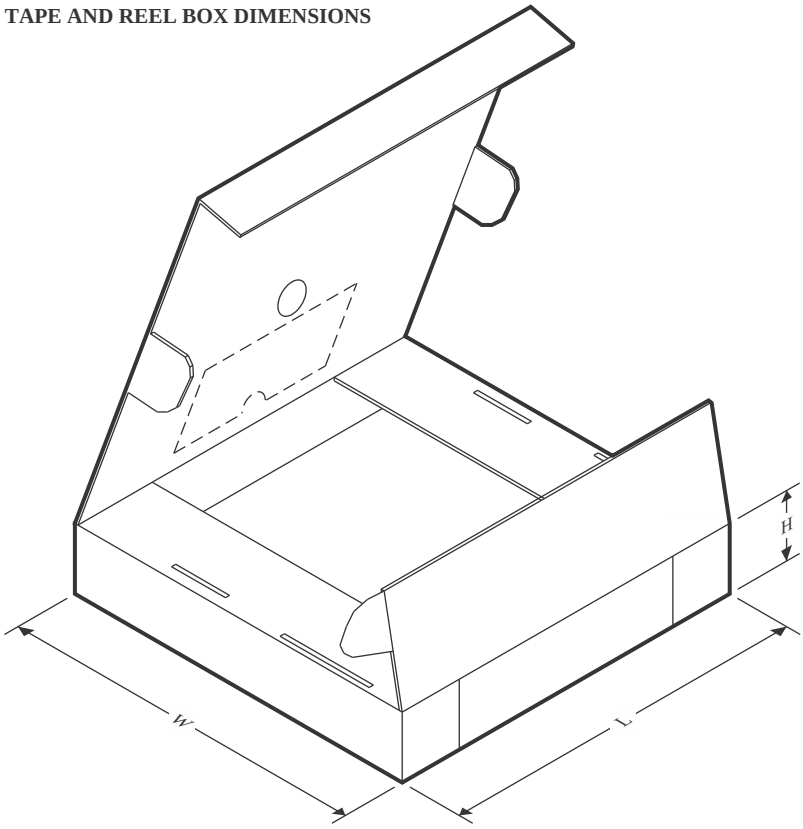
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7031QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV7031QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7032QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7032QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV7034QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV7041QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV7041QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7042QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7042QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV7044QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

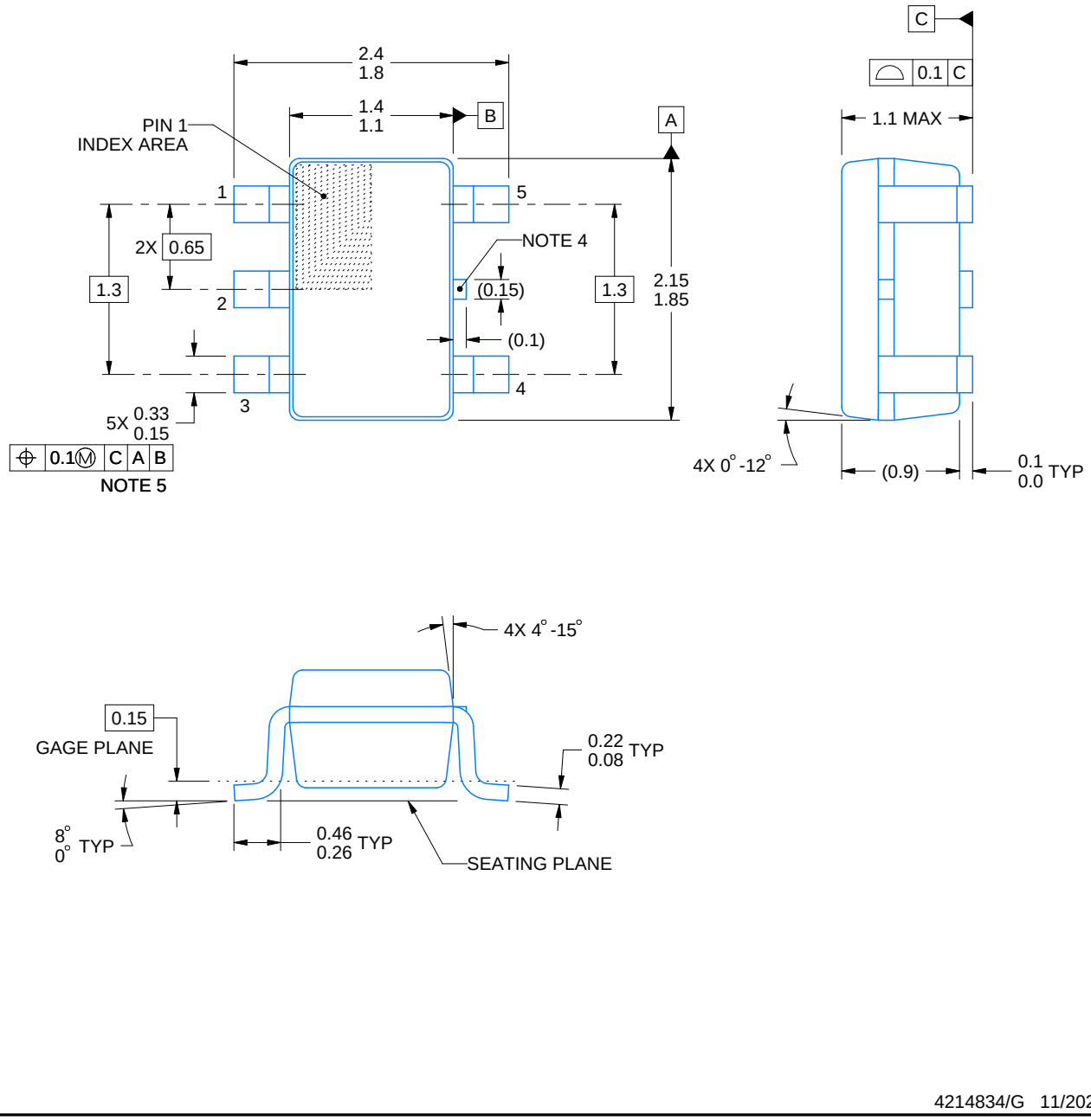
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7031QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7031QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7032QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7032QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV7034QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV7041QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7041QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7042QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7042QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV7044QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

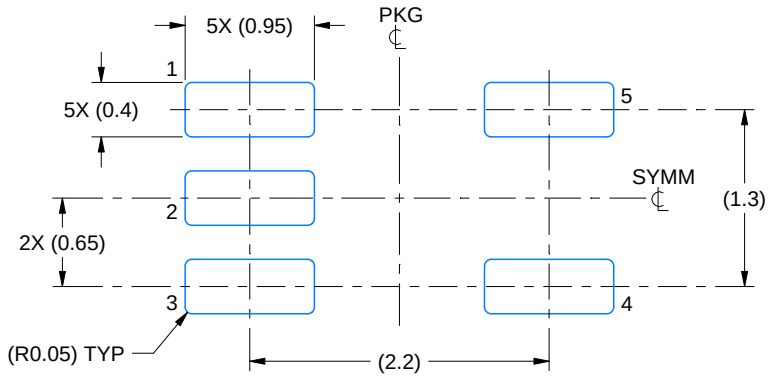
SMALL OUTLINE TRANSISTOR



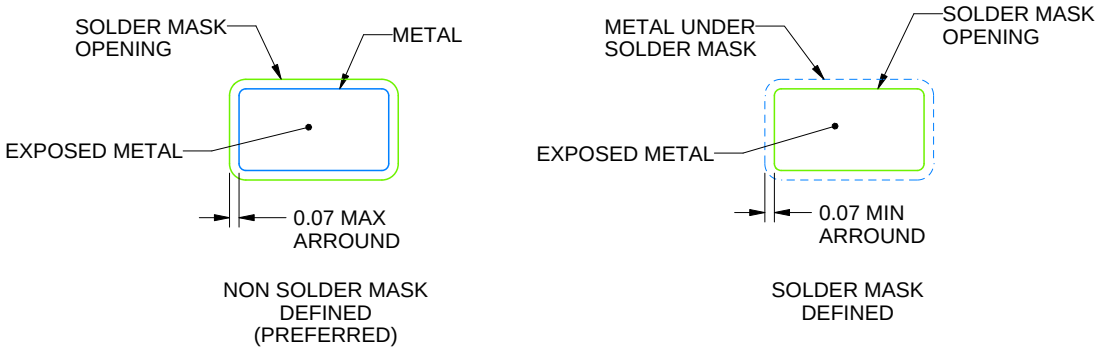
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

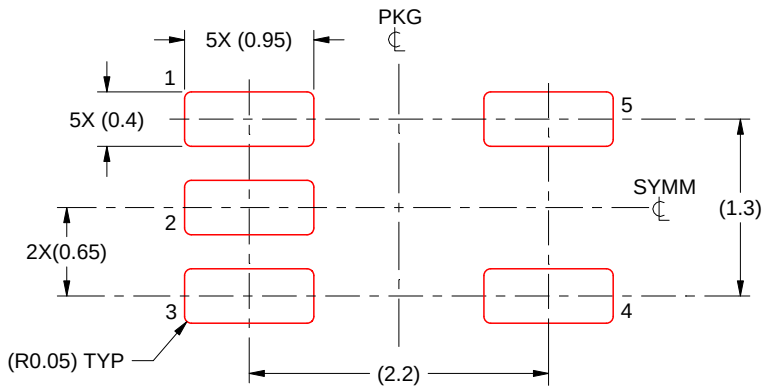


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

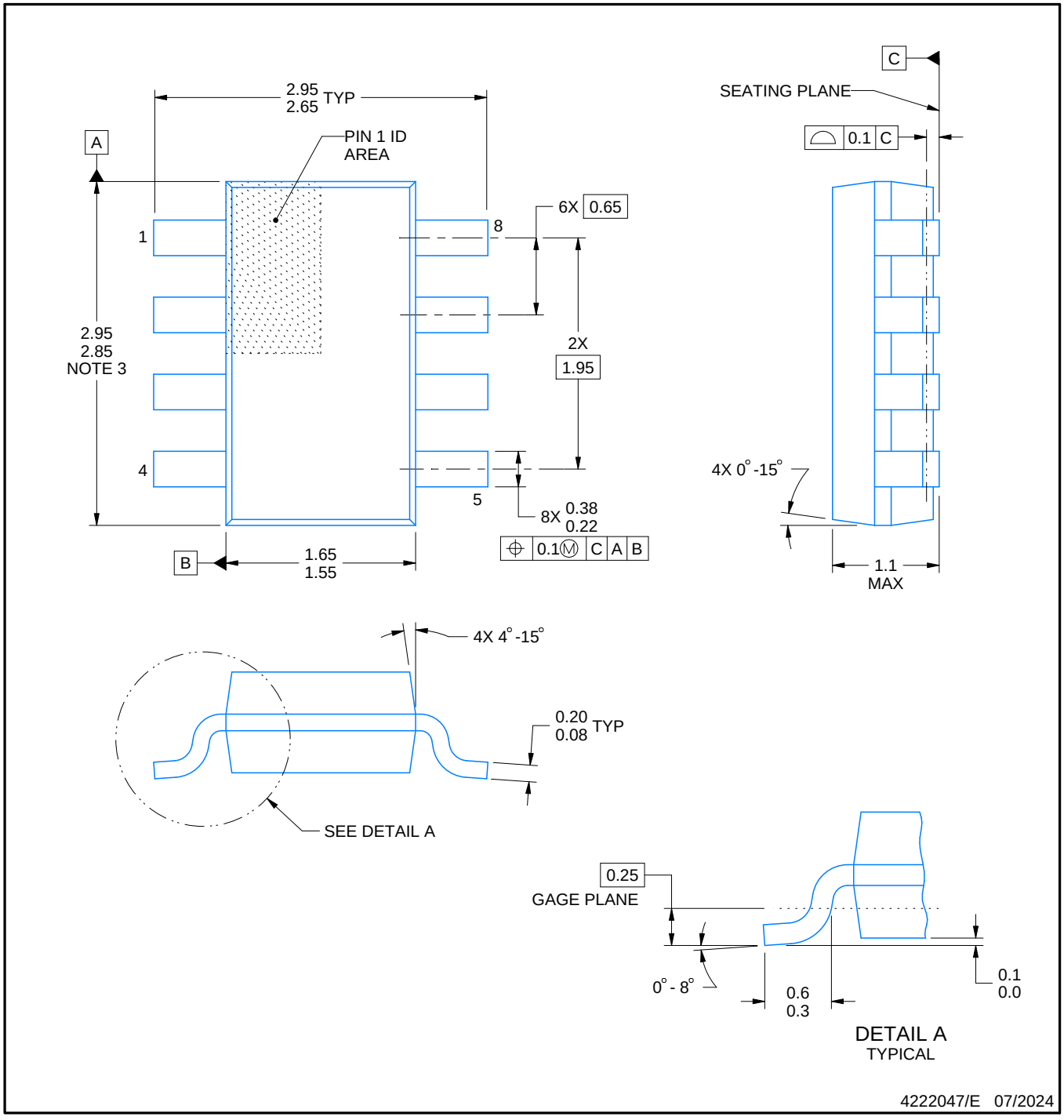
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

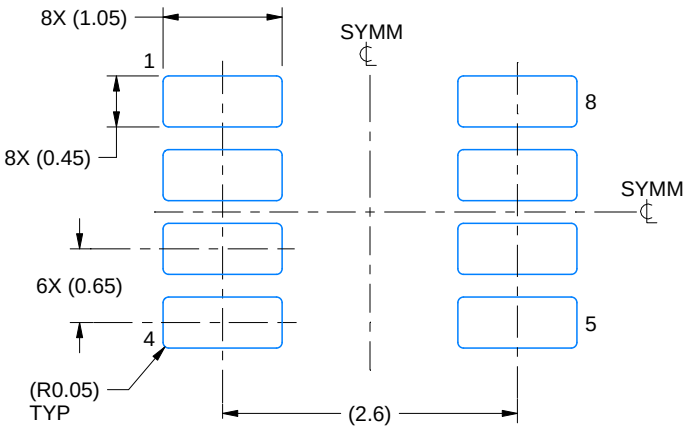
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

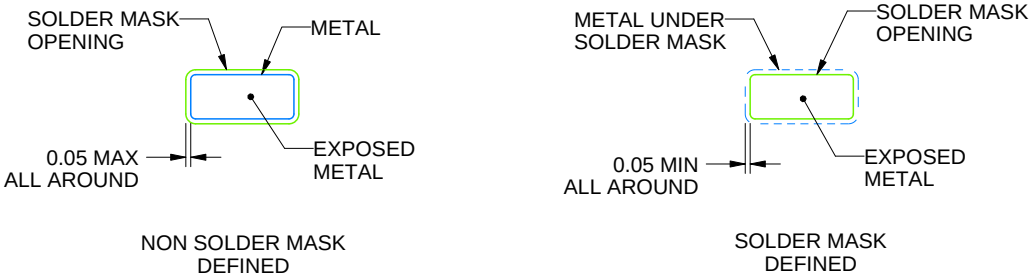


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

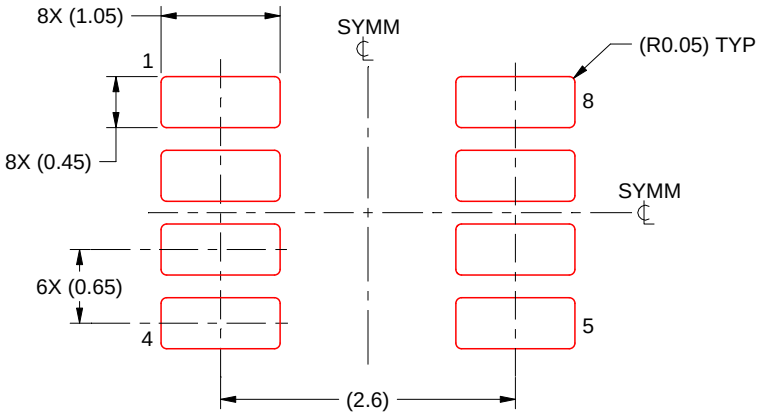
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

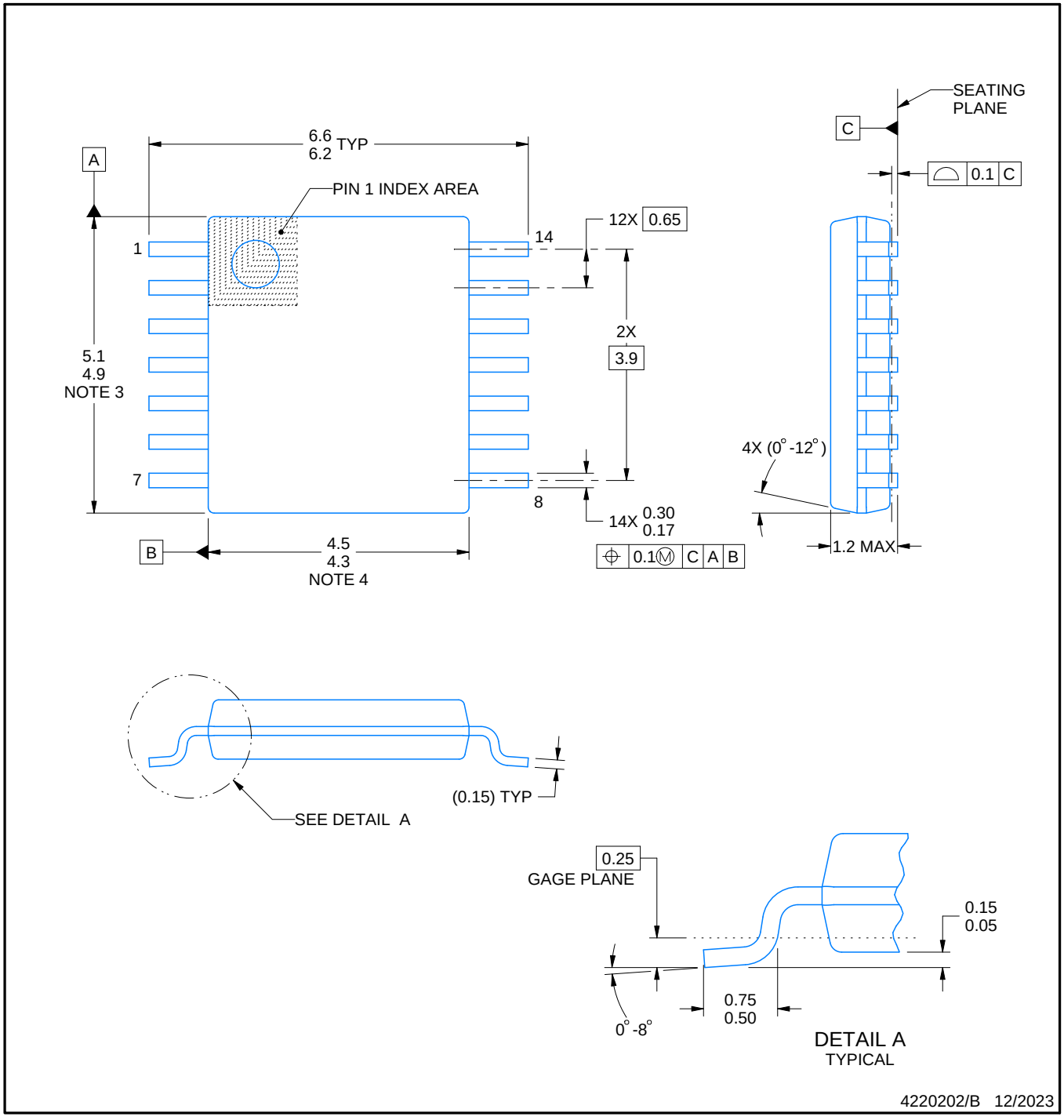
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

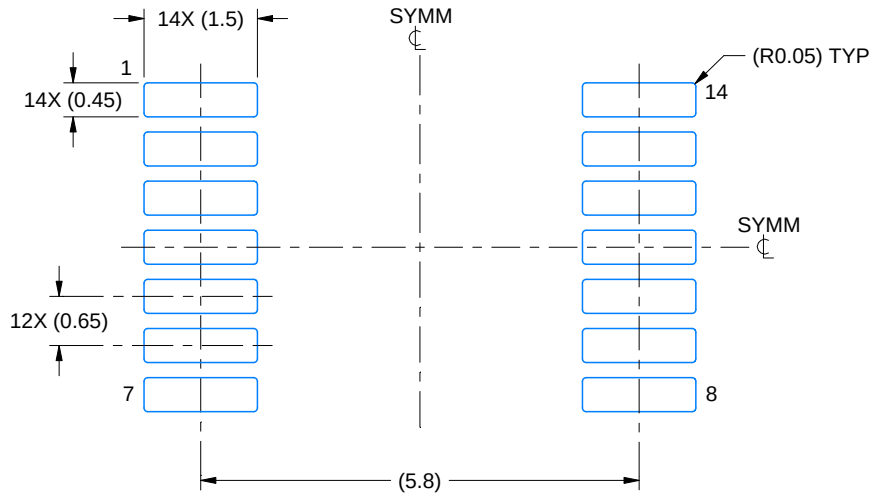
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

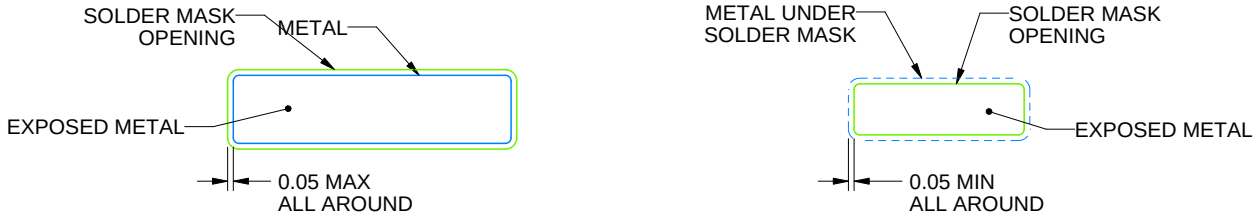


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

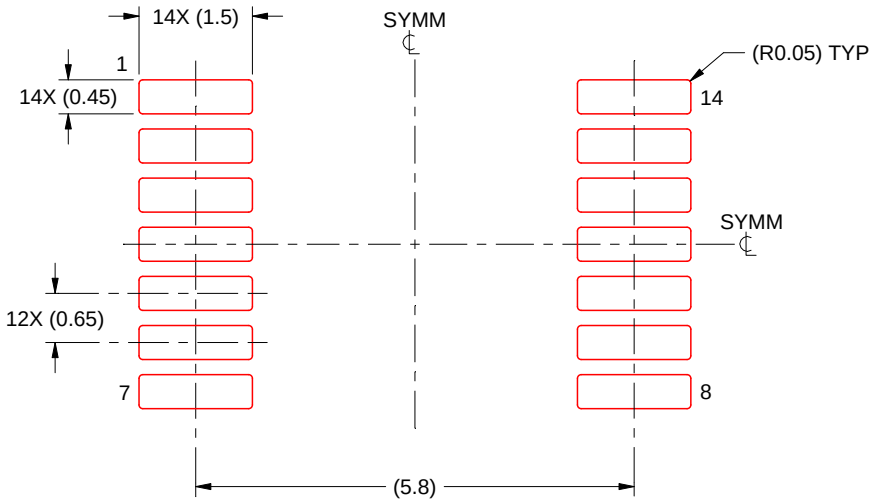


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

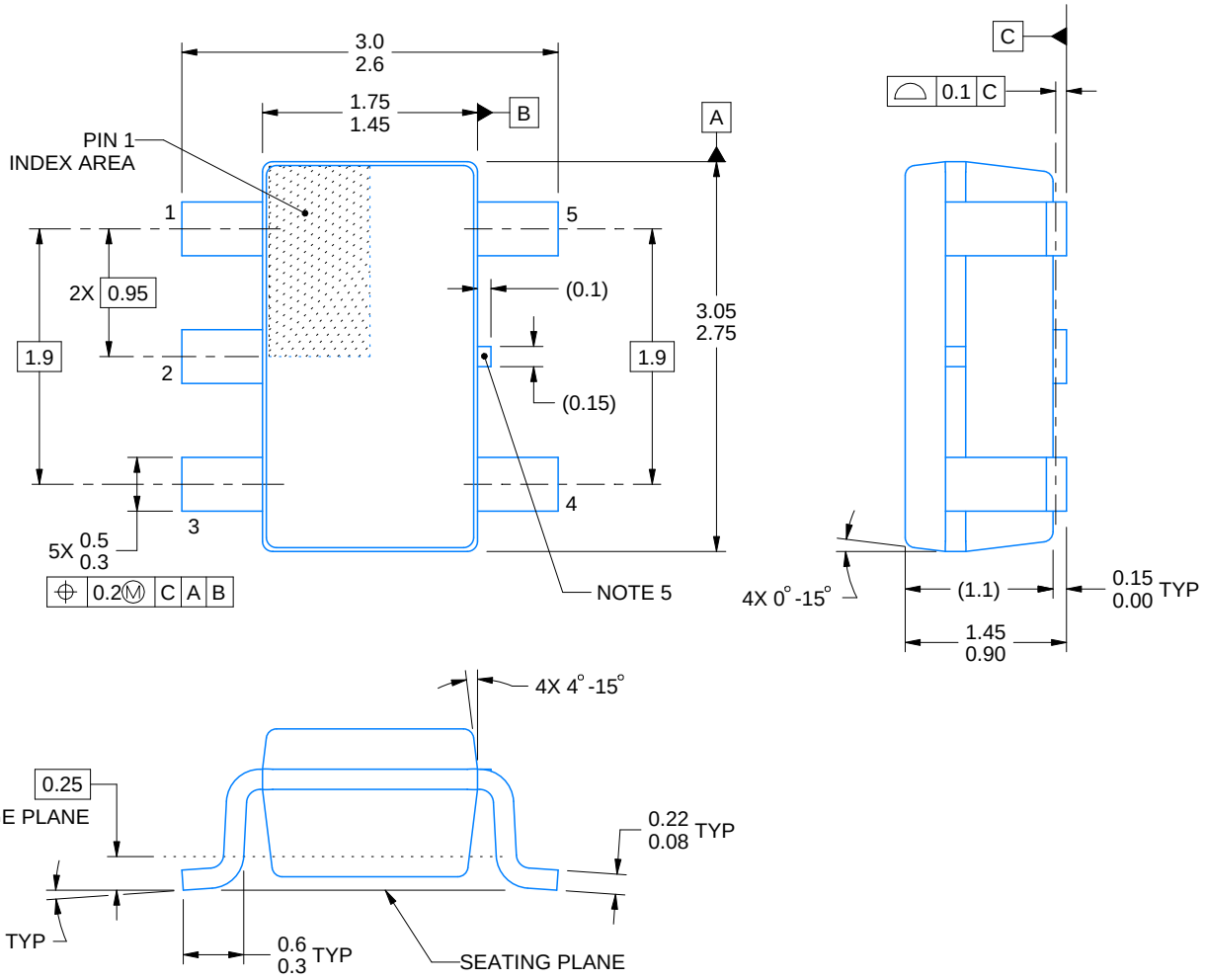
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

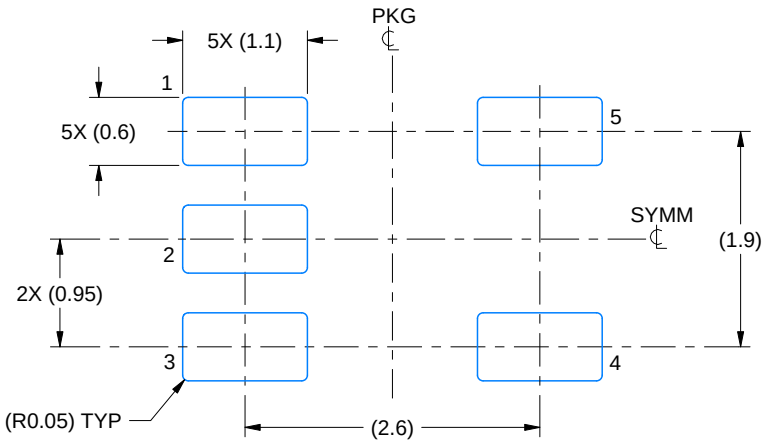
SMALL OUTLINE TRANSISTOR



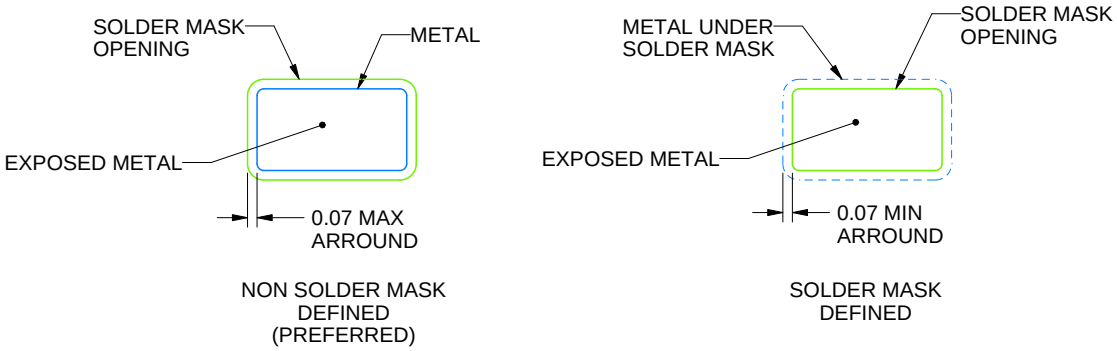
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

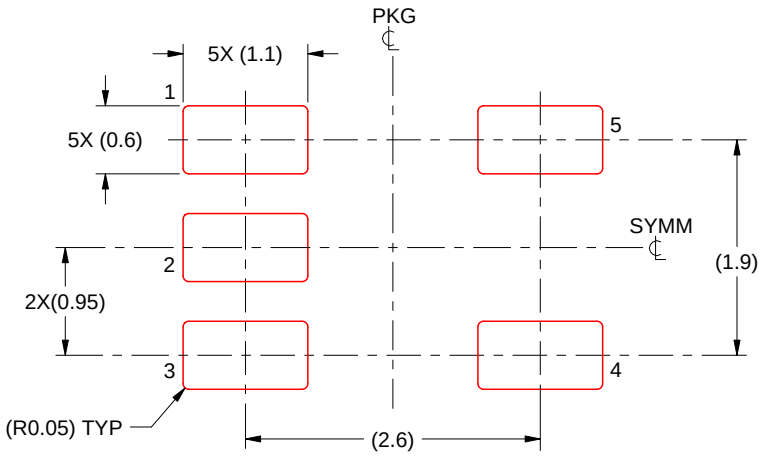


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

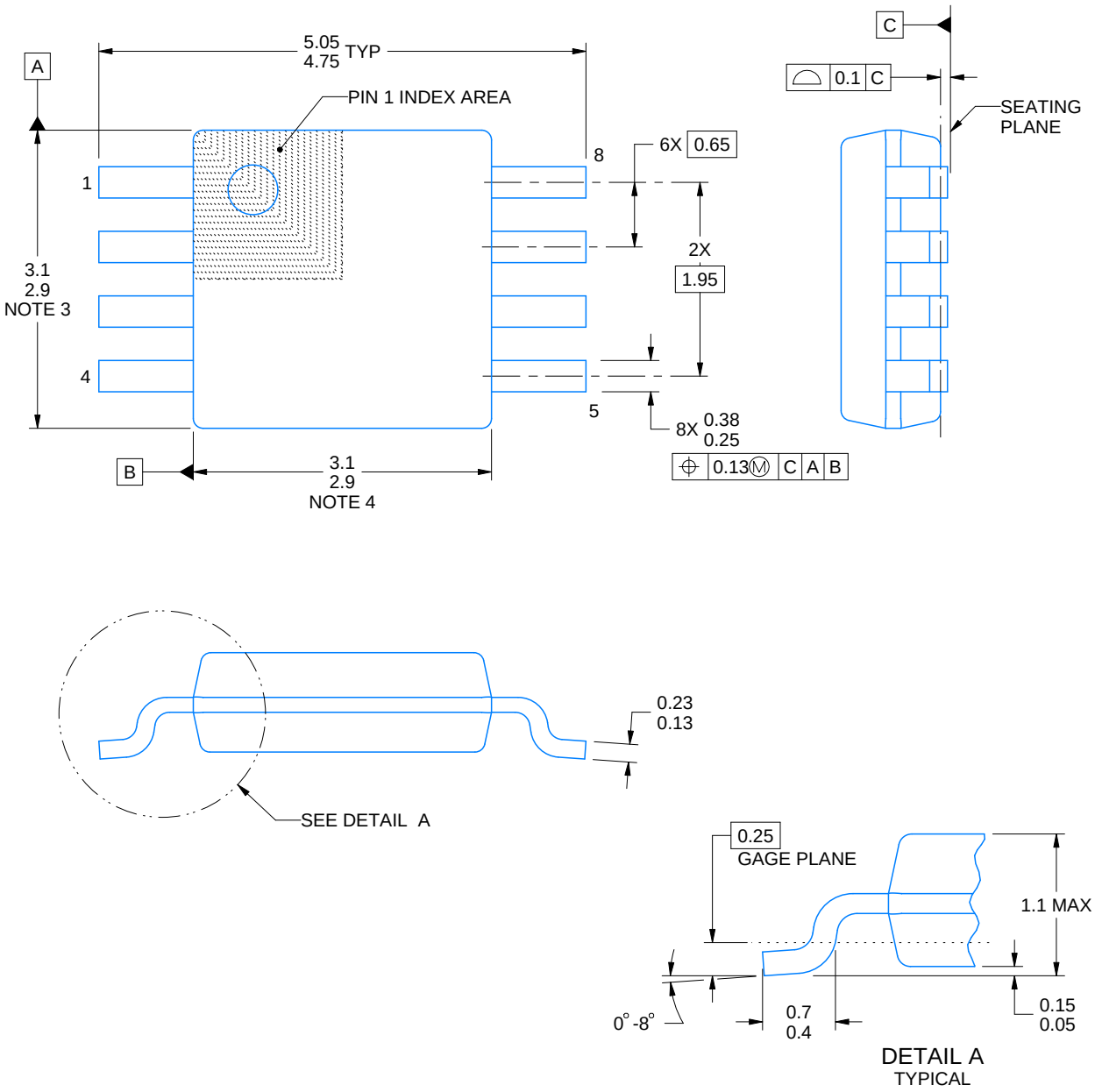
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

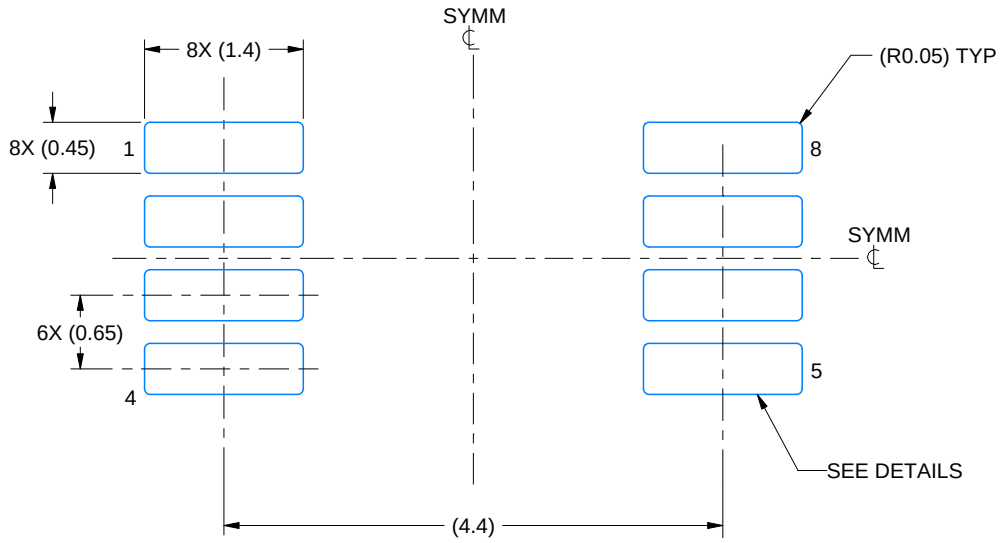
SMALL OUTLINE PACKAGE



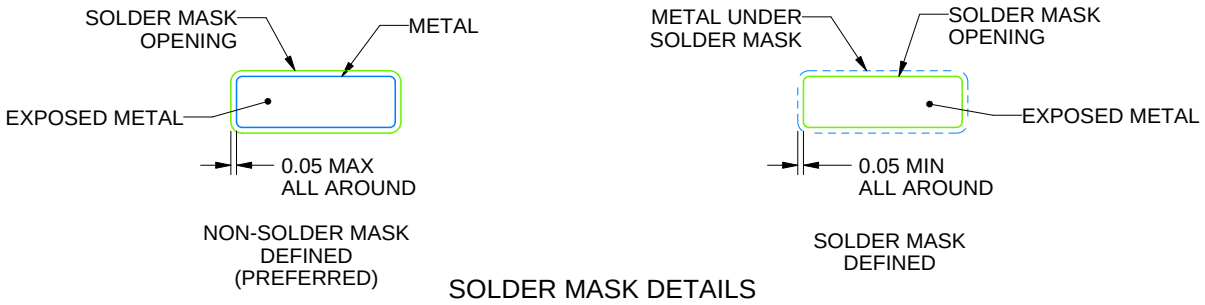
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

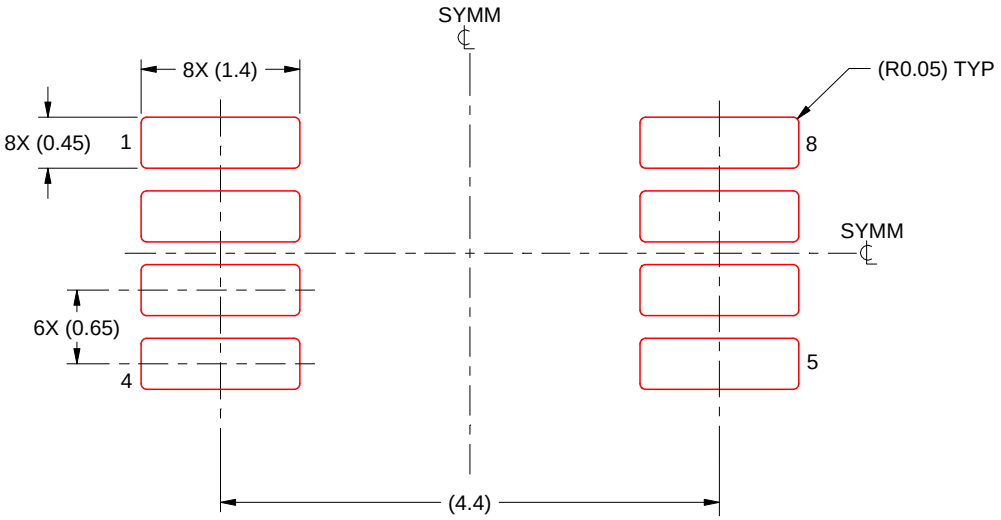


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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