

TLV6710 400mV基準電圧搭載、Micropower、36Vのウィンドウ・コンパレータ

1 特長

- 広い電源電圧範囲: 1.8V~36V
- スレッシュホールドを変更可能: 最低400mV
- スレッシュホールドの高い精度
 - 0.25% (標準値)
 - 温度範囲全体で最大0.75%
- 低い静止電流: 7 μ A (標準値)
- オープン・ドレイン出力
- 内部ヒステリシス: 5.5mV (標準値)
- 温度範囲: -40°C~125°C
- パッケージ: Thin SOT-23-6

2 アプリケーション

- ノートPCおよびタブレット
- スマートフォン
- デジタル・カメラ
- ビデオゲーム・コントローラ
- リレーおよびサーキット・ブレーカ
- ポータブル医療機器
- ドアまたは窓のセンサ
- 携帯用およびバッテリー駆動の製品

3 概要

TLV6710は、1.8V~36Vの電源電圧範囲で動作する高電圧ウィンドウ・コンパレータです。このデバイスには、400mVの内部基準電圧付きの2つの高精度コンパレータと、25V定格の2つのオープン・ドレイン出力が搭載されています。TLV6710はウィンドウ・コンパレータとしても、2つの独立したコンパレータとしても使用でき、監視対象の電圧は外付け抵抗により設定できます。

OUTAは、INA+の電圧が($V_{ITP} - V_{HYS}$)より低くなるとLOWに駆動され、対応するスレッシュホールド(V_{ITP})より高い電圧に戻るとHIGHに復帰します。OUTBは、INB-の電圧が V_{ITP} より高くなるとLOWに駆動され、対応するスレッシュホールド($V_{ITP} - V_{HYS}$)より低い電圧に戻るとHIGHに復帰します。TLV6710のコンパレータは両方とも、短時間のグリッチを除去するためヒステリシスが組み込まれているので、誤ったトリガが発生せず、安定した出力動作が確保されます。

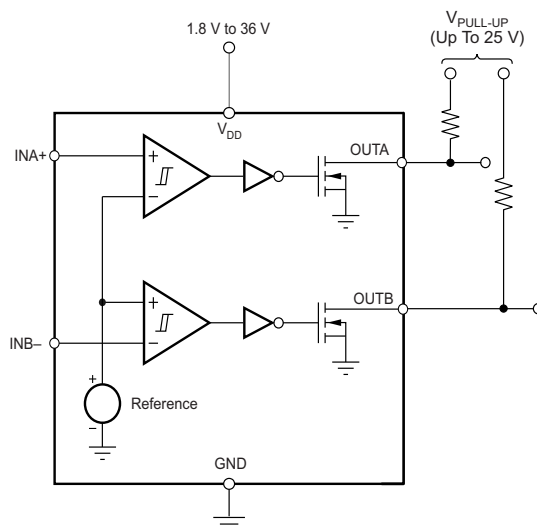
TLV6710はThin SOT-23-6パッケージで供給され、-40°C~+125°Cの接合部温度範囲で動作が規定されています。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TLV6710	SOT-23 (6)	2.90mmx1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

ブロック概略図



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4 改訂履歴

Revision A (April 2018) から Revision B に変更

Page

- 表紙の「ブロック概略図」、「概要」、「アプリケーション情報」セクションで、出力の説明のテキストを36Vから25Vに 1

2018年1月発行のものから更新

Page

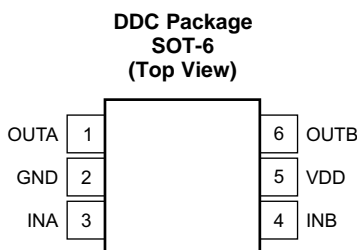
- 事前情報から量産データに 1

5 デバイス比較表

表 1. TLV67xx統合コンパレータ・ファミリ

型番	構成	動作電圧範囲	温度範囲全体にわたるスレッシュホールド精度
TLV6700	ウィンドウ	1.8V~18V	1%
TLV6703	非反転シングルチャネル	1.8V~18V	1%
TLV6710	ウィンドウ	1.8V~36V	0.75%
TLV6713	非反転シングルチャネル	1.8V~36V	0.75%

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
INA	3	I	Comparator A input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage $V_{IT-(INA)}$, OUTA is driven low.
INB	4	I	Comparator B input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage $V_{IT+(INB)}$, OUTB is driven low.
OUTA	1	O	INA comparator open-drain output. OUTA is driven low when the voltage at this comparator is less than $V_{IT-(INA)}$. The output goes high when the sense voltage rises above $V_{IT+(INA)}$.
OUTB	6	O	INB comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds $V_{IT+(INB)}$. The output goes high when the sense voltage falls below $V_{IT-(INB)}$.
VDD	5	I	Supply voltage input. Connect a 1.8-V to 36-V supply to VDD to power the device. It is good analog design practice to place a 0.1- μ F ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range, unless otherwise noted.⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	V_{DD}	-0.3	+40	V
	V_{OUTA}, V_{OUTB}	-0.3	+28	V
	V_{INA}, V_{INB}	-0.3	+7	V
Current	Output pin current		40	mA
Temperature	Operating junction, T_J	-40	+125	°C
	Storage temperature, T_{stg}	-65	+150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.8		36	V
V_{INA}, V_{INB}	Input pin voltage	0		1.7	V
V_{OUTA}, V_{OUTB}	Output pin voltage	0		25	V
I_{OUTA}, I_{OUTB}	Output pin current	0		10	mA
T_J	Junction temperature	-40	+25	+125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV6710	UNITS
		DDC (SOT)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

7.5 Electrical Characteristics

Over the operating temperature range of $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} < 36\text{ V}$, and pullup resistors $RP_{1,2} = 100\text{ k}\Omega$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$ and $V_{DD} = 12\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		36	V
$V_{(POR)}$	Power-on reset voltage ⁽¹⁾	$V_{OL} \leq 0.2\text{ V}$			0.8	V
$V_{IT-(INA)}$	INA pin negative input threshold voltage	$V_{DD} = 1.8\text{ V to } 36\text{ V}$	397	400	403	mV
$V_{IT+(INA)}$	INA pin positive input threshold voltage	$V_{DD} = 1.8\text{ V to } 36\text{ V}$	400	405.5	413	mV
$V_{HYS(INA)}$	INA pin hysteresis voltage ($HYS = V_{IT+(INA)} - V_{IT-(INA)}$)		2	5.5	12	mV
$V_{IT-(INB)}$	INB pin negative input threshold voltage	$V_{DD} = 1.8\text{ V to } 36\text{ V}$	387	394.5	400	mV
$V_{IT+(INB)}$	INB pin positive input threshold voltage	$V_{DD} = 1.8\text{ V to } 36\text{ V}$	397	400	403	mV
$V_{HYS(INB)}$	INB pin hysteresis voltage ($HYS = V_{IT+(INB)} - V_{IT-(INB)}$)		2	5.2	12	mV
V_{OL}	Low-level output voltage	$V_{DD} = 1.8\text{ V}, I_{OUT} = 3\text{ mA}$		130	250	mV
		$V_{DD} = 5\text{ V}, I_{OUT} = 5\text{ mA}$		150	250	mV
I_{IN}	Input current (at INA, INB pins)	$V_{DD} = 1.8\text{ V and } 36\text{ V}, V_{INA}, V_{INB} = 6.5\text{ V}$	-25	+1	+25	nA
		$V_{DD} = 1.8\text{ V and } 36\text{ V}, V_{INA}, V_{INB} = 0.1\text{ V}$	-15	+1	+15	nA
$I_{D(leak)}$	Open-drain output leakage current	$V_{DD} = 1.8\text{ V and } 36\text{ V}, V_{OUT} = 25\text{ V}$		10	300	nA
I_{DD}	Supply current	$V_{DD} = 1.8\text{ V} - 36\text{ V}$		8	11	μA
UVLO	Undervoltage lockout ⁽²⁾	V_{DD} falling	1.3	1.5	1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)} > 15\text{ }\mu\text{s/V}$. If less than $V_{(POR)}$, the output is undetermined.

(2) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined if less than $V_{(POR)}$.

7.6 Timing Requirements

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay ⁽¹⁾ $V_{DD} = 24\text{ V}$, $\pm 10\text{-mV}$ input overdrive, $R_L = 100\text{ k}\Omega$, $V_{OH} = 0.9 \times V_{DD}$, $V_{OL} = 250\text{ mV}$		9.9		μs
$t_{pd(LH)}$	Low-to-high propagation delay ⁽¹⁾ $V_{DD} = 24\text{ V}$, $\pm 10\text{-mV}$ input overdrive, $R_L = 100\text{ k}\Omega$, $V_{OH} = 0.9 \times V_{DD}$, $V_{OL} = 250\text{ mV}$		28.1		μs
$t_{d(start)}$ ⁽²⁾	Startup delay $V_{DD} = 5\text{ V}$		155		μs
t_r	Output rise time $V_{DD} = 12\text{ V}$, 10-mV input overdrive, $R_L = 100\text{ k}\Omega$, $C_L = 10\text{ pF}$, $V_O = (0.1\text{ to }0.9) \times V_{DD}$		2.7		μs
t_f	Output fall time $V_{DD} = 12\text{ V}$, 10-mV input overdrive, $R_L = 100\text{ k}\Omega$, $C_L = 10\text{ pF}$, $V_O = (0.9\text{ to }0.1) \times V_{DD}$		0.12		μs

- (1) High-to-low and low-to-high refers to the transition at the input pins (INA and INB).
- (2) During power on, V_{DD} must exceed 1.8 V for at least 150 μs (typ) before the output state reflects the input condition.

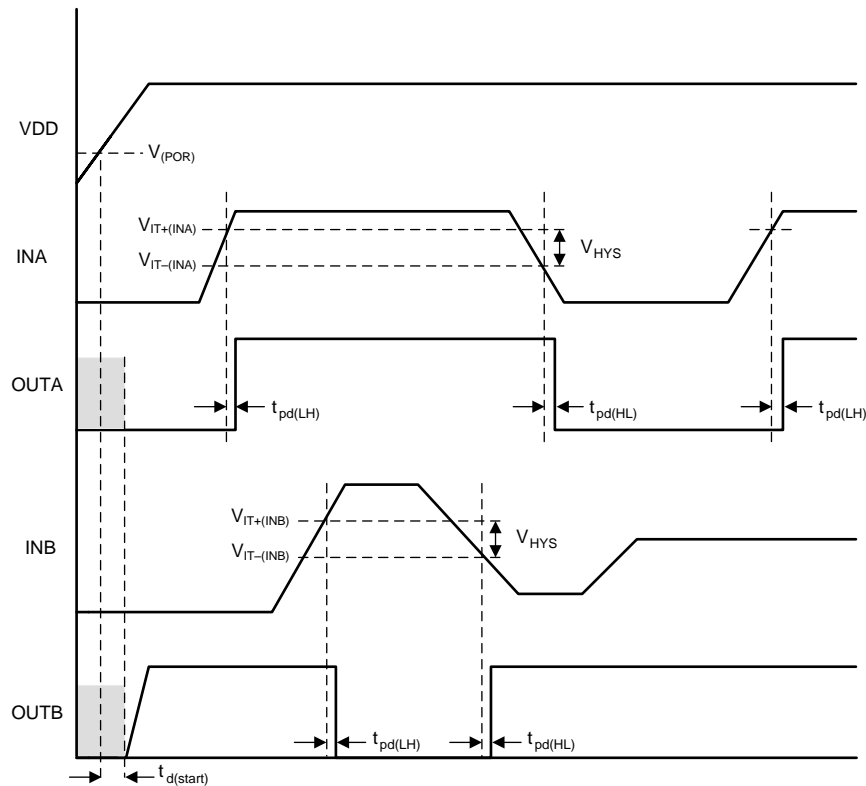


Figure 1. Timing Diagram

7.7 Typical Characteristics

At $T_J = 25^\circ\text{C}$ and $V_{DD} = 12\text{ V}$, unless otherwise noted.

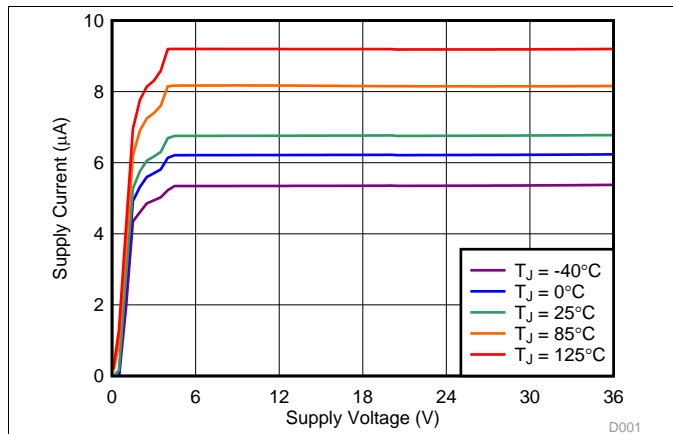


Figure 2. Supply Current vs Supply Voltage

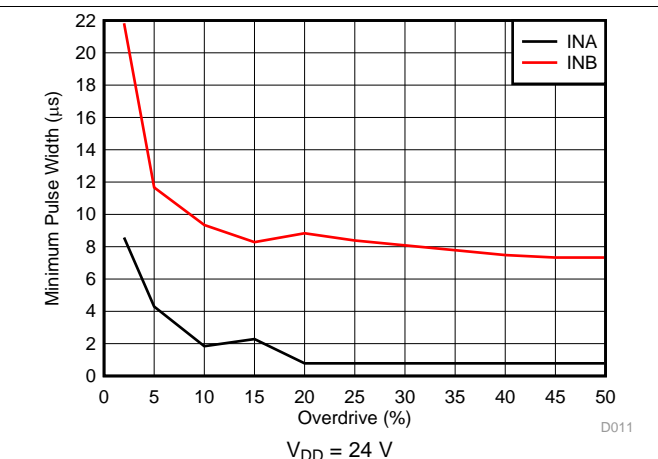


Figure 3. Minimum Pulse Duration vs Threshold Overdrive Voltage⁽¹⁾ (1)

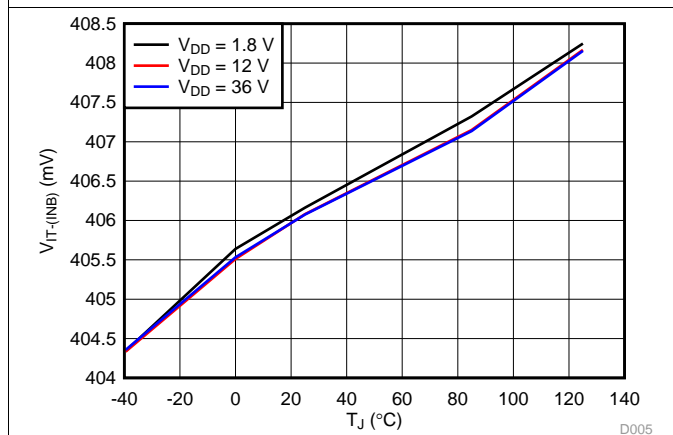


Figure 4. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) vs Temperature

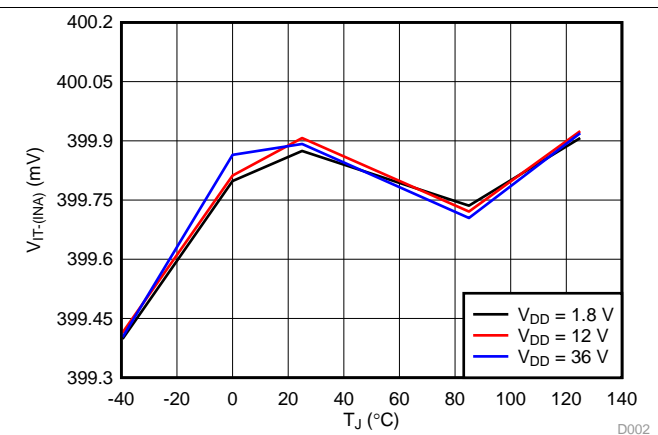


Figure 5. INA Negative Input Threshold Voltage ($V_{IT-(INA)}$) vs Temperature

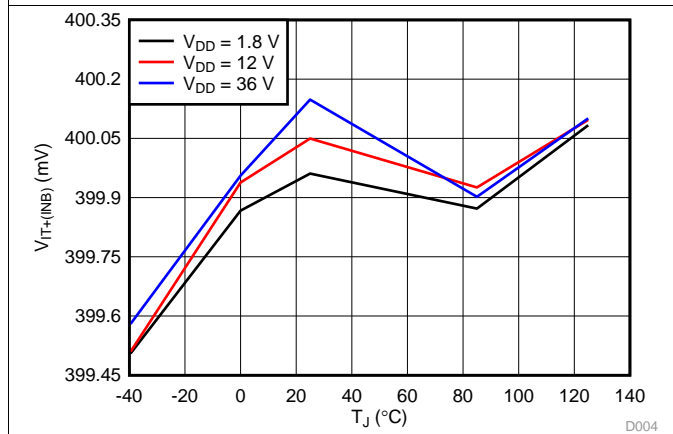


Figure 6. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) vs Temperature

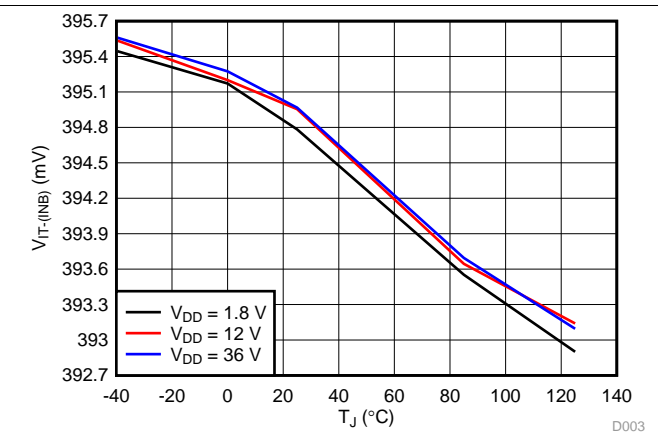


Figure 7. INB Negative Input Threshold Voltage ($V_{IT-(INB)}$) vs Temperature

(1) Minimum pulse duration required to trigger output high-to-low transition. INA = negative spike below V_{IT-} and INB = positive spike above V_{IT+} .

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$ and $V_{DD} = 12\text{ V}$, unless otherwise noted.

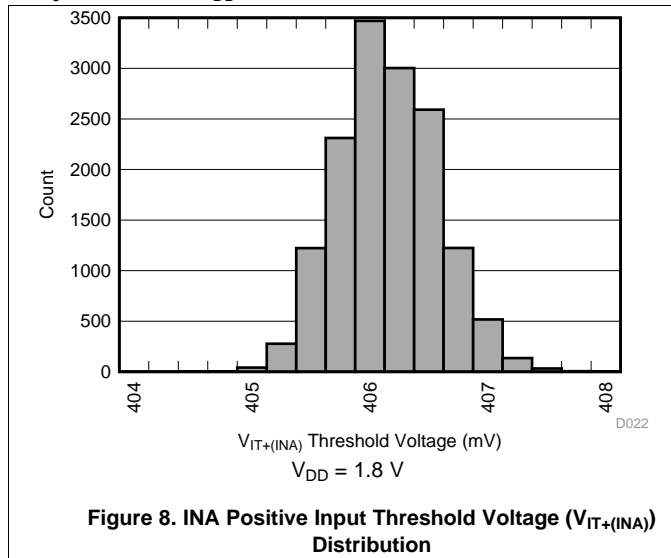


Figure 8. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) Distribution

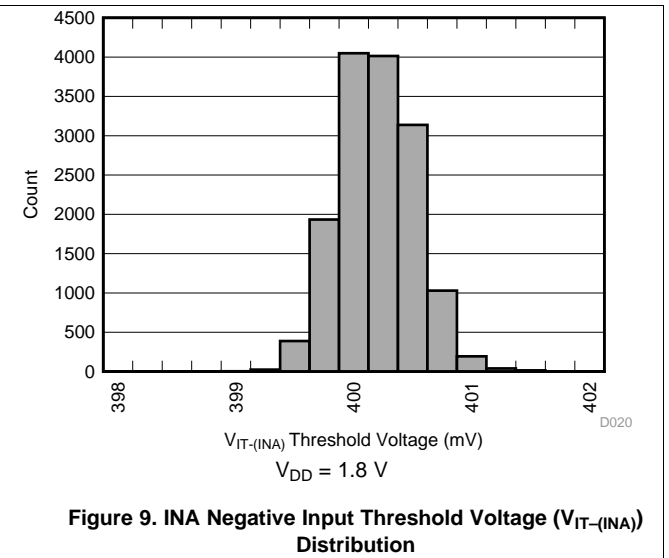


Figure 9. INA Negative Input Threshold Voltage ($V_{IT-(INA)}$) Distribution

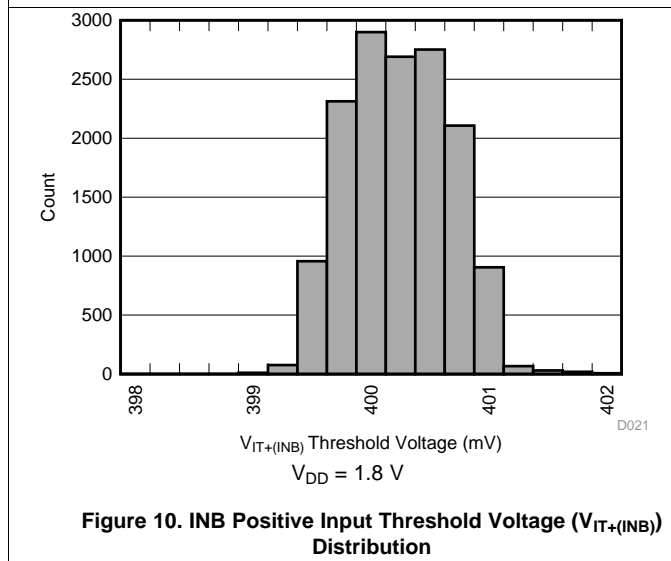


Figure 10. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) Distribution

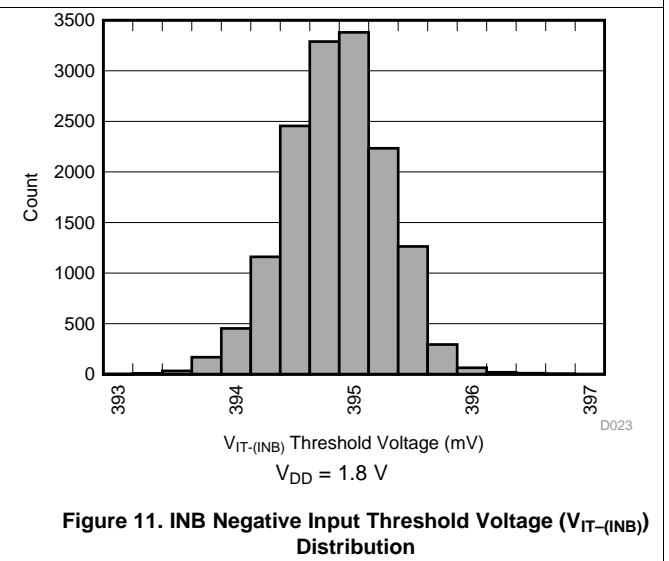


Figure 11. INB Negative Input Threshold Voltage ($V_{IT-(INB)}$) Distribution

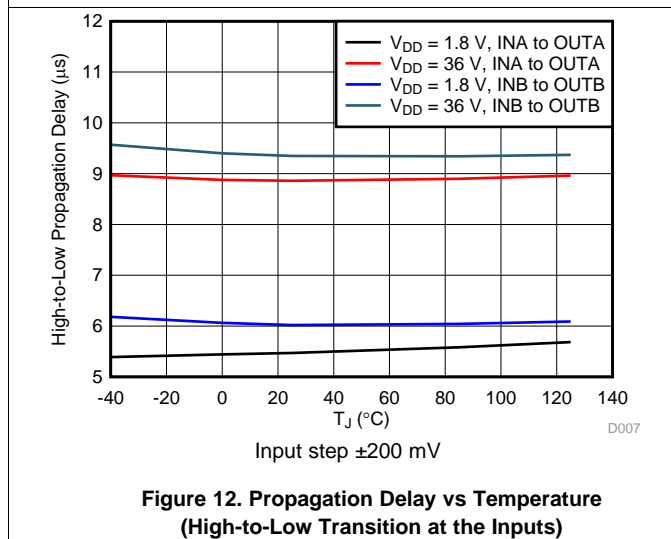


Figure 12. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

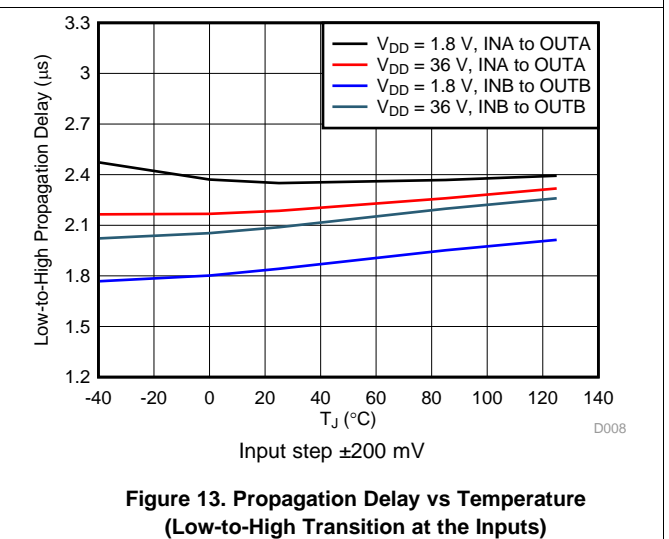


Figure 13. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$ and $V_{DD} = 12\text{ V}$, unless otherwise noted.

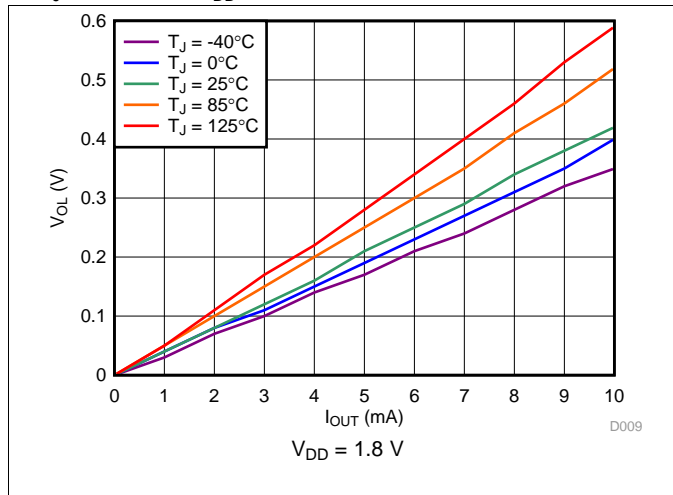


Figure 14. Output Voltage Low vs Output Sink Current

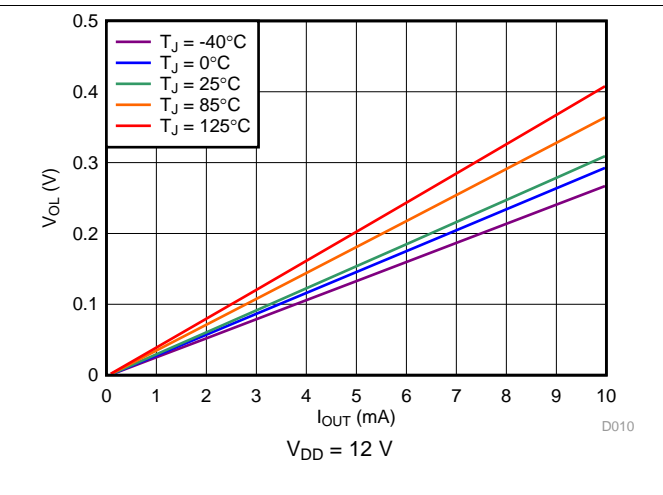


Figure 15. Output Voltage Low vs Output Sink Current

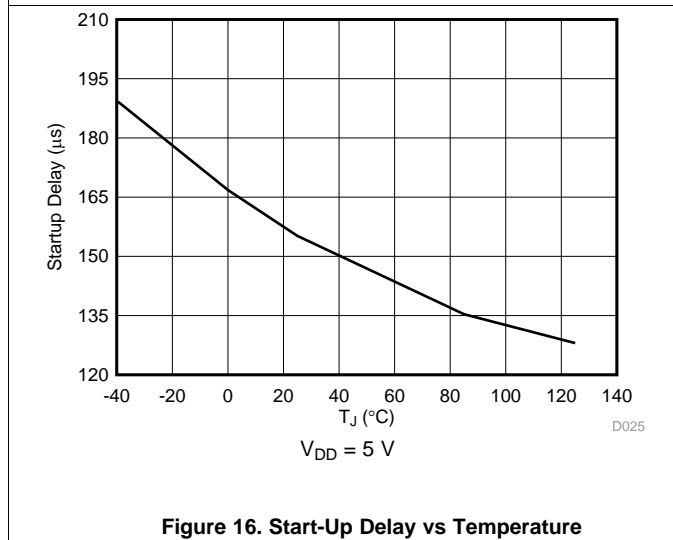


Figure 16. Start-Up Delay vs Temperature

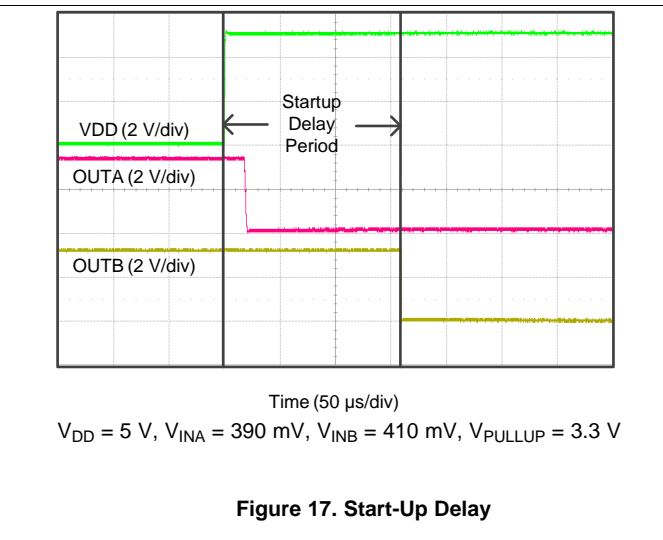


Figure 17. Start-Up Delay

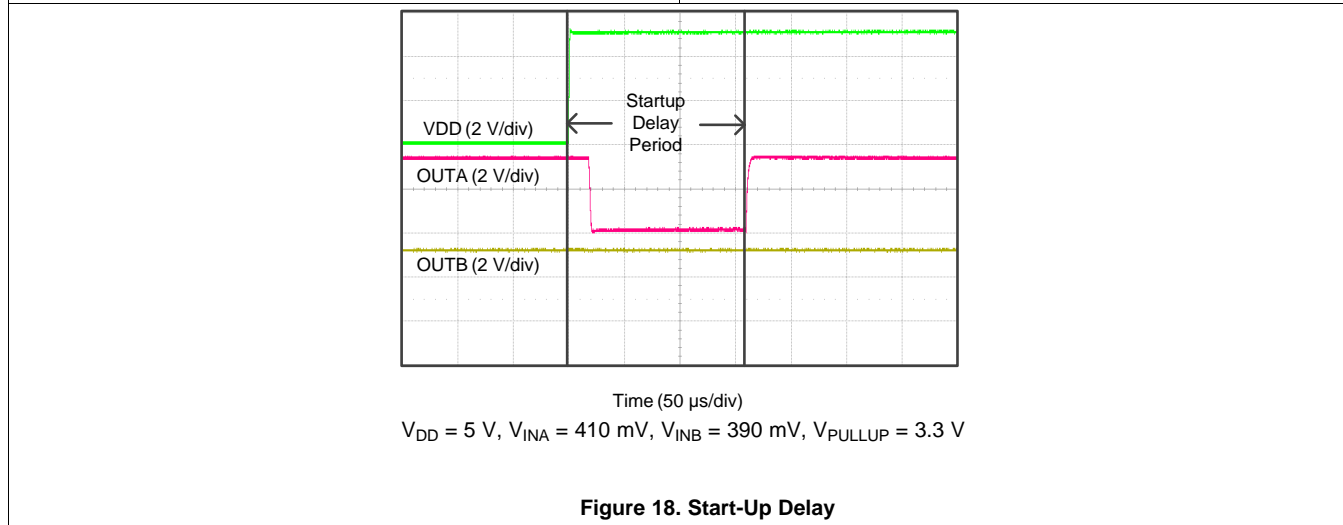


Figure 18. Start-Up Delay

8 Detailed Description

8.1 Overview

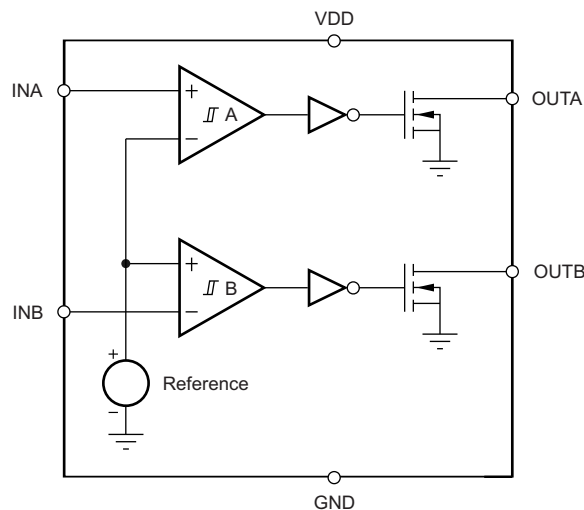
The TLV6710 combines two comparators (referred to as A and B) and a precision reference for overvoltage and undervoltage detection. The TLV6710 features a wide supply voltage range (1.8 V to 36 V) and high-accuracy window threshold voltages of 400 mV (0.75% over temperature) with built-in hysteresis. The outputs are rated to 25 V and can sink up to 10 mA.

Set each input pin (INA, INB) to monitor any voltage above 0.4 V by using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. To form a window comparator, use the two input pins and three resistors (see the [Window Comparator Considerations](#) section). In this configuration, the TLV6710 is designed to assert the output signals when the monitored voltage is within the window band. Each input can also be used independently. The relationship between the inputs and the outputs is shown in [Table 2](#). Broad voltage thresholds are supported that enable the device to be used in a wide array of applications.

Table 2. Truth Table

CONDITION	OUTPUT	OUTPUT STATE
$INA > V_{IT+(INA)}$	OUTA high	Output A high impedance
$INA < V_{IT-(INA)}$	OUTA low	Output A sinking
$INB > V_{IT+(INB)}$	OUTB low	Output B sinking
$INB < V_{IT-(INB)}$	OUTB high	Output B high impedance

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Inputs (INA, INB)

The TLV6710 combines two comparators with a precision reference voltage. Each comparator has one external input; the other input is connected to the internal reference. The rising threshold on INB and the falling threshold on INA are designed and trimmed to be equal to the reference voltage (400 mV). This configuration optimizes the device accuracy when used as a window comparator. Both comparators also have built-in hysteresis that proves immunity to noise and ensures stable operation.

The comparator inputs swings from ground to 1.7 V (7.0 V absolute maximum), regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for noisy applications in order to reduce sensitivity to transient voltage changes on the monitored signal.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA voltage drops below $V_{IT-(INA)}$. When the voltage exceeds $V_{IT+(INA)}$, OUTA goes to a high-impedance state; see [Figure 1](#).

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB exceeds $V_{IT+(INB)}$. When the voltage drops below $V_{IT-(INB)}$ OUTB goes to a high-impedance state; see [Figure 1](#). Together, these two comparators form a window-detection function as described in the [Window Comparator Considerations](#) section.

8.3.2 Outputs (OUTA, OUTB)

In a typical TLV6710 application, the outputs are connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6710 provides two open-drain outputs (OUTA and OUTB); use pullup resistors to hold these lines high when the output goes to a high-impedance state. Connect pullup resistors to the proper voltage rails to enable the outputs to be connected to other devices at correct interface voltage levels. The TLV6710 outputs can be pulled up to 25 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by V_{OL} , output capacitive loading, and output leakage current ($I_{D(leak)}$). These values are specified in the [Electrical Characteristics](#) table. Use wired-OR logic to merge OUTA and OUTB into one logic signal.

[Table 2](#) and the [Inputs \(INA, INB\)](#) section describe how the outputs are asserted or high impedance. See [Figure 1](#) for a timing diagram that describes the relationship between threshold voltages and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation ($V_{DD} > UVLO$)

When the voltage on VDD is greater than 1.8 V for at least 155 μ s, the OUTA and OUTB signals correspond to the voltage on INA and INB as listed in [Table 2](#).

8.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} < UVLO$)

When the voltage on VDD is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA and INB.

8.4.3 Power On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are in a high-impedance state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV6710 device is a wide-supply voltage window comparator that operates over a V_{DD} range of 1.8 V to 36 V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 25 V for overvoltage and undervoltage detection. The device can be used either as a window comparator or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

9.1.1 Window Comparator Considerations

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as shown in Figure 19 and Figure 20. The input pins can monitor any system voltage above 400 mV with the use of a resistor divider network. INA and INB monitor for undervoltage and overvoltage conditions, respectively.

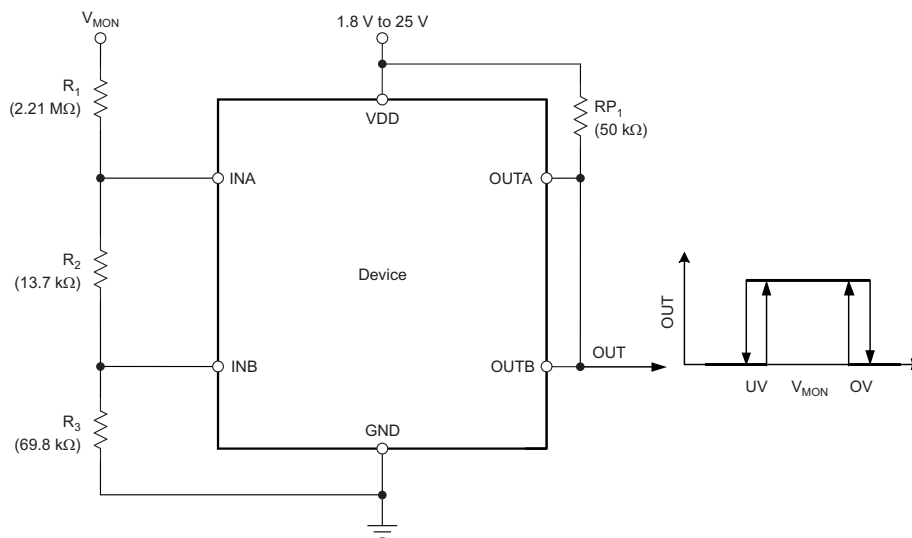


Figure 19. Window Comparator Block Diagram

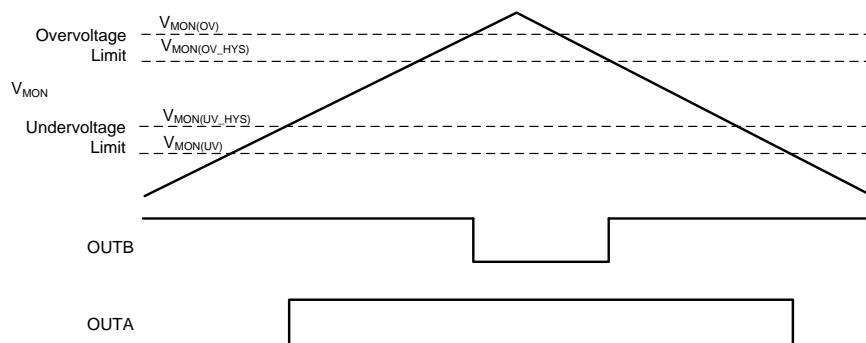


Figure 20. Window Comparator Timing Diagram

Application Information (continued)

The TLV6710 flags the overvoltage or undervoltage condition with the greatest accuracy. The highest accuracy threshold voltages are $V_{IT-(INA)}$ and $V_{IT+(INB)}$, and correspond with the falling undervoltage flag, and the rising overvoltage flag, respectively. These thresholds represent the accuracy when the monitored voltage is within the valid window (both OUTA and OUTB are in a high-impedance state), and correspond to the $V_{MON(UV)}$ and $V_{MON(OV)}$ trigger voltages, respectively. If the monitored voltage is outside of the valid window (V_{MON} is less than the undervoltage limit, $V_{MON(UV)}$, or greater than overvoltage limit, $V_{MON(OV)}$), then the input threshold voltages to re-enter the valid window are $V_{IT+(INA)}$ or $V_{IT-(INB)}$, and correspond with the $V_{MON(UV_HYS)}$ and $V_{MON(OV_HYS)}$ monitored voltages, respectively.

The resistor divider values and target threshold voltage can be calculated by using [Equation 1](#) through [Equation 4](#):

$$R_{TOTAL} = R_1 + R_2 + R_3 \quad (1)$$

Choose an R_{TOTAL} value so that the current through the divider is approximately 100 times higher than the input current at the INA and INB pins. Resistors with high values minimize current consumption; however, the input bias current degrades accuracy if the current through the resistors is too low. See application report [Optimizing Resistor Dividers at a Comparator Input](#) (SLVA450), for details on sizing input resistors.

R_3 is determined by [Equation 2](#):

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \cdot V_{IT+(INB)}$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected. (2)

R_2 is determined by either [Equation 3](#) or [Equation 4](#):

$$R_2 = \left[\frac{R_{TOTAL}}{V_{MON(UV_HYS)}} \cdot V_{IT+(INA)} \right] - R_3$$

where

- $V_{MON(UV_HYS)}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises. (3)

$$R_2 = \left[\frac{R_{TOTAL}}{V_{MON(UV)}} \cdot V_{IT-(INA)} \right] - R_3$$

where

- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected. (4)

9.1.2 Input and Output Configurations

[Figure 21](#) to [Figure 23](#) show examples of the various input and output configurations.

Application Information (continued)

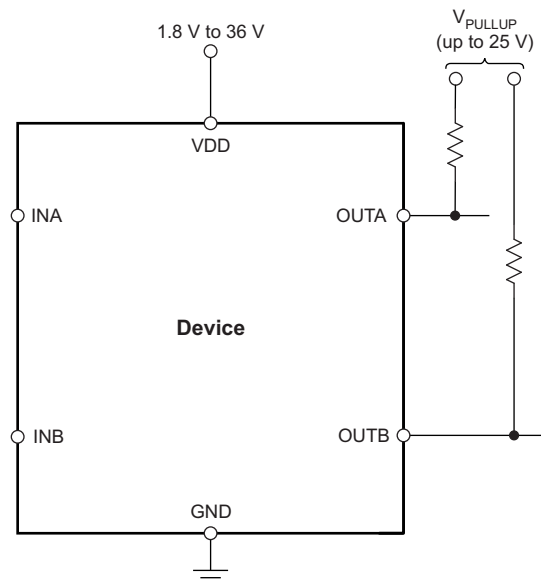


Figure 21. Interfacing to Voltages Other than V_{DD}

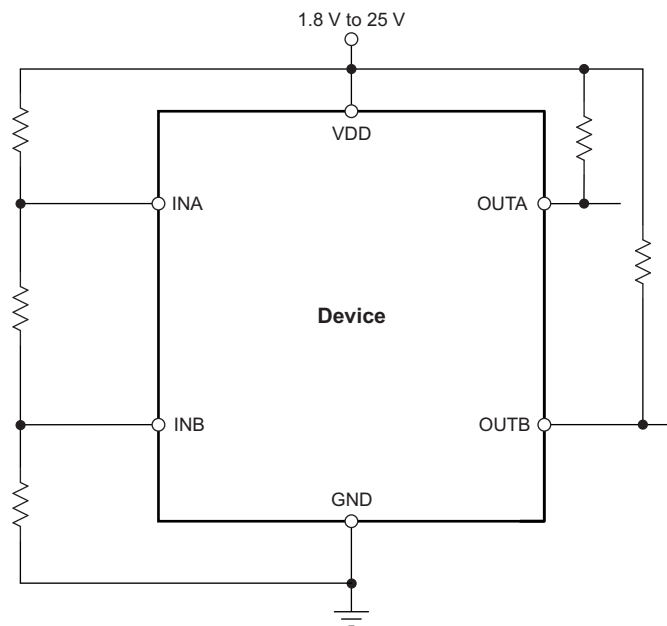
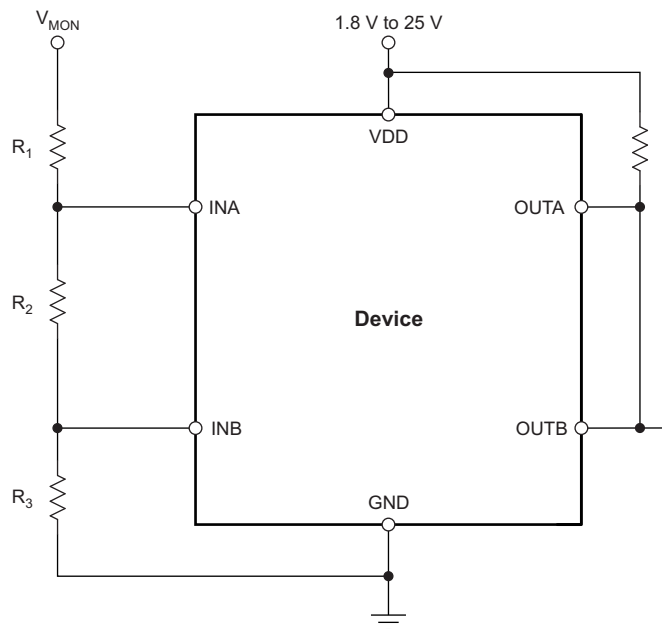


Figure 22. Monitoring the Same Voltage as V_{DD}

Application Information (continued)



NOTE: The inputs can monitor a voltage higher than V_{DD} (max) with the use of an external resistor divider network.

Figure 23. Monitoring a Voltage Other than V_{DD}

9.1.3 Immunity to Input Pin Voltage Transients

The TLV6710 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and amplitude; see [Figure 3, Minimum Pulse Duration vs Threshold Overdrive Voltage](#).

9.2 Typical Application

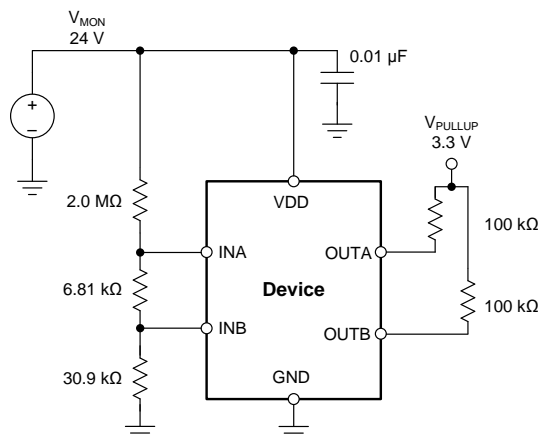


Figure 24. 24-V, 10% Window Comparator

Typical Application (continued)

9.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	24-V nominal, rising ($V_{\text{MON(OV)}}$) and falling ($V_{\text{MON(UV)}}$) threshold $\pm 10\%$ nominal (26.4 V and 21.6 V, respectively)	$V_{\text{MON(OV)}} = 26.4 \text{ V} \pm 2.7\%$, $V_{\text{MON(UV)}} = 21.6 \text{ V} \pm 2.7\%$
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Maximum current consumption	30 μA	24 μA

9.2.2 Detailed Design Procedure

- Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification by using [Equation 1](#). For this example, the current flow through the resistor network was chosen to be 13 μA ; a lower current can be selected, however, care should be taken to avoid leakage currents that are artifacts of the manufacturing process. Leakage currents significantly impact the accuracy if they are greater than 1% of the resistor network current.

$$R_{\text{TOTAL}} = \frac{V_{\text{MON(OV)}}}{I} = \frac{26.4 \text{ V}}{13 \mu\text{A}} = 2.03 \text{ M}\Omega$$

where

- $V_{\text{MON(OV)}}$ is the target voltage at which an overvoltage condition is detected as V_{MON} rises.
 - I is the current flowing through the resistor network.
- (5)

- After R_{TOTAL} is determined, R_3 can be calculated using [Equation 6](#). Select the nearest 1% resistor value for R_3 . In this case, 30.9 k Ω is the closest value.

$$R_3 = \frac{R_{\text{TOTAL}}}{V_{\text{MON(OV)}}} \cdot V_{\text{IT+(INB)}} = \frac{2.03 \text{ M}\Omega}{26.4 \text{ V}} \cdot 0.4 \text{ V} = 30.7 \text{ k}\Omega$$
(6)

- Use [Equation 7](#) to calculate R_2 . Select the nearest 1% resistor value for R_2 . In this case, 6.81 k Ω is the closest value.

$$R_2 = \frac{R_{\text{TOTAL}}}{V_{\text{MON(UV)}}} \cdot V_{\text{IT-(INA+)}} - R_3 = \frac{2.03 \text{ M}\Omega}{21.6 \text{ V}} \cdot 0.4 \text{ V} - 30.9 \text{ k}\Omega = 6.69 \text{ k}\Omega$$
(7)

- Use [Equation 8](#) to calculate R_1 . Select the nearest 1% resistor value for R_1 . In this case, 2 M Ω is the closest value.

$$R_1 = R_{\text{TOTAL}} - R_2 - R_3 = 2.03 \text{ M}\Omega - 6.81 \text{ k}\Omega - 30.9 \text{ k}\Omega = 1.99 \text{ M}\Omega$$
(8)

- The worst-case tolerance can be calculated by referring to [Equation 13](#) in application report [Optimizing Resistor Dividers at a Comparator Input](#) (SLVA450). An example of the rising threshold error, $V_{\text{MON(OV)}}$, is given in [Equation 9](#):

$$\% \text{ ACC} = \% \text{ TOL}(V_{\text{IT+(INB)}}) + 2 \cdot \left(1 - \frac{V_{\text{IT+(INB)}}}{V_{\text{MON(OV)}}} \right) \cdot \% \text{ TOL}_R = 0.75 \% + 2 \cdot \left(1 - \frac{0.4}{26.4} \right) \cdot 1\% = 2.72 \%$$

where

- $\% \text{ TOL}(V_{\text{IT+(INB)}})$ is the tolerance of the INB positive threshold.
 - $\% \text{ ACC}$ is the total tolerance of the $V_{\text{MON(OV)}}$ voltage.
 - $\% \text{ TOL}_R$ is the tolerance of the resistors selected.
- (9)

- When the outputs switch to the high-Z state, the rise time of the OUTA or OUTB node depends on the pullup resistance and the capacitance on the node. Choose pullup resistors that satisfy the downstream timing requirements; 100-k Ω resistors are a good choice for low-capacitive loads.

9.2.3 Application Curve

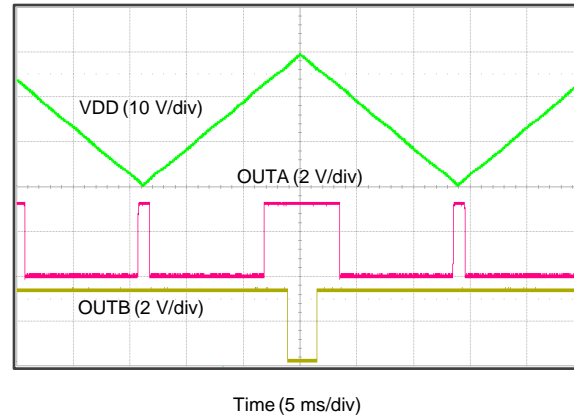


Figure 25. 24-V Window Monitor Output Response

9.3 Do's and Don'ts

It is good analog design practice to have a 0.1- μ F decoupling capacitor from V_{DD} to GND.

If the monitored rail is noisy, connect decoupling capacitors from the comparator inputs to GND.

Do not use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparators without also accounting for the effect to the accuracy.

Do not use pullup resistors that are too small, because the larger current sunk by the output then exceeds the desired low-level output voltage (V_{OL}).

10 Power Supply Recommendations

The TLV6710 has a 40-V absolute maximum rating on the VDD pin, with a recommended operating condition of 36 V. If the voltage supply that is providing power to VDD is susceptible to any large voltage transient that may exceed 40 V, or if the supply exhibits high voltage slew rates greater than 1 V/ μ s, take additional precautions. Place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. A 100- Ω resistor and 0.01- μ F capacitor is required in these cases, as shown in [Figure 26](#).

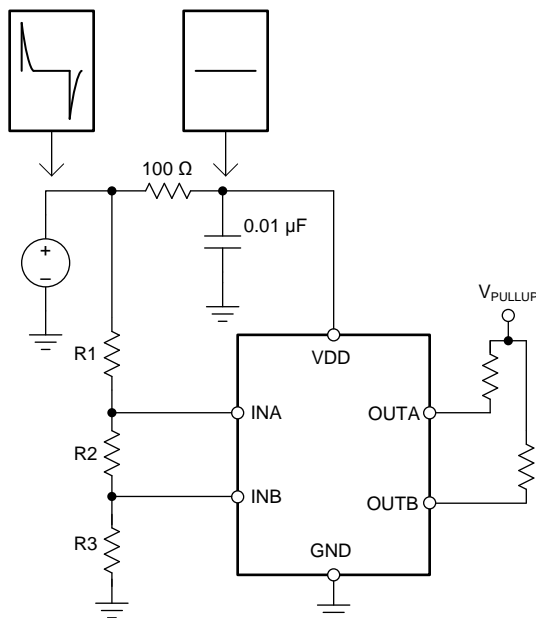


Figure 26. Using an RC Filter to Remove High-Frequency Disturbances on VDD

11 Layout

11.1 Layout Guidelines

- Place R_1 , R_2 , and R_3 close to the device to minimize noise coupling into the INA and INB nodes.
- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, may form an LC tank and create ringing with peak voltages above the maximum VDD voltage. If this is unavoidable, see [Figure 26](#) for an example of filtering VDD.

11.2 Layout Example

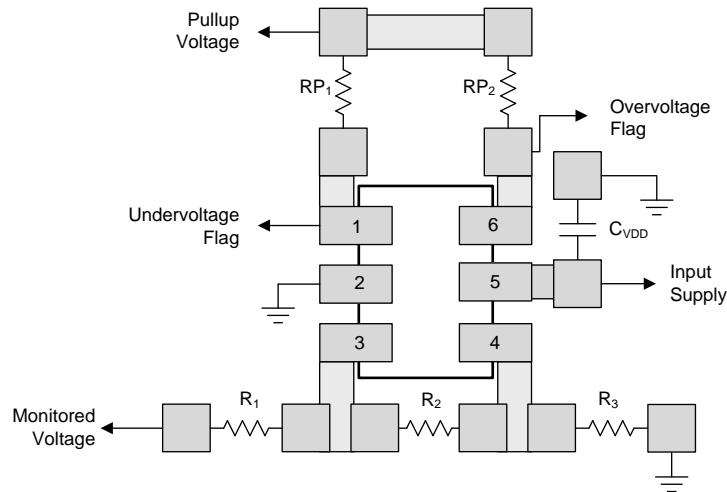


Figure 27. Recommended Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

[DIPアダプタ評価モジュール](#)では、SOT-23-6パッケージを標準のDIP-6ピン配置に変換して、プロトタイプ製作とベンチ評価を簡単に行うことができます。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

『[コンパレータ入力の分圧抵抗の最適化](#)』(SLVA450)

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

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12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV6710DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1161	Samples
TLV6710DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1161	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6710DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6710DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6710DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TLV6710DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0

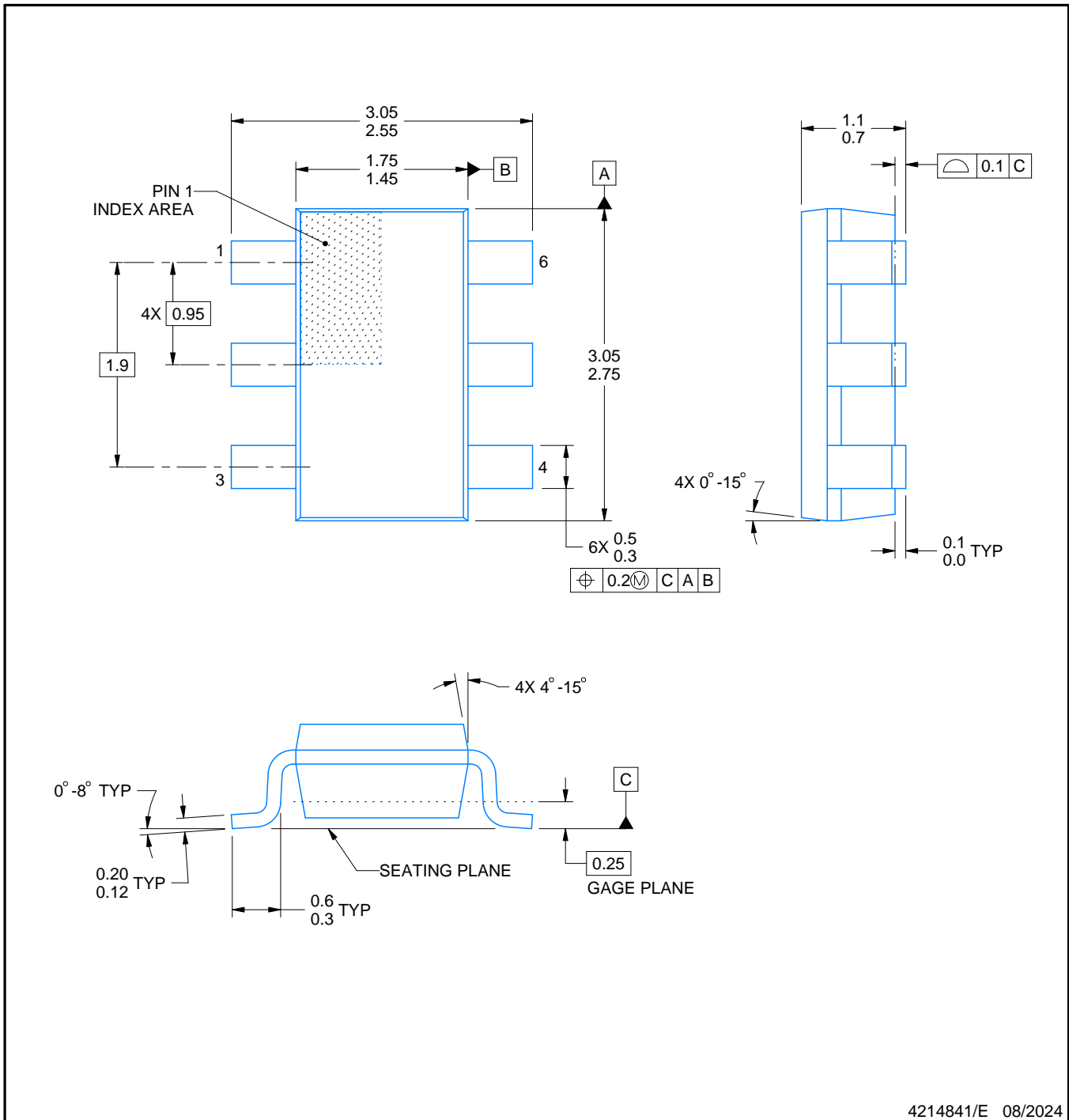
DDC0006A



PACKAGE OUTLINE

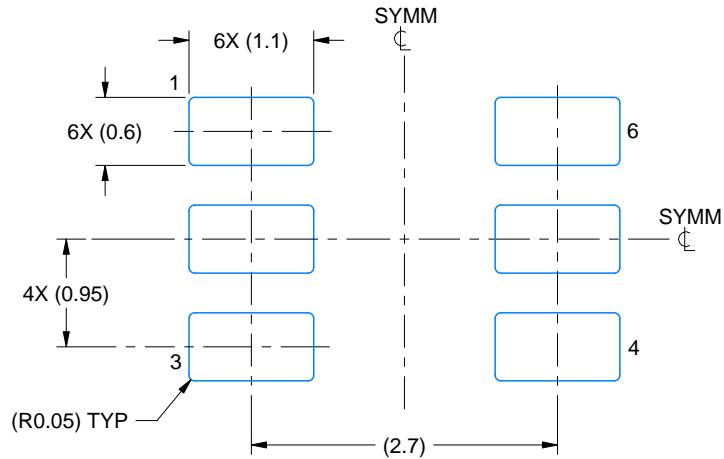
SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

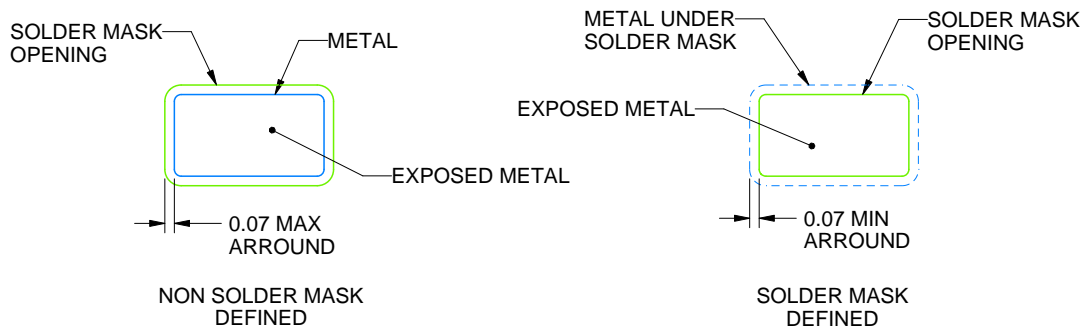


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X



SOLDEMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

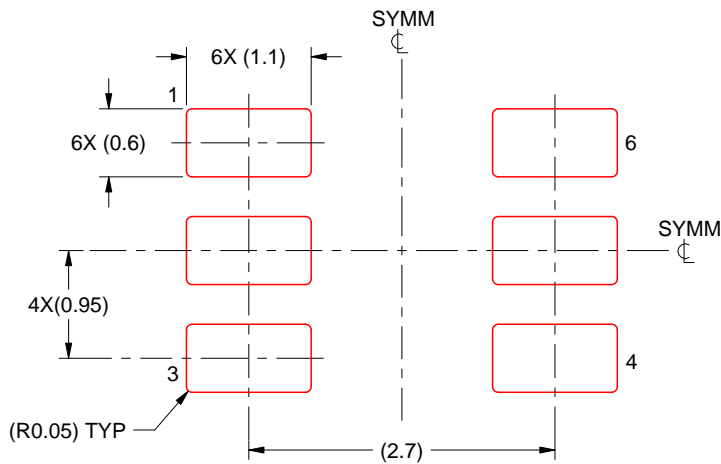
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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