

TLV61048 15V 出力電圧、非同期整流昇圧コンバータ SOT-23 パッケージ版

1 特長

- 入力電圧：2.61V～5.5V (2.4V まで低下)
- 出力電圧：最大 15V
- ローサイド FET 内蔵：85mΩ (3.3V_{IN} 時)
- スイッチ電流制限：4.7A (標準値)
- 600kHz または 1MHz のスイッチング周波数を選択可能
- シャットダウン時電流：1μA
- 出力電圧精度：±2.5%
- 軽負荷時の PFM 動作モード
- 2ms の内部ソフトスタート時間
- サーマル・シャットダウン保護機能
- 3mm × 3mm 6 ピン SOT-23 パッケージ

2 アプリケーション

- PLC バックアップ電源
- LCD バイアス電源
- 産業用絶縁 DC/DC

3 概要

TLV61048 は、低電圧の電気二重層コンデンサおよびシングルセル・リチウムイオン・バッテリーで駆動する製品向けの電源ソリューションを提供する非同期整流昇圧コンバータです。4.7A (標準値) の電流制限付き電源スイッチを内蔵し、最大負荷電流の供給を犠牲にすることなく、入力電源の放電性能を拡張できます。また、さまざまな小型の外付けインダクタおよび出力コンデンサを使用して、簡単に設計できます。

FREQ ピンの設定で 600kHz または 1MHz のスイッチング周波数を選択でき、軽負荷時には PFM 動作に移行して効率を高めます。また、内蔵された 2ms のソフトスタート機能により、突入電流を最小限に抑制できます。

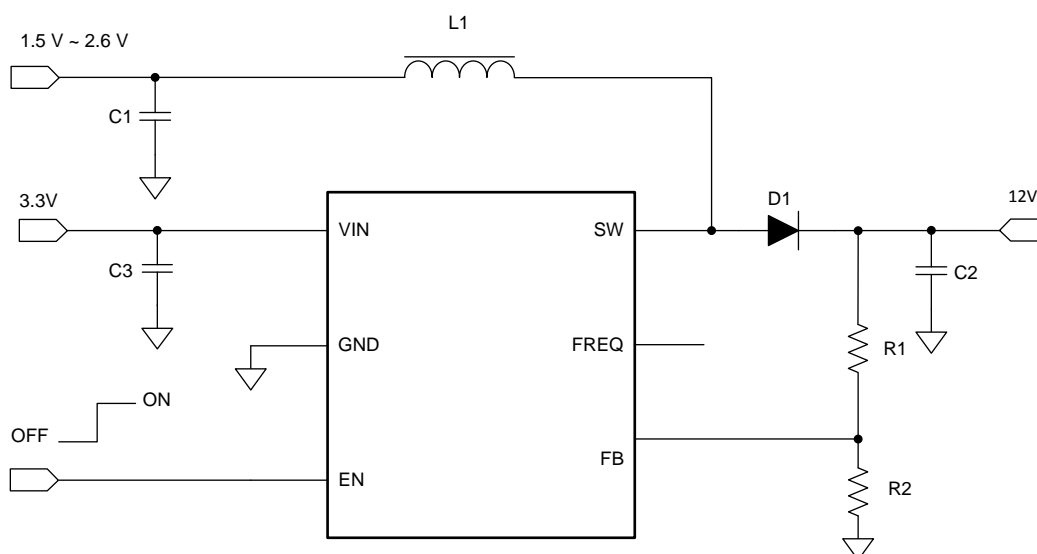
TLV61048 は 3mm × 3mm の 6 ピン SOT-23 パッケージで供給されます。

製品情報⁽¹⁾

| 型番 | パッケージ | 本体サイズ(公称) |
|----------|------------|---------------|
| TLV61048 | SOT-23 (6) | 2.90mm×1.60mm |

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



目次

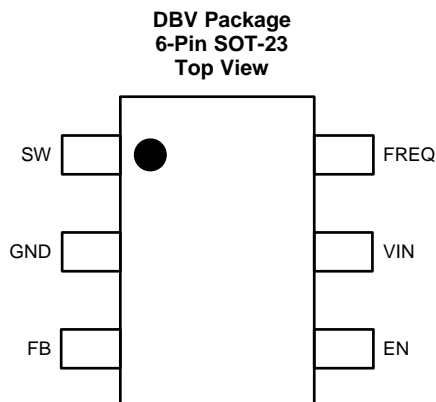
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|----------|--|----------|-----------|---|-----------|
| 1 | 特長 | 1 | 8 | Application and Implementation | 9 |
| 2 | アプリケーション | 1 | 8.1 | Application Information..... | 9 |
| 3 | 概要 | 1 | 8.2 | Typical Applications | 9 |
| 4 | 改訂履歴 | 2 | 9 | Power Supply Recommendations | 14 |
| 5 | Pin Configuration and Functions | 3 | 10 | Layout | 14 |
| 6 | Specifications | 4 | 10.1 | Layout Guidelines | 14 |
| 6.1 | Absolute Maximum Ratings | 4 | 10.2 | Layout Example | 14 |
| 6.2 | ESD Ratings | 4 | 11 | デバイスおよびドキュメントのサポート | 15 |
| 6.3 | Recommended Operating Conditions..... | 4 | 11.1 | デバイス・サポート | 15 |
| 6.4 | Thermal Information | 4 | 11.2 | ドキュメントの更新通知を受け取る方法..... | 15 |
| 6.5 | Electrical Characteristics..... | 5 | 11.3 | コミュニティ・リソース | 15 |
| 7 | Detailed Description | 6 | 11.4 | 商標 | 15 |
| 7.1 | Overview | 6 | 11.5 | 静電気放電に関する注意事項 | 15 |
| 7.2 | Functional Block Diagram | 6 | 11.6 | Glossary | 15 |
| 7.3 | Feature Description..... | 6 | 12 | メカニカル、パッケージ、および注文情報 | 15 |
| 7.4 | Device Functional Modes..... | 7 | | | |

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| 日付 | リビジョン | 注 |
|---------|-------|----|
| 2019年3月 | * | 初版 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|------|-----|---|
| NO. | NAME | | |
| 1 | SW | PWR | The switch pin of the converter. It is connected to the drain of the internal power MOSFET. |
| 2 | GND | PWR | Ground |
| 3 | FB | I | Voltage feedback of adjustable output voltage. Connected to the center tap of a resistor divider to program the output voltage. |
| 4 | EN | I | Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode. |
| 5 | VIN | I | IC power supply input |
| 6 | FREQ | I | Frequency select pin. The device operates at 600 kHz if FREQ is left floating and at 1 MHz if connected to GND. |

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|--|---------------|------|-----|------|
| Voltage range at terminals ⁽²⁾ | VIN, EN, FREQ | -0.3 | 6 | V |
| | SW | -0.3 | 18 | V |
| | FB | -0.3 | 3.6 | V |
| Operating junction temperature range, T _J | | -40 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|-----------------------------------|-------------------------|--|-------|------|
| V _(ESD) ⁽¹⁾ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽²⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽³⁾ | ±500 | V |

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|------------------|------------------------------------|------|-----|-----|------|
| V _{IN} | Input voltage range | 2.6 | | 5.5 | V |
| V _{OUT} | Output voltage range | 3.3 | | 14 | V |
| L | Effective inductance range | 2.2 | 4.7 | 10 | μH |
| C _{IN} | Effective input capacitance range | 0.22 | 1 | | μF |
| C _{OUT} | Effective output capacitance range | 4.7 | | | μF |
| T _J | Operating junction temperature | -40 | | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TLV61048 | UNIT |
|-------------------------------|--|-------------|------|
| | | DBV (SOT23) | |
| | | 6 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 177.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 120.6 | |
| R _{θJB} | Junction-to-board thermal resistance | 33.2 | |
| ψ _{JT} | Junction-to-top characterization parameter | 21.5 | |
| ψ _{JB} | Junction-to-board characterization parameter | 32.6 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{IN} = 3.3\text{ V}$. Typical values are at $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---------------------------------|---|------|------|------|--------------------|
| POWER SUPPLY | | | | | | |
| V_{IN} | Input voltage range | | 2.6 | | 5.5 | V |
| V_{IN_UVLO} | Under voltage lockout threshold | V_{IN} rising | | 2.55 | 2.61 | V |
| | | V_{IN} falling | 2.3 | 2.4 | | |
| V_{IN_HYS} | VIN UVLO hysteresis | | | 150 | | mV |
| I_{Q_VIN} | Quiescent current into VIN pin | IC enabled, no load, no switching | | 100 | | μA |
| I_{SD} | Shutdown current into VIN pin | IC disabled, $V_{IN} = 2.6\text{ V}$ to 5.5 V , $T_A = 25^{\circ}\text{C}$ | | | 1.0 | μA |
| OUTPUT | | | | | | |
| V_{OUT} | Output voltage range | | 3.3 | | 15 | V |
| V_{REF} | Feedback voltage | PWM mode, $T_J = -40^{\circ}\text{C}$ to 125°C | 0.78 | 0.8 | 0.82 | V |
| | | PFM mode, $T_A = 25^{\circ}\text{C}$ | | 0.81 | | V |
| I_{FB_LKG} | Leakage current into FB pin | $T_A = 25^{\circ}\text{C}$ | | | 50 | nA |
| I_{SW_LKG} | Leakage current into SW pin | IC disabled, $SW = 5.5\text{V}$ | | | 500 | nA |
| POWER SWITCH | | | | | | |
| $R_{DS(on)}$ | Low-side MOSFET on resistance | $V_{in} = 3.3, V_{out} = 12\text{V}$ | | 85 | | m Ω |
| f_{SW} | Switching frequency | Default, $SW = 1.5\text{V}$ | 480 | 550 | 620 | kHz |
| | | Default, $SW = 2.6\text{V}$ | 1020 | 1150 | 1280 | |
| t_{OFF_min} | Min. off time | 600kHz, $SW = 1.5\text{V}$ | | 130 | | ns |
| I_{LIM_SW} | Peak switch current limit | 600kHz, $V_{IN} = 3.3\text{V}$ | 3.8 | 4.7 | 5.6 | A |
| $t_{STARTUP}$ | Startup time | | | 2 | | ms |
| LOGIC INTERFACE | | | | | | |
| V_{EN_H} | EN Logic high threshold | | | | 1.2 | V |
| V_{EN_L} | EN Logic low threshold | | 0.4 | | | V |
| R_{EN} | EN Pull Down Resistor | | | 1 | | M Ω |
| R_{FREQ} | FREQ pull up resistance | | | 800 | | k Ω |
| V_{FREQ_H} | FREQ logic high threshold | | | | 1.2 | V |
| V_{FREQ_L} | FREQ logic low threshold | | 0.4 | | | V |
| PROTECTION | | | | | | |
| T_{SD} | Thermal shutdown threshold | T_J rising | | 150 | | $^{\circ}\text{C}$ |
| T_{SD_HYS} | Thermal shutdown hysteresis | T_J falling below T_{SD} | | 20 | | $^{\circ}\text{C}$ |

7 Detailed Description

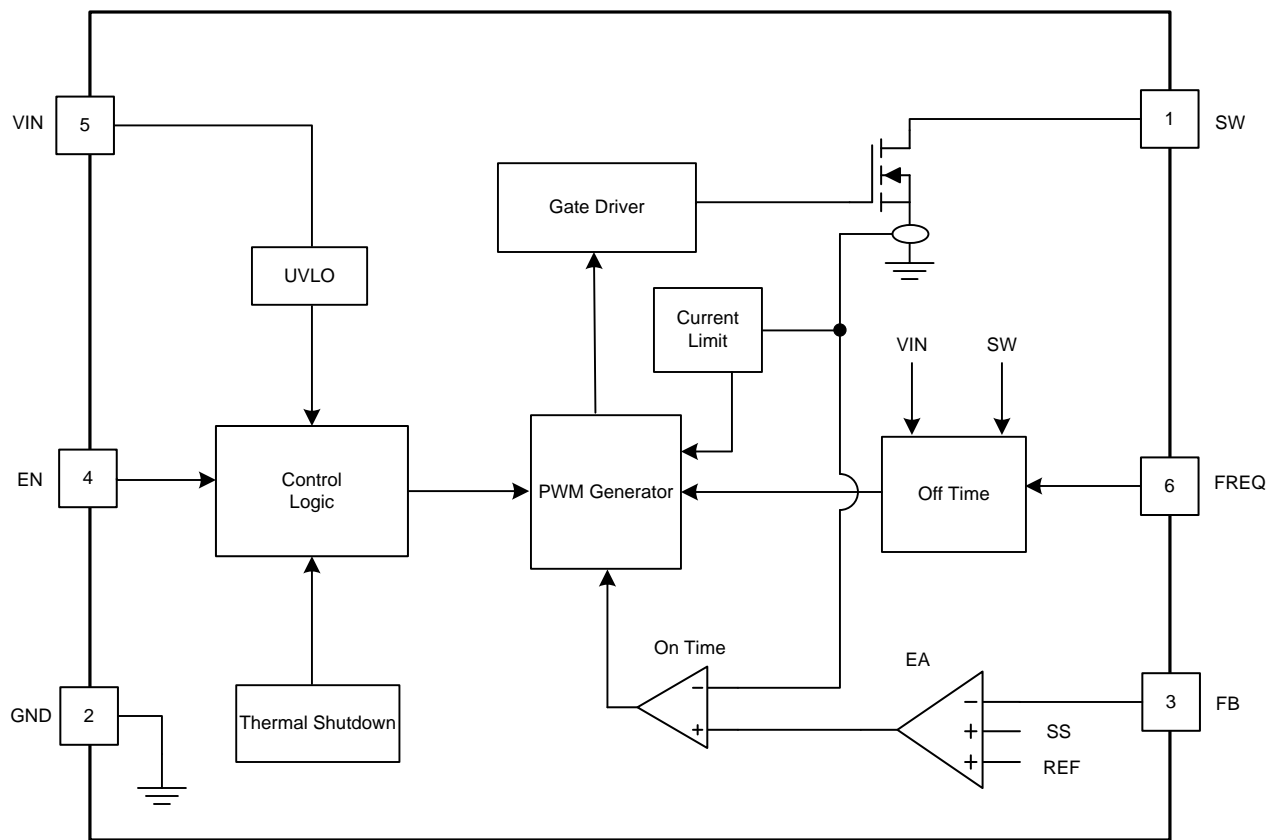
7.1 Overview

The TLV61048 is a non-synchronous boost converter supporting output voltage up to 15 V with input ranging from 2.61 V to 5.5 V. The TLV61048 integrates a power switch with current limit up to 4.7 A (typical). The device operates in a current mode scheme with quasi-constant frequency with internal loop compensation built in. The switching frequency is selectable between 600 kHz and 1 MHz. There is internal fixed soft start time which is 2 ms typically to control the inrush current during startup.

Topology of the TLV61048 boost converter is adaptive off-time with peak current control, which provides superior load and line transient responses. The selectable switching frequency offers the possibility to optimize the design either for the use of small sized inductor (1 MHz) or for higher system efficiency (600 kHz).

The converter operates in continuous conduction mode (CCM) when the inductor valley current is above zero, while switches into discontinuous conduction mode (DCM) if valley current crossing zero. If the load is further lowered, the device enters into PFM operation to achieve even higher efficiency.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 2.4 V. A hysteresis of 150 mV is added so that the device cannot be enabled again until the input voltage goes up to 2.55 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 2.4 V and 2.55 V.

Feature Description (continued)

7.3.2 Enable and Disable

When the input voltage is above typical UVLO rising threshold of 2.55 V and the EN pin is pulled high, the TLV61048 is enabled. When the EN pin is pulled low, the TLV61048 stops the PWM switch and turns off the low side switch. The EN pin has an internal pull-down resistance of 1M Ω , the device is disabled when the EN pin is floating. In shutdown mode, less than 1- μ A input current is consumed.

7.3.3 Soft Start

The soft-start feature helps the regulator to gradually reach the steady state operating point, thus reducing start-up stresses and surge. When the input voltage is applied, the output capacitor is charged to VIN through the inductor and high side rectifier diode. After reaching the 2.55 V (typical) UVLO threshold, the internal soft-start control circuit initiates to ramp the reference voltage to 0.8 V within 2 ms (typical), while the low side FET starts switching after output capacitor is charged to the input voltage.

7.3.4 Frequency Select (FREQ)

The frequency select pin FREQ allows to set the switching frequency of the device to 600 kHz (FREQ = floating) or 1 MHz (FREQ = GND). Higher switching frequency improves load transient response but reduces efficiency slightly. The other benefit of higher switching frequency is lower output ripple voltage.

7.4 Device Functional Modes

The TLV61048 has two operation modes: PWM mode and PFM mode.

7.4.1 PWM Mode

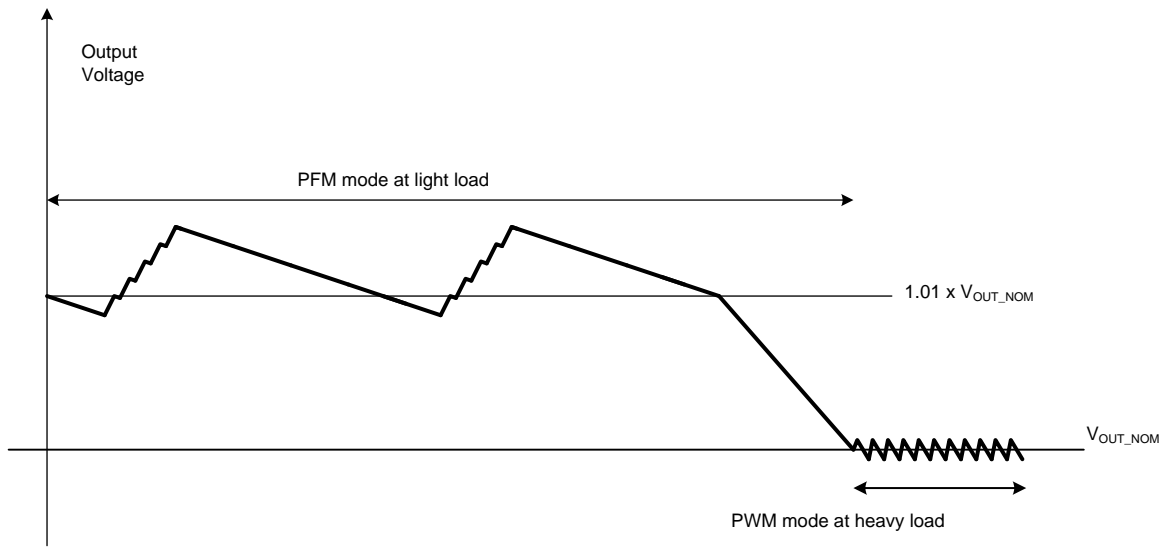
The TLV61048 uses a quasi-constant frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the VIN/VOU ratio, a circuit predicts the required off-time. At the beginning of the switching cycle, the integrated NMOS switching FET, shown in the functional block diagram, is turned on. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the inductor current hits the current threshold that is set by the error amplifier output, the PWM switch is turned off, and the external power diode is forward-biased. The inductor transfers its stored energy to replenish the output capacitor and supply the load. When the off-time is expired, the next switching cycle starts again. The error amplifier compares the FB pin voltage with an internal reference, and its output determines the duty cycle of the PWM switching.

The TLV61048 has a built-in compensation circuit that can accommodate a wide range of input and output voltages for stable operation.

7.4.2 PFM Mode

The TLV61048 integrates a power save mode with pulse frequency modulation (PFM) to improve efficiency at light load. When the load current decreases, the inductor peak current set by the output of the error amplifier declines to regulate the output voltage. When the inductor peak current hits the low limit (400 mA typical), the output voltage exceeds the set threshold voltage as the load current decreases further. When the FB voltage hits the PFM reference voltage, the TLV61048 goes into power-save mode. In the power-save mode, the device only switches when the output voltage trips below a set threshold voltage. It ramps up the output with several pulses and enters the power save mode when the output voltage exceeds the set threshold voltage.

Device Functional Modes (continued)



ADVANCE INFORMATION

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TLV61048 is a boost DC/DC converter integrating a power switch and loop compensation circuits. The device supports up to 15-V output with the input range from 2.61 V to 5.5 V. The device can operate down to 1.5 V if an external 3.3-V bias supply is applied to the VIN pin. The TLV61048 adopts the current-mode control with adaptive constant off-time. The switching frequency is quasi-constant and selectable between 600 kHz and 1 MHz. The following design procedure can be used to select component values for the TLV61048.

8.2 Typical Applications

8.2.1 12-V Output Boost Converter With External Bias

In this design example, TLV61048 VIN pin is supplied by an external 3.3-V bias voltage to keep internal circuitry on in order to extend power stage operating V_{IN} to 1.5 V. 600-kHz switching frequency is selected to reduce switching loss in order to improve overall efficiency.

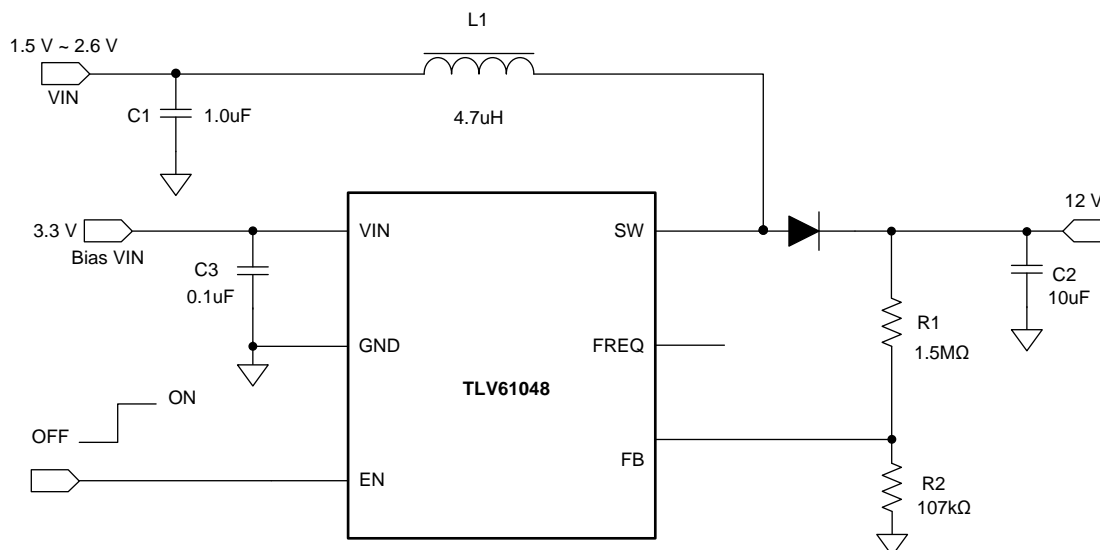


图 1. 12-V Boost Converter With External Bias

8.2.1.1 Design Requirements

For this design example, see parameters are shown in 表 1:

表 1. Design Requirements

| PARAMETERS | VALUE |
|-----------------------|----------------|
| Power input voltage | 1.5 V to 2.7 V |
| Control input voltage | 3.3 V |
| Output voltage | 12 V |
| Frequency | 600 kHz |
| Output current | 0 - 100 mA |

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Programming the Output Voltage

Output voltage is programmed via external resistor divider. By selecting the external resistor divider R1 and R2, as shown in 式 1, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is V_{REF} of 800 mV.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2$$

where

- V_{OUT} is the desired output voltage
 - V_{REF} is the internal reference voltage at the FB pin
- (1)

For best accuracy, R2 should be kept smaller than 150 k Ω to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. Changing the R2 towards a higher value reduces the quiescent current for achieving higher efficiency at low load currents.

8.2.1.2.2 Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and DC resistance (DCR). The TLV61048 is designed to work with inductor values between 2.2 μ H and 10 μ H. Use 式 2 to 式 4 to calculate the peak current of the application inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margin, choose the inductor value with –30% tolerance, and a low power-conversion efficiency for the calculation. In a boost regulator, the inductor dc current can be calculated with 式 2.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

where

- V_{OUT} = output voltage
 - I_{OUT} = output current
 - V_{IN} = input voltage
 - η = power conversion efficiency, use 80% for most applications
- (2)

The inductor ripple current is calculated with the 式 3 for an asynchronous boost converter in continuous conduction mode (CCM).

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} + 0.8V - V_{IN})}{L \times f_{SW} \times (V_{OUT} + 0.8V)}$$

where

- $\Delta I_{L(P-P)}$ = inductor ripple current
 - L = inductor value
 - f_{SW} = switching frequency
 - V_{OUT} = output voltage
 - V_{IN} = input voltage
- (3)

Therefore, the inductor peak current is calculated with 式 4.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2}$$
(4)

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. However, in the same way, load transient response time is increased. 表 2 lists the recommended inductor for the TLV61048 in the 600-kHz configuration.

表 2. Recommended Inductors for the TLV61048 at 600-kHz Configuration

| PART NUMBER | L (μH) | DCR MAX (mΩ) | SATURATION CURRENT TYPICAL (A) | SIZE (L×W×H) (mm) | VENDOR ⁽¹⁾ |
|----------------|--------|--------------|--------------------------------|-------------------|-----------------------|
| SWPA5040S4R7NT | 4.7 | 39 | 3.9 | 5 × 5 × 4 | Sunlord |
| XAL4030-472ME | 4.7 | 44.1 | 4.5 | 4 × 4 × 3 | Coilcraft |
| SWPA5040S100MT | 10 | 83 | 2.9 | 5 × 5 × 4 | Sunlord |
| XAL4040-103ME | 10 | 92.4 | 3 | 4 × 4 × 4 | Coilcraft |

(1) See [Third-party Products Disclaimer](#)

8.2.1.2.3 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}}$$

where

- D_{MAX} = maximum switching duty cycle
- V_{RIPPLE} = peak to peak output voltage ripple (5)

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used.

Take care when evaluating the derating of a ceramic capacitor under DC bias, aging, and AC signal. For example, the DC bias can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

TI recommends using the output capacitor with effective capacitance in the range of 4.7 μF to 10 μF for 600-kHz configuration. TI also recommends placing a small 1 μF capacitor right across the rectifier diode cathode to the GND pin of the TLV61048 to reduce the high RMS current loop's inductance. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output voltage ripple smaller in PWM mode. 表 3 lists the recommended capacitor for the TLV61048.

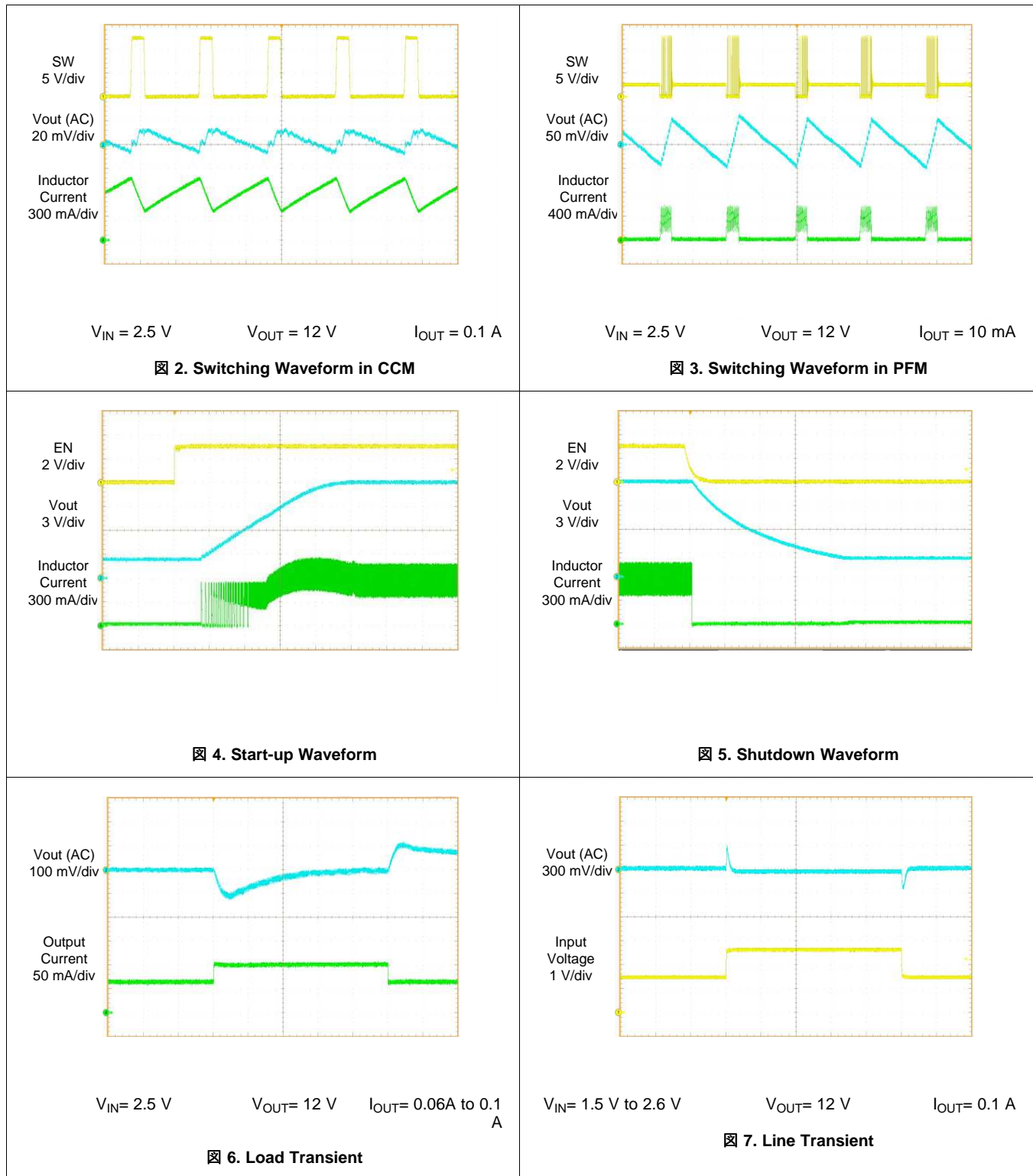
表 3. Recommended Output Capacitors for the TLV61048

| PART NUMBER | C _{OUT} (μF) | RATING | PACKAGE | VENDOR ⁽¹⁾ |
|-------------------|-----------------------|-----------|---------|-----------------------|
| TMK316BLD106KL | 10 | 25 V, X5R | 1206 | Taiyo Yuden |
| CC1206KKX5R8BB106 | 10 | 25 V, X5R | 1206 | Yageo |

(1) See [Third-party Products Disclaimer](#).

For input capacitor, a ceramic capacitor with more than 1 μF is enough for most applications.

8.2.1.3 Application Curves



8.2.2 15-V Output Boost Converter

In this design example, TLV61048 is configured to output 15-V DC voltage. 1-MHz switching frequency is selected to reduce output ripple and improve load transient performance. TI recommends placing an RC snubber from the switch node to the ground node to ensure voltage spike does not exceed the specified absolute maximum rating.

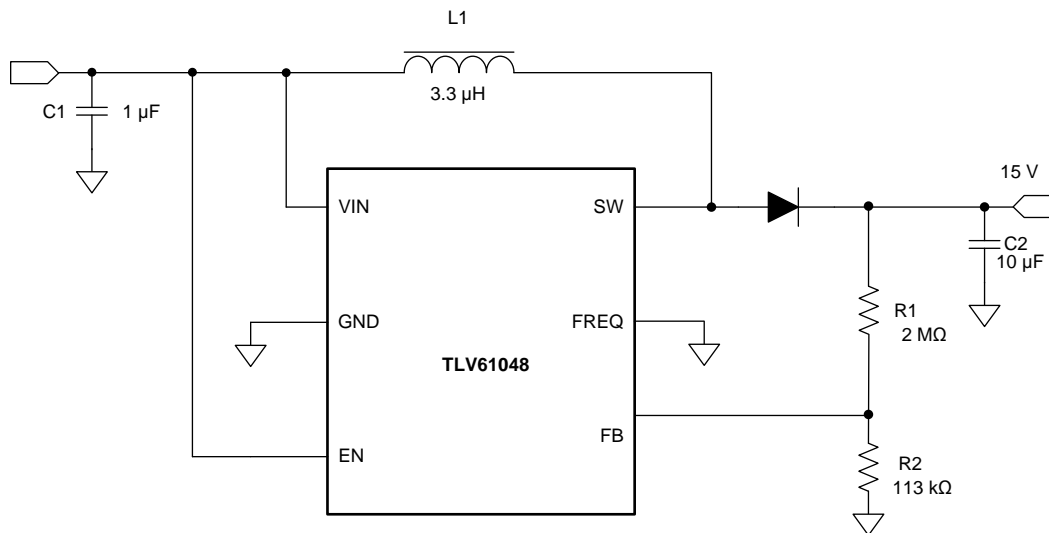


图 8. 15-V Boost Converter

8.2.2.1 Design Requirements

表 4. Design Requirements

| PARAMETER | VALUE |
|---------------------|----------------|
| Power input voltage | 2.6 V to 5.5 V |
| Output voltage | 15 V |
| Frequency | 1 MHz |
| Output current | 0 to 300 mA |

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Inductor Selection

Load transient and loop response performance is optimized at 1-MHz configuration, a smaller inductance is selected to push the right-half-plane-zero to a higher frequency beyond the crossover frequency of the control loop. The recommended inductors for 1-MHz operation are listed in 表 5.

表 5. Recommended Inductors for the TLV61048 at 1-MHz Configuration

| PART NUMBER | L (μH) | DCR MAX (mΩ) | SATURATION CURRENT TYPICAL (A) | SIZE (LxWxH) (mm) | VENDOR ⁽¹⁾ |
|----------------|--------|--------------|--------------------------------|-------------------|-----------------------|
| SWPA5040S2R2NT | 2.2 | 25 | 5.6 | 5 × 5 × 4 | Sunlord |
| XAL4020-222ME | 2.2 | 38.7 | 5.6 | 4 × 4 × 3 | Coilcraft |
| SWPA5040S3R3NT | 3.3 | 31 | 4.6 | 5 × 5 × 4 | Sunlord |
| XAL4030-332ME | 3.3 | 28.6 | 5.5 | 4 × 4 × 4 | Coilcraft |

(1) See [Third-party Products Disclaimer](#).

8.2.2.2.2 Input and Output Capacitor Selection

For 1-MHz configuration, use the information provided in [Input and Output Capacitor Selection](#).

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.5 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 μ F. Output current of the input power supply must be rated according to the supply voltage, output voltage and output current of the TLV61048.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor must not only be close to the VIN pin, but also to the GND in order to reduce input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise and fall time and must be kept as short as possible. Therefore, the output capacitor must not only be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin.

10.2 Layout Example

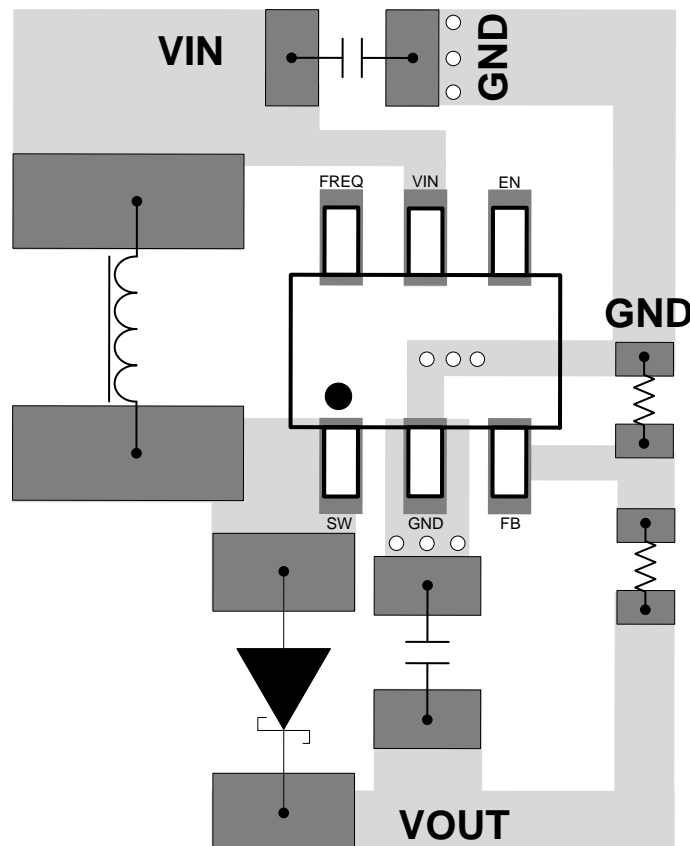


图 9. TLV61048 Layout

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

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11.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV61048DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1VSF | Samples |
| TLV61048DBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1VSF | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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