TLV4H290-SEP, TLV4H390-SEP
JAJSN18A – MAY 2024 – REVISED DECEMBER 2024

# TLV4H290-SEP および TLV4H390-SEP 宇宙向け強化プラスチックの耐放射線高精度クワッド コンパレータ

## 1 特長

- VID
  - V62/24636-01XE
  - V62/24636-02XE
- 放射線 - トータル ドーズ効果 (TID)
  - 30krad (Si) まで吸収線量 (TID) 特性を評価済み
  - 30krad (Si) まで ELDRS フリー
  - 30krad (Si) まで RHA/RLAT
- 放射線 - シングル イベント効果 (SEE)
  - SEL 耐性:LET = 43MeV·cm2 /mg
  - SET 特性:LET = 43MeV·cm2 /mg
- 宇宙向け強化プラスチック
  - 管理されたベースライン
  - 単一のアセンブリ / テスト施設
  - 単一の製造施設
  - 長期にわたる製品ライフ サイクル
  - 製品のトレーサビリティ
- 電源電圧範囲:1.65V～5.5V
- 高精度入力オフセット電圧:300µV
- フォルト トレラントな入力
- 伝搬遅延時間:100ns (代表値)
- 低い静止電流:チャネルあたり 25µA
- 低い入力バイアス電流:5pA
- オープン ドレイン出力オプション (TLV4H290-SEP)
- プッシュプル出力オプション (TLV4H390-SEP)
- 全温度範囲 (-55℃～125℃)
- ESD 保護:2kV

## 2 アプリケーション

- 低軌道衛星用途のサポート
- 電化製品
- ビル オートメーション
- ファクトリ オートメーション / 制御
- モーター ドライブ
- インフォテインメントおよびクラスタ

## 3 概要

TLV4H290-SEP および TLV4H390-SEP は、入力オフセット電圧が低く、速度と消費電力の組み合わせが非常に優れており、伝搬遅延が 100ns のクワッド チャネル コンパレータです。動作電圧範囲は 1.65V～5.5V で、静止時消費電流は 1 チャネルあたり 25µA です。

このデバイス ファミリにはフォルト トレラントな入力が内蔵されており、コンパレータに電源が印加されていない場合でも入力ピンに電圧を印加できるため、電源シーケンシングが課題となるアプリケーションに最適です。同様に、これらのコンパレータは最高 6V までのフォルト トレラントな入力で損傷を受けず、出力の位相反転も起きません。

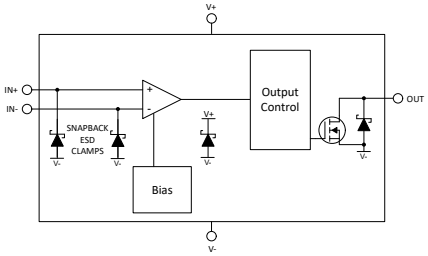
TLV4H290-SEP コンパレータにはオープン ドレイン出力段があり、電源電圧の下や上にプルできるため、レベル変換に適しています。TLV4H390-SEP にはプッシュプル出力段があり、シンク電流とソース電流の両方を供給できます。

TLV4H290-SEP および TLV4H390-SEP は、プラスチックの 14 ピン SOT-23 パッケージで供給され、放射線耐性は最大 43MeV·cm$^2$ /mg です。

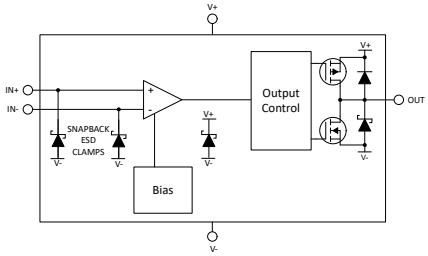
**製品情報**

| 部品番号 | パッケージ (1) | 本体サイズ (公称)(2) |
|---|---|---|
| TLV4H290-SEP、TLV4H390-SEP | SOT-23 (14) | 4.2 mm × 2.0mm |

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。




オープン ドレイン出力のブロック図




プッシュプル出力のブロック図

# Table of Contents

# 4 Pin Configuration and Functions

## 4.1 Pin Functions:TLV4H290-SEP and TLV4H390-SEP Quad

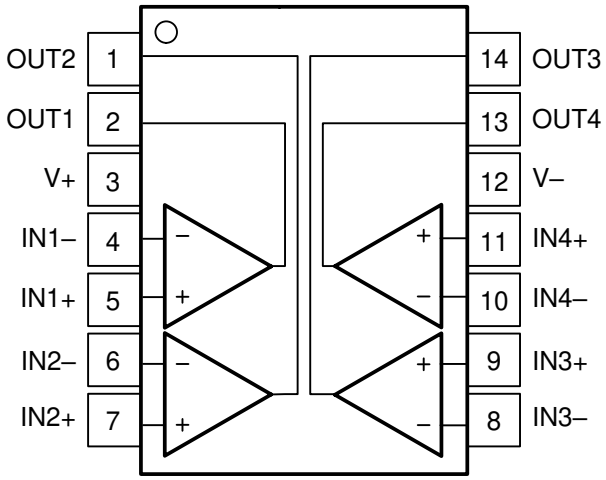



**図 4-1. DYY Package**
**14-Pin SOT-23**
**Top View**

**表 4-1. Pin Functions: TLV4H290-SEP and TLV4H390-SEP Quad**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| OUT2 | 1 | O | Output pin of the comparator 2 |
| OUT1 | 2 | O | Output pin of the comparator1 |
| V+ | 3 | — | Positive supply |
| IN1– | 4 | I | Negative input pin of the comparator 1 |
| IN1+ | 5 | I | Positive input pin of the comparator 1 |
| IN2– | 6 | I | Negative input pin of the comparator 2 |
| IN2+ | 7 | I | Positive input pin of the comparator 2 |
| IN3– | 8 | I | Negative input pin of the comparator 3 |
| IN3+ | 9 | I | Positive input pin of the comparator 3 |
| IN4– | 10 | I | Negative input pin of the comparator 4 |
| IN4+ | 11 | I | Positive input pin of the comparator 4 |
| V– | 12 | — | Negative supply |
| OUT4 | 13 | O | Output pin of the comparator 4 |
| OUT3 | 14 | O | Output pin of the comparator 3 |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage: $V_S$ = (V+) – (V–) | –0.3 | 6 | V |
| Input pins (IN+, IN–) from (V–)(2) | –0.3 | 6 | V |
| Current into Input pins (IN+, IN–) | –10 | 10 | mA |
| Output (OUT) from (V–), open-drain only(3) | –0.3 | 6 | V |
| Output (OUT) from (V–), push-pull only | –0.3 | (V+) + 0.3 | V |
| Output short circuit duration(4) | | 10 | s |
| Junction temperature, $T_J$ | | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less. Additionally, Inputs (IN+, IN–) can be greater than (V+) and OUT as long as input is within the –0.3V to 6V range
(3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as the input is within the –0.3V to 6V range
(4) Short-circuit to (V–) or (V+).

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage: $V_S$ = (V+) – (V–) | 1.65 | 5.5 | V |
| Input voltage range (IN+, IN–) from (V–) | –0.3 | 5.7 | V |
| Ambient temperature, $T_A$ | –55 | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | TLV4H290-SEP, TLV4H390-SEP DYY (SOT23) 14 PINS | UNIT |
|---|---|---|---|
| $R_{qJA}$ | Junction-to-ambient thermal resistance | 218.1 | °C/W |
| $R_{qJC(top)}$ | Junction-to-case (top) thermal resistance | 127.0 | °C/W |
| $R_{qJB}$ | Junction-to-board thermal resistance | 129.6 | °C/W |
| $y_{JT}$ | Junction-to-top characterization parameter | 24.7 | °C/W |
| $y_{JB}$ | Junction-to-board characterization parameter | 126.8 | °C/W |
| $R_{qJC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics appnote.

## 5.5 Electrical Characteristics

For $V_S$ (Total Supply Voltage) = (V+) – (V–) = 5V, $V_{CM}$ = (V–) at $T_A$ = 25°C (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_S$ = 1.8V and 5V | –3 | ±0.3 | 3 | mV |
| $V_{OS}$ | Input offset voltage | $V_S$ = 1.8V and 5V, $T_A$ = –55°C to +125°C | –4 | | 4 | mV |
| $dV_{IO}/dT$ | Input offset voltage drift | $V_S$ = 1.8V and 5V, $T_A$ = –55°C to +125°C | | ±0.5 | | µV/°C |
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current per comparator | $V_S$ = 1.8V and 5V, No Load, Output Low | | 25 | 35 | µA |
| $I_Q$ | Quiescent current per comparator | $V_S$ = 1.8V and 5V, No Load, Output Low, $T_A$ = –55°C to +125°C | | | 40 | µA |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8V to 5V, $T_A$ = –55°C to +125°C | | 95 | | dB |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $V_{CM} = V_S/2$ | | 5 | | pA |
| $I_{OS}$ | Input offset current | $V_{CM} = V_S/2$ | | 1 | | pA |
| **INPUT CAPACITANCE** | | | | | | |
| $C_{ID}$ | Input Capacitance, Differential | $V_{CM} = V_S/2$ | | 2 | | pF |
| $C_{IC}$ | Input Capacitance, Common Mode | $V_{CM} = V_S/2$ | | 3 | | pF |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM\text{-}Range}$ | Common-mode voltage range | $V_S$ = 1.8V and 5V, $T_A$ = –55°C to +125°C | (V–) – 0.2 | | (V+) - 1.5 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 5V, (V–) < $V_{CM}$ < (V+ - 1.5), $T_A$ = –55°C to +125°C | | 70 | | dB |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{VD}$ | Large signal differential voltage amplification | For open-drain version only | | 200 | | V/mV |
| **OUTPUT** | | | | | | |
| $V_{OL}$ | Voltage swing from (V–) | $I_{SINK}$ = 4mA, $T_A$ = 25°C | | 75 | 125 | mV |
| $V_{OL}$ | Voltage swing from (V–) | $I_{SINK}$ = 4mA, $T_A$ = –55°C to +125°C | | | 175 | mV |
| $V_{OH}$ | Voltage swing from (V+) | $I_{SOURCE}$ = 4mA, $T_A$ = 25°C (push-pull only) | | 75 | 125 | mV |
| $V_{OH}$ | Voltage swing from (V+) | $I_{SOURCE}$ = 4mA, $T_A$ = –55°C to +125°C (push-pull only) | | | 175 | mV |
| $I_{LKG}$ | Open-drain output leakage current | $V_{PULLUP}$ = (V+), $T_A$ = 25°C (open drain only) | | 10 | | nA |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5V, Sinking | 90 | 100 | | mA |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5V, Sourcing (push-pull only) | 90 | 100 | | mA |

## 5.6 Switching Characteristics

For $V_S$ (Total Supply Voltage) = (V+) – (V–) = 5V, $V_{CM}$ = $V_S$ / 2, $C_L$ = 15pF at $T_A$ = 25°C (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $T_{PD-HL}$ | Propagation delay time, high-to-low | $V_{ID}$ = –100mV; Delay from mid-point of input to mid-point of output ($R_P$ = 2.5KΩ for open drain only) | | 100 | | ns |
| $T_{PD-LH}$ | Propagation delay time, low-to-high | $V_{ID}$ = 100mV; Delay from mid-point of input to mid-point of output (for push-pull only) | | 115 | | ns |
| $T_{PD-LH}$ | Propagation delay time, low-to-high | $V_{ID}$ = 100mV; Delay from mid-point of input to mid-point of output ($R_P$ = 2.5KΩ for open drain only) | | 150 | | ns |
| $T_{FALL}$ | 5V Output Fall Time, 80% to 20% | $V_{ID}$ = –100mV | | 3 | | ns |
| $T_{RISE}$ | 5V Output Rise Time, 20% to 80% | $V_{ID}$ = 100mV, for push-pull only | | 3 | | ns |
| $F_{TOGGLE}$ | 5V, Toggle Frequency | $V_{ID}$ = 100mV ($R_P$ = 2.5KΩ for open drain only) | | 3 | | MHz |
| **POWER ON TIME** | | | | | | |
| $P_{ON}$ | Power on-time | $V_S$ = 1.8V and 5V, $V_{CM}$ = (V–), $V_{ID}$ = –0.1V, $V_{PULL-UP}$ = $V_S$ / 2, Delay from $V_S$ / 2 to $V_{OUT}$ = 0.1 x $V_S$ / 2 ($R_P$ = 2.5KΩ for open drain only) | | 30 | | µs |

# 6 Typical Characteristics

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

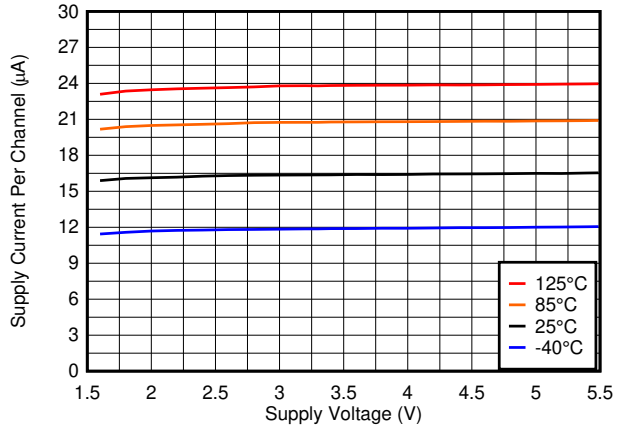



図 6-1. Supply Current vs. Supply Voltage

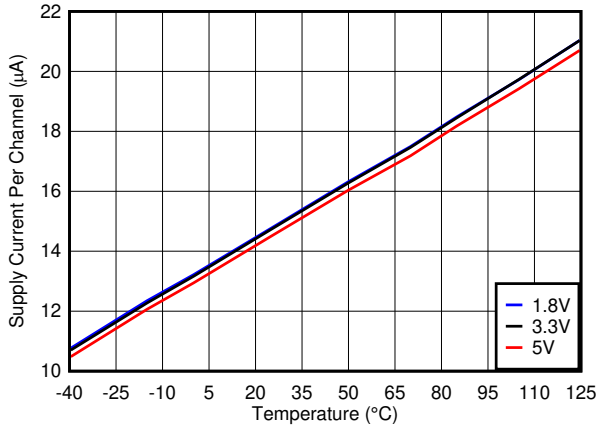



図 6-2. Supply Current vs. Temperature

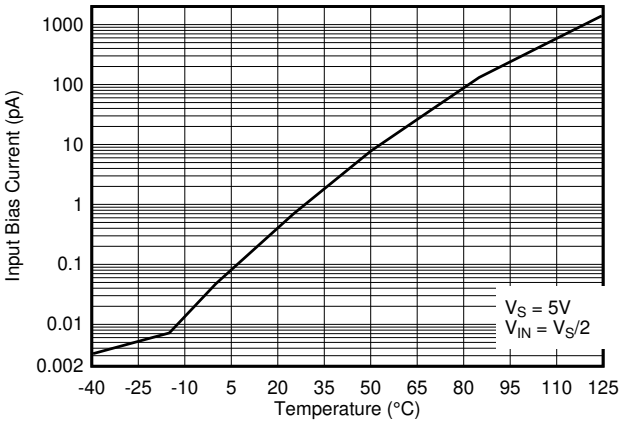



図 6-3. Input Bias Current vs. Temperature

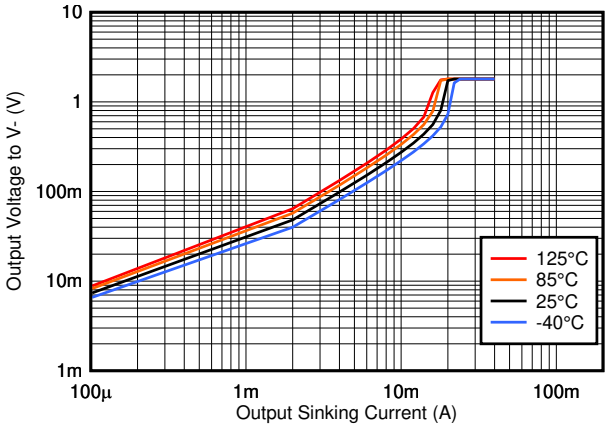



図 6-4. Output Sinking Current vs. Output Voltage, 1.8V

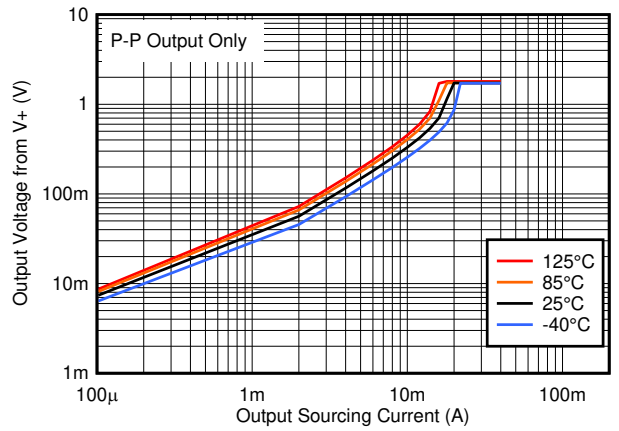



図 6-5. Output Sourcing Current vs. Output Voltage, 1.8V

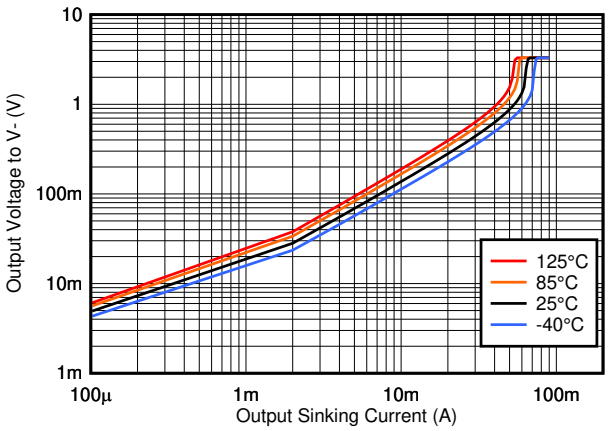



図 6-6. Output Sinking Current vs. Output Voltage, 3.3V

## 6 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

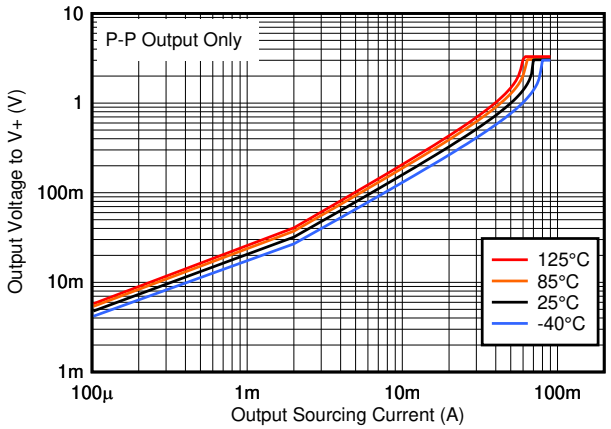



図 6-7. Output Sourcing Current vs. Output Voltage, 3.3V

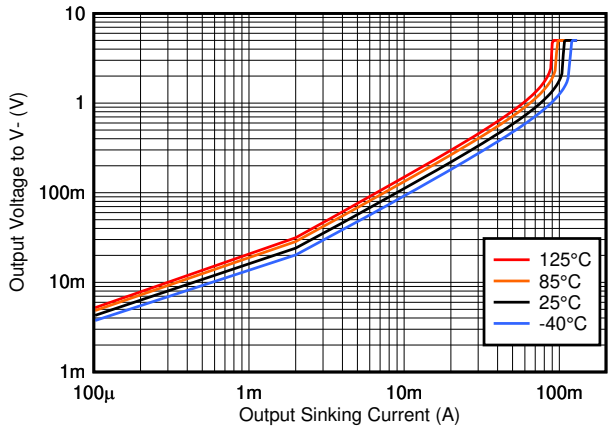



図 6-8. Output Sinking Current vs. Output Voltage, 5V

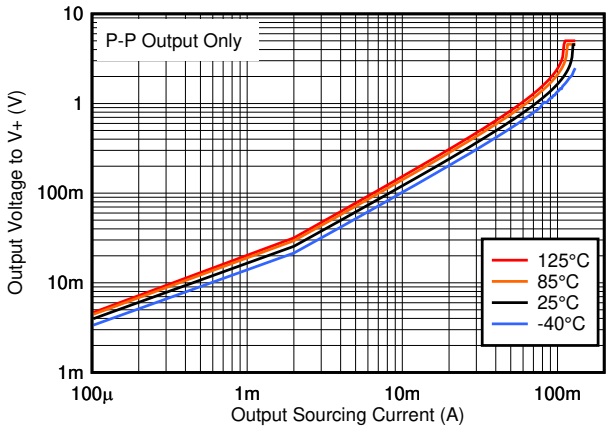



図 6-9. Output Sourcing Current vs. Output Voltage, 5V

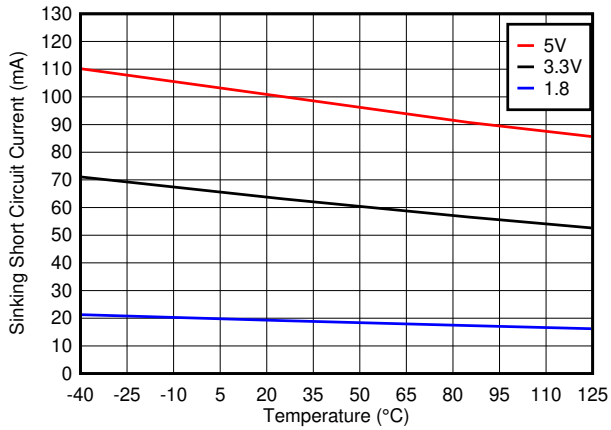



図 6-10. Sinking Short Circuit Current vs. Temperature

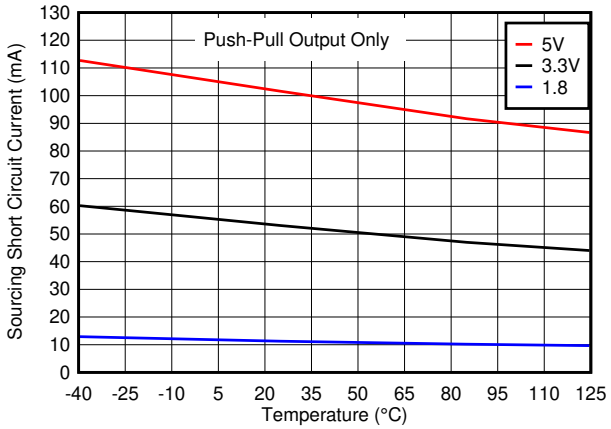



図 6-11. Sourcing Short Circuit Current vs. Temperature

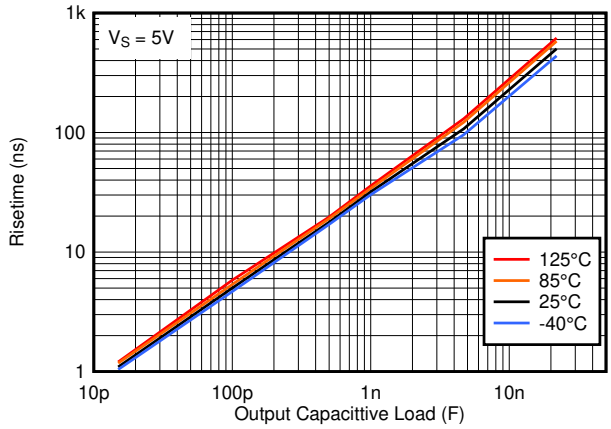



図 6-12. Risetime vs. Capacitive Load

## 6 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

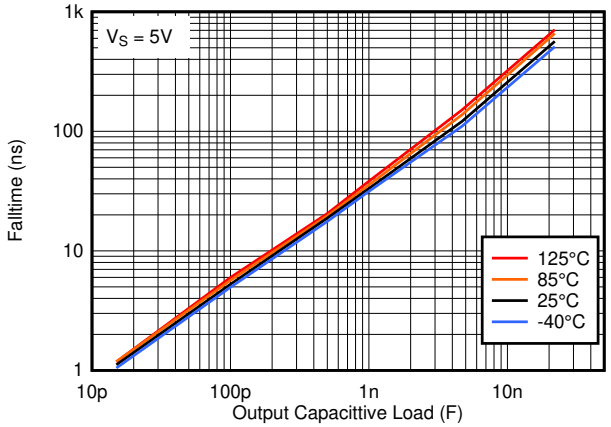



図 6-13. Falltime vs. Capacitive Load

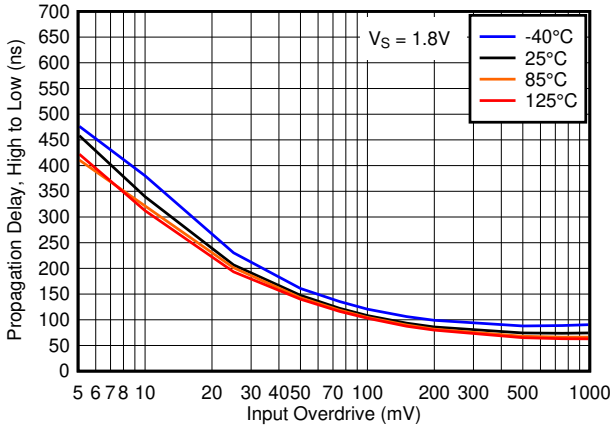



図 6-14. Propagation Delay, High to Low, 1.8V

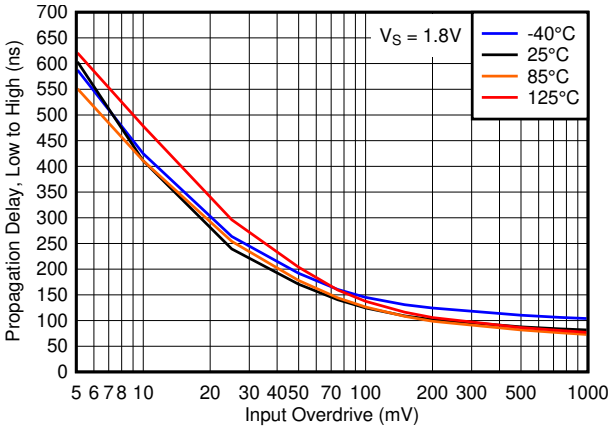



図 6-15. Propagation Delay, Low to High, 1.8V

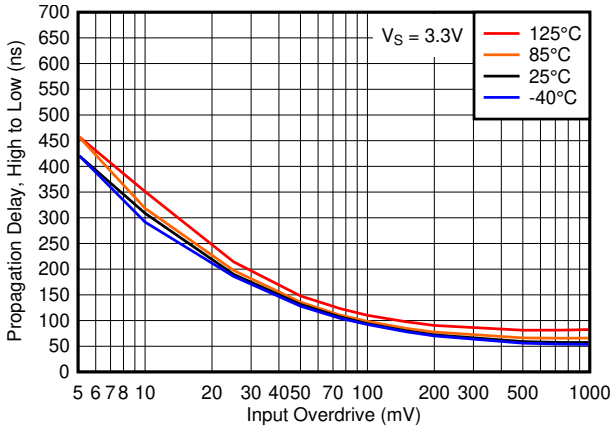



図 6-16. Propagation Delay, High to Low, 3.3V

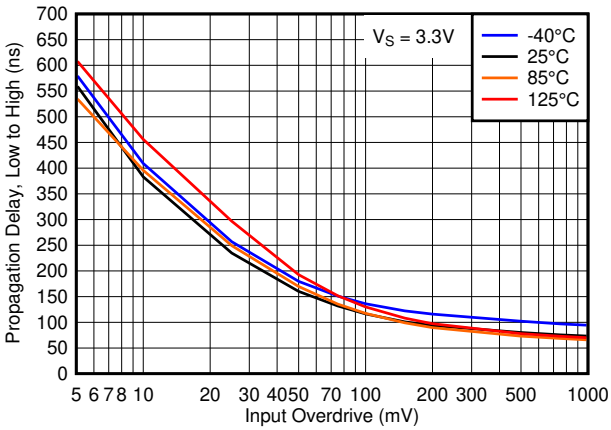



図 6-17. Propagation Delay, Low to High, 3.3V

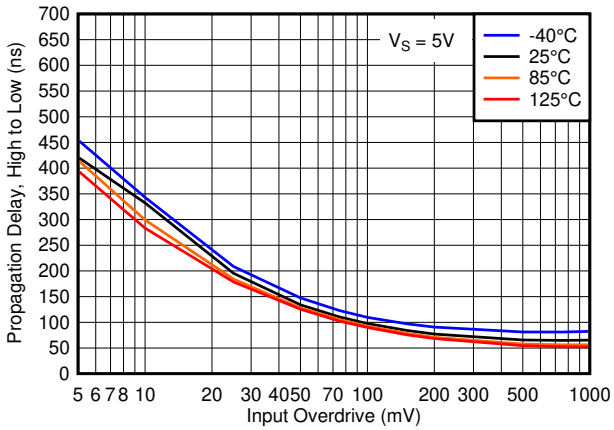



図 6-18. Propagation Delay, High to Low, 5V

## 6 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

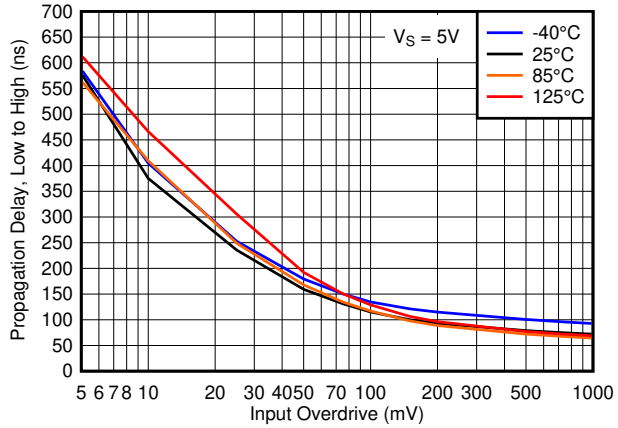



図 6-19. Propagation Delay, Low to High, 5V

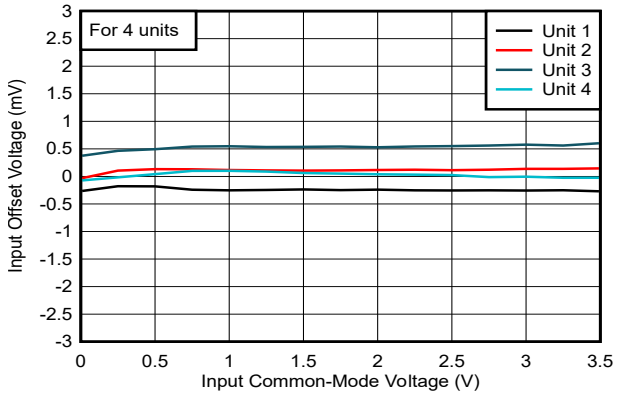



図 6-20. Offset Voltage vs. Common-Mode at 125°C, 5V

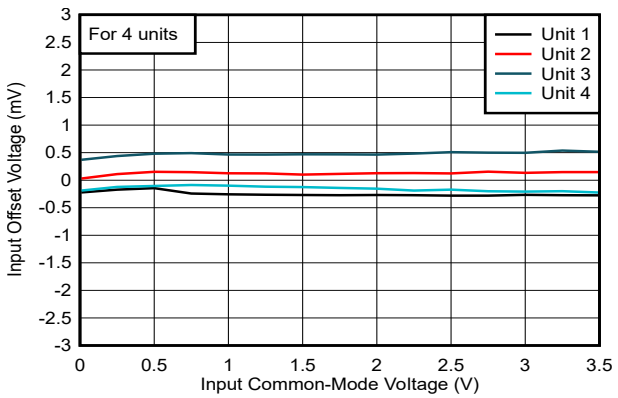



図 6-21. Offset Voltage vs. Common-Mode at 25°C, 5V

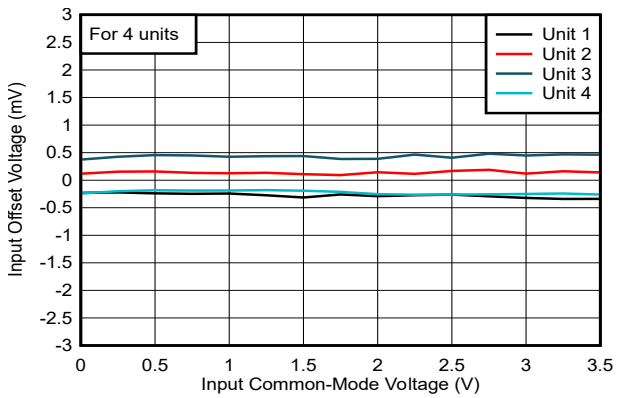



図 6-22. Offset Voltage vs. Common-Mode at -40°C, 5V

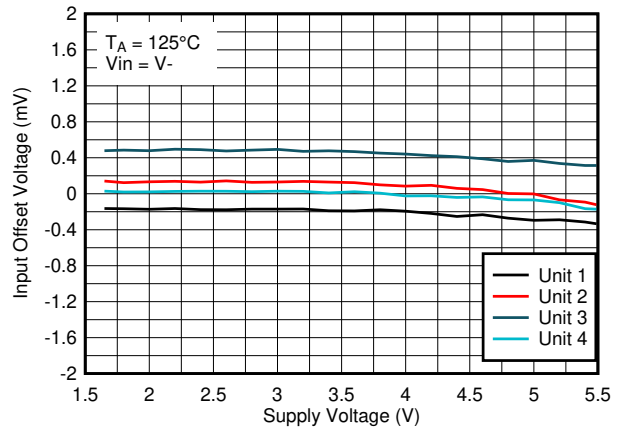



図 6-23. Offset Voltage vs. Supply Voltage at 125°C, $V_{IN}$=V-

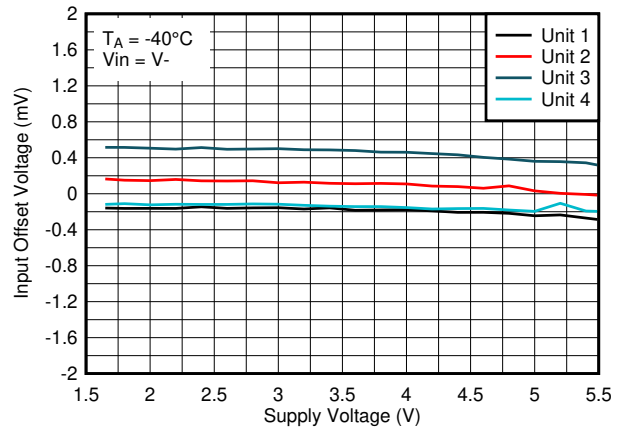



図 6-24. Offset Voltage vs. Supply Voltage at 25°C, $V_{IN}$=V-

## 6 Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 5V, $R_{PULLUP}$ = 2.5k, $C_L$ = 15pF, $V_{CM}$ = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

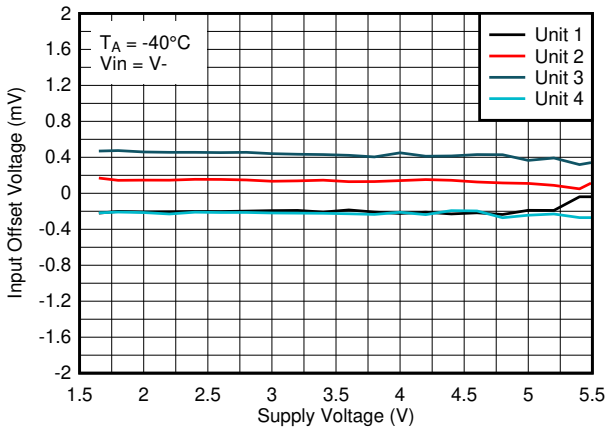


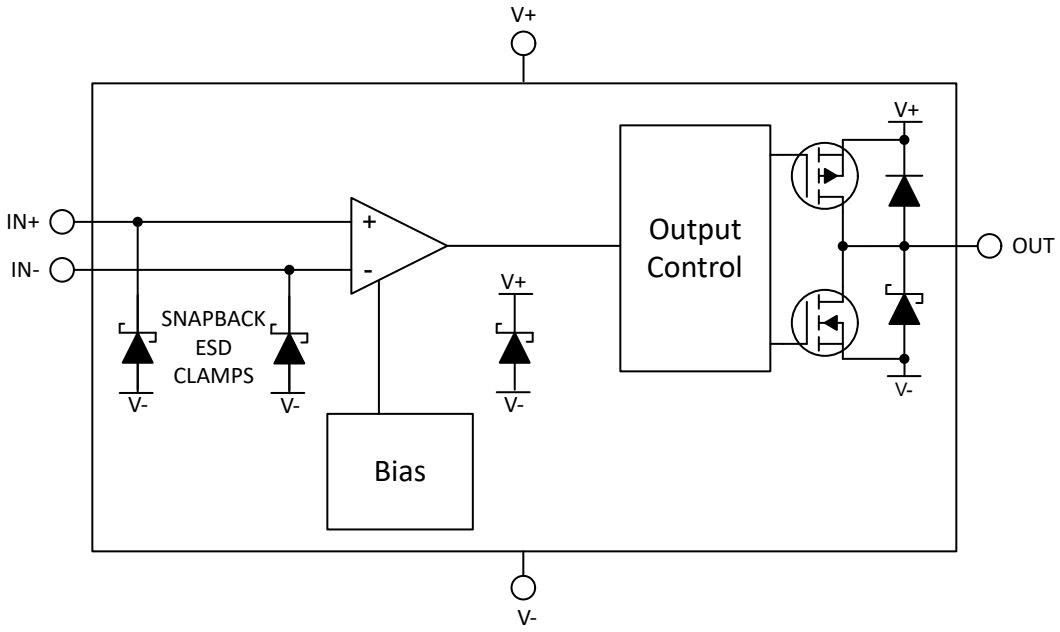

**図 6-25. Offset Voltage vs. Supply Voltage at -40°C, $V_{IN}$=V-**

# 7 Detailed Description

## 7.1 Overview

The TLV4H290-SEP and TLV4H390-SEP devices are quad channel Space Grade Enhanced Products, micro-power comparators with push-pull and open-drain outputs and low input offset voltage. Operating down to 1.65V while only consuming only 25µA per channel. The radiation hardened TLVLV4H290-SEP and TLV4390-SEP are designed for low orbit and space applications. Fault-tolerant inputs can tolerate input transients up to the absolute maximum voltage without damage or false outputs.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The TLV4H290-SEP (open-drain output) and TLV4H390-SEP (push-pull output) devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The TLV4H290-SEP and TLV4H390-SEP family feature push-pull and open-drain output stage options and fault-tolerant input pins.

## 7.4 Device Functional Modes

### *7.4.1 Outputs*

#### 7.4.1.1 TLV4H290-SEP Open Drain Output

The TLV4H290-SEP features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 5.5V, independent of the comparator supply voltage ($V_S$). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower pull-up resistor values help increase the rising edge risetime, but at the expense of increasing $V_{OL}$ and higher power dissipation. The risetime is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1MΩ) create an exponential rising edge due to the RC time constant and increase the risetime.

Unused open drain outputs must be left floating, or can be tied to the V- pin if floating pins are not allowed. While an individual output can typically sink up to 125mA, the total combined current for all channels must be less than 200mA.

#### 7.4.1.2 TLV4H390-SEP Push-Pull Output

The TLV4H390-SEP features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output. While an individual output can typically sink and source up to 100mA, the total combined current for all channels must be less than 200mA.

### *7.4.2 Inputs*

#### 7.4.2.1 Fault Tolerant Inputs

The TLV4H290-SEP and TLV4H390-SEP inputs are fault tolerant up to 5.5V independent of $V_S$. Fault tolerant is defined as maintaining the same high input impedance when $V_S$ is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0V and 5.5V, even while $V_S$ is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains the high impedance value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input common-mode range, and the supply voltage is valid, the output state is correct.

The following is a summary of input voltage excursions and the outcomes:

1. When both IN- and IN+ are within the specified input common-mode voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is outside the specified input common-mode voltage range and IN+ is within the specified common-mode voltage range, the output is low.
3. When IN+ is higher than the specified input common-mode voltage range and IN- is within the specified input common-mode voltage range, the output is high
4. When IN- and IN+ are both outside the specified input common-mode voltage range, the output is **indeterminate** (random). *Do not* operate in this region.

Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

#### 7.4.2.2 Input Protection

The input bias current is typically 5pA for input voltages between V+ and V-. The comparator inputs are protected from reverse voltage by the internal ESD diodes connected to V-. As the input voltage goes under V-, or above the input Absolute Maximum ratings the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct. The current must be limited 10mA or less. This series resistance can be part of any resistive input dividers or networks.

### *7.4.3 ESD Protection*

The TLV4H290-SEP and TLV4H390-SEP family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to V-, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapback "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener.

The TLV4H290-SEP open-drain output protection also consists of a ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 5.5V.

The TLV4H390-SEP push-pull output protection consists of a ESD clamp between the output and V-, but also includes a ESD diode clamp to V+, as the output must not exceed the supply rails.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents the clamps conduct. The current must be limited 10mA or less. This series resistance can be part of any resistive input dividers or networks. TI does not specify the performance of the ESD clamps and external clamping must be added if the inputs or output exceeds the maximum ratings as part of normal operation.

### *7.4.4 Unused Inputs*

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency "chatter" as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ as long as the input is directly connected to the V+ pin (to avoid transients).

### *7.4.5 Hysteresis*

The TLV4H290-SEP and TLV4H390-SEP family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, there is a possiblity for the output to "chatter" when the absolute differential voltage near zero as the comparator triggers on it's own internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See セクション 8.1.2 in the following section.

# 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### *8.1.1 Basic Comparator Definitions*

#### 8.1.1.1 Operation

The basic comparator compares the input voltage ($V_{IN}$) on one input to a reference voltage ($V_{REF}$) on the other input. In the 図 8-1 example below, if $V_{IN}$ is less than $V_{REF}$, the output voltage ($V_O$) is logic low ($V_{OL}$). If $V_{IN}$ is greater than $V_{REF}$, the output voltage ($V_O$) is at logic high ($V_{OH}$). 表 8-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

**表 8-1. Output Conditions**

| Inputs Condition | Output |
|---|---|
| IN+ > IN- | HIGH ($V_{OH}$) |
| IN+ = IN- | Indeterminate (chatters - see Hysteresis) |
| IN+ < IN- | LOW ($V_{OL}$) |

#### 8.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as $t_{pLH}$ and $t_{pHL}$ in 図 8-1 and is measured from the mid-point of the input to the midpoint of the output.

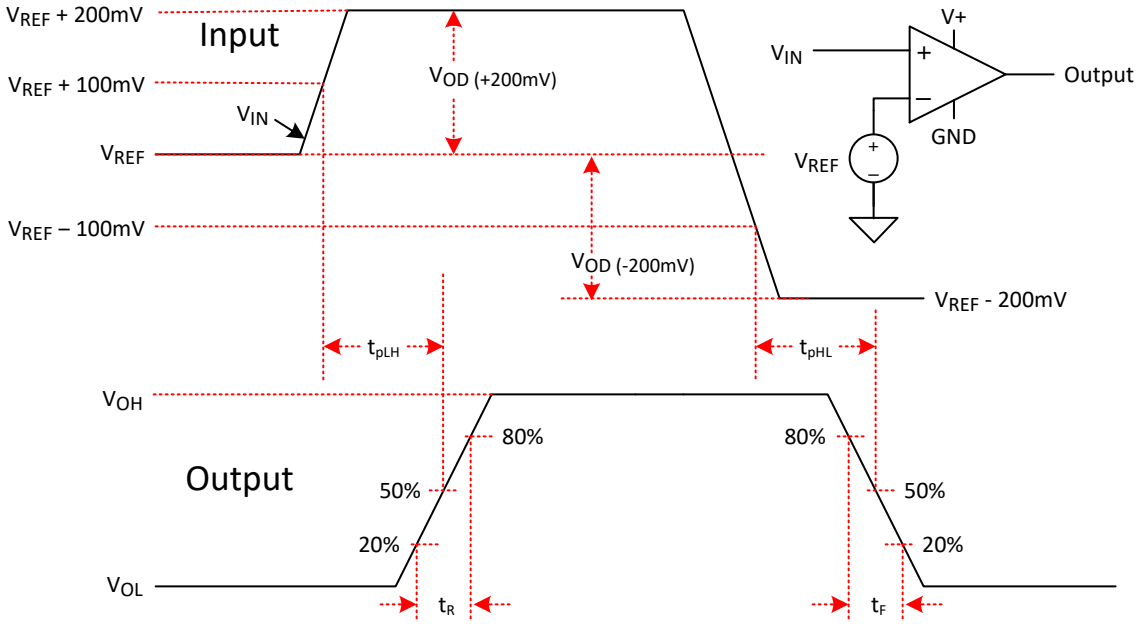



**図 8-1. Comparator Timing Diagram**

#### 8.1.1.3 Overdrive Voltage

The overdrive voltage, $V_{OD}$, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the 図 8-1 example. The overdrive voltage can influence the propagation delay ($t_p$). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, TI recommends applying the highest amount of overdrive possible.

The risetime ($t_r$) and falltime ($t_f$) is the time from the 20% and 80% points of the output waveform.

### *8.1.2 Hysteresis*

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Hysteresis Transfer Curve. This curve is a function of three components: $V_{TH}$, $V_{OS}$, and $V_{HYST}$:

- $V_{TH}$ is the actual set voltage or threshold trip voltage.
- $V_{OS}$ is the internal offset voltage between $V_{IN+}$ and $V_{IN–}$. This voltage is added to $V_{TH}$ to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$ is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

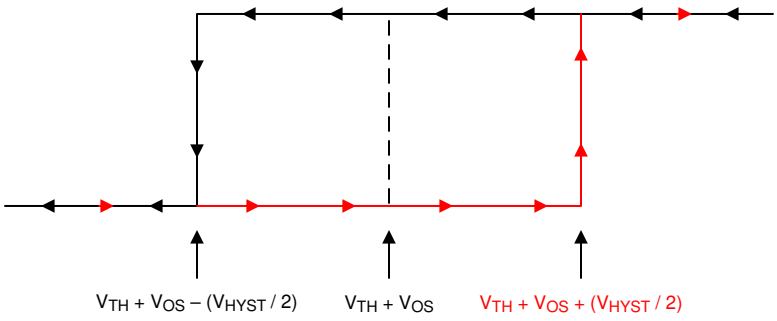



**図 8-2. Hysteresis Transfer Curve**

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

#### 8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V+), as shown in 図 8-3.

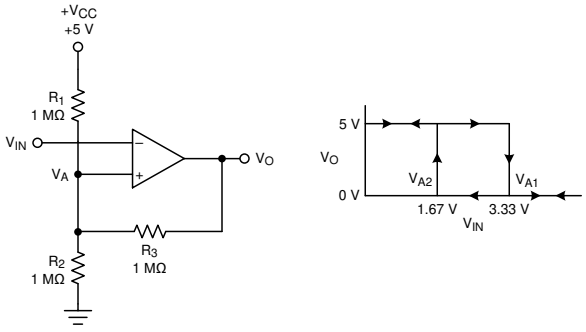



**図 8-3. TLV4H390-SEP in an Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in 図 8-3.

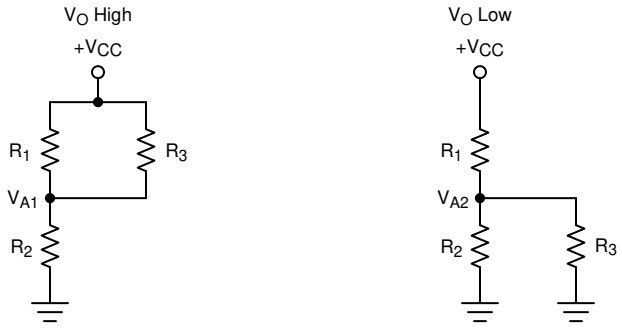



**図 8-4. Inverting Configuration Resistor Equivalent Networks**

When $V_{IN}$ is less than $V_A$, the output voltage is high (for simplicity, assume $V_O$ switches as high as $V_{CC}$). The three network resistors can be represented as R1 || R3 in series with R2, as shown in 図 8-4.

式 1 below defines the high-to-low trip voltage ($V_{A1}$).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When $V_{IN}$ is greater than $V_A$, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in 式 2.

Use 式 2 to define the low to high trip voltage ($V_{A2}$).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

#### 8.1.2.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference ($V_{REF}$) at the inverting input, as shown in TLV4H390-SEP in a Non-Inverting Configuration With Hysteresis,

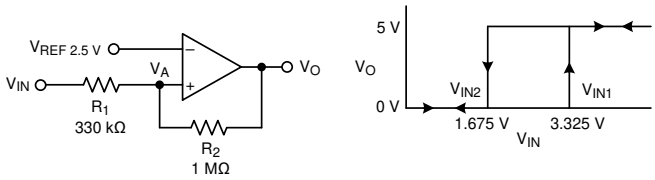



**図 8-5. TLV4H390-SEP in a Non-Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in Non-Inverting Configuration Resistor Networks.

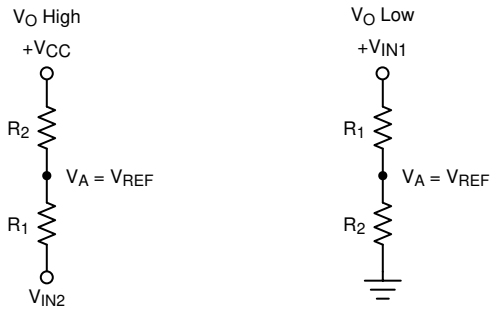



**図 8-6. Non-Inverting Configuration Resistor Networks**

When $V_{IN}$ is less than $V_{REF}$,, the output is low. For the output to switch from low to high, $V_{IN}$ must rise above the $V_{IN1}$ threshold. Use 式 4 to calculate $V_{IN1}$.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When $V_{IN}$ is greater than $V_{REF}$, the output is high. For the comparator to switch back to a low state, $V_{IN}$ must drop below $V_{IN2}$. Use 式 5 to calculate $V_{IN2}$.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between $V_{IN1}$ and $V_{IN2}$, as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

#### 8.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

An open drain output device, such as the TLV4H390-SEP, can also be used, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + $R_{PULLUP}$. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

## 8.2 Typical Applications

### *8.2.1 Window Comparator*

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 図 8-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV4H290-SEP) if the outputs are directly connected together.

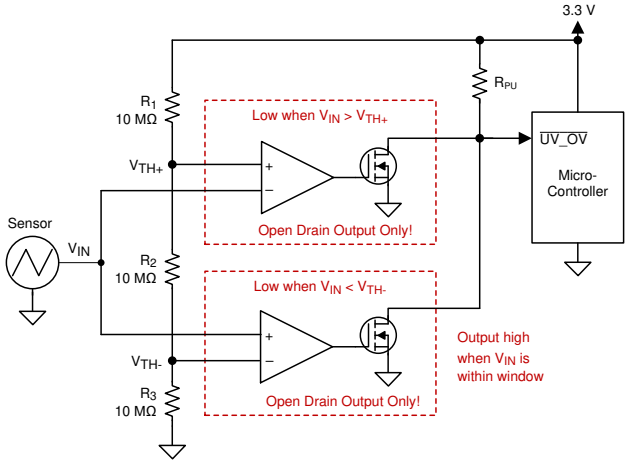



**図 8-7. Window Comparator**

#### 8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

#### 8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 8-7. Connect $V_{CC}$ to a 3.3V power supply and $V_{EE}$ to ground. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator ($V_{TH+}$ and $V_{TH–}$).

With each resistor being equal, $V_{TH+}$ is 2.2V and $V_{TH-}$ is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs are low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs are high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in 図 8-8.

#### 8.2.1.3 Application Curve

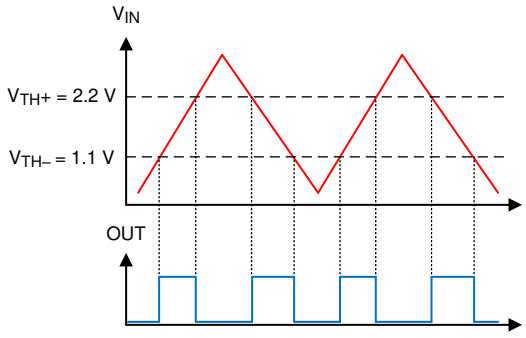



**図 8-8. Window Comparator Results**

For more information, please see Application note SBOA221 "Window comparator circuit".

### 8.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV4H390-SEP) is recommended for best symmetry.

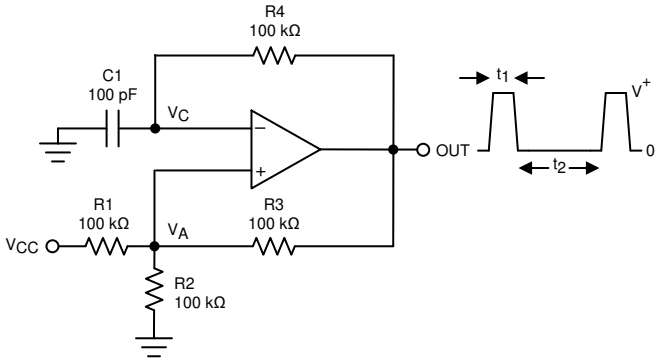



**図 8-9. Square-Wave Oscillator**

#### 8.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor $C_1$ and resistor $R_4$. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which can help to reduce BOM cost and board space. R4 must be over several kilo-ohms to minimize loading the output.

#### 8.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

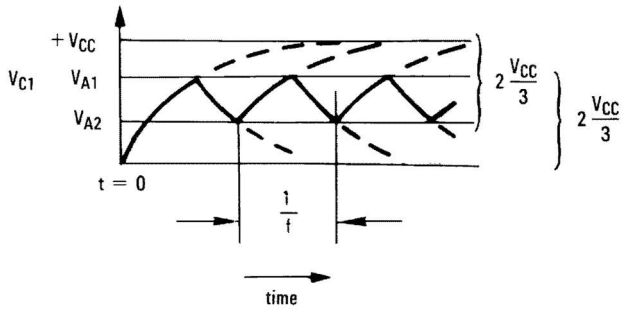



**図 8-10. Square-Wave Oscillator Timing Thresholds**

First consider the output of Figure 図 8-9 as high, which indicates the inverted input $V_C$ is lower than the noninverting input ($V_A$). This causes the $C_1$ to be charged through $R_4$, and the voltage $V_C$ increases until the inverting input is equal to the noninverting input. The value of $V_A$ at the point is calculated by 式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by 式 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \quad (8)$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The $C_1$ now discharges though the $R_4$, and the voltage $V_{CC}$ decreases until the input reaches $V_{A2}$. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for $C_1$ from $2V_{CC}/3$ to $V_{CC}$ / 3 then back to $2V_{CC}/3$, which is given by $R_4C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2\ R_4C_1 \times \ln 2$.

The oscillation frequency can be obtained by 式 9:

$$f = 1/(2\ R4 \times C1 \times In2) \quad (9)$$

#### 8.2.2.3 Application Curve

図 8-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100k\Omega$
- $C_1 = 100pF$, $C_L = 20pF$
- V+ = 5V, V– = GND
- $C_{stray}$ (not shown) from $V_A$ TO GND = 10pF

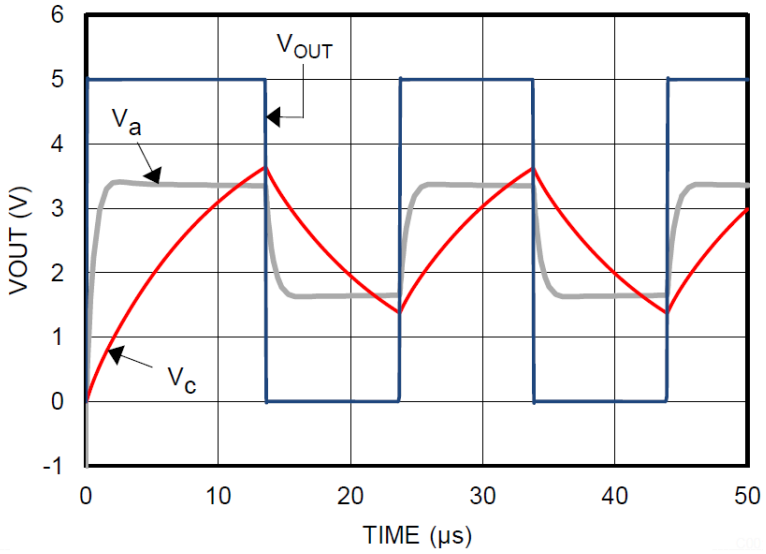



**図 8-11. Square-Wave Oscillator Output Waveform**

### *8.2.3 Adjustable Pulse Width Generator*

The *Adjustable Pulse Width Generator* is a variation on the Square-Wave Oscillator that allows adjusting the pulse widths.

$R_4$ and $R_5$ provide separate charge and discharge paths for the capacitor C depending on the output state.

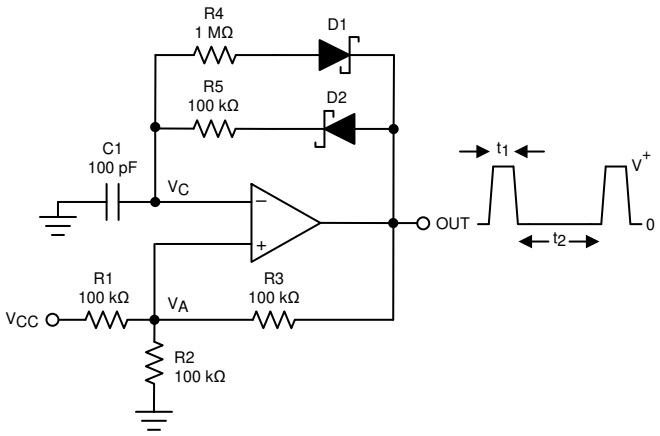



**図 8-12. Adjustable Pulse Width Generator**

The charge path is set through $R_5$ and $D_2$ when the output is high. Similarly, the discharge path for the capacitor is set by $R_4$ and $D_1$ when the output is low.

The pulse width $t_1$ is determined by the RC time constant of $R_5$ and C. Thus, the time $t_2$ between the pulses can be changed by varying $R_4$, and the pulse width can be altered by $R_5$. The frequency of the output can be changed by varying both $R_4$ and $R_5$. At low voltages, the effects of the diode forward drop (0.8V, or 0.15V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

### *8.2.4 Time Delay Generator*

The circuit shown in 図 8-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

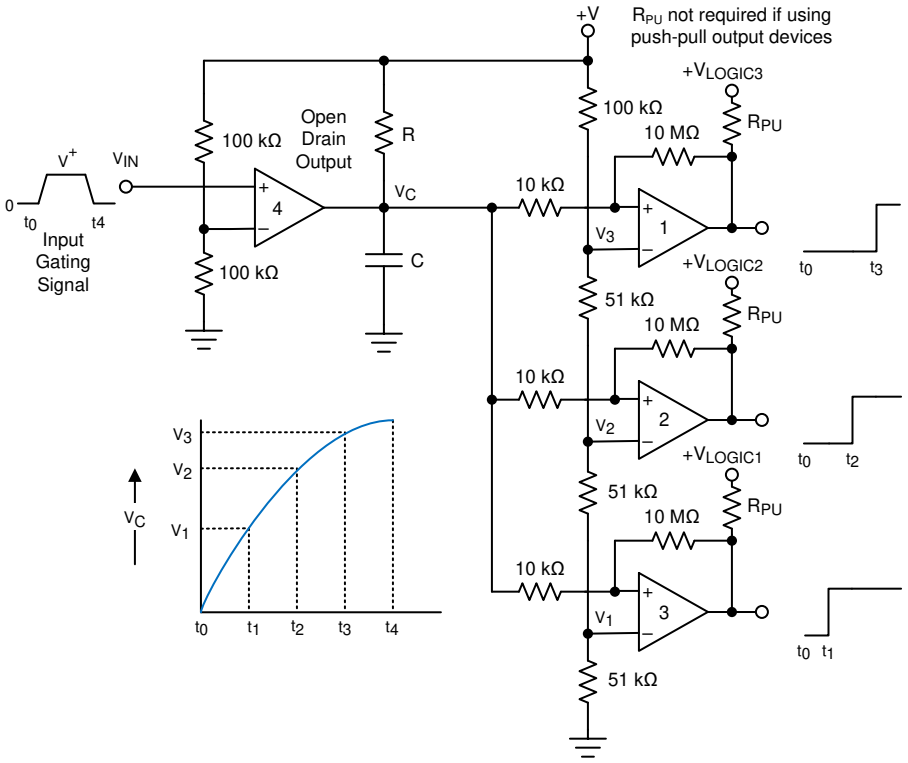



**図 8-13. Time Delay Generator**

Consider the case of $V_{IN}$ = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when $V_C$ rises above the reference voltages $V_1$, $V_2$ and $V_3$. A small amount of hysteresis has been provided by the 10kΩ and 10MΩ resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100kΩ and C = 0.01µF to 1µF.

All outputs immediately go low when $V_{IN}$ falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV4H290-SEP), whereas comparators 1 though 3 can be either open drain or push-pull output, depending on system requirements. $R_{PU}$ is not required for push-pull output devices.

### *8.2.5 Logic Level Shifter*

The output of the TLV4H290-SEP is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

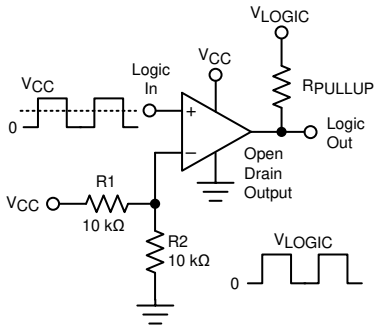



**図 8-14. Universal Logic Level Shifter**

The two 10kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and can be connected to any pull-up voltage between 0V and 5.5V. The pullup voltage must match the driven logic input "high" level.

### *8.2.6 One-Shot Multivibrator*

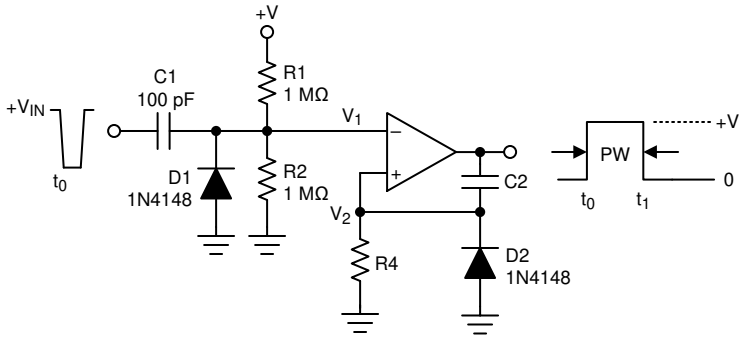



**図 8-15. One-Shot Multivibrator**

A monostable multivibrator has one stable state in which the output can remain indefinitely. The circuit can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of $C_2$ and $R_4$. The resistor divider of $R_1$ and $R_2$ can be used to determine the magnitude of the input trigger pulse. The output chnages state when $V_1 < V_2$. Diode $D_2$

provides a rapid discharge path for capacitor $C_2$ to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

### 8.2.7 Bi-Stable Multivibrator

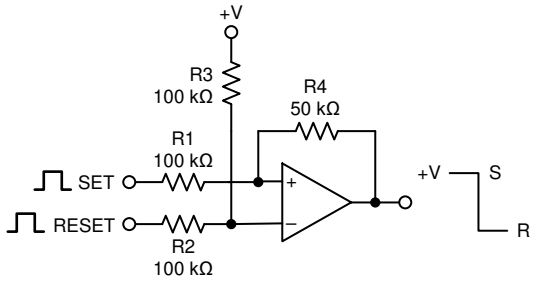



**図 8-16. Bi-Stable Multivibrator**

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of $R_2$ and $R_3$. A pulse applied to the SET terminal sets the output of the comparator high. The resistor divider of $R_1$, $R_4$, and $R_5$ now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET toggles the output low.

### 8.2.8 Zero Crossing Detector

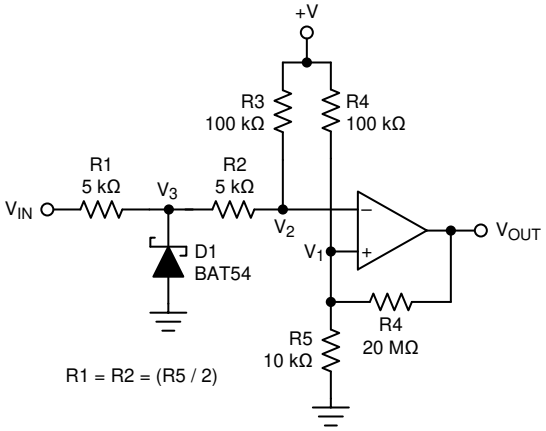



**図 8-17. Zero Crossing Detector**

A voltage divider of $R_4$ and $R_5$ establishes a reference voltage $V_1$ at the non-inverting input. By making the series resistance of $R_1$ and $R_2$ equal to $R_5$, the comparator switches when $V_{IN}$ = 0. Diode $D_1$ imakes sure that $V_3$ clamps near ground. The voltage divider of $R_2$ and $R_3$ then prevents $V_2$ from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

### 8.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of $R_1$ and $C_1$ establishes an mean reference voltage $V_{REF}$, which tracks the mean amplitude of the $V_{IN}$ signal. The noninverting input is directly connected to $V_{REF}$ through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, TI recommends that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs can suffer from timing distortions caused by the changing $V_{REF}$ average voltage.

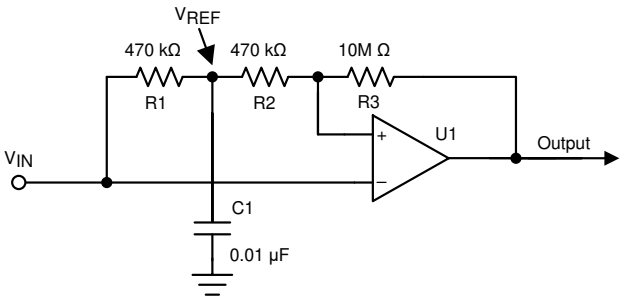



**図 8-18. Pulse Slicer using TLV4H390-SEP**

For this design, follow these design requirements:

- The RC constant value ($R_2$ and $C_1$) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with $R_2$ and $R_{43}$ helps to avoid spurious output toggles.

The TLV4H290-SEP may also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

図 8-19 shows the results of a 9600 baud data signal riding on a varying baseline.

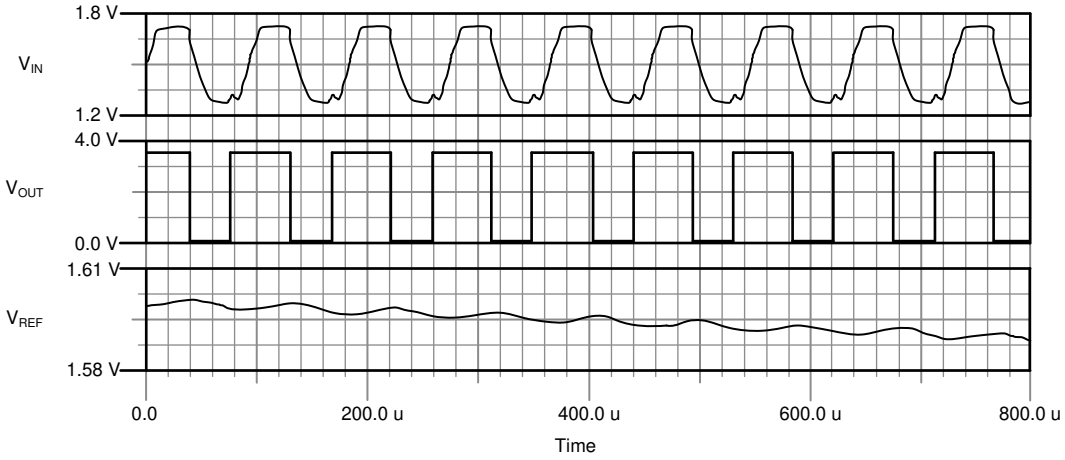



**図 8-19. Pulse Slicer Waveforms**

## 8.3 Power Supply Recommendations

Due to the fast output edges, bypass capacitors are critical to have on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between $V_{CC}$ pin and ground pins. Narrow, peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from either "split" supplies (V+, V- & GND), or a "single" supply (V+ and GND), with GND applied to the V- pin.

Input signals must stay within the specified input range (between V+ and V-) for either type.

Note that on "split" supplies, the output now swings "low" ($V_{OL}$) to V- potential and not GND.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For accurate comparator applications, a stable power supply with minimized noise and glitches is required. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the $V_{CC}$ and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a $V_{CC}$ or GND trace between output to reduce coupling. When series resistance is added to inputs, place the resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

### 8.4.2 Layout Example

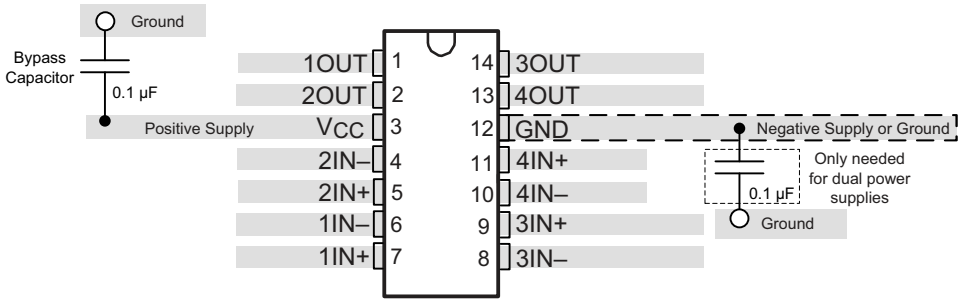



**図 8-20. Layout Example**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

*Analog Engineers Circuit Cookbook: Amplifiers* (See Comparators section) - SLYY137

*Precision Design, Comparator with Hysteresis Reference Design*— TIDU020

*Window comparator circuit* - SBOA221

*Reference Design, Window Comparator Reference Design*— TIPD178

*Comparator with and without hysteresis circuit* - SBOA219

*Inverting comparator with hysteresis circuit* - SNOA997

*Non-Inverting Comparator With Hysteresis Circuit* - SBOA313

*Zero crossing detection using comparator circuit* - SNOA999

*PWM generator circuit* - SBOA212

*How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications* - SNOAA41

*A Quad of Independently Func Comparators* - SNOA654

## 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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## 9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision * (May 2024) to Revision A (December 2024)** **Page**

- 量産データのリリース....1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P4H390MDYYTSEP | ACTIVE | SOT-23-THIN | DYY | 14 | 250 | TBD | Call TI | Call TI | -55 to 125 | | Samples |
| TLV4H290MDYYTSEP | ACTIVE | SOT-23-THIN | DYY | 14 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | (4H290SEP, T4H290SEP) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

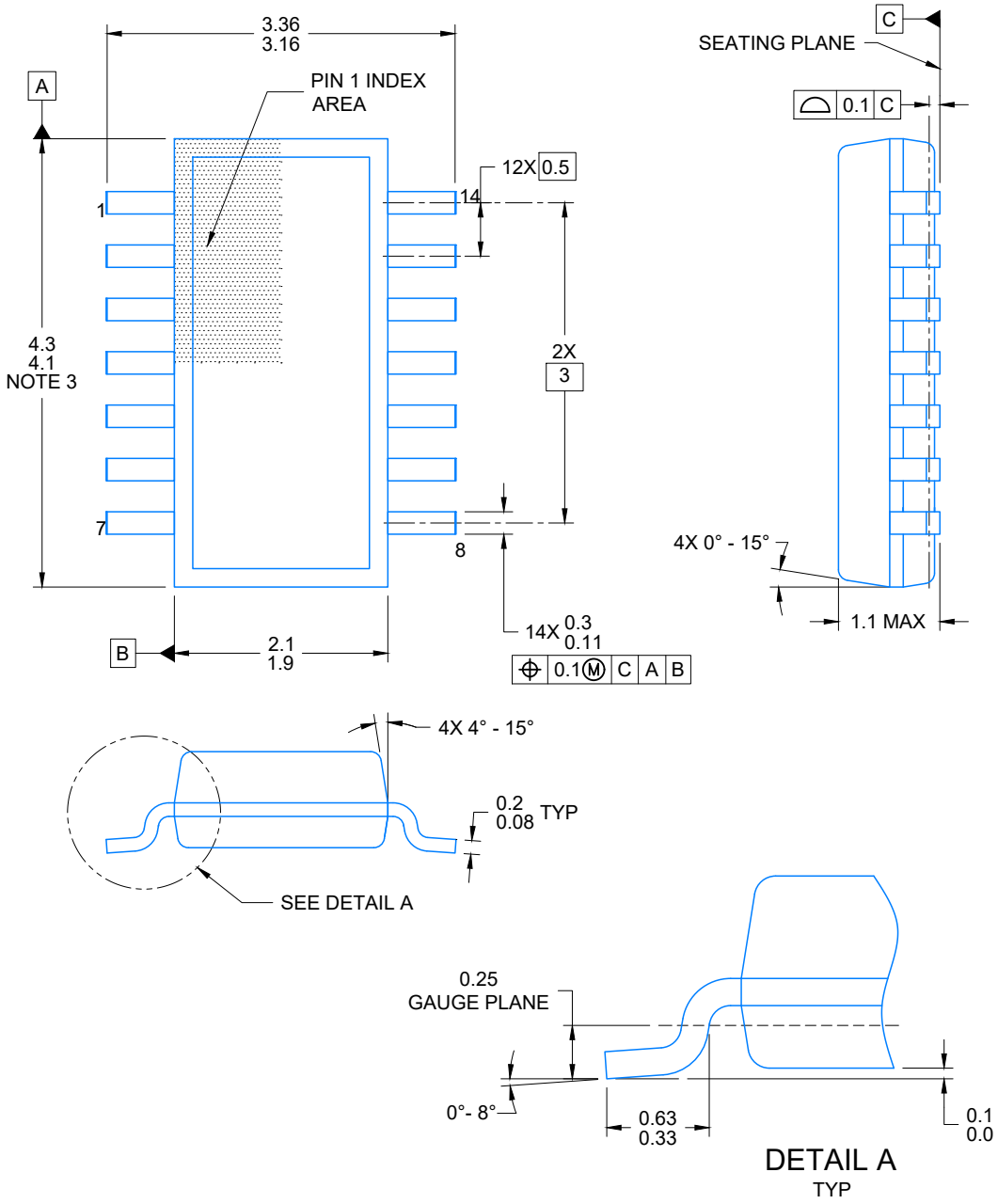
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE OUTLINE

## DYY0014A

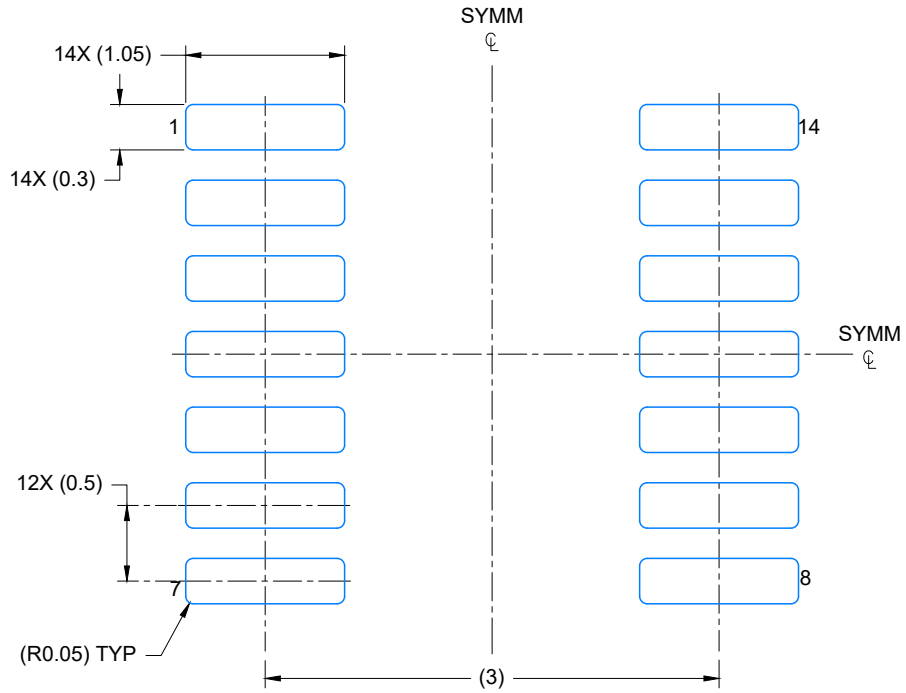
## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

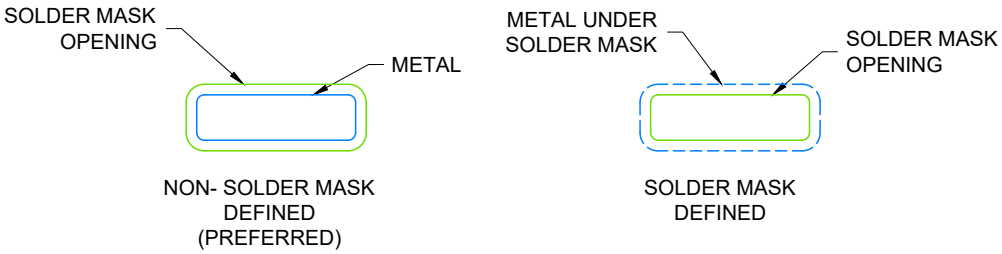



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

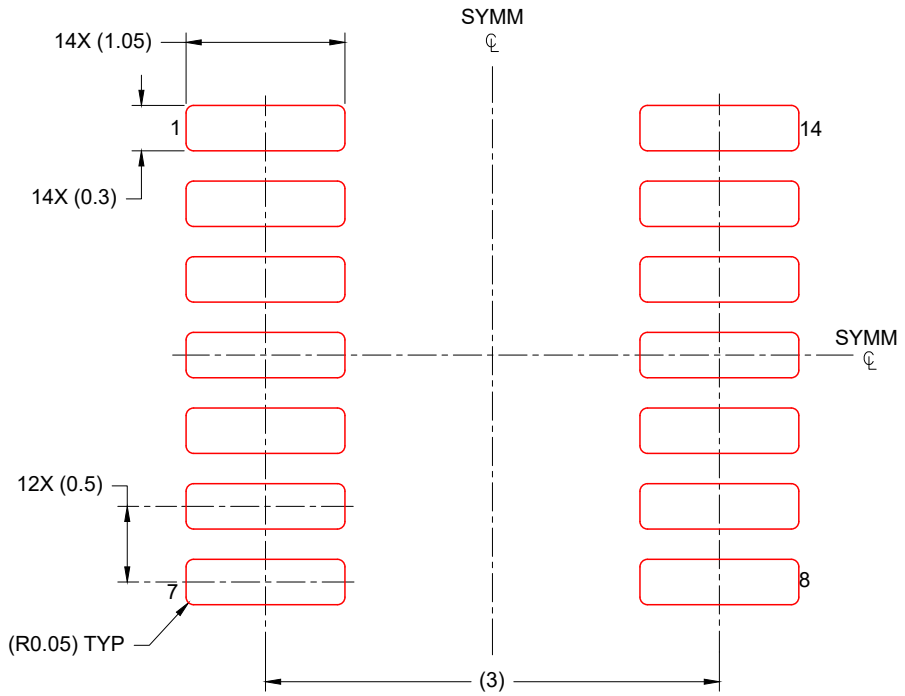



SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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