

TLV323x レール ツー レール入力の 20ns 高速コンパレータ

1 特長

- 伝搬遅延: 20ns
- 入力オフセット電圧: $\pm 4\text{mV}$ (最大値)
- 低い消費電流: 200 μA (チャンネルあたり)
- 各レールから 100mV 拡張された入力電圧同相範囲
- 内部ヒステリシス: 1.55 mV
- 既知の起動条件を提供するパワーオンリセット (デュアルチャンネルのみ)
- プッシュプル出力
- 温度範囲: $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$

2 アプリケーション

- 携帯電話、タブレット
- ヘッドセット / ヘッドホン、小型イヤホン
- PC、ノート PC
- ガス検出器
- 煙感知器、熱感知器
- モーション センサ
- ガス メーター
- サーボドライブ位置センサ

3 概要

TLV323x は、プッシュプル出力を備えた 5V シングルおよびデュアル チャンネル コンパレータのファミリです。このファミリは速度と消費電力の組み合わせが非常に優れており、伝搬遅延は 20ns、電源電圧範囲は 2.7V~5V で、チャンネルあたりの静止時電流はわずか 200 μA です。

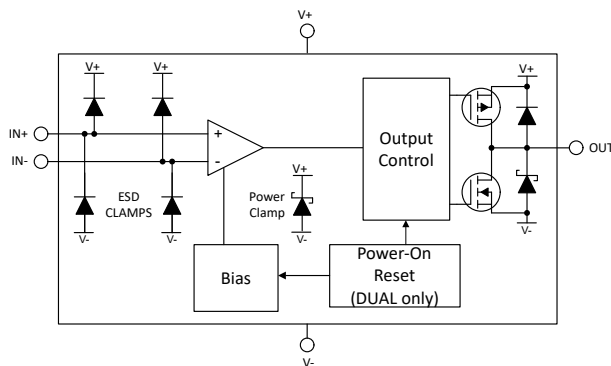
同様に、TLV323x は標準のリード付きおよびリードレスパッケージで供給され、レール ツー レール入力、低オフセット電圧、大きな出力駆動電流などの特長があります。これらの特長と高速な応答時間により、本コンパレータは電流センシング、ゼロクロス検出、その他精度と速度が重要なさまざまなアプリケーションに最適です。

すべてのデバイスは、 $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$ の拡張工業用温度範囲で仕様が規定されています。

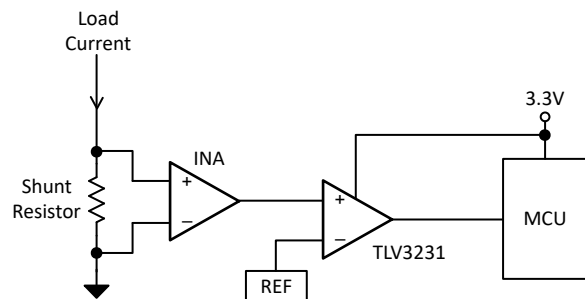
製品情報

部品番号	パッケージ (1)	本体サイズ (公称) (2)
TLV3231	SC-70 (5)	1.25mm × 2.00mm
	SOT-23 (5)	1.60mm × 2.90mm
TLV3232	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	2.00mm × 2.00mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



ブロック図



ローサイド電流センシング

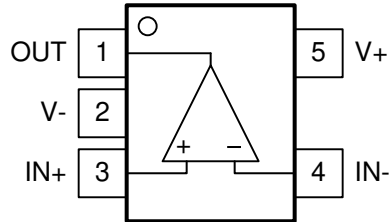


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4 Pin Configuration and Functions

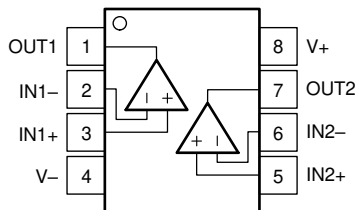
Pin Configurations: TLV3231 and TLV3232



**DCK, DBV Packages
SC70, SOT-23-5
Top View
(Standard "North West" Pinout)**

表 4-1. Pin Functions: TLV3231

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output
V-	2	-	Negative supply voltage
IN+	3	I	Non-inverting (+) input
IN-	4	I	Inverting (-) input
V+	5	-	Positive supply voltage



**図 4-1. DGK, DSG Packages
8-Pin VSSOP, WSON
Top View**

表 4-2. Pin Functions: TLV3232

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1-	2	I	Inverting input, channel 1
IN2-	3	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	7	O	Output, channel 1
OUT2	6	O	Output, channel 2
V-	5	-	Negative (lowest) supply or ground
V+	8	-	Positive (highest) supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage $V_S = (V+) - (V-)$		6	V
Differential input voltage, VID	-6	6	V
Input pins (IN+, IN-) from (V-) ⁽²⁾	-0.5	(V+) + 0.5	V
Current into input pins (IN+, IN-)	-10	10	mA
Output short-circuit current	-100	100	mA
Output short-circuit duration		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to (V-) and (V+). Input signals that can swing more than 0.5V beyond the supply rails must be current-limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = (V+) - (V-)$	2.7	5.5	V
Input voltage range	(V-) - 0.1	(V+) + 0.1	V
Ambient temperature, T_A	-40	125	°C

5.4 Thermal Information, TLV3231

THERMAL METRIC ⁽¹⁾		TLV3231		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance		220	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		135	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		65	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		34	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		65	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Thermal Information, TLV3232

THERMAL METRIC ⁽¹⁾		TLV3232		UNIT
		DGK (VSSOP)	DSG (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154.5	78.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.8	99.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	44.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	87.4	44.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	19.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics

$V_S = 2.7V$ to $5V$, $V_{CM} = V_S / 2$; at $T_A = 25^\circ C$ (unless otherwise noted). Typical values are at $T_A = 25^\circ C$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input Offset Voltage	$V_S = 5V$, $V_{CM} = V_S / 2$		± 0.5	± 4	mV
V_{IO}	Input Offset Voltage	$V_S = 5V$, $V_{CM} = V_S / 2$, $T_A = -40$ to $125^\circ C$			± 4.5	mV
V_{HYS}	Hysteresis	$V_S = 5V$, $V_{CM} = V_S / 2$	0.5	1.55	3	mV
V_{HYS}	Hysteresis	$V_S = 5V$, $V_{CM} = V_S / 2$, $T_A = -40$ to $125^\circ C$			3.5	mV
V_{CM}	Common-mode voltage range		(V-) - 0.1		(V+) + 0.1	V
I_B	Input bias current	$V_S = 5V$, $V_{CM} = V_S / 2$, $T_A = -40$ to $125^\circ C$		0.01	10	nA
I_{OS}	Input offset current	$V_S = 5V$, $V_{CM} = V_S / 2$			1	nA
C_{IN}	Input capacitance			2		pF
CMRR	Common-mode rejection ratio	$V_{CM} = V_{EE} - 0.1V$ to $V_{CC} + 0.1V$		82		dB
DC Output Characteristics						
V_{OH}	Voltage swing from (V+)	$V_S = 5V$, (V-) = 0V, $I_{Source} = 2mA$			200	mV
V_{OL}	Voltage swing from (V-)	$V_S = 5V$, (V-) = 0V, $I_{Sink} = 2mA$			200	mV
I_{SC}	Short-circuit current	$V_S = 5V$, sourcing		45		mA
		$V_S = 5V$, sinking		45		
Power Supply						
I_Q	Supply current / Channel	$V_S = 2.7V$ and $5V$, no load, Output Low		200	250	μA
I_Q	Supply current / Channel	$V_S = 2.7V$ and $5V$, no load, Output Low, $T_A = -40$ to $125^\circ C$			350	μA
$V_{POR (positive)}$	Power-On Reset Voltage (dual only)			2.1		V
PSRR	Power Supply Rejection Ratio	$V_S = 1.8V$ to $5.5V$, no load, $T_A = -40$ to $125^\circ C$		92		dB

5.7 Switching Characteristics

For $V_S = 5V$, $V_{CM} = V_S / 2$; $C_L = 15pF$ at $T_A = 25^\circ C$ (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to low	Midpoint of input to midpoint of output, $V_{OD} = 10mV$		22		ns
t_{PHL}	Propagation delay time, high to low	Midpoint of input to midpoint of output, $V_{OD} = 50mV$		15	25	ns
t_{PLH}	Propagation delay time, low to high	Midpoint of input to midpoint of output, $V_{OD} = 10mV$		20		ns
t_{PLH}	Propagation delay time, low to high	Midpoint of input to midpoint of output, $V_{OD} = 50mV$		15	25	ns
f_{TOGGLE}	Input toggle frequency	$V_{IN} = 200mV_{PP}$ Sine Wave, When output high reaches 90% of $V_{CC} - V_{EE}$ or output low reaches 10% of $V_{CC} - V_{EE}$		55		MHz
t_R	Rise time	Measured from 20% to 80%		1.6		ns
t_F	Fall time	Measured from 20% to 80%		1.6		ns
t_{ON}	Power-up time	During power on, (V+) must exceed 2.1V for 4 μs before the output reflects the input.		4.5		μs

5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $C_L = 15\text{pF}$, $V_{CM} = V_S/2\text{V}$, $V_{\text{UNDERDRIVE}} = 50\text{mV}$, $V_{\text{OVERDRIVE}} = 50\text{mV}$ unless otherwise noted.

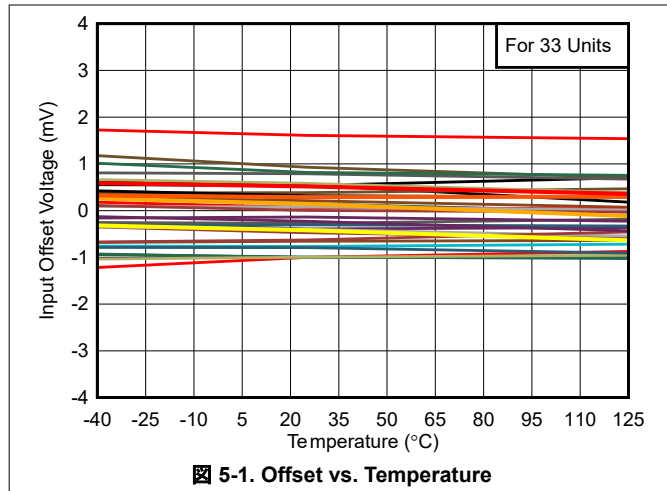


图 5-1. Offset vs. Temperature

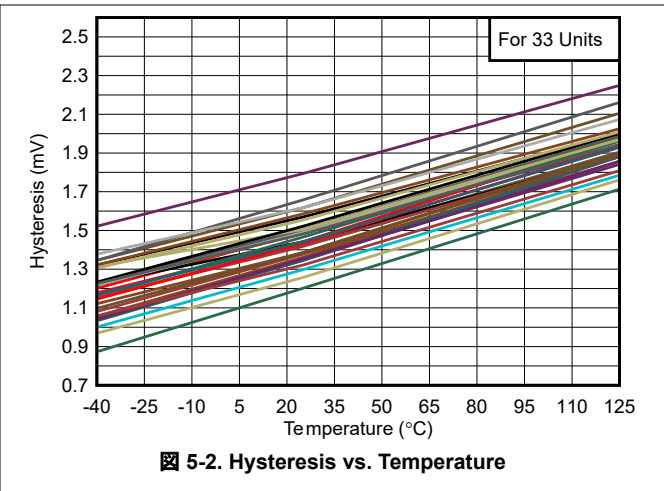


图 5-2. Hysteresis vs. Temperature

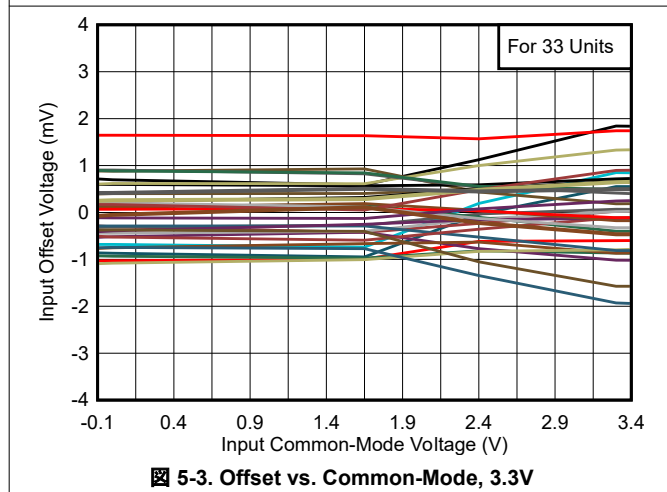


图 5-3. Offset vs. Common-Mode, 3.3V

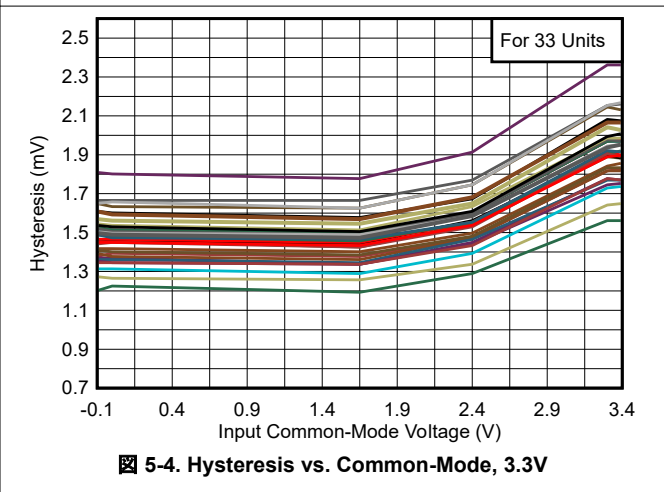


图 5-4. Hysteresis vs. Common-Mode, 3.3V

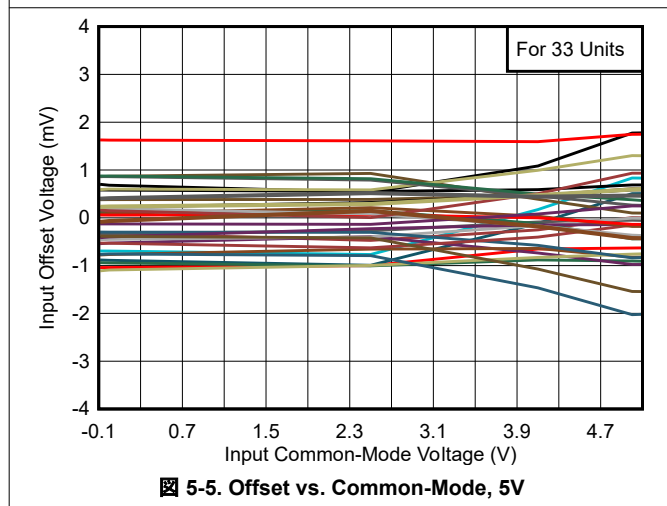


图 5-5. Offset vs. Common-Mode, 5V

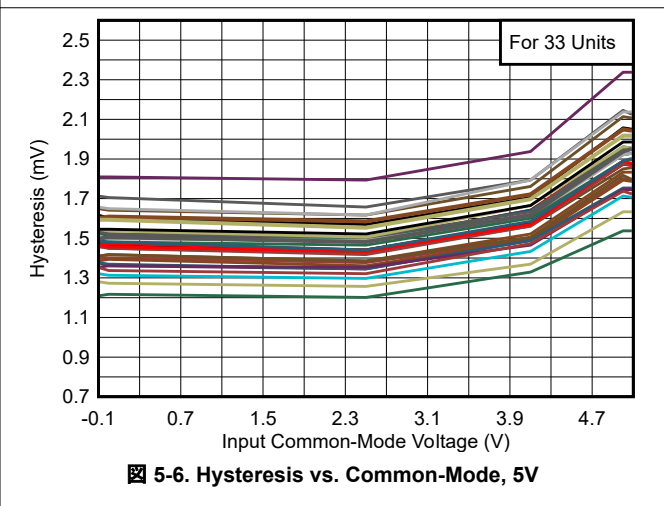
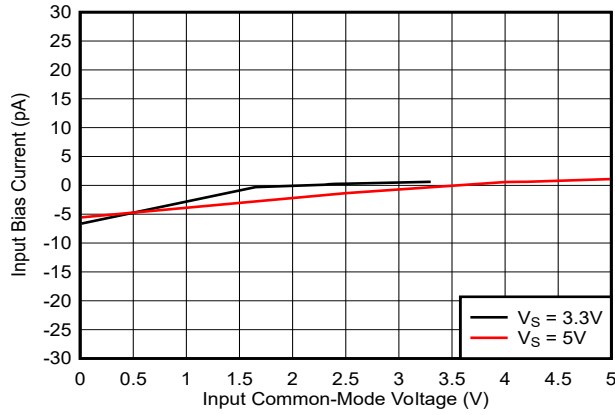


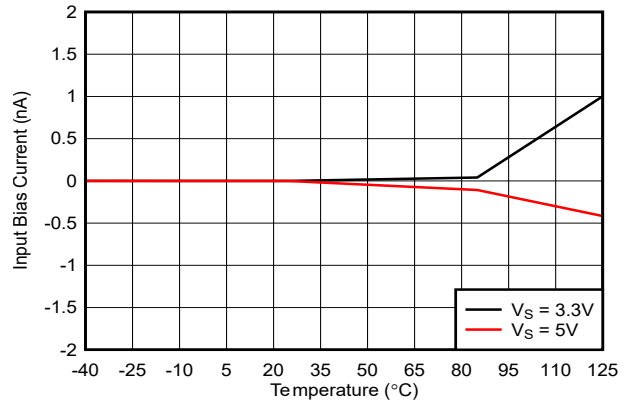
图 5-6. Hysteresis vs. Common-Mode, 5V

5.8 Typical Characteristics (continued)

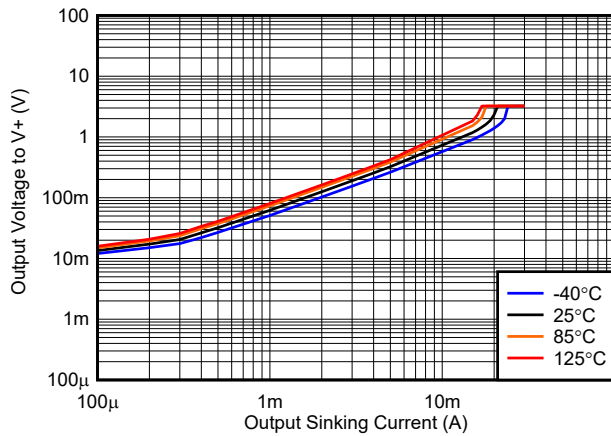
$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $C_L = 15\text{pF}$, $V_{CM} = V_S/2\text{V}$, $V_{UNDERDRIVE} = 50\text{mV}$, $V_{OVERDRIVE} = 50\text{mV}$ unless otherwise noted.



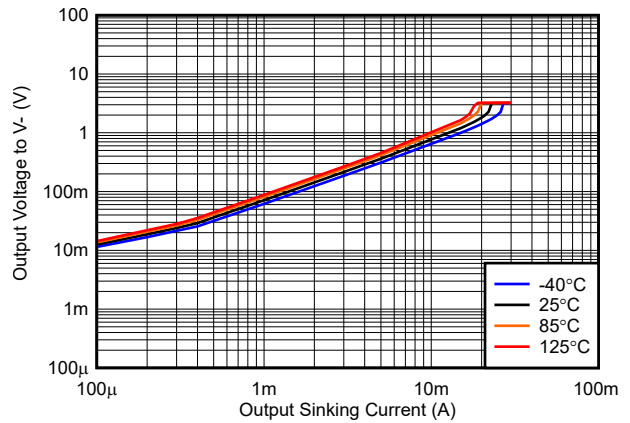
5-7. Bias Current vs. Common-Mode



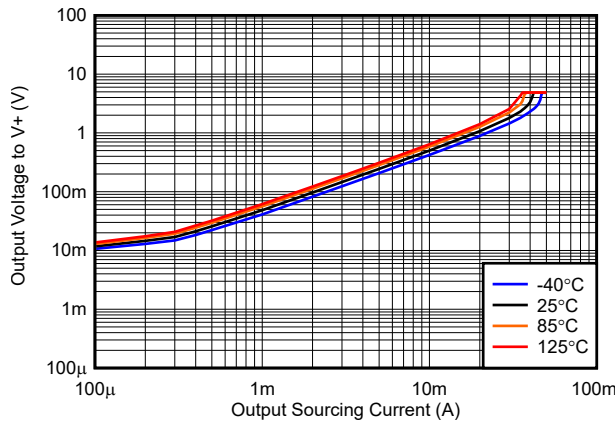
5-8. Bias Current vs. Temperature



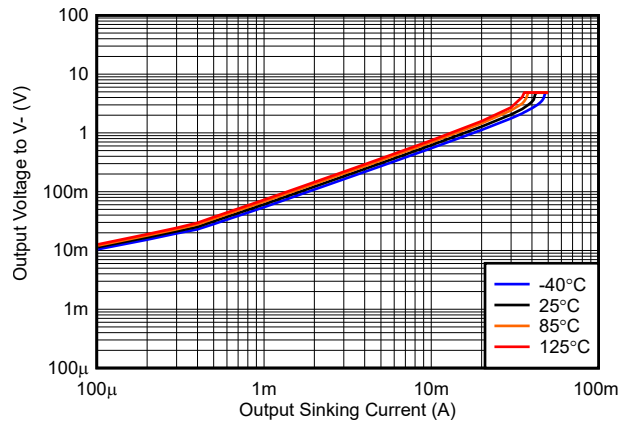
5-9. Output Voltage vs. Output Sourcing Current, 3.3V



5-10. Output Voltage vs. Output Sinking Current, 3.3V



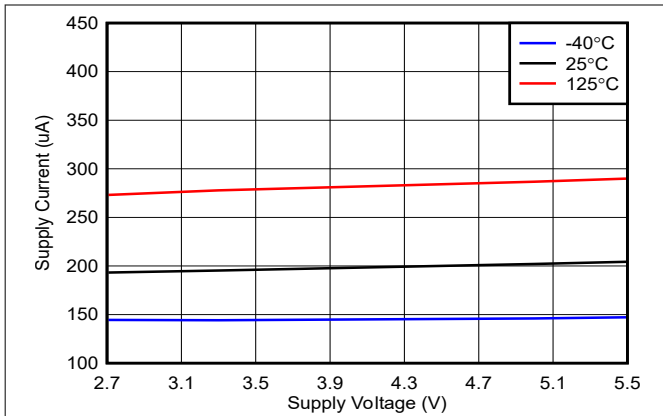
5-11. Output Voltage vs. Output Sourcing Current, 5V



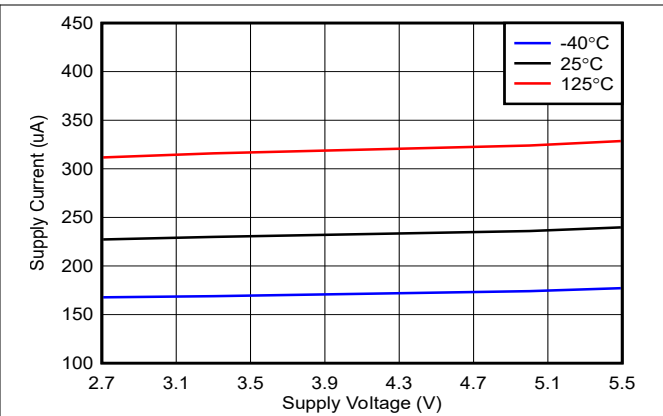
5-12. Output Voltage vs. Output Sinking Current, 5V

5.8 Typical Characteristics (continued)

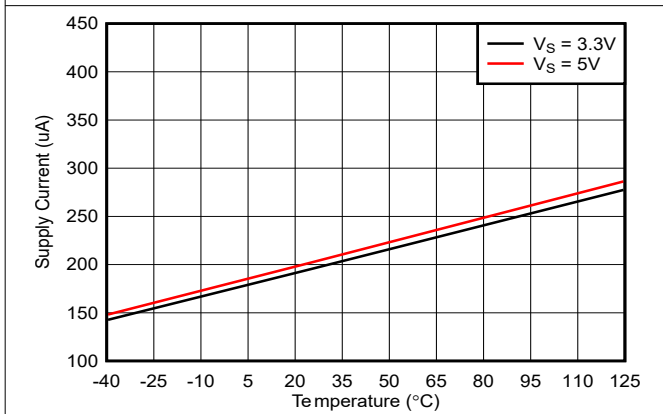
$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $C_L = 15\text{pF}$, $V_{CM} = V_S/2\text{V}$, $V_{UNDERDRIVE} = 50\text{mV}$, $V_{OVERDRIVE} = 50\text{mV}$ unless otherwise noted.



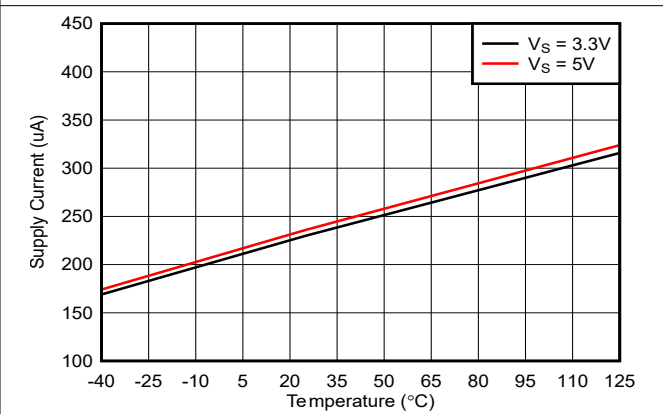
5-13. Supply Current vs. Supply Voltage (Output Low)



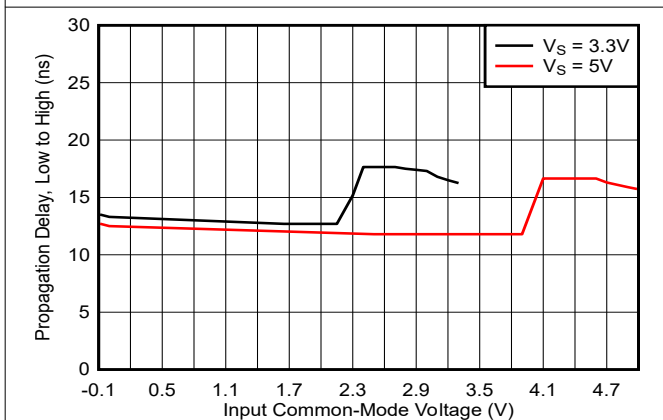
5-14. Supply Current vs. Supply Voltage (Output High)



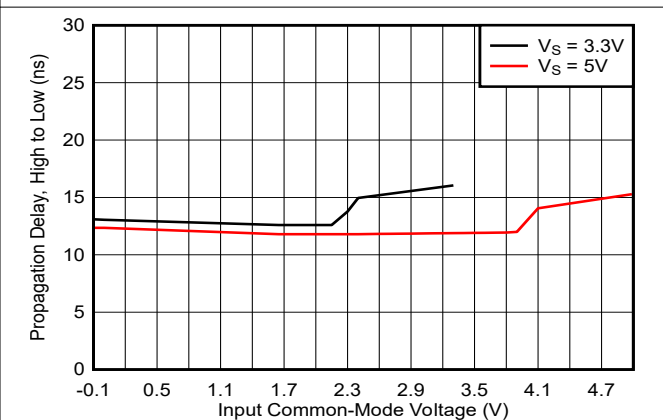
5-15. Supply Current vs. Temperature (Output Low)



5-16. Supply Current vs. Temperature (Output High)



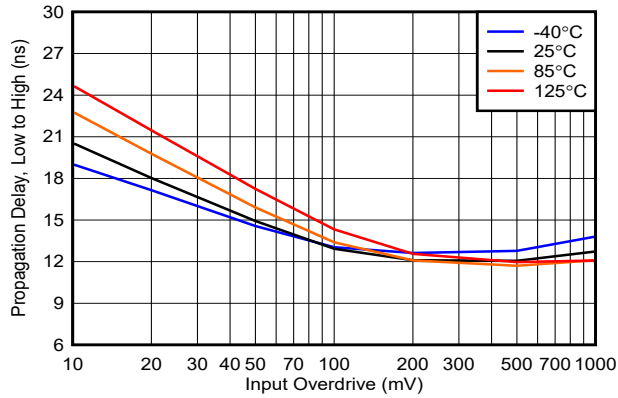
5-17. Propagation Delay (Low to High) vs. Common-Mode



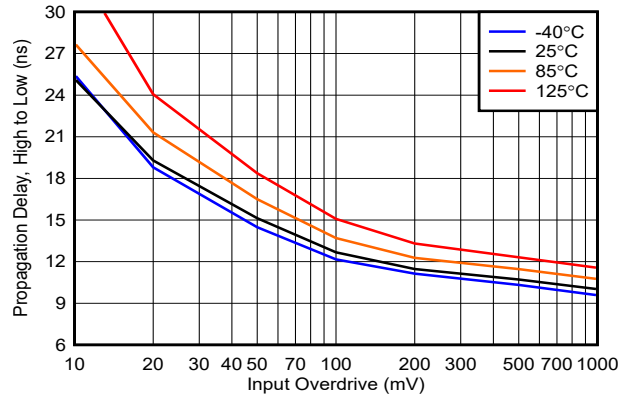
5-18. Propagation Delay (High to Low) vs. Common-Mode

5.8 Typical Characteristics (continued)

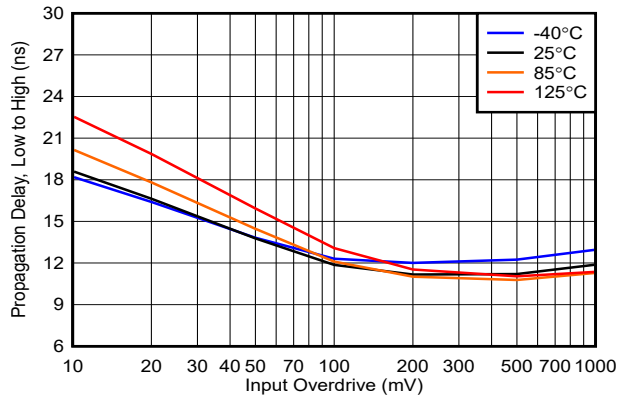
$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $C_L = 15\text{pF}$, $V_{CM} = V_S/2\text{V}$, $V_{UNDERDRIVE} = 50\text{mV}$, $V_{OVERDRIVE} = 50\text{mV}$ unless otherwise noted.



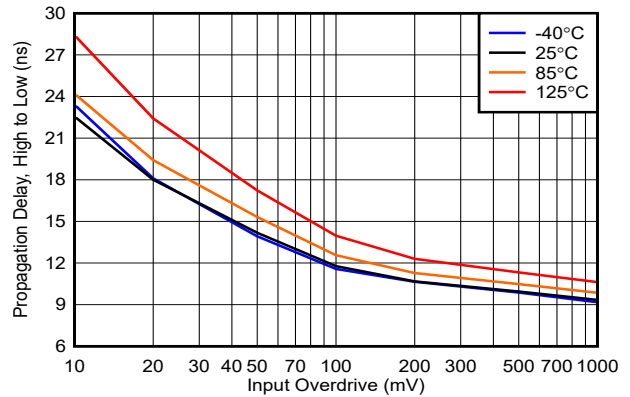
5-19. Propagation Delay (Low to High) vs. Overdrive (3.3V)



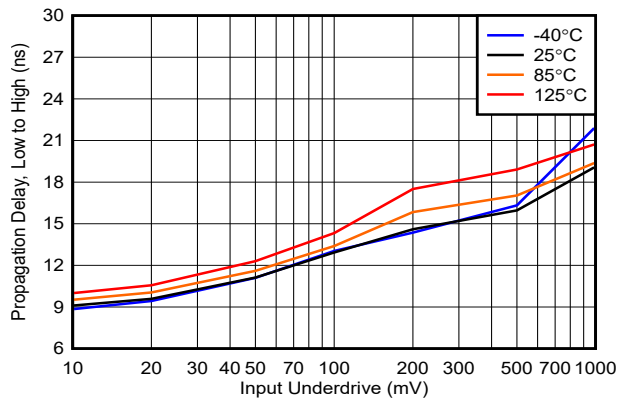
5-20. Propagation Delay (High to Low) vs. Overdrive (3.3V)



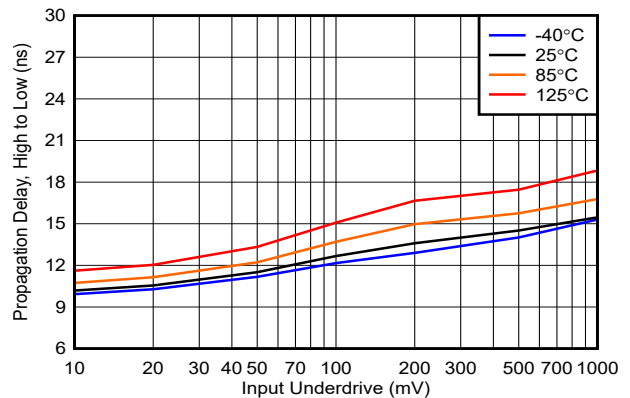
5-21. Propagation Delay (Low to High) vs. Overdrive (5V)



5-22. Propagation Delay (High to Low) vs. Overdrive (5V)



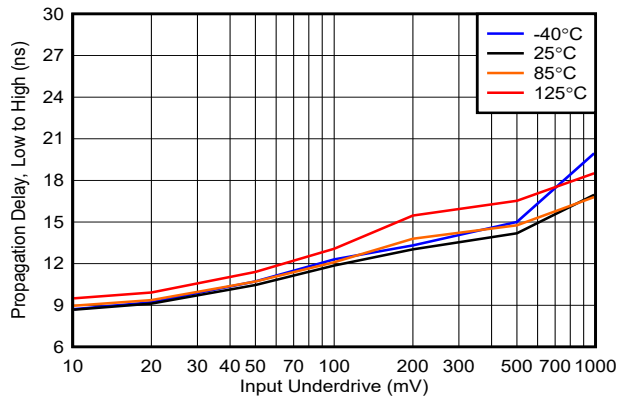
5-23. Propagation Delay (Low to High) vs. Underdrive (3.3V)



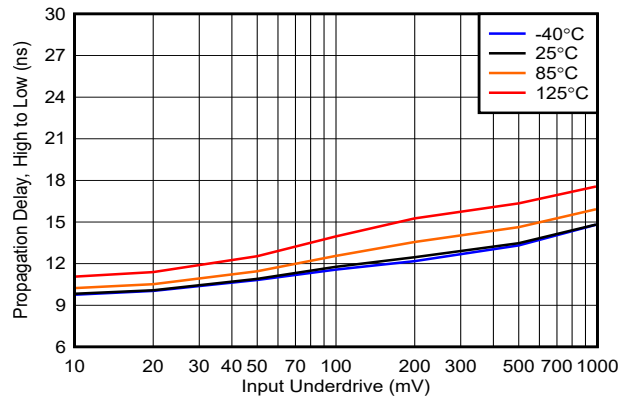
5-24. Propagation Delay (High to Low) vs. Underdrive (3.3V)

5.8 Typical Characteristics (continued)

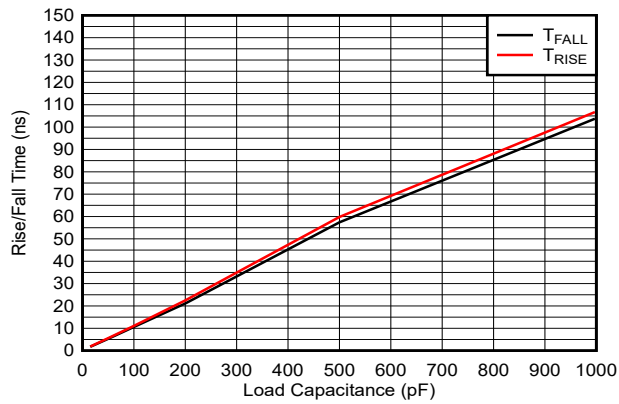
$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $C_L = 15\text{pF}$, $V_{CM} = V_S/2\text{V}$, $V_{UNDERDRIVE} = 50\text{mV}$, $V_{OVERDRIVE} = 50\text{mV}$ unless otherwise noted.



5-25. Propagation Delay (Low to High) vs. Underdrive (5V)



5-26. Propagation Delay (High to Low) vs. Underdrive (5V)



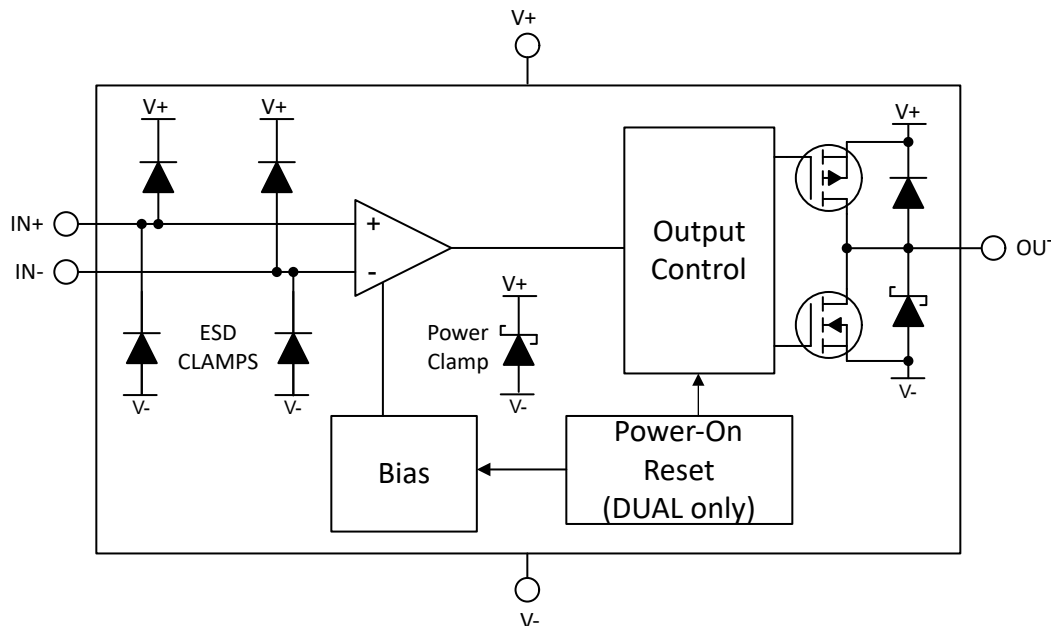
5-27. Rise and Fall Times vs. Capacitive Loads

6 Detailed Description

6.1 Overview

The TLV323x devices are high-speed comparators with push-pull outputs.

6.2 Functional Block Diagrams



6-1. Block Diagram

6.3 Feature Description

The TLV323x consumes 200 μ A per channel with 20ns of propagation delay. The TLV323x detects fast voltage and current transients while maintaining low power consumption with single-ended, push-pull outputs.

6.4 Device Functional Modes

6.4.1 Inputs

The inputs incorporate internal ESD protection circuits to (V+) and (V-). Voltages on the inputs are limited to 0.3V beyond the rails.

When connecting to a low impedance source such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct. Limit the current to 10mA or less. One form of series resistance is any resistive input dividers or networks.

6.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown below. This curve is a function of three components: V_{TH} , V_{OS} , and V_{HYST} :

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-} . This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

(typically 1.55mV for the TLV323x family)

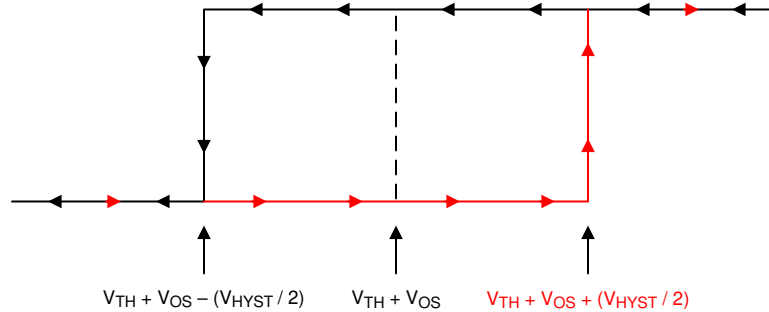


图 6-2. Hysteresis Transfer Curve

6.4.3 Outputs

The TLV323x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

6.4.4 ESD Protection

The inputs and outputs incorporate internal ESD protection circuits to (V+) and (V-).

Voltages on the inputs are limited to 0.3V beyond the rails. If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents in case the clamps conduct. Limit the current to 10mA or less.

6.4.5 Power-On Reset (POR) - Dual Channel Only

The TLV3232 devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 2.5us after the V_{POR} of 2.2V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV3232 devices, the output is held low during the POR period (t_{on}) as shown below.

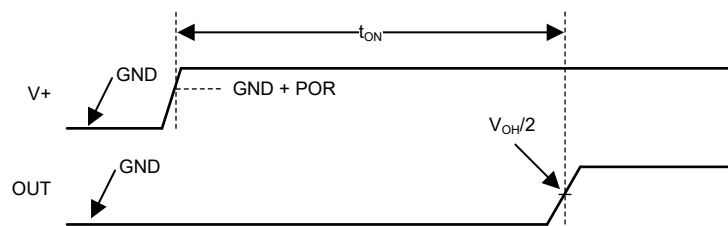


图 6-3. Power-On Reset Timing Diagram

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the [図 7-1](#) example below, if V_{IN} is less than V_{REF} , the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF} , the output voltage (V_O) is at logic high (V_{OH}). [表 7-1](#) summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 7-1. Output Conditions

Inputs Condition	Output
$IN+ > IN-$	HIGH (V_{OH})
$IN+ = IN-$	Indeterminate (chatters - see Hysteresis)
$IN+ < IN-$	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to-low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in [図 7-1](#) and is measured from the mid-point of the input to the midpoint of the output.

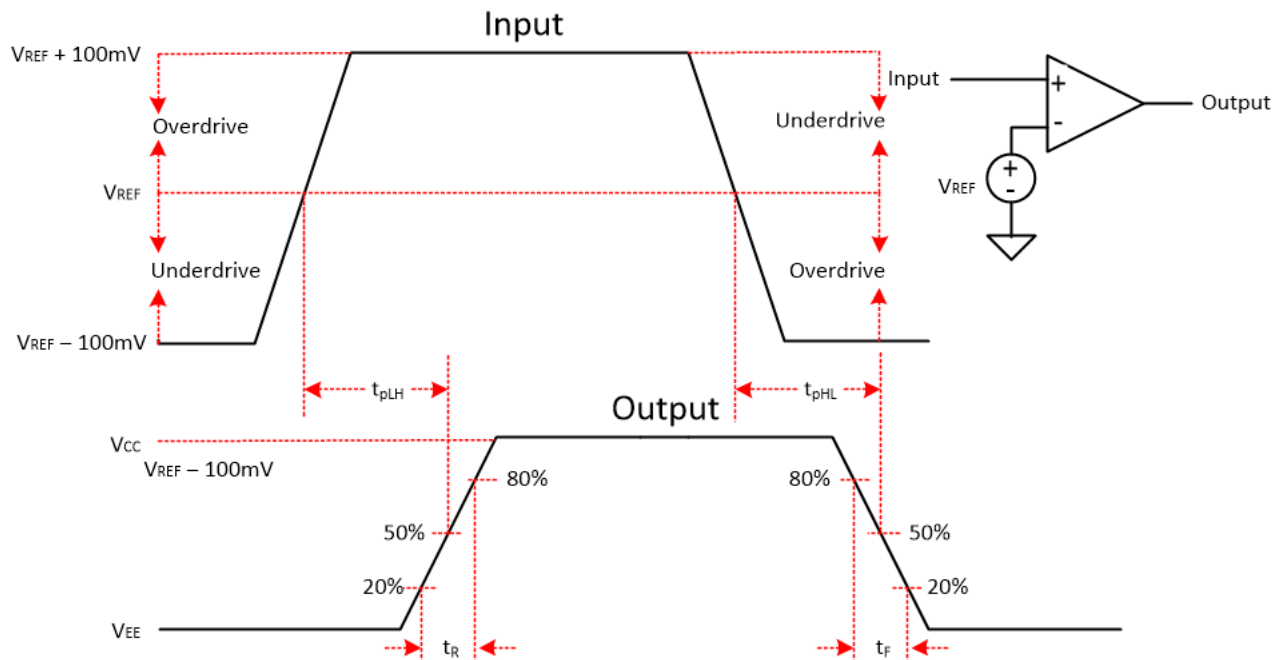


図 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD} , is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when $<100\text{mV}$. If the fastest speeds are desired, TI recommends applying the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration can produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV323x devices only have a minimal amount of internal hysteresis of 1.55mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on the current output state.

The hysteresis transfer curve is shown in [Figure 7-2](#). This curve is a function of three components: V_{TH} , V_{OS} , and V_{HYST} :

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-} . This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

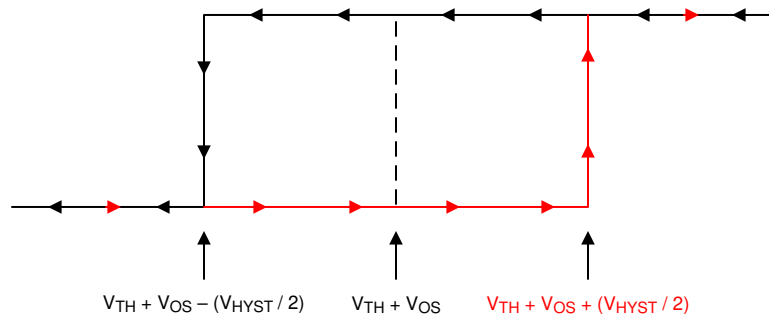


Figure 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "[Comparator with and without hysteresis circuit](#)".

7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in [Figure 7-3](#).

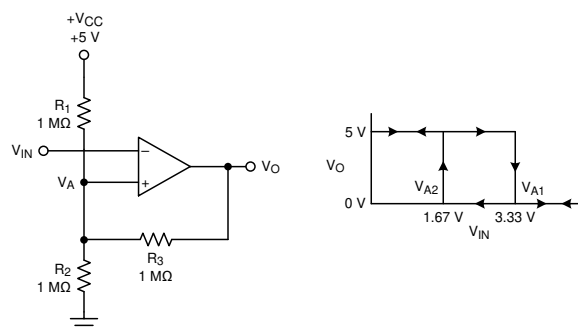


Figure 7-3. TLV3231 in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in [Figure 7-3](#).

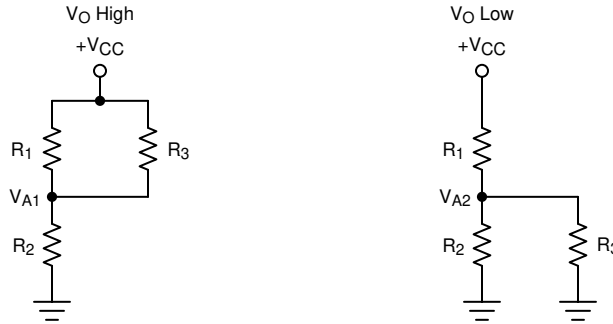


Figure 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A , the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R1 \parallel R3$ in series with $R2$, as shown in [Figure 7-4](#).

[Equation 1](#) below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than V_A , the output voltage is low. In this case, the three network resistors can be presented as $R2 \parallel R3$ in series with $R1$, as shown in [Equation 2](#).

Use [Equation 2](#) to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

[Equation 3](#) defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in [Figure 7-5](#),

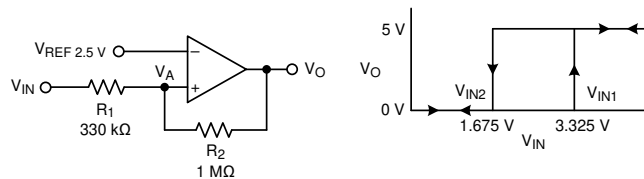


Figure 7-5. TLV3231 in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in [Figure 7-6](#).

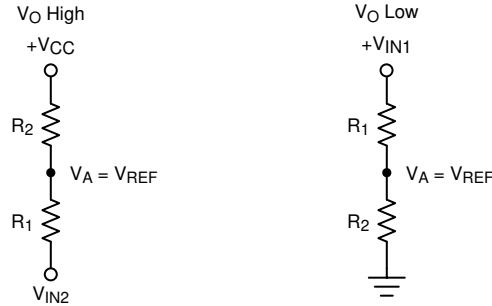


図 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF} , the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use 式 4 to calculate V_{IN1} .

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF} , the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2} . Use 式 5 to calculate V_{IN2} .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2} , as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7.2 Typical Applications

7.2.1 Low-Side Current Sensing

The figure below shows a simple low-side current sensing circuit using a high-speed comparator. Since this design does not utilize an amplifier, the response time is only limited by the propagation delay of the comparator. With faster response time, the design is well-suited for short-circuit detection when speed is more important than accuracy. When the voltage across the shunt resistor reaches the critical over-current threshold created by R1 and R2, the comparator output changes state.

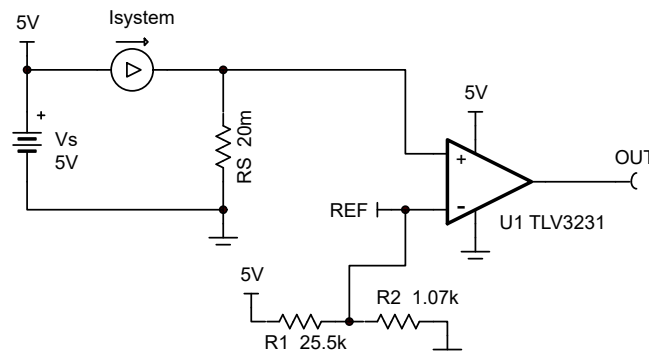


図 7-7. Current Sensing

7.2.1.1 Design Requirements

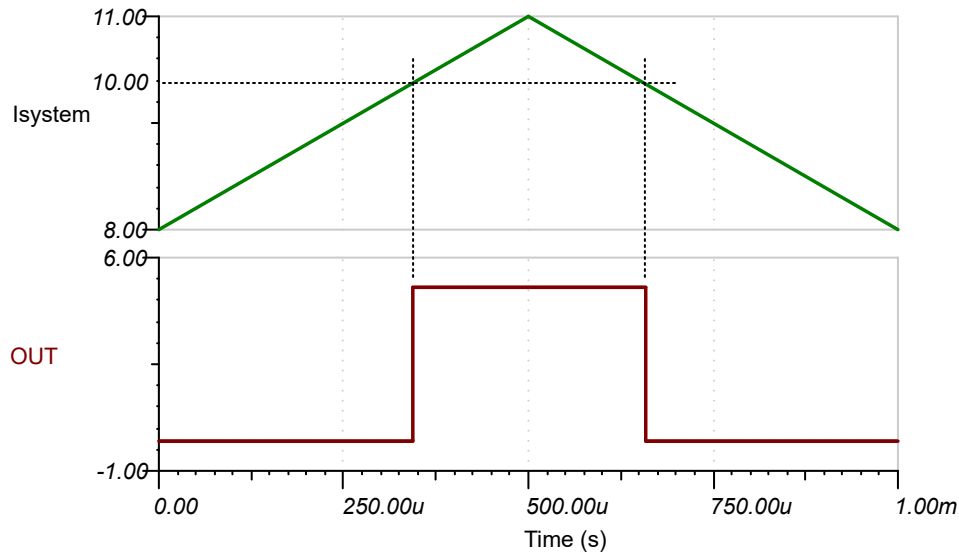
For this design, follow these design requirements:

- Alert (overcurrent) event occurs when system current (I_{system}) reaches 10A
- Alert signal (OUT) is active high
- Operate from a 5V power supply

7.2.1.2 Detailed Design Procedure

To minimize power dissipation and voltage drop across the shunt resistor (R_S), a value of $20m\Omega$ is selected. Since the overcurrent level of 10A creates a $200mV$ drop across R_S , R_1 and R_2 are calculated to create the voltage divider value of $200mV$ from the regulated 5V supply voltage. If the system is expected to operate close to the 10A maximum, hysteresis can be added to the design as shown in [Non-Inverting Comparator With Hysteresis](#).

7.2.1.3 Application Curve



☒ 7-8. Overcurrent Results

7.3 Power Supply Recommendations

Due to the fast output edges, bypass capacitors are required on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR $0.1\mu F$ ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents can be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ((V+) & (V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output now swings "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

Accurate comparator applications require a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a (V+) or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<math><100\Omega</math>) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations can be used when routing long distances.

7.4.2 Layout Example

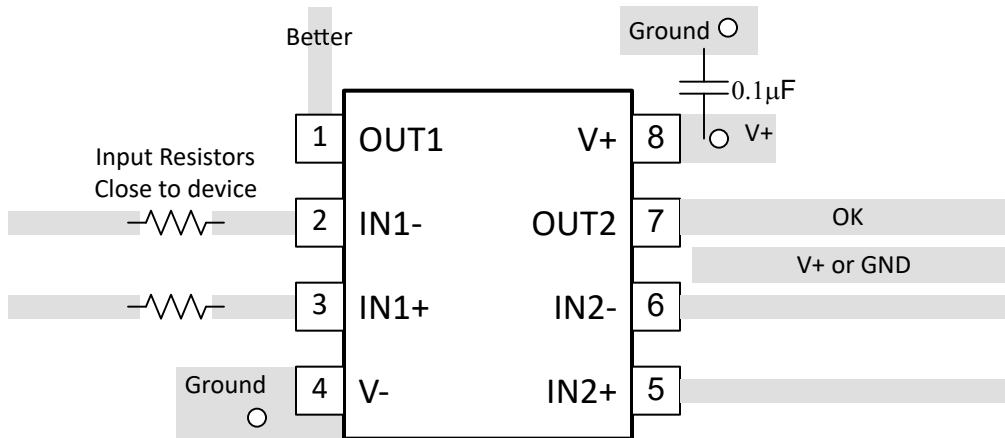


图 7-9. Dual Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

[Analog Engineers Circuit Cookbook: Amplifiers \(See Comparators section\) - SLYY137](#)

[Precision Design, Comparator with Hysteresis Reference Design— TIDU020](#)

[Comparator with and without hysteresis circuit - SBOA219](#)

[Inverting comparator with hysteresis circuit - SNOA997](#)

[Non-Inverting Comparator With Hysteresis Circuit - SBOA313](#)

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.4 Trademarks

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8.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2024) to Revision B (December 2024) Page

• ドキュメント全体でデュアル TLV3232 をリリース.....	1
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Changes from Revision * (August 2024) to Revision A (September 2024) Page

• SOT-23 パッケージの量産データのリリース.....	1
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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3231DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3HGH	Samples
TLV3231DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1SQ	Samples
TLV3232DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3MSS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3231 :

- Automotive : [TLV3231-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3231DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3231DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV3232DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3231DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV3231DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV3232DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0

EXAMPLE BOARD LAYOUT

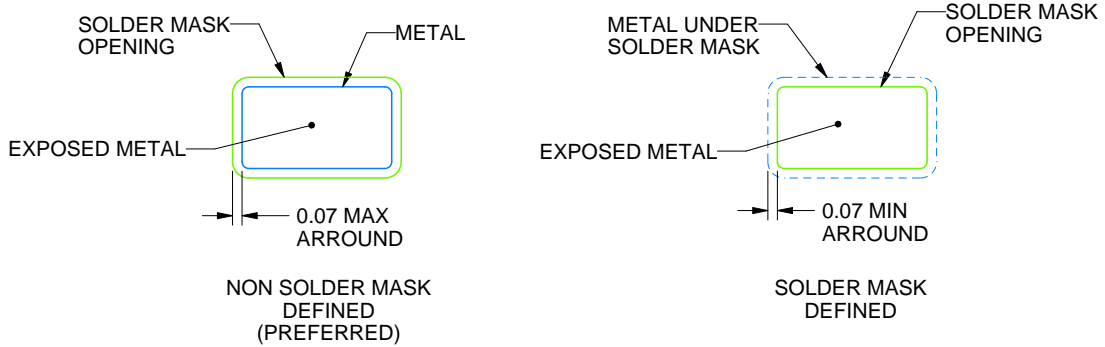
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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