TLV320x-Q1 40ns、Micropower、プッシュプル出力車載用コンパレータ

1 特長

- 車載アプリケーションに対応
- 以下の結果でAEC Q100認定済み
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～+125°C
  - デバイスHBM ESD分類レベル2 (TLV3201-Q1)
  - デバイスHBM ESD分類レベル3A (TLV3202-Q1)
  - デバイスCDM ESD分類レベルC5
- 短い伝搬遅延: 40ns
- 低い静止電流: チャネルごとに40µA
- 各レールから200mV拡張された入力同相範囲
- 低い入力オフセット電圧: 1mV
- プッシュプル出力
- 電源電圧範囲: 2.7V～5.5V
- 小型のパッケージ: 5ピンSC70および8ピンVSSOP

2 アプリケーション

- エンジン制御ユニット(ECU)
- 車体制御モジュール(BCM)
- バッテリ管理システム(BMS)
- HEV/EVのインバータおよびモーター制御
- 超音波距離測定およびLIDAR
- ステアリングおよびトラクション・コントローラ
- 在室者検出
- インフォテインメント・システム

3 概要

TLV3201-Q1およびTLV3202-Q1はシングルおよびデュアル・チャネルのコンパレータで、高速(40ns)と低消費電力(40µA)の両方を非常に小さいパッケージで実現し、レール・ツー・レール入力、低オフセット電圧(1mV)、大きな出力駆動電流などの特長があります。応答時間が重要であるさまざまなアプリケーションに容易に実装できます。

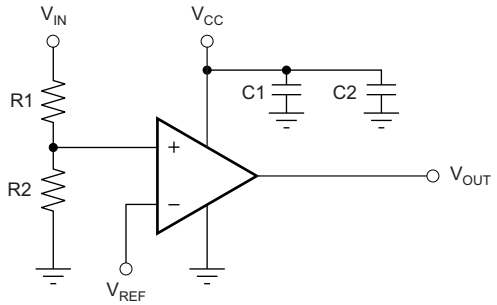
TLV320x-Q1ファミリはシングル(TLV3201-Q1)およびデュアル(TLV3202-Q1)チャネルのバージョンで利用でき、いずれもプッシュプル出力が付属します。TLV3201-Q1は5ピンのSC70パッケージで供給されます。TLV3202-Q1は8ピンのVSSOPパッケージで供給されます。すべてのデバイスは、-40°C～+125°Cの拡張工業用温度範囲で仕様が規定されています。

製品情報(1)

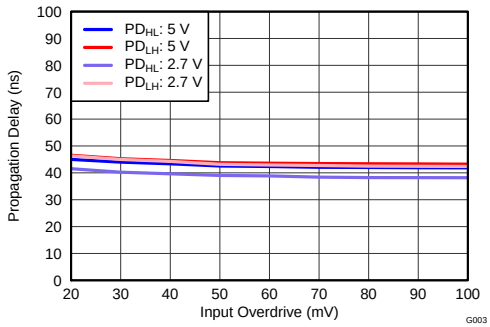
型番	パッケージ	本体サイズ(公称)
TLV3201-Q1	SC70 (5)	2.00mm×1.25mm
TLV3202-Q1	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

スレッショルド検出器



伝搬遅延とオーバードライブ



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年2月発行のものから更新 **Page**

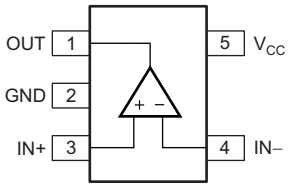
- Changed figure 29 ... 15

5 Device Comparison Table

DEVICE	DESCRIPTION
TLV3011	5-µA (maximum) open-drain, 1.8-V to 5.5-V with integrated voltage reference in 1.5-mm × 1.5-mm micro-sized packages
TLV3012	5-µA (maximum) push-pull, 1.8-V to 5.5-V with integrated voltage reference in micro-sized packages
TLV3501	4.5-ns, rail-to-rail, push-pull comparator in micro-sized packages
LMV7235	75-ns, 65-µA, 2.7-V to 5.5-V, rail-to-rail input comparator with open-drain output
LMV7239	75-ns, 65-µA, 2.7-V to 5.5-V, rail-to-rail input comparator with push-pull output
LMV7239-Q1	Automotive 75-ns, 65-µA, 2.7-V to 5.5-V, rail-to-rail input comparator with push-pull output
REF3333	30-ppm/°C drift, 3.9-µA, SOT23-3, SC70-3 voltage reference

6 Pin Configuration and Functions

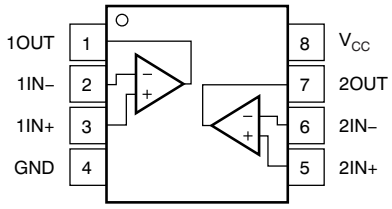
TLV3201-Q1 DCK Package
5-Pin SC70-5
Top View



Pin Functions: TLV3201-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Negative supply, ground
IN–	4	I	Negative input
IN+	3	I	Positive input
OUT	1	O	Output
V_{CC}	5	—	Positive supply

TLV3202-Q1 DGK Package
8-Pin VSSOP
Top View



Pin Functions: TLV3202-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Negative input, comparator 1
1IN+	3	I	Positive input, comparator 1
1OUT	1	O	Output, comparator 1
2IN–	6	I	Negative input, comparator 2
2IN+	5	I	Positive input, comparator 2
2OUT	7	O	Output, comparator 2
GND	4	—	Negative supply, ground
V_{CC}	8	—	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		7	V
	Signal input pins(2)	–0.5	(V_{CC}) + 0.5	
Current	Signal input pins(2)	–10	10	mA
	Output short circuit(3)		100	
Temperature	Operating	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground.

7.2 ESD Ratings

			VALUE	UNIT
TLV3201-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±3000	V
		Charged-device model (CDM), per AEC Q100-011	±750	
TLV3202-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, $V_S = (V_{S+}) – (V_{S–})$	2.7 (±1.35)	5.5 (±2.75)	V
T_A	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV3201-Q1 DCK (SC-70) 5 PINS	TLV3202-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	281.9	201.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.6	92.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.3	123.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	23	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.3	212.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: V_{CC} = 5 V

at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		T_A = –40°C to 125°C			6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			5	nA
I_{IO}	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio	–0.2 V < V_{CM} < 5.2 V	60	70		dB
INPUT IMPEDANCE						
	Common mode			10^{13} || 2		Ω || pF
	Differential			10^{13} || 4		Ω || pF
OUTPUT						
V_{OL}	Voltage output swing from lower rail	I_{SINK} = 4 mA		175	190	mV
		T_A = –40°C to 125°C			225	
V_{OH}	Voltage output swing from upper rail	I_{SOURCE} = 4 mA		120	140	mV
		T_A = –40°C to 125°C			170	
I_{SC}	Short-circuit current (per comparator)	I_{SC} sinking	40	48		mA
		T_A = –40°C to 125°C		See Figure 14		
		I_{SC} sourcing	52	60		
		T_A = –40°C to 125°C		See Figure 14		
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A = 25°C		40	50	µA
		T_A = –40°C to 125°C			65	

7.6 Electrical Characteristics: V_{CC} = 2.7 V

at T_A = 25°C and V_{CC} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		T_A = –40°C to 125°C			6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			5	nA
I_{IO}	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio	–0.2 V < V_{CM} < 2.9 V	56	68		dB

Electrical Characteristics: V_{CC} = 2.7 V (continued)

at T_A = 25°C and V_{CC} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT IMPEDANCE						
	Common mode			10^{13} || 2		Ω || pF
	Differential			10^{13} || 4		Ω || pF
OUTPUT						
V_{OL}	Voltage output swing from lower rail	I_{SINK} = 4 mA		230	260	mV
		T_A = –40°C to 125°C			325	
V_{OH}	Voltage output swing from upper rail	I_{SOURCE} = 4 mA		210	250	mV
		T_A = –40°C to 125°C			350	
I_{SC}	Short-circuit current (per comparator)	I_{SC} sinking	13	19		mA
		T_A = –40°C to 125°C	See Figure 14			
		I_{SC} sourcing	15	21		
		T_A = –40°C to 125°C	See Figure 14			
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A = 25°C		36	46	µA
		T_A = –40°C to 125°C			60	

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay time	Low to high	Input overdrive = 20 mV, C_L = 15 pF		47	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		42	50	
			T_A = –40°C to 125°C			55	
		High to low	Input overdrive = 20 mV, C_L = 15 pF		40	50	
			Input overdrive = 100 mV, C_L = 15 pF		38	50	
			T_A = –40°C to 125°C			55	
	Propagation delay skew	Input overdrive = 20 mV, C_L = 15 pF			2		ns
	Propagation delay matching (TLV3202-Q1)	High to low or low to high, input overdrive = 20 mV, C_L = 15 pF				5	ns
t_R	Rise time	10% to 90%			2.9		ns
t_F	Fall time	10% to 90%			3.7		ns

7.8 Typical Characteristics

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

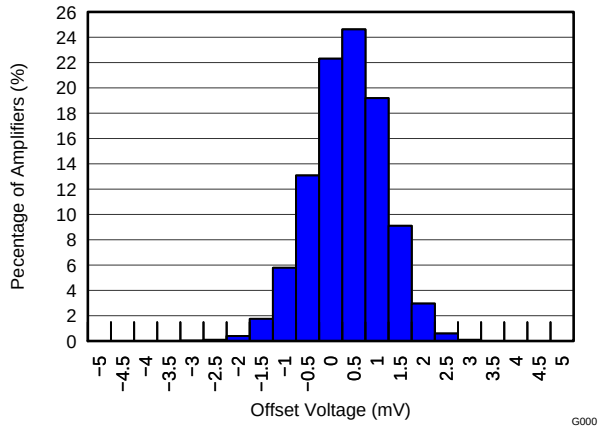


Figure 1. Offset Voltage Distribution

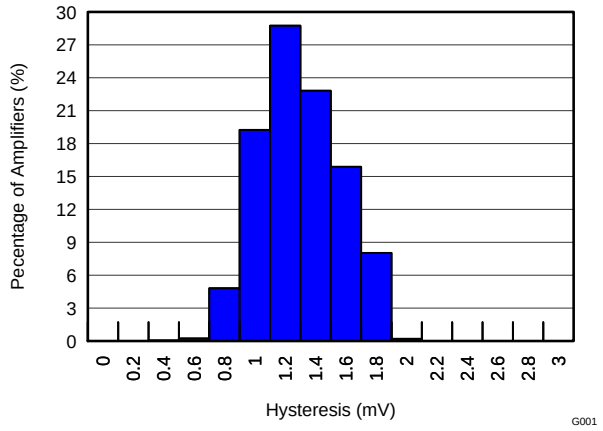


Figure 2. Hysteresis Distribution

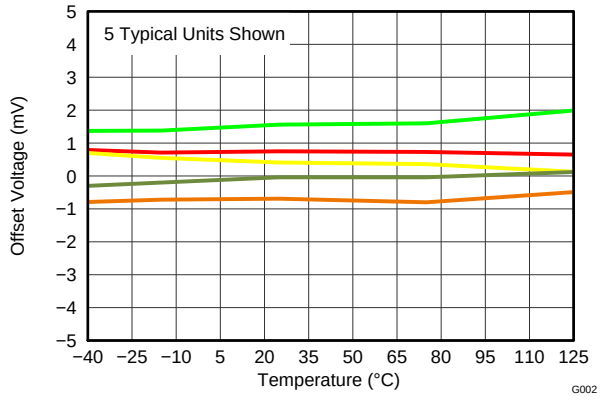


Figure 3. Offset Voltage vs Temperature

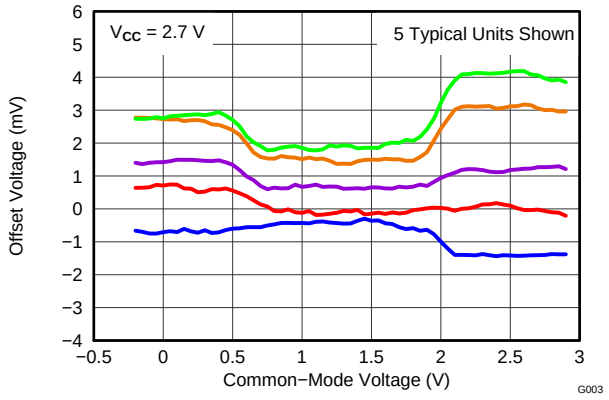


Figure 4. Offset Voltage vs Common-Mode Voltage

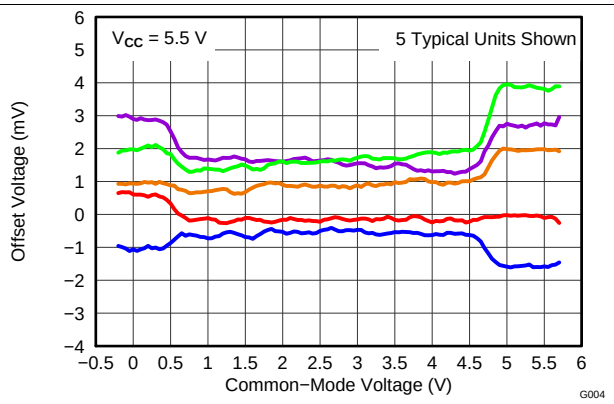


Figure 5. Offset Voltage vs Common-Mode Voltage

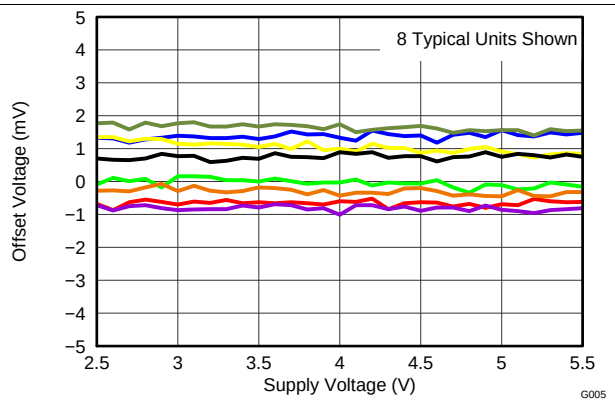


Figure 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

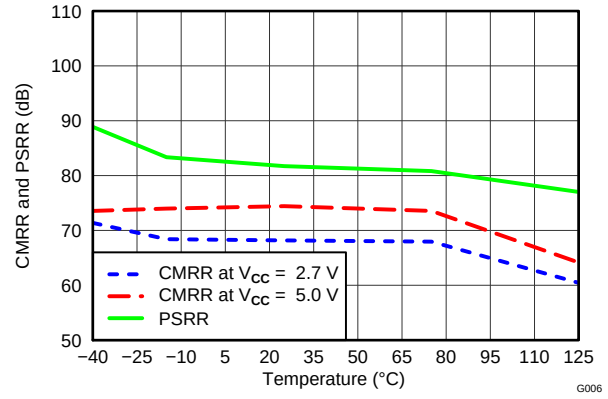


Figure 7. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

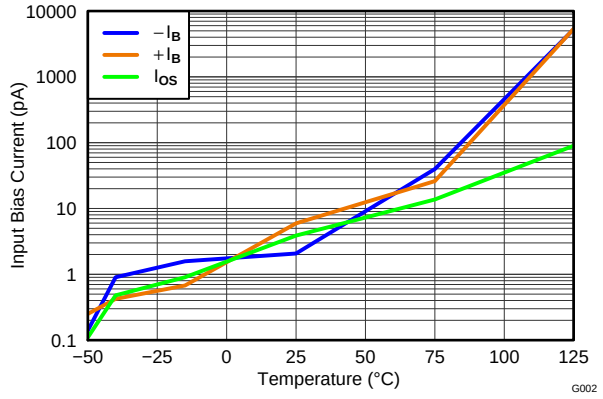


Figure 8. Input Bias Current and Input Offset Current vs Temperature

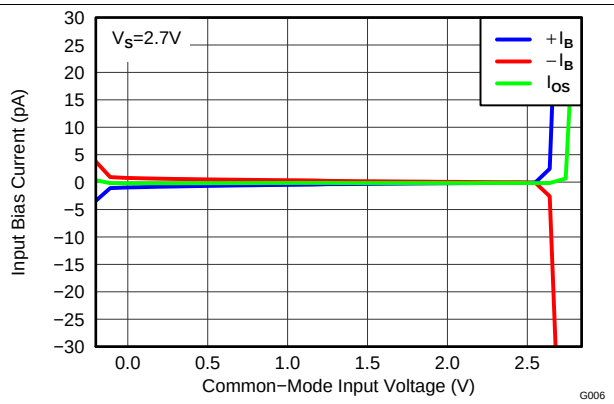


Figure 9. Input Bias Current and Input Offset Current vs Common-Mode Input Voltage

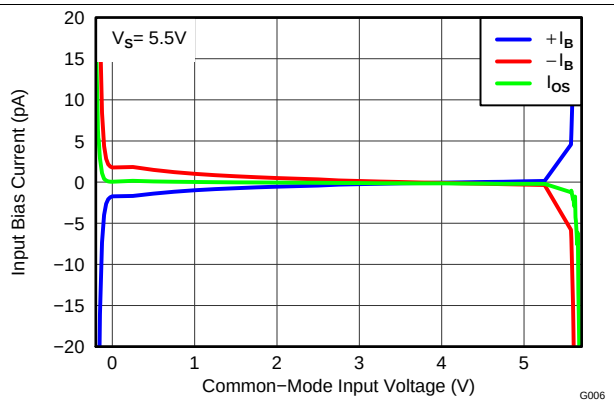


Figure 10. Input Bias Current and Input Offset Current vs Common-Mode Input Voltage

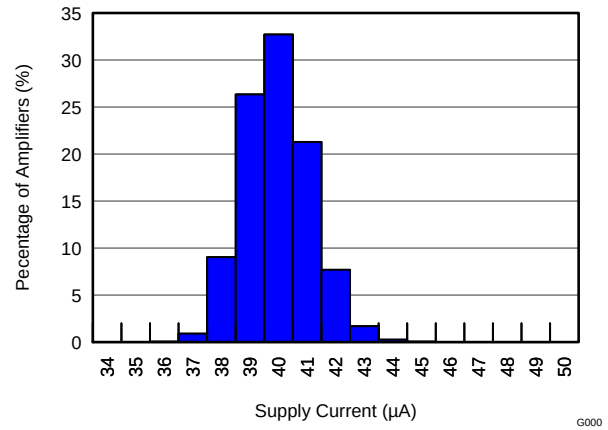


Figure 11. Quiescent Current Distribution

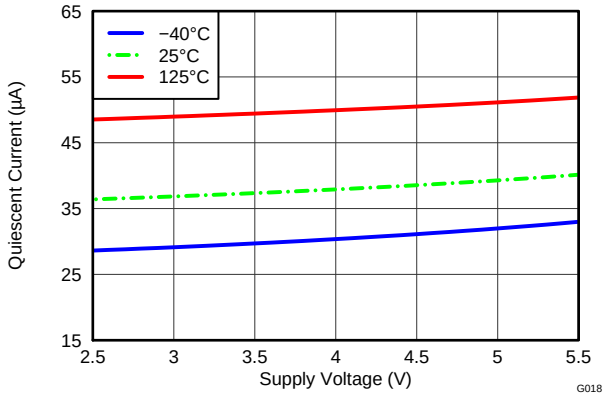


Figure 12. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

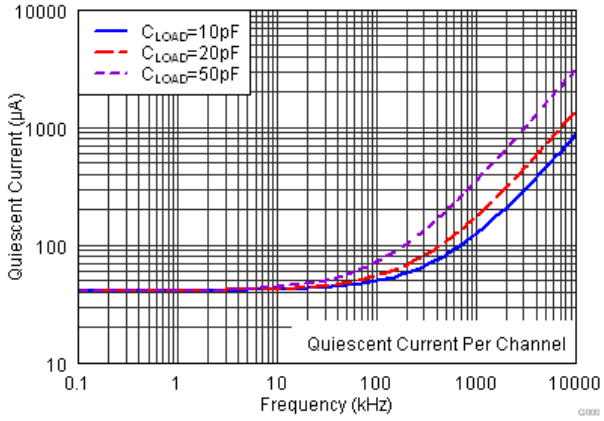


Figure 13. Quiescent Current vs Switching Frequency

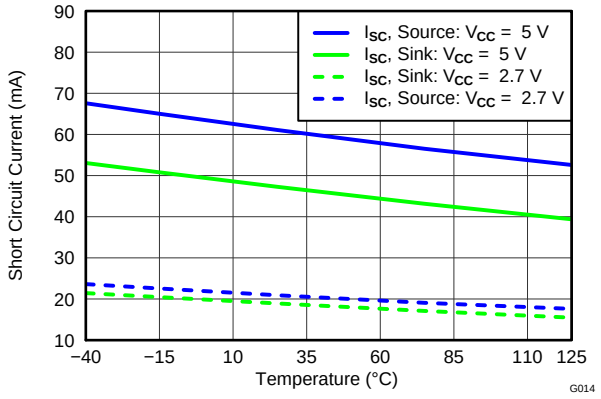


Figure 14. Short-Circuit Current vs Temperature

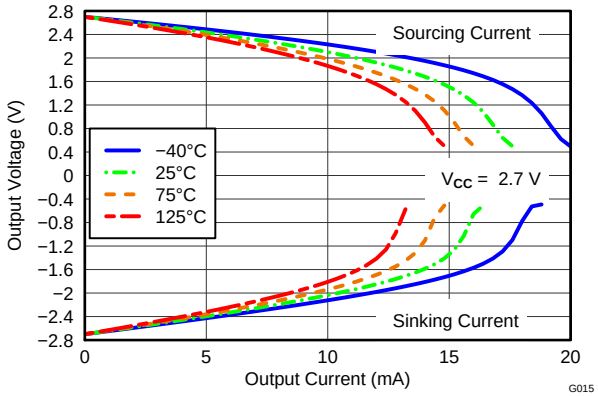


Figure 15. Output Voltage vs Output Current

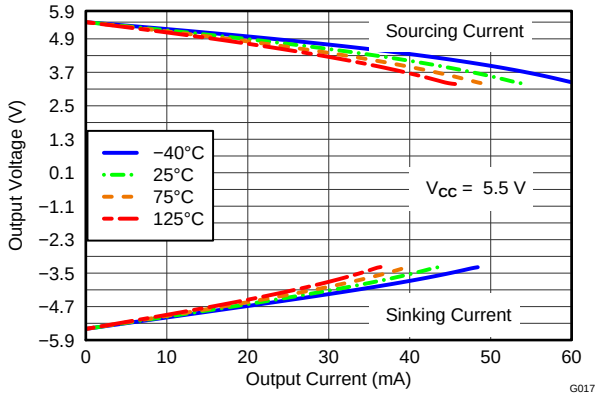


Figure 16. Output Voltage vs Output Current

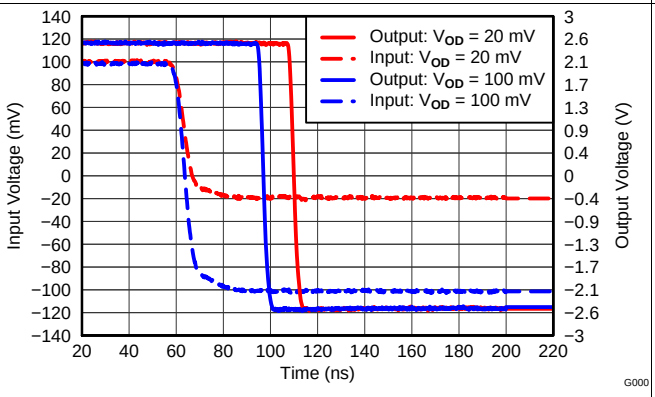


Figure 17. Propagation Delay Falling Edge

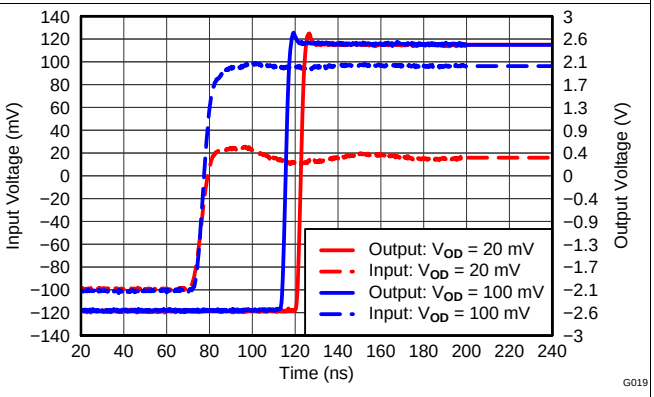


Figure 18. Propagation Delay Rising Edge

Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

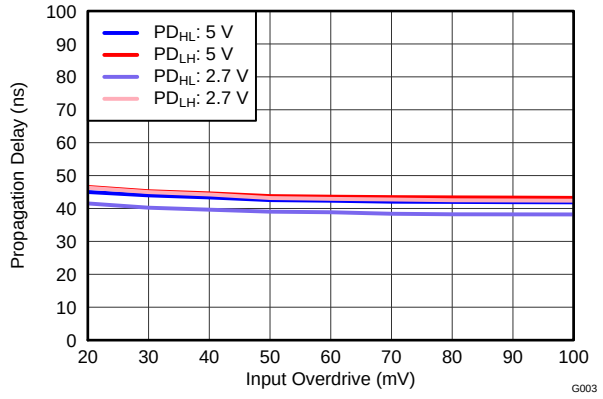


Figure 19. Propagation Delay vs Input Overdrive

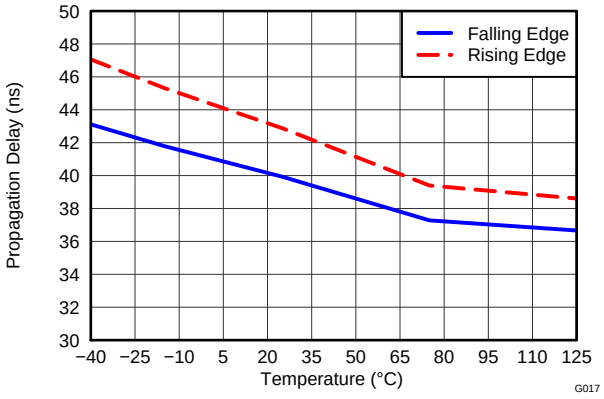


Figure 20. Propagation Delay vs Temperature

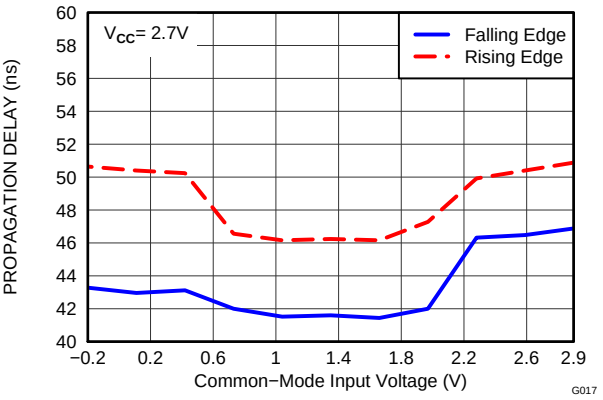


Figure 21. Propagation Delay vs Common-Mode Voltage

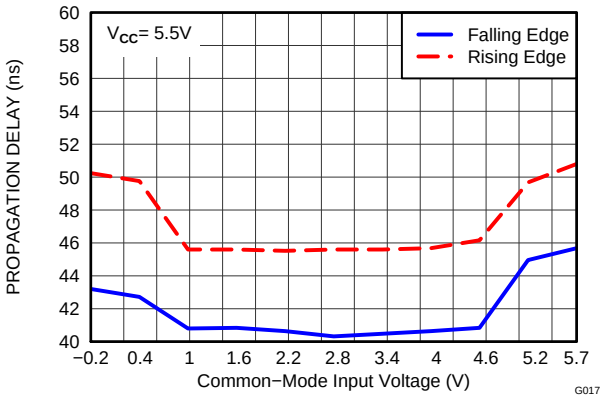


Figure 22. Propagation Delay vs Common-Mode Voltage

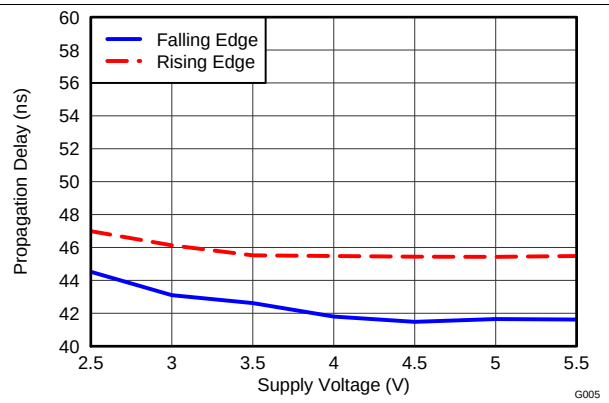


Figure 23. Propagation Delay vs Supply Voltage

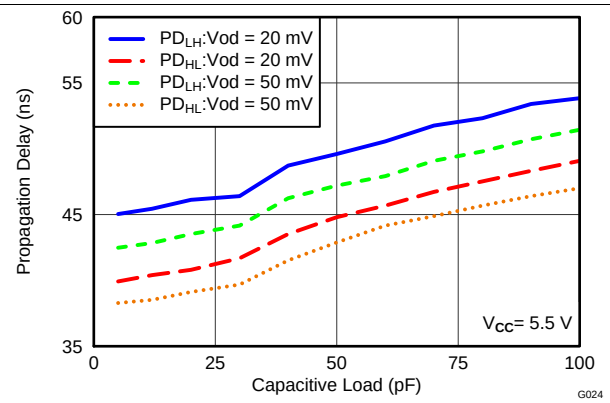


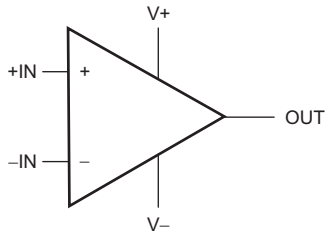
Figure 24. Propagation Delay vs Capacitive Load

8 Detailed Description

8.1 Overview

The TLV3201-Q1 and TLV3202-Q1 devices feature 40-ns response time and include 1.2 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2 V beyond the power-supply rails.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV3201-Q1 and TLV3202-Q1 comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to +125°C. The device continues to function below this range, but performance is not specified.

8.3.2 Input Overvoltage Protection

The device inputs are protected by electrostatic discharge (ESD) diodes that conduct if the input voltages exceed the power supplies by more than approximately 300 mV. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the input to the comparator.

8.4 Device Functional Modes

The device is fully functional when powered by rail-to-rail supply voltage greater than 2.7 V.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV3201-Q1 and TLV3202-Q1 are single- and dual-supply (respectively), push-pull comparators featuring 40 ns of propagation delay on only 40 µA of supply current. This combination of fast response time and minimal power consumption make the TLV3201-Q1 and TLV3202-Q1 excellent comparators for portable, battery-powered applications as well as fast-switching threshold detection such as pulse-width modulation (PWM) output monitors and zero-cross detection.

9.1.1 Comparator Inputs

The TLV3201-Q1 and TLV3202-Q1 are rail-to-rail input comparators, with an input common-mode range that exceeds the supply rails by 200 mV for both positive and negative supplies. The devices are specified from 2.7 V to 5.5 V, with room temperature operation from 2.5 V to 5.5 V. The TLV3201-Q1 and TLV3202-Q1 are designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 25 shows the TLV320x-Q1 response when input voltages exceed the supply, resulting in no phase inversion.

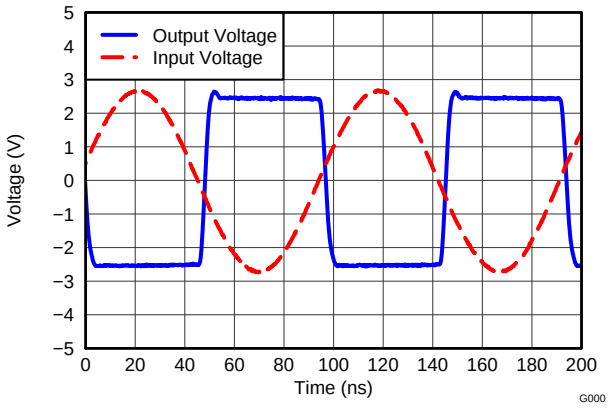


Figure 25. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

The ESD protection input structure of two back-to-back diodes and 1-kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed V_{CC} beyond the specified operating conditions. If potential overvoltage conditions that exceed absolute maximum ratings are present, the addition of external bypass diodes and resistors is recommended, as shown in Figure 26. Large differential voltages greater than the supply voltage must be avoided to prevent damage to the input stage.

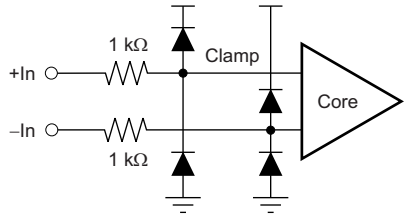


Figure 26. TLV3201-Q1 Equivalent Input structure

Application Information (continued)

9.1.2 External Hysteresis

The TLV3201-Q1 and TLV3202-Q1 have a hysteresis transfer curve (shown in Figure 27) that is a function of three components: V_{TH}, V_{OS}, and V_{HYST}.

- V_{TH}: the actual set voltage or threshold trip voltage
- V_{OS}: the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST}: internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

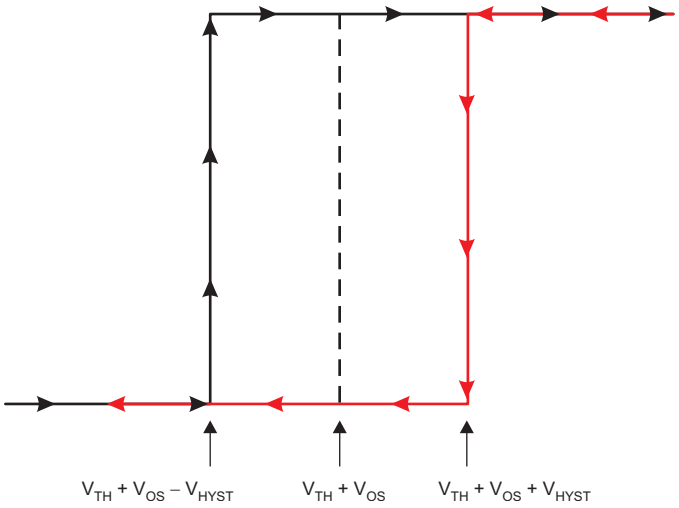


Figure 27. TLV320x-Q1 Hysteresis Transfer Curve

9.1.2.1 Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 28. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. The lower input trip voltage (V_{A1}) is defined by Equation 1.

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than [V_A × (V_{IN} > V_A)], the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. The upper trip voltage (V_{A2}) is defined by Equation 2.

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

The total hysteresis provided by the network is defined by Equation 3.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

Application Information (continued)

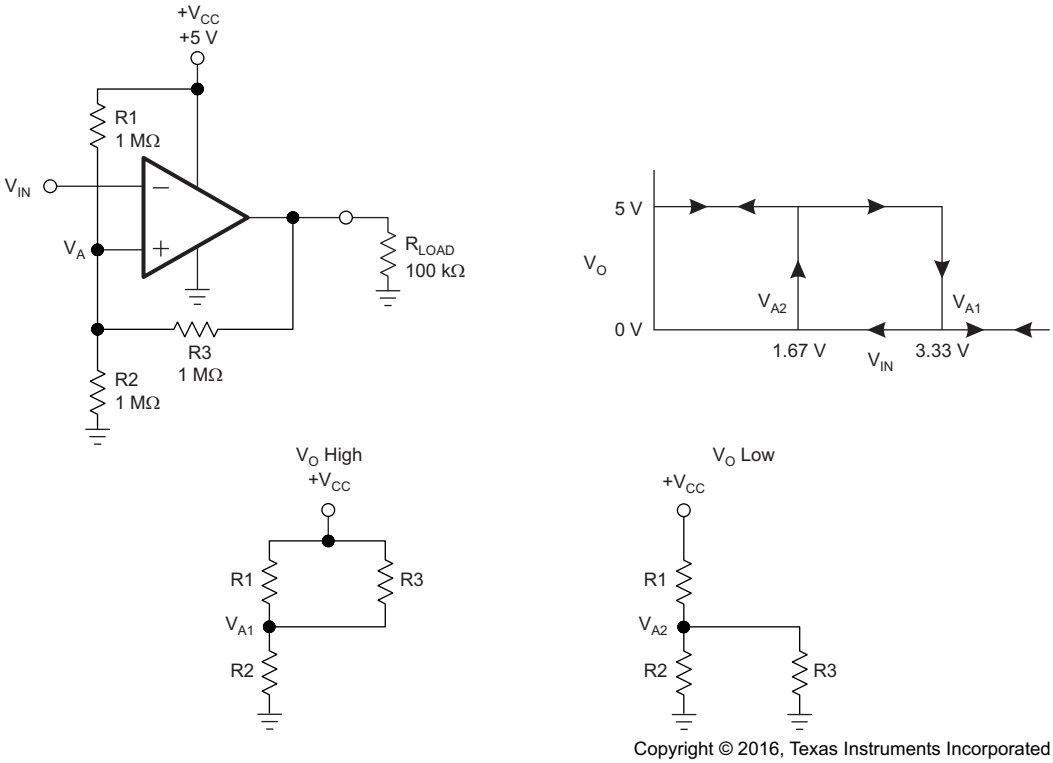


Figure 28. TLV3201-Q1 in Inverting Configuration With Hysteresis

9.1.2.2 Noninverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 29 and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}. V_{IN1} is calculated by Equation 4.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} \times V_{REF} \tag{4}$$

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} must equal V_{REF} before V_A is again equal to V_{REF}. V_{IN} can be calculated by Equation 5.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as defined by Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

Application Information (continued)

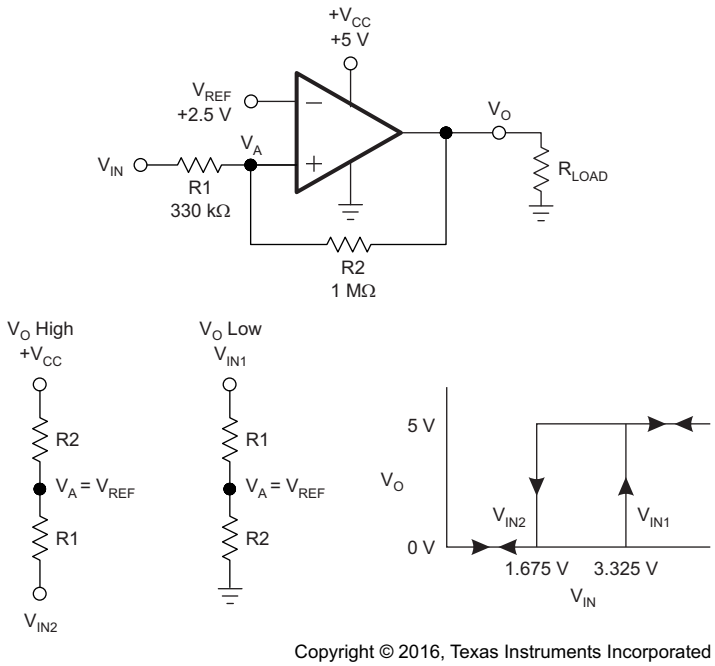


Figure 29. TLV3201-Q1 in Noninverting Configuration With Hysteresis

9.1.3 Capacitive Loads

The TLV3201-Q1 and TLV3202-Q1 feature a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing increased output sinking or sourcing current during the transition. Following the transition the output current decreases and supply current returns to 40 µA, thus maintaining low power consumption. Under reasonable capacitive loads, the TLV3201-Q1 and TLV3202-Q1 maintain specified propagation delay (see *Typical Characteristics*), but excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

9.2 Typical Applications

9.2.1 TLV3201-Q1 Configured as an AC-Coupled Comparator

One of the benefits of ac coupling a single-supply comparator circuit is that it can block dc offsets induced by ground-loop offsets that could potentially produce either a false trip or a common-mode input violation. Figure 30 shows the TLV3201-Q1 configured as an ac-coupled comparator.

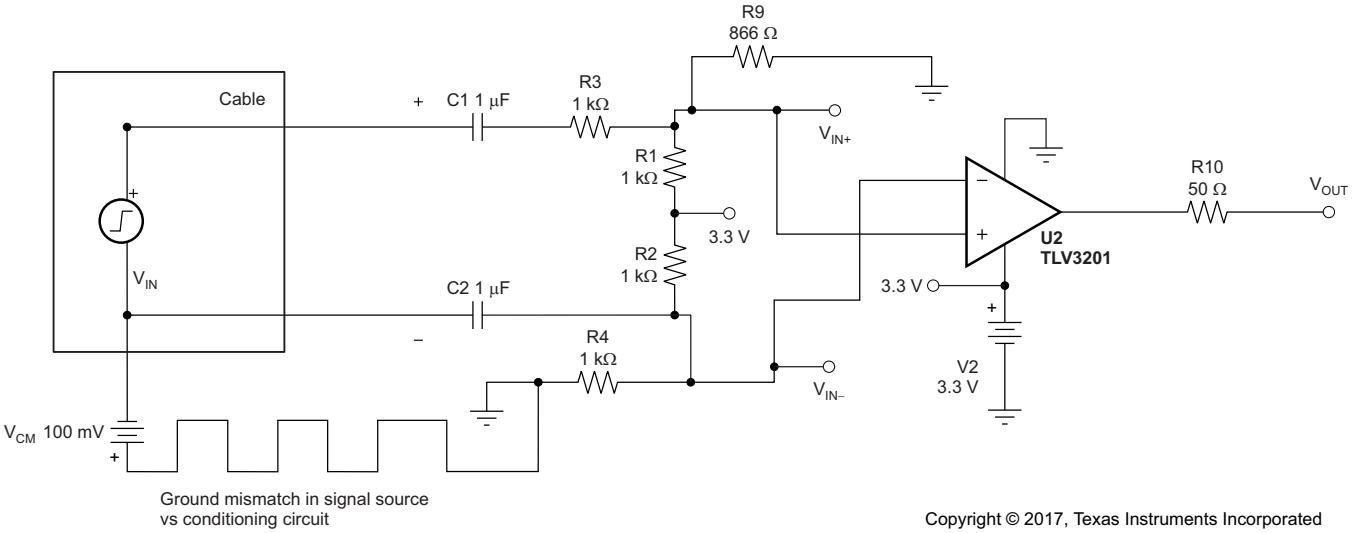


Figure 30. TLV3201-Q1 Configured as an AC-Coupled Comparator (Schematic)

9.2.1.1 Design Requirements

Design requirements include:

- Ability to tolerate up to ±100 mV of common-mode signal.
- Trigger only on ac signals (such as zero-cross detection).

9.2.1.2 Detailed Design Procedure

Design analysis:

- AC-coupled, high-pass frequency
- Large capacitors require longer start-up time from device power on
- Use 1-µF capacitor to achieve high-pass frequency of approximately 159 Hz
- For high-pass equivalent, use C_{IN} = 0.5 µF, R_{IN} = 2 kΩ
  1. Set up input dividers initially for one-half supply (to be in center of acceptable common-mode range).
  2. Adjust either divider slightly upwards or downwards as desired to establish quiescent output condition.
  3. Select coupling capacitors based on lowest expected frequency.

Typical Applications (continued)

9.2.1.3 Application Curve

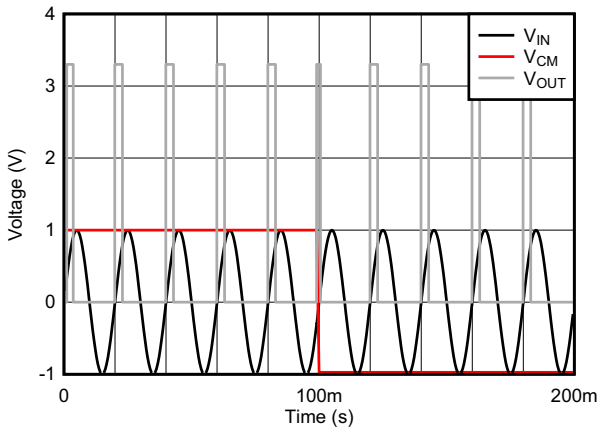


Figure 31. AC-Coupled Comparator Results

9.2.2 TLV3201-Q1 and OPA320 Configured as a Fast-Response Output Current Monitor

Figure 32 shows a single-supply current monitor configured as a difference amplifier with a gain of 50 to trip at 500µA. The OPA320 was chosen for this circuit because of its gain bandwidth (20 MHz), which allows higher speed triggering and monitoring of the current across the shunt resistor followed by the fast response of the TLV3201-Q1.

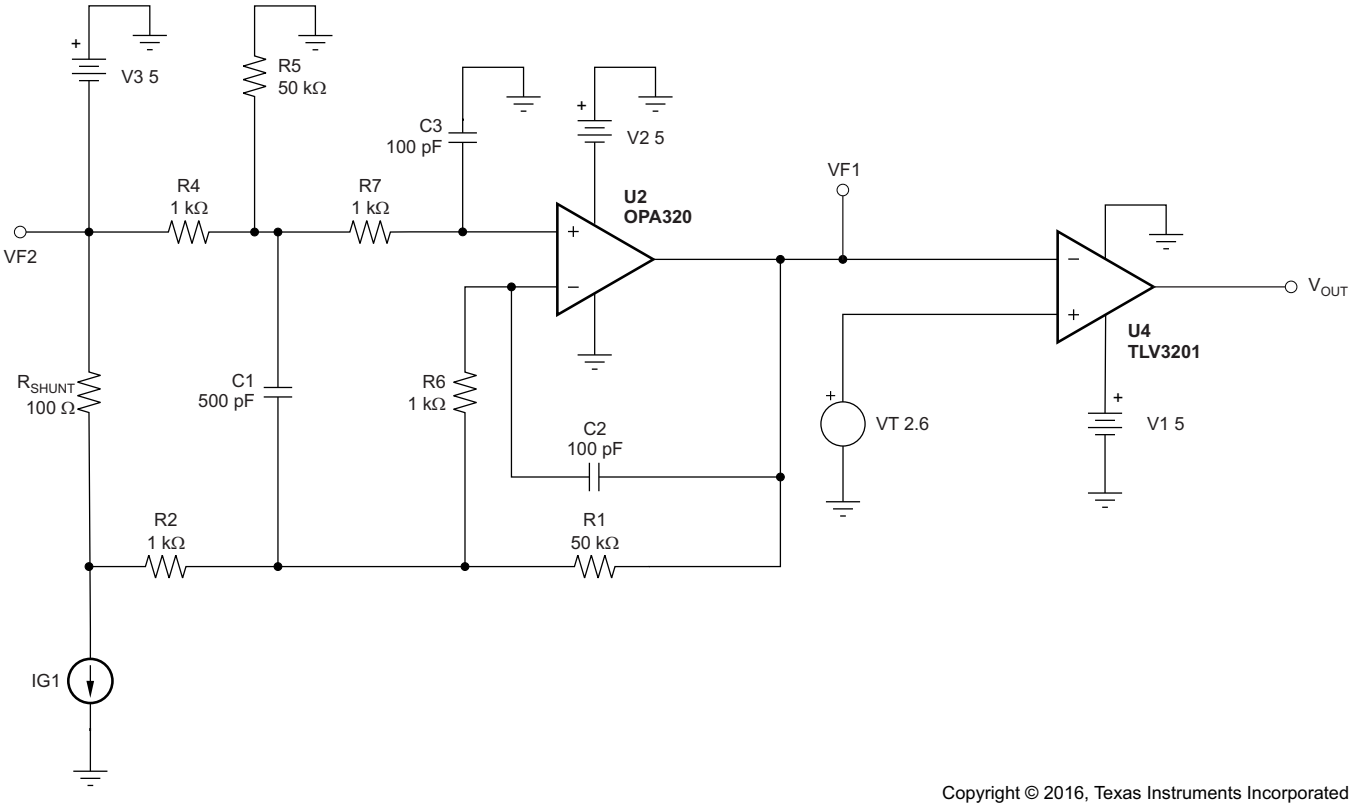


Figure 32. TLV3201-Q1 and OPA320 Configured as a Fast-Response Output Current Monitor

Typical Applications (continued)

9.2.3 TLV3201-Q1 and TMP20 Configured as a Precision Analog Temperature Switch

Figure 33 shows the TMP20 and TLV3201-Q1 designed as a high-speed temperature switch. The TMP20 is an analog output temperature sensor where output voltage decreases with temperature. The comparator output is tripped when the output reaches a critical trip threshold.

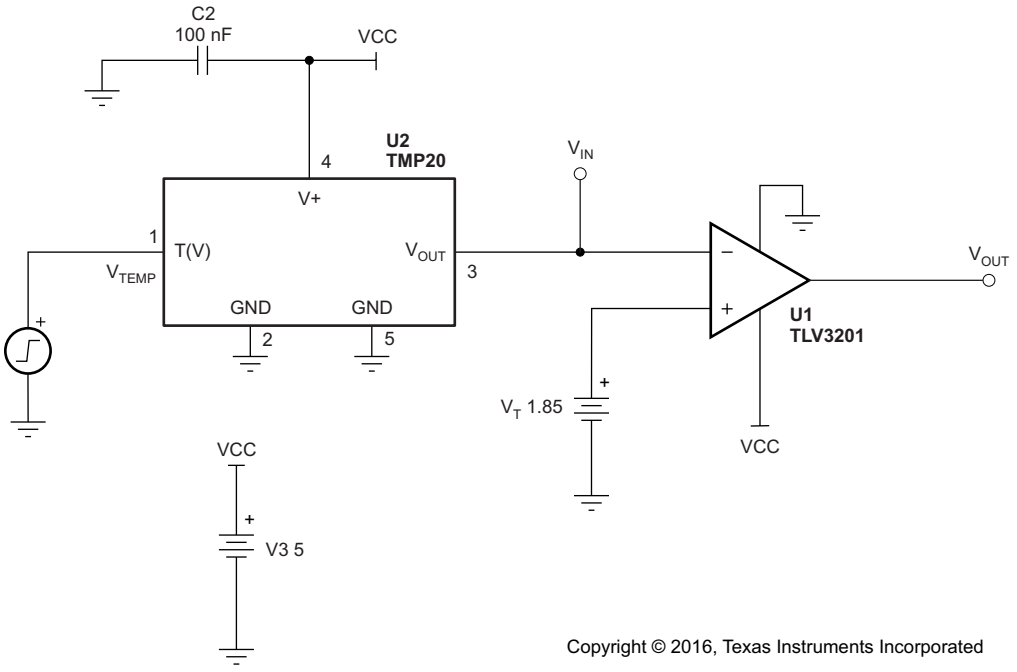


Figure 33. TLV3201-Q1 and TMP20 Configured as a Precision Analog Temperature Switch

10 Power Supply Recommendations

The TLV3201-Q1 and TLV3202-Q1 comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to +125°C. The device continues to function below this range, but performance is not specified. Place bypass capacitors close to the power-supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

The TLV3201-Q1 and TLV3202-Q1 are fast-switching, high-speed comparators and require high-speed layout considerations. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
- Place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
- The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

11.2 Layout Example

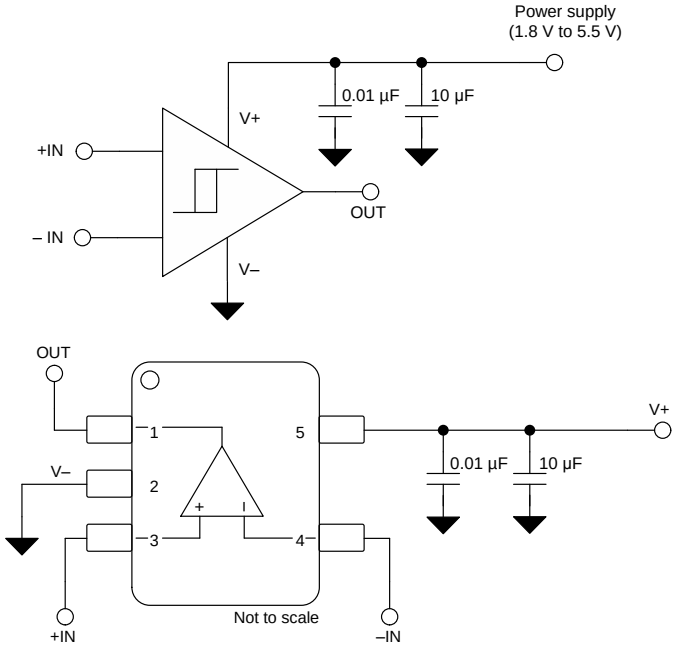


Figure 34. TLV3201-Q1 SOT-23 Board Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 TINA-TI™ シミュレーション・ソフトウェア(無償ダウンロード)

TINA-TI™ソフトウェアはSPICEエンジンを基礎とする、単純かつ強力で使いやすい回路シミュレーション・プログラムです。TINA-TIソフトウェアは、TINAソフトウェアの完全な機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIソフトウェアには従来型のDC、過渡、および周波数ドメインのSPICEによる分析と、追加の設計機能が搭載されています。

TINA-TIソフトウェアはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

> 注
> これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

12.1.1.2 ユニバーサル・オペアンプ評価モジュール

ユニバーサル・オペアンプ評価モジュールは一連の汎用のブランクアウト回路基板で、各種のICパッケージ・タイプ向けの回路のプロトタイプ作成を容易にします。基本的にはオペアンプ用ですが、ピン配列はTLV320x-Q1コンパレータと同じなので、コンパレータ回路のプロトタイプを簡単かつ迅速に作成するため使用できます。5つのモデルが提供されており、それぞれのモデルは特定のパッケージ・タイプを対象としています。PDIP、SOIC、MSOP、TSSOP、およびSOT23のパッケージがすべてサポートされています。

> 注
> これらの基板には部品が搭載されていないため、ユーザーが独自のICを供給する必要があります。ユニバーサル・オペアンプ評価モジュールを注文するときに、オペアンプ・デバイスのサンプルをいくつか要求することをお勧めします。

12.1.1.3 TI Precision Designs

TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。TI Precision Designsは、http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。

12.1.1.4 WEBENCH® Filter Designer

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。コンパレータの前にフィルタを配置することで、ノイズを除去し誤ったトリガ遷移を大幅に改善できます。WEBENCH® Filter Designerは、WEBENCH® Design CenterからWebベースのツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

12.2 ドキュメントのサポート

12.2.1 関連資料

以下に示すドキュメントはTLV320x-Q1の使用に関連しており、参照用にお勧めします。すべてのドキュメントは、特に記述のない限りwww.ti.comからダウンロードできます。

- *『UCC28950とTLV3201での周波数ディザリング』*
- *『UCC28180とTLV3201での周波数ディザリング』*

ドキュメントのサポート (continued)

- *『ヒステリシス付きコンパレータのリファレンス・デザイン』*

12.3 関連リンク

表 1 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV3201-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV3202-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.6 商標

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.
TINA-TI is a trademark of Texas Insturments and DesignSoft, Inc..
All other trademarks are the property of their respective owners.

12.7 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3201AQDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5HF	Samples
TLV3202AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1C8Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV3201-Q1, TLV3202-Q1 :

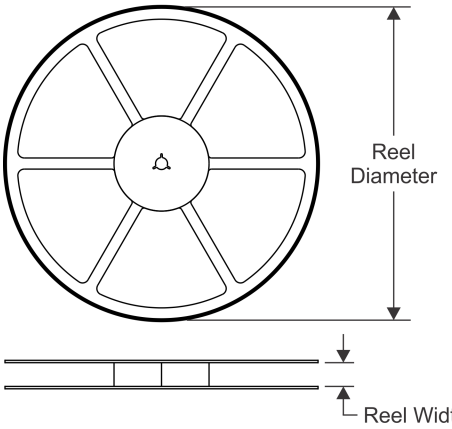
- Catalog : TLV3201, TLV3202

NOTE: Qualified Version Definitions:

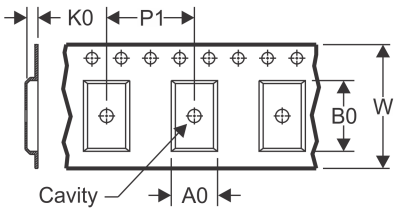
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

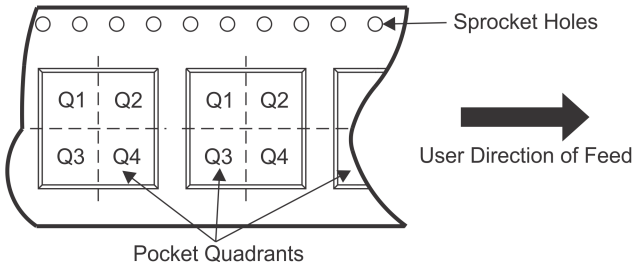


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

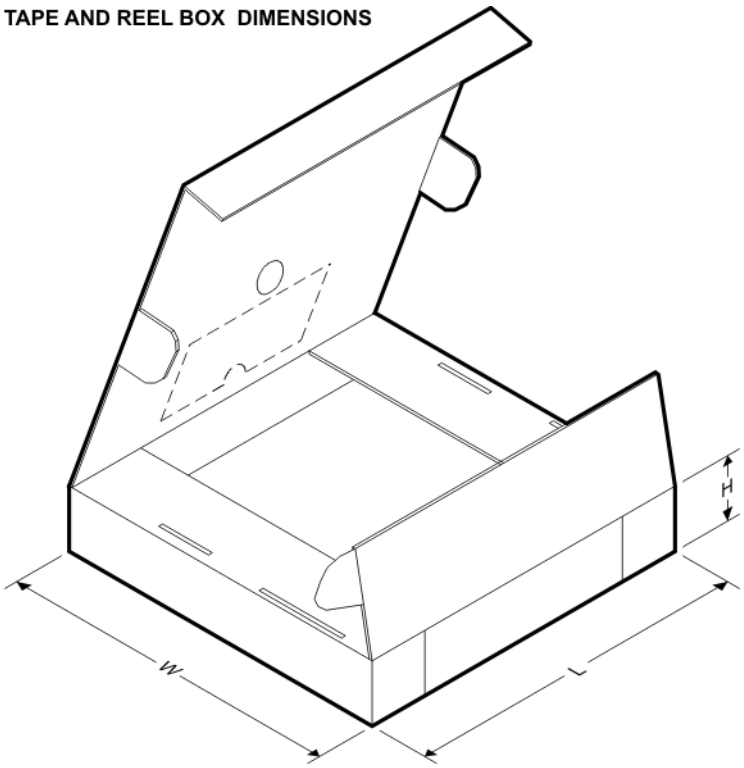
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3201AQDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3202AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

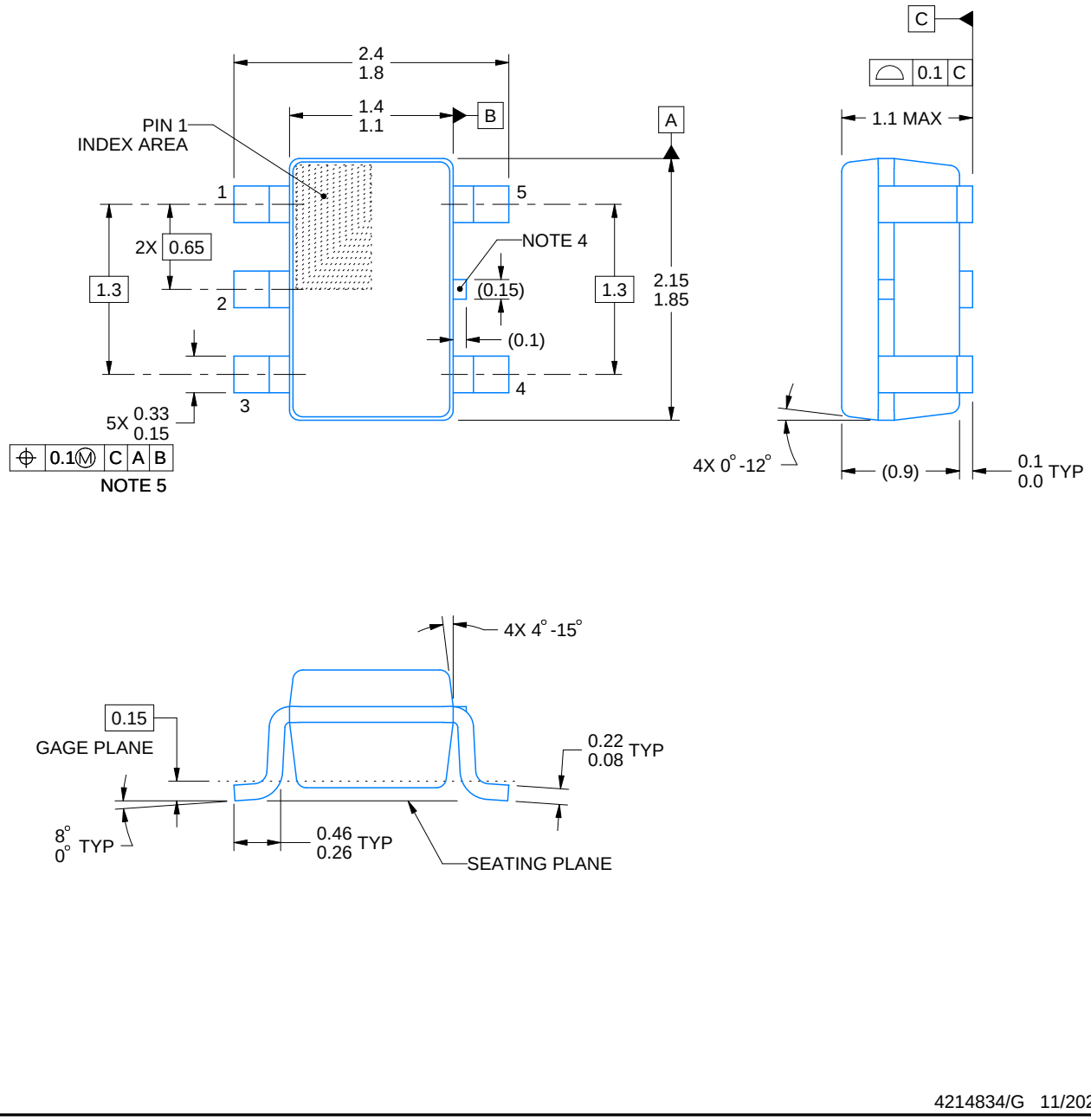
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3201AQDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV3202AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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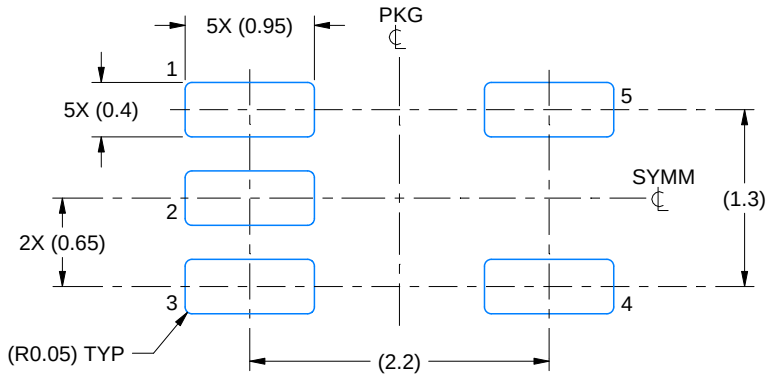
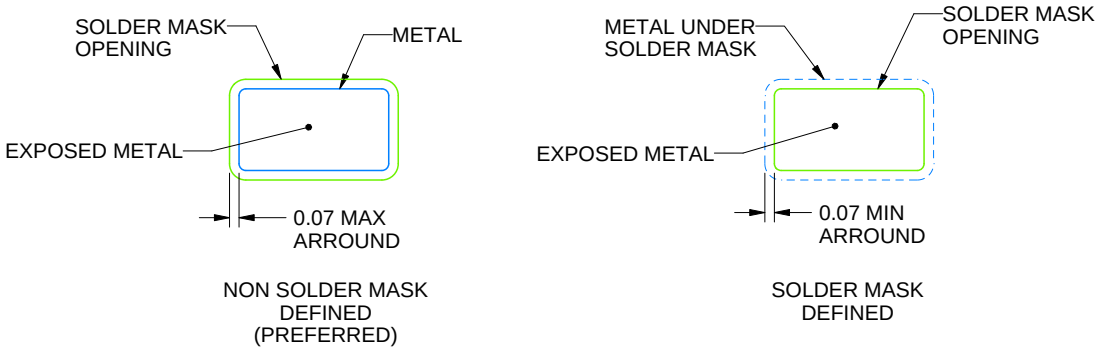
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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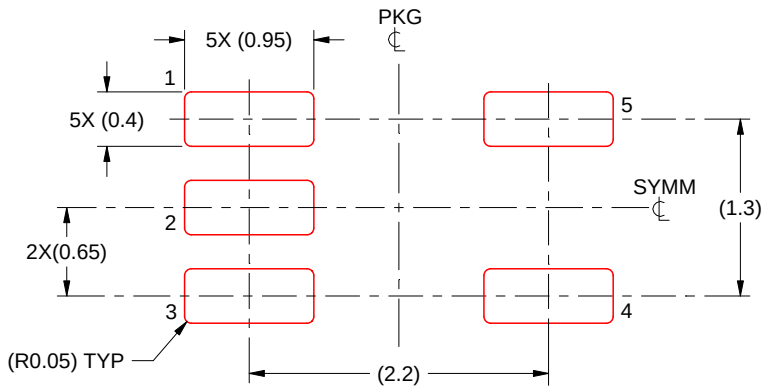
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

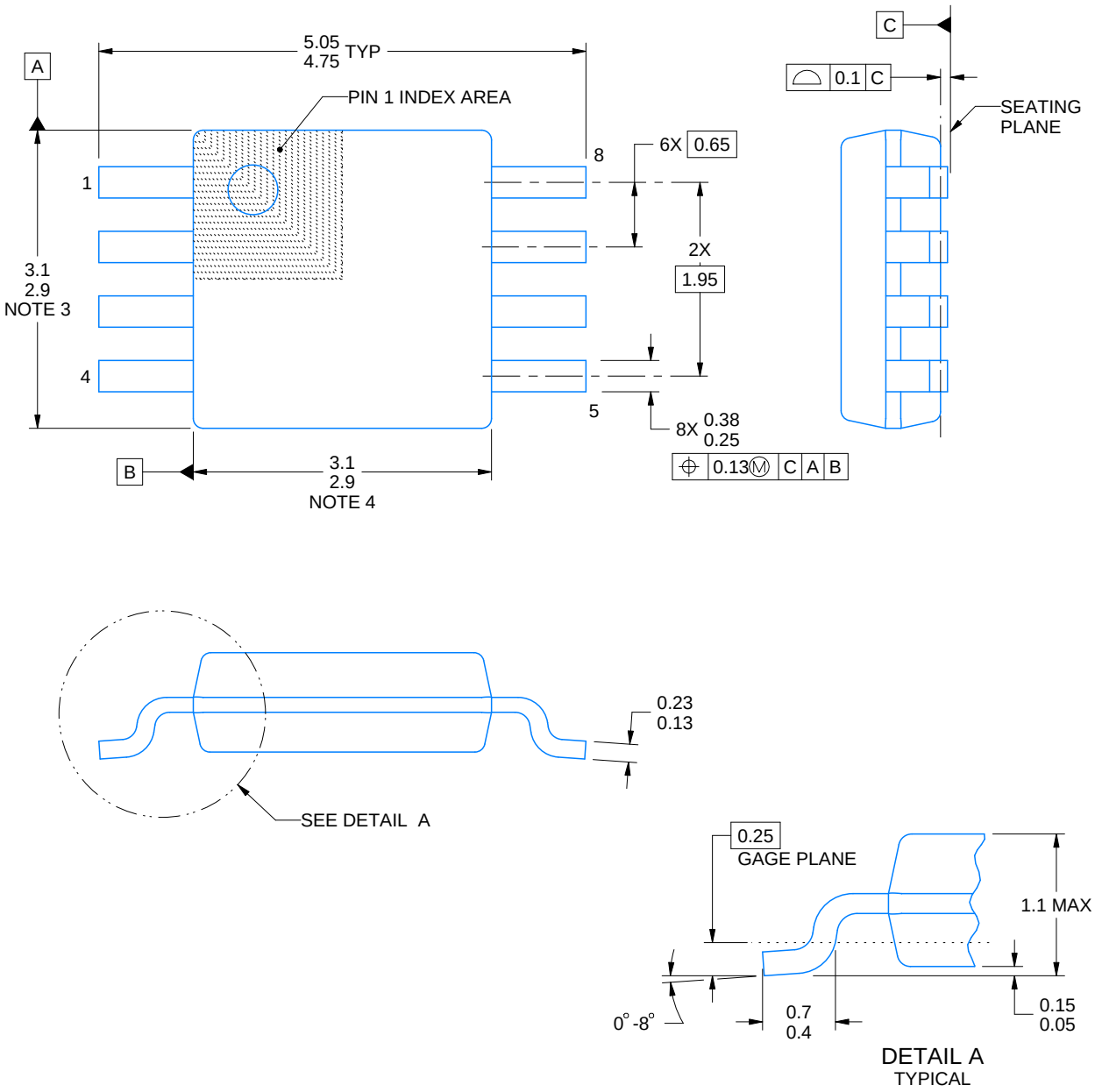
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

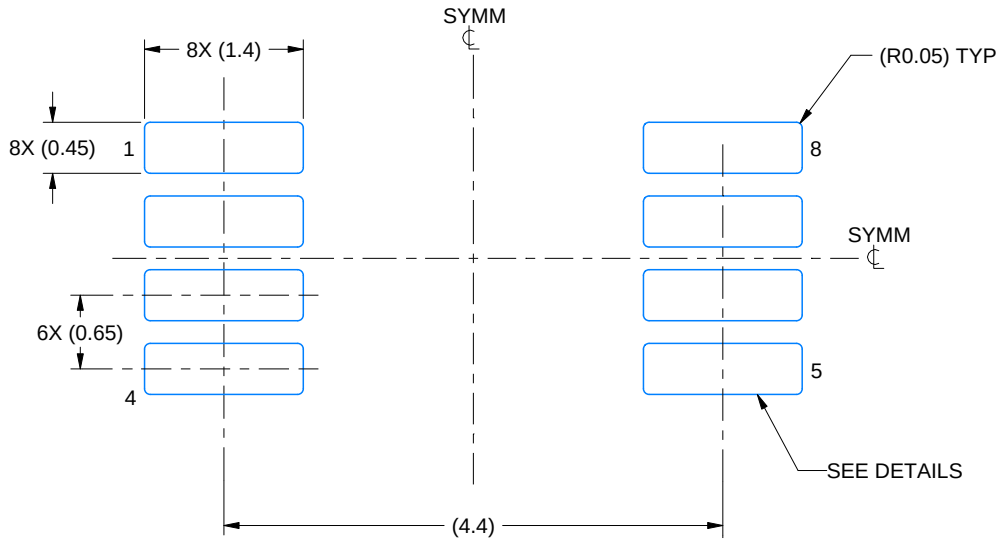
SMALL OUTLINE PACKAGE



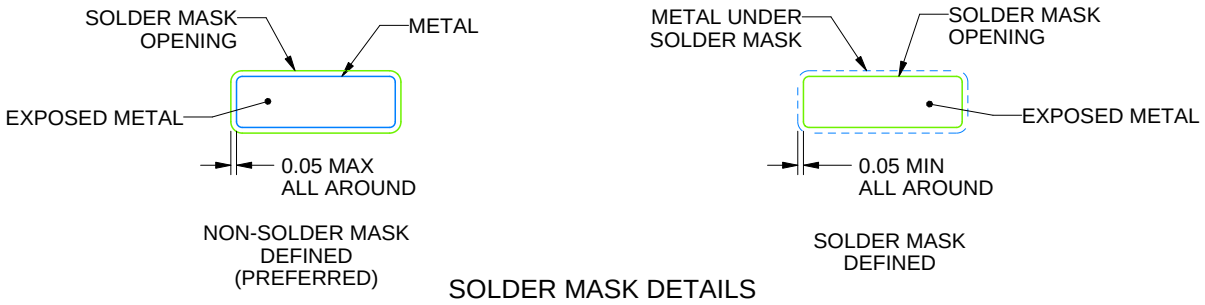
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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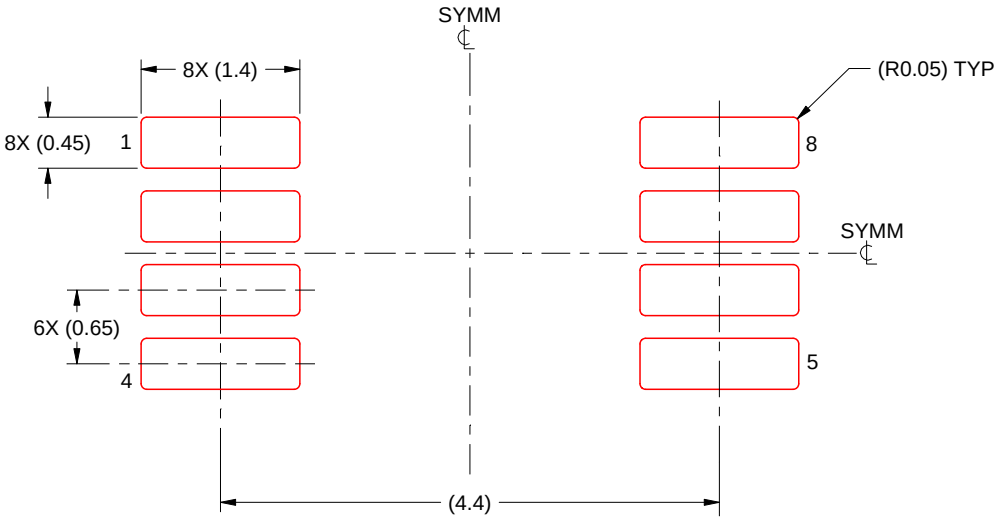
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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