TLV1704-SEP 2.2V～24V、宇宙向け強化プラスチックの耐放射線マイクロパワー クワッド コンパレータ

1 特長

- VID V62/18613
- 耐放射線
  - 単一イベント ラッチアップ (SEL) 耐性：125℃で 43MeV-cm^2/mg まで
  - 30krad(Si) まで ELDRS フリー
  - すべてのウェハー ロットについて、30krad(Si) までの吸収線量 (TID) RLAT
- 宇宙向け強化プラスチック
  - 管理されたベースライン
  - 金線
  - NiPdAu リード仕上げ
  - 単一のアセンブリ / テスト施設
  - 単一の製造施設
  - 軍用温度範囲 (–55℃～125℃) を供給可能
  - 長期にわたる製品ライフ サイクル
  - 製品変更通知期間の延長
  - 製品のトレーサビリティ
  - モールド コンパウンドの改良による低いガス放出
- 電源電圧範囲：2.2V～24V
- 低い静止電流：55µA (コンパレータあたり)
- 入力同相範囲に両レールを含む
- 小さい伝搬遅延：560ns
- 低い入力オフセット電圧：300µV
- オープン コレクタ出力：
  - 電源電圧に関係なく負電源を最大 24V 上回る
- 小型パッケージ：
  - クワッド：TSSOP-14

2 アプリケーション

- コマンドとデータの処理 (C&DH)
- 航空機のコックピット・ディスプレイ
- 飛行制御ユニット
- 衛星用電源システム (EPS)

3 概要

TLV1704-SEP (クワッド) デバイスは広い電源電圧範囲、レール ツー レール入力、小さい静止電流、短い伝搬遅延が特長です。これらの機能はすべて業界標準の TSSOP-14 プラスチック パッケージで提供されているため、これらのデバイスは、サイズ、重量、設計の柔軟性が重要なアプリケーションに適しています。

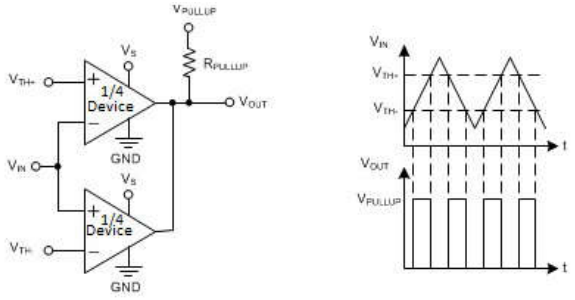
オープン コレクタ出力により、TLV1704-SEP の電源電圧に関係なく、負電源を最大 24V 上回る電圧レールまで出力をレベルシフトすることができます。同様に、出力を互いに接続して 1 つの ALERT 信号を形成できます。

このデバイスはマイクロパワー コンパレータです。低い入力オフセット電圧、小さい入力バイアス電流、小さい消費電流、オープン コレクタ構成により、TLV1704-SEP デバイスは電圧監視、電流センシング、ゼロクロス検出などのシステム診断に最適です。

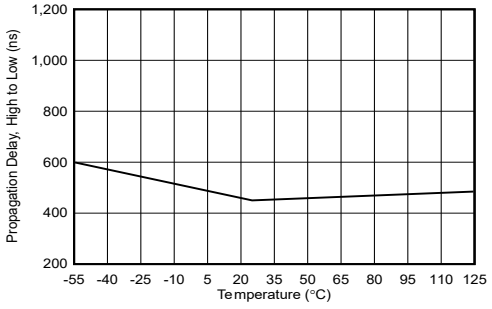
製品情報

部品番号	グレード (1)	パッケージ (2)
TLV1704AMPWTPSEP	30krad(Si) RLAT	TSSOP (14)
TLV1704AMPWPSEP		

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ オプションについての付録を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



ウィンドウ コンパレータとしての TLV1704-SEP



安定した伝搬遅延 対 温度

Table of Contents

4 Pin Configuration and Functions

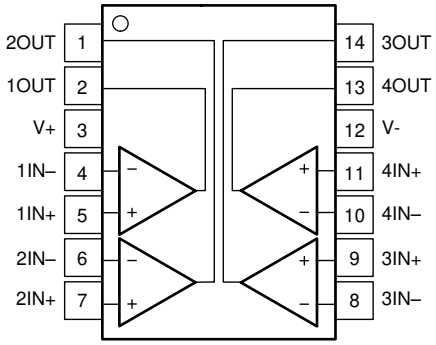


図 4-1. TLV1704-SEP PW Package
14-Pin TSSOP
Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	—	I	Noninverting input.
1IN+	5	I	Noninverting input, channel 1.
2IN+	7	I	Noninverting input, channel 2.
3IN+	9	I	Noninverting input, channel 3.
4IN+	11	I	Noninverting input, channel 4.
IN–	—	I	Inverting input.
1IN–	4	I	Inverting input, channel 1.
2IN–	6	I	Inverting input, channel 2.
3IN–	8	I	Inverting input, channel 3.
4IN–	10	I	Inverting input, channel 4.
OUT	—	O	Output.
1OUT	2	O	Output, channel 1.
2OUT	1	O	Output, channel 2.
3OUT	14	O	Output, channel 3.
4OUT	13	O	Output, channel 4.
V+	3	—	Positive (highest) power supply.
V–	12	—	Negative (lowest) power supply.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage			24	V
Signal input pins	Voltage(2)	(V_S–) – 0.5	(V_S+) + 0.5	V
	Current(2)		±10	mA
Output short-circuit(3)		Continuous		mA
Operating Junction temperature, T_J		–55	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground; one comparator per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V_S = (V_S+) – (V_S–)	2.2		24	V
Specified temperature	–55		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TLV1704-SEP PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = –55°C to 125°C, V_S = 2.2V to 24V, C_L = 15pF, R_{PULLUP} = 5.1kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C, V_S = 2.2V		±0.5	±3.5	mV
		T_A = 25°C, V_S = 24V		±0.3	±2.5	mV
		T_A = –55°C to 125°C			±5.5	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –55°C to 125°C		±4	±20	µV/°C
PSRR	Power-supply rejection ratio	T_A = 25°C		15	100	µV/V
		T_A = –55°C to 125°C		20		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –55°C to 125°C	(V–)		(V+)	V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		5	15	nA
		T_A = –55°C to 125°C			20	nA
I_{OS}	Input offset current	T_A = 25°C		0.5		nA
C_{LOAD}	Capacitive load drive		See *セクション 5.7*			
OUTPUT						
V_O	Voltage output swing from rail	I_O ≤ 4mA, input overdrive = 100mV, V_S = 24V			1100	mV
		I_O = 0mA, input overdrive = 100mV, V_S = 24V			700	mV
I_{SC}	Short circuit sink current	T_A = 25°C		20		mA
	Output leakage current	V_{IN+} > $V_{IN–}$, T_J = 25°C		70		nA
POWER SUPPLY						
V_S	Specified voltage range		2.2		24	V
I_Q	Quiescent current (per channel)	I_O = 0A , T_A = 25°C		55	75	µA
		I_O = 0A, T_A = –55°C to 125°C			100	µA

5.6 Switching Characteristics

at T_A = –55°C to 125°C, V_S = 2.2V to 24V, C_L = 15pF, R_{PULLUP} = 5.1kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL}	Propagation delay time, high-to-low	Input overdrive = 100mV, T_A = 25°C		460		ns
t_{pLH}	Propagation delay time, low-to-high	Input overdrive = 100mV, T_A = 25°C		560		ns
t_R	Rise time	Input overdrive = 100mV, T_A = 25°C		365		ns
t_F	Fall time	Input overdrive = 100mV, T_A = 25°C		240		ns

5.7 Typical Characteristics

at T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1kΩ, and input overdrive = 100mV (unless otherwise noted)

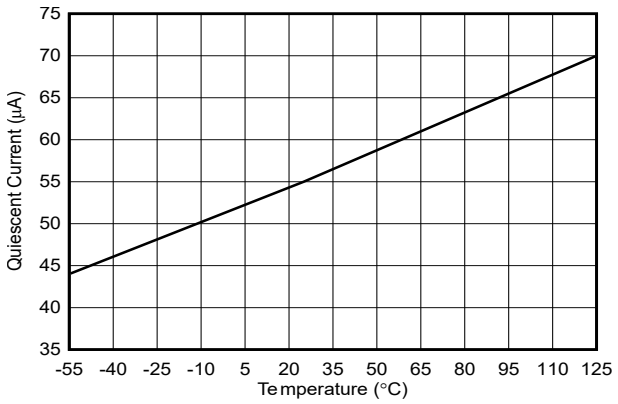


図 5-1. Quiescent Current vs Temperature

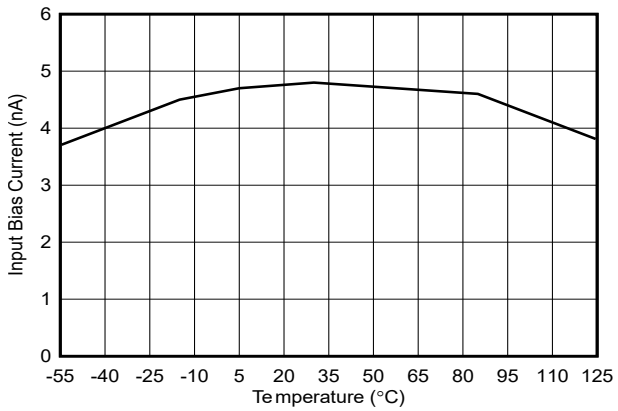


図 5-2. Input Bias Current vs Temperature

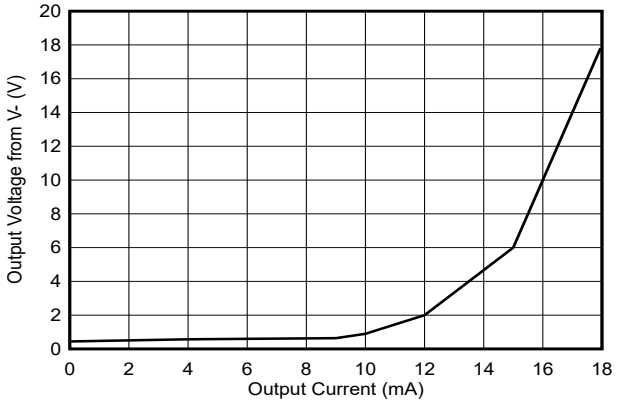
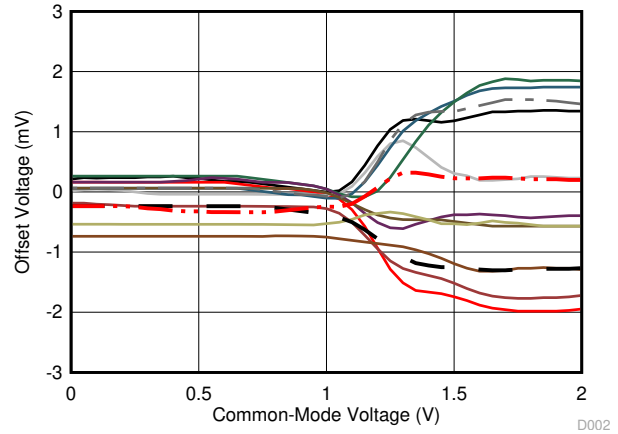


図 5-3. Output Voltage vs Output Current



V_S = 2.2V 13 typical units shown

図 5-4. Offset Voltage vs Common-Mode Voltage

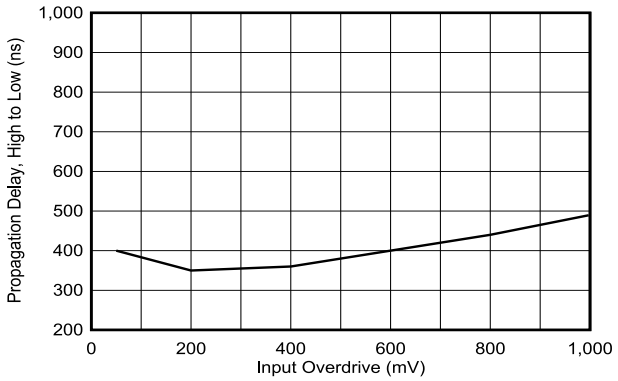
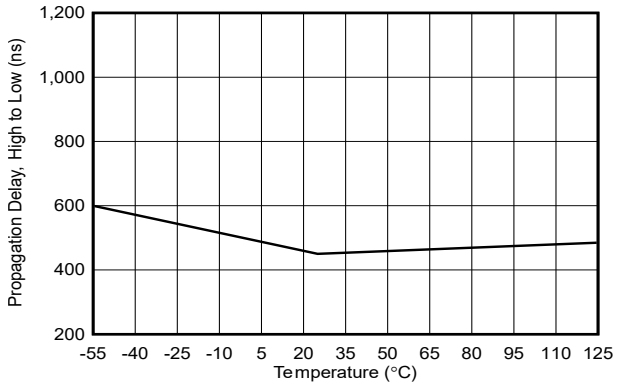


図 5-5. Propagation Delay vs Input Overdrive

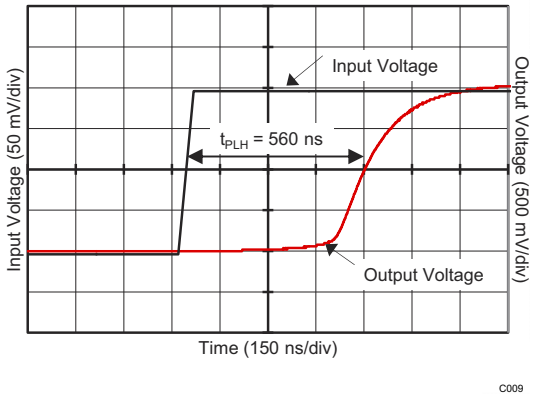


V_{OD} = 100mV

図 5-6. Propagation Delay vs Temperature

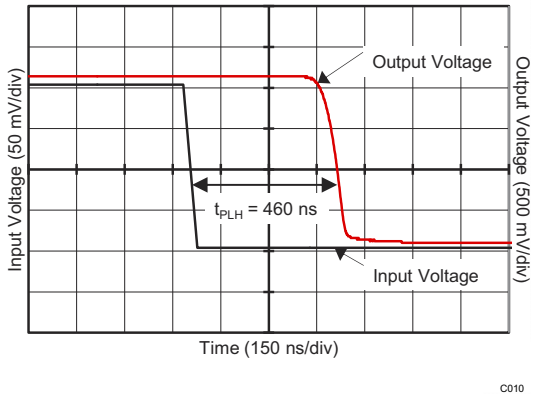
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1kΩ, and input overdrive = 100mV (unless otherwise noted)



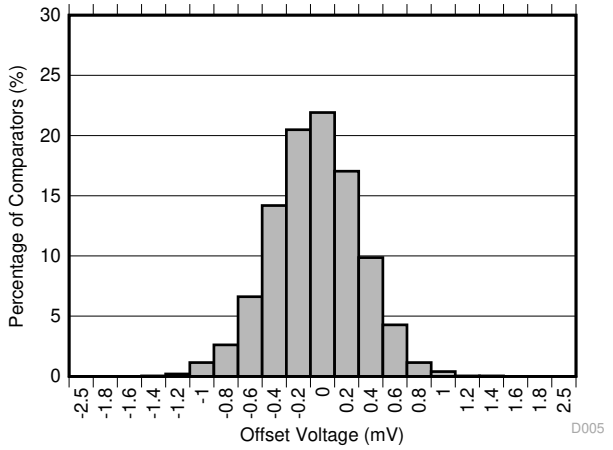
V_S = 2.2V Overdrive = 100mV

図 5-7. Propagation Delay (T_{pLH})



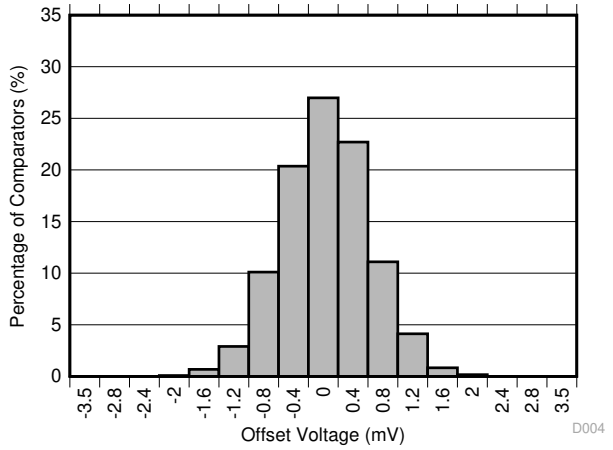
V_S = 2.2V Overdrive = 100mV

図 5-8. Propagation Delay (T_{pHL})



V_S = 24V Distribution taken from 2524 comparators

図 5-9. Offset Voltage Production Distribution



V_S = 2.2V Distribution taken from 2524 comparators

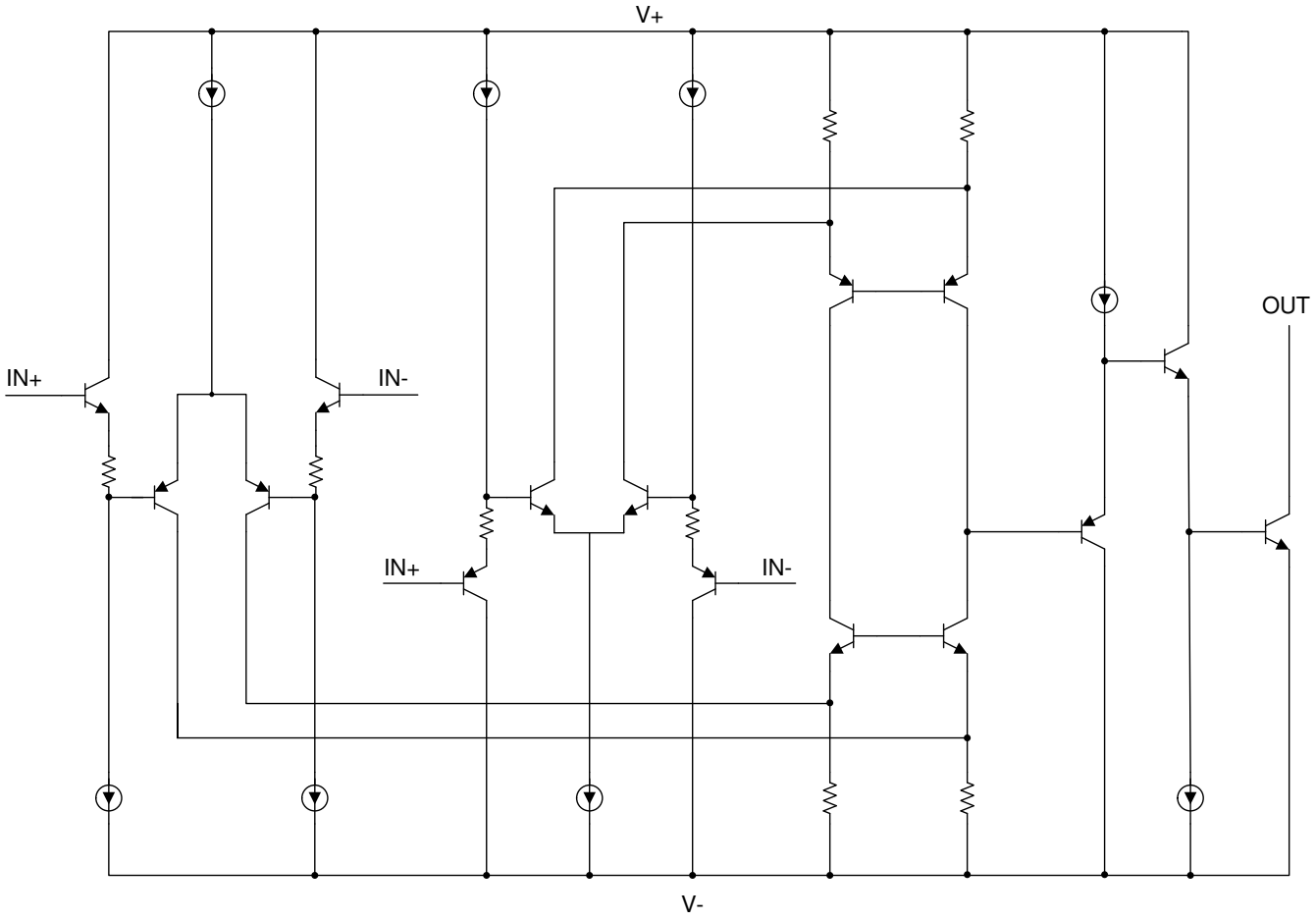
図 5-10. Offset Voltage Production Distribution

6 Detailed Description

6.1 Overview

The TLV1704-SEP comparator features rail-to-rail input and output on supply voltages as high as 24V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open-collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55µA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Comparator Inputs

The TLV1704-SEP device is a rail-to-rail input comparator, with an input common-mode range that includes the supply rails. The TLV1704-SEP device is designed to prevent phase inversion when the input pins exceed the supply voltage. 図 6-1 shows the TLV1704-SEP device response when input voltages exceed the supply, resulting in no phase inversion.

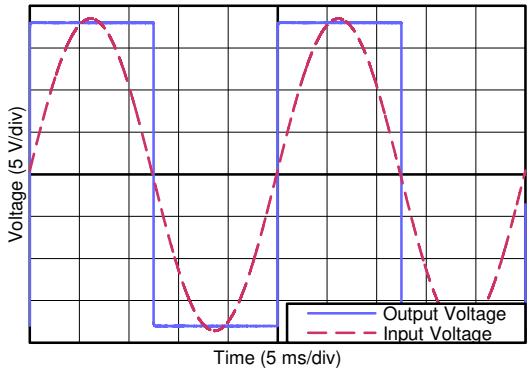


図 6-1. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

6.4 Device Functional Modes

6.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV1704-SEP device. The REF3333, as shown in 図 6-2, provides a 3.3V reference voltage with low drift and only 3.9µA of quiescent current.

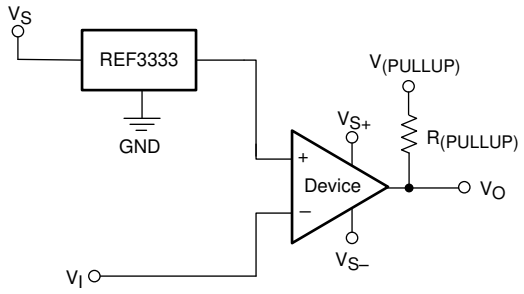


図 6-2. Reference Voltage for the TLV1704-SEP

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The TLV1704-SEP device can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

7.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

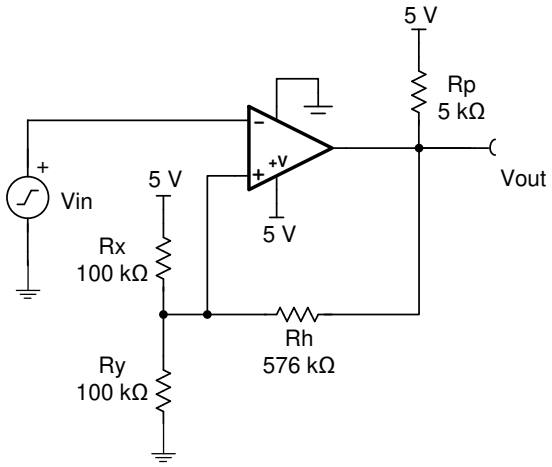


図 7-1. Comparator Schematic With Hysteresis

7.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5V
- Input: 0V to 5V
- Lower threshold (VL) = 2.3V ±0.1V
- Upper threshold (VH) = 2.7V ±0.1V
- VH – VL = 2.4V ±0.1V
- Low-power consumption

7.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

図 7-1 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if Rh > 100 Rp.

When the output is at a logic high (5V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7V. The input signal must drive above VH = 2.7V to cause the output to transition to logic low (0V).

When the output is at logic low (0V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3V. The input signal must drive below VL = 2.3V to cause the output to transition to logic high (5V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design TIPD144, *Comparator with Hysteresis Reference Design*.

7.2.3 Application Curve

図 7-2 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76V and the lower threshold is 2.34V, both of which are close to the design target.

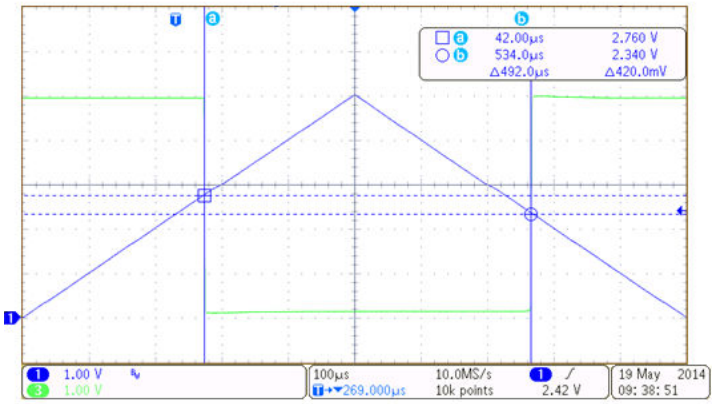


図 7-2. TLV1701 Upper and Lower Threshold With Hysteresis

7.3 Power Supply Recommendations

The TLV1704-SEP device is specified for operation from 2.2V to 24V; many specifications apply from –55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *セクション 5.7* section.

> **注意**
>
> Supply voltages larger than 40V can permanently damage the device; see the *セクション 5.1*.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *セクション 7.4.1* section.

7.4 Layout

7.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV1704-SEP device.
- To minimize supply noise, place a decoupling capacitor (0.1µF ceramic, surface-mount capacitor) as close as possible to V_S as shown in 図 7-3.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

7.4.2 Layout Example

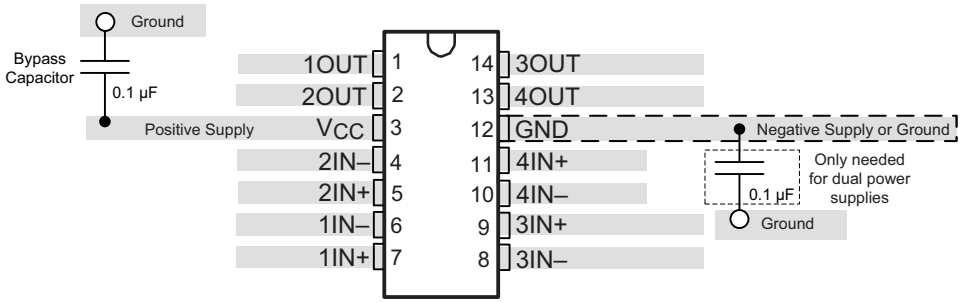


図 7-3. Comparator Board Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- *Precision Design, Comparator with Hysteresis Reference Design*, TIDU020
- *REF33xx 3.9-µA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/°C Drift Voltage Reference*, SBOS392

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2022) to Revision B (July 2024)	Page
• 最大電源電圧を 36V から 24V に変更	1
• 「製品情報」表のデバイス グレードを 20krad(Si) RLAT から 30krad(Si) RLAT に変更	1
• ドキュメント全体を通して計測のフォーマットを更新	1
• Updated the *Typical Performance Characteristics* graphs	6

Changes from Revision * (November 2018) to Revision A (November 2022)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• タイトルを「放射線耐性を強化」から「耐放射線」に更新	1
• 「アプリケーション」を更新し、リンクを追加	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1704AMPWPSEP	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
TLV1704AMPWTPSEP	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
V62/18613-01XE	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
V62/18613-01XE-T	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV1704-SEP :

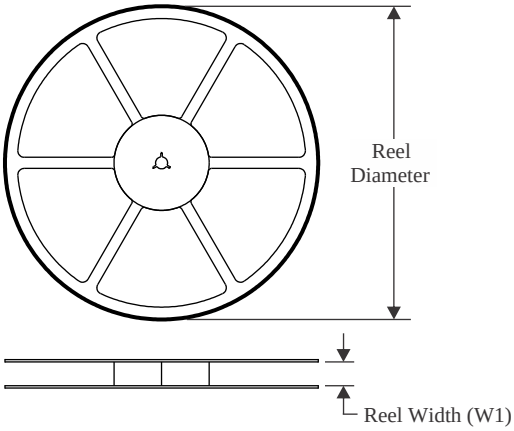
- Automotive : TLV1704-Q1

NOTE: Qualified Version Definitions:

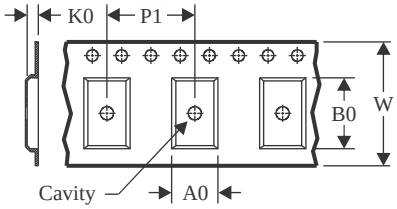
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

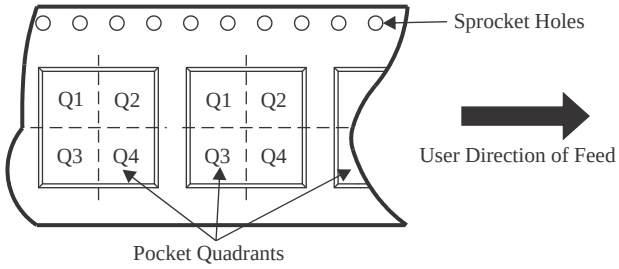


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

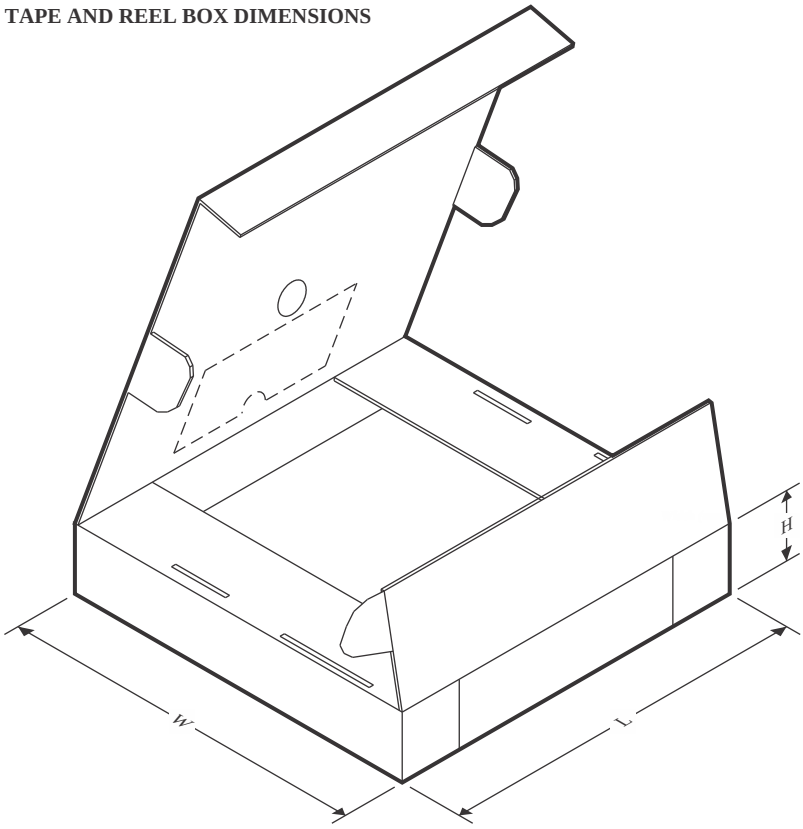
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1704AMPWTPSEP	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

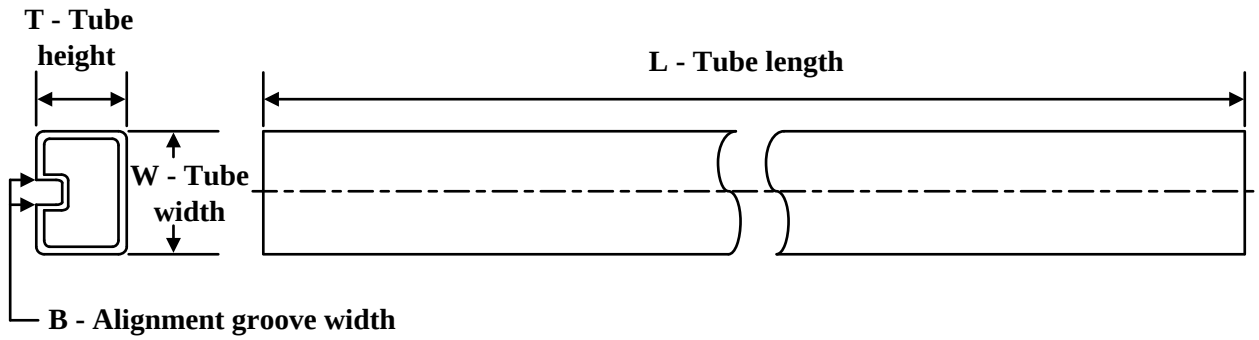
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1704AMPWTPSEP	TSSOP	PW	14	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

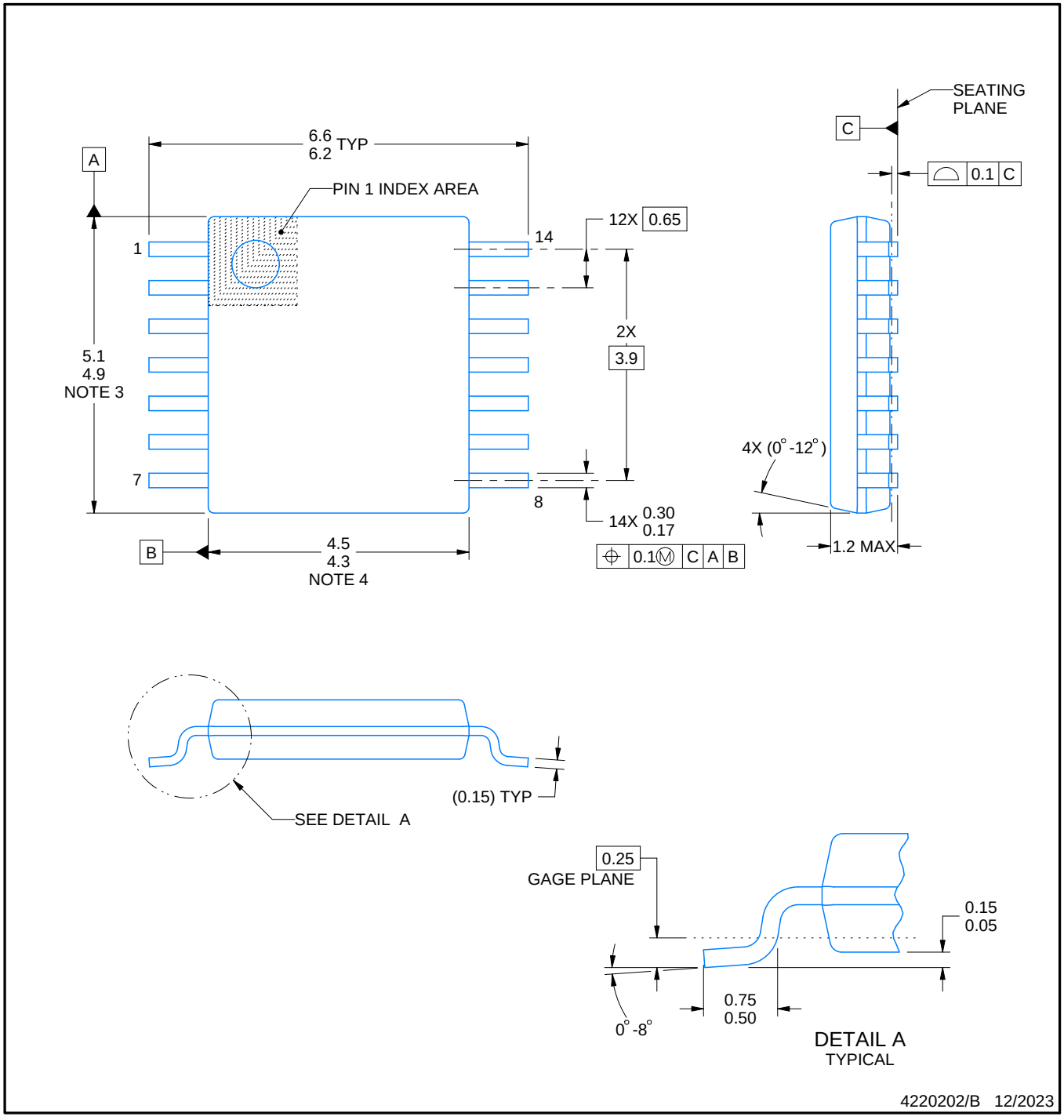
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV1704AMPWPSEP	PW	TSSOP	14	90	530	10.2	3600	3.5
V62/18613-01XE-T	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

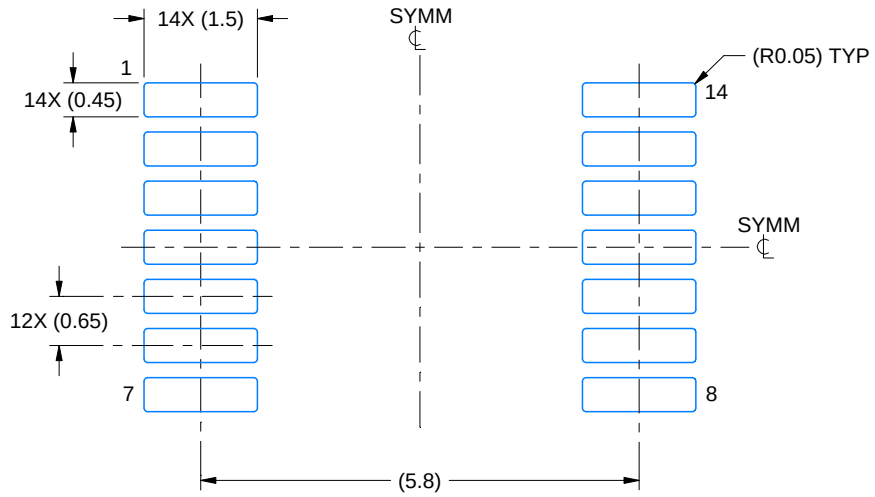
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

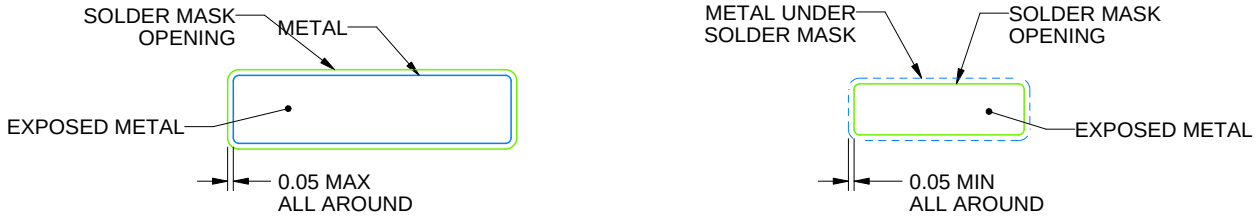


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

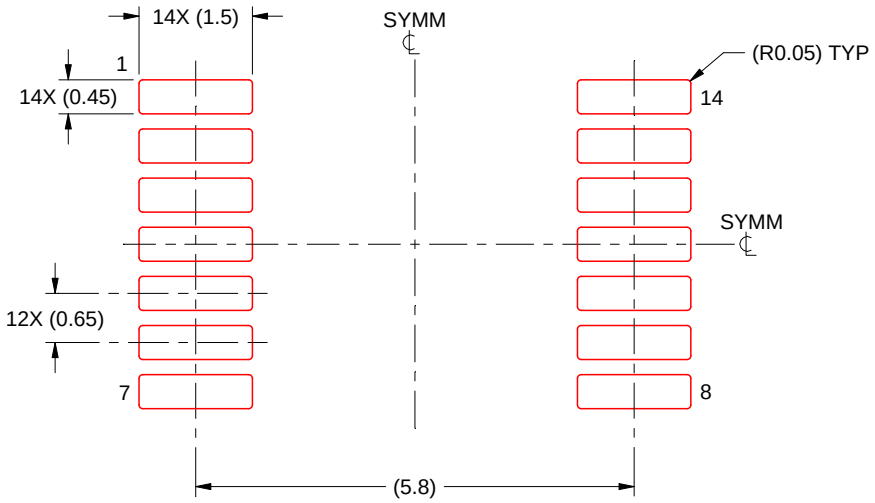


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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