TLC69629-Q1 Automotive 60mA, 48-Channel LED Driver with Integrated Oscillator , Advance Diagnostics and Cascaded Serial Interface

1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1: –40°C to 125°C ambient operating temperature
  - Device HBM classification level H1C
  - Device CDM classification level C4B
- Targeted Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL B
- 48 integrated current sinks
  - Programmable 16-bit PWM / Hybrid dimming
  - Programmable 7-bit analog dot correction (DC)
  - Maximum output current / voltage: 60mA / 16V
- Integrated 33MHz oscillator
  - 16-bit PWM output in 500Hz
  - >20KHz refresh rate with enhanced spectrum (ES) PWM
- High speed communication
  - Cascaded serial interface (CSI)
  - Data rates up to 17Mbps
- Power efficiency optimization
  - Adaptive headroom voltage control (AHVC)
  - Device power save mode (PSM)
- EMI mitigation
  - Interface: programmable buffer driving capability
  - Current sinks: phase shifting / spread spectrum
- Protection and Diagnostic
  - LED: open / short detection / health check
  - Current sink: adjacent-pin short / health check
  - Interface: CRC / command error / time-out error / communication watchdog
  - Device: under voltage / ISET out of range / thermal shutdown / memory CRC / OTP CRC / OSC watchdog

2 Applications

- Automotive Central Information Display
- Automotive Cluster Display
- Automotive Head-up Display

3 Description

The TLC69629-Q1 is a LED driver with 48 constant current sink channels which could provide up to 16-bit individual pixel-level LED PWM control. The additional 7-bit dot correction (DC) is also implemented to each channel to control peak current. Each device shares data stream by cascaded serial interface (CSI) which supports up to 511 devices connection. The interface is software compatible with LED drivers in the same group which can be applied to different application scenarios based on LED current and total LED number.
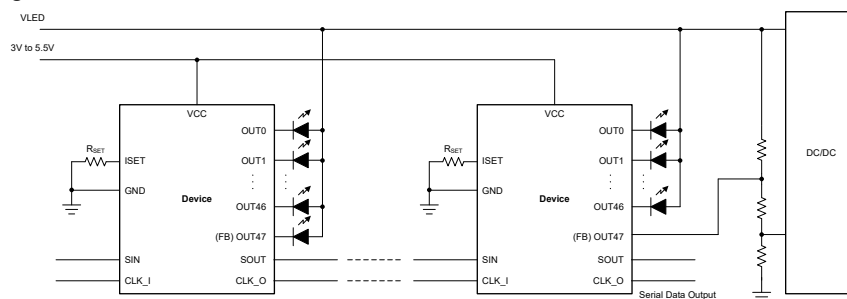
To optimize overall systematic power efficiency, the device is equipped with adaptive headroom voltage control (AHVC) scheme to optimize headroom voltage across each channel and device. Only the OUT47 pin from the last device of daisy chain is required to be programmed as FB pin to optimize LED supply voltage from DC/DC.

The TLC69629-Q1 is equipped diagnostics for LED, current sink, communication and device.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
TLC69629-Q1	VQFN (56) Wettable flank	8mm × 8mm
	HTSSOP (56)	14mm × 6.1mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

Table of Contents

ADVANCE INFORMATION

Product Folder Links: *TLC69629-Q1*

4 Device Comparison

PART NUMBER	CHANNEL NUMBER	MAX. CHANNEL CURRENT	FUNCTIONAL SAFETY CLASSIFICATION	INTERFACE	SOFTWARE COMPATIBLE
TLC69621-Q1 [(1)]	8	60mA	Functional Safety-Capable	SPI	Group 1
TLC69624-Q1 [(1)]	24				
TLC69627-Q1	48				
TLC69631-Q1 [(1)]	8	100mA			
TLC69634-Q1 [(1)]	24				
TLC69637-Q1	48				
TLC69622-Q1 [(1)]	8	60mA	Functional Safety-Compliant	SPI	Group 2
TLC69625-Q1 [(1)]	24				
TLC69628-Q1	48				
TLC69632-Q1 [(1)]	8	100mA			
TLC69635-Q1 [(1)]	24				
TLC69638-Q1	48				
TLC69623-Q1 [(1)]	8	60mA	Functional Safety-Compliant	CSI	Group 3
TLC69626-Q1 [(1)]	24				
TLC69629-Q1	48				
TLC69633-Q1 [(1)]	8	100mA			
TLC69636-Q1 [(1)]	24				
TLC69639-Q1	48				

(1)   Product preview

ADVANCE INFORMATION

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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5.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

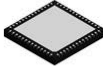TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

6 Revision History
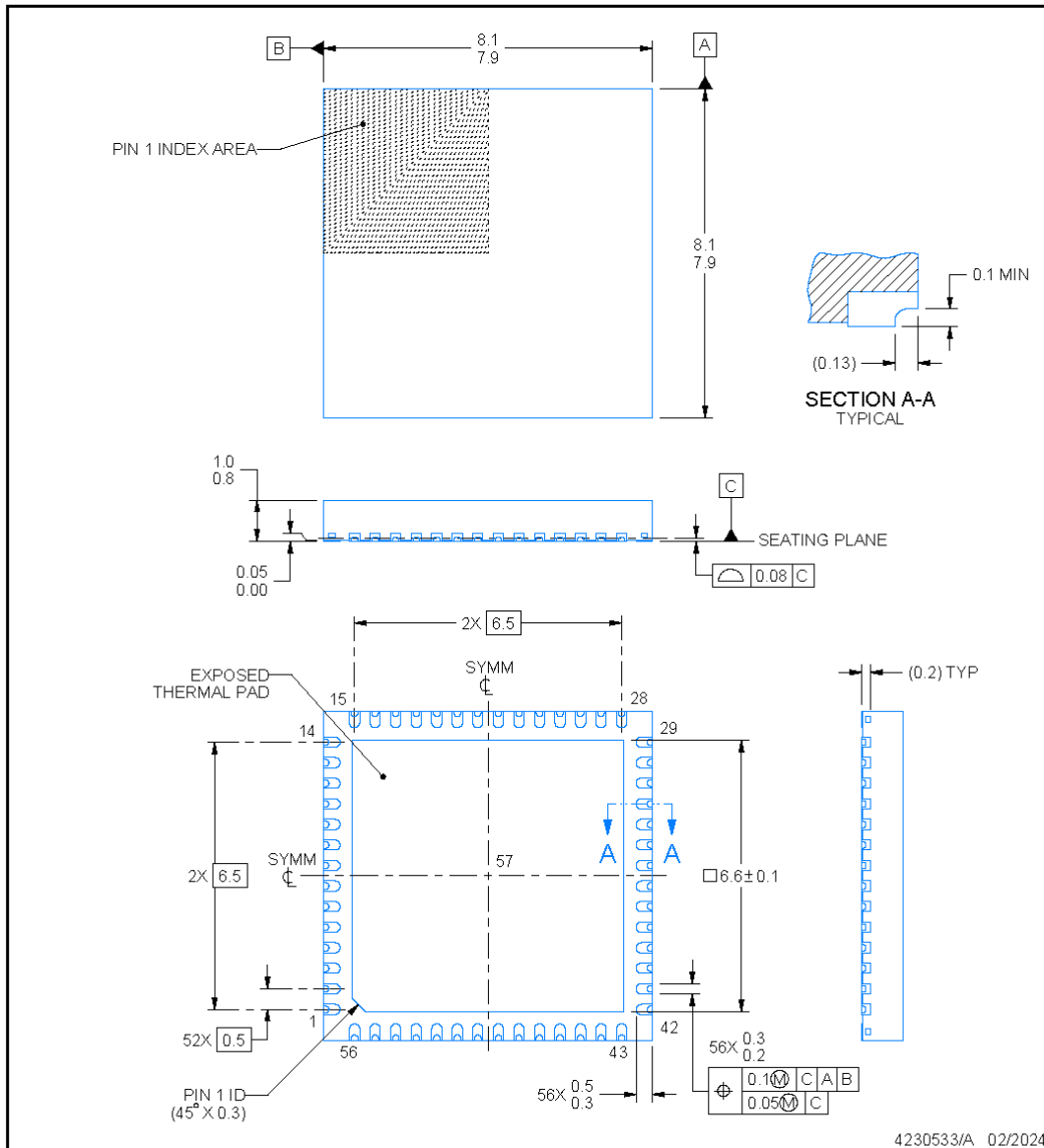
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2025	*	Advance Information Release

Product Folder Links: *TLC69629-Q1*

ADVANCE INFORMATION

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

RTQ0056K

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

PIN 1 INDEX AREA

8.1
7.9

8.1
7.9

0.1 MIN

(0.13)

SECTION A-A
TYPICAL

1.0
0.8

0.05
0.00

SEATING PLANE

0.08 C

EXPOSED
THERMAL PAD

2X 6.5

SYMM

2X 6.5

SYMM

57

□6.6±0.1

(0.2) TYP

PIN 1 ID
(45° X 0.3)

52X 0.5

56X 0.3
0.2

56X 0.5
0.3

56X 0.1 M C A B
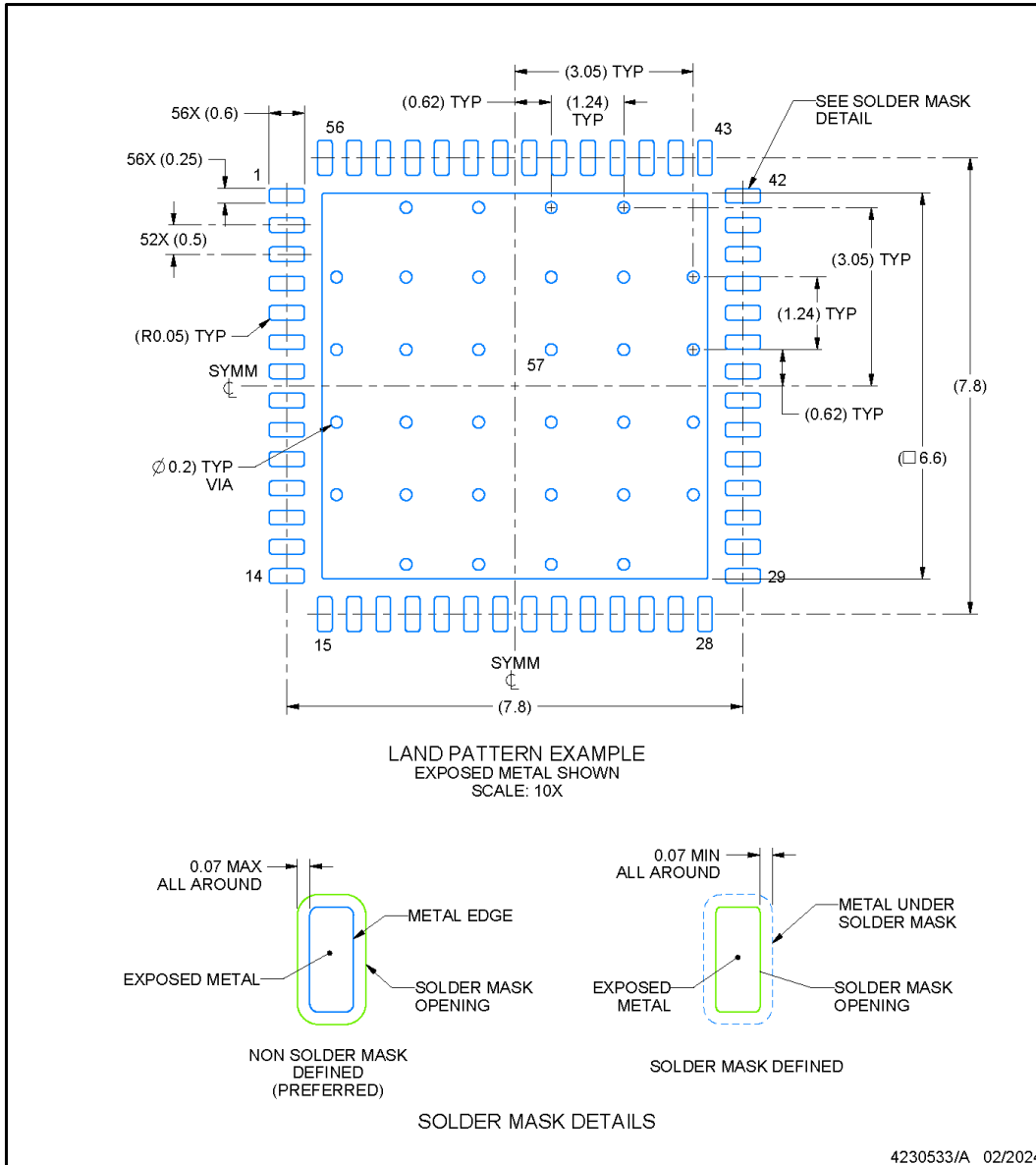0.05 M C

4230533/A 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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Product Folder Links: *TLC69629-Q1*

EXAMPLE BOARD LAYOUT

RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4230533/A 02/2024

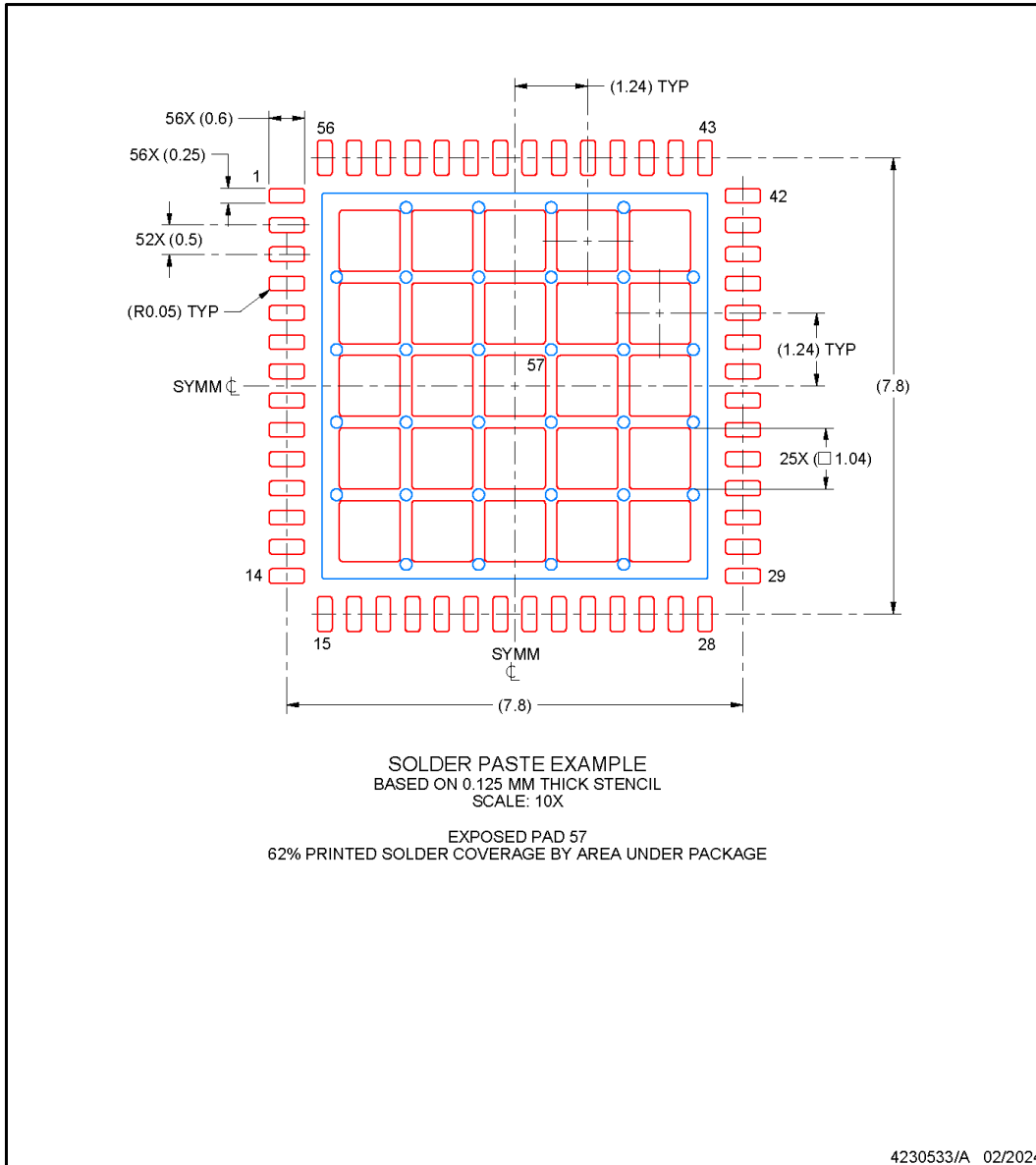**ADVANCE INFORMATION**

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
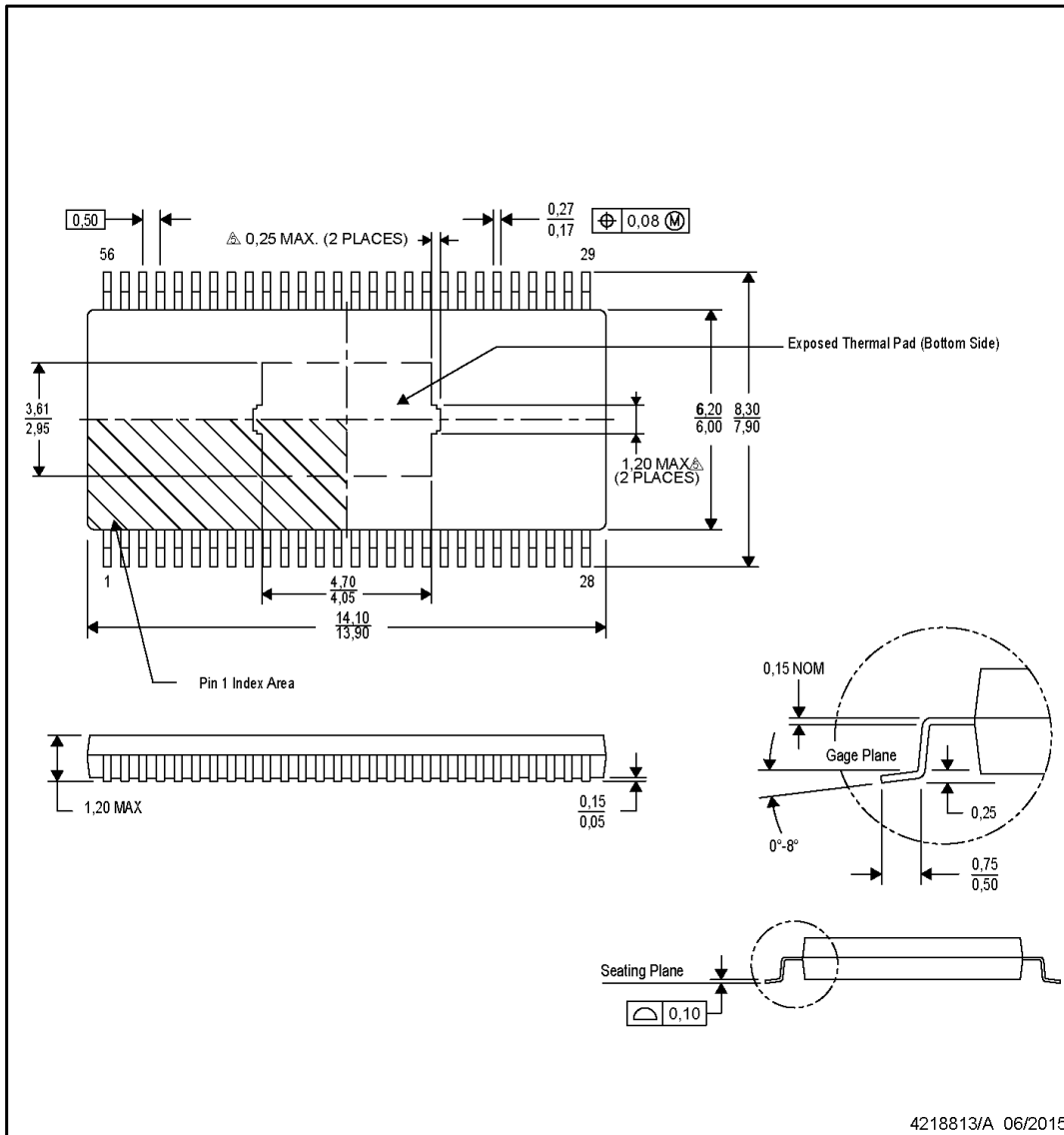
4230533/A   02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

![Texas Instruments logo]
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Product Folder Links: *TLC69629-Q1*

PACKAGE OUTLINE

DCA0056F

HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP

Exposed Thermal Pad (Bottom Side)

Pin 1 Index Area

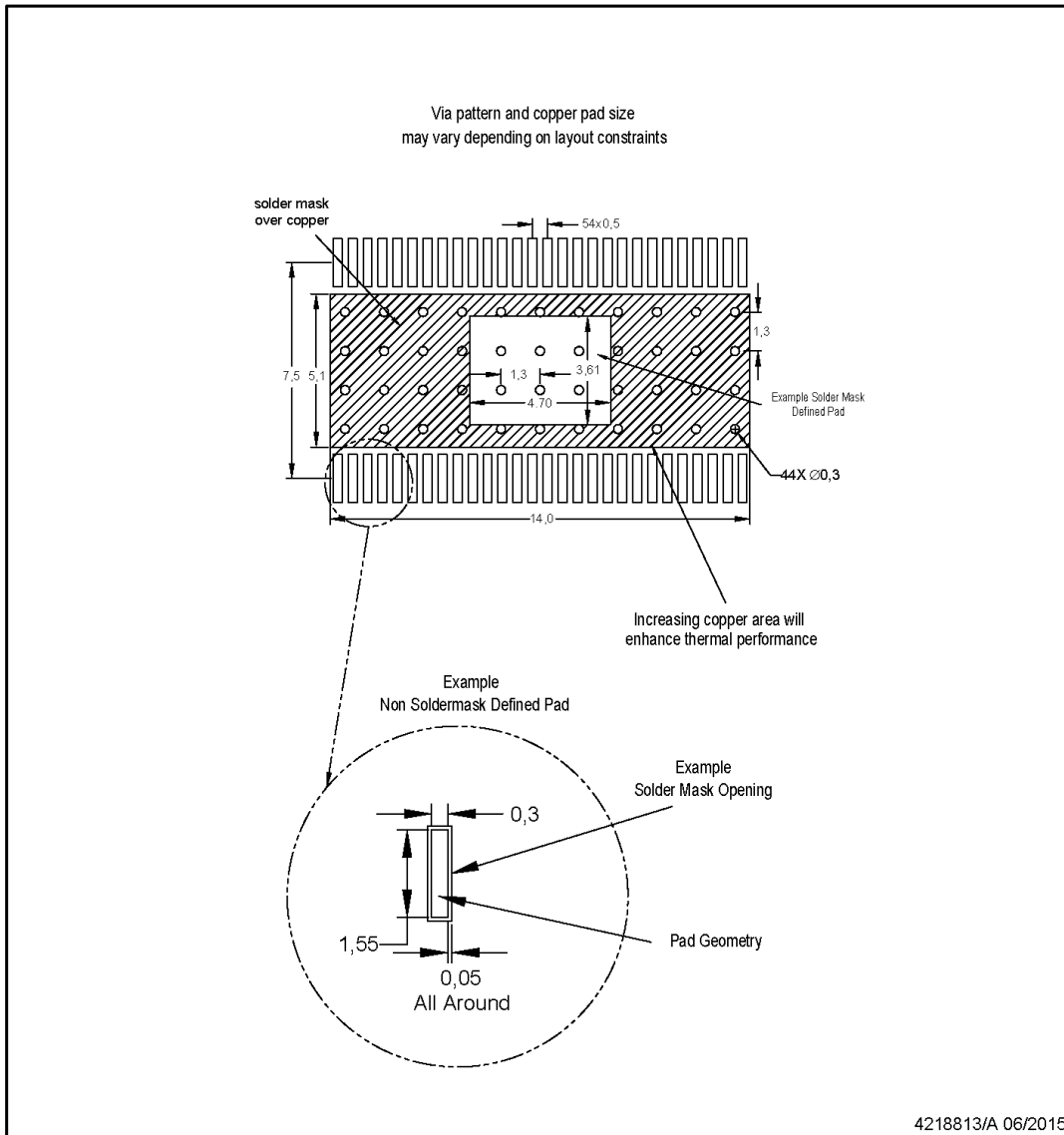Gage Plane

Seating Plane

4218813/A 06/2015

PowerPAD is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This package falls within JEDEC MO-153.
5. Keep- out features are identified to prevent board routing interference. These exposed metal features may vary within the identified area or completely absent on some devices.

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ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DCA0056F

HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP

Via pattern and copper pad size
may vary depending on layout constraints

solder mask over copper

54x0,5

1,3

7,5 5,1

1,3 3,61

4,70

Example Solder Mask Defined Pad

44X ⌀0,3

14,0

Increasing copper area will enhance thermal performance

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening

0,3

1,55

Pad Geometry
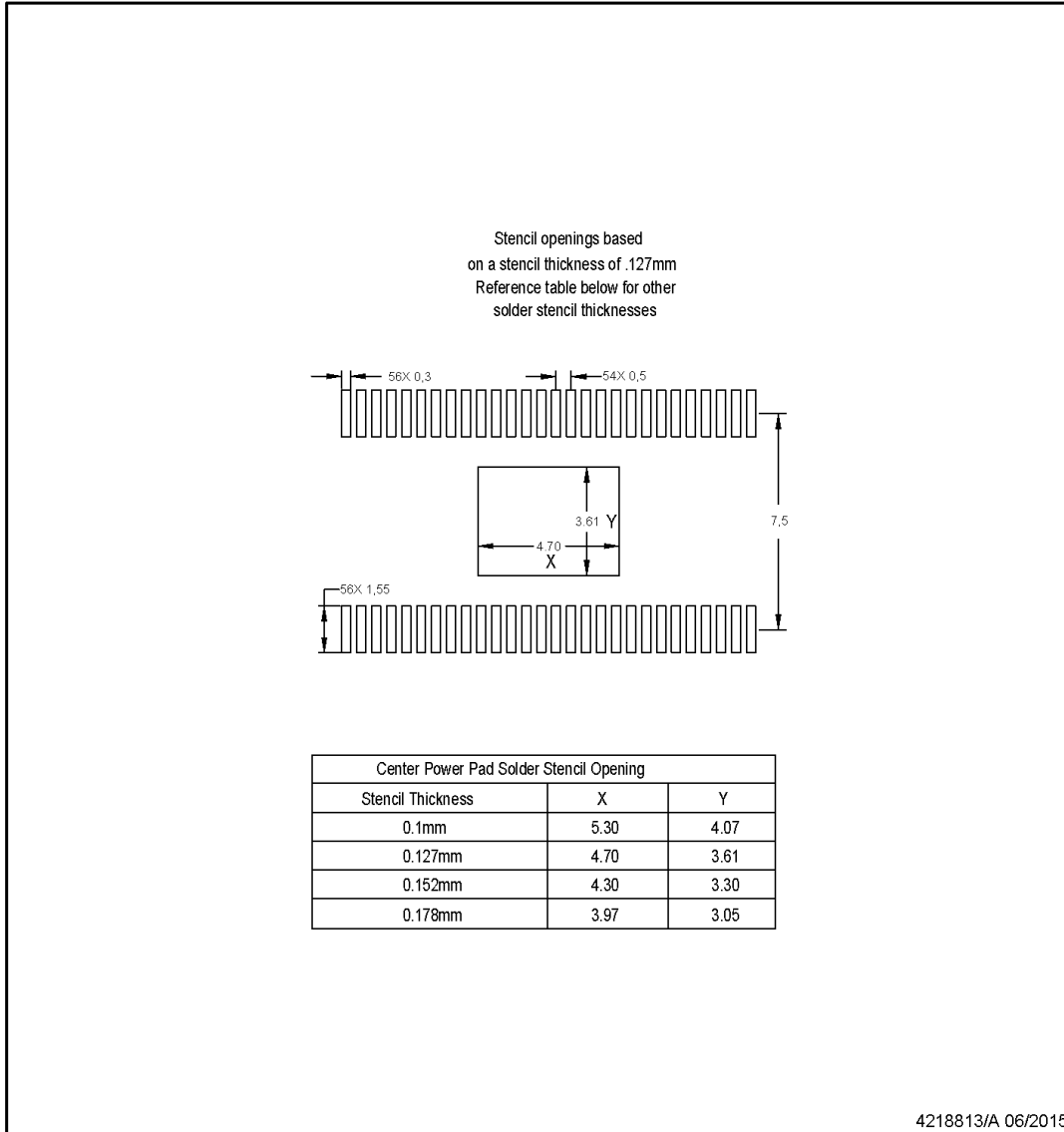
0,05
All Around

4218813/A 06/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, Powerpad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

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Product Folder Links: *TLC69629-Q1*

EXAMPLE STENCIL DESIGN

DCA0056F

HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP

Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses

56X 0,3   54X 0,5

3.61 Y

4.70

X

7,5

56X 1,55

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

4218813/A 06/2015
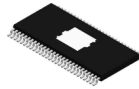
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.
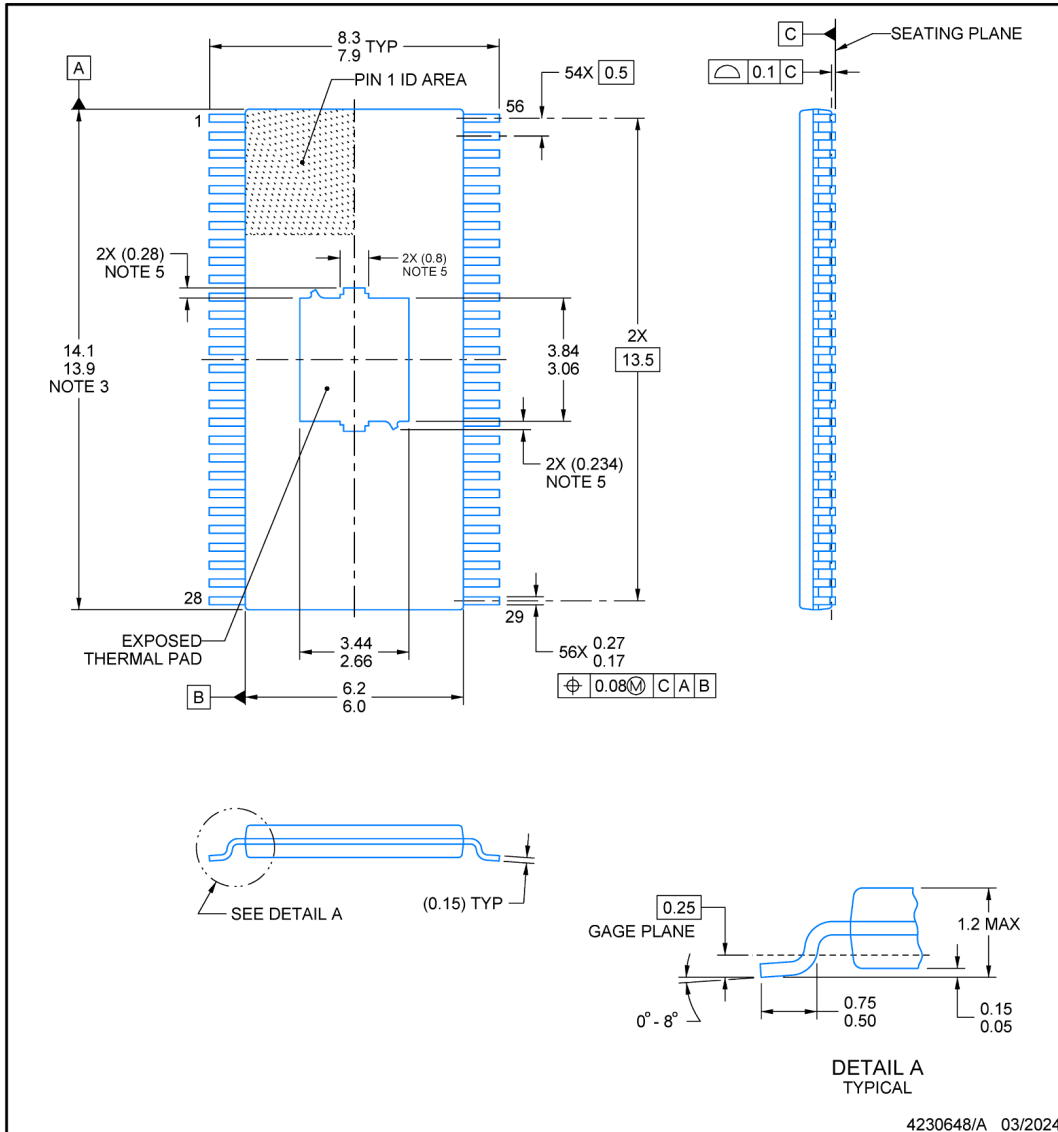
ADVANCE INFORMATION

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ADVANCE INFORMATION

PACKAGE OUTLINE

DFD0056D

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

8.3
7.9 TYP

PIN 1 ID AREA

54X 0.5

56

2X (0.28)
NOTE 5

2X (0.8)
NOTE 5

14.1
13.9
NOTE 3

3.84
3.06

2X
13.5

2X (0.234)
NOTE 5

28

29

EXPOSED
THERMAL PAD

3.44
2.66

6.2
6.0

56X 0.27
0.17

⊕ 0.08 Ⓜ C A B

C SEATING PLANE

0.1 C

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0° - 8°

0.75
0.50

1.2 MAX

0.15
0.05

DETAIL A
TYPICAL

4230648/A 03/2024

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NOTES:
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not present.
6. This package incorporates an exposed thermal pad that is designed to be attached directly to an external heat sink. This optimizes the heat transfer from the integrated circuit (IC).
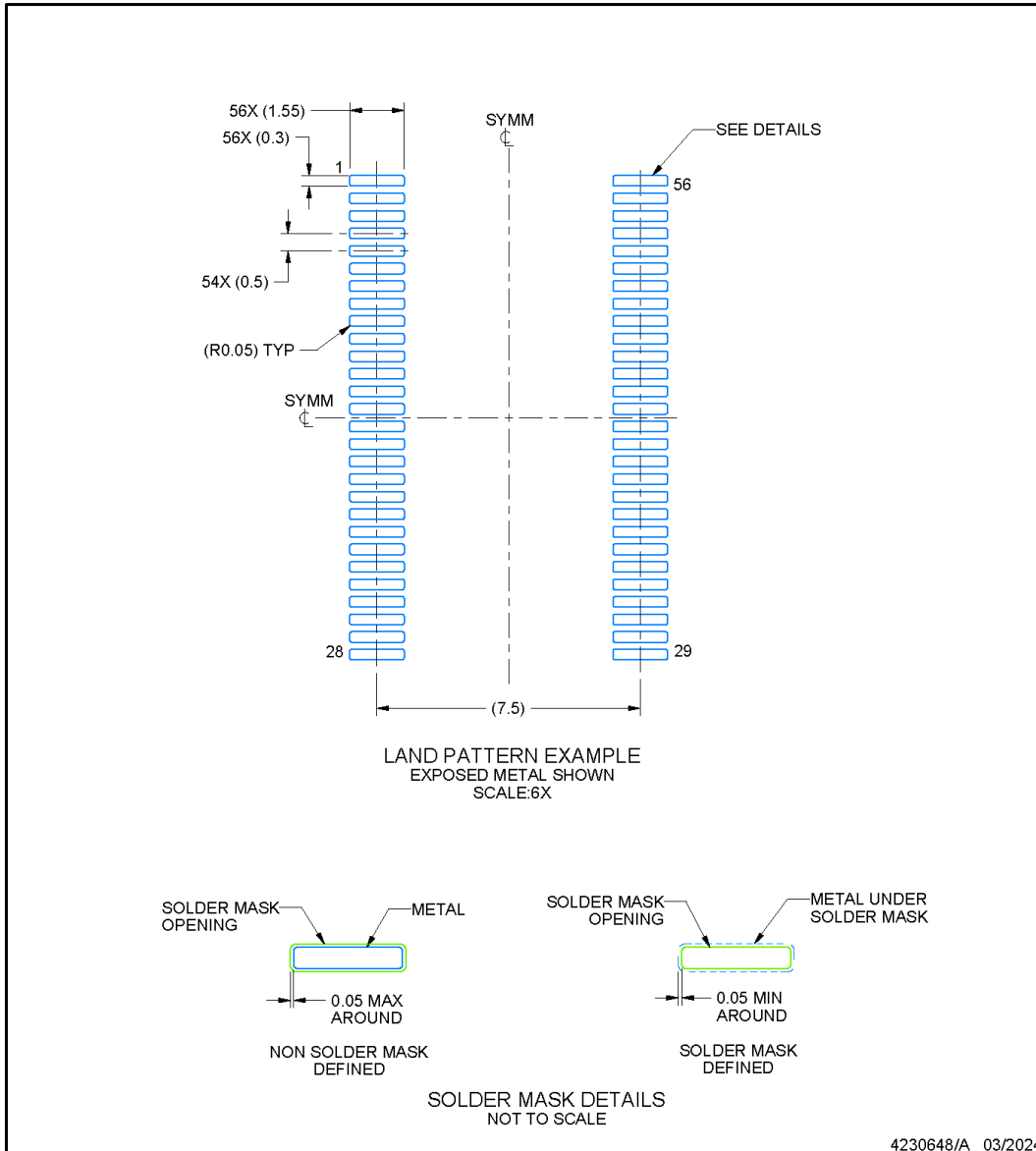
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Product Folder Links: *TLC69629-Q1*

EXAMPLE BOARD LAYOUT

DFD0056D   PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

SOLDER MASK DETAILS
NOT TO SCALE

4230648/A   03/2024

ADVANCE INFORMATION
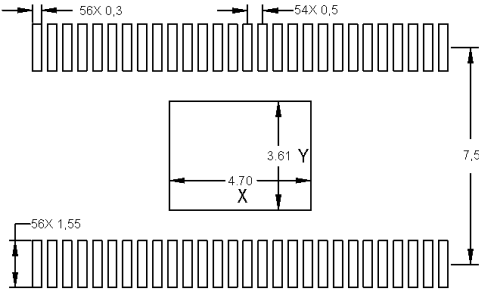
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DCA0056F
HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP

Stencil openings based
on a stencil thickness of .127mm
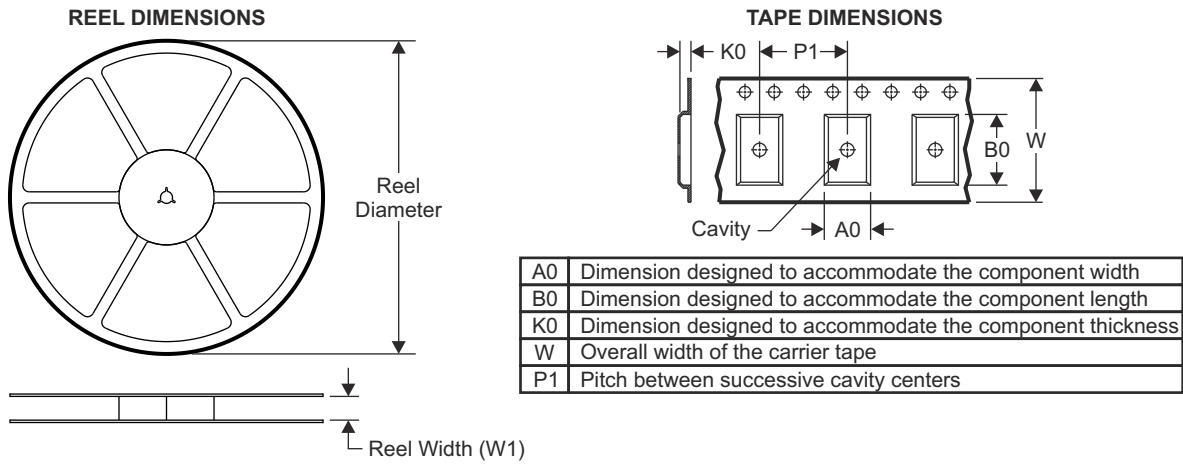Reference table below for other
solder stencil thicknesses

56X 0,3   54X 0,5

3.61 Y
4.70
X

7,5

56X 1,55

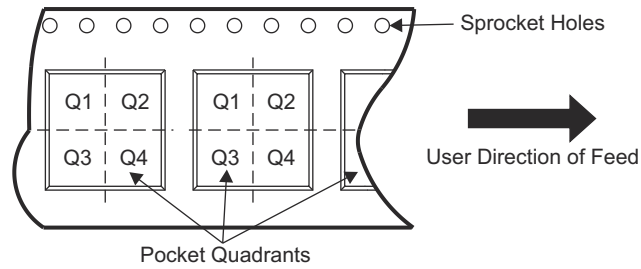| Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

4218813/A 06/2015

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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Product Folder Links: *TLC69629-Q1*

7.1 Tape and Reel Information

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC69629QDCARQ1	HTSSOP	DCA	56	2500	330	24.4	8.6	15.6	1.8	12	24	Q1
TLC69629QRTQRQ1	VQFN	RTQ	56	3500	330	16.4	8.3	8.3	1.1	12	16	Q2
TLC69629QDFDRQ1	HTSSOP	DFD	56	2500	330	24.4	8.9	14.7	1.4	12	24	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS
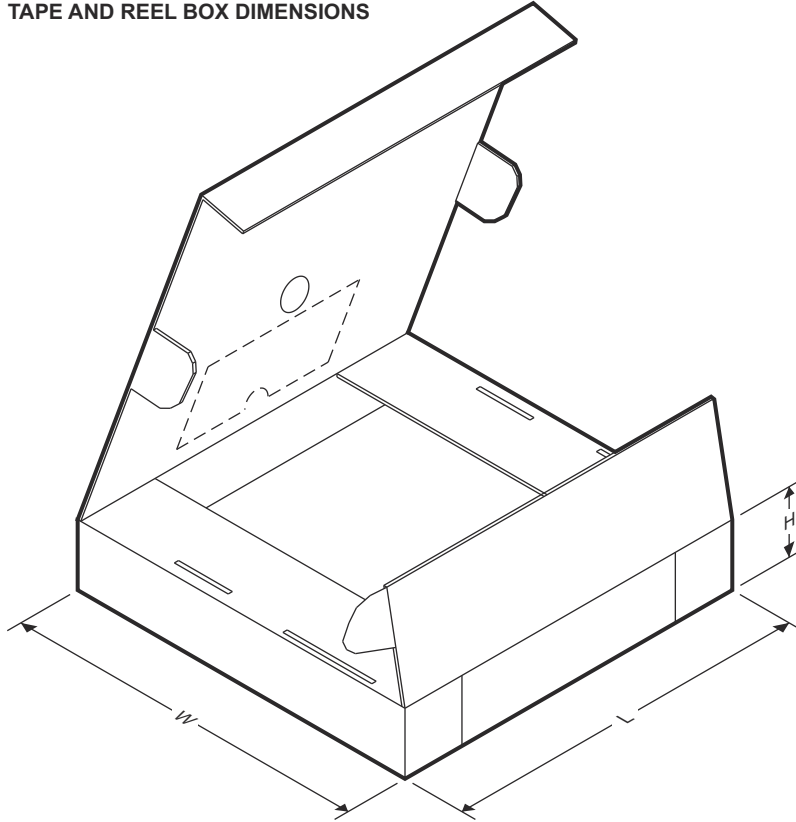
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC69629QDCARQ1	HTSSOP	DCA	56	2500	367	367	45
TLC69629QRTQRQ1	VQFN	RTQ	56	3500	367	367	35
TLC69629QDFDRQ1	HTSSOP	DFD	56	2500	350	350	43

Product Folder Links: *TLC69629-Q1*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLC69629QRTQRQ1	ACTIVE	QFN	RTQ	56	3500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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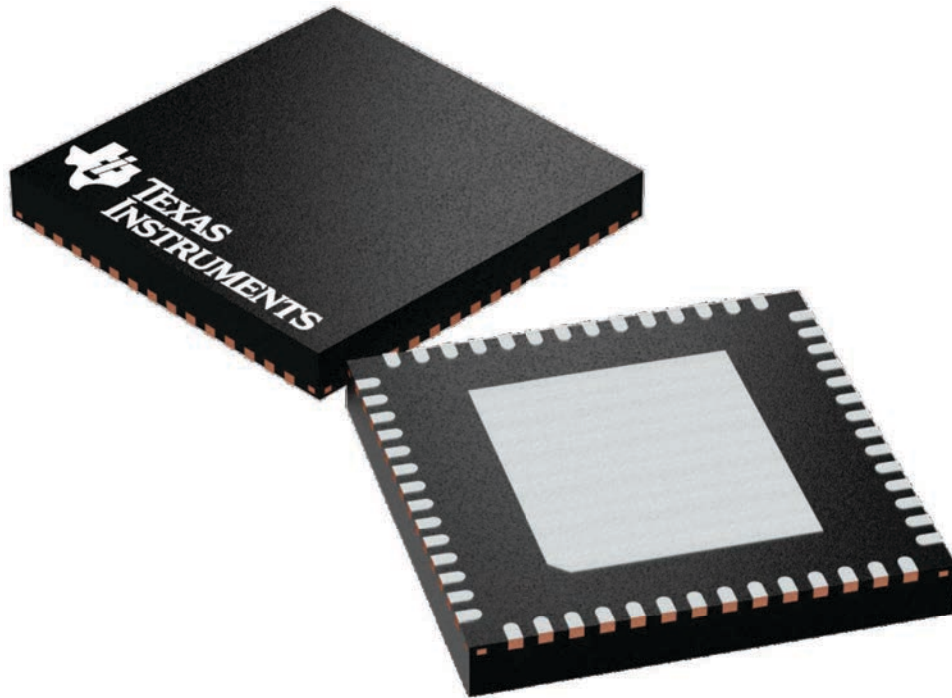
RTQ 56

8 x 8, 0.5 mm pitch

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224653/A

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