TL331B-Q1、TL391B-Q1、TL331-Q1 車載用シングル・コンパレータ

1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～125℃ (B および Q バージョン)
  - デバイス温度グレード 3:–40℃～85℃ の周囲動作温度範囲 (I バージョン)
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C5
- 新製品 TL331B-Q1 および TL391B-Q1
- 広い電源電圧範囲、2V～36V
- 電源電圧にかかわらず低い電源電流ドレイン: 標準値 0.43mA (B バージョン)
- 低い入力バイアス電流、3.5nA (標準値)
- 低い入力オフセット電圧、代表値 0.37mV (B バージョン)
- 差動入力電圧範囲は最大定格電源電圧と同じ、±36V
- 入力範囲はグランドを含む
- ピン配置が異なる TL391B-Q1
- TTL、MOS、CMOS 互換出力

2 アプリケーション

- 車載用
- HEV/EV およびパワートレイン
- インフォテインメントとクラスタ
- ボディ・コントロール・モジュール

3 概要

TL331B-Q1 および TL391B-Q1 デバイスは、業界標準の TL331-Q1 コンパレータの次世代バージョンです。これらの次世代デバイスは、小さいオフセット電圧、高い電源電圧への対応、小さい消費電流、小さい入力バイアス電流、小さい伝搬遅延、専用の ESD 保護セル、負電圧入力対応の改善などの特長があり、コストの制約が厳しい用途で大きな価値を提供します。TL331B-Q1 は、TL331-Q1 の「I」バージョンと「Q」バージョンの両方にそのまま代替可能です。TL391B-Q1 は、TL331B-Q1 のピン配置が異なる製品です。

このデバイスは、広い電圧範囲にわたって単一電源で動作するように設計されたシングル電圧コンパレータです。デュアル電源での動作も可能です。この場合、2 つの電源の差が 2V～36V で、V_{CC} が入力同相電圧よりも 1.5V 以上高いことが条件です。電流ドレインは、電源電圧に依存しません。出力を他のオープンコレクタ出力に接続して、ワイヤード AND の関係を構成できます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TL331B-Q1、TL391B-Q1、TL331-Q1	SOT-23 (5)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ファミリ比較表

仕様	TL331B-Q1 TL391B-Q1	TL331I-Q1	TL331Q-Q1	単位
電源電圧	2～36	2～36	2～36	V
総電源電流 (5V～36V (最大値))	0.43	0.7	0.7	mA
温度範囲	-40～125	-40～85	-40～125	℃
ESD (HBM)	2000	2000	2000	V
オフセット電圧 (全温度範囲での最大値)	±4	±9	±9	mV
入力バイアス電流 (標準値 / 最大値)	3.5/25	25/250	25/250	nA
応答時間 (標準値)	1	1.3	1.3	µsec

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (January 2021) to Revision G (August 2023) — **Page**

- Added reference to Application Note ... 16

Changes from Revision E (November 2020) to Revision F (January 2021) — **Page**

- 表紙のリンク・テキストで欠けていた「B」を追加 ... 1

Changes from Revision D (June 2020) to Revision E (November 2020) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 全体にわたって TL331B-Q1 および TL391B-Q1 の最小推奨電源電圧を 2V に変更 ... 1
- 「ファミリ比較表」ですべてのデバイスの電源電圧を訂正 ... 1
- Added TL331B-Q1 and TLV391B-Q1 Typical Graphs ... 9

Changes from Revision C (October 2013) to Revision D (June 2020) — **Page**

- B デバイスを追加。最新の TI データシートのフォーマットに更新。表紙のテキストを変更し、B バージョンを強調。 ... 1
- 「ファミリ比較表」を追加。 ... 1
- 「ファミリ表」にリンクを追加 ... 1

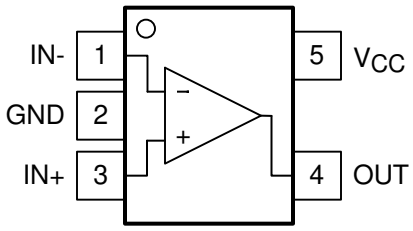
Changes from Revision B (September 2012) to Revision C (October 2013) — **Page**

- Changed V_{ICR} in the Electrical Characteristics ... 7
- Changed test conditions of I_{OL} in the Electrical Characteristics ... 7

Changes from Revision A (July 2010) to Revision B (September 2012) — **Page**

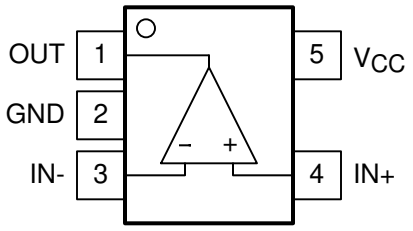
- Changed V_{ICR} in the Electrical Characteristics ... 7

5 Pin Configuration and Functions



Note reversed inputs compared to similar popular pinout

図 5-1. TL331-Q1, TL331B-Q1 DBV Package
5-Pin SOT-23
Top View



Note reversed inputs compared to similar popular pinout

図 5-2. TL391B-Q1 DBV Package
5-Pin SOT-23
Top View

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
	TL331-Q1, TL331B-Q1	TL391B-Q1		
NAME	NO.	NO.		
IN+	3	4	I	Positive Input
IN–	1	3	I	Negative Input
OUT	4	1	O	Open Collector/Drain Output
V_{CC}	5	5	—	Power Supply Input
GND	2	2	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings, TL331-Q1

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	0	36	V
V_{ID}	Differential input voltage(3)	–36	36	V
V_I	Input voltage range (either input)	–0.3	36	V
V_O	Output voltage	0	36	V
I_O	Output current	0	20	mA
	Duration of output short-circuit to ground(4)	Unlimited		
T_J	Operating virtual junction temperature	150		°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 Absolute Maximum Ratings, TL331B-Q1 and TL391B-Q1

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	-0.3	38	V
V_{ID}	Differential input voltage(3)	–38	38	V
V_I	Input voltage range (either input)	–0.3	38	V
V_O	Output voltage	-0.3	38	V
I_O	Output current		20	mA
	Duration of output short-circuit to ground(4)	Unlimited		
I_{IK}	Input current(5)		–50	mA
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
(5) Input current flows thorough parasitic diode to ground and will turn on parasitic transistors that will increase ICC and may cause output to be incorrect. Normal operation resumes when input current is removed.

6.3 ESD Ratings, All Devices

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions, TL331-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	36	V
T_J	Junction temperature, TL331IDBVRQ1	–40	85	°C
T_J	Junction temperature, TL331QDBVRQ1	–40	125	°C

6.5 Recommended Operating Conditions, TL331B-Q1 and TL391B-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	36	V
T_J	Junction temperature	–40	125	°C

6.6 Thermal Information

THERMAL METRIC[1]		TL331-Q1	TL331B-Q1, TL391B-Q1	UNIT
		DBV (SOT-23)	DBV (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	218.3	211.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.3	133.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.9	79.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	56.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.1	79.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics, TL331B-Q1 and TL391B-Q1

V_S = 5 V, V_{CM} = (V–) ; T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_S = 5 to 36V	–2.5	±0.37	2.5	mV
		V_S = 5 to 36V, T_A = –40°C to +125°C	–4		4	
I_B	Input bias current			–3.5	–25	nA
		T_A = –40°C to +125°C			–50	nA
I_{OS}	Input offset current		–10	±0.5	10	nA
		T_A = –40°C to +125°C	–25		25	nA
VCM	Common mode range	V_S = 3 to 36V	(V–)		(V+) – 1.5	V
		V_S = 3 to 36V, T_A = –40°C to +125°C	(V–)		(V+) – 2.0	V
A_{VD}	Large signal differential voltage amplification	V_S = 15V, V_O = 1.4V to 11.4V; R_L ≥ 15k to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V–)}	I_{SINK} ≤ 4mA, V_{ID} = -1V		110	400	mV
		I_{SINK} ≤ 4mA, V_{ID} = -1V T_A = –40°C to +125°C			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 5 V; V_{ID} = 1V		0.1	20	nA
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 36V; V_{ID} = 1V; T_A = –40°C to +125°C			1000	nA
I_{OL}	Low level output current	V_{OL} = 1.5V; V_{ID} = -1V; V_S = 5V	6	18		mA
I_Q	Quiescent current	V_S = 5 V, no load		210	330	µA
		V_S = 36 V, no load, T_A = –40°C to +125°C		275	430	µA

6.8 Switching Characteristics, TL331B-Q1 and TL391B-Q1

V_S = 5V, V_{O_PULLUP} = 5V, V_{CM} = V_S/2, C_L = 15pF, R_L = 5.1k Ohm, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{response}$	Propagation delay time, high-to-low; Small scale input signal (1)	Input overdrive = 5mV, Input step = 100mV		1000		ns
$t_{response}$	Propagation delay time, high-to-low; TTL input signal (1)	TTL input with V_{ref} = 1.4V		300		ns

(1) High-to-low and low-to-high refers to the transition at the input.

6.9 Electrical Characteristics, TL331-Q1

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V, V_{IC} = $V_{IC(min)}$	25°C		2	5	mV
			–40°C to 125°C			9	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		5	50	nA
			–40°C to 125°C			250	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		–25	–250	nA
			–40°C to 125°C			–400	
V_{ICR}	Common-mode input voltage range[2]		25°C	0 to V_{CC} – 1.5			V
			–40°C to 125°C	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}	25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V, V_{ID} = 1 V	25°C		0.1	50	nA
		V_{OH} = 30 V, V_{ID} = 1 V	–40°C to 125°C			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, V_{ID} = –1 V	25°C		150	400	mV
			–40°C to 125°C			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V, V_{ID} = –1 V	25°C	6			mA
I_{CC}	Supply current	R_L = ∞, V_{CC} = 5 V	25°C		0.4	0.7	mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V at 25°C, but either or both inputs can go to 30 V without damage.

6.10 Switching Characteristics, TL331-Q1

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF[1] [2]	100-mV input step with 5-mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

6.11 Typical Characteristics, TL331-Q1

T_A= 25°C, V_S= 5V, R_{PULLUP}=5.1k, C_L = 15 pF, V_{CM}= 0 V unless otherwise noted.

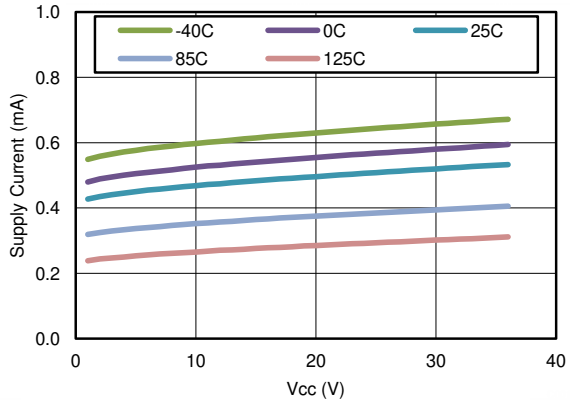


図 6-1. Supply Current vs Supply Voltage

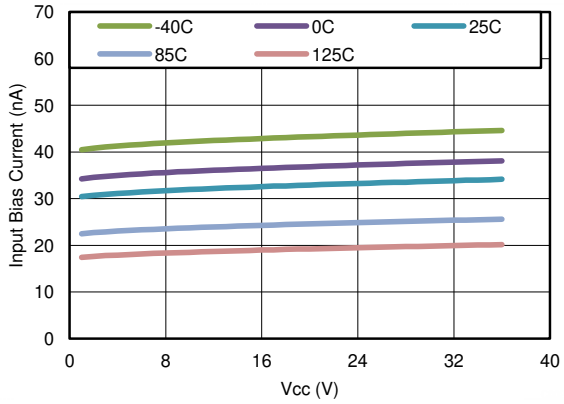


図 6-2. Input Bias Current vs Supply Voltage

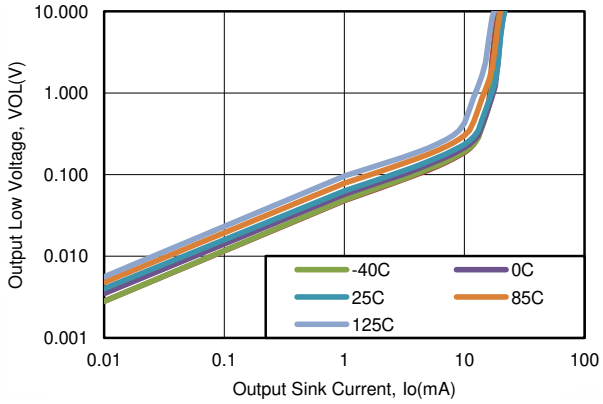


図 6-3. Output Low Voltage vs Output Current (I_{OL})

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

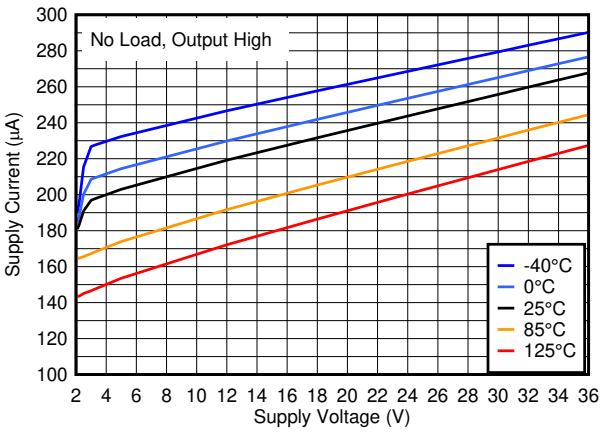


図 6-4. Supply Current vs. Supply Voltage

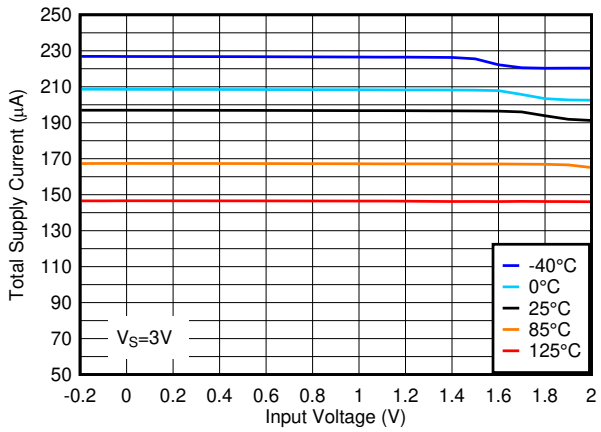


図 6-5. Total Supply Current vs. Input Voltage at 3V

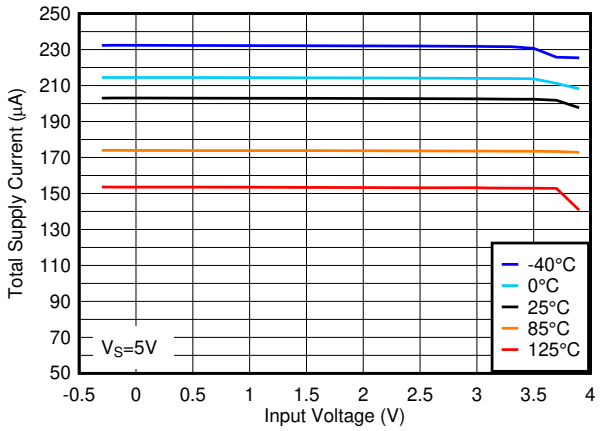


図 6-6. Total Supply Current vs. Input Voltage at 3.3V

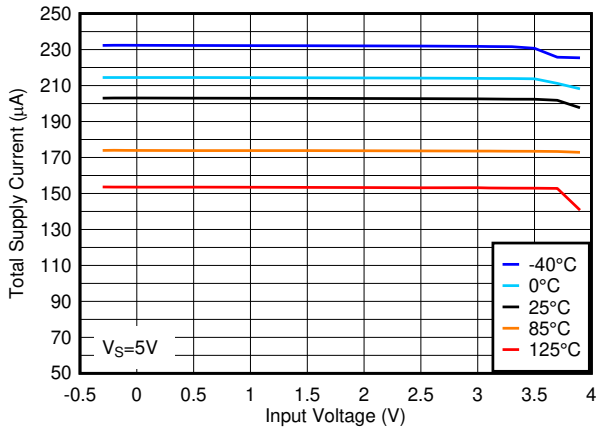


図 6-7. Total Supply Current vs. Input Voltage at 5V

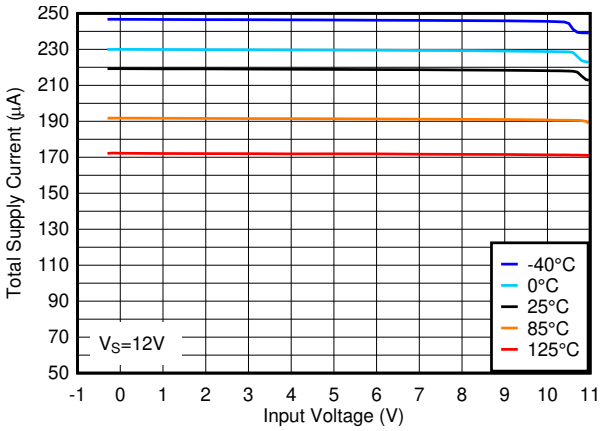


図 6-8. Total Supply Current vs. Input Voltage at 12V

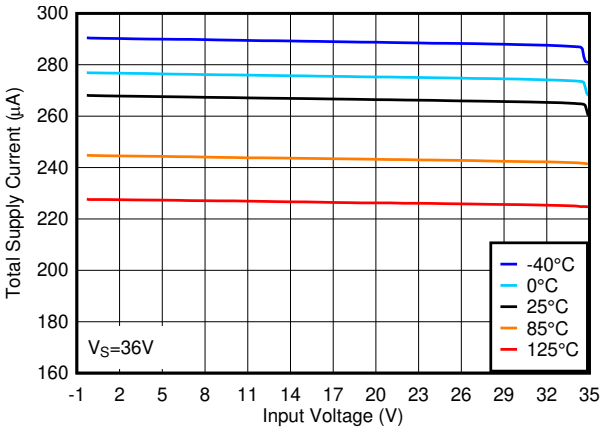


図 6-9. Total Supply Current vs. Input Voltage at 36V

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

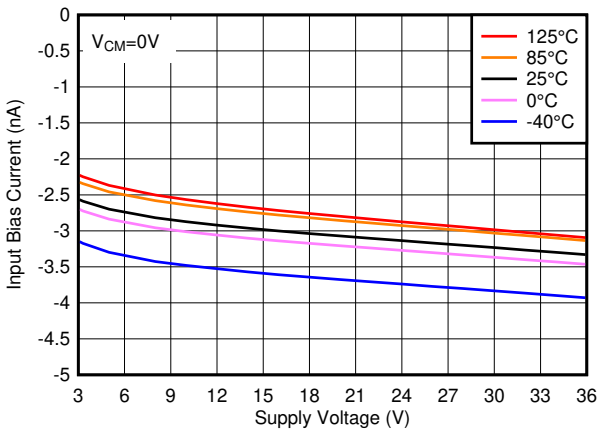


図 6-10. Input Bias Current vs. Supply Voltage

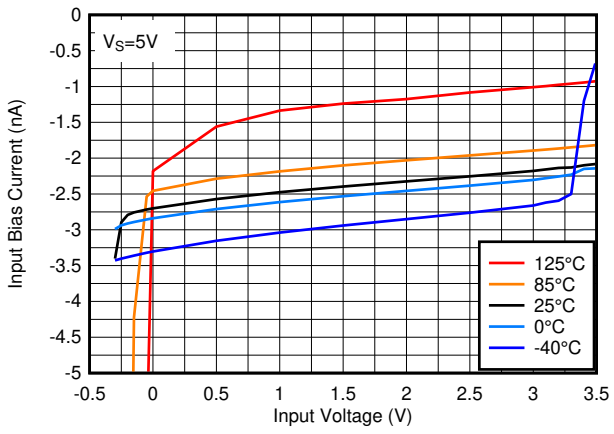


図 6-11. Input Bias Current vs. Input Voltage at 5V

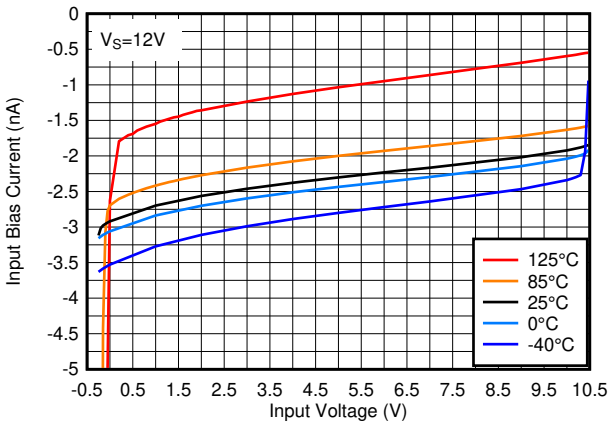


図 6-12. Input Bias Current vs. Input Voltage at 12V

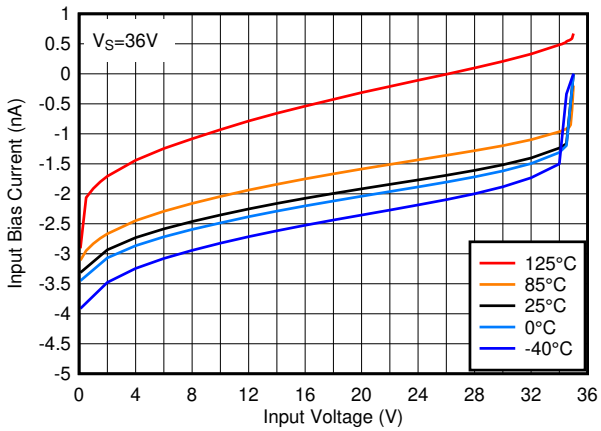


図 6-13. Input Bias Current vs. Input Voltage at 36V

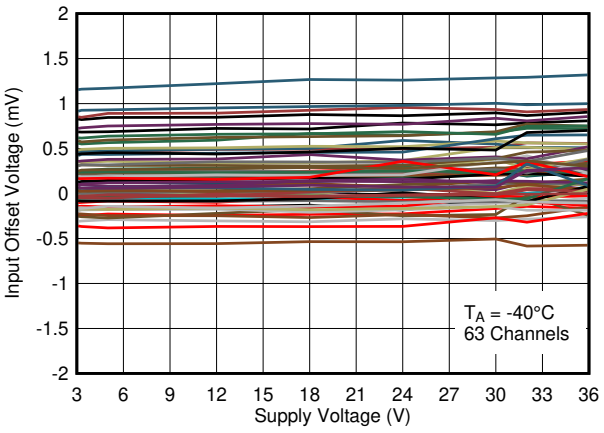


図 6-14. Input Offset Voltage vs. Supply Voltage at -40°C

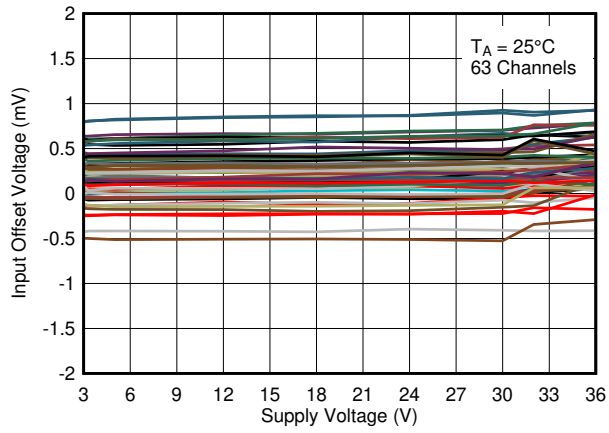


図 6-15. Input Offset Voltage vs. Supply Voltage at 25°C

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

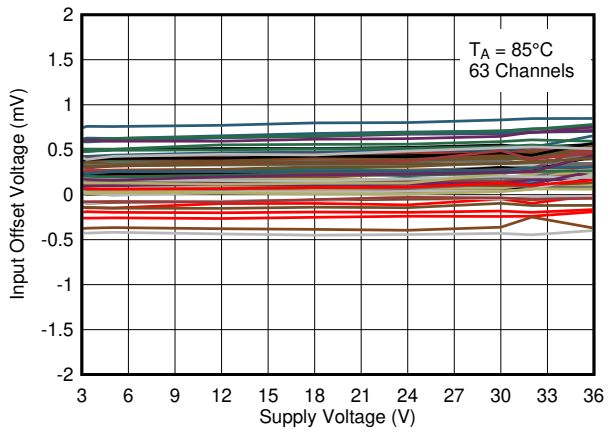


図 6-16. Input Offset Voltage vs. Supply Voltage at 85°C

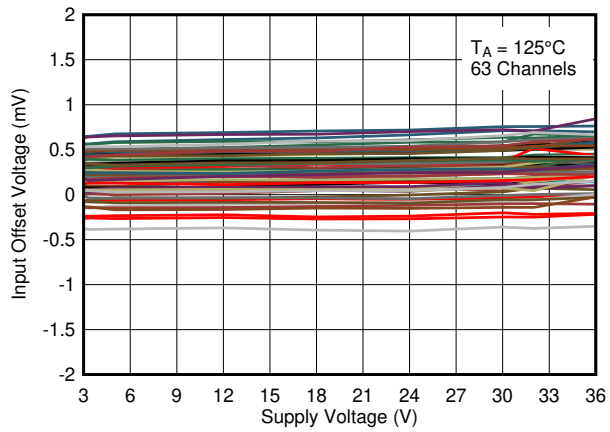


図 6-17. Input Offset Voltage vs. Supply Voltage at 125°C

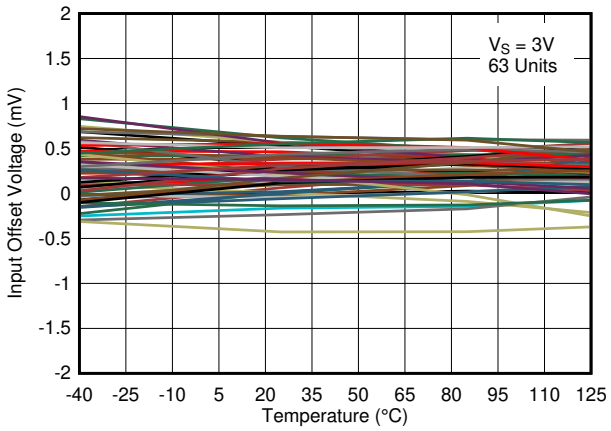


図 6-18. Input Offset Voltage vs. Temperature at 3V

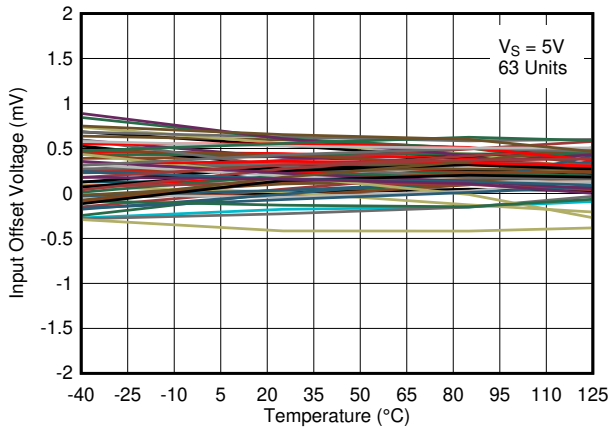


図 6-19. Input Offset Voltage vs. Temperature at 5V

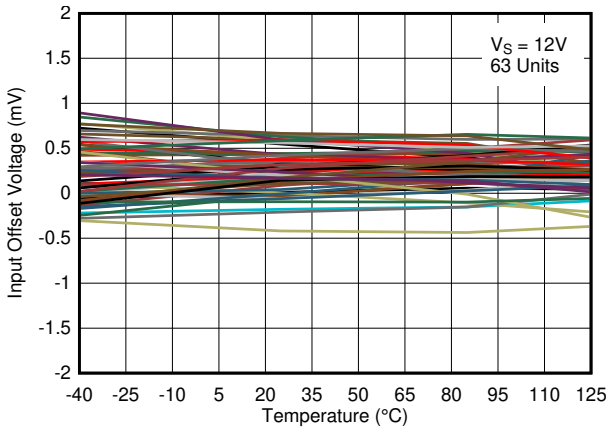


図 6-20. Input Offset Voltage vs. Temperature at 12V

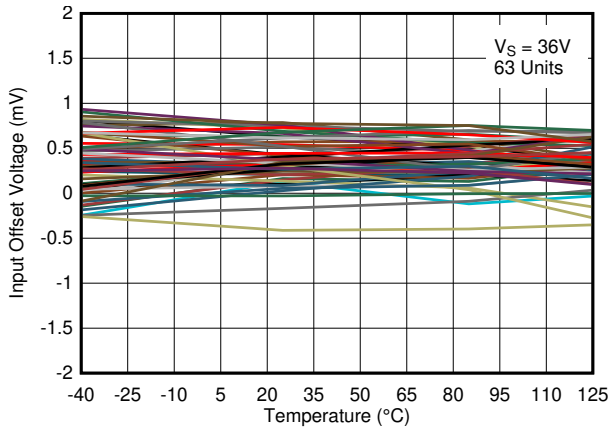


図 6-21. Input Offset Voltage vs. Temperature at 36V

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

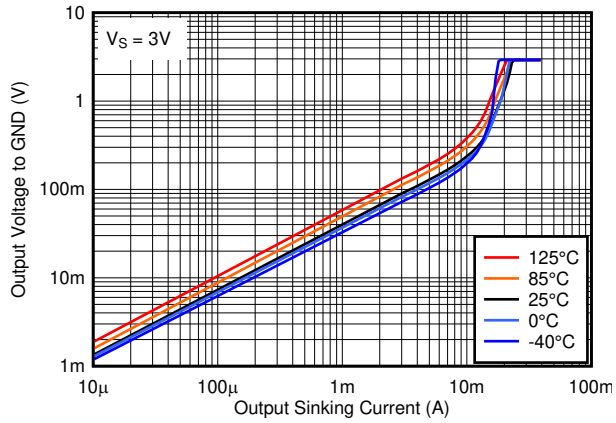


図 6-22. Output Low Voltage vs. Output Sinking Current at 3V

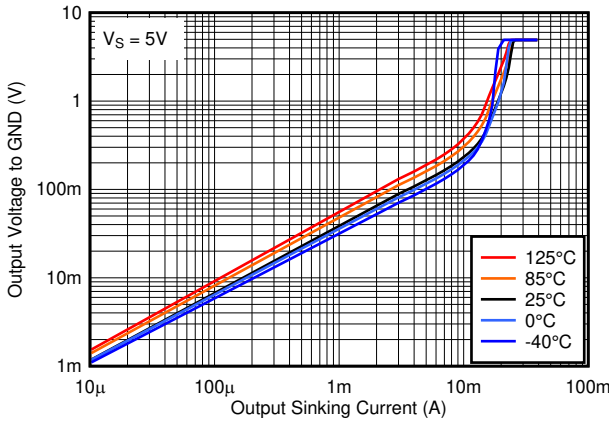


図 6-23. Output Low Voltage vs. Output Sinking Current at 5V

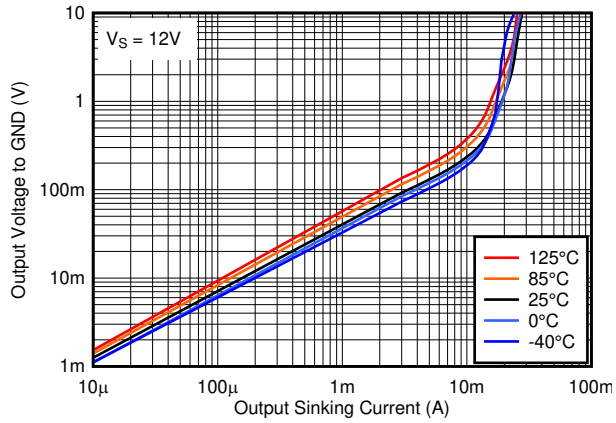


図 6-24. Output Low Voltage vs. Output Sinking Current at 12V

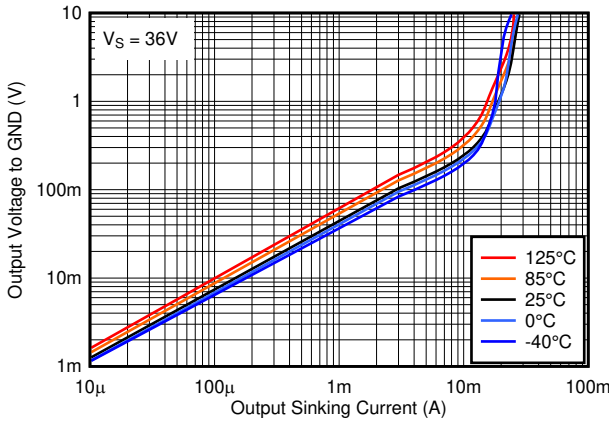


図 6-25. Output Low Voltage vs.Output Sinking Current at 36V

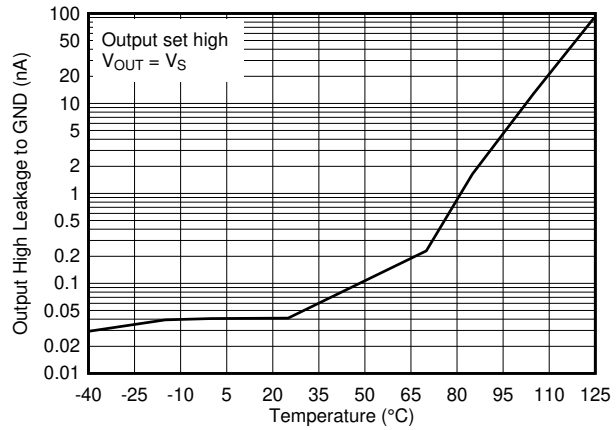


図 6-26. Output High Leakage Current vs.Temperature at 5V

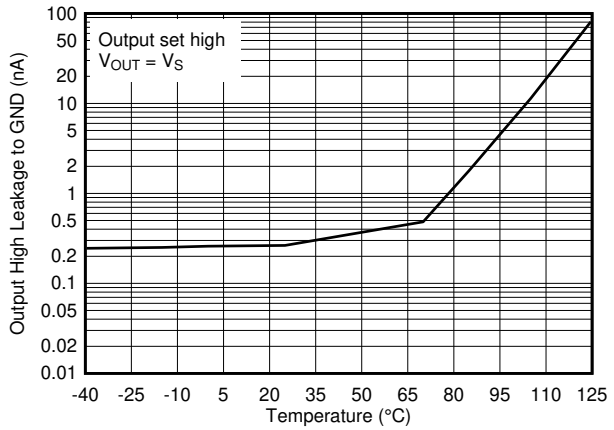


図 6-27. Output High Leakage Current vs. Temperature at 36V

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

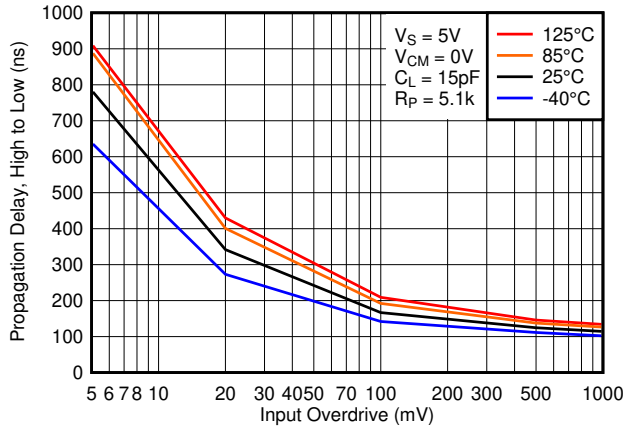


図 6-28. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

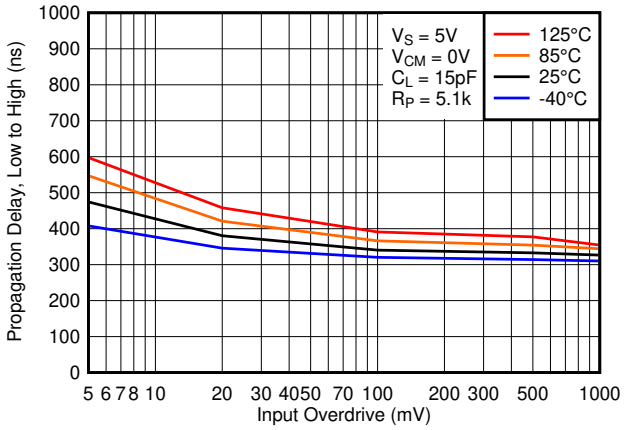


図 6-29. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

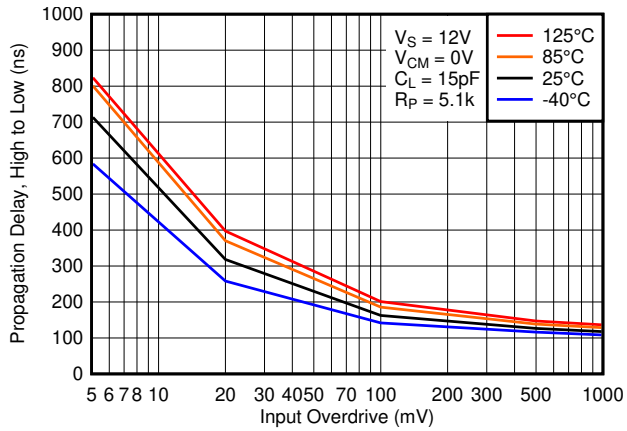


図 6-30. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V

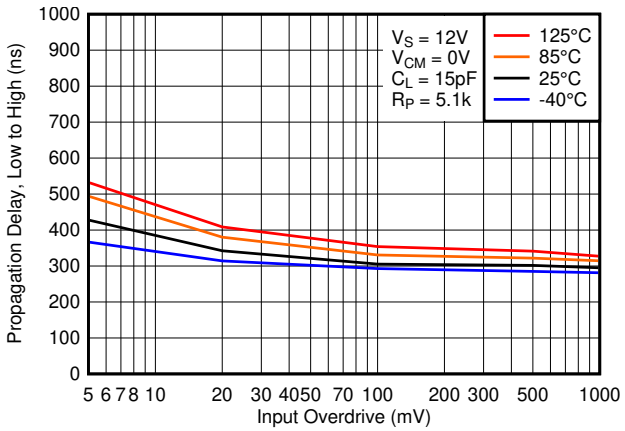


図 6-31. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V

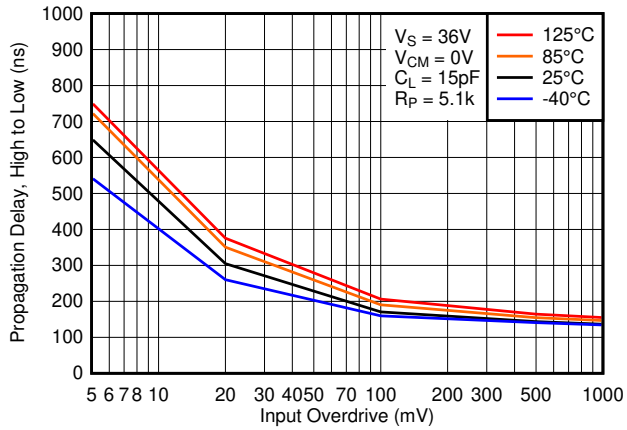


図 6-32. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V

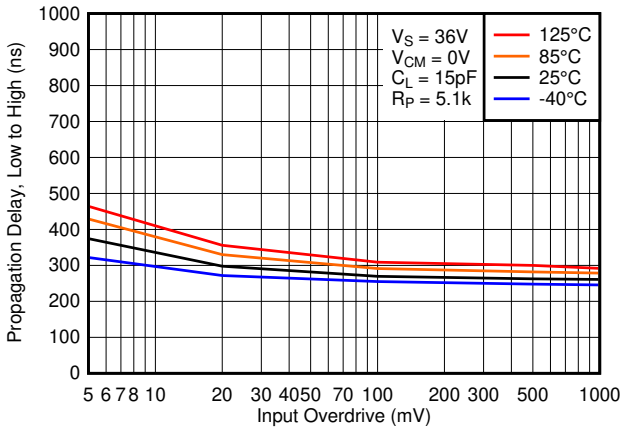


図 6-33. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

6.12 Typical Characteristics, TL331B-Q1 and TL391B-Q1 (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

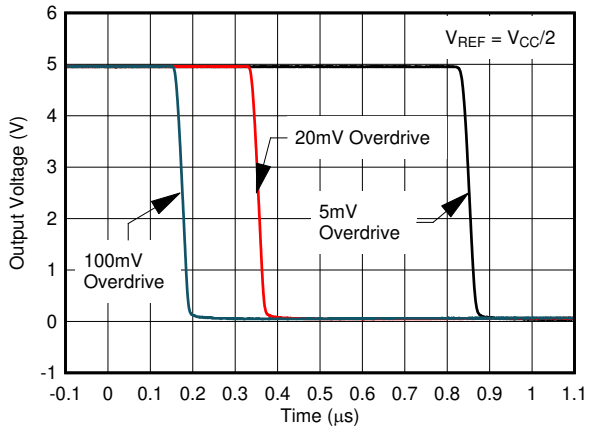


図 6-34. Response Time for Various Overdrives, High-to-Low Transition

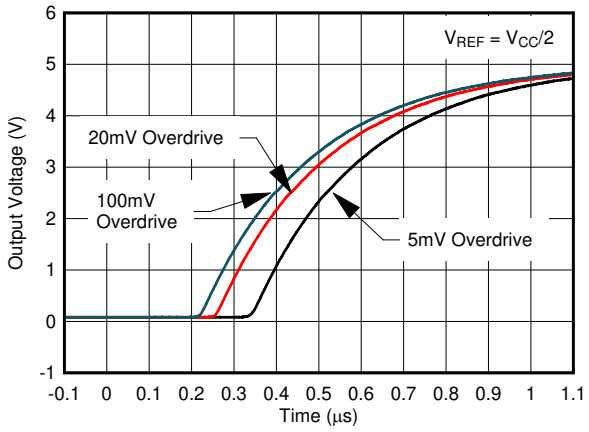


図 6-35. Response Time for Various Overdrives, Low-to-High Transition

7 Detailed Description

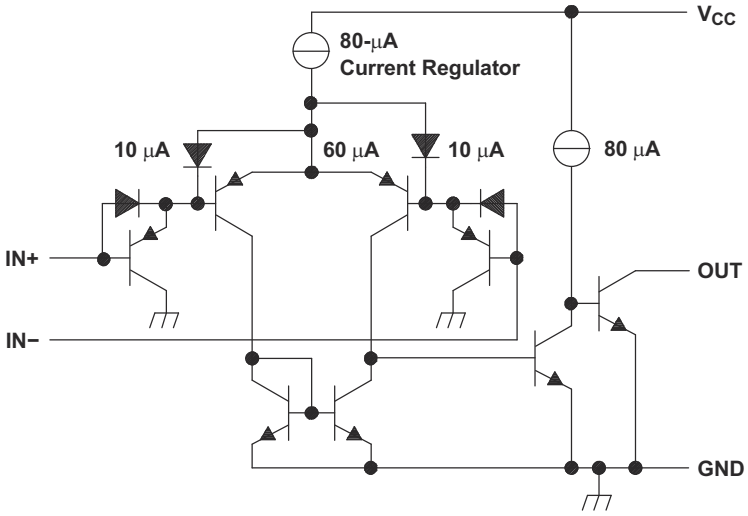
7.1 Overview

The TL331-Q1 is a single comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its very wide supply voltages range (2 V to 36 V), low Iq, and fast response.

The open-collector output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

The TL331B-Q1 and TL391B-Q1 are performance upgrades to industry standard TL331-Q1 using the latest semiconductor process technologies that allows for lower offset voltages, lower input bias and supply currents and faster response times. The TL331B can drop-in replace the "I" or "Q" versions of TL331-Q1. The TL391B-Q1 is an alternate pinout of the TL331B-Q1 for replacing competitive devices.

7.2 Functional Block Diagram



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	1
Transistors	20

Current values shown are nominal.

7.3 Feature Description

The TL331-Q1 consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing TL331-Q1 to accurately function from ground to V_{CC} – 1.5 V differential input.

The output consists of an open collector NPN (pull-down or low side) transistor. The output NPN will sink current when the negative input voltage is higher than the positive input voltage and the offset voltage. The VOL is resistive and will scale with the output current. Please see 図 6-3 for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The TL331-Q1 operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

TL331-Q1 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes TL331-Q1 optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

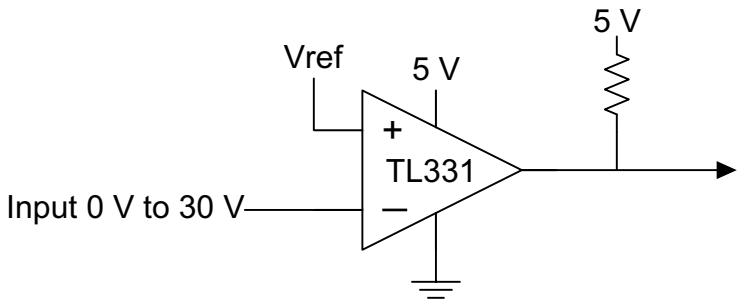


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to V_{CC} – 1.5 V
Supply Voltage	2 V to 36 V
Logic Supply Voltage (R_{PULLUP} Voltage)	2 V to 36 V
Output Current (V_{LOGIC}/R_{PULLUP})	1 µA to 4 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using TL331-Q1 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to V_{CC} – 1.5 V. This limits

the input voltage range to as high as V_{CC} – 1.5 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, see Section 2 of Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions.

8.2.2.2 TL331B-Q1 and TL391B-Q1 ESD Protection

The "B" versions add dedicated ESD protections on all the pins for improved ESD performance as well as improved negative input voltage handling. Please see Application Note SNOAA35 for more information.

8.2.2.3 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). In order to make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 図 8-2 and 図 8-3 show positive and negative response times with respect to overdrive voltage.

8.2.2.4 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use 図 6-3 to determine V_{OL} based on the output current.

The output current can also effect the transient response. More is explained in the next section.

8.2.2.5 Response Time

Response time is a function of input over drive. See *セクション 8.2.3* for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}), and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F \sim R_{CE} \times C_L$
  – R_{CE} can be determined by taking the slope of 図 6-3 in its linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1 kΩ, and 50 pF scope probe.

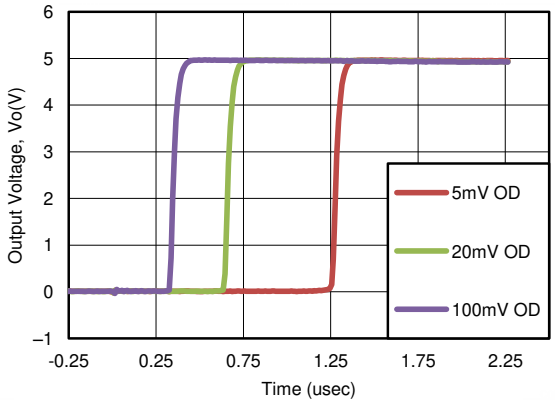


図 8-2. Response Time for Various Overdrives (Positive Transition)

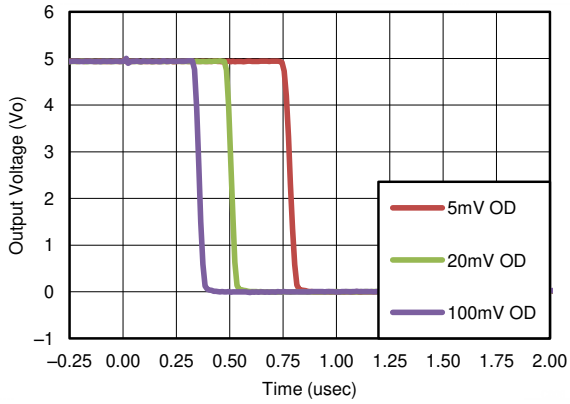


図 8-3. Response Time for Various Overdrives (Negative Transition)

8.3 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

8.4 Layout

8.4.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

8.4.2 Layout Example

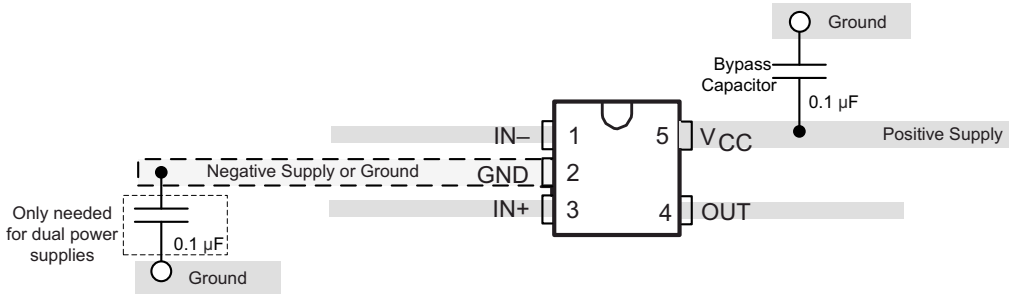


図 8-4. TL331-Q1 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

Application Design Guidelines for LM339, LM393, TL331 Family Comparators - SNOAA35

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design- TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design- TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

Zero crossing detection using comparator circuit - SNOA999

A Quad of Independently Functioning Comparators - SNOA654

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL331BQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31BQ	Samples
TL331EDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	3ISF	Samples
TL331IDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TQ1U	Samples
TL331QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1RU	Samples
TL391BQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	91BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL331-Q1, TL331B-Q1, TL391B-Q1 :

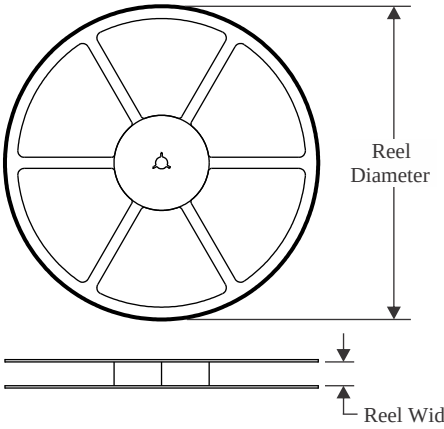
- Catalog : TL331, TL331B, TL391B
- Enhanced Product : TL331-EP

NOTE: Qualified Version Definitions:

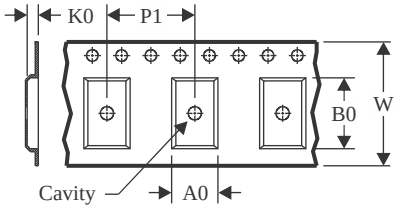
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

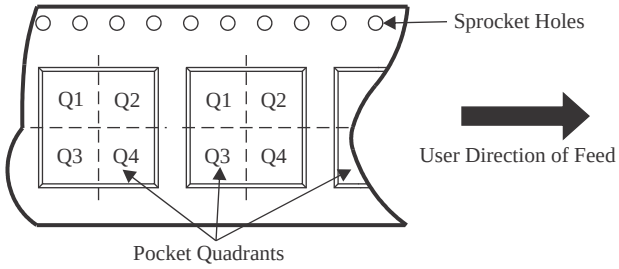


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

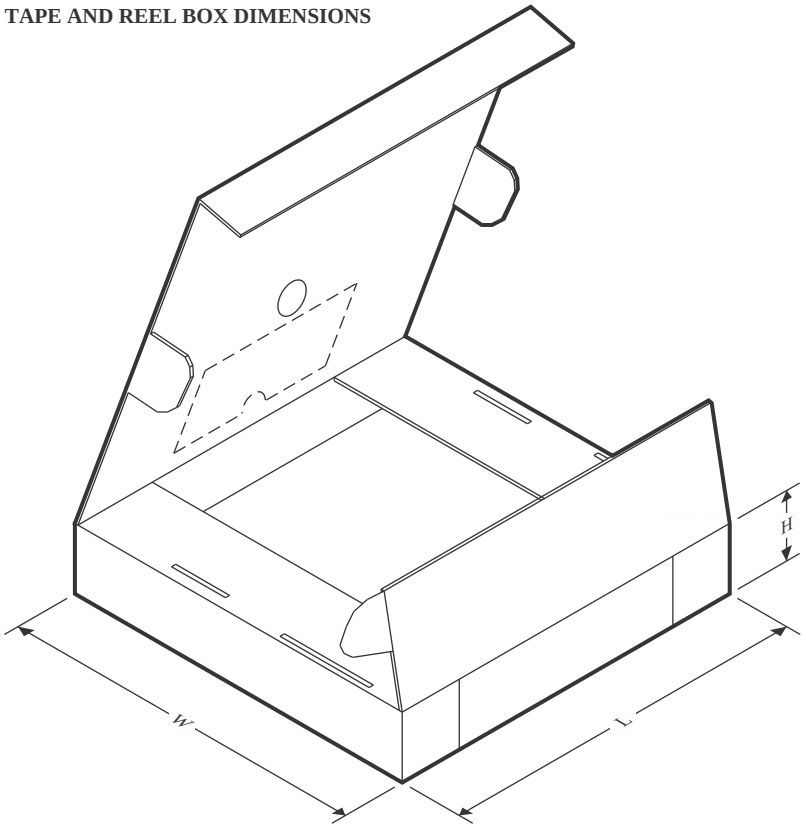
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL331BQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331EDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331IDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331IDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL331QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL391BQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL391BQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

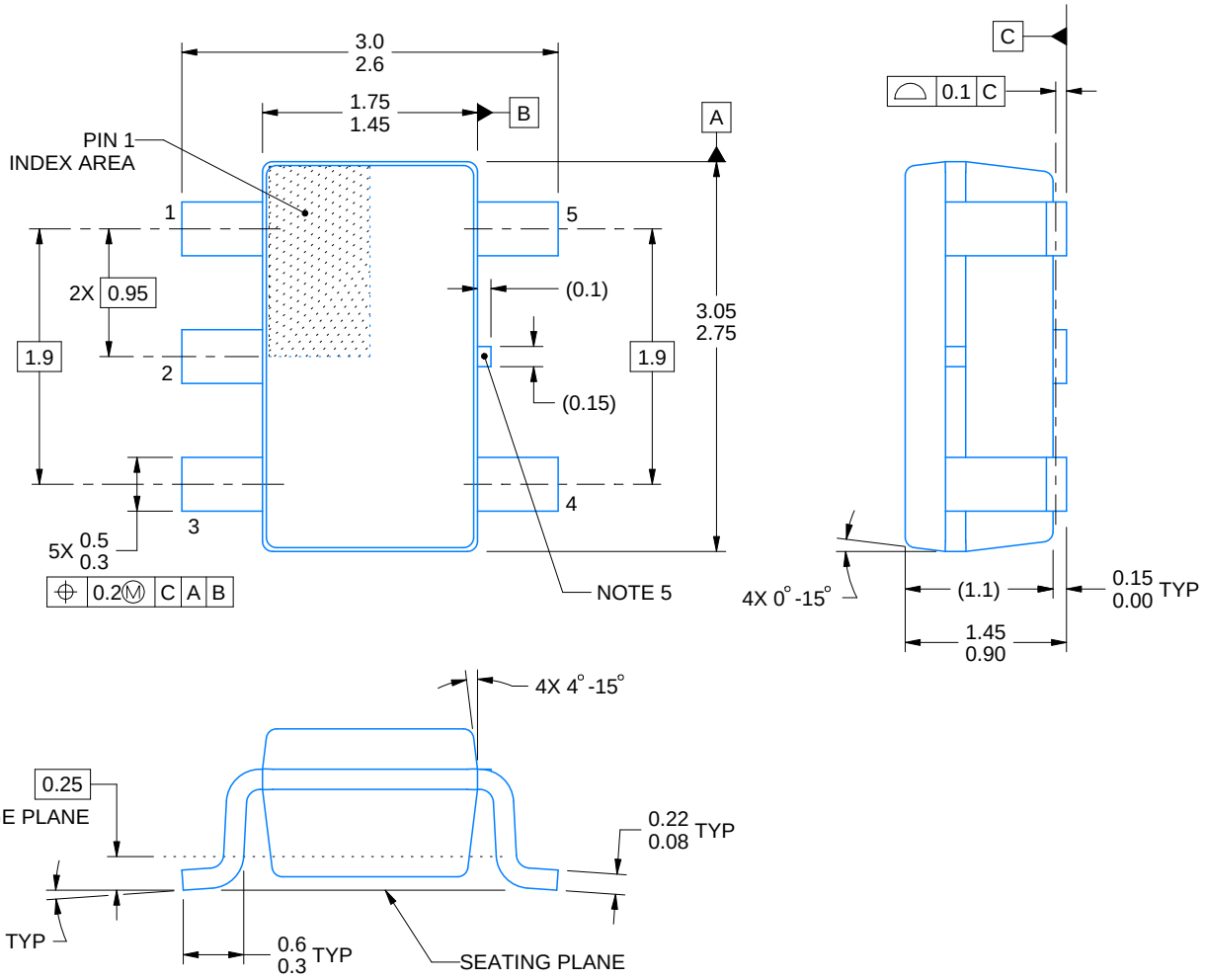
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL331BQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331EDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331IDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TL331IDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL331QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TL331QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL391BQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL391BQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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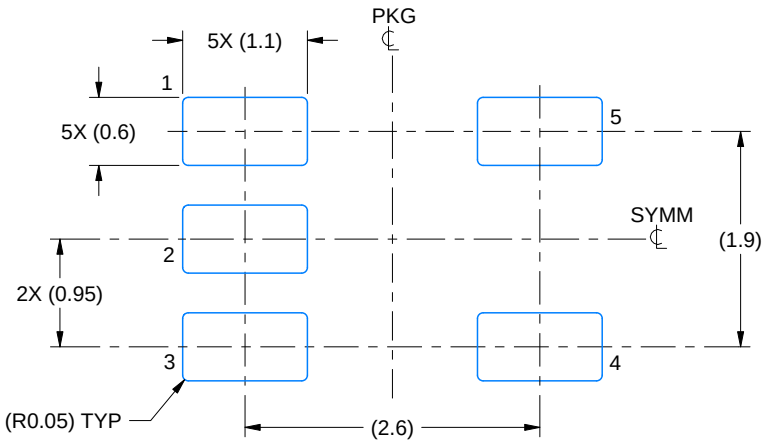
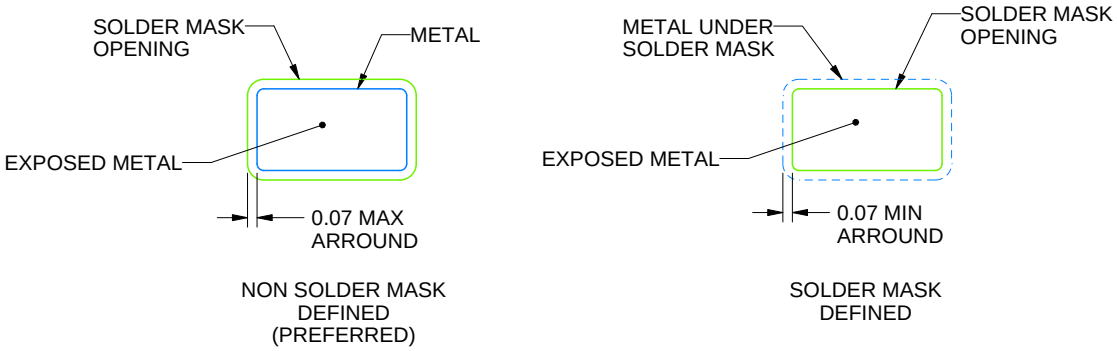
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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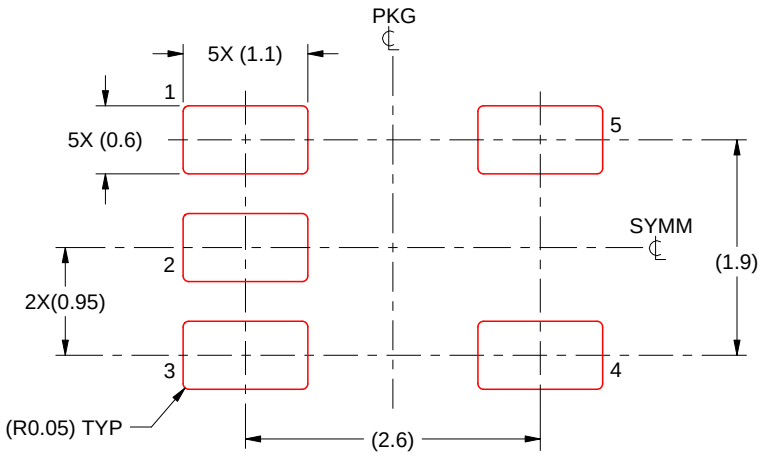
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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