

TLx84xB 高性能電流モード PWM コントローラ

1 特長

- 低いスタートアップ電流 (0.5mA 未満)
- トリムされた発振器放電電流
- 最大 500kHz の電流モード動作
- 自動フィードフォワード補償
- ラッチ PWM によるサイクルごとの電流制限
- 内部トリムされたリファレンス電圧、低電圧誤動作防止付き
- ヒステリシス付きの大電流トータムポール出力低電圧誤動作防止
- ダブルパルス抑制

2 アプリケーション

- あらゆる極性のスイッチングレギュレータ
- トランス結合型 DC/DC コンバータ

3 概要

TL284xB および TL384xB シリーズの制御 IC には、オフラインまたは DC-DC 固定周波数の電流モード制御方式を最小限の外付け部品で実装するために必要な機能が搭載されています。低電圧誤動作防止 (UVLO) および高精度リファレンス電圧を内蔵し、エラーアンプ入力における精度を向上するようにトリムされています。それ以外にも、ラッチ動作を保証するロジック、パルス幅変調 (PWM) コンパレータ (電流制限制御の機能も兼ねています)、大きなピーク電流をソースまたはシンクするように設計されたトータムポール出力段が内蔵されています。出力段は N チャネル MOSFET の駆動に適しており、オフ状態では Low になります。

TL284xB および TL384xB シリーズは、標準の TL284x および TL384x とピン互換であり、以下の点が改善されています。スタートアップ電流は 0.5mA (最大値) に規定され、発振器放電電流は 8.3mA (標準値) にトリムされています。また、低電圧誤動作防止状態では、10mA をシンクしているときの出力の飽和電圧は 1.2V です ($V_{CC} = 5V$)。

これらのシリーズに属する製品間の主な違いは、UVLO スレッシュホールドおよび最大デューティサイクル範囲です。UVLO スレッシュホールドの標準値は、TLx842B および TLx844B デバイスでは 16V (オン) と 10V (オフ) であり、オフラインのアプリケーションに理想的です。TLx843B および TLx845B デバイスについては、対応するスレッシュホールドの標準値は、8.4V (オン) と 7.6V (オフ) です。TLx842B および TLx843B デバイスは、100% に近いデューティサイクルで動作可能です。TLx844B および TLx845B には、内部にトグルフリップフロップが追加されているため、

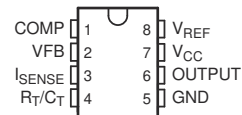
デューティサイクルの範囲は 0%~50% となります。この結果、2 クロックサイクルごとに出力がオフになります。TL284xB シリーズのデバイスは -40°C~85°C、TL384xB シリーズのデバイスは 0°C~70°C での動作が規定されています。

パッケージ情報

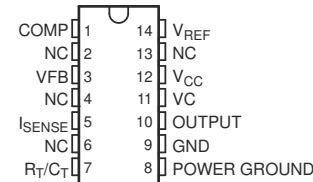
部品番号	パッケージ(1)	パッケージサイズ(2)
TLx84x	D (SOIC, 8)	4.90mm × 6.00mm
	D (SOIC, 14)	8.65mm × 6.00mm
	P (PDIP, 8)	9.81mm × 9.43mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

D (SOIC) OR P (PDIP) PACKAGE
(TOP VIEW)



D (SOIC) PACKAGE
(TOP VIEW)



NC – No internal connection

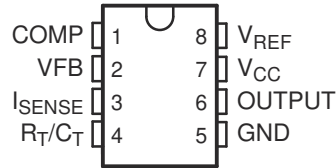


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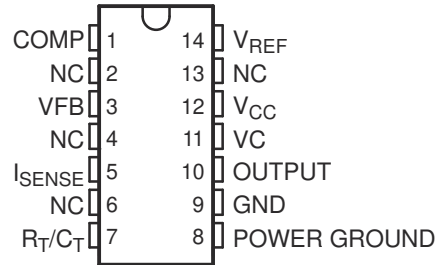
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4 Pin Configuration and Functions

**D (SOIC) OR P (PDIP) PACKAGE
(TOP VIEW)**



**D (SOIC) PACKAGE
(TOP VIEW)**



NC – No internal connection

PIN			Type ⁽¹⁾	DESCRIPTION
NAME	D (14 pins)	D or P (8 pins)		
COMP	1	1	I/O	Error amplifier compensation pin
GND	9	5	-	Device power supply ground terminal
ISENSE	5	3	I	Current sense comparator input
NC	2, 4, 6, 13	-	-	Do not connect
OUTPUT	10	6	O	PWM Output
POWER GROUND	8	-	-	Output PWM ground terminal
REF	14	8	O	Oscillator voltage reference
RT/CT	7	4	I/O	Oscillator RC input
VC	11	-	-	Output PWM positive voltage supply
VCC	12	7	-	Device positive voltage supply
VFB	3	2	I	Error amplifier input

(1) I = Input; O = Output; I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Low impedance source	30	V	
		I _{CC} < 30 mA	Self limiting		
V _I	Analog input voltage range	VFB and I _{SENSE}	-0.3	6.3	V
I _{CC}	Supply current		30	mA	
I _O	Output current		±1	A	
I _{O(sink)}	Error amplifier output sink current		10	mA	
	Output energy	Capacitive load	5	μJ	
T _J	Virtual junction temperature		150	°C	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to the device GND terminal.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	V _{CC}		30	V
		VC ⁽¹⁾		30	
V _I	Input voltage	R _T /C _T	0	5.5	V
		VFB and I _{SENSE}	0	5.5	
V _O	Output voltage	OUTPUT	0	30	V
		POWER GROUND ⁽¹⁾	-0.1	1	
I _{CC}	Supply current, externally limited			25	mA
I _O	Average output current			200	mA
I _{O(ref)}	Reference output current			-20	mA
f _{osc}	Oscillator frequency		100	500	kHz
T _J	Operating free-air temperature	TL284xB	-40	85	°C
		TL384xB	0	70	

- (1) The recommended voltages for VC and POWER GROUND apply only to the 14-pin D package.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TLx84xB			UNIT
	D	P	D	
	8 PINS	8 PINS	14 PINS	
R _{θJA} Junction-to-ambient thermal resistance	117.4	74.1	87.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Reference Section Electrical Characteristics

V_{CC} = 15 V⁽¹⁾, R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP ⁽²⁾	MAX	MIN	TYP ⁽²⁾	MAX	
Output voltage	I _O = 1 mA, T _J = 25°C	4.95	5	5.05	4.9	5	5.1	V
Line regulation	V _{CC} = 12 V to 25 V		6	20		6	20	mV
Load regulation	I _O = 1 mA to 20 mA		6	25		6	25	mV
Average temperature coefficient of output voltage			0.2	0.4		0.2	0.4	mV/°C
Output voltage, worst-case variation	V _{CC} = 12 V to 25 V, I _O = 1 mA to 20 mA	4.9		5.1	4.82		5.18	V
Output noise voltage	f = 10 Hz to 10 kHz, T _J = 25°C		50			50		μV
Output-voltage long-term drift	After 1000 h at T _J = 25°C		5	25		5	25	mV
Short-circuit output current		-30	-100	-180	-30	-100	-180	mA

(1) Adjust V_{CC} above the start threshold before setting V_{CC} to 15 V.

(2) All typical values are at T_J = 25°C.

5.6 Oscillator Section Electrical Characteristics

V_{CC} = 15 V⁽¹⁾, R_T = 10 kΩ, C_T = 3.3 nF, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP ⁽²⁾	MAX	MIN	TYP ⁽²⁾	MAX	
Initial accuracy	T _J = 25°C	47	52	57	47	52	57	kHz
	T _A = T _{low} to T _{high}			60			60	
	T _J = 25°C, R _T = 6.2 kΩ, C _T = 1 nF	225	250	275	225	250	275	
Voltage stability	V _{CC} = 12 V to 25 V		0.2	1		0.2	1	%
Temperature stability			5			5		%
Amplitude	Peak to peak		1.7			1.7		V
Discharge current	T _J = 25°C, R _T /C _T = 2 V	7.8	8.3	8.8	7.8	8.3	8.8	mA
	R _T /C _T = 2 V		7.5	8.8		7.6	8.8	

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.

(2) All typical values are at T_J = 25°C.

(3) Output frequency equals oscillator frequency for the TL3842B and TL3843B. Output frequency is one-half the oscillator frequency for the TL3844B and TL3845B.

5.7 Error-Amplifier Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(1)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP ⁽²⁾	MAX	MIN	TYP ⁽²⁾	MAX	
Feedback input voltage	COMP = 2.5 V	2.45	2.5	2.55	2.42	2.5	2.58	V
Input bias current			-0.3	-1		-0.3	-2	μA
Open-loop voltage amplification	$V_O = 2\text{ V to }4\text{ V}$	65	90		65	90		dB
Gain-bandwidth product		0.7	1		0.7	1		MHz
Supply-voltage rejection ratio	$V_{CC} = 12\text{ V to }25\text{ V}$	60	70		60	70		dB
Output sink current	VFB = 2.7 V, COMP = 1.1 V	2	6		2	6		mA
Output source current	VFB = 2.3 V, COMP = 5 V	-0.5	-0.8		-0.5	-0.8		mA
High-level output voltage	VFB = 2.3 V, $R_L = 15\text{ k}\Omega$ to GND	5	6		5	6		V
Low-level output voltage	VFB = 2.7 V, $R_L = 15\text{ k}\Omega$ to GND		0.7	1.1		0.7	1.1	V

(1) Adjust V_{CC} above the start threshold before setting it to 15 V.

(2) All typical values are at $T_J = 25^\circ\text{C}$.

5.8 Current-Sense Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(4)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
Voltage amplification ^{(2) (3)}		2.85	3	3.15	2.85	3	3.15	V/V
Current-sense comparator threshold ⁽²⁾	COMP = 5 V	0.9	1	1.1	0.9	1	1.1	V
Supply-voltage rejection ratio ⁽²⁾	$V_{CC} = 12\text{ V to }25\text{ V}$		70			70		dB
Input bias current			-2	-10		-2	-10	μA
Delay time to output	VFB = 0 V to 2 V		150	300		150	300	ns

(1) All typical values are at $T_J = 25^\circ\text{C}$.

(2) Measured at the trip point of the latch, with VFB at 0 V.

(3) Measured between I_{SENSE} and COMP, with the input changing from 0 V to 0.8 V.

(4) Adjust V_{CC} above the start threshold before setting V_{CC} to 15 V.

5.9 Output Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(2)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
High-level output voltage	$I_{OH} = -20\text{ mA}$	13	13.5		13	13.5		V
	$I_{OH} = -200\text{ mA}$	12	13.5		12	13.5		
Low-level output voltage	$I_{OL} = 20\text{ mA}$		0.1	0.4		0.1	0.4	V
	$I_{OL} = 200\text{ mA}$		1.5	2.2		1.5	2.2	
Rise time	$C_L = 1\text{ nF}$, $T_J = 25^\circ\text{C}$		25	150		25	150	ns
Fall time	$C_L = 1\text{ nF}$, $T_J = 25^\circ\text{C}$		25	150		25	150	ns
UVLO saturation	$V_{CC} = 5\text{ V}$, $I_{OL} = 1\text{ mA}$		0.7	1.2		0.7	1.2	V

- (1) All typical values are at $T_J = 25^\circ\text{C}$.
(2) Adjust V_{CC} above the start threshold before setting V_{CC} to 15 V.

5.10 Undervoltage-Lockout Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(2)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
Start threshold voltage	TLx842B, TLx844B	15	16	17	14.5	16	17.5	V
	TLx843B, TLx845B	7.8	8.4	9	7.8	8.4	9	
Minimum operating voltage after start-up	TLx842B, TLx844B	9	10	11	8.5	10	11.5	V
	TLx843B, TLx845B	7	7.6	8.2	7	7.6	8.2	

- (1) All typical values are at $T_J = 25^\circ\text{C}$.
(2) Adjust V_{CC} above the start threshold before setting V_{CC} to 15 V.

5.11 Pulse-Width Modulator Section Electrical Characteristics

$V_{CC} = 15\text{ V}^{(2)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
Maximum duty cycle	TLx842B, TLx843B	92	96	100	92	96	100	%
	TLx844B, TLx845B	46	48	50	46	48	50	
Minimum duty cycle				0			0	%

- (1) All typical values are at $T_J = 25^\circ\text{C}$.
(2) Adjust V_{CC} above the start threshold before setting it to 15 V.

5.12 Supply Voltage Electrical Characteristics

$V_{CC} = 15\text{ V}^{(2)}$, $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	TL284xB			TL384xB			UNIT
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
Start-up current			0.3	0.5		0.3	0.5	mA
Operating supply current	VFB and I_{SENSE} at 0 V		11	17		11	17	mA
Limiting voltage	$I_{CC} = 25\text{ mA}$	30	39		30	39		V

- (1) All typical values are at $T_J = 25^\circ\text{C}$.
(2) Adjust V_{CC} above the start threshold before setting it to 15 V.

5.13 Typical Characteristics

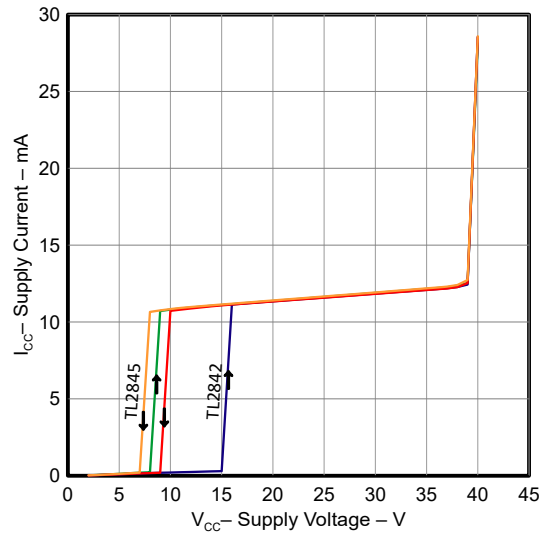


図 5-1. Supply Current vs Supply Voltage

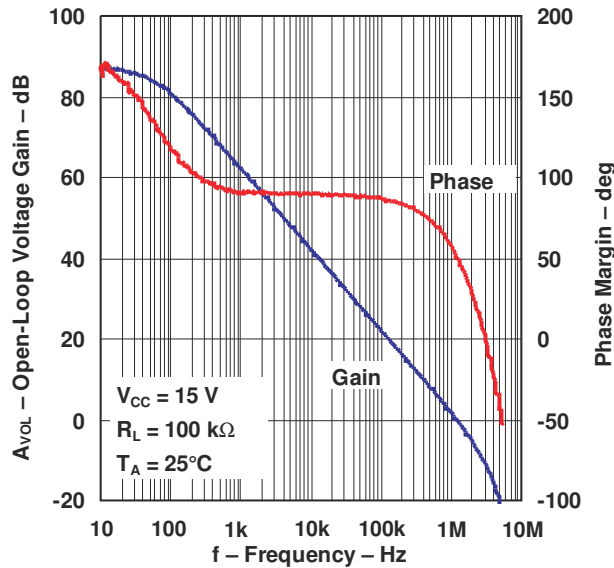


図 5-2. Error Amplifier Open-Loop Gain And Phase vs Frequency

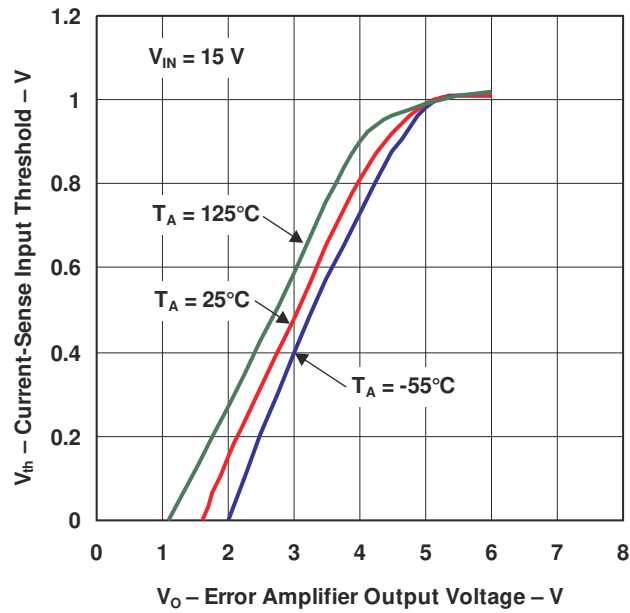


図 5-3. Current-Sense Input Threshold vs Error Amplifier Output Voltage

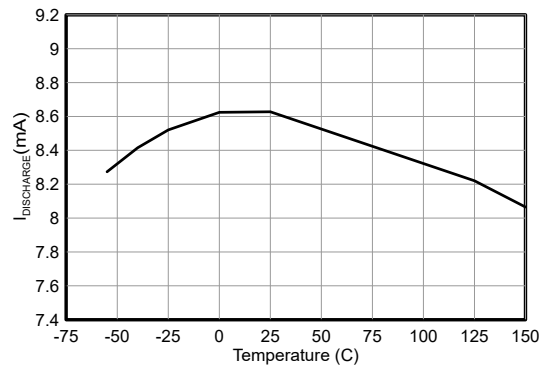


図 5-4. Oscillator Discharge Current vs Temperature

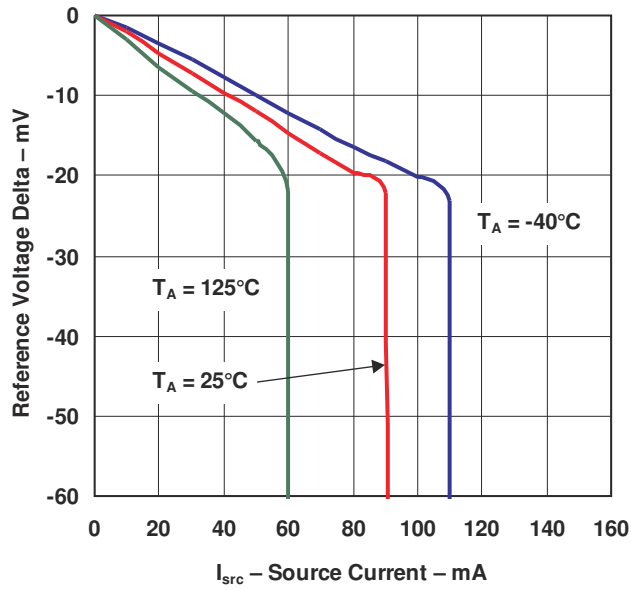


図 5-5. Reference Voltage vs Source Current

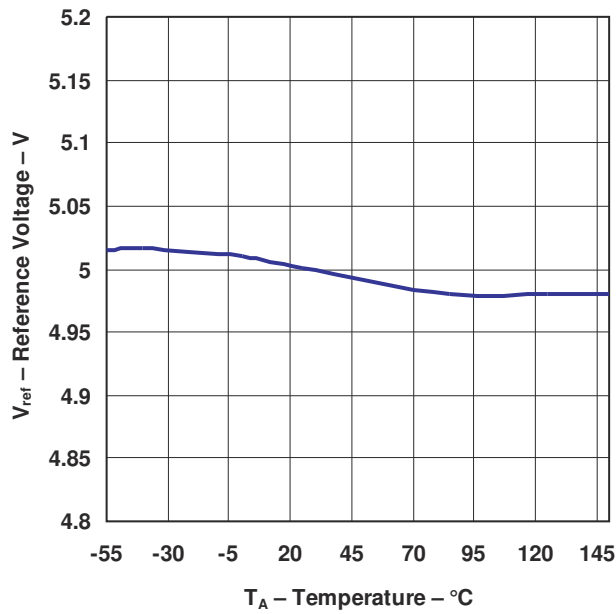
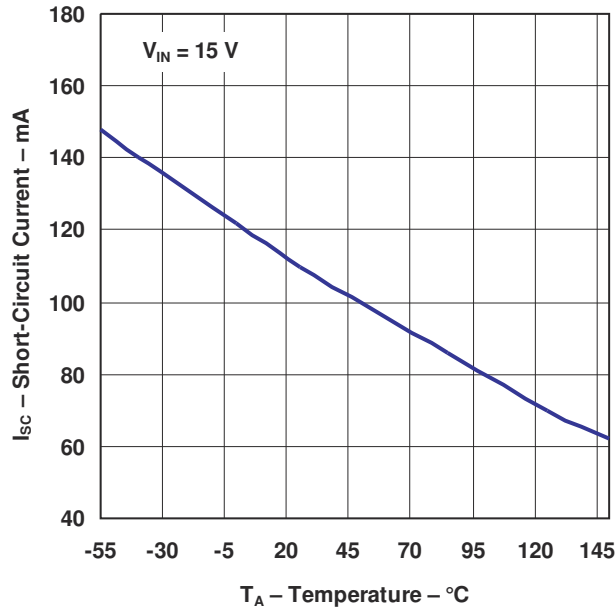
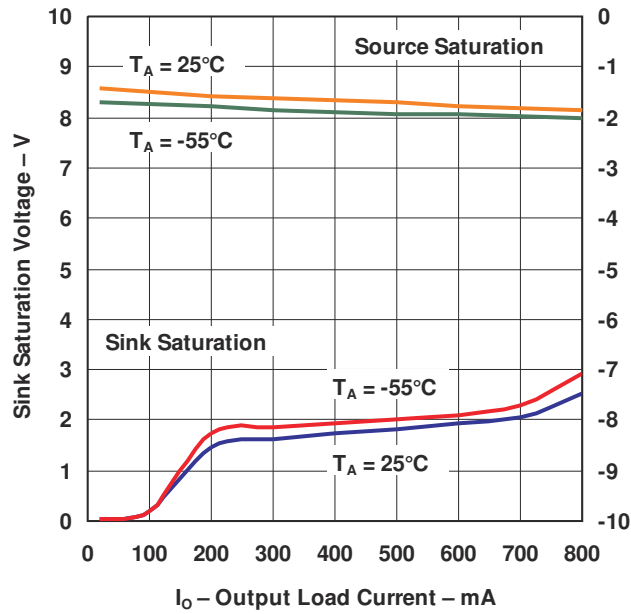


図 5-6. Reference Voltage vs Temperature




5-7. Reference Short-Circuit Current vs Temperature




5-8. Output Saturation Voltage vs Load Current

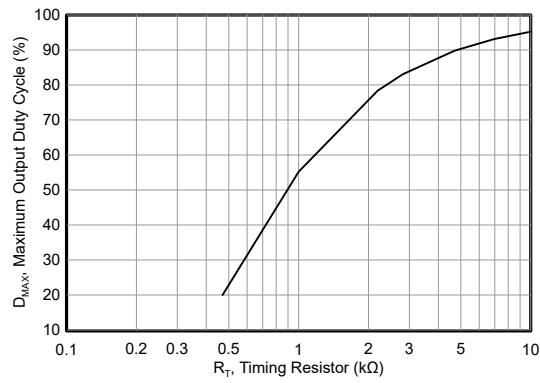
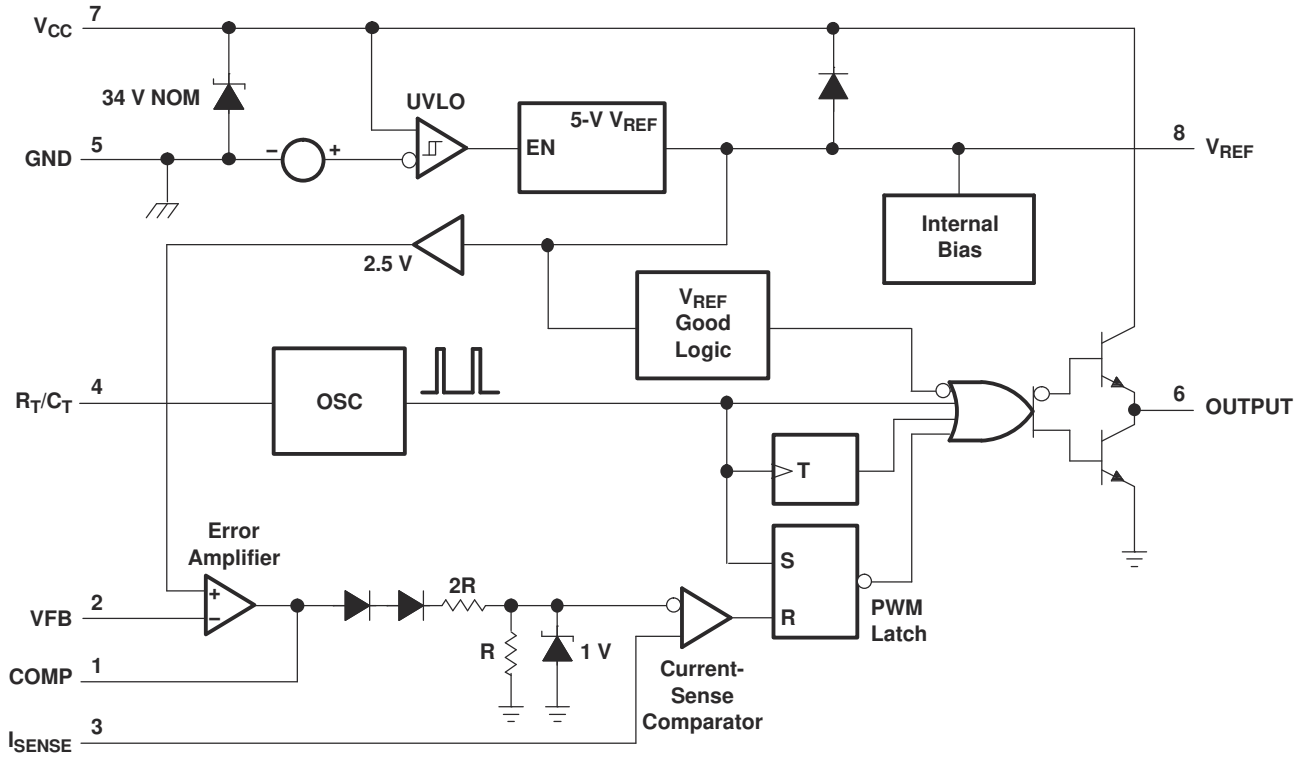


図 5-9. Maximum Output Duty Cycle vs Timing Resistor

6 Detailed Description

6.1 Functional Block Diagram



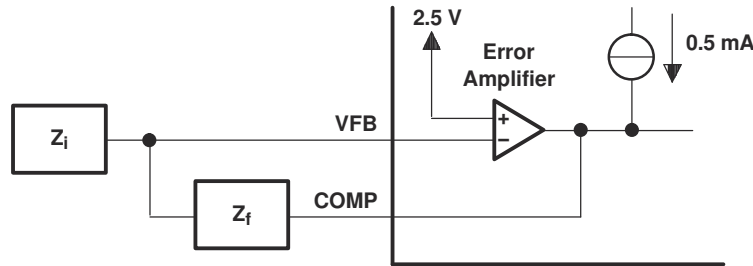
7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

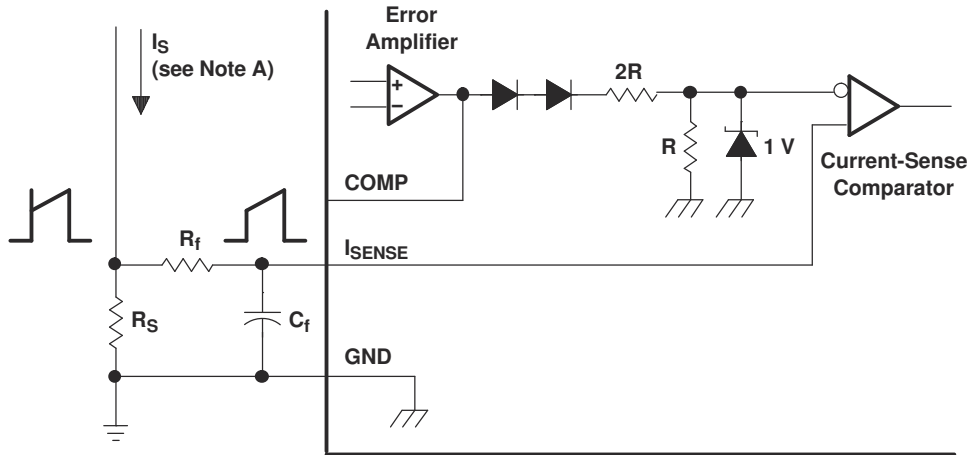
The error-amplifier configuration circuit is shown in [図 7-1](#).



A. Error amplifier can source or sink up to 0.5 mA.

図 7-1. Error-Amplifier Configuration

The current-sense circuit is shown in [図 7-2](#).



A. Peak current (I_S) is determined by the formula: $I_{S(max)} = 1 V/R_S$

B. A small RC filter formed by resistor R_f and capacitor C_f may be required to suppress switch transients.

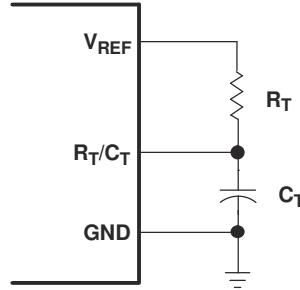
図 7-2. Current-Sense Circuit

The oscillator frequency is set using the circuit shown in [図 7-3](#). The frequency is calculated as:

$$f = 1 / R_T C_T$$

For $R_T > 5 \text{ k}\Omega$:

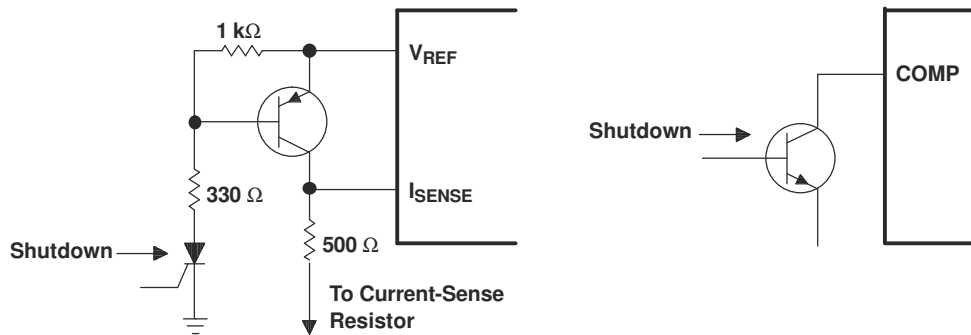
$$f \approx 1.72 / R_T C_T$$



7-3. Oscillator Section

7.2 Shutdown Technique

The PWM controller (see 7-4) can be shut down by two methods: either raise the voltage at I_{SENSE} above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or I_{SENSE} terminal is removed. In one example, an externally latched shutdown can be accomplished by adding an SCR that resets by cycling V_{CC} below the lower UVLO threshold. At this point, the reference turns off, allowing the SCR to reset.



7-4. Shutdown Techniques

A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% (see 7-5). Note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

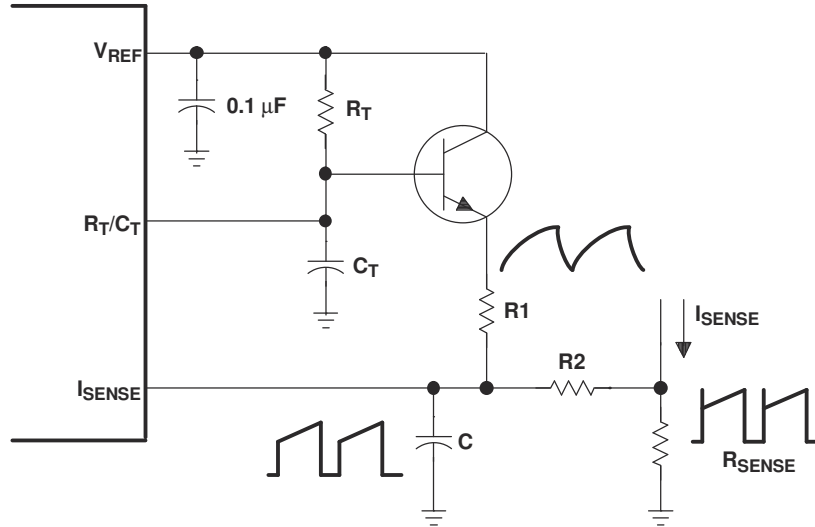


図 7-5. Slope Compensation

7.3 Open-Loop Laboratory Test Fixture

In the open-loop laboratory test fixture (see 図 7-6), high peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single-point ground. The transistor and 5-kΩ potentiometer sample the oscillator waveform and apply an adjustable ramp to the I_{SENSE} terminal.

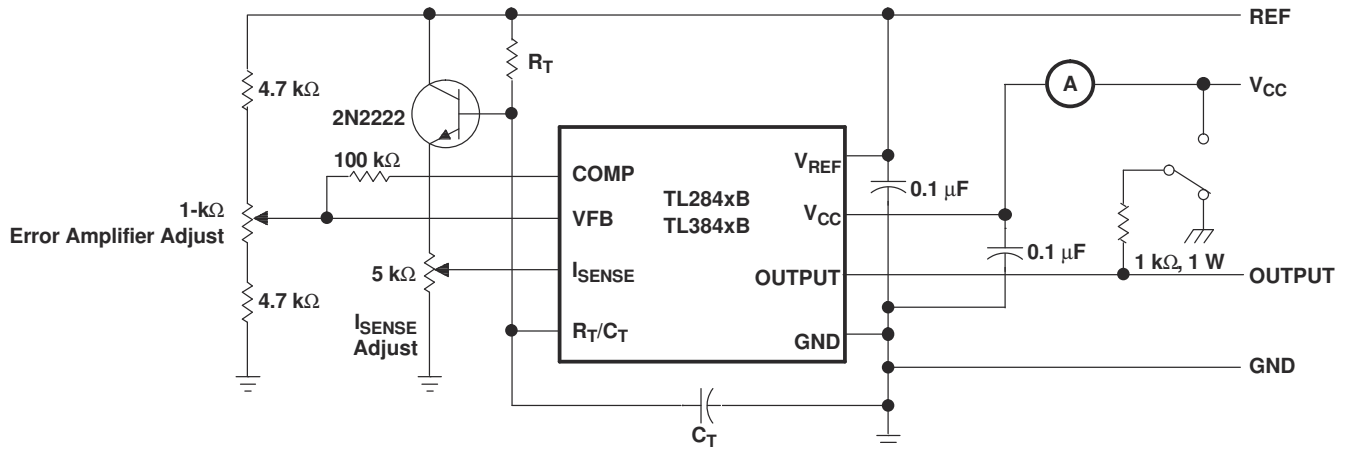
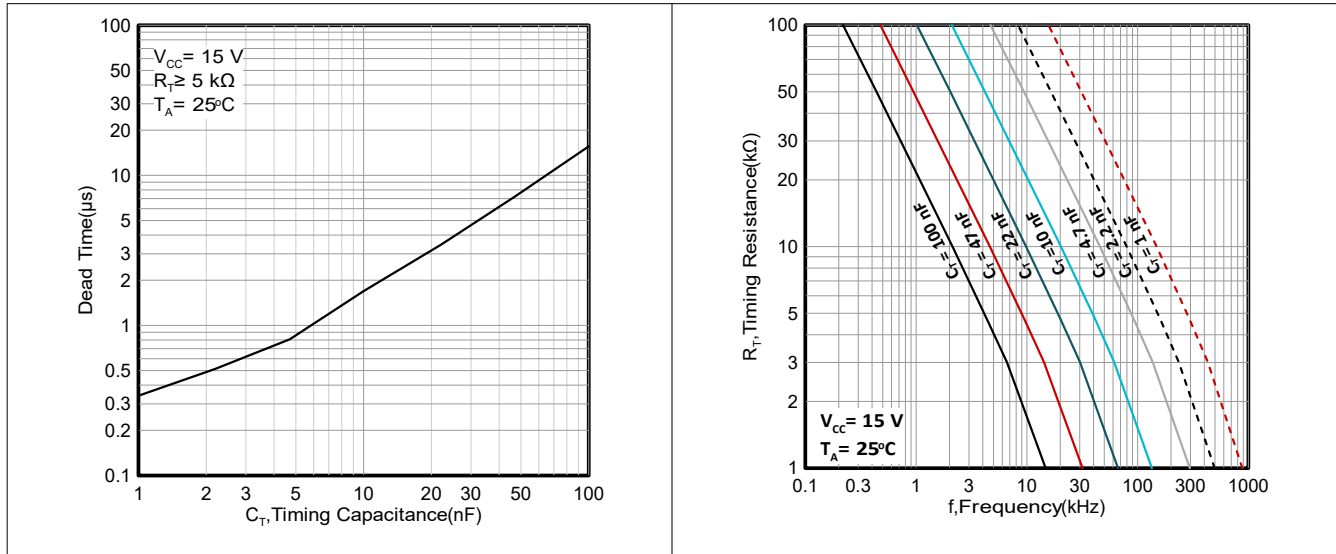


図 7-6. Open-Loop Laboratory Test Fixture

7.4 Typical Application

7.4.1 Application Curves



8 Device and Documentation Support

8.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL284xB	Click here	Click here	Click here	Click here	Click here
TL384xB	Click here	Click here	Click here	Click here	Click here

8.2 Trademarks

すべての商標は、それぞれの所有者に帰属します。

8.3 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

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8.4 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision B (July, 2007) to Revision C (October, 2024)

Page

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新..... 1
- Changed ESD ratings, CDM rating from $\pm 3000\text{V}$ to $\pm 2000\text{V}$ 4
- Changed thermal information for D-8, D-14, and P-8 packages..... 5
- Changed Electrical Char. table, TOTAL STANDBY CURRENT, VCC Zener voltage, typical value from 34V to 39V..... 5

• Changed in Electrical Char. table, Oscillator Section: at $T_j=25^{\circ}\text{C}$, min. value from 49kHz to 47kHz, max. value from 55kHz to 57kHz.....	5
• Changed in Electrical Char. table, Oscillator Section: at $T_A=T_{\text{low}}$ to T_{high} , min. value from 48kHz to 44kHz, max. value from 56kHz to 60kHz.....	5
• Changed in Electrical Char. table, OUTPUT Section: Rise and fall time, typical value from 50ns to 25ns.....	7
• Changed in Electrical Char. table, PWM: maximum duty cycle of TLx842/3B, minimum value from 94% to 92%.....	7
• Changed in Electrical Char. table, PWM: maximum duty cycle of TLx844/5B, minimum value from 47% to 46%.....	7
• Changed Part numbers edited.....	7
• Updated the <i>Typical Characteristics</i> graphs for $I_{\text{discharge}}$ and T_a , $I_{V_{\text{CC}}-V_{\text{CC}}}$, and D_{max} and R_t	8
• Updated Application Curves for $t_{\text{deadtime-Ct}}$ and $R_t\text{-f}$	17

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL2842BD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	TL2842B	
TL2842BD-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	2842B	
TL2842BDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL2842B	Samples
TL2842BDR-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2842B	Samples
TL2842BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL2842BP	Samples
TL2843BD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	TL2843B	
TL2843BD-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	2843B	
TL2843BDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL2843B	Samples
TL2843BDR-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2843B	Samples
TL2843BDRG4-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2843B	Samples
TL2843BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL2843BP	Samples
TL2844BD-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	2844B	
TL2844BDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL2844B	Samples
TL2844BDR-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2844B	Samples
TL2844BDRG4-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2844B	Samples
TL2845BD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	TL2845B	
TL2845BD-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	2845B	
TL2845BDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL2845B	Samples
TL2845BDR-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2845B	Samples
TL2845BDRG4-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2845B	Samples
TL3842BD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	TL3842B	
TL3842BD-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	3842B	
TL3842BDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3842B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL3842BDR-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3842B	Samples
TL3842BP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70	TL3842BP	
TL3843BD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	TL3843B	
TL3843BD-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	3843B	
TL3843BDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3843B	Samples
TL3843BDR-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3843B	Samples
TL3843BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL3843BP	Samples
TL3844BD-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	3844B	
TL3844BDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3844B	Samples
TL3844BDR-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3844B	Samples
TL3844BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL3844BP	Samples
TL3845BD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	TL3845B	
TL3845BD-8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	3845B	
TL3845BDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	TL3845B	
TL3845BDR-8	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3845B	Samples
TL3845BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL3845BP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TL2843B :

- Automotive : [TL2843B-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL2842BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL2842BDR-8	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL2843BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL2843BDR-8	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL2844BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL2844BDR-8	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL2845BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL2845BDR-8	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3842BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3842BDR-8	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3843BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3843BDR-8	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3844BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3844BDR-8	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3845BDR-8	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL2842BDR	SOIC	D	14	2500	356.0	356.0	35.0
TL2842BDR-8	SOIC	D	8	2500	353.0	353.0	32.0
TL2843BDR	SOIC	D	14	2500	356.0	356.0	35.0
TL2843BDR-8	SOIC	D	8	2500	353.0	353.0	32.0
TL2844BDR	SOIC	D	14	2500	356.0	356.0	35.0
TL2844BDR-8	SOIC	D	8	2500	353.0	353.0	32.0
TL2845BDR	SOIC	D	14	2500	356.0	356.0	35.0
TL2845BDR-8	SOIC	D	8	2500	353.0	353.0	32.0
TL3842BDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3842BDR-8	SOIC	D	8	2500	353.0	353.0	32.0
TL3843BDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3843BDR-8	SOIC	D	8	2500	353.0	353.0	32.0
TL3844BDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3844BDR-8	SOIC	D	8	2500	353.0	353.0	32.0
TL3845BDR-8	SOIC	D	8	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TL2842BP	P	PDIP	8	50	506	13.97	11230	4.32
TL2843BP	P	PDIP	8	50	506	13.97	11230	4.32
TL2844BDR	D	SOIC	14	2500	507	8	3940	4.32
TL3843BP	P	PDIP	8	50	506	13.97	11230	4.32
TL3844BDR	D	SOIC	14	2500	507	8	3940	4.32
TL3844BP	P	PDIP	8	50	506	13.97	11230	4.32
TL3845BP	P	PDIP	8	50	506	13.97	11230	4.32

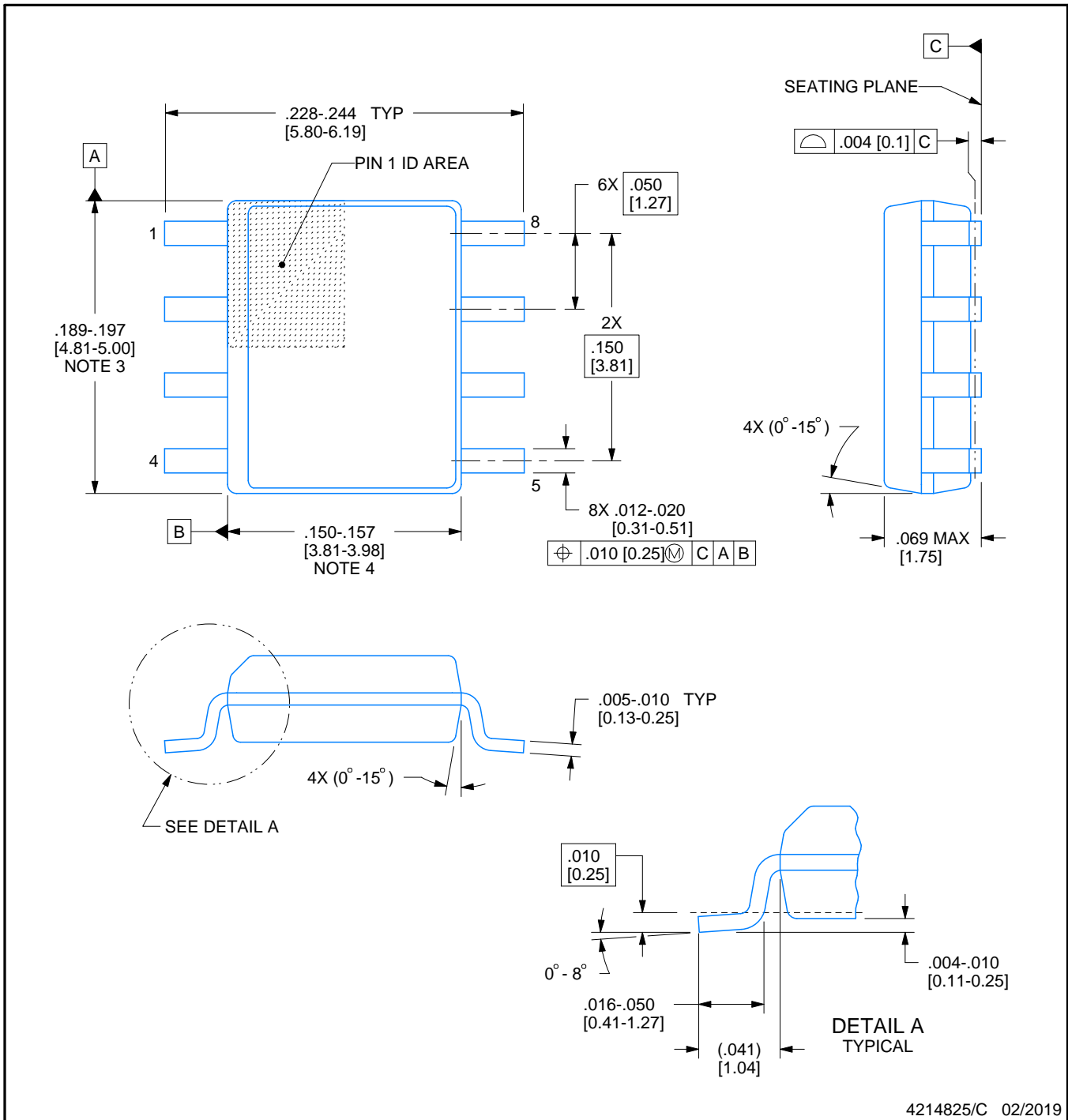


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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