# LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIER

**Check for Samples: TL072-EP, TL074-EP**

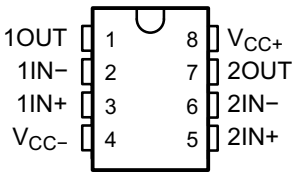
## FEATURES

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion: 0.003% Typ**
- **Low Noise**
  **$V_n$ = 18 nV/$\sqrt{Hz}$ Typ at f = 1 kHz**
- **High Input Impedance: JFET Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate: 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes $V_{CC+}$**

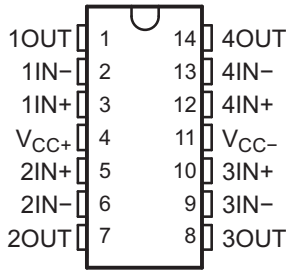
## SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Extended (–40°C to 125°C) or Military (–55°C to 125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

**TL072**
**D PACKAGE**
**(TOP VIEW)**




**TL074**
**D PACKAGE**
**(TOP VIEW)**




## DESCRIPTION/ORDERING INFORMATION

The JFET-input operational amplifiers in the TL07x is similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07x ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The TL07x is characterized for operation over the extended temperature range of –40°C to 125°C or military temperature range of –55°C to 125°C.

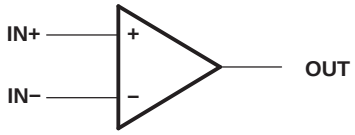
**ORDERING INFORMATION(1)**

| $T_A$ | $V_{IO}$maX AT 25°C | PACKAGE | | ORDERABLE PART NUMBER | TOP-SIDE MARKING | VID NUMBER |
|---|---|---|---|---|---|---|
| –40°C to 125°C | 6 mV | SOIC – D | Reel of 2500 | TL072QDREP | TL072Q | V62/12604-01XE |
| | | | | TL074QDREP | TL074Q | V62/11621-01XE |
| –55°C to 125°C | 6 mV | SOIC – D | Reel of 2500 | TL074MDREP | TL074M | V62/11621-02XE |
| | | | Tube of 75 | TL074MDEP | TL074M | V62/11621-02XE-T |

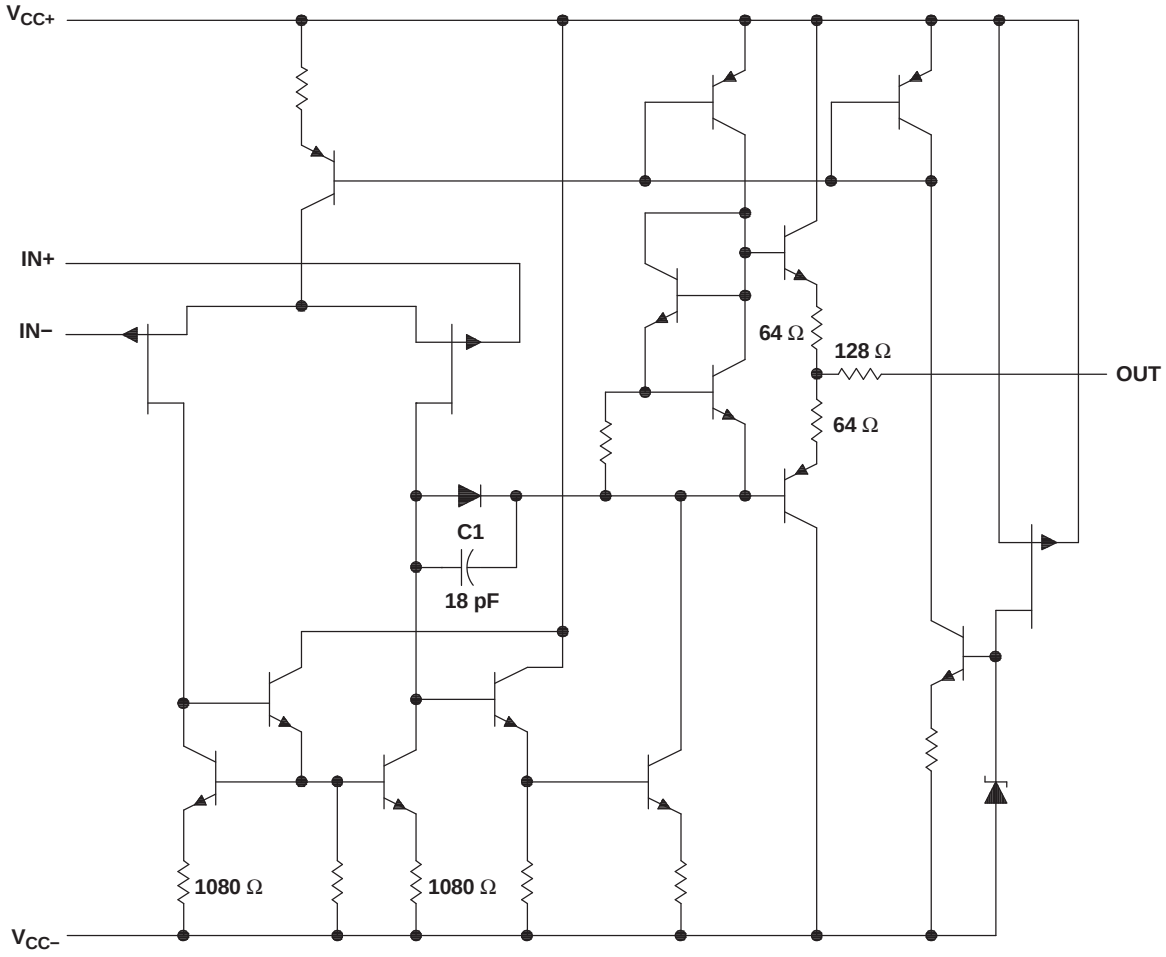
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## TL072 and TL074 SYMBOL (EACH AMPLIFIER)




## SCHEMATIC (EACH AMPLIFIER)




All component values shown are nominal.

| COMPONENT COUNT(1) | | |
|---|---|---|
| **COMPONENT TYPE** | **TL072** | **TL074** |
| Resistors | 22 | 44 |
| Transistors | 28 | 56 |
| JFET | 4 | 6 |
| Diodes | 2 | 4 |
| Capacitors | 2 | 4 |
| epi-FET | 2 | 4 |

(1) Includes bias and trim circuitry

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC+}$ | Supply voltage(2) | | | 18 | V |
| $V_{CC-}$ | | | | 18 | |
| $V_{ID}$ | Differential input voltage(3) | | | ±30 | V |
| $V_I$ | Input voltage(2) (4) | | | ±15 | V |
| | Duration of output short circuit(5) | | Unlimited | | |
| $\theta_{JA}$ | Thermal resistance, junction-to-ambient(6) (7) | TL072 | | 97.5 | °C/W |
| | | TL074 | | 86 | |
| $\theta_{JC}$ | Thermal resistance, junction-to-case(7) | TL072 | | 38.3 | °C/W |
| | | TL074 | | 51.5 | |
| $T_J$ | Operating virtual junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between $V_{CC+}$ and $V_{CC-}$.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
(6) Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

## ELECTRICAL CHARACTERISTICS

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS(1) | $T_A$ (2) | TL072 | | | TL074 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_O$ = 0, $R_S$ = 50 Ω | 25°C | | 3 | 6 | | 3 | 6 | mV |
| | | | Full range | | | 8 | | | 8 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | $V_O$ = 0, $R_S$ = 50 Ω | Full range | | 18 | | | 18 | | μV/°C |
| $I_{IO}$ | Input offset current | $V_O$ = 0 | 25°C | | 5 | 100 | | 5 | 100 | pA |
| | | | 125°C | | | 2 | | | 2 | nA |
| $I_{IB}$ | Input bias current | $V_O$ = 0 | 25°C | | 65 | 200 | | 65 | 200 | pA |
| | | | 125°C | | | 20 | | | 20 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | ±11 | –12 to 15 | | ±11 | –12 to 15 | | V |
| $V_{OM}$ | Maximum peak output voltage swing | $R_L$ = 10 kΩ | 25°C | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| | | $R_L$ ≥ 10 kΩ | Full range | ±12 | | | ±12 | | | |
| | | $R_L$ ≥ 2 kΩ | | ±10 | | | ±10 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_O$ = ±10 V, $R_L$ ≥ 2 kΩ | 25°C | 35 | 200 | | 35 | 200 | | V/mV |
| | | | Full range | 15 | | | 15 | | | |
| $B_1$ | Unity-gain bandwidth | | 25°C | | 3 | | | 3 | | MHz |
| $r_i$ | Input resistance | | 25°C | | $10^{12}$ | | | $10^{12}$ | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$min, $V_O$ = 0, $R_S$ = 50 Ω | 25°C | 80 | 86 | | 80 | 86 | | dB |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$) | $V_{CC}$ = ±9 V to ±15 V, $V_O$ = 0, $R_S$ = 50 Ω | 25°C | 80 | 86 | | 80 | 86 | | dB |
| $I_{CC}$ | Supply current (each amplifier) | $V_O$ = 0, No load | 25°C | | 1.4 | 2.5 | | 1.4 | 2.5 | mA |
| $V_{O1}/V_{O2}$ | Crosstalk attenuation | $A_{VD}$ = 100 | 25°C | | 120 | | | 120 | | dB |

(1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 3. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

(2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is $T_A$ = –40°C to 125°C for TL07xQ and $T_A$ = -55°C to 125°C for TL07xM.

## OPERATING CHARACTERISTICS

$V_{CC\pm}$ = ±15 V, $T_A$= 25°C

| PARAMETER | | TEST CONDITIONS | | TL072 | | | TL074 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR | Slew rate at unity gain | $V_I$ = 10 V, $C_L$ = 100 pF, | $R_L$ = 2 kΩ, See Figure 1 | 8 | 13 | | 8 | 13 | | V/μs |
| $t_r$ | Rise-time overshoot factor | $V_I$ = 20 V, $C_L$ = 100 pF, | $R_L$ = 2 kΩ, See Figure 1 | | 0.1 | | | 0.1 | | μs |
| | | | | | 20 | | | 20 | | % |
| $V_n$ | Equivalent input noise voltage | $R_S$ = 20 Ω | f = 1 kHz | | 18 | | | 18 | | nV/√Hz |
| | | | f = 10 Hz to 10 kHz | | 4 | | | 4 | | μV |
| $I_n$ | Equivalent input noise current | $R_S$ = 20 Ω, | f = 1 kHz | | 0.01 | | | 0.01 | | pA/√Hz |
| THD | Total harmonic distortion | $V_I$rms = 6 V, $R_L$ ≥ 2 kΩ, f = 1 kHz, | $A_{VD}$ = 1, RS ≤ 1 kΩ, | | 0.003 | | | 0.003 | | % |

## PARAMETER MEASUREMENT INFORMATION

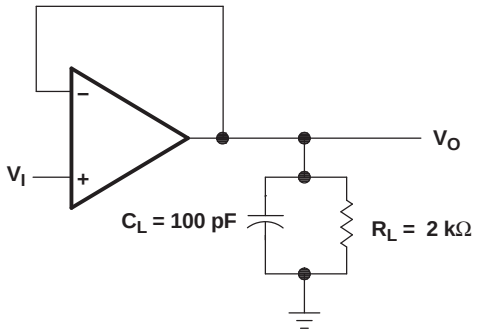



**Figure 1. Unity-Gain Amplifier**

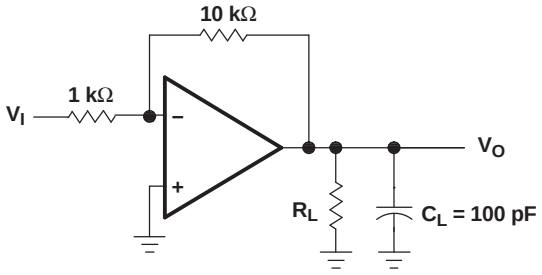



**Figure 2. Gain-of-10 Inverting Amplifier**

## TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE**

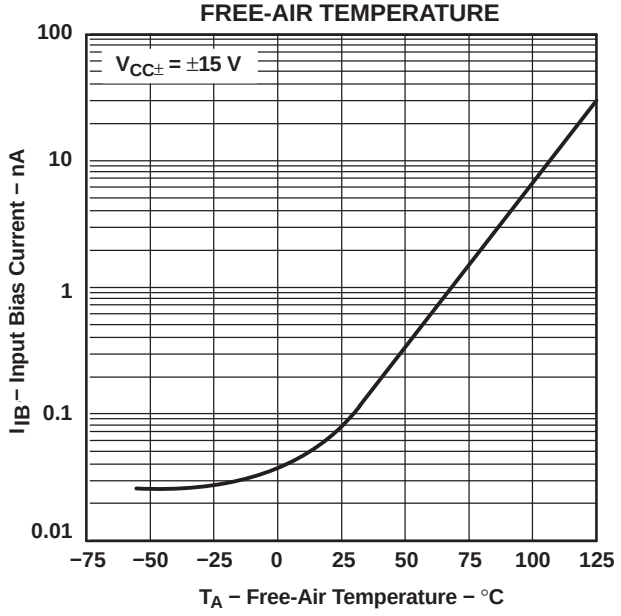



Figure 3.

**MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY**

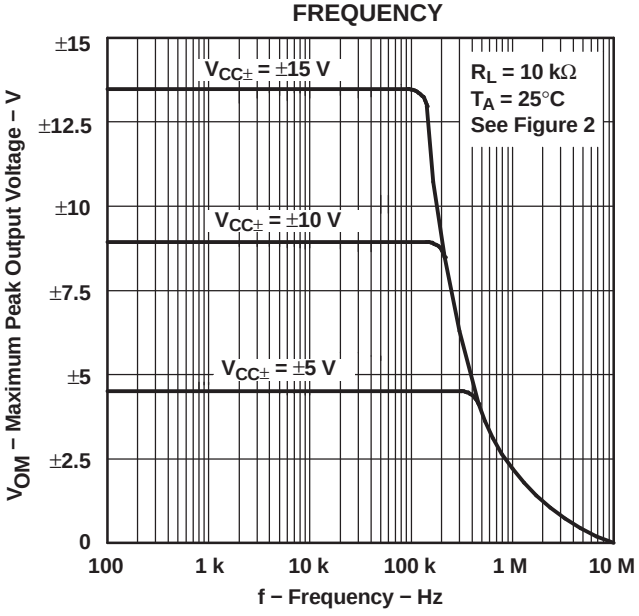



Figure 4.

**MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY**

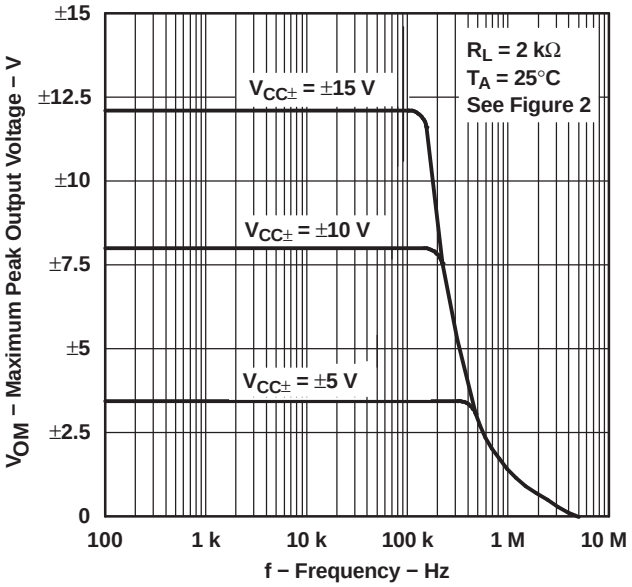



Figure 5.

**MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY**

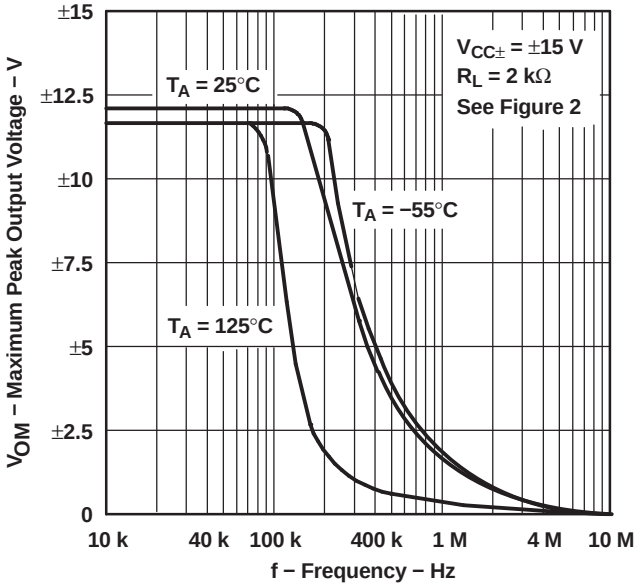



Figure 6.

## TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

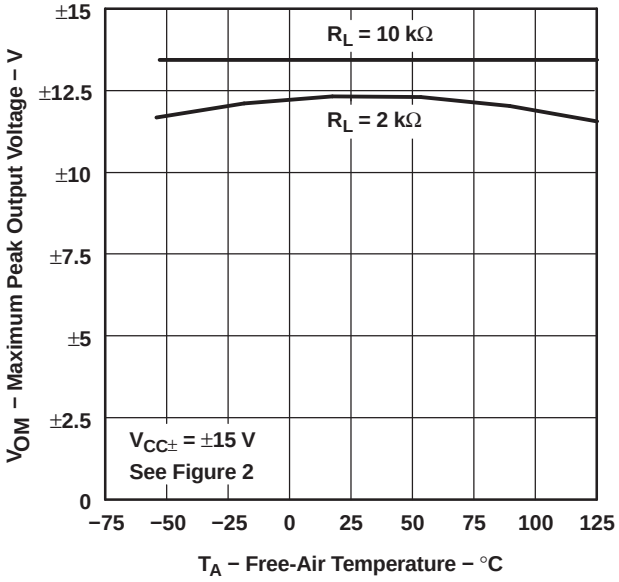



**Figure 7.**

**MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE**

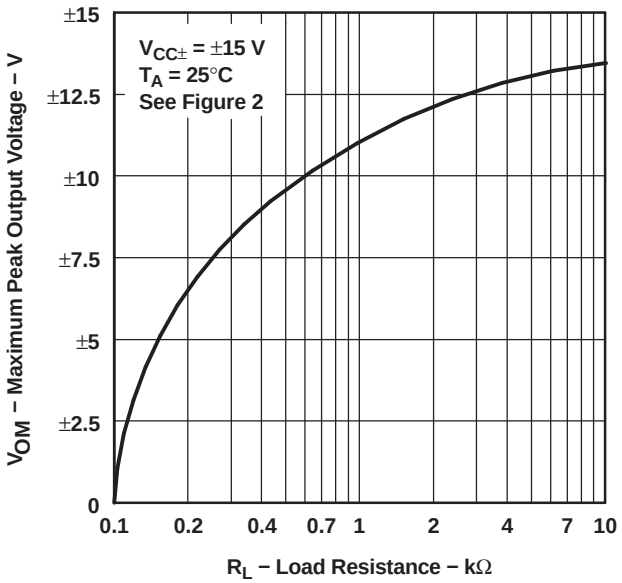



**Figure 8.**

**MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE**

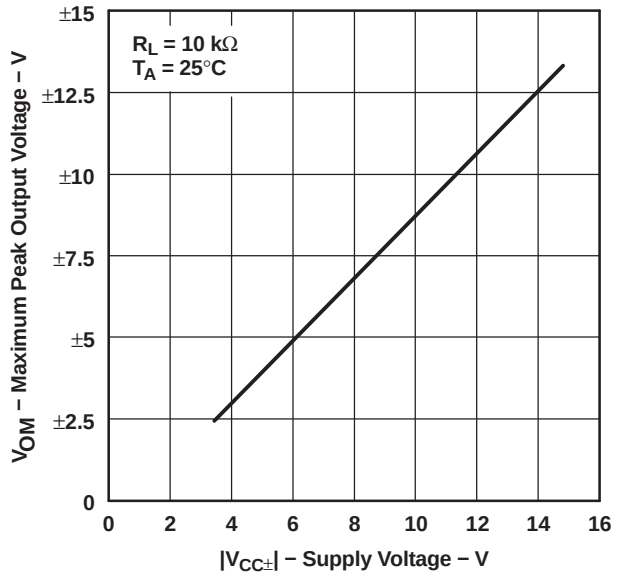



**Figure 9.**

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE**

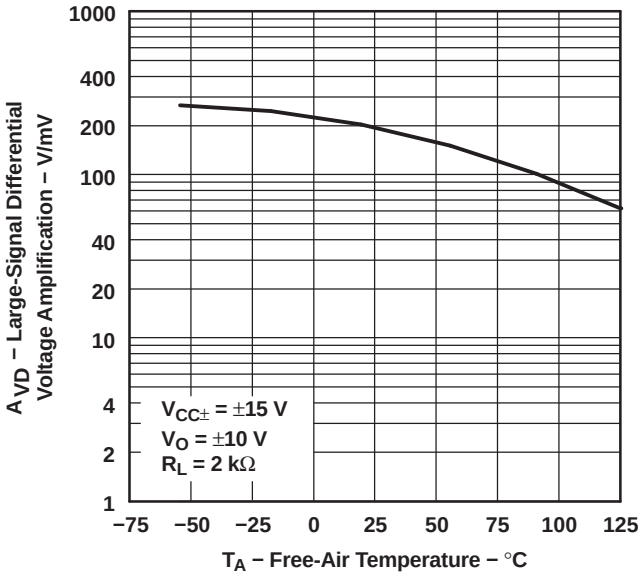



**Figure 10.**

## TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY**

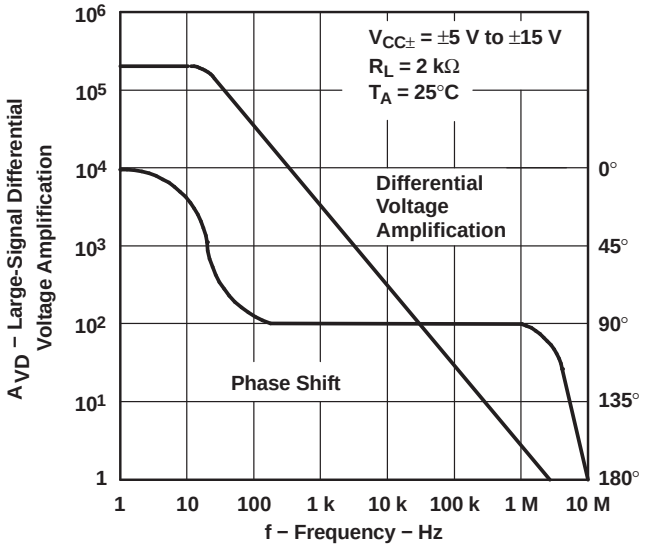



Figure 11.

**NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE**

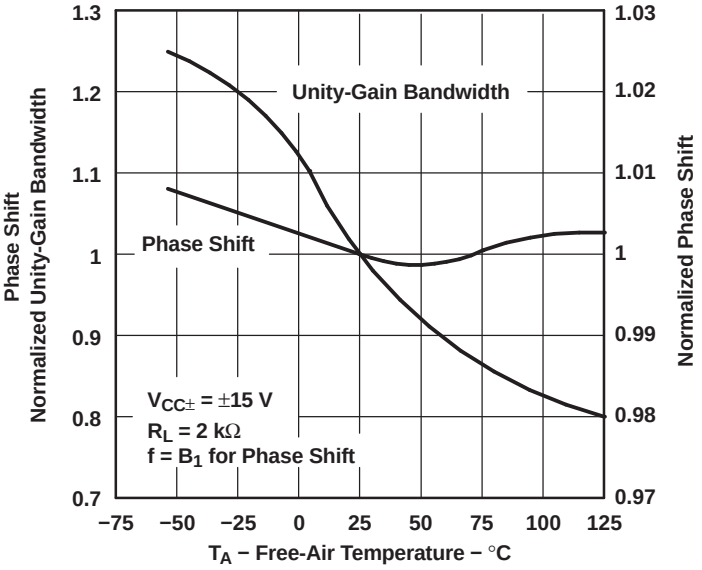



Figure 12.

**COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE**

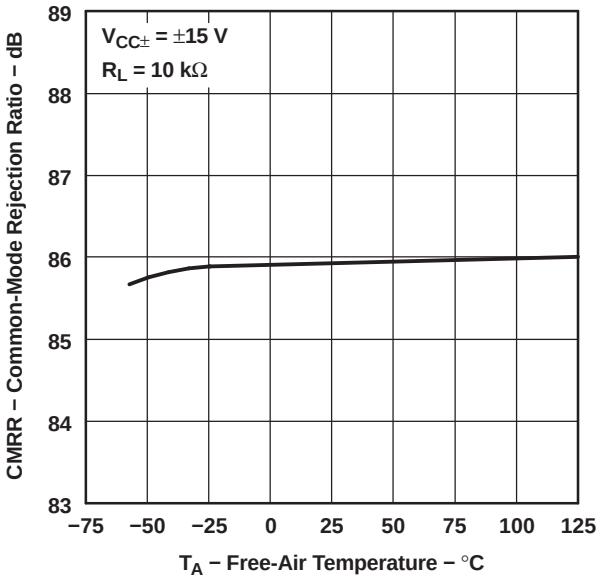



Figure 13.

**SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE**

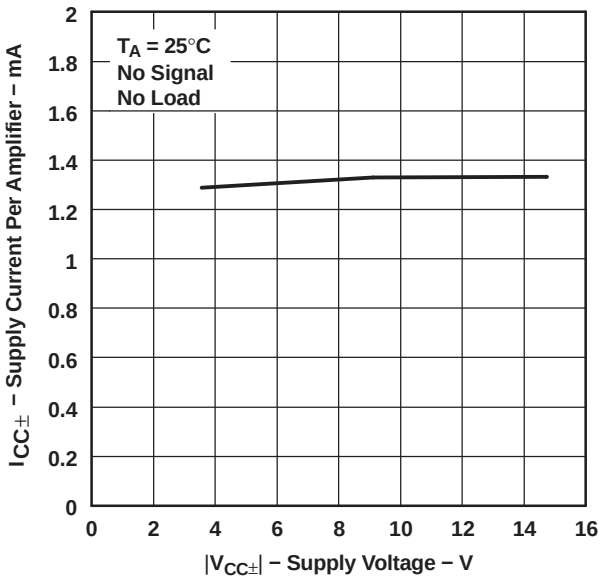



Figure 14.

## TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE**

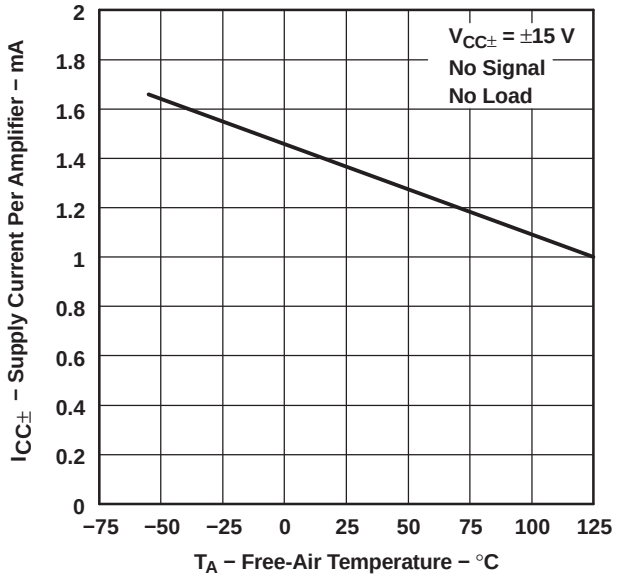



**Figure 15.**

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

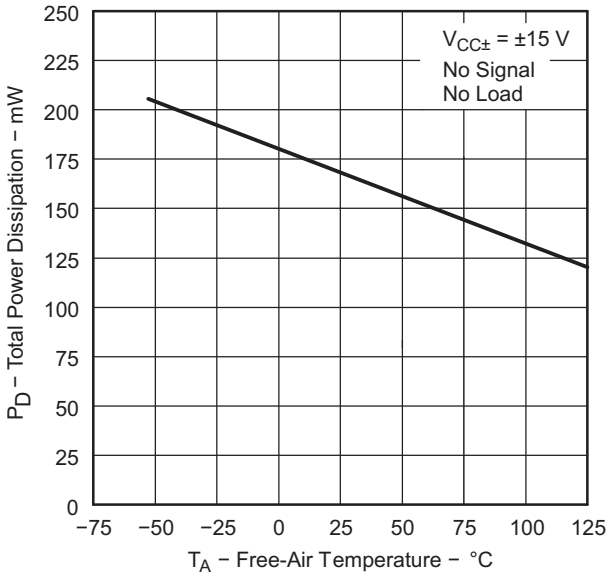



**Figure 16.**

**NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE**

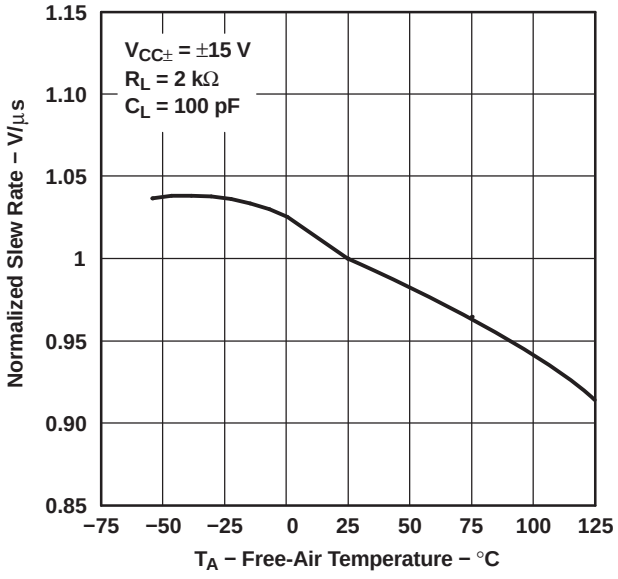



**Figure 17.**

**EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY**

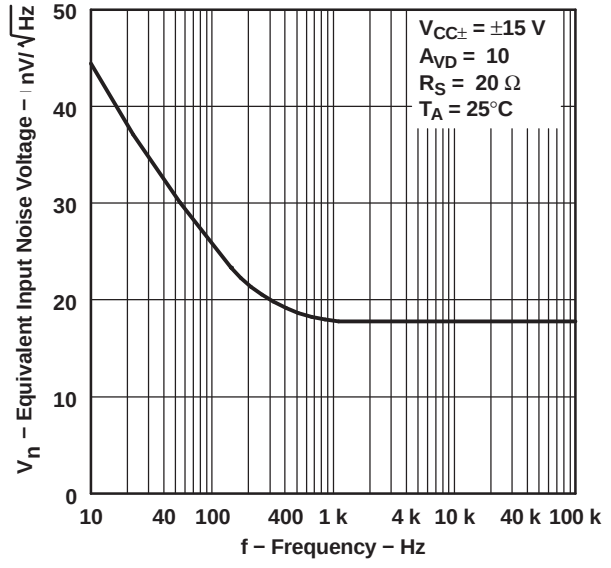



**Figure 18.**

## TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

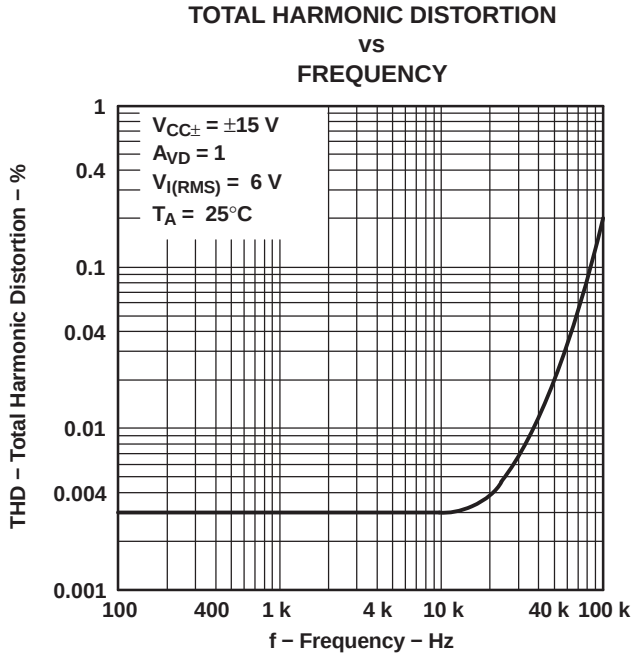



Figure 19.

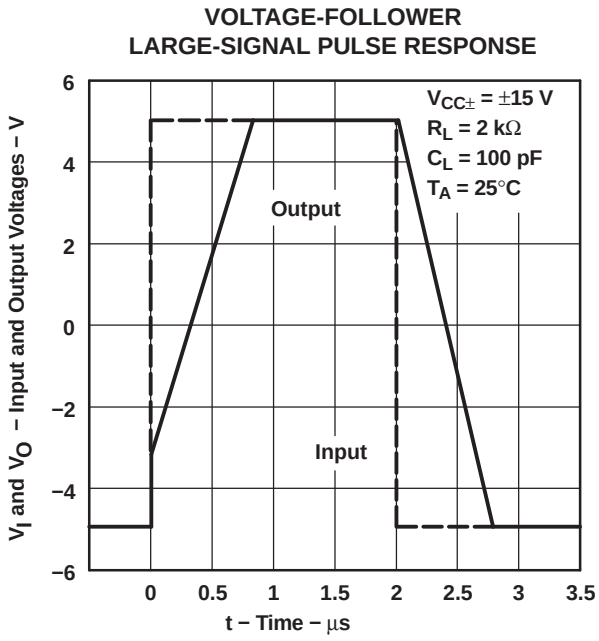



Figure 20.

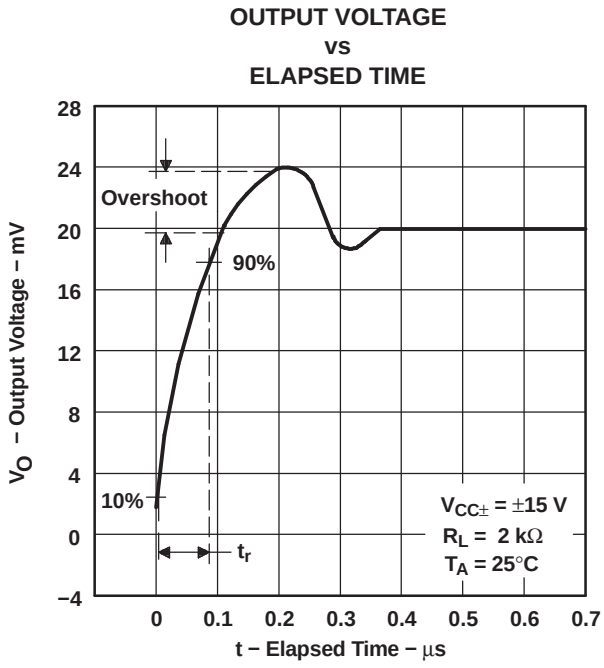
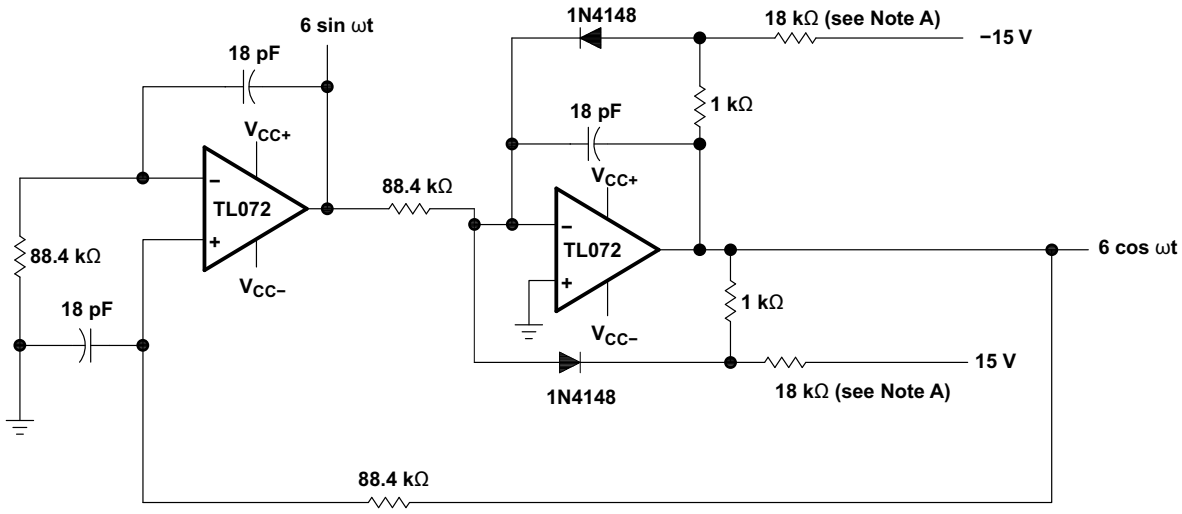



Figure 21.

## APPLICATION INFORMATION




NOTE A: These resistor values may be adjusted for a symmetrical output.

**Figure 22. 100-kHz Quadrature Oscillator**

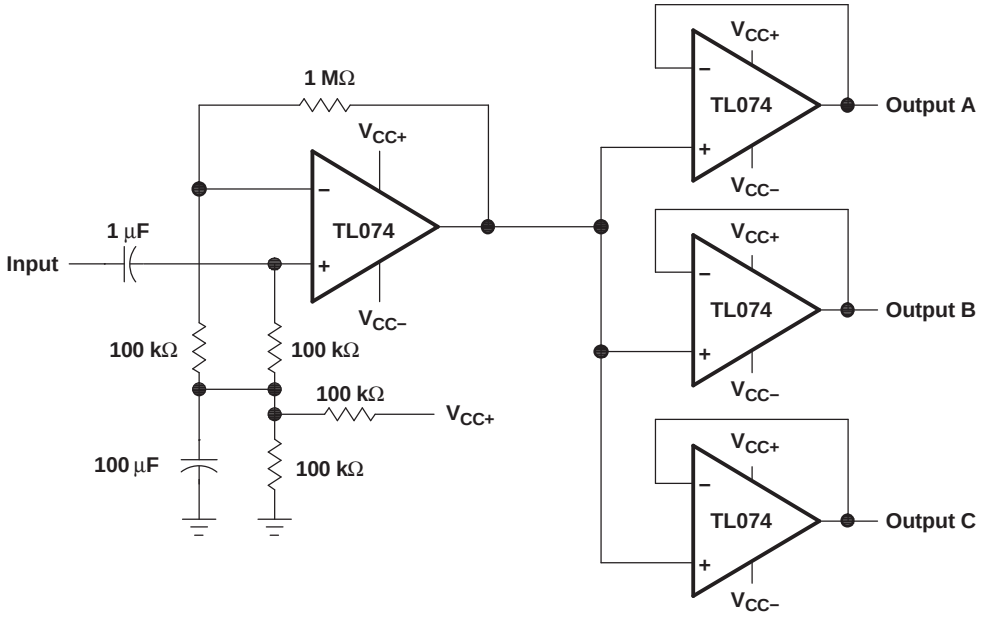



**Figure 23. Audio-Distribution Amplifier**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL072QDREP | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL072Q | Samples |
| TL074MDEP | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TL074M | Samples |
| TL074MDREP | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TL074M | Samples |
| TL074QDREP | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL074Q | Samples |
| V62/11621-01XE | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL074Q | Samples |
| V62/11621-02XE | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TL074M | Samples |
| V62/11621-02XE-T | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TL074M | Samples |
| V62/12604-01XE | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL072Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF TL072-EP, TL074-EP :**

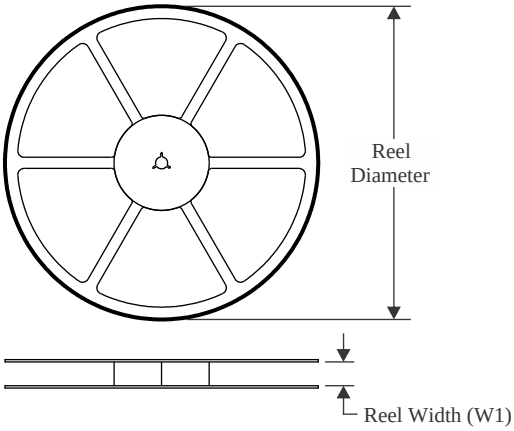
- Catalog : TL072, TL074
- Military : TL072M, TL074M

NOTE: Qualified Version Definitions:

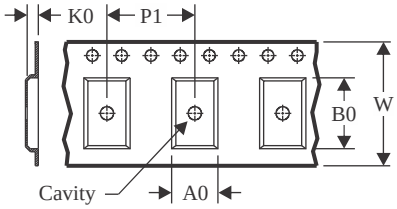
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

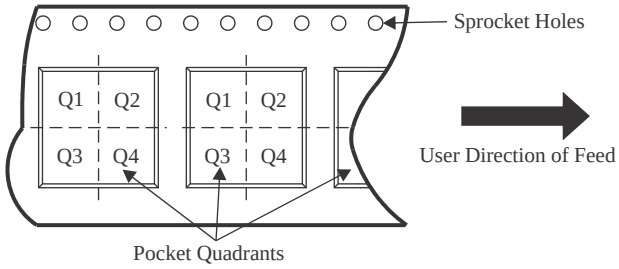



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

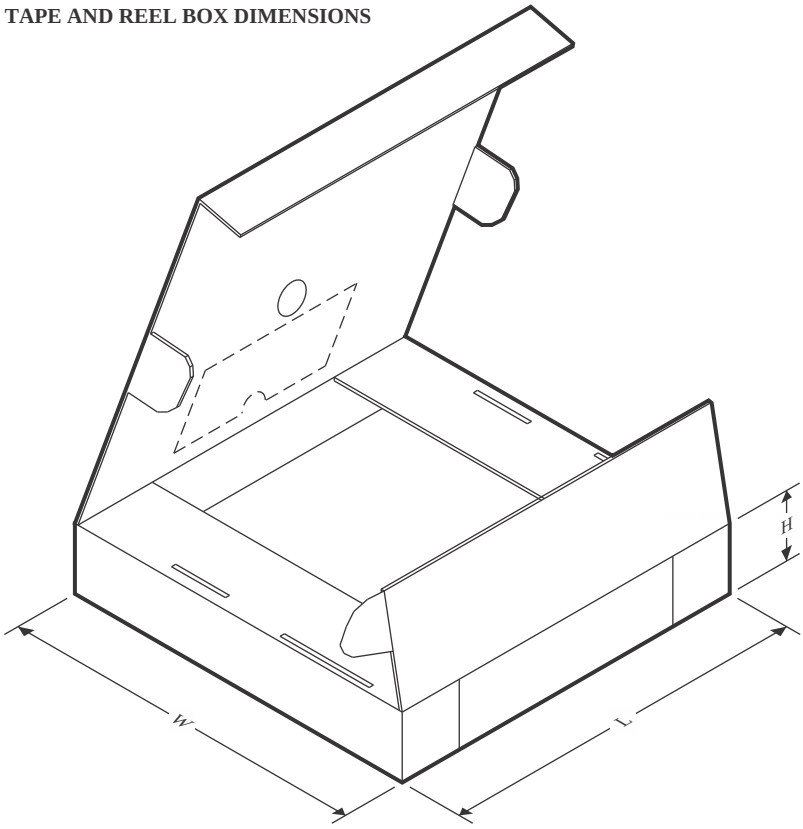
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL072QDREP | SOIC | D | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL074MDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL074QDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

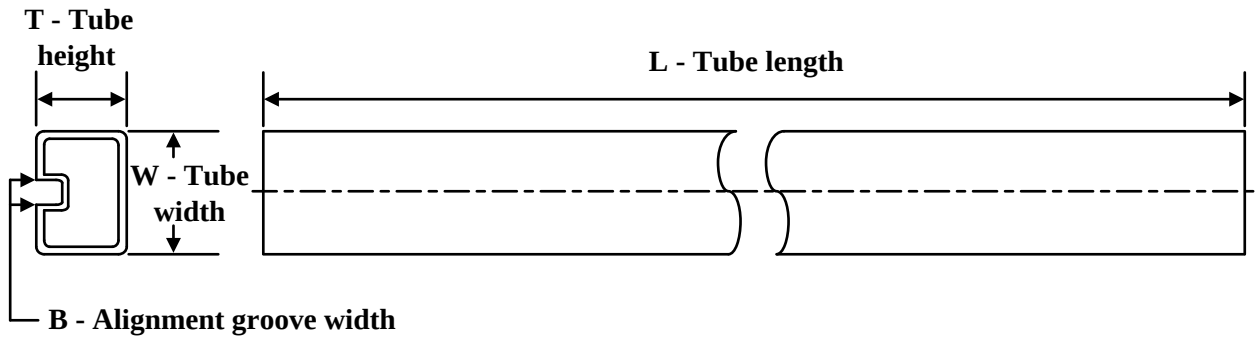
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

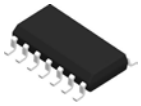
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL072QDREP | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL074MDREP | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TL074QDREP | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TL074MDEP | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| V62/11621-02XE-T | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |

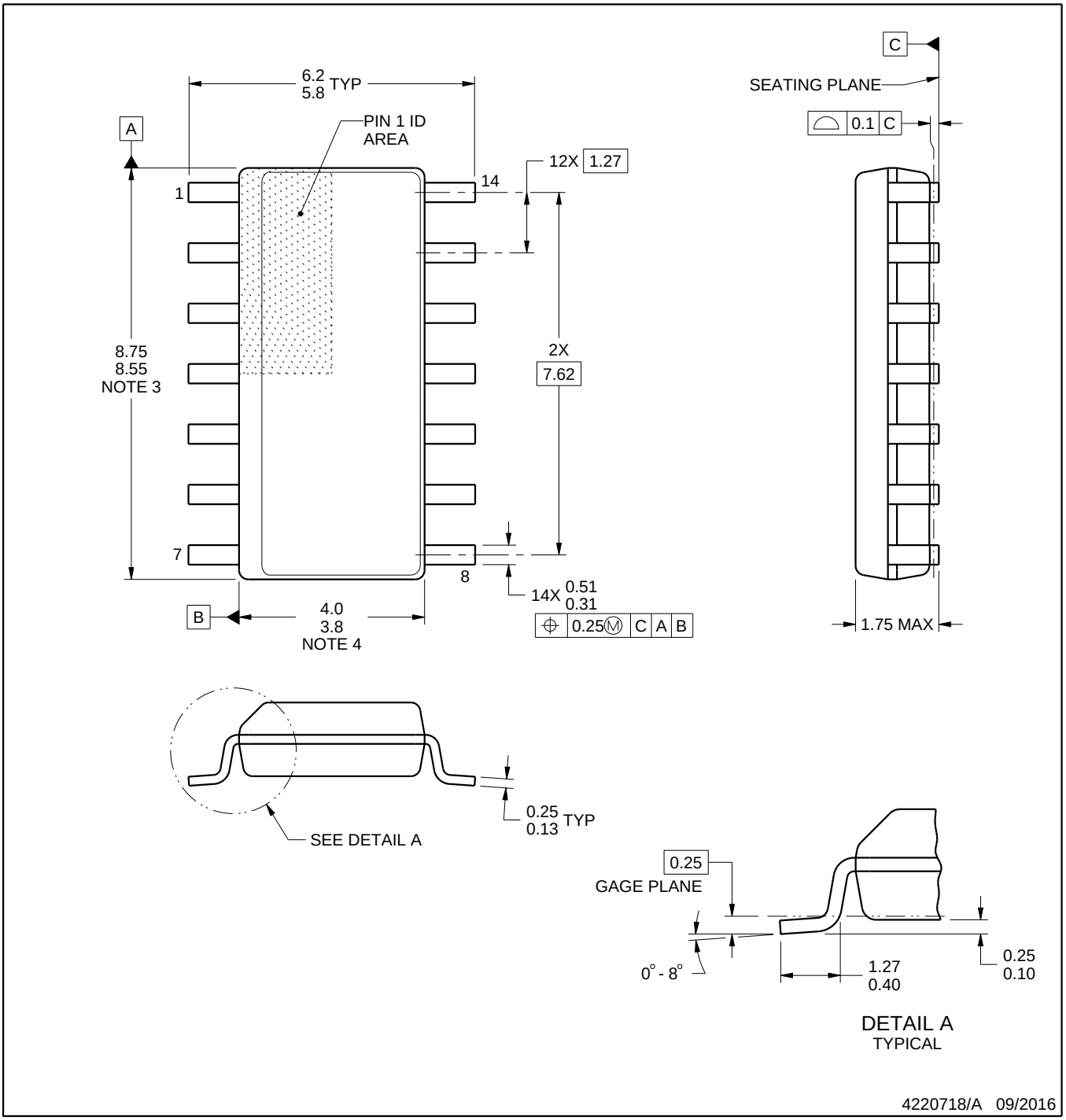


# PACKAGE OUTLINE

## D0014A

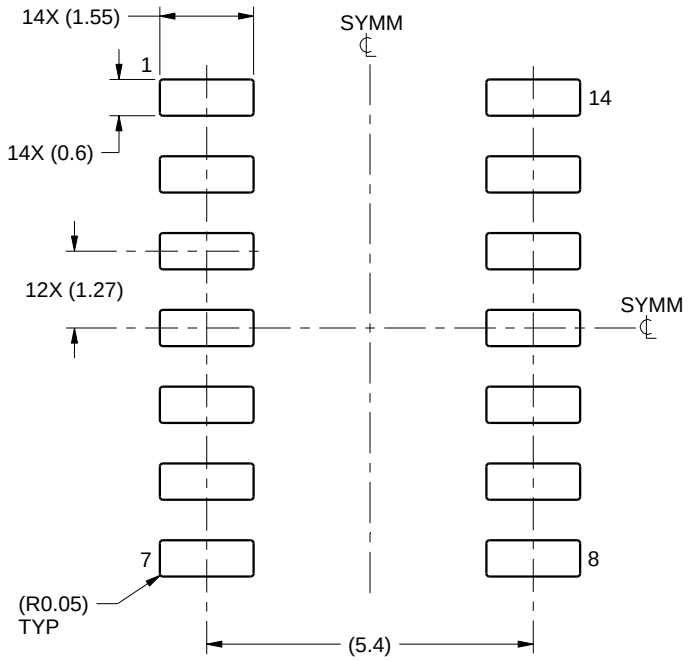
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

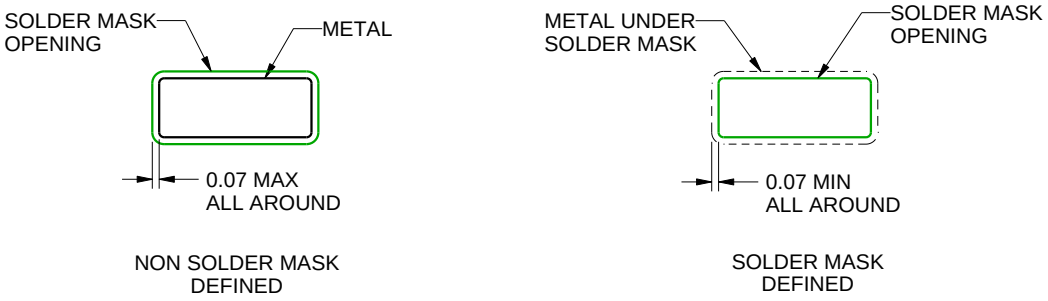



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

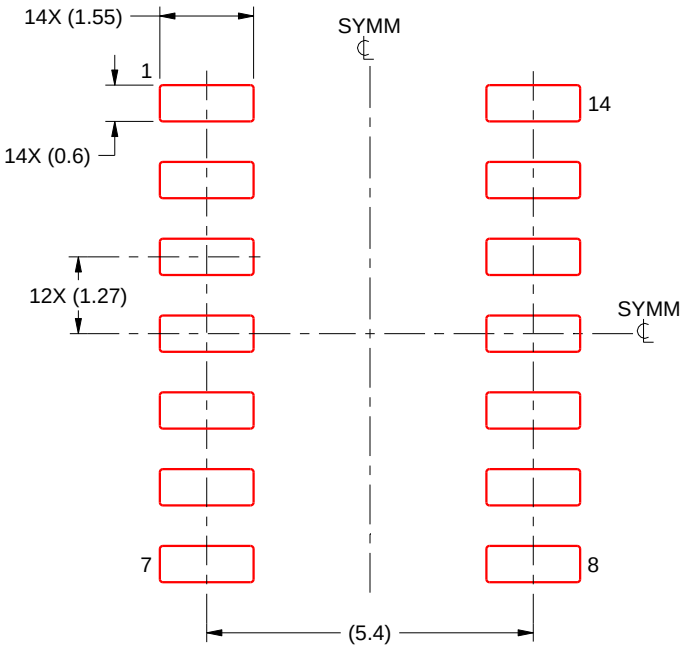
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

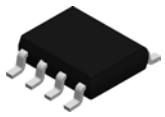



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

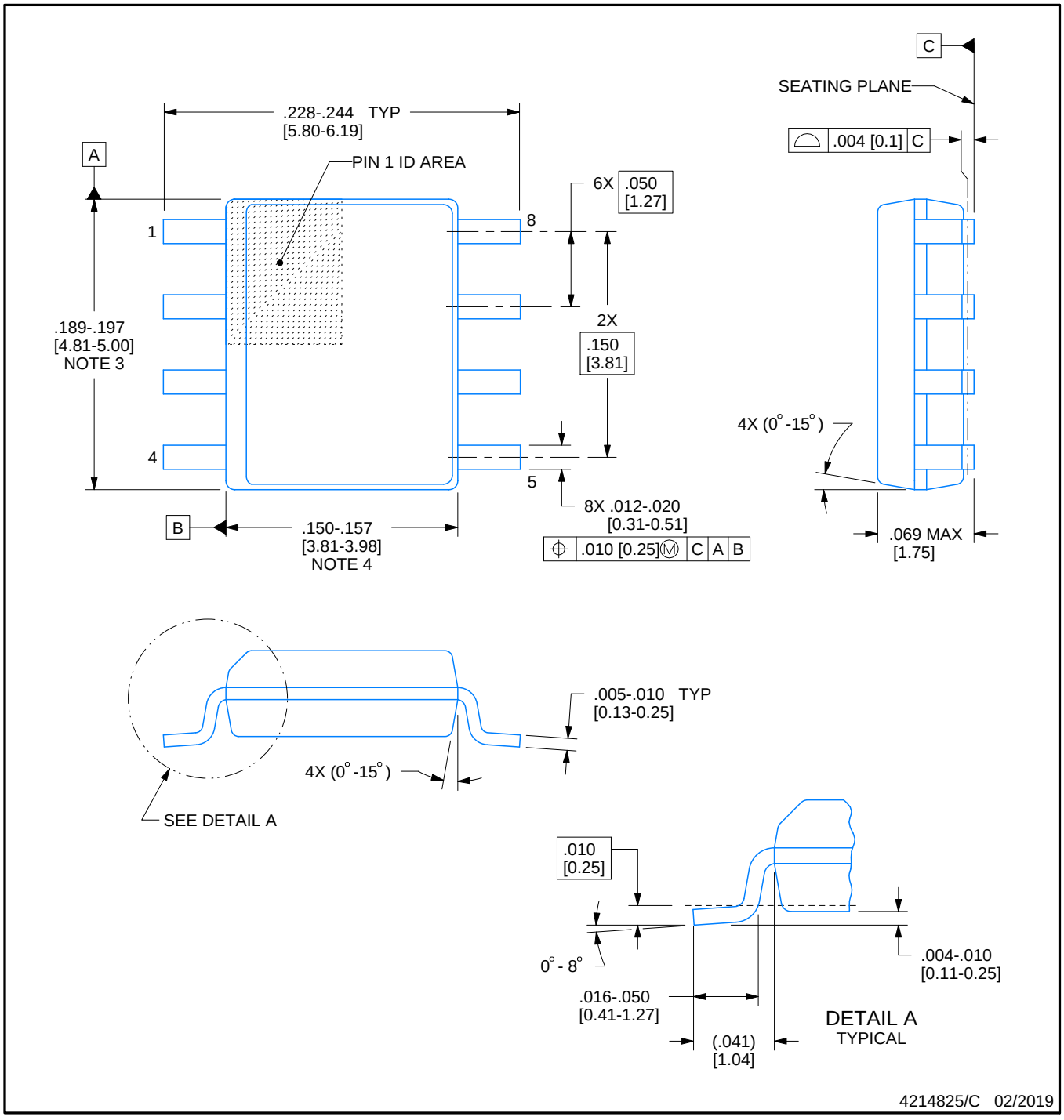


# PACKAGE OUTLINE

## D0008A

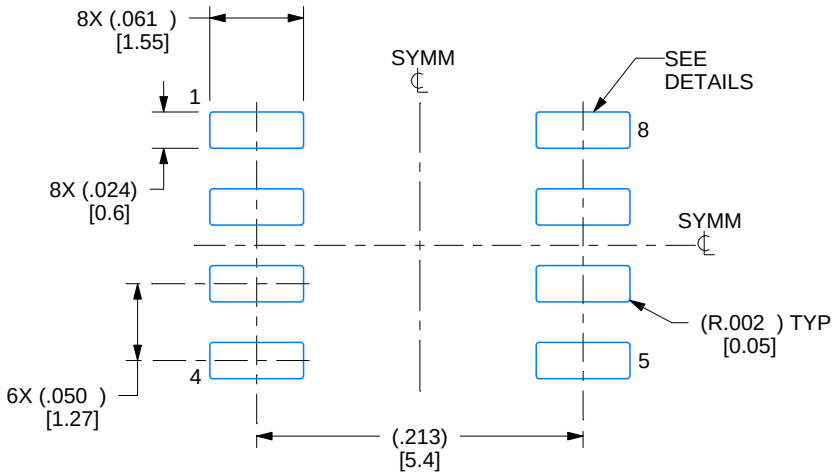
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

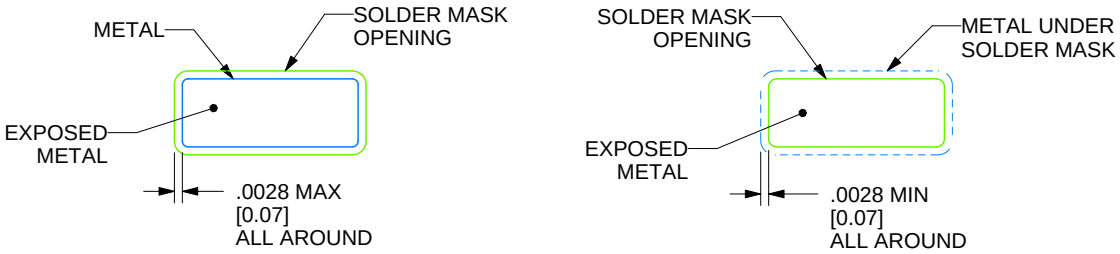



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

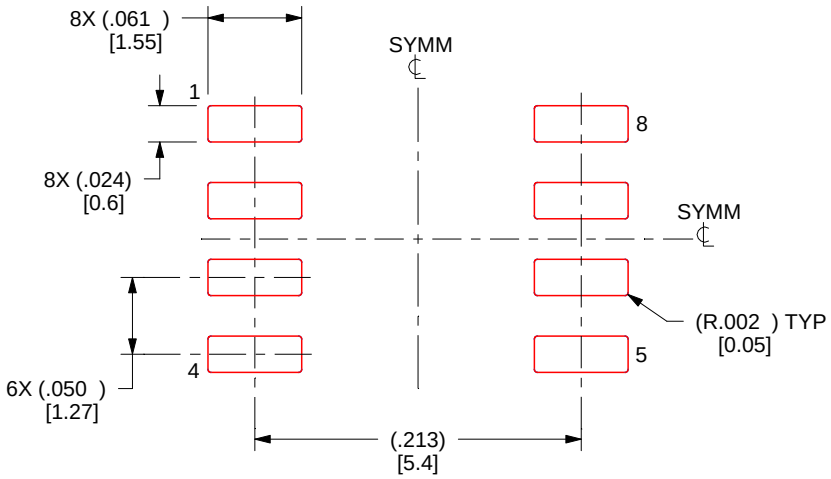
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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