TCA9537 リモート 4 ビット I²C/SMBus I/O エクスパンダ、構成レジスタ付き

1 特長

- I²C から GPIO へのエクスパンダ
- 1.65V～5.5V の動作電源電圧範囲
- 5V 許容の I/O ポート
- I²C ゼネラル・コールによるソフトウェア・リセット
- 外部リセット制御用の $\overline{\text{RESET}}$ 入力ピン
- 専用 $\overline{\text{INT}}$ 出力
- 1MHz の Fast mode plus I²C バス
- 入力 / 出力構成レジスタ
- 極性反転レジスタ
- パワーオン・リセット内蔵
- 電源投入時はすべてのチャネルが入力に構成された状態
- SCL/SDA 入力のノイズ・フィルタ
- 大電流の最大駆動能力を持つラッチ付き出力により LED を直接駆動
- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- パーソナル・エレクトロニクス
  - ウェアラブル
  - 携帯電話 / スマートフォン
  - ゲーム機
- サーバー
- ルータ

3 概要

TCA9537 は I²C バス用の 4 ビット I/O エクスパンダで、1.65V～5.5V の V_{CC} で動作するように設計されています。I²C インターフェイスにより、ほとんどのマイクロコントローラ・ファミリの汎用リモート I/O 拡張に使用できます。

システム・コントローラは、I/O 構成レジスタ・ビットに書き込むことで、I/O を入力にするか出力にするかを設定できます。それぞれの入力または出力のデータは、対応する入力または出力レジスタに保持されています。入力ポート・レジスタの極性は、極性反転レジスタで反転できます。

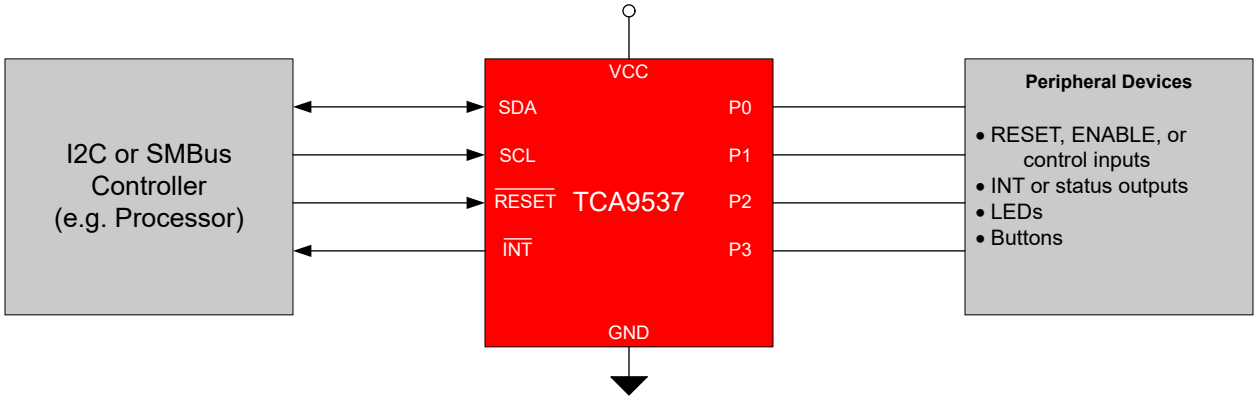
TCA9537 のオープンドレイン割り込み出力 ($\overline{\text{INT}}$) は、いずれかの入力が、対応する入力ポート・レジスタの状態と異なるときにアクティブになり、入力状態が変化したことをシステム・コントローラに通知するため使用されます。

システム・プロセッサは、タイムアウトまたはその他の不適切な動作があった場合、I²C ソフト・リセット・コマンドを使って TCA9537 をリセットできます。このコマンドにより、レジスタはデフォルト状態に設定されます。この操作には $\overline{\text{RESET}}$ ピンを使用することもできます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TCA9537	VSSOP (10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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4 Revision History

DATE	REVISION	NOTES
February 2022	*	Initial Release

5 Pin Configuration and Functions

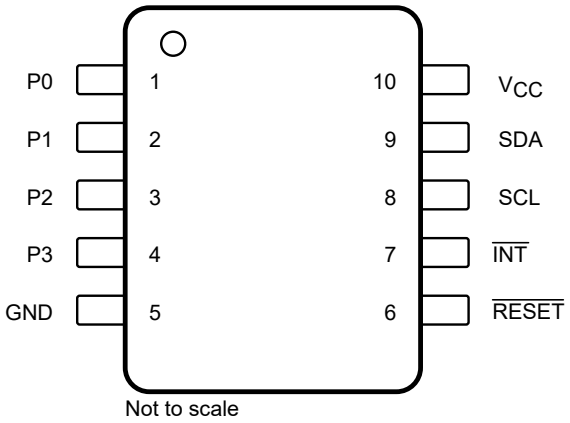


図 5-1. DGS Package, 10-Pin VSSOP, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
DGS	NAME		
1	P0	I/O	P-port input-output. Push-pull design structure.
2	P1	I/O	P-port input-output. Push-pull design structure.
3	P2	I/O	P-port input-output. Push-pull design structure.
4	P3	I/O	P-port input-output. Push-pull design structure.
5	GND	—	Ground
6	$\overline{\text{RESET}}$	I	Active low reset input. If unused, connect to V_{CC} through a pull-up resistor
7	$\overline{\text{INT}}$	O	Interrupt open drain output, requires a pull-up resistor.
8	SCL	I/O	Serial clock bus. Connect to V_{CC} through a pull-up resistor
9	SDA	I/O	Serial data bus. Connect to V_{CC} through a pull-up resistor
10	V_{CC}	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply current		–0.5	6	V
V_I	Input voltage(2)		–0.5	6	V
V_O	Output voltage(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input-output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins P0-P3, VCC	±4000	V
			Pins SDA, SCL	±2000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC specification JS-002(2)	All pins	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input voltage	SCL, SDA, $\overline{INT}$, $\overline{RESET}$	0	5.5	V
		P0-P3(1)	0	5.5	
I_{OH}	High-level output current	P3-P0		–10	mA
I_{OL}	Low-level output current (V_{CC} > 1.8 V)	P3-P0		25	mA
	Low-level output current (V_{CC} ≤ 1.8 V)	P3-P0		15	mA
T_A	Ambient temperature		–40	125	°C
T_J	Junction temperature			125	°C

(1) When the internal pull up resistors are enabled, input voltages above V_{CC} will result in current flowing to VCC from the port.

6.4 Thermal Information

THERMAL METRIC[1]		TCA9537 DGS (VSSOP) 10-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	104.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = -18 mA	1.65 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising		V_I = V_{CC} or GND, I_O = 0			1.2	1.6	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		V_I = V_{CC} or GND, I_O = 0		0.75	1		V
V_{IH}	High-level input voltage	SDA,SCL		1.65 to 5.5 V	0.7 × V_{CC}			V
V_{IH}	High-level input voltage	P ports, $\overline{RESET}$		1.65 to 5.5 V	0.7 × V_{CC}			V
V_{IL}	Low-level input voltage	SDA,SCL		1.65 to 5.5 V			0.4 × V_{CC}	V
V_{IL}	Low-level input voltage	P ports, $\overline{RESET}$		1.65 to 5.5 V			0.3 × V_{CC}	V
V_{OH}	P-port high-level output voltage[1]		I_{OH} = -8 mA	1.65 V	1.2			V
				2.3 V	1.8			
				3 V	2.6			
				4.5 V	4.1			
				4.75 V	4.1			
			I_{OH} = -10 mA	1.65 V	1			
				2.3 V	1.7			
				3 V	2.5			
				4.5 V	4			
				4.75 V	4			
I_{OL}	Low-level output current	SDA	V_{OL} = 0.4 V	1.65 V to 5.5 V	20			mA
		P0-P3	V_{OL} = 0.5 V		8			
			V_{OL} = 0.7 V		10			
I_{OL}	Low-level output current	$\overline{INT}$	V_{OL} = 0.4 V	1.65 V to 5.5 V	4			mA
I_I	Input leakage current	P ports	V_I = V_{CC}	1.65 V to 5.5 V		0	±1	µA
			V_I = 5.5 V (T_A ≤ 105 °C)	0 V		0	±1	
			V_I = 5.5 V	0 V		0	±2	
			V_I = GND	1.65 V to 5.5 V		0	±1	

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_I	Input leakage current	SCL, SDA input leakage	$V_I = V_{CC}$ or GND	1.65 V to 5.5 V		0	±1	µA
I_I	Input leakage current	RESET input leakage	$V_I = V_{CC}$	1.65 V to 5.5 V		0	±1	µA
			V_I = GND			0	±1	
I_{CC}	Quiescent current	Operating mode	$V_I = V_{CC}$, I/O = inputs, f_{SCL} = 400 kHz, $t_r = t_f$ = 300 ns	5.5 V		22	40	µA
				3.6 V		11	20	
				2.7 V		8	10	
				1.95 V		5	8	
I_{CC}	Quiescent current	Operating mode	$V_I = V_{CC}$, I/O = inputs, f_{SCL} = 1 MHz, $t_r = t_f$ = 120 ns	5.5 V			100	µA
				3.6 V			40	
				2.7 V			25	
				1.95 V			15	
I_{CC}	Quiescent current	Standby mode	$V_I = V_{CC}$, I_O = 0, I/0 = inputs, f_{SCL} = 0 kHz	5.5 V		1.5	3.9	µA
				3.6 V		0.9	2.2	
				2.7 V		0.6	1.8	
				1.95 V		0.6	1.5	
C_I	Input pin capacitance	SCL	$V_I = V_{CC}$ or GND	1.65 V to 5.5 V		4	5	pF
C_{IO}	Input-output pin capacitance	SDA	$V_{IO} = V_{CC}$ or GND	1.65 V to 5.5 V		7	10	pF
		P port	$V_{IO} = V_{CC}$ or GND	1.65 V to 5.5 V		7	10	

(1) Each I/O must be externally limited to a maximum of 25 mA

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Device				
t_{READY}	Power on to start condition time	10		µs
$\overline{RESET}$				
t_w	Reset pulse duration	30		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset	400		ns

6.7 I²C Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I²C Bus - Standard Mode				
f_{scl}	I²C clock frequency	0	100	kHz
t_{sch}	I²C clock high time	4		µs
t_{scl}	I²C clock low time	4.7		µs
t_{sp}	I²C spike time		50	ns
t_{sds}	I²C serial-data setup time	250		ns
t_{sdh}	I²C serial-data hold time	0		ns

6.7 I²C Bus Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capactive load			400	pF
I²C Bus - Fast Mode					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	20 × (V_{CC} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capactive load			400	pF
I²C Bus - Fast Mode Plus					
f_{scl}	I²C clock frequency		0	1000	kHz
t_{sch}	I²C clock high time		0.26		µs
t_{scl}	I²C clock low time		0.5		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		50		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			120	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5 V)	120	ns

6.7 I²C Bus Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t_{ocf}	I²C output fall time	10-pF to 550-pF bus	20 × (V_{CC} / 5.5 V)	120	ns
t_{buf}	I²C bus free time between stop and start		0.5		µs
t_{sts}	I²C start or repeated start condition setup		0.26		µs
t_{sth}	I²C start or repeated start condition hold		0.26		µs
t_{sps}	I²C stop condition setup		0.26		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.45	µs
C_b	I²C bus capactive load			550	pF

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$			4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$			4	µs
t_{pv}	Output data valid; For V_{CC} ≥ 2.3 V	SCL	P port			200	ns
	Output data valid; For V_{CC} < 2.3 V					400	ns
t_{ps}	Input data setup time	P port	SCL	100			ns
t_{ph}	Input data hold time	P port	SCL	300			ns

6.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

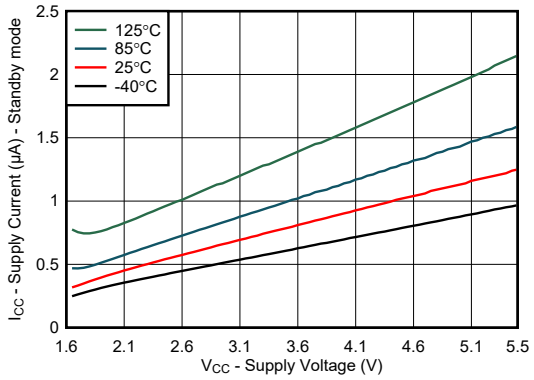


図 6-1. Supply Current (Standby) vs Supply Voltage for Different Temperature (T_A)

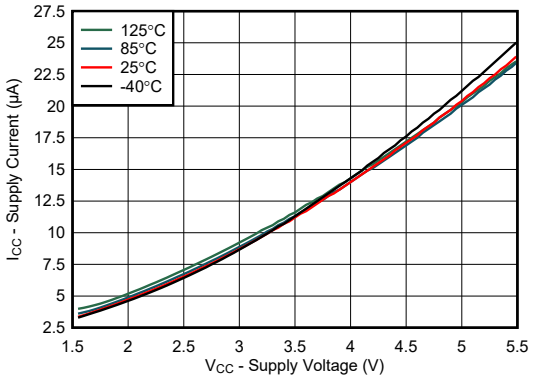


図 6-2. Supply Current vs Supply Voltage for Different Temperature (T_A)

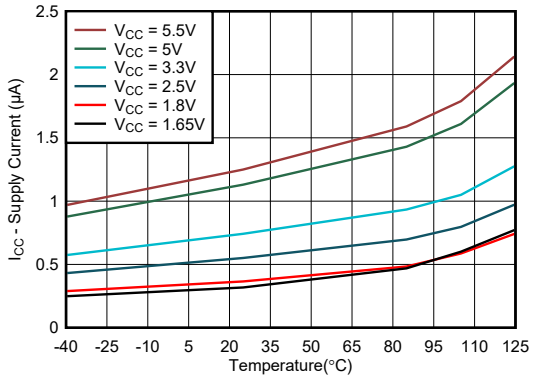


図 6-3. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

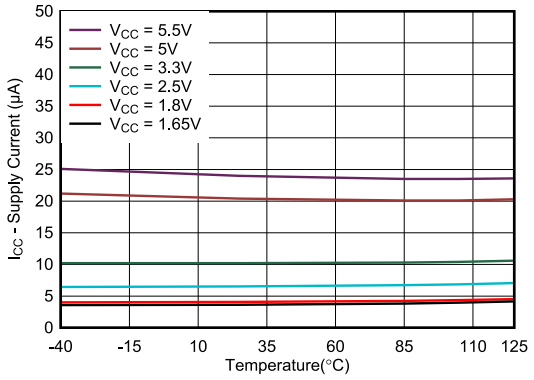


図 6-4. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

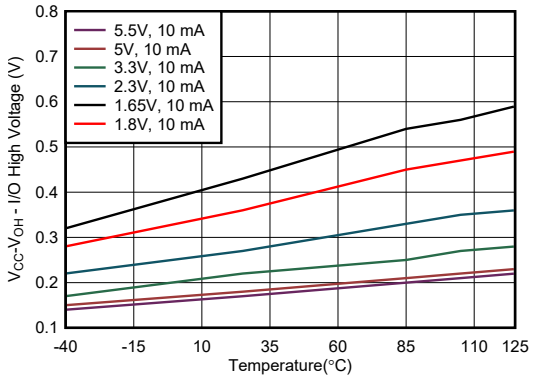


図 6-5. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

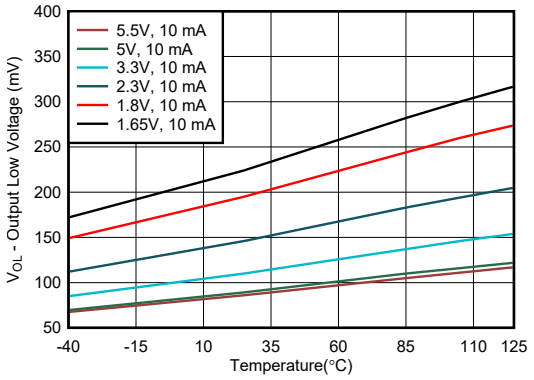


図 6-6. V_{OL} vs Temperature for Different V_{CC}

6.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

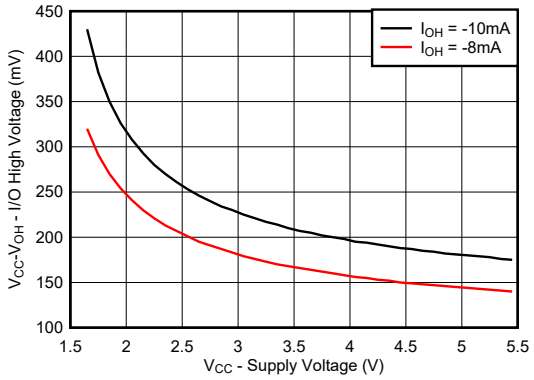


図 6-7. V_{CC} – V_{OH} Voltage at 25°C for Different V_{CC}

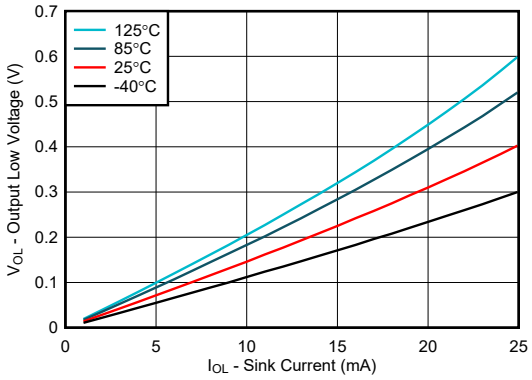


図 6-8. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.3 V

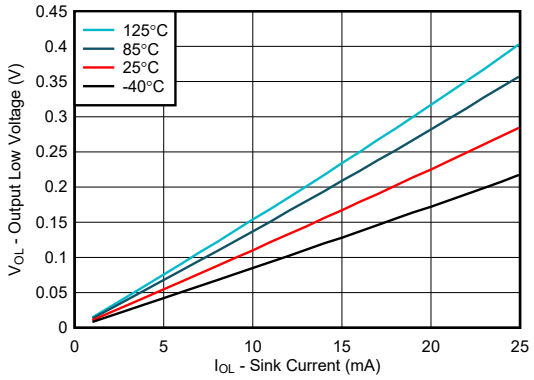


図 6-9. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

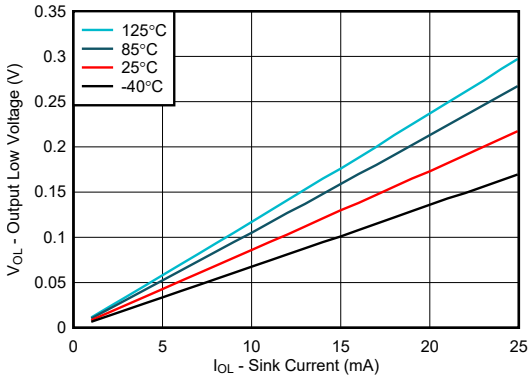


図 6-10. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

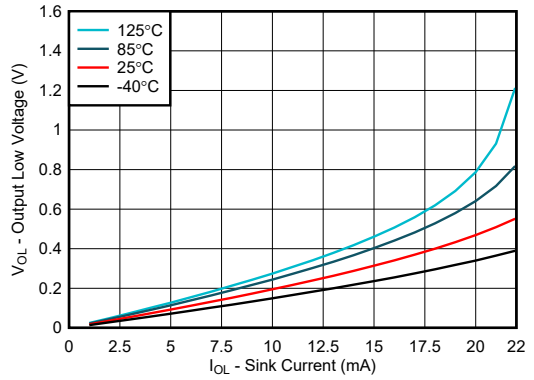


図 6-11. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

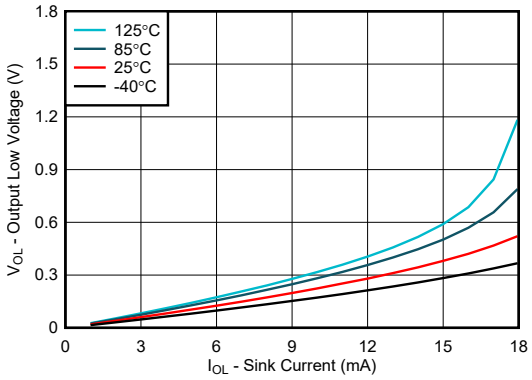
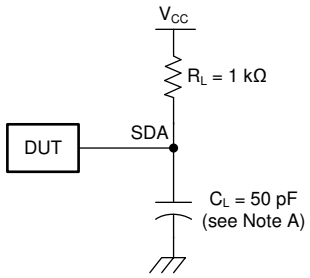
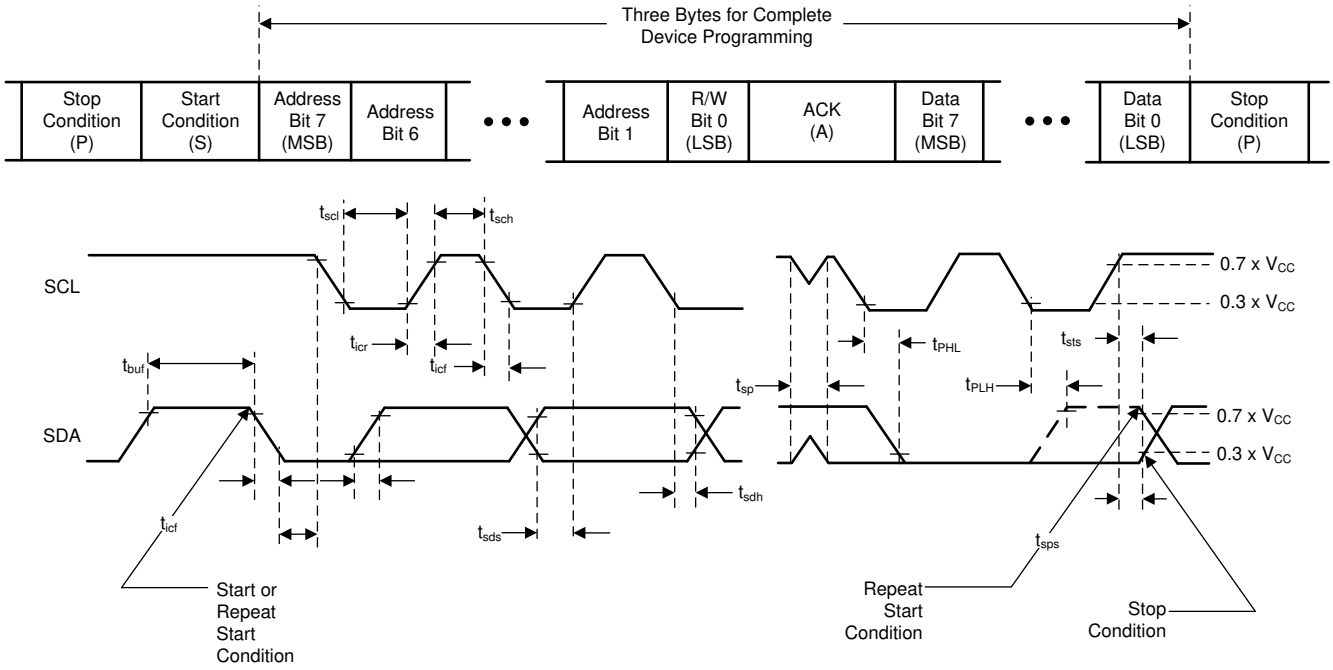


図 6-12. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

7 Parameter Measurement Information



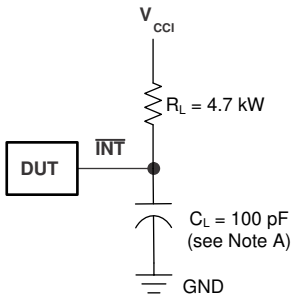
SDA LOAD CONFIGURATION



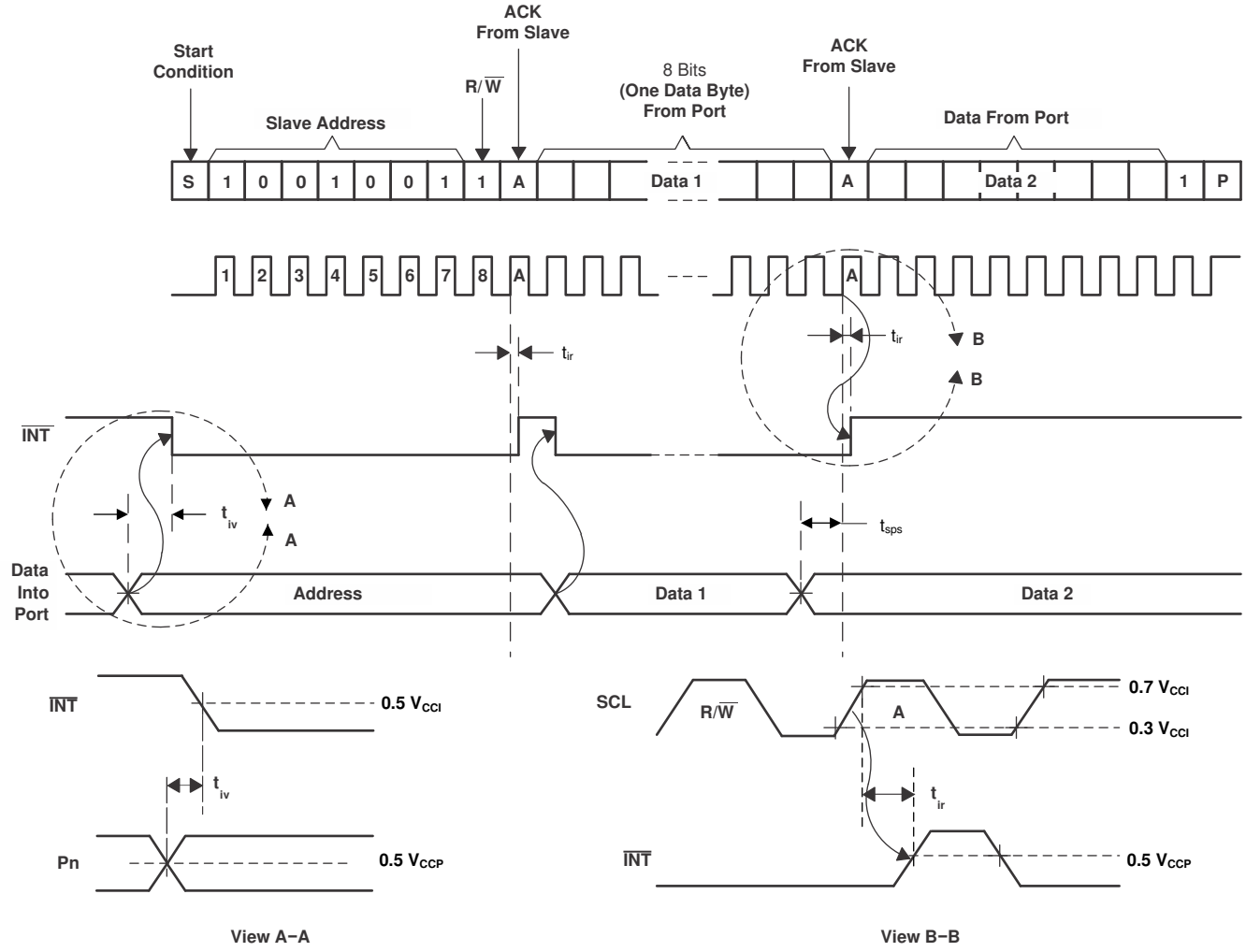
VOLTAGE WAVEFORMS

A. C_L include probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

図 7-1. I²C Interface Load Circuit and Voltage Waveforms

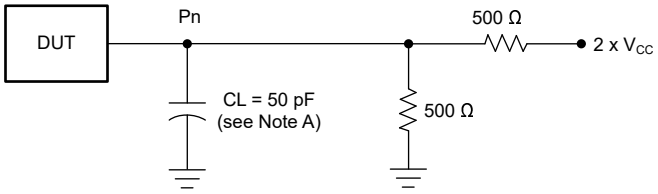


INTERRUPT LOAD CONFIGURATION

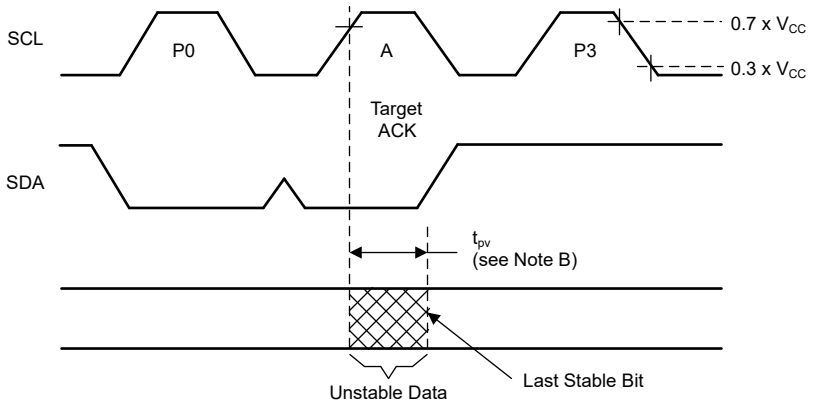


A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

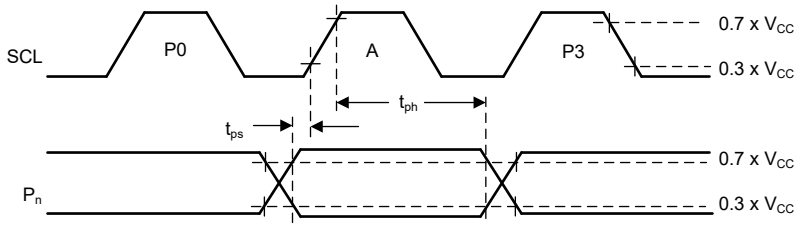
図 7-2. Interrupt Load Circuit And Voltage Waveforms



P-PORT LOAD CONFIGURATION



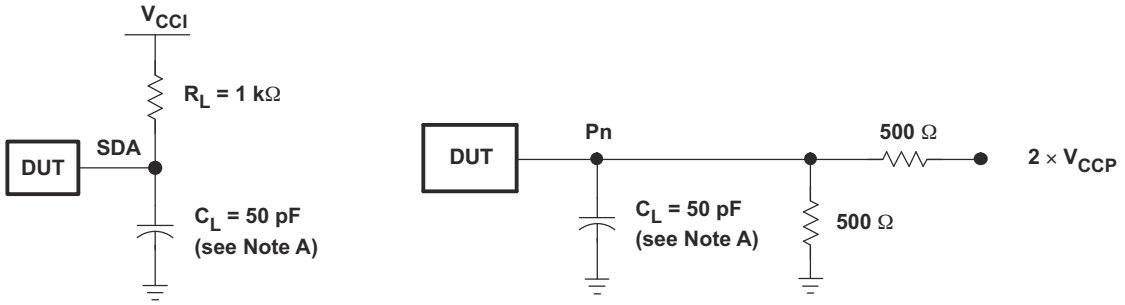
WRITE MODE (R/W = 0)



READ MODE (R/W = 1)

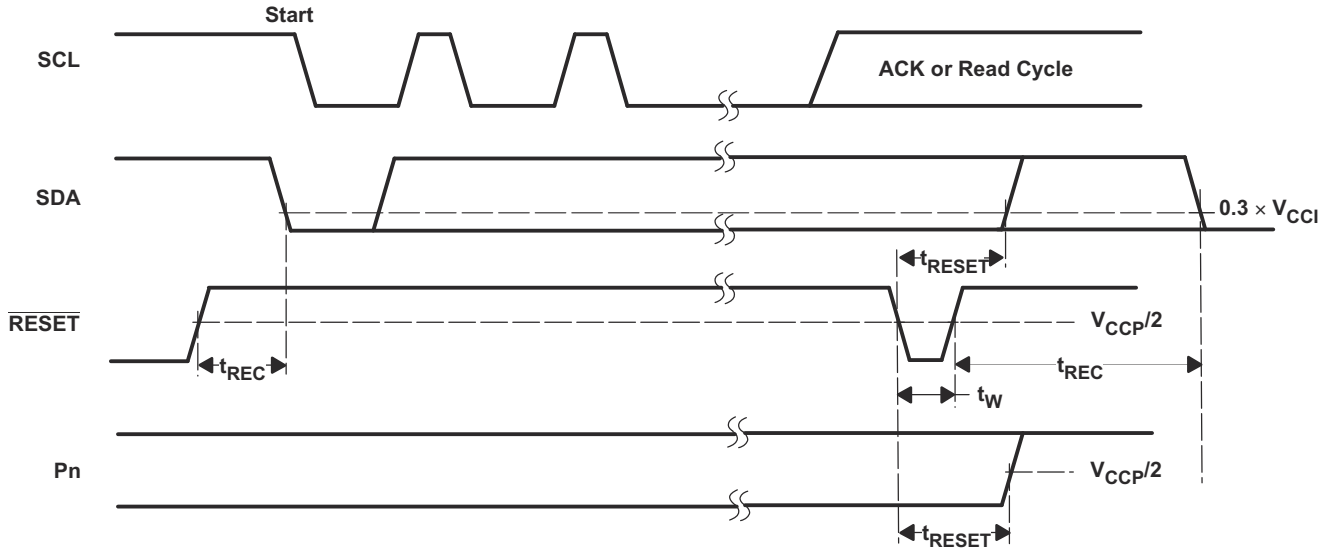
A. C_L include probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 7-3. P-Port Load Circuit and Voltage Waveforms



SDA LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

図 7-4. Reset Load Circuits And Voltage Waveforms

8 Detailed Description

8.1 Overview

The TCA9537 device is a 4-bit I/O expander for the I^2C bus and is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface.

The TCA9537 consists of a configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller.

The TCA9537 open-drain interrupt output ($\overline{INT}$) is activated when any input differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed.

The system processor can reset the TCA9537 in the event of a timeout or other improper operation by using an I^2C soft reset command, which puts the registers in their default state, or with the use of the $\overline{RESET}$ pin.

The device outputs (latched) have high-current drive capability for directly driving LEDs.

8.2 Functional Block Diagram

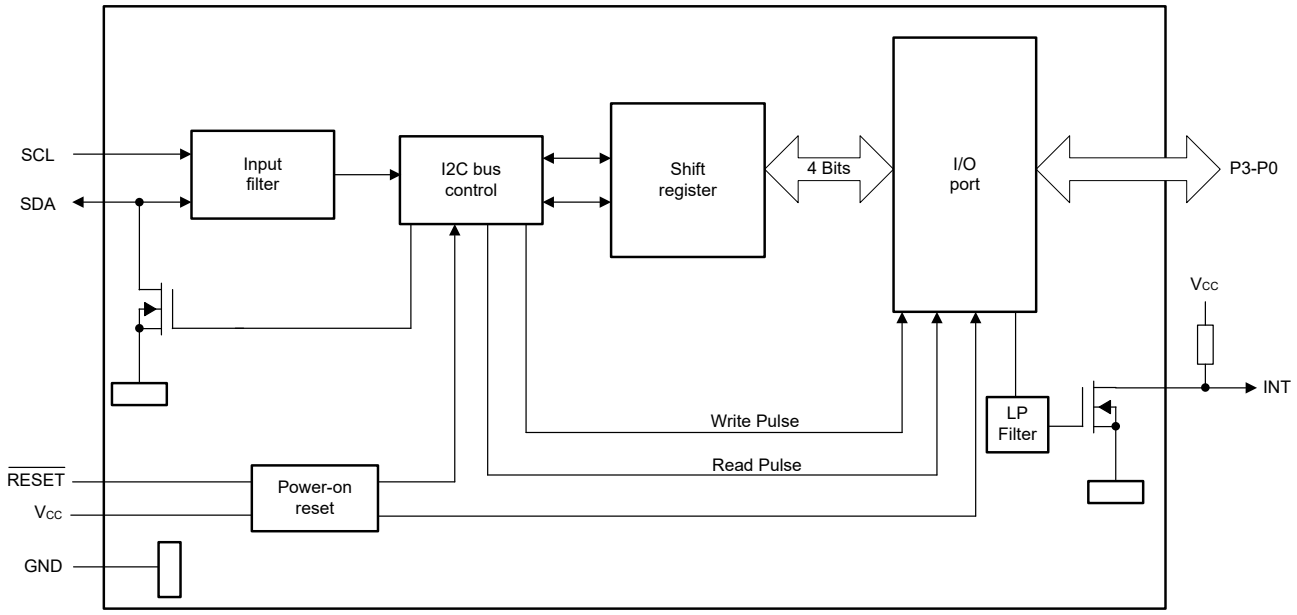


図 8-1. Logic Diagram

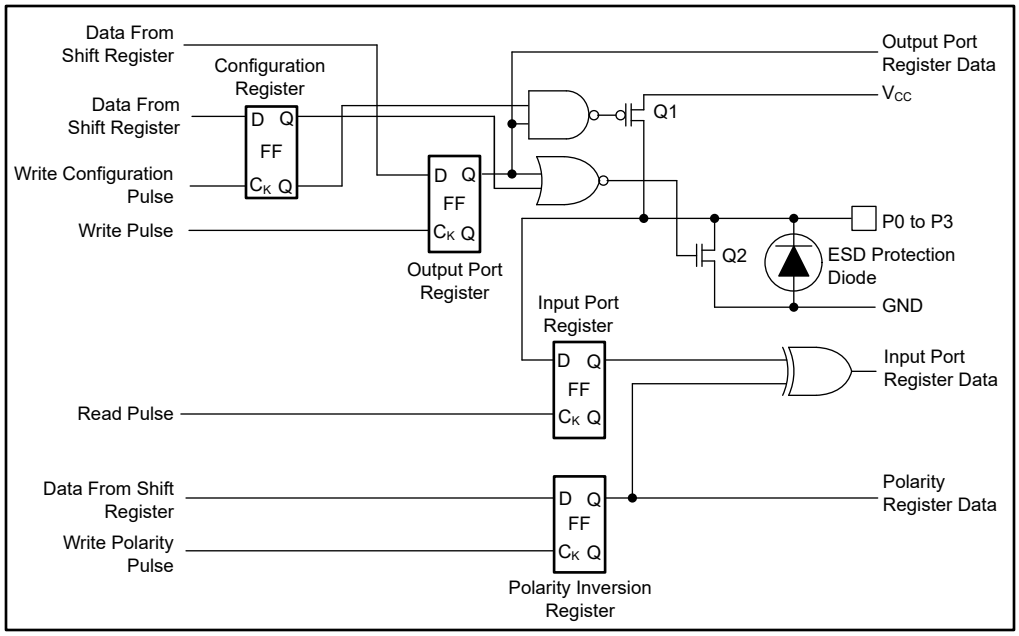


図 8-2. Simplified Schematic Of P0 - P3

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.3.2 Interrupt ($\overline{INT}$) Output

The TCA9537 has a dedicated $\overline{INT}$ output.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the $\overline{INT}$ is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

$\overline{INT}$ has an open-drain structure and requires a pull-up resistor to V_{CC} of moderate value (typically about 10 kΩ).

8.3.3 $\overline{RESET}$ Input

The $\overline{RESET}$ input can be asserted to reset the system while keeping the V_{CC} at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of t_w. The TCA9537 registers and I^2C/SMBus state machine are changed to their default states once $\overline{RESET}$ is low (0). Once $\overline{RESET}$ is high (1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to V_{CC} if no active connection is used.

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the device in a reset condition until V_{CC} has reached V_{POR}. At that time, the reset condition is released and the TCA9537 registers and I^2C/SMBus state machine initialize to their default states. See セクション 10.1 for more details.

8.4.2 Powered-Up

When power has been applied to V_{CC} above V_{PORR}, and the POR has taken place, the device is in a functioning mode. In this state, the device is ready to accept any incoming I^2C requests and is monitoring for changes on the input ports.

8.5 Programming

8.5.1 I^2C Interface

The TCA9537 has a standard bidirectional I^2C interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the I^2C bus has a specific device address to differentiate between other target devices that are on the same I^2C bus. Many target devices require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see *Understanding the I^2C Bus* application report, SLVA704.

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^2C lines. For further details, see *I^2C Pull-up Resistor Calculation* application report, SLVA689. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition. See *Interface Definition*.

図 8-3 and 図 8-4 show the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
   - Controller-transmitter sends a START condition and addresses the target-receiver.
   - Controller-transmitter sends data to target-receiver.
   - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
   - Controller-receiver sends a START condition and addresses the target-transmitter.
   - Controller-receiver sends the requested register to read to target-transmitter.
   - Controller-receiver receives data from the target-transmitter.
   - Controller-receiver terminates the transfer with a STOP condition.

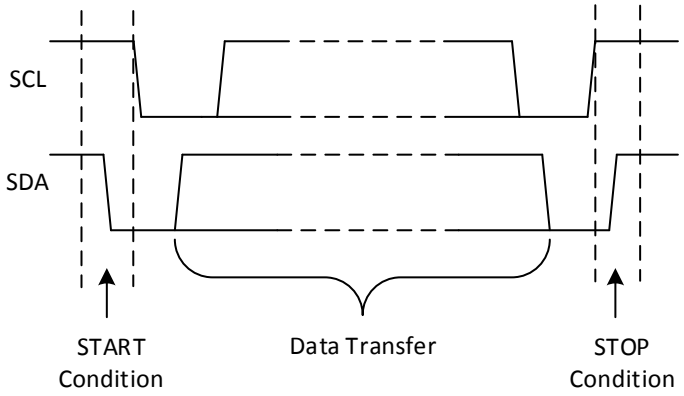


図 8-3. Definition of Start and Stop Conditions

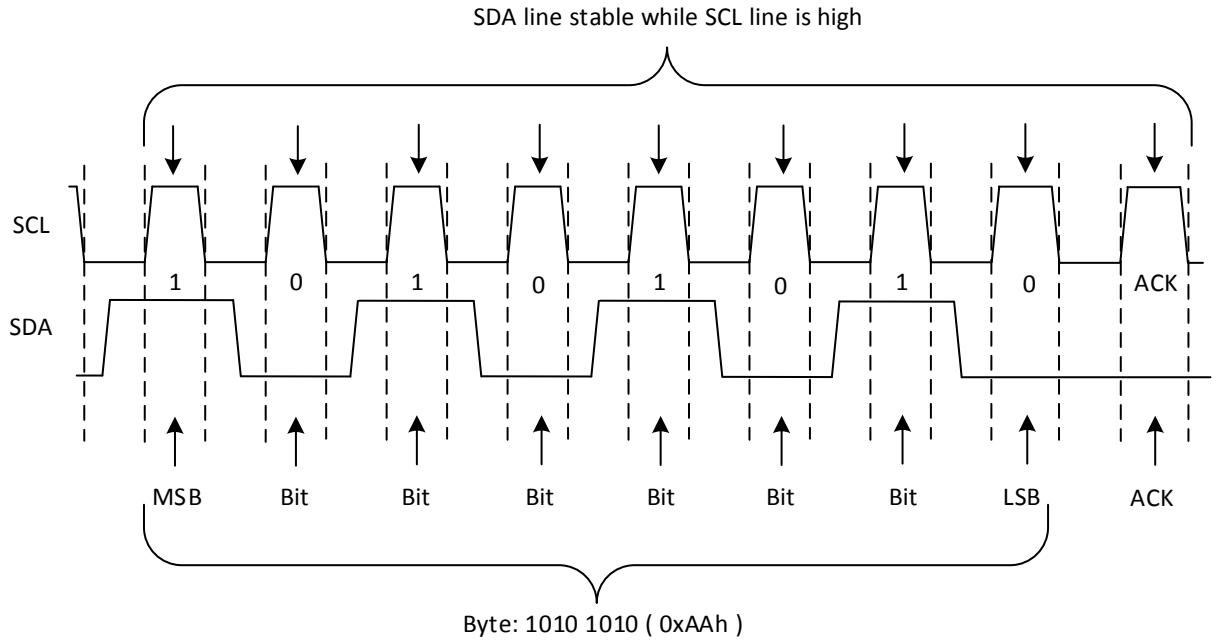


図 8-4. Bit Transfer

8.5.1.1 Writes

To write on the I²C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/ $\overline{W}$ bit) set to 0, which signifies a write. After the target sends the acknowledge bit, the controller then sends the register address of the register to which it wishes to write. The target acknowledges again, letting the controller know it is ready. After this, the controller starts sending the register data to the target until the controller has sent all the data necessary (which is sometimes only a single byte), and the controller terminates the transmission with a STOP condition.

See the *Control Register and Command Byte* section to see list of the TCA9537 internal registers and a description of each one.

図 8-5 shows an example of writing a single byte to a target register.

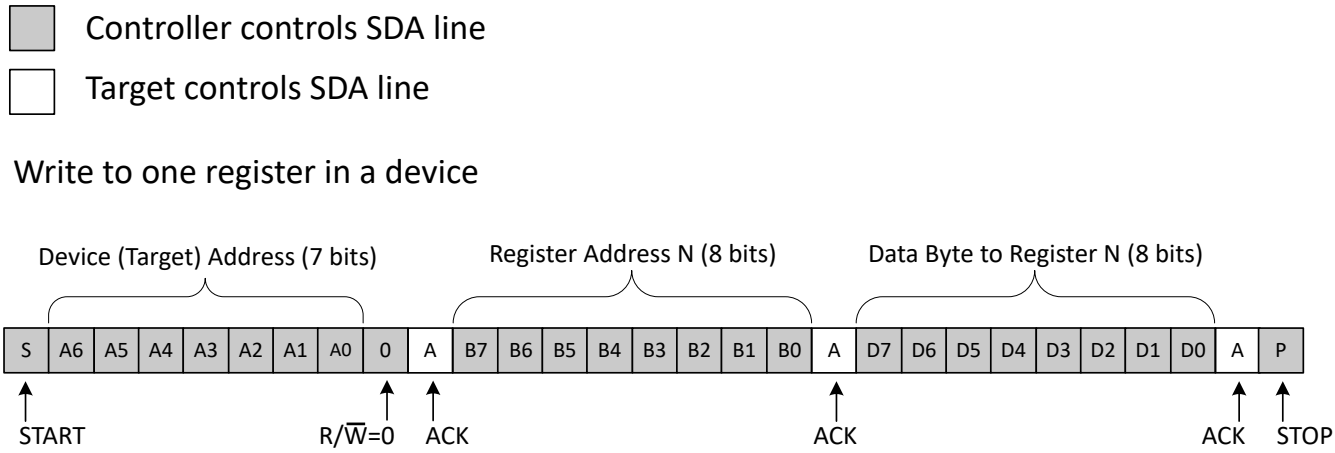


図 8-5. Write to Register

図 8-6 shows the Write to Output Port Registers.

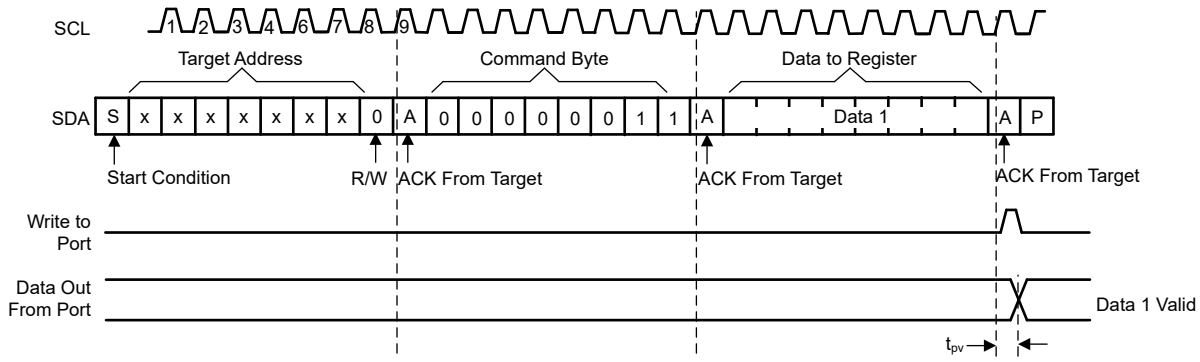


図 8-6. Write to Output Port Register

8.5.1.2 Reads

The bus controller first must send the TCA9537 address with the LSB set to a logic 0 (see 表 8-1 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA9537 (see 図 8-8). The command byte does not increment automatically. If multiple bytes are read, data from the specified command byte/register is going to be continuously read.

図 8-7 shows an example of reading a single byte from a target register.

Controller controls SDA line

Target controls SDA line

Read from one register in a device

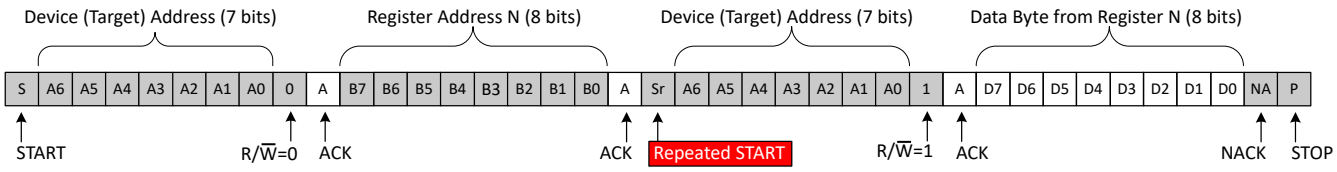
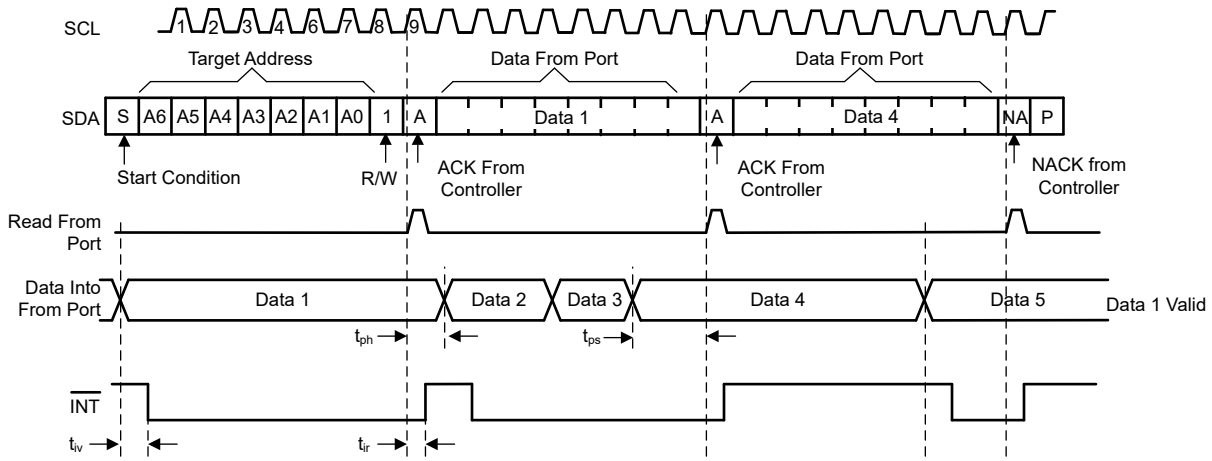


図 8-7. Read from Register

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte, additional bytes may be read, but the same register specified by the command byte is read.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus controller must not acknowledge the data.



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from the P port (see 図 8-7 for these details).

図 8-8. Read Input Port Register

8.5.2 Software Reset Call

The Software Reset call is a command send from the controller on the I^2C bus that instructs all devices that support the command to be reset to power-up values. In order for it to function as expected, the I^2C bus must be functional and no devices can be hanging the bus.

The Software Reset Call is defined as the following steps:

1. A START condition is sent by the I^2C bus controller.
2. The address used is the reserved General Call I^2C bus address '0000 000' with the R/$\overline{W}$ bit set to 0. The byte sent is 0x00.
3. Any devices supporting the General Call functionality will ACK. If the R/$\overline{W}$ bit is set to 1 (read), the device will NACK.
4. Once the General Call address is acknowledged, the controller sends only 1 byte of data equal to 0x06. If the data byte is any other value, the device will NOT acknowledge or reset. If more than 1 byte is sent, no more bytes will be acknowledged, and the device will ignore this I^2C message, considering it invalid.
5. After the 1 byte of data (0x06) is sent, the controller sends a STOP condition to end the Software Reset sequence. A repeated START condition will be ignored by the device, and no reset is performed.

Once the above steps are completed successfully, the device performs a reset. This clears all register values back to power-on defaults. All P-ports are configured as inputs.

8.6 Register Maps

8.6.1 Device Address

表 8-1 shows the fixed 7-bit address of the device. Note that I^2C uses a 7-bit address with a 1-bit READ/$\overline{WRITE}$ bit for the LSB.

表 8-1. Device Address

Device	A6	A5	A4	A3	A2	A1	A0	Hex	Decimal
TCA9537	1	0	0	1	0	0	1	0x49	73

The last bit of the 8-bit address byte defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

8.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the TCA9537. This data byte states the operation (read or write) and the internal register (Input, Output, Polarity Inversion, or Configuration) that sre affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

表 8-2. Command Byte

COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
0x00	Input Port	Read byte	1111 XXXX
0x01	Output Port	Read/write byte	1111 1111
0x02	Polarity Inversion	Read/write byte	0000 0000
0x03	Configuration	Read/write byte	1111 1111

8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level. See 表 8-3.

Before a read operation, a write transmission is sent with the command byte to instruct the I^2C device that the Input Port register will be accessed next.

表 8-3. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
	Not Used							
DEFAULT	1	1	1	1	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See 表 8-4.

表 8-4. Register 0x01 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained. See 表 8-5.

表 8-5. Register 0x02 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
	Not Used							
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See 表 8-6.

表 8-6. Register 0x03 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

9 Application Information Disclaimer

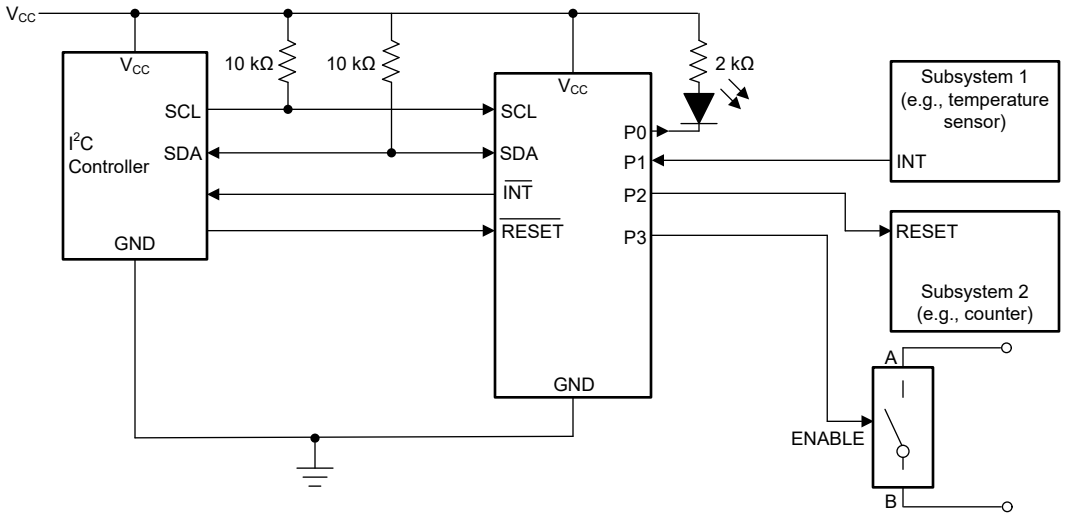
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

This section discusses a typical application in which the device is used to both handle an interrupt input, and output several control signals.



A. P0, P2, and P3 are configured as outputs.
B. P1 is configured as an input.

図 9-1. Typical Application

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in セクション 9.2. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off. 図 9-2 shows a high-value resistor in parallel with the LED. 図 9-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

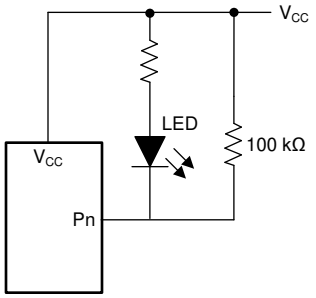


図 9-2. High-Value Resistor in Parallel with the LED

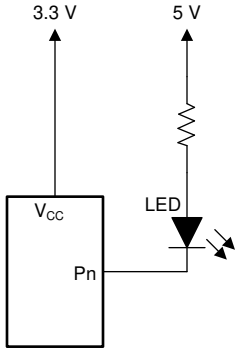


図 9-3. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in 式 1:

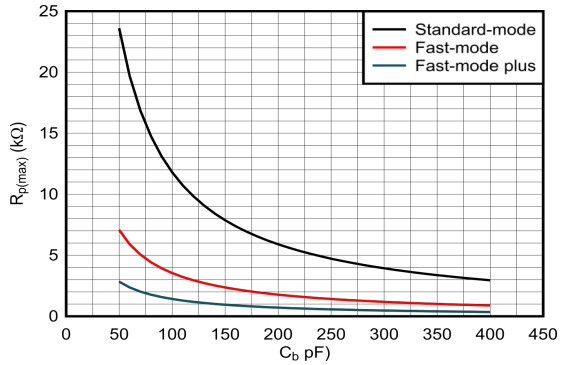
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in 式 2:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

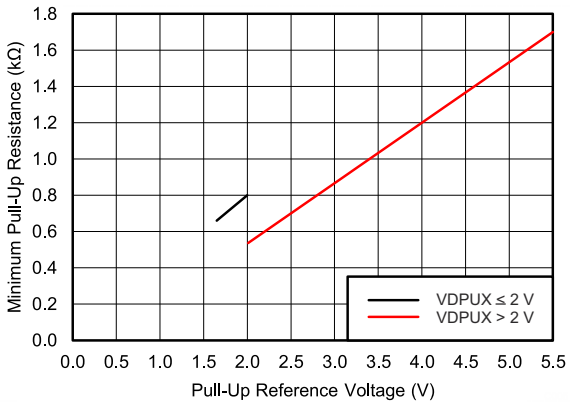
The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9537, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

9.2.3 Application Curves



Standard mode (f_{SCL} = 100 kHz, t_r = 1 µs)
Fast mode (f_{SCL} = 400 kHz, t_r = 300 ns)
Fast mode plus (f_{SCL} = 1000 kHz, t_r = 120 ns)

図 9-4. Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 x V_{DPUX} , I_{OL} = 2 mA when V_{DPUX} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

図 9-5. Minimum Pullup Resistance ($R_{p(min)}$) vs Pullup Reference Voltage (V_{DPUX})

10 Power Supply Recommendations

10.1 Power-On Reset

In the event of a glitch or data corruption, the TCA9537 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in and 図 10-1.

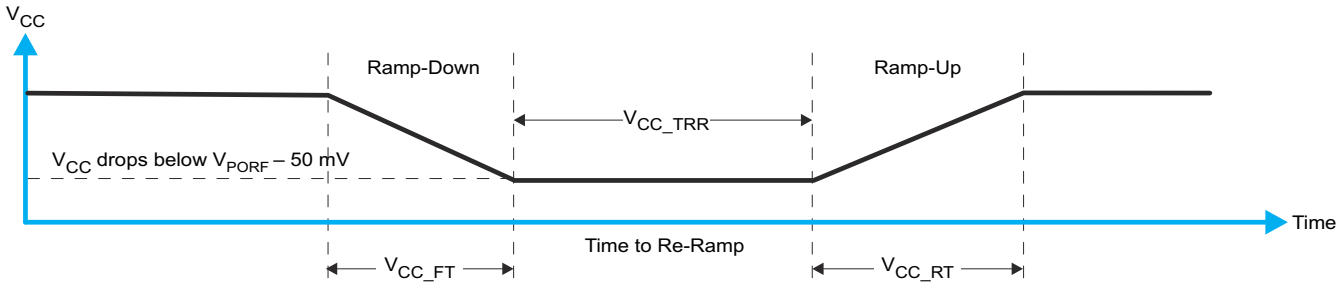


図 10-1. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

表 10-1 specifies the performance of the power-on reset feature for the device for both types of power-on reset.

表 10-1. Recommended Supply Sequencing And Ramp Rates

PARAMETER(1)			MIN	MAX	UNIT
V_{CC_FT}	Fall rate	See 図 10-1	1		ms
V_{CC_RT}	Rise rate	See 図 10-1	0.1		ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV or when V_{CC} drops to GND)	See 図 10-1	2		µs
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW} = 1 µs	See 図 10-2		1.2	V
V_{CC_GW}	Glitch width that does not cause a functional disruption when V_{CC_GH} = 0.5 × V_{CC} (For VCC > 3 V)	See 図 10-2		10	µs

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. 図 10-2 and 表 10-1 provide more information on how to measure these specifications.

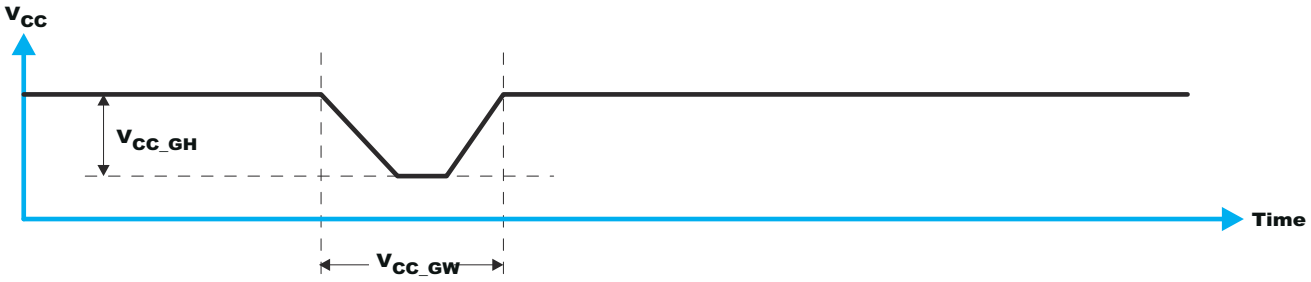


図 10-2. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 図 10-3 and 表 10-1 provide more details on this specification.

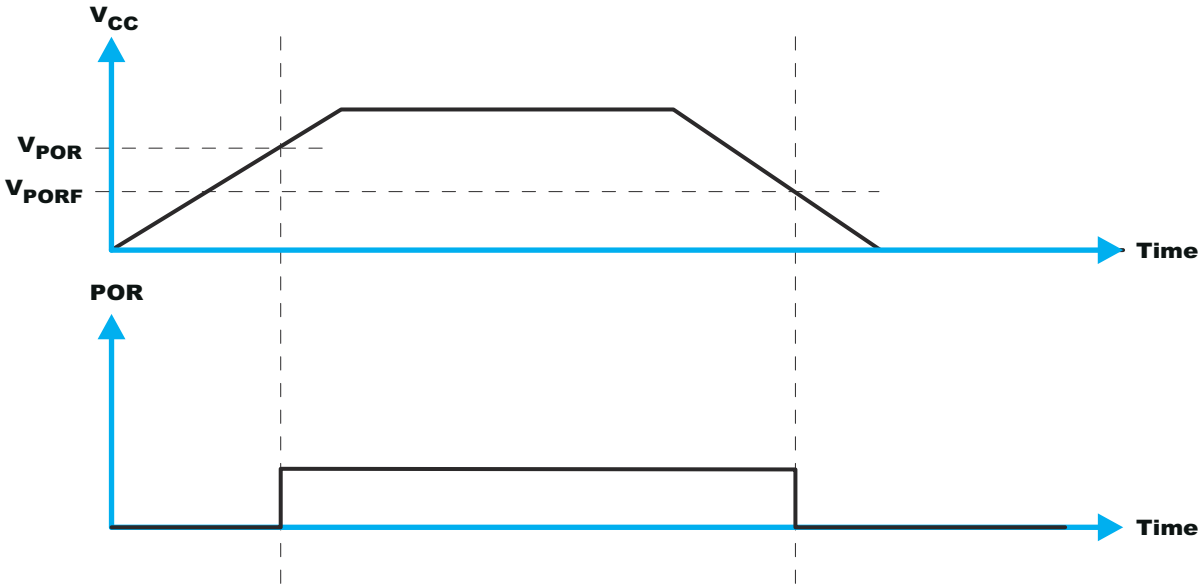


図 10-3. V_{POR}

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9537, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9537 as possible.

For the layout example provided, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a 4-layer board is preferable for boards with higher density signal routing. On a 4-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to VCC or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated.

11.2 Layout Example

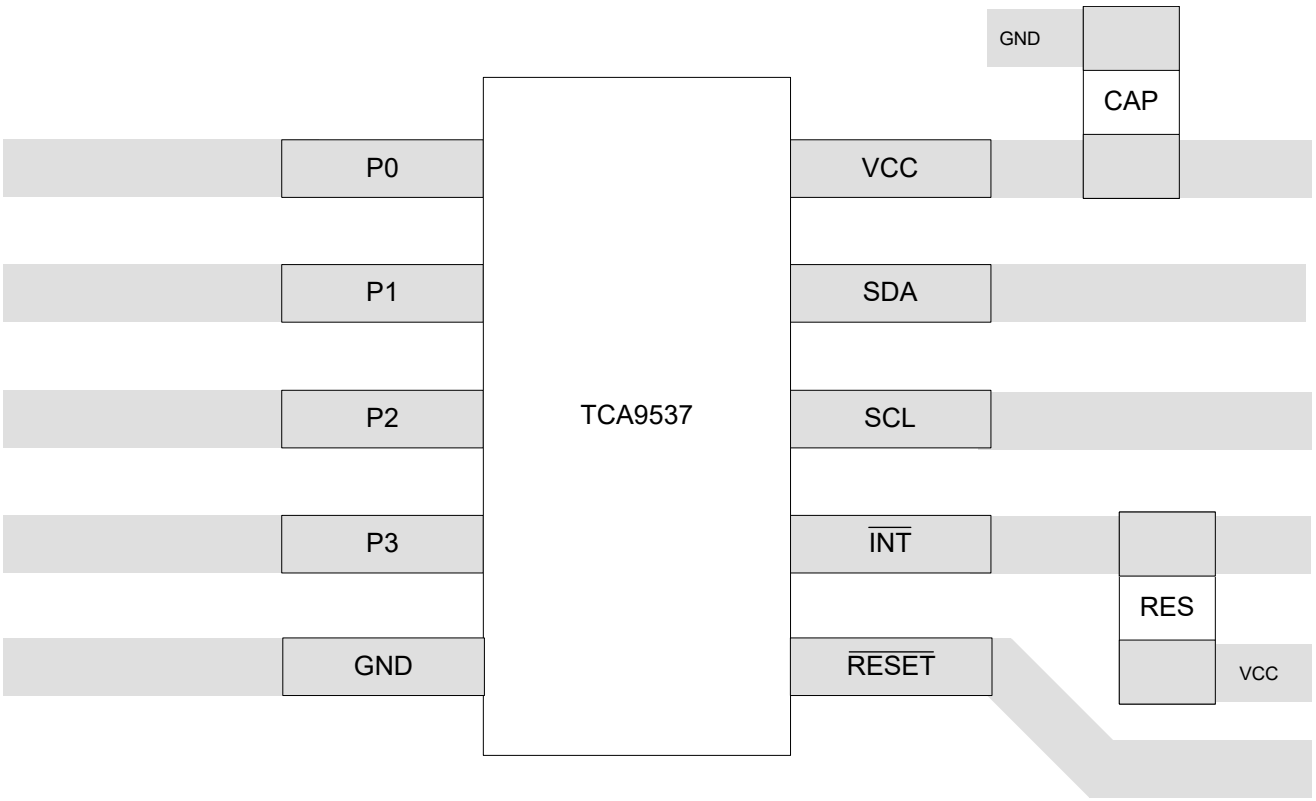


図 11-1. Layout Example (DGS)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *I2C Bus Pull-Up Resistor Calculation*
- *Maximum Clock Frequency of I2C Bus Using Repeaters*
- *Introduction to Logic*
- *Understanding the I2C Bus*
- *Choosing the Correct I2C Device for New Designs*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9537DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2I3T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

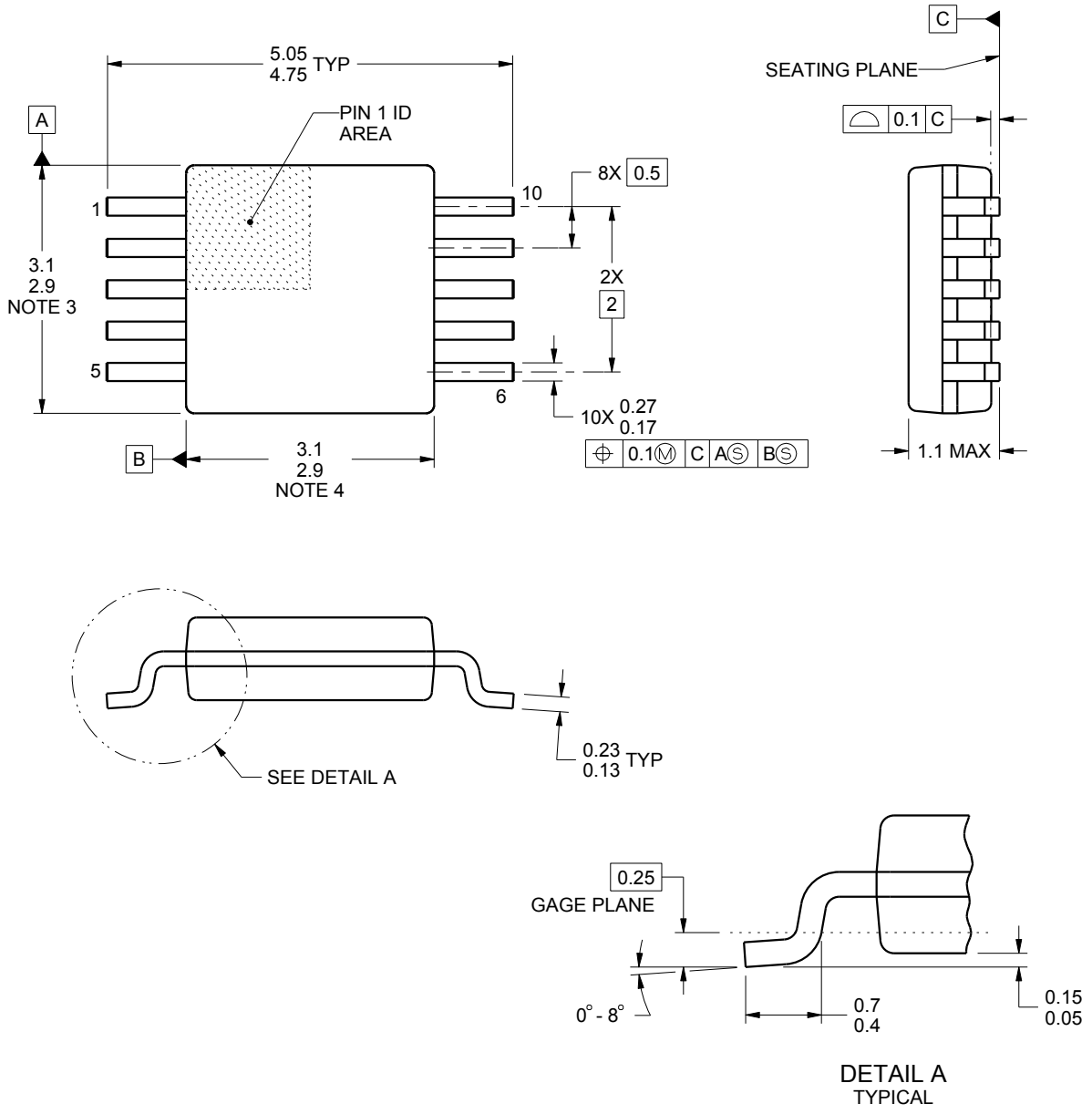
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DGS0010A

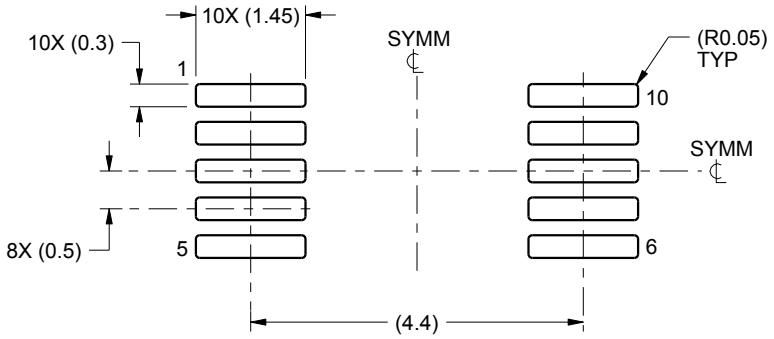
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

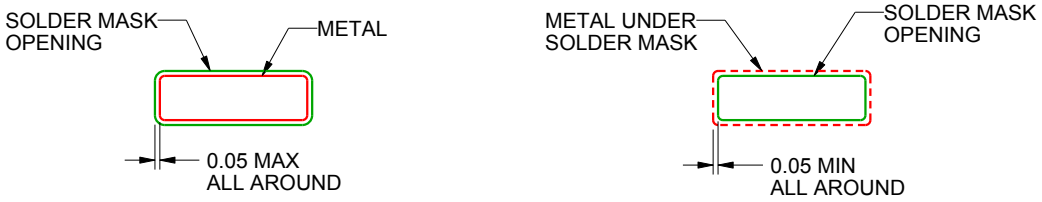


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

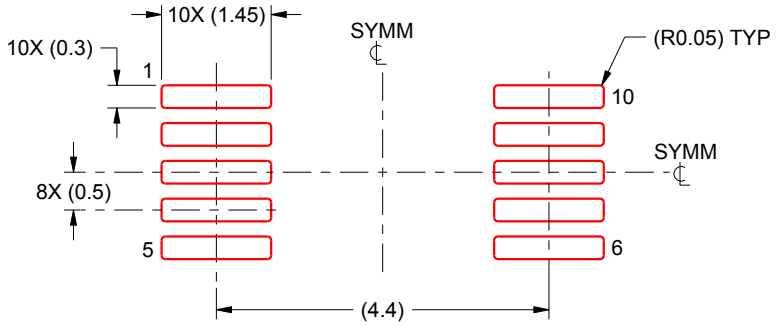


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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