TAS5751M - EQおよび3バンドAGL付きのデジタル入力オーディオ・パワーアンプ

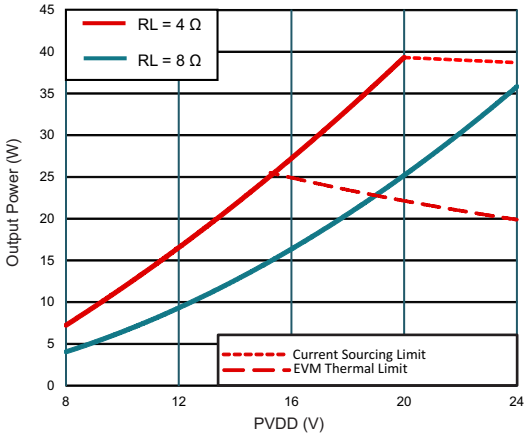
1 特長

- **オーディオ入力/出力**
  - 1つのステレオ・シリアル・オーディオ入力
  - 44.1kHzおよび48kHzのサンプル・レートをサポート(LJ/RJ/I²S)
  - 3線式I²Sモードをサポート(MCLK不要)
  - オーディオ・ポート速度の自動検出
  - BTLおよびPBTL構成をサポート
  - 10% THD+NでP$_{OUT}$ = 25W
    - PVDD = 20V、8Ω、1kHz
- **オーディオ/PWM処理**
  - 独立したチャネルのボリューム制御、ゲインは24dBからミュートまで0.125dB刻み
  - プログラム可能な3バンドの自動ゲイン制限(AGL)
  - 20のプログラム可能なバイクワッド・フィルタにより、スピーカーの特性補償や、他のオーディオ処理機能を実現
- **全般的な仕様**
  - 106-dB SNR、Aウェイト、フルスケール(0dB)を基準
  - 2つのアドレスを持つI²Cシリアル制御インターフェイス
  - 熱、短絡、低電圧からの保護
  - 高効率(最高90%)
  - AD、BD、および3値変調
  - PWMレベル・メーター

2 アプリケーション

- LCD TV、LED TV
- 低コストのオーディオ機器

電力とPVDDとの関係



3 概要

TAS5751Mデバイスは高効率のデジタル入力オーディオ・アンプで、ブリッジ結合負荷(BTL)として構成されているステレオ・スピーカーの駆動用です。パラレル・ブリッジ結合負荷(PBTL)入力は、単一の低インピーダンス負荷へのパラレル出力を駆動することにより、大電力を生成できます。1系統のシリアル・データ入力を備え、最大2つの独立したオーディオ・チャネルを処理でき、ほとんどのデジタル・オーディオ・プロセッサおよびMPEGデコーダとシームレスに統合できます。このデバイスは、広い範囲の入力データおよびデータ速度に対応できます。これらのチャネルは、完全にプログラム可能なデータ・パスを通して内部スピーカー・ドライバにルーティングされます。

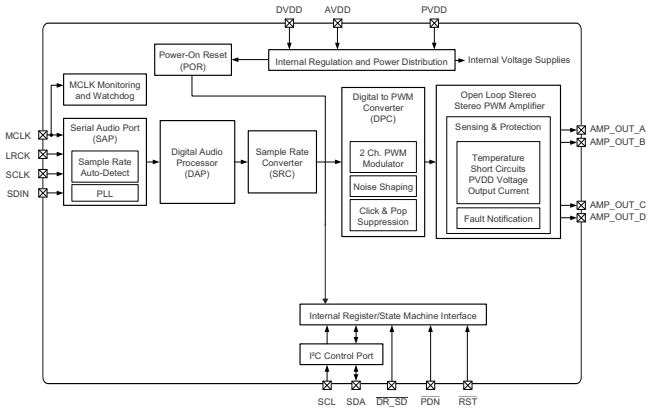
TAS5751Mデバイスはスレーブ専用のデバイスで、クロックはすべて外部ソースから供給されます。TAS5751Mデバイスは、入力サンプル・レートに応じて、384kHz～288kHzのスイッチング・レートのPWMキャリアで動作します。オーバーサンプリングと4次ノイズ・シェーパの組み合わせにより、平坦なノイズ・フロアと、20Hz～20kHzの優れたダイナミック・レンジが得られます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TAS5751M	HTSSOP(48)	12.50mm×6.10mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ブロック概略図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (March 2016) から **Revision B** に変更 **Page**

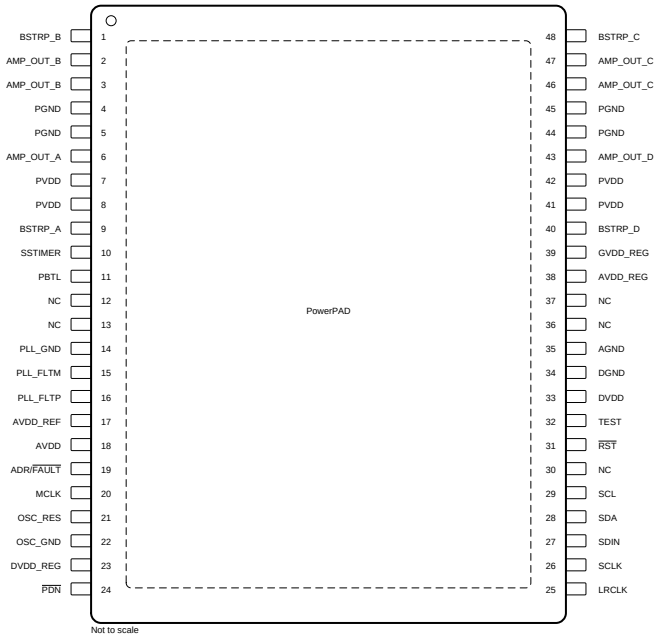
- Added PVDD to the *Absolute Maximum Ratings* table ... 5
- Moved the units values From the MAX value column to the UNITS column in the *I²C Interface Timing Requirements* table ... 8
- Changed text "Multiplex channel 2 to AMP_OUT_D" To: Multiplex $\overline{\text{channel 2}}$ to AMP_OUT_D" in the Functions column of Table 21 ... 49

2016年3月 発行のものから更新 **Page**

- 製品プレビューから量産データ・リリースに移行 ... 1

5 Pin Configuration and Functions

DCA Package
48-Pin HTSSOP With PowerPAD™
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ADR/FAULT	19	DI/DO	Dual function terminal which sets the LSB of the I²C Address to 0 if pulled to GND, 1 if pulled to AVDD. Also, if configured to be a fault output by the methods described in the *Fault Indication* section, this terminal will be pulled low when an internal fault occurs.
AGND	35	P	Ground reference for analog circuitry (NOTE: This terminal should be connected to the system ground)
AMP_OUT_A	6	AO	Speaker amplifier outputs
AMP_OUT_B	2		
	3		
AMP_OUT_C	46		
	47		
AMP_OUT_D	43		
AVDD	18	P	Power supply for internal analog circuitry
AVDD_REF	17	P	Internal power supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
AVDD_REG	38	P	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
BSTRP_A	9	P	Connection points to for the bootstrap capacitors, which are used to create a power supply for the gate drive for the high-side device
BSTRP_B	1		
BSTRP_C	48		
BSTRP_D	40		
DGND	34	P	Ground reference for digital circuitry (NOTE: This terminal should be connected to the system ground)
DVDD	33	P	Power supply for the internal digital circuitry

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DVDD_REG	23	P	Voltage regulator derived from DVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
GVDD_REG	39	P	Voltage regulator derived from PVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
LRCLK	25	DI	Word select clock for the digital signal that is active on the input data line of the serial port
MCLK	20	DI	Master clock used for internal clock tree and sub-circuit/state machine clocking
NC(2)	12	P	Not connected inside the device (all "no connect" terminals should be connected to system ground)
	13		
	30		
	36		
	37		
OSC_GND	22	P	Ground reference for oscillator circuitry (NOTE: These terminals should be connected to the system ground)
OSC_RES	21	AO	Connection point for precision resistor used by internal oscillator circuit. Details for this resistor are shown in the *Typical Applications* section
PBTL	11	DI	Places the power stage in BTL mode when pulled low, or in PBTL mode when pulled high
$\overline{\text{PDN}}$	24	DI	Places the device in power down when pulled low
PGND	4	—	Ground reference for power device circuitry (NOTE: This terminal should be connected to the system ground)
	5		
	44		
	45		
PLL_FLTM	15	AO	Negative connection point for the PLL loop filter components
PLL_FLTP	16	AO	Positive connection point for the PLL loop filter components
PLL_GND	14	P	Ground reference for PLL circuitry (NOTE: This terminal should be connected to the system ground)
PVDD	7	P	Power supply for internal power circuitry
	8		
	41		
	42		
$\overline{\text{RST}}$	31	DI	Places the devices in reset when pulled low
SCL	29	DI	I²C serial control port clock
SCLK	26	DI	Bit clock for the digital signal that is active on the input data line of the serial data port
SDA	28	DI/DO	I²C serial control port data
SDIN	27	DI	Data line to the serial data port
SSTIMER	10	AO	Connection point for the capacitor that is used by the ramp timing circuit, as described in the *SSTIMER Pin Functionality* section
TEST	32	—	Used by TI for testing during device production (NOTE: This terminal should be connected to system ground)
PowerPAD	—	P	Exposed metal pad on the underside of the device, which serves as an electrical connection point for ground as well as a heat conduction path from the device into the board (NOTE: This terminal should be connected to ground through a land pattern defined in the *Mechanical Data* section)

(2) Although these pins are not connected internally, optimum thermal performance is realized when these pins are connected to the ground plane. Doing so allows copper on the PCB to fill up to and including these pins, providing a path for heat to conduct away from the device and into the surrounding PCB area.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	DVDD, AVDD, DR_VDD	–0.3	3.6	V
	PVDD	–0.3	30	
Input voltage	3.3-V digital input	–0.5	DVDD +. 0.5	V
	5-V tolerant(2) digital input (except MCLK)	–0.5	DVDD + 2.5(3)	
	5-V tolerant MCLK input	–0.5	AVDD + 2.5(3)	
AMP_OUT_x to GND			32(4)	V
BSTRP_x to GND			39(4)	V
PVDD	Supply voltage for power stage		28(5)(6)	V
Operating free-air temperature		0	85	°C
Storage temperature range, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are $\overline{PDN}$, $\overline{RST}$, SCLK, LRCK, MCLK, SDIN, SDA, and SCL.
(3) Maximum pin voltage should not exceed 6 V.
(4) DC voltage + peak ac waveform measured at the pin should be below the allowed limit for all conditions.
(5) For operation at PVDD levels greater than 18 V, the modulation limit must be set to 96.1 % or lower via the control port register 0x10.
(6) 26.4 V is the maximum recommended operating voltage for continuous operation of the TAS5751M device. Testing and characterization of the device is performed up to and including 28 V to ensure “in system” design margin. Continuous operation at these levels is not recommended. Operation above the maximum recommended voltage may result in reduced performance, errant operation, and reduction in device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
DVDD, AVDD	Digital, analog supply voltage		3	3.3	3.6	V
PVDD	Output power devices supply voltage		8		26.4(1)(2)	V
V_{IH}	High-level input voltage	5-V tolerant	2			V
V_{IL}	Low-level input voltage	5-V tolerant			0.8	V
T_A	Operating ambient temperature range		0		85	°C
T_J (2)	Operating junction temperature range		0		125	°C
R_L	Load impedance		4	8		Ω
R_L	Load impedance in PBTL		2			Ω
L_O	Output-filter inductance	Minimum output inductance under short-circuit condition	10			µH

(1) For operation at PVDD levels greater than 18 V, the modulation limit must be set to 96.1 % or lower via the control port register 0x10.
(2) 26.4 V is the maximum recommended operating voltage for continuous operation of the TAS5751M device. Testing and characterization of the device is performed up to and including 28 V to ensure “in system” design margin. Continuous operation at these levels is not recommended. Operation above the maximum recommended voltage may result in reduced performance, errant operation, and reduction in device reliability.

6.4 Thermal Characteristics

THERMAL METRIC(1)		DCA (48 PINS)				UNITS
		Special Test Case	JEDEC Standard 2-Layer PCB	JEDEC Standard 4-Layer PCB	TAS5751MEVM	
θ_{JA}	Junction-to-ambient thermal resistance(2)		49.9	26.2	24.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	14.9				°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	6.9				°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)		1.1	0.8	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)		10.8	6.8	1.7	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.7				°C/W

(1) 従来および新しい熱測定値の詳細については、『*Semiconductor and IC Package Thermal Metrics*』アプリケーション・レポート (SPRA953)を参照してください。
(2) 自然対流における、接合部と周囲の空気との間の熱抵抗は、JESD51-2aに記述されている環境において、JESD51-7で規定されているJEDEC標準のHigh-Kボード上でのシミュレーションによって求められます。
(3) 接合部とケース(上面)との間の熱抵抗は、パッケージ上面での冷却板試験のシミュレーションによって求められます。JEDEC規格試験では規定されていませんが、ANSIが策定したSEMI規格のG30-88に類似した記述があります。
(4) 接合部と基板との間の熱抵抗は JESD51-8で説明されているように、PCB温度を制御するリング型冷却板治具で環境をシミュレーションすることにより求められます。
(5) 接合部とケース上部との間の特性パラメータψ_{JT}は、実際のシステムにおけるデバイスの接合部温度を推定するもので、JESD51-2a (セクション6および7)に記述されている手順を用いて、$R_{\theta JA}$を求めるためのシミュレーションデータから抽出されます。
(6) 接合部と基板との間の特性パラメータψ_{JB}は、実際のシステムにおけるデバイスの接合部温度を推定するもので、JESD51-2a (セクション6および7)に記述されている手順を用いて、$R_{\theta JA}$を求めるためのシミュレーションデータから抽出されます。
(7) 接合部とケース(底面)との間の熱抵抗は、露出したパッド(Power PAD)上での冷却板試験のシミュレーションによって求められます。JEDEC規格試験では規定されていませんが、ANSIが策定したSEMI規格のG30-88に類似した内容があります。

6.5 Electrical Characteristics

T_A = 25°, PVDD_x = 24 V, DVDD = AVDD = 3.3 V, R_L= 8 Ω, BTL BD mode, f_S = 48 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	ADR/$\overline{\text{SPK\_FAULT}}$ and SDA	I_{OH} = –4 mA DVDD = AVDD = 3 V	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA DVDD = AVDD = 3 V			0.5	V
I_{IL}	Low-level input current	Digital Inputs	$V_I < V_{IL}$ DVDD = AVDD = 3.6 V			75	µA
I_{IH}	High-level input current		$V_I > V_{IH}$ DVDD = AVDD = 3.6 V			75	µA
I_{DD}	3.3-V supply current	3.3-V supply voltage (DVDD, AVDD)	Normal mode		49	68	mA
			Reset ($\overline{\text{RST}}$ = low, $\overline{\text{PDN}}$ = high)		23	38	

6.6 Speaker Amplifier Characteristics

PVDD = 18 V, BTL AD mode, AVDD = DVDD = 3.3 V, f_S = 48 KHz, R_L = 8 Ω, audio frequency = 1 kHz, AES17 filter, f_{PWM} = 384 kHz, T_A = 25°C (unless otherwise specified). All performance is in accordance with recommended operating conditions.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Power output per channel	PVDD = 18 V,10% THD, 1-kHz input signal			21.5		W
		PVDD = 18 V, 7% THD, 1-kHz input signal			20		
		PVDD = 12 V, 10% THD, 1-kHz input signal			9.5		
		PVDD = 12 V, 7% THD, 1-kHz input signal			9		
		PVDD = 8 V, 10% THD, 1-kHz input signal			4.2		
		PVDD = 8 V, 7% THD, 1-kHz input signal			4		
THD+N	Total harmonic distortion + noise	PVDD = 18 V, P_O = 1 W			0.07%		
		PVDD = 12 V, P_O = 1 W			0.03%		
		PVDD = 8 V, P_O = 1 W			0.1%		
V_n	Output integrated noise (rms)	A-weighted			44		μV
	Crosstalk	P_O = 1 W, f = 1 kHz (BD Mode), PVDD = 24 V			–82		dB
		P_O =1 W, f = 1 kHz (AD Mode), PVDD = 24 V			–62		dB
SNR	Signal-to-noise ratio	A-weighted, f = 1 kHz, maximum power at THD < 1%			106		dB
	Output switching frequency	11.025/22.05/44.1-kHz data rate ±2%			288		kHz
		48/24/12/8/16/32-kHz data rate ±2%			384		
I_{PVDD}	Supply current	No load (PVDD)	Normal mode		32	50	mA
			Reset ($\overline{RST}$ = low, $\overline{PDN}$ = high)		3	8	
$r_{DS(on)}$ (1)	Drain-to-source resistance, LS	T_J = 25°C, includes metallization resistance			80		mΩ
	Drain-to-source resistance, HS	T_J = 25°C, includes metallization resistance			80		
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when drivers are in the high-impedance state to provide bootstrap capacitor charge.			3		kΩ

(1) This does not include bond-wire or pin resistance.

6.7 Protection Characteristics

T_A = 25°, PVDD_x = V, DVDD = AVDD = 3.3 V, R_L= 8 Ω, BTL BD mode, f_S = 48 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{uvp(fall)}$	Undervoltage protection limit	PVDD falling		5.4		V
$V_{uvp(rise)}$	Undervoltage protection limit	PVDD rising		5.8		V
OTE	Overtemperature error			150		°C
I_{OC}	Overcurrent limit protection			4		A
I_{OCT}	Overcurrent response time			150		ns

6.8 Master Clock Characteristics(1)

PVDD = 24 V, BTL BD mode, AVDD = DVDD = 3.3 V, f_S = 48 kHz, R_L = 8 Ω, audio frequency = 1 kHz, AES17 filter, f_{PWM} = 384 kHz, T_A = 25°C (unless otherwise specified). All performance is in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PLL INPUT PARAMETERS						
f_{MCLKI}	MCLK frequency		2.8224		24.576	MHz
	MCLK duty cycle		40%	50%	60%	
t_r / $t_{f(MCLK)}$	Rise/fall time for MCLK				5	ns

(1) For clocks related to the serial audio port, please see Serial Audio Port Timing Requirements.

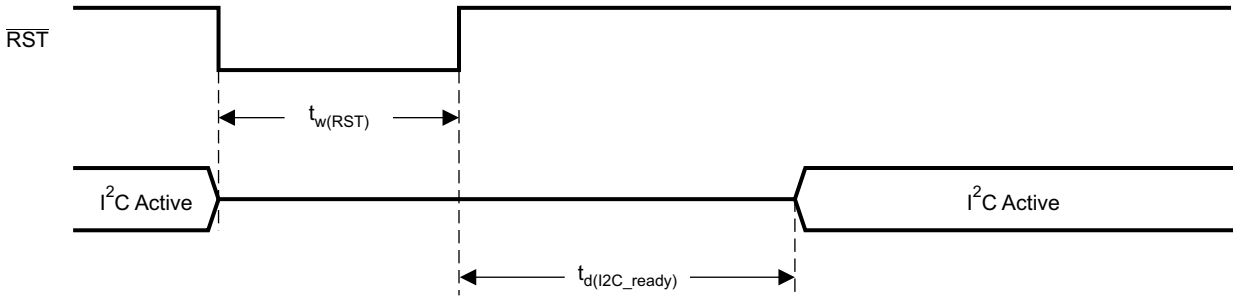
6.9 I²C Interface Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{w(RST)}$	Pulse duration, $\overline{RST}$ active	100			µs
$t_{d(I^2C\_ready)}$	Time to enable I²C after $\overline{RST}$ goes high		13.5		ms
f_{SCL}	Frequency, SCL		400		kHz
$t_{w(H)}$	Pulse duration, SCL high	0.6			µs
$t_{w(L)}$	Pulse duration, SCL low	1.3			µs
t_r	Rise time, SCL and SDA		300		ns
t_f	Fall time, SCL and SDA		300		ns
t_{su1}	Setup time, SDA to SCL	100			ns
t_{h1}	Hold time, SCL to SDA	0			ns
$t_{(buf)}$	Bus free time between stop and start conditions	1.3			µs
t_{su2}	Setup time, SCL to start condition	0.6			µs
t_{h2}	Hold time, start condition to SCL	0.6			µs
t_{su3}	Setup time, SCL to stop condition	0.6			µs
C_L	Load capacitance for each bus line		400		pF

6.10 Serial Audio Port Timing Requirements

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	Frequency, SCLK 32 × f_S, 48 × f_S, 64 × f_S	C_L ≤ 30 pF	1.024		12.288	MHz
t_{su1}	Setup time, LRCK to SCLK rising edge		10			ns
t_{h1}	Hold time, LRCK from SCLK rising edge		10			ns
t_{su2}	Setup time, SDIN to SCLK rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLK rising edge		10			ns
	LRCK frequency		8	48	48	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCK duty cycle		40%	50%	60%	
	SCLK rising edges between LRCK rising edges		32		64	SCLK edges
$t_{(edge)}$	LRCK clock edge with respect to the falling edge of SCLK		–1/4		1/4	SCLK period
t_r/t_f	Rise/fall time for SCLK/LRCK				8	ns
	LRCK allowable drift before LRCK reset				4	MCLKs



NOTE: On power up, hold the TAS5751M $\overline{RST}$ LOW for at least 100 µs after DVDD has reached 3 V.

NOTE: If $\overline{RST}$ is asserted LOW while $\overline{PDN}$ is LOW, then $\overline{RST}$ must continue to be held LOW for at least 100 µs after $\overline{PDN}$ is deasserted (HIGH).

図 1. Reset Timing

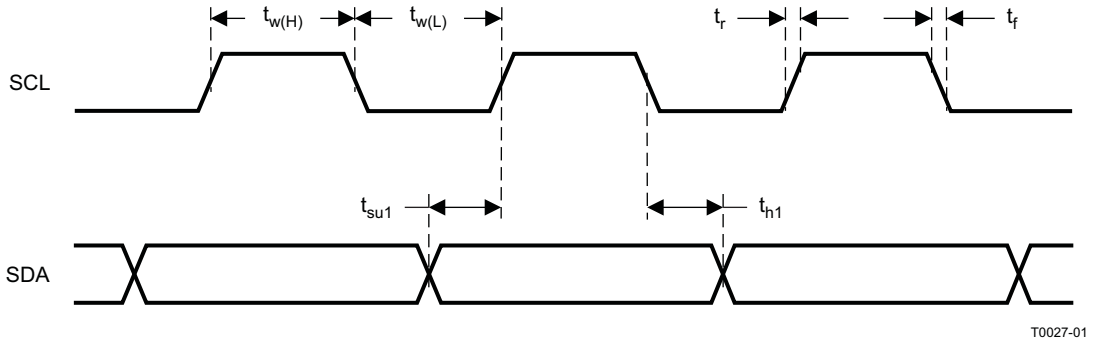


図 2. SCL and SDA Timing

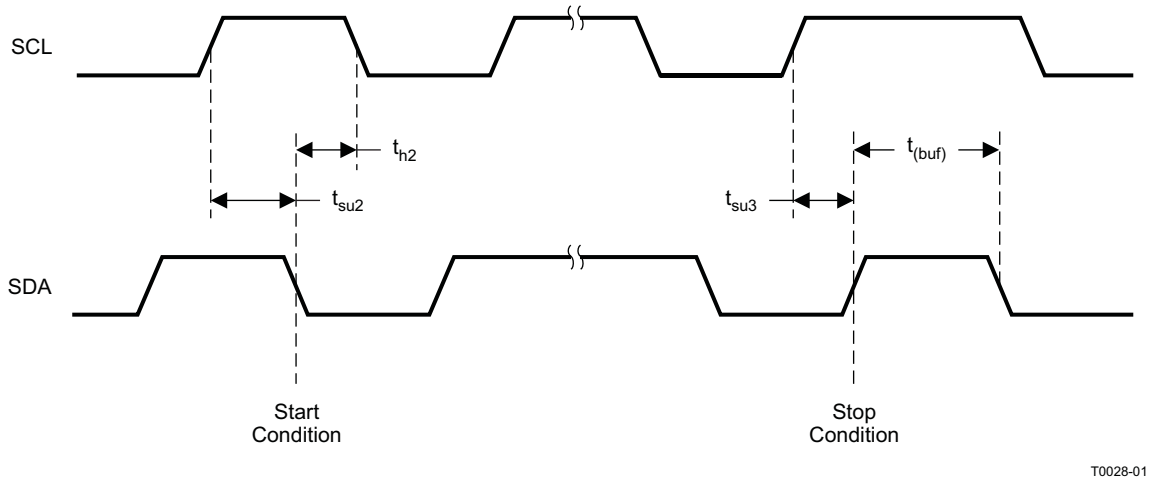


図 3. Start and Stop Conditions Timing

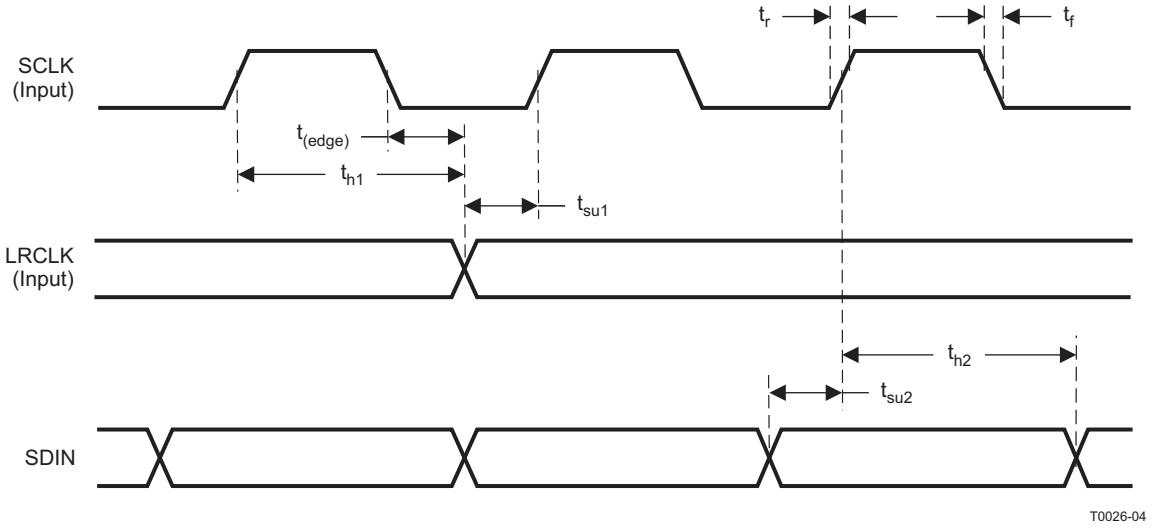


図 4. Serial Audio Port Timing

6.11 Typical Characteristics

6.11.1 Typical Characteristics - Stereo BTL Mode

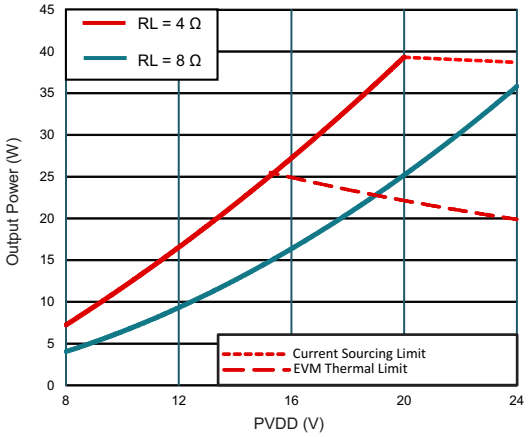


図 5. Output Power vs Supply Voltage

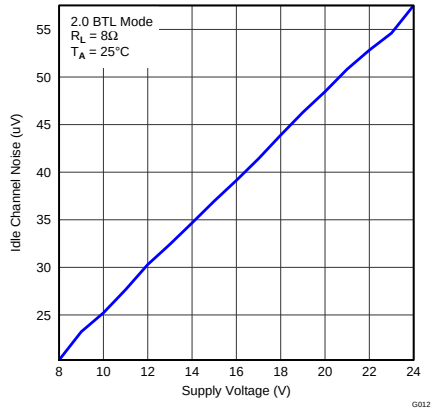


図 6. Idle Channel Noise vs Supply Voltage

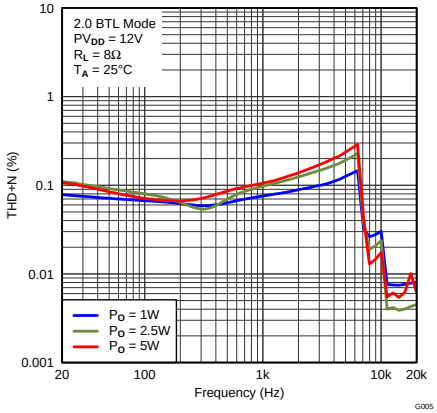


図 7. THD+N vs Frequency

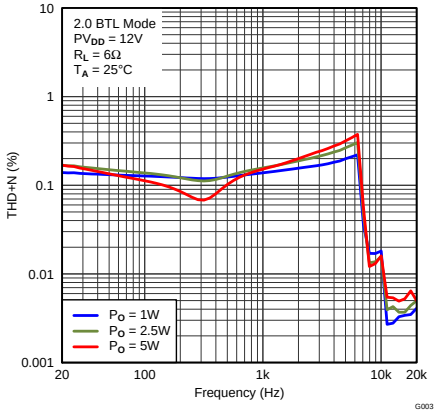


図 8. THD+N vs Frequency

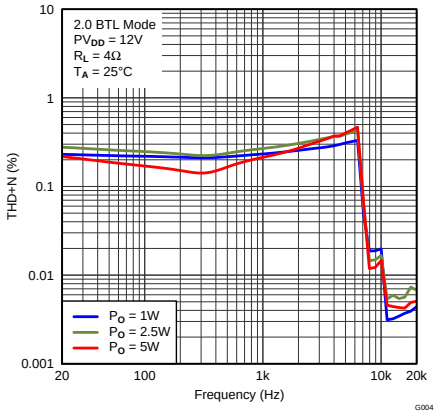


図 9. THD+N vs Frequency

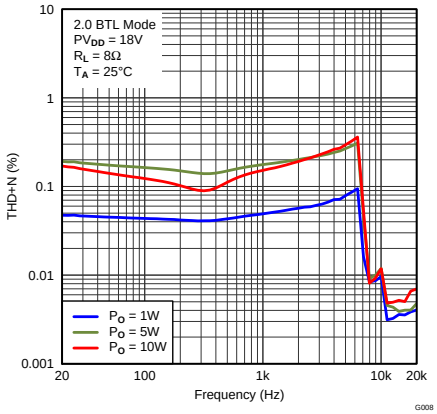


図 10. THD+N vs Frequency

Typical Characteristics - Stereo BTL Mode (continued)

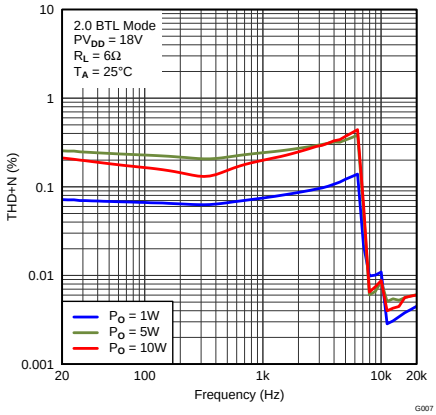


図 11. THD+N vs Frequency

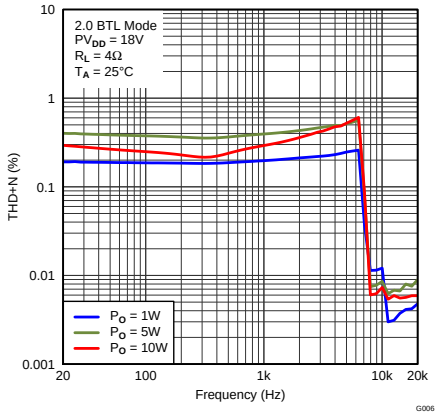


図 12. THD+N vs Frequency

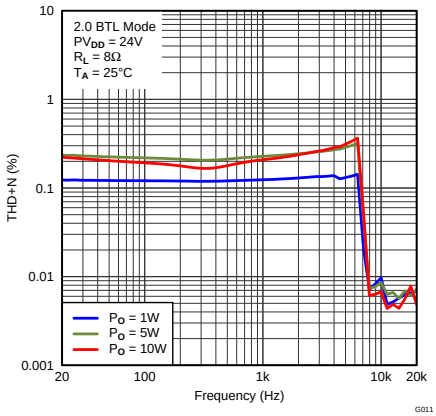


図 13. THD+N vs Frequency

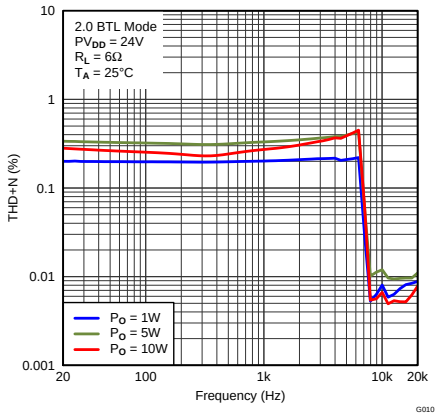


図 14. THD+N vs Frequency

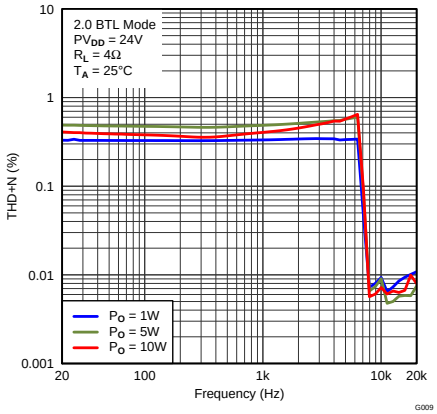


図 15. THD+N vs Frequency

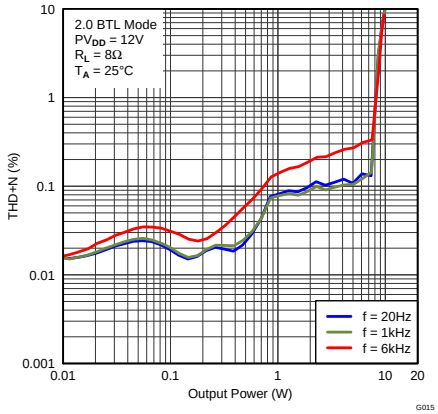


図 16. THD+N vs Output Power

Typical Characteristics - Stereo BTL Mode (continued)

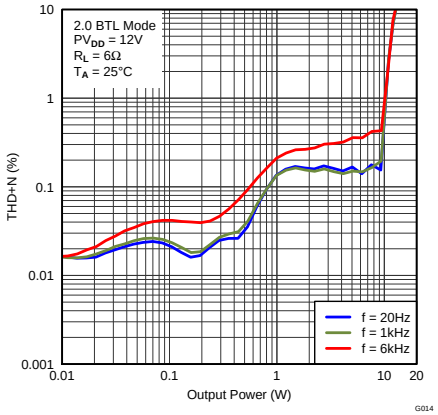


図 17. THD+N vs Output Power

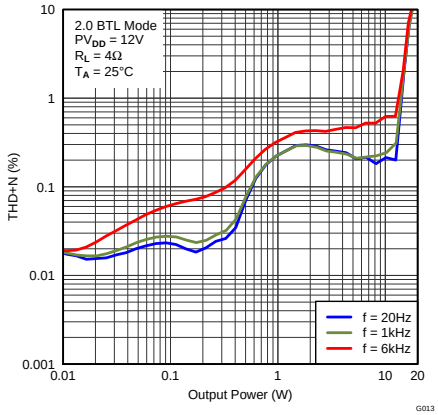


図 18. THD+N vs Output Power

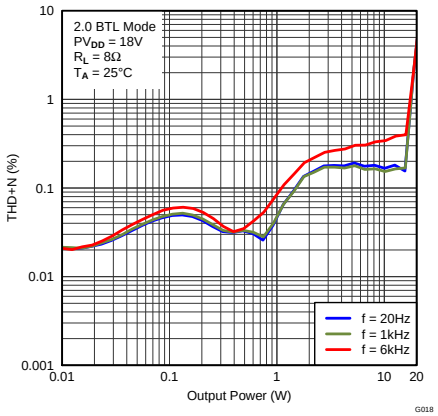


図 19. THD+N vs Output Power

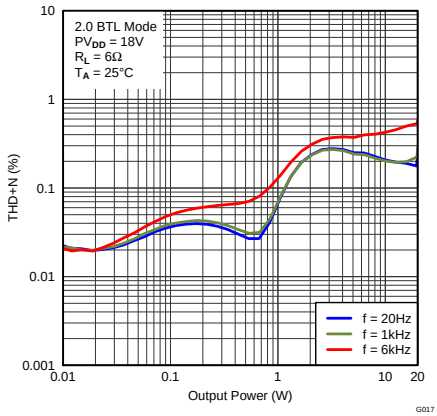


図 20. THD+N vs Output Power

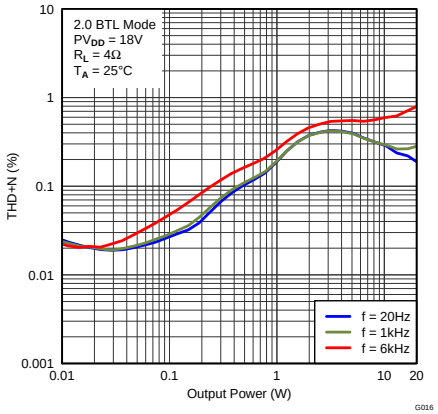


図 21. THD+N vs Output Power

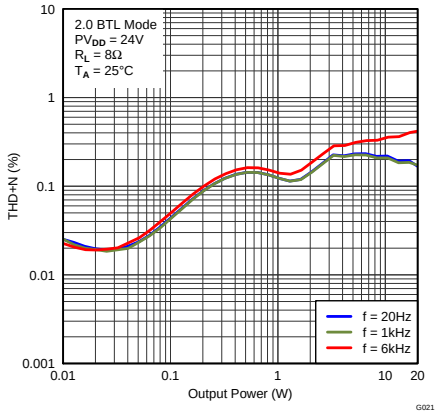


図 22. THD+N vs Output Power

Typical Characteristics - Stereo BTL Mode (continued)

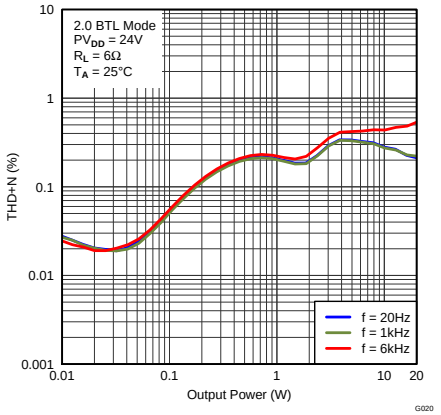


図 23. THD+N vs Output Power

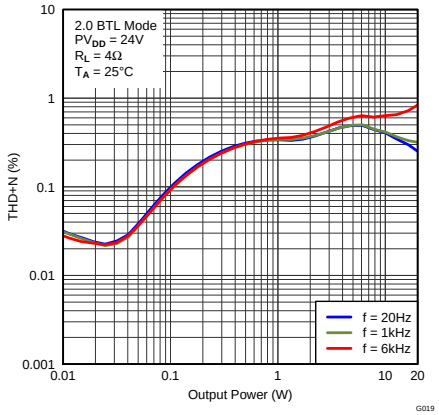
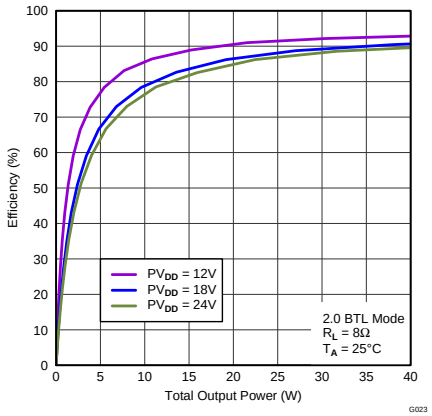
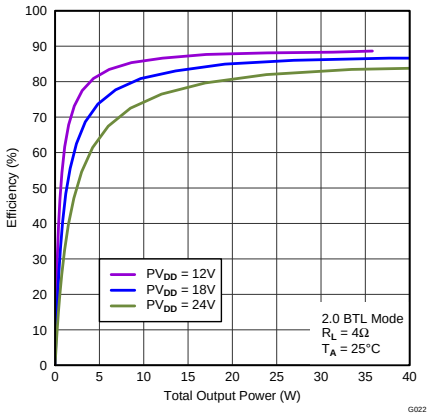


図 24. THD+N vs Output Power



Total Output Power includes power delivered from both amplifier outputs. For instance, 40 W of total output power means 2 × 20 W, with 20 W delivered by one channel and 20 W delivered by the other channel.

図 25. Efficiency vs Total Output Power



Total Output Power includes power delivered from both amplifier outputs. For instance, 40 W of total output power means 2 × 20 W, with 20 W delivered by one channel and 20 W delivered by the other channel.

図 26. Efficiency vs Total Output Power

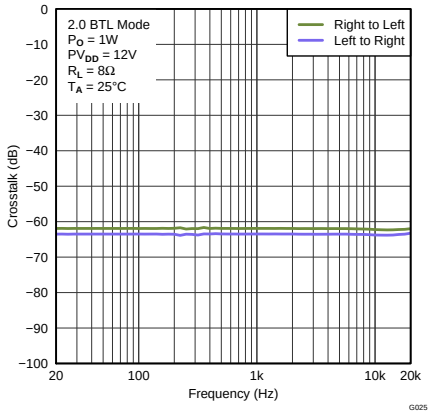


図 27. Crosstalk vs Frequency

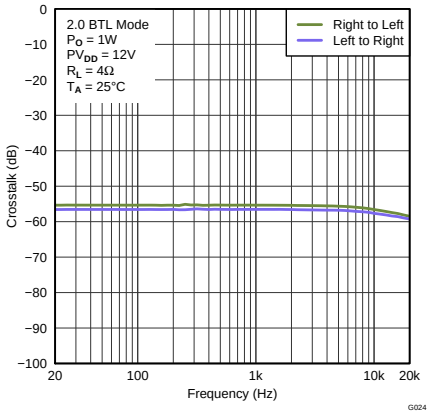


図 28. Crosstalk vs Frequency

Typical Characteristics - Stereo BTL Mode (continued)

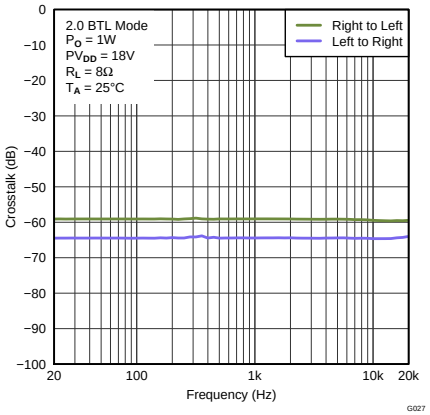


図 29. Crosstalk vs Frequency

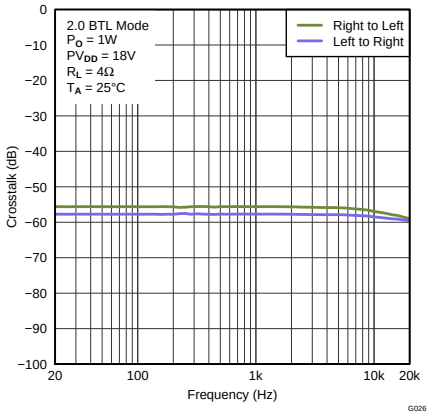


図 30. Crosstalk vs Frequency

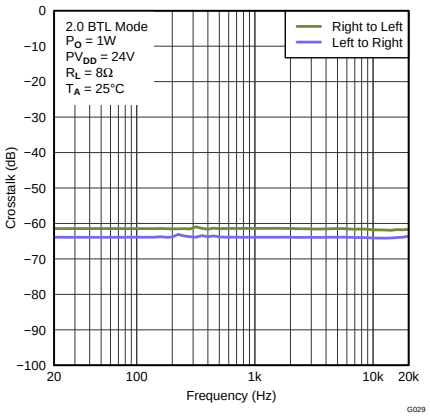


図 31. Crosstalk vs Frequency

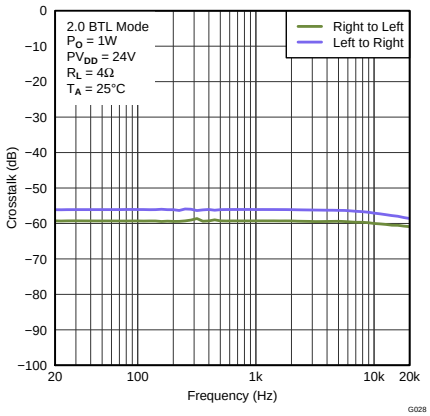


図 32. Crosstalk vs Frequency

6.11.2 Typical Characteristics - Mono PBTL Mode

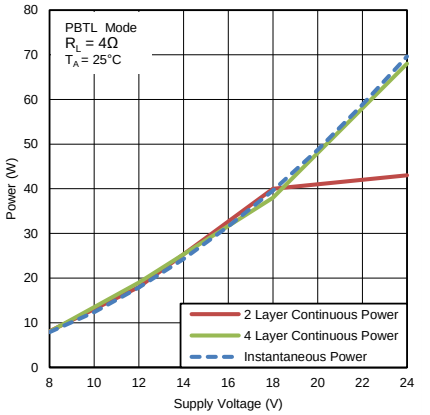


図 33. Output Power vs Supply Voltage (PBTL Mode)

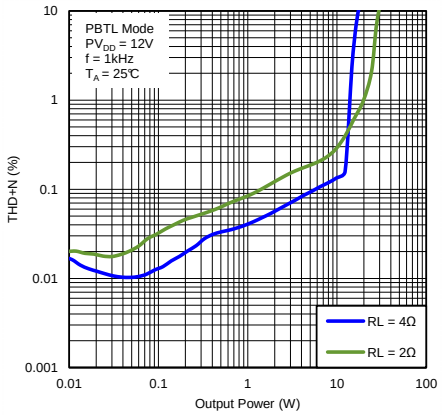


図 34. Total Harmonic Distortion + Noise vs Output Power (PBTL Mode)

Typical Characteristics - Mono PBTL Mode (continued)

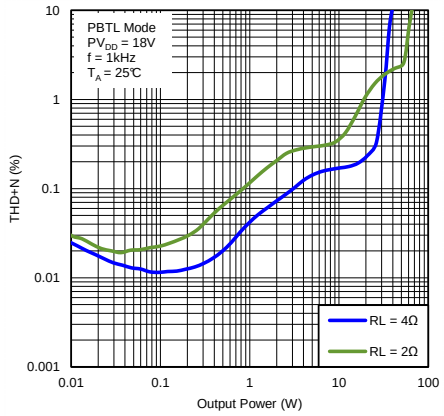


図 35. Total Harmonic Distortion + Noise vs Output Power (PBTL Mode)

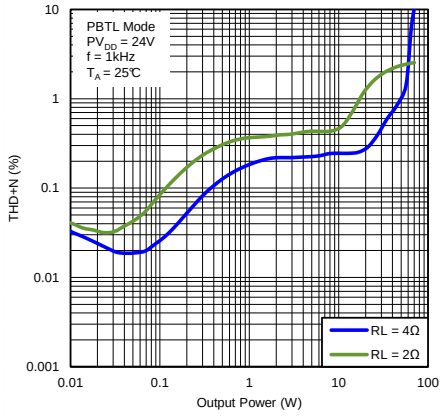


図 36. Total Harmonic Distortion + Noise vs Output Power (PBTL Mode)

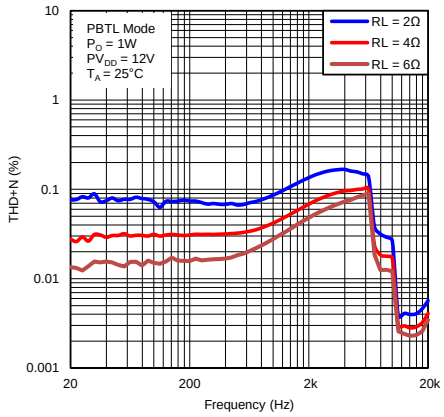


図 37. Total Harmonic Distortion + Noise vs Frequency (PBTL Mode)

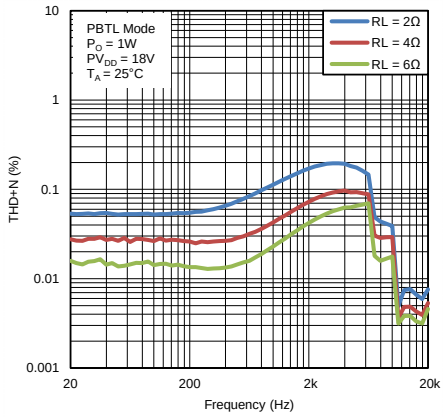


図 38. Total Harmonic Distortion + Noise vs Frequency (PBTL Mode)

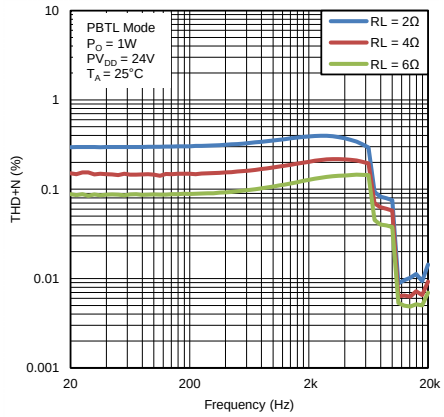
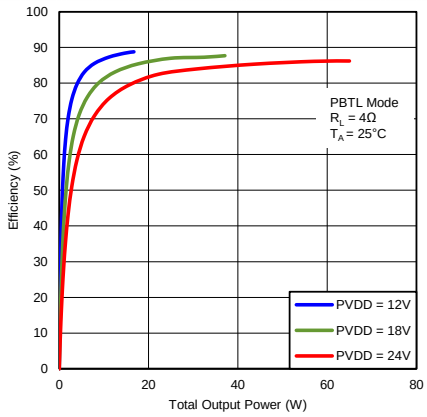


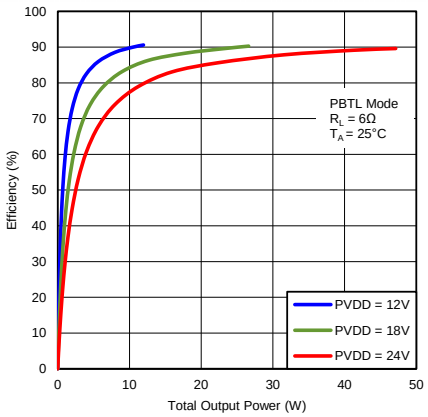
図 39. Total Harmonic Distortion + Noise vs Frequency (PBTL Mode)



Total Output Power includes power delivered from both amplifier outputs. For instance, 40 W of total output power means 2 × 20 W, with 20 W delivered by one channel and 20 W delivered by the other channel.

図 40. Efficiency vs Output Power (PBTL Mode)

Typical Characteristics - Mono PBTL Mode (continued)



Total Output Power includes power delivered from both amplifier outputs. For instance, 40 W of total output power means 2 × 20 W, with 20 W delivered by one channel and 20 W delivered by the other channel.

図 41. Efficiency vs Output Power (PBTL Mode)

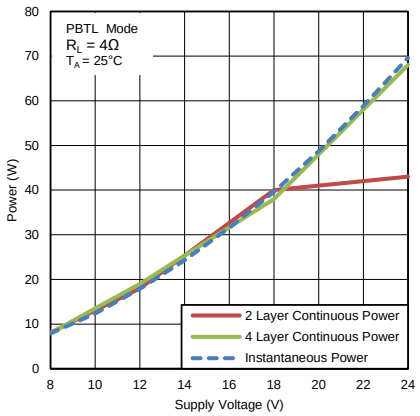


図 42. Power vs Supply Voltage (PBTL Mode)

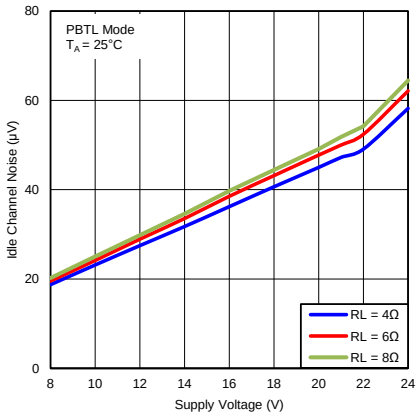


図 43. Idle Channel Noise vs Supply Voltage (PBTL Mode)

7 Detailed Description

7.1 Overview

The TAS5751M device is an efficient, digital-input audio amplifier for driving stereo speakers configured as a bridge tied load (BTL). In parallel bridge tied load (PBTL) in can produce higher power by driving the parallel outputs into a single lower impedance load. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors and MPEG decoders. The device accepts a wide range of input data and data rates. A fully programmable data path routes these channels to the internal speaker drivers.

The TAS5751M device is a slave-only device receiving all clocks from external sources. The TAS5751M device operates with a PWM carrier between a 384-kHz switching rate and a 288-kHz switching rate, depending on the input sample rate. Oversampling combined with a fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

7.2 Functional Block Diagram

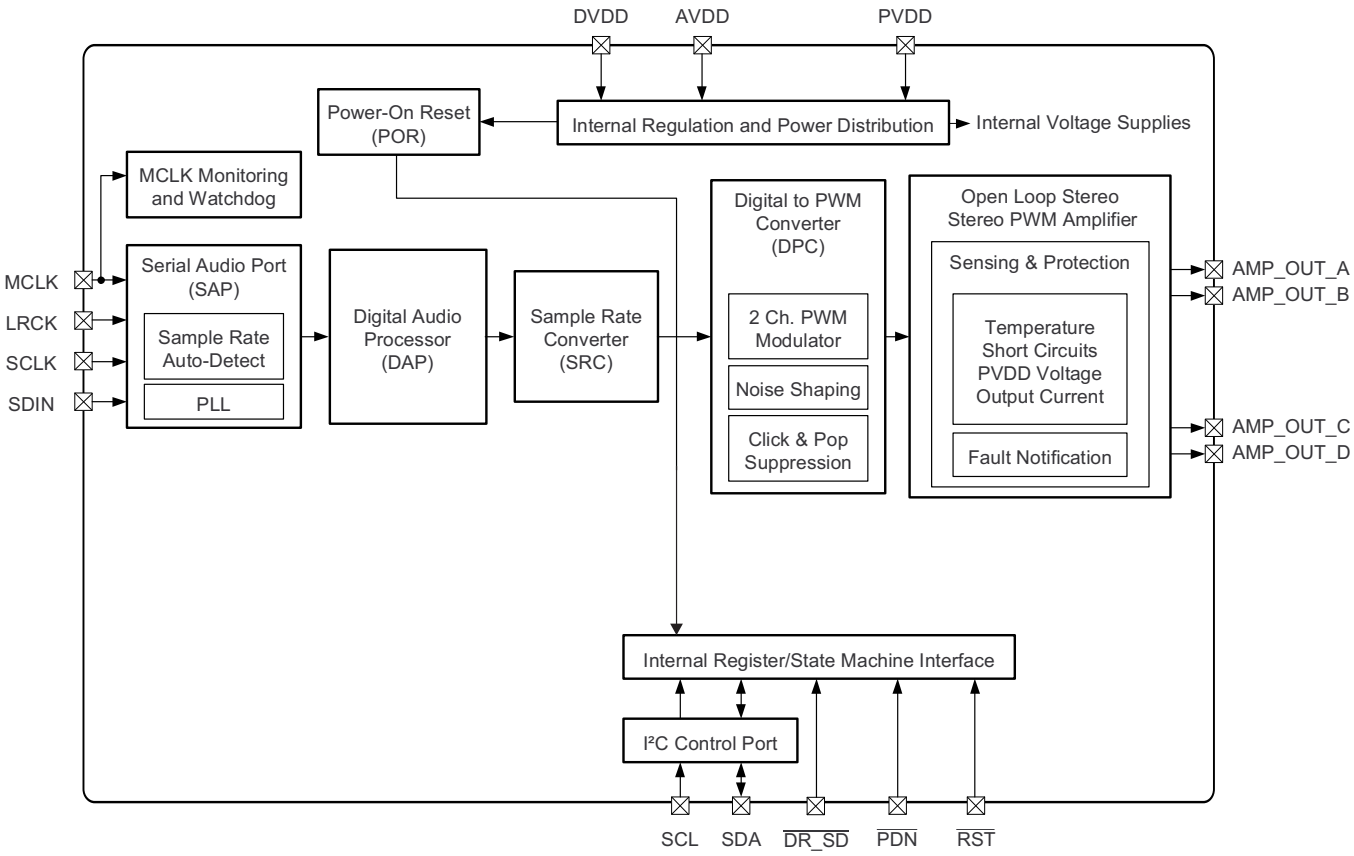


図 44. TAS5751M Functional Block Diagram

7.3 Audio Signal Processing Overview

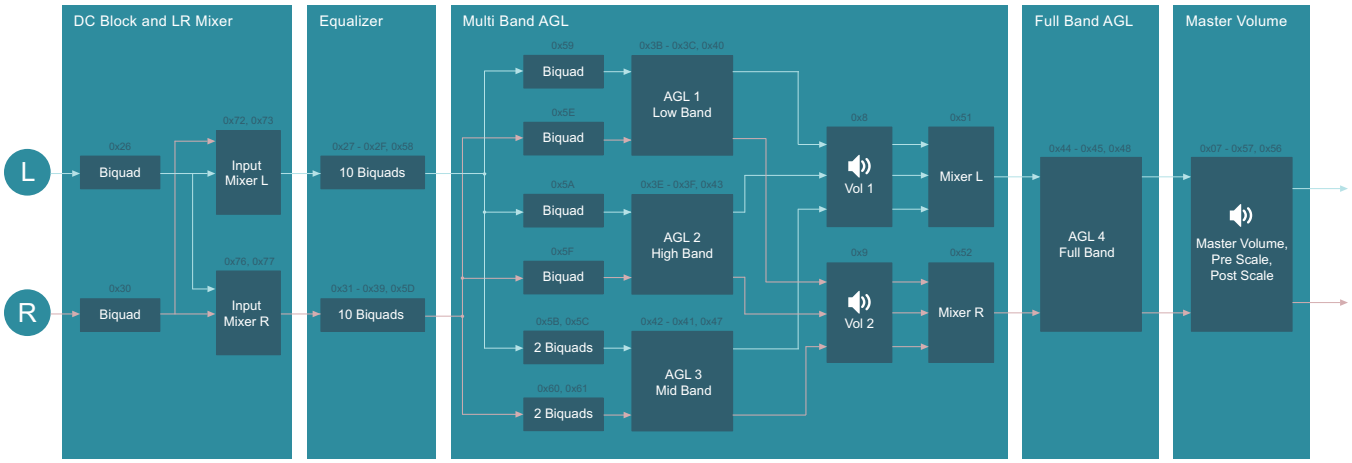


図 45. TAS5751M Audio Process Flow

7.4 Feature Description

7.4.1 Clock, Autodetection, and PLL

The TAS5751M device is an I²S slave device. The TAS5751M device accepts MCLK, SCLK, and LRCK. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the *Clock Control Register*.

The TAS5751M device checks to verify that SCLK is a specific value of 32 f_S, 48 f_S, or 64 f_S. The DAP only supports a 1 × f_S LRCK. The timing relationship of these clocks to SDIN is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable, out of range, or absent) to produce the internal clock (DCLK) running at 512 times the PWM switching frequency.

The DAP can autodetect and set the internal clock control logic to the appropriate settings for all supported clock rates as defined in the *Clock Control Register*.

The TAS5751M device has robust clock error handling that uses the built-in trimmed oscillator clock to quickly detect changes/errors. Once the system detects a clock change/error, the system mutes the audio (through a single-step mute) and then forces PLL to limp using the internal oscillator as a reference clock. Once the clocks are stable, the system autodetects the new rate and reverts to normal operation. During this process, the default volume is restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in the *Volume Configuration Register*.

7.4.2 PWM Section

The TAS5751M DAP device uses noise-shaping and customized nonlinear correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts 24-bit PCM data from the DAP and outputs two BTL PWM audio output channels.

The PWM section has individual-channel dc-blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz.

The PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%. For PVDD > 18 V the modulation index must be limited to 96.1% for safe and reliable operation.

7.4.3 PWM Level Meter

The structure in 図 46 shows the PWM level meter that can be used to study the power profile.

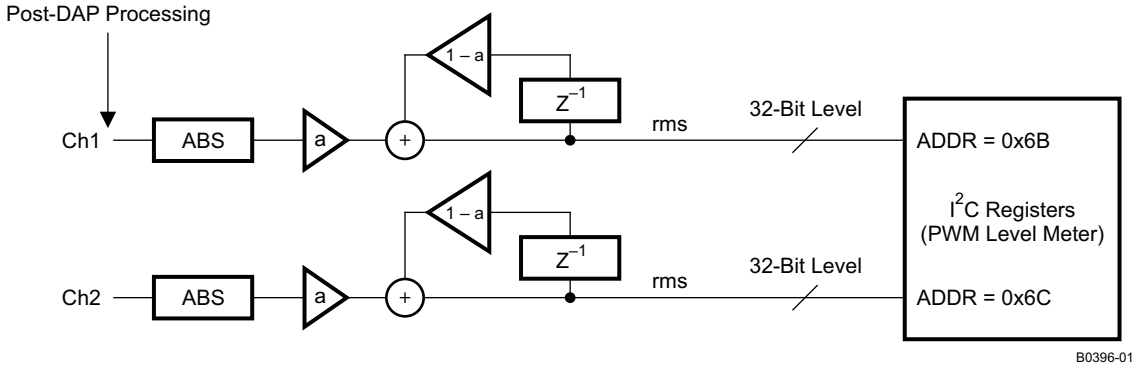


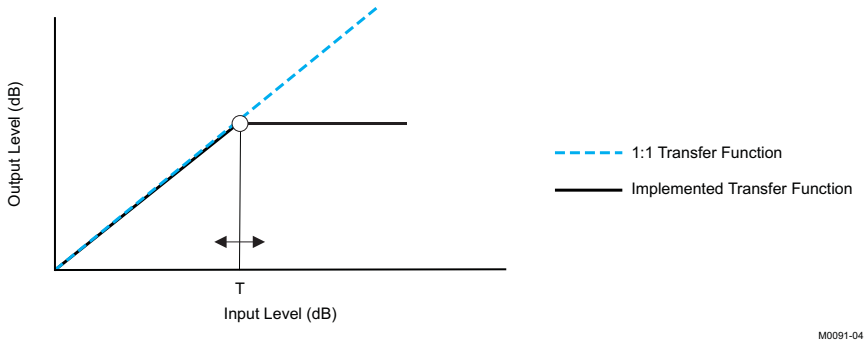
図 46. PWM Level Meter Structure

7.4.4 Automatic Gain Limiter (AGL)

The AGL scheme has three AGL blocks. One ganged AGL exists for the high-band left/right channels, the mid-band left/right channels, and the low-band left/right channels.

The AGL input/output diagram is shown in 図 47.

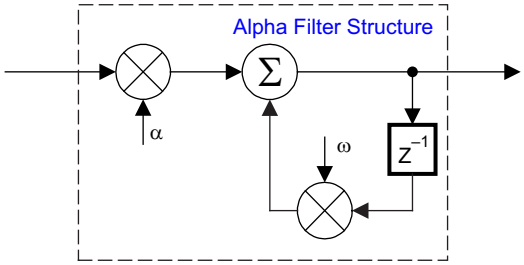
Feature Description (continued)



Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

- Each AGL has adjustable threshold levels.
- Programmable attack and decay time constants
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

図 47. Automatic Gain Limiter



T = 9.23 format, all other AGL coefficients are 3.23 format

図 48. AGL Structure

表 1. AGL Structure

	α, ω	T	αa, ωa / αd, ωd
AGL 1	0x3B	0x40	0x3C
AGL 2	0x3E	0x43	0x3F
AGL 3	0x47	0x41	0x42
AGL 4	0x48	0x44	0x45

7.4.5 Headphone/Line Amplifier

An integrated ground centered DirectPath combination headphone amplifier and line driver is integrated in the TAS5729MD. This headphone/line amplifier can be used independently from the device speaker amplifier modes, with analog single-ended inputs DR_INA and DR_INB, linked to the respective analog outputs DR_OUTA, and DR_OUTB. A basic diagram of the headphone/line amplifier is shown in 図 49.

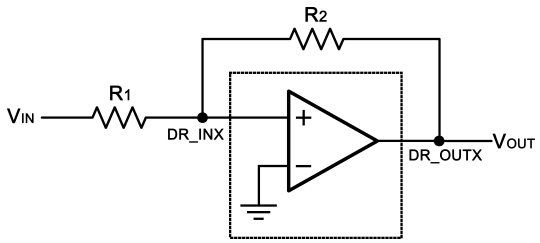


図 49. Headphone/Line Amplifier

The $\overline{\text{DR\_SDI}}$ pin can be used to turn on or off the headphone amplifier and line driver. The DirectPath amplifier makes use of the provided positive and negative supply rails generated by the IC. The output voltages are centered at zero volts with the capability to swing to the positive rail or negative rail; combining this capability with the built-in click and pop reduction circuit, the DirectPath amplifier requires no output dc blocking capacitors.

7.4.6 Fault Indication

ADR/$\overline{\text{FAULT}}$ is an input pin during power up. This pin can be programmed after $\overline{\text{RST}}$ to be an output by writing 1 to bit 0 of I²C register 0x05. In that mode, the ADR/$\overline{\text{FAULT}}$ pin has the definition shown in 表 2.

Any fault resulting in device shutdown is signaled by the ADR/$\overline{\text{FAULT}}$ pin going low (see 表 2). A latched version of this pin is available on D1 of register 0x02. This bit can be reset only by an I²C write.

表 2. ADR/$\overline{\text{FAULT}}$ Output States

ADR/$\overline{\text{FAULT}}$	DESCRIPTION
0	Overcurrent (OC) or undervoltage (UVP) error or overtemperature error (OTE) or overvoltage error
1	No faults (normal operation)

7.4.7 SSTIMER Pin Functionality

The SSTIMER pin uses a capacitor connected between this pin and ground to control the output duty cycle when exiting all-channel shutdown. The capacitor on the SSTIMER pin is slowly charged through an internal current source, and the charge time determines the rate at which the output transitions from a near-zero duty cycle to the desired duty cycle. This allows for a smooth transition that minimizes audible pops and clicks. When the part is shut down, the drivers are placed in the high-impedance state and transition slowly down through an internal 3-kΩ resistor, similarly minimizing pops and clicks. The shutdown transition time is independent of the SSTIMER pin capacitance. Larger capacitors increase the start-up time, while smaller capacitors decrease the start-up time. The SSTIMER pin can be left floating for BD modulation.

7.4.8 Device Protection System

7.4.8.1 Overcurrent (OC) Protection With Current Limiting

The TAS5751M device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored to prevent the output current from increasing beyond the overcurrent threshold defined in the Protection Characteristics table.

If the output current increases beyond the overcurrent threshold, the device shuts down and the outputs transition to the off or high impedance (Hi-Z) state. The device returns to normal operation once the fault condition (i.e., a short circuit on the output) is removed. Current-limiting and overcurrent protection are not independent for half-bridges. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D shut down.

7.4.8.2 Overtemperature Protection

The TAS5751M device has an overtemperature-protection system. If the device junction temperature exceeds 150°C (nominal), the device enters thermal shutdown, where all half-bridge outputs enter the high-impedance (Hi-Z) state, and ADR/$\overline{\text{FAULT}}$ asserts low if the device is configured to function as a fault output. The TAS5751M device recovers automatically once the junction temperature of the device drops approximately 30°C.

7.4.8.3 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5751M device fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach 7.6 V and 2.7 V, respectively. Although PVDD and AVDD are independently monitored. For PVDD, if the supply voltage drops below the UVP threshold, the protection feature immediately sets all half-bridge outputs to the high-impedance (Hi-Z) state and asserts ADR/$\overline{\text{FAULT}}$ low.

7.5 Device Functional Modes

The TAS5751M device is a digital input class-d amplifier with audio processing capabilities. The TAS5751M device has numerous modes to configure and control the device.

7.5.1 Serial Audio Port Operating Modes

The serial audio port in the TAS5751M device supports industry-standard audio data formats, including I²S, Left-justified(LJ) and Right-justified(RJ) formats. To select the data format that will be used with the device can controlled by using the serial data interface registers 0x04. The default is 24bit, I²S mode. The timing diagrams for the various serial audio port are shown in the *Serial Interface Control and Timing* section

7.5.2 Communication Port Operating Modes

The TAS5751M device is configured via an I²C communication port. The I²C communication protocol is detailed in the *7.7 I²C Serial Control Port Requirements and Specifications* section.

Device Functional Modes (continued)

7.5.3 Speaker Amplifier Modes

The TAS5751M device can be configured as:

- Stereo Mode
- Mono Mode

7.5.3.1 Stereo Mode

Stereo mode is the most common option for the TAS5751M. TAS5751M can be connected in 2.0 mode to drive stereo channels. Detailed application section regarding the stereo mode is discussed in the *Stereo Bridge Tied Load Application* section.

7.5.3.2 Mono Mode

Mono mode is described as the operation where the two BTL outputs of amplifier are placed in parallel with one another to provide increase in the output power capability. This mode is typically used to drive subwoofers, which require more power to drive larger loudspeakers with high-amplitude, low-frequency energy. Detailed application section regarding the mono mode is discussed in the *Mono Parallel Bridge Tied Load Application* section.

7.6 Programming

7.6.1 I²C Serial Control Interface

The TAS5751M device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum). The DAP performs all I²C operations without I²C wait cycles.

7.6.1.1 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in 図 50. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5751M device holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

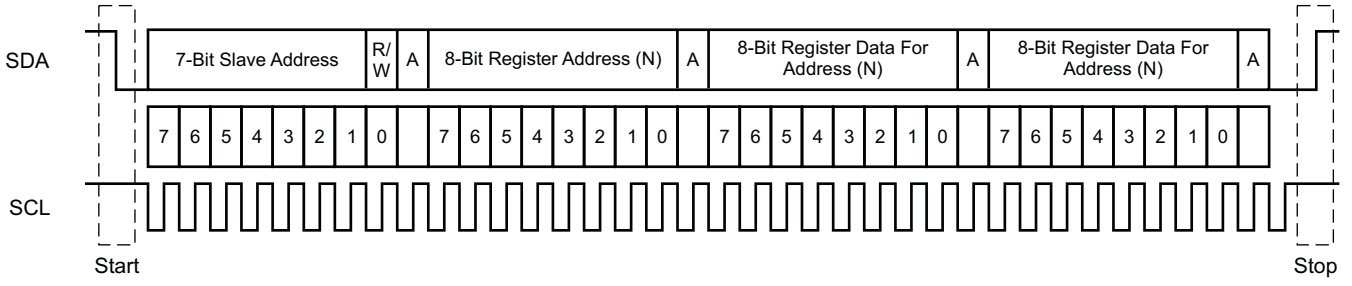


図 50. Typical I²C Sequence

Programming (continued)

No limit exists for the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in 図 50.

The 7-bit address for the TAS5751M device is 0101 010 (0x54) or 0101 011 (0x56) as defined by ADR/$\overline{\text{FAULT}}$ (external pulldown for 0x54 and pullup for 0x56).

7.6.1.2 I²C Slave Address

The ADR/$\overline{\text{FAULT}}$ is an input pin during power-up and after each toggle of $\overline{\text{RST}}$, which is used to set the I²C sub-address of the device. The ADR/$\overline{\text{FAULT}}$ can also operate as a fault output after power-up is complete and the address has been latched in.

At power-up, and after each toggle of $\overline{\text{RST}}$, the pin is read to determine its voltage level. If the pin is left floating, an internal pull-up will set the I²C sub-address to 0x56. This will also be the case if an external resistor is used to pull the pin up to AVDD. To set the sub-address to 0x54, an external resistor (specified in Typical Applications) must be connected to the system ground.

As mentioned, the pin can also be reconfigured as an output driver via I²C for fault monitoring. Use System Control Register 2 (0x05) to set ADR/$\overline{\text{FAULT}}$ pin to be used as a fault output during fault conditions.

7.6.1.2.1 I²C Device Address Change Procedure

1. Write to device address change enable register, 0xF8 with a value of 0xF9A5 A5A5.
2. Write to device register 0xF9 with a value of 0x0000 00XX, where XX is the new address.
3. Any writes after that should use the new device address XX.

7.6.1.3 Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for subaddresses 0x00 to 0x1F. However, for the subaddresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. For example, if a write command is received for a biquad subaddress, the DAP must receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the received data is discarded.

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. The TAS5751M device also supports sequential I²C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5751M device. For I²C sequential-write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted before a stop or start is transmitted determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Programming (continued)

7.6.1.4 Single-Byte Write

As shown in 図 51, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the TAS5751M device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5751M device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

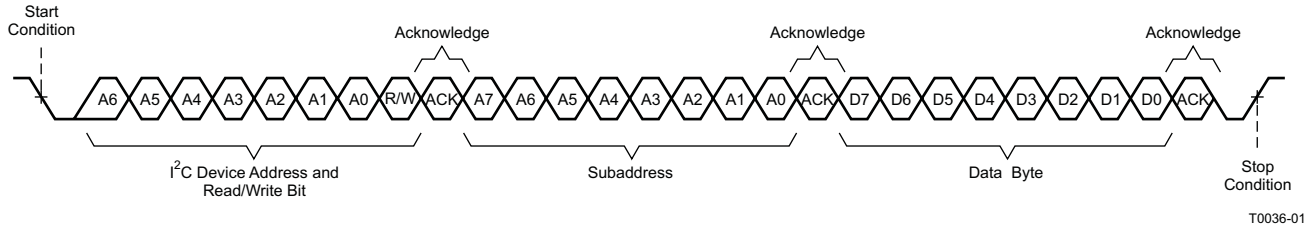


図 51. Single-Byte Write Transfer

7.6.1.5 Multiple-Byte Write

A multiple-byte data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in 図 52. After receiving each data byte, the TAS5751M device responds with an acknowledge bit.

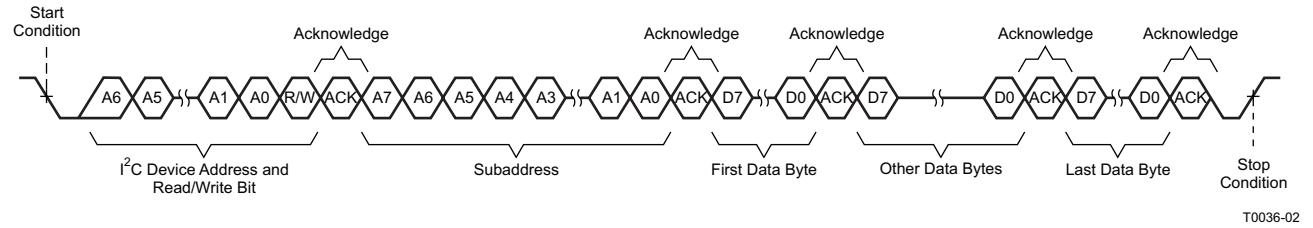


図 52. Multiple-Byte Write Transfer

7.6.1.6 Single-Byte Read

As shown in 図 53, a single-byte data-read transfer begins with the master device transmitting a start condition, followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5751M address and the read/write bit, TAS5751M device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5751M address and the read/write bit again. This time, the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5751M device again responds with an acknowledge bit. Next, the TAS5751M device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

Programming (continued)

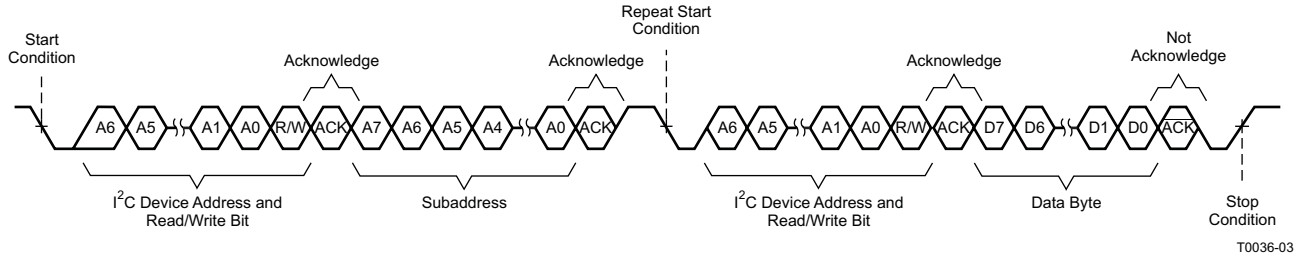


図 53. Single-Byte Read Transfer

7.6.1.7 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS5751M device to the master device as shown in 図 54. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

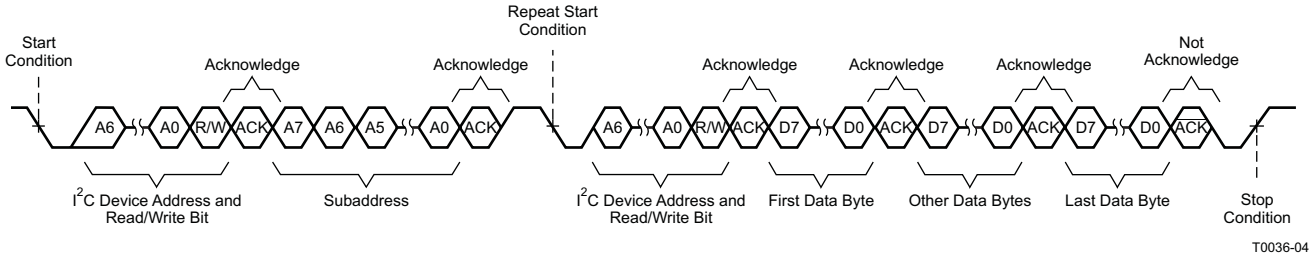


図 54. Multiple-Byte Read Transfer

7.6.2 Serial Interface Control and Timing

7.6.2.1 Serial Data Interface

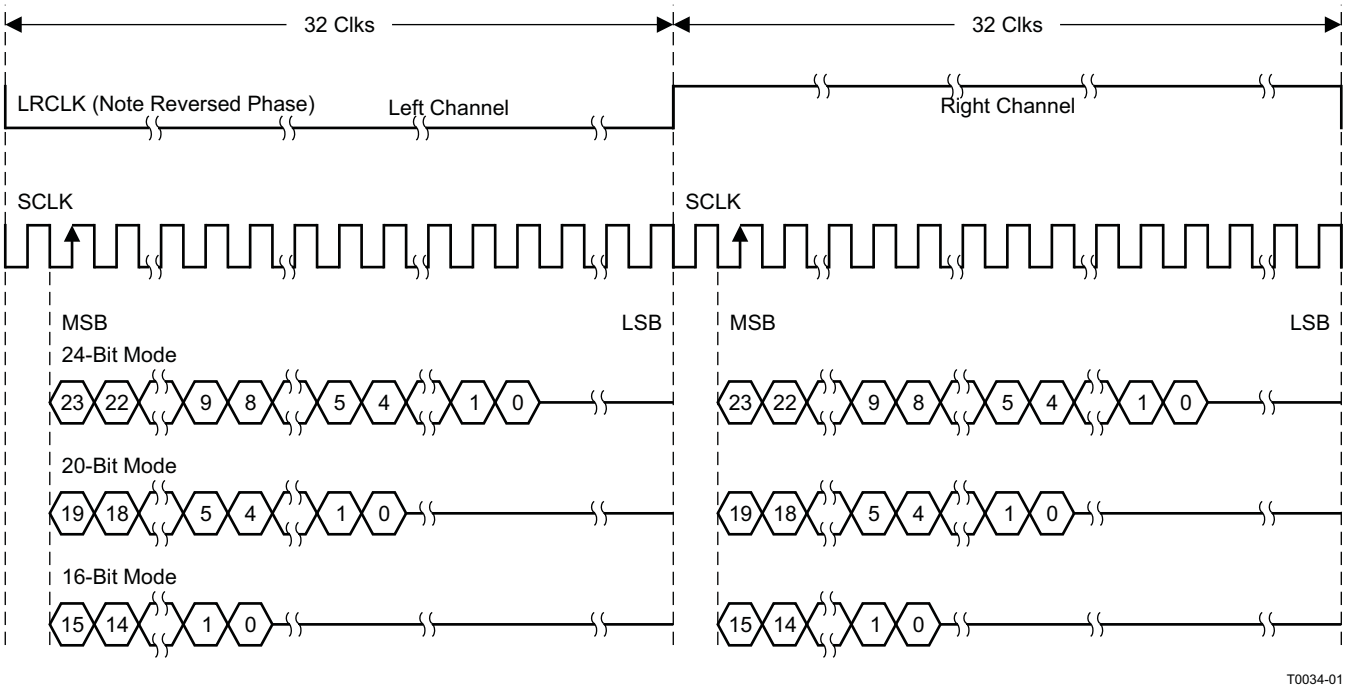
Serial data is input on SDIN. The PWM outputs are derived from SDIN. The TAS5751M DAP accepts serial data in 16-bit, 20-bit, or 24-bit left-justified, right-justified, and I²S serial data formats.

7.6.2.2 I²S Timing

I²S timing uses LRCK to define when the data being transmitted is for the left channel and when the data is for the right channel. LRCK is low for the left channel and high for the right channel. A bit clock running at 32 × f_S, 48 × f_S, or 64 × f_S is used to clock in the data. A delay of one bit clock exists from the time the LRCK signal changes state to the first bit of data on the data lines. The data is written MSB-first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

Programming (continued)

2-Channel I^{2}S (Philips Format) Stereo Input

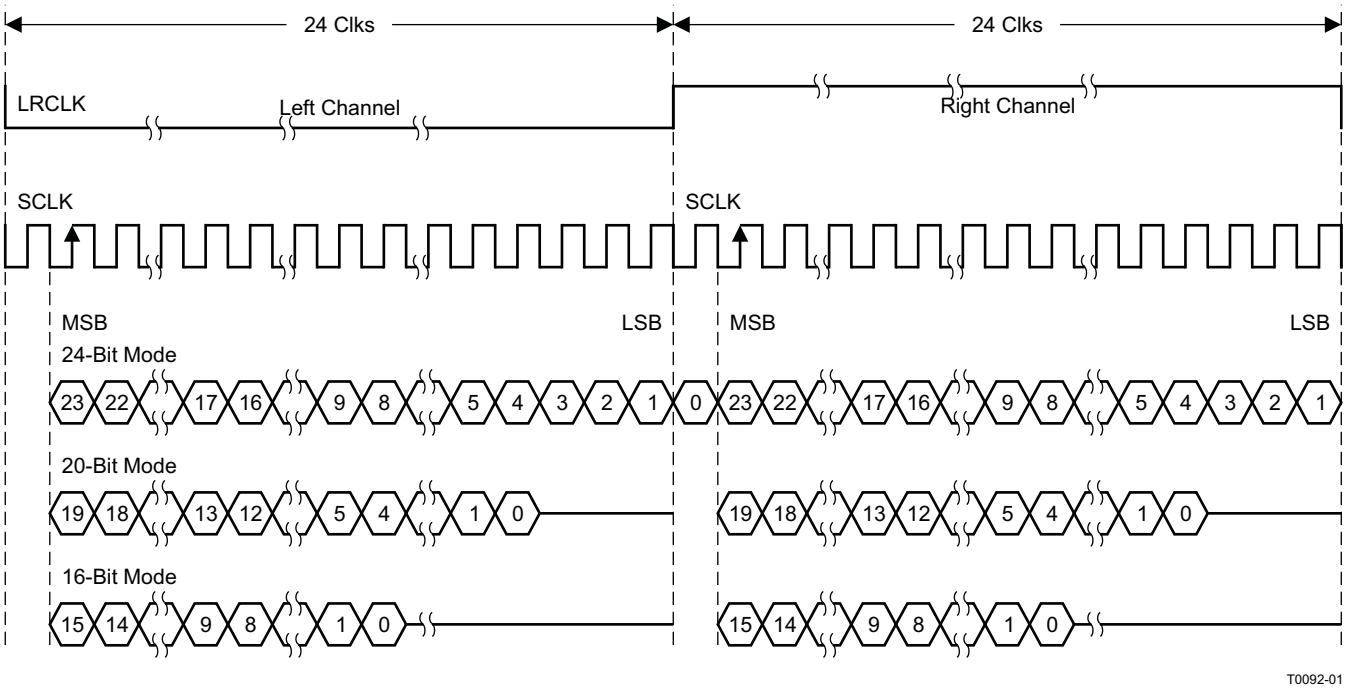


NOTE: All data presented in two's-complement form with MSB first.

図 55. I²S 64-f_S Format

Programming (continued)

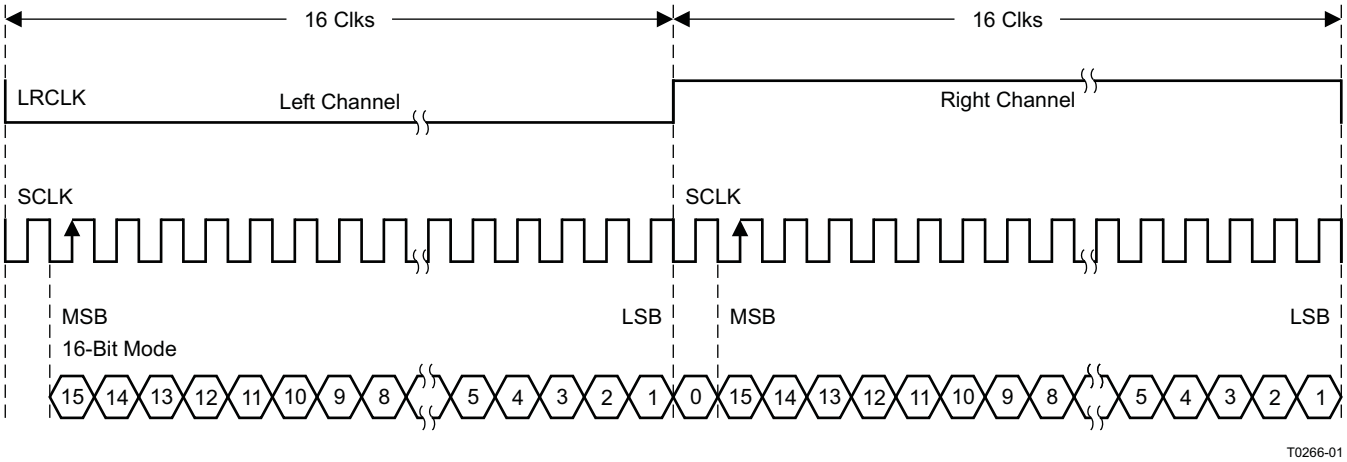
2-Channel I²S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)



NOTE: All data presented in two's-complement form with MSB first.

図 56. I²S 48-f_S Format

2-Channel I²S (Philips Format) Stereo Input



NOTE: All data presented in two's-complement form with MSB first.

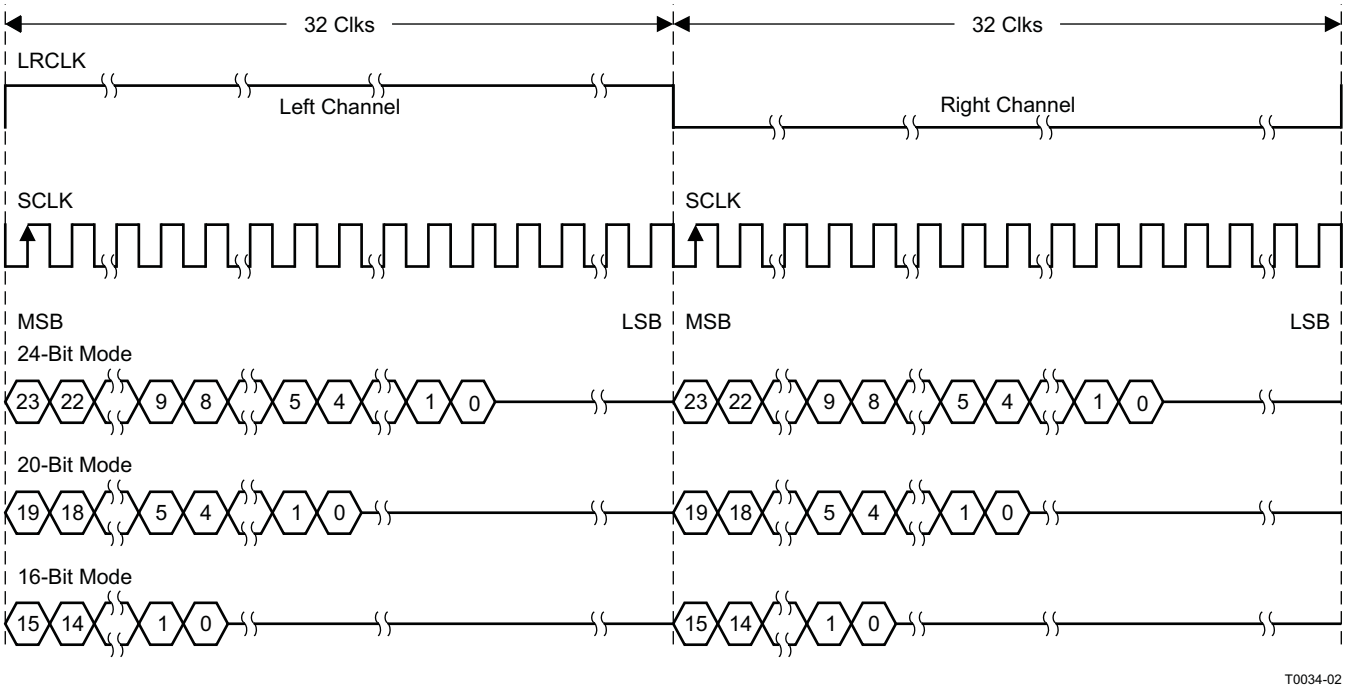
図 57. I²S 32-f_S Format

Programming (continued)

7.6.2.3 Left-Justified

Left-justified (LJ) timing uses LRCK to define when the data being transmitted is for the left channel and when the data is for the right channel. LRCK is high for the left channel and low for the right channel. A bit clock running at 32 × f_S, 48 × f_S, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

2-Channel Left-Justified Stereo Input

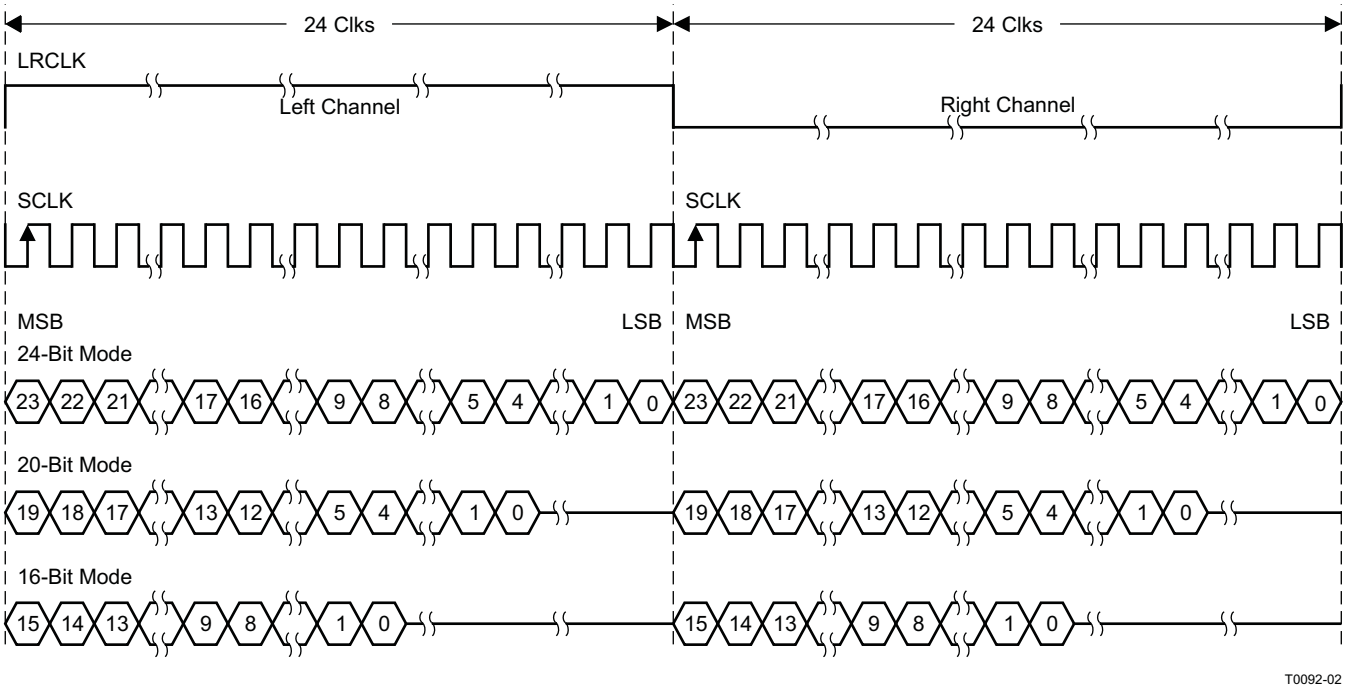


NOTE: All data presented in two's-complement form with MSB first.

図 58. Left-Justified 64-f_S Format

Programming (continued)

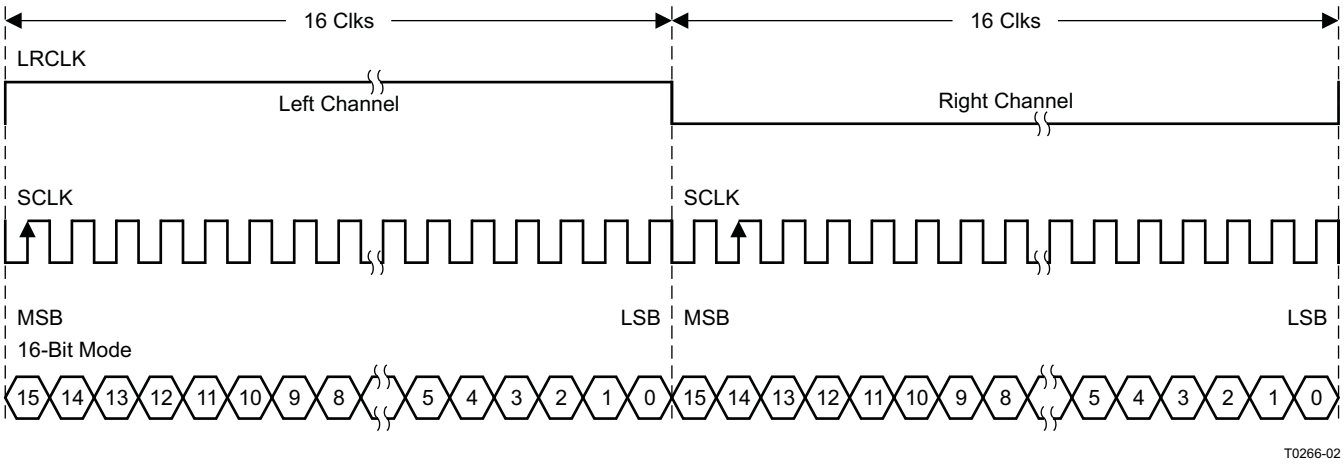
2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)



NOTE: All data presented in two's-complement form with MSB first.

図 59. Left-Justified 48-f_S Format

2-Channel Left-Justified Stereo Input



NOTE: All data presented in two's-complement form with MSB first.

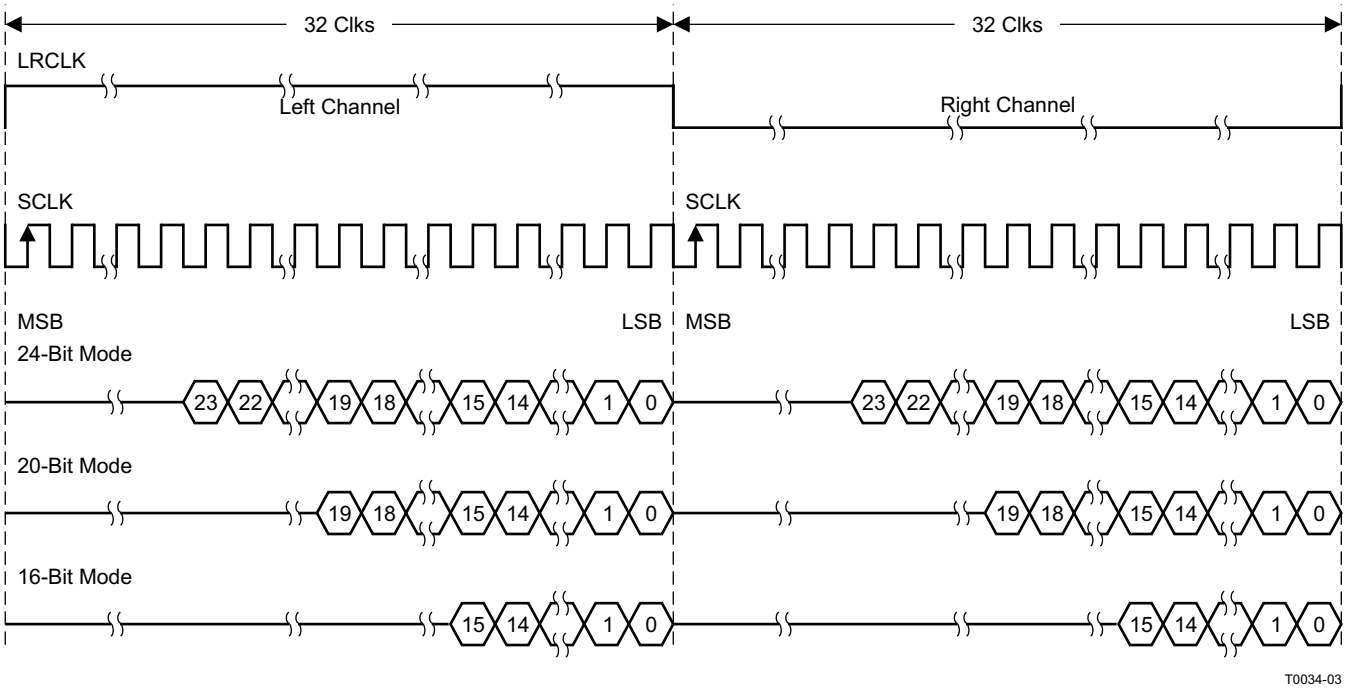
図 60. Left-Justified 32-f_S Format

Programming (continued)

7.6.2.4 Right-Justified

Right-justified (RJ) timing uses LRCK to define when the data being transmitted is for the left channel and when the data is for the right channel. LRCK is high for the left channel and low for the right channel. A bit clock running at 32 × f_S, 48 × f_S, or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCK toggles. In RJ mode, the LSB of data is always clocked by the last bit clock before LRCK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

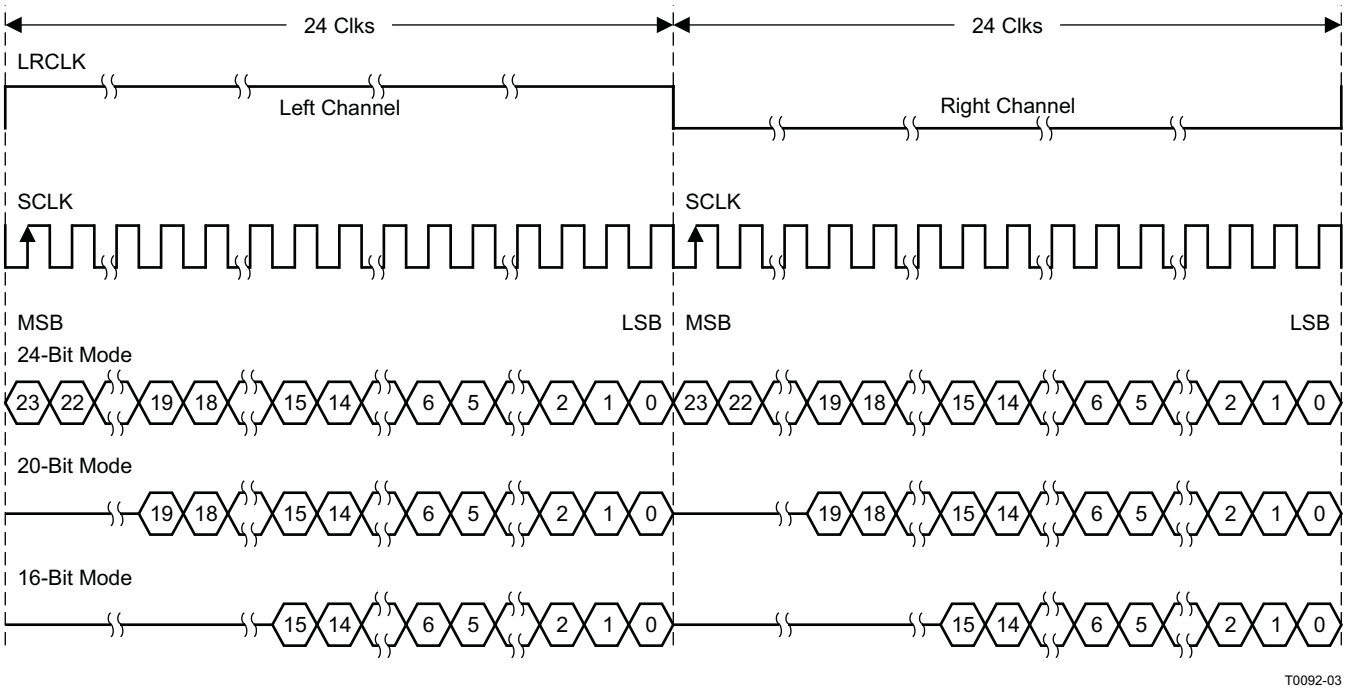


All data presented in two's-complement form with MSB first.

図 61. Right-Justified 64-f_S Format

Programming (continued)

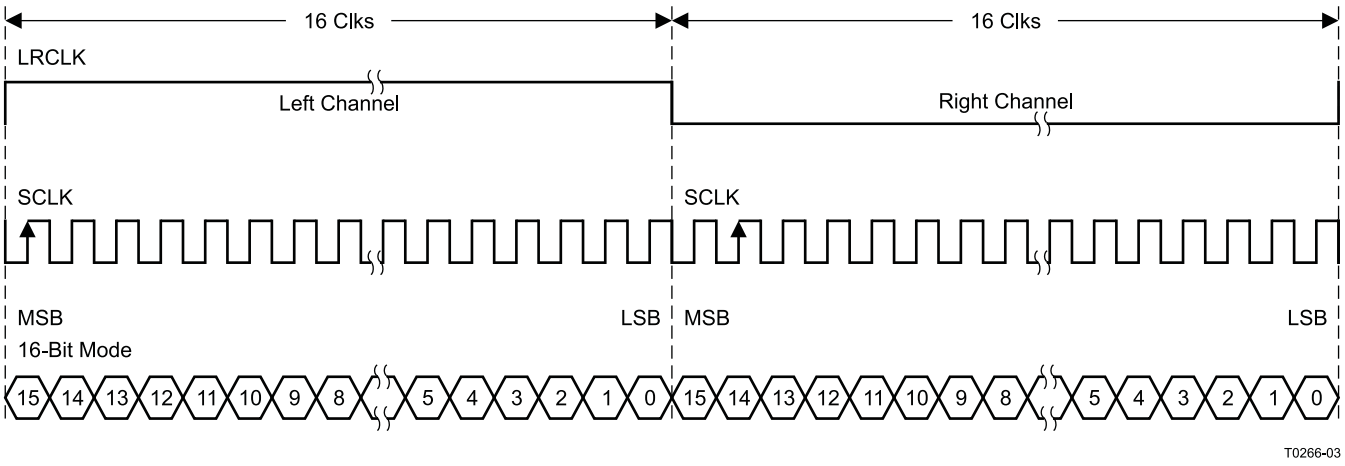
2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)



All data presented in two's-complement form with MSB first.

図 62. Right-Justified 48-f_S Format

2-Channel Right-Justified (Sony Format) Stereo Input



All data presented in two's-complement form with MSB first.

図 63. Right-Justified 32-f_S Format

7.6.3 26-Bit 3.23 Number Format

All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. Numbers formatted as 3.23 numbers mean that the binary point has 3 bits to the left and 23 bits to the right. This is shown in 図 64.

Programming (continued)

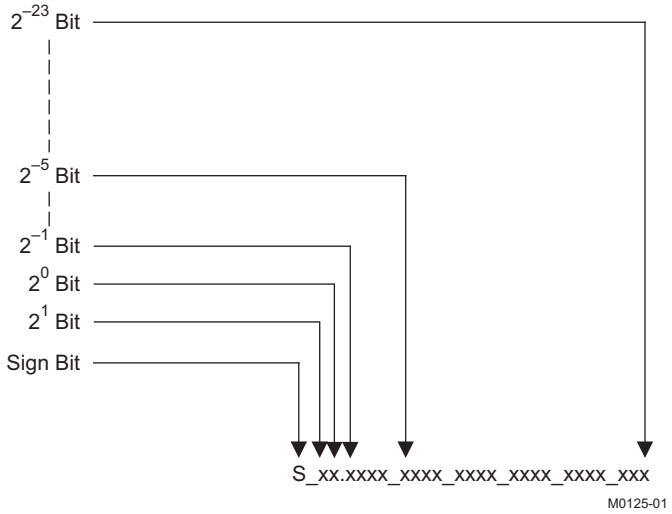


図 64. 3.23 Format

The decimal value of a 3.23 format number can be found by following the weighting shown in 図 64. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In the case every bit must be inverted, a 1 added to the result, and then the weighting shown in 図 65 applies to obtain the magnitude of the negative number.

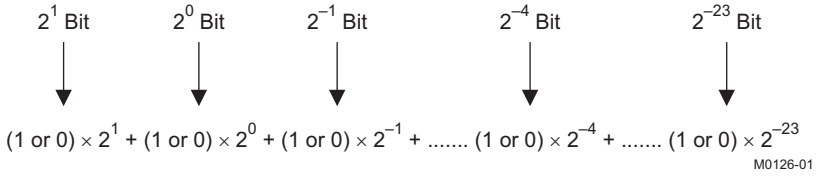


図 65. Conversion Weighting Factors—3.23 Format to Floating Point

Gain coefficients, entered via the I²C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in 図 66.

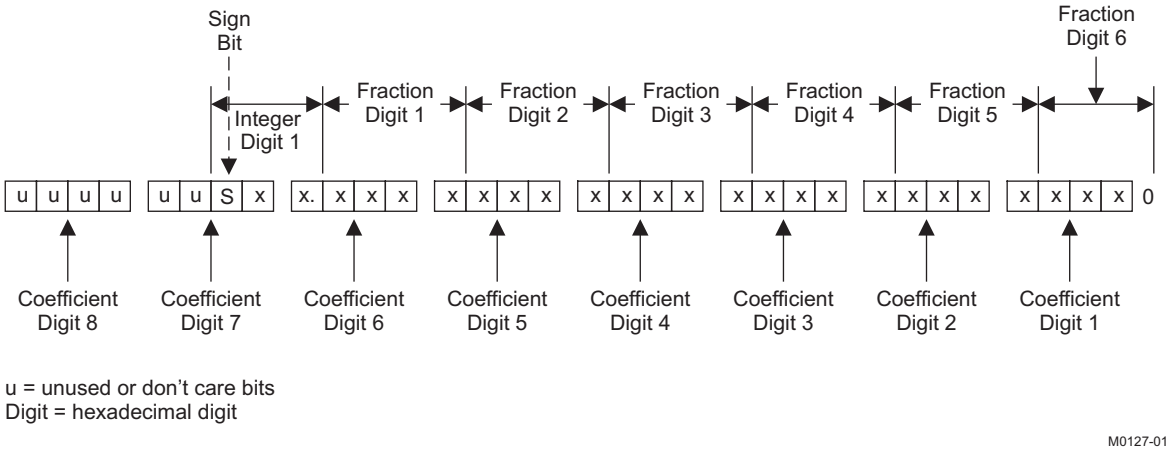


図 66. Alignment of 3.23 Coefficient in 32-Bit I²C Word

表 3. Sample Calculation for 3.23 Format

db	Linear	Decimal	Hex (3.23 Format)
0	1	8,388,608	80 0000
5	1.77	14,917,288	00E3 9EA8
–5	0.56	4,717,260	0047 FACC
X	$L = 10^{(X / 20)}$	D = 8,388,608 × L	H = dec2hex (D, 8)

表 4. Sample Calculation for 9.17 Format

db	Linear	Decimal	Hex (9.17 Format)
0	1	131,072	2 0000
5	1.77	231,997	3 8A3D
–5	0.56	73,400	1 1EB8
X	$L = 10^{(X / 20)}$	D = 131,072 × L	H = dec2hex (D, 8)

7.7 Register Maps

7.7.1 Register Summary

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
			A u indicates unused bits.	
0x00	Clock control register	1	Description shown in subsequent section	0x6C
0x01	Device ID register	1	Description shown in subsequent section	0x40
0x02	Error status register	1	Description shown in subsequent section	0x00
0x03	System control register 1	1	Description shown in subsequent section	0xA0
0x04	Serial data interface register	1	Description shown in subsequent section	0x05
0x05	System control register 2	1	Description shown in subsequent section	0x40
0x06	Soft mute register	1	Description shown in subsequent section	0x00
0x07	Master volume	2	Description shown in subsequent section	0x03FF (mute)
0x08	Channel 1 vol	2	Description shown in subsequent section	0x00C0 (0 dB)
0x09	Channel 2 vol	2	Description shown in subsequent section	0x00C0 (0 dB)
0x0A	Channel 3 vol	2	Description shown in subsequent section	0x00C0 (0 dB)
0x0B	Reserved	2	Reserved(1)	0x03FF
0x0C		2	Reserved(1)	0x00C0
0x0D		1	Reserved(1)	0xC0
0x0E	Volume configuration register	1	Description shown in subsequent section	0xF0
0x0F	Reserved	1	Reserved(1)	0x97
0x10	Modulation limit register	1	Description shown in subsequent section	0x01
0x11	IC delay channel 1	1	Description shown in subsequent section	0xAC
0x12	IC delay channel 2	1	Description shown in subsequent section	0x54
0x13	IC delay channel 3	1	Description shown in subsequent section	0xAC
0x14	IC delay channel 4	1	Description shown in subsequent section	0x54
0x15	Reserved	1	Reserved(1)	0xAC
0x16				0x54
0x17				0x00
0x18	PWM Start			0x0F
0x19	PWM Shutdown Group Register	1	Description shown in subsequent section	0x30
0x1A	Start/stop period register	1	Description shown in subsequent section	0x68
0x1B	Oscillator trim register	1	Description shown in subsequent section	0x82

(1) Do not access reserved registers.

Register Maps (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x1C	BKND_ERR register	1	Description shown in subsequent section	0x57
0x1D–0x1F		1	Reserved (1)	0x00
0x20	Input MUX register	4	Description shown in subsequent section	0x0001 7772
0x21	Reserved	4	Reserved (1)	0x0000 4303
0x22		4		0x0000 0000
0x23		4		0x0000 0000
0x24		4		0x0000 0000
0x25	PWM MUX register	4	Description shown in subsequent section	0x0102 1345
0x26	ch1_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x27	ch1_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x28	ch1_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x29	ch1_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2A	ch1_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2B	ch1_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2C	ch1_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Register Maps (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x2D	ch1_bq[7]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2E	ch1_bq[8]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2F	ch1_bq[9]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x30	ch2_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x31	ch2_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x32	ch2_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x33	ch2_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x34	ch2_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x35	ch2_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Register Maps (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x36	ch2_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x37	ch2_bq[7]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x38	ch2_bq[8]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x39	ch2_bq[9]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x3A	Reserved	4	Reserved(1)	0x0080 0000 0000 0000
0x3B	AGL1 softening filter alpha	8	u[31:26], ae[25:0]	0x0008 0000
	AGL1 softening filter omega		u[31:26], oe[25:0]	0x0078 0000
0x3C	AGL1 attack rate	8	Description shown in subsequent section	0x0000 0100
	AGL1 release rate		Description shown in subsequent section	0xFFFF FF00

Register Maps (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x3D		8	Reserved (1)	
0x3E	AGL2 softening filter alpha	8	u[31:26], ae[25:0]	0x0008 0000
	AGL2 softening filter omega		u[31:26], oe[25:0]	0x0078 0000
0x3F	AGL2 attack rate	8	u[31:26], at[25:0]	0x0008 0000
	AGL2 release rate		u[31:26], rt[25:0]	0xFFF8 0000
0x40	AGL1 attack threshold	4	T1[31:0] (9.23 format)	0x0800 0000
0x41	AGL3 attack threshold	4	T1[31:0] (9.23 format)	0x0074 0000
0x42	AGL3 attack rate	8	Description shown in subsequent section	0x0008 0000
	AGL3 release rate		Description shown in subsequent section	0xFFF8 0000
0x43	AGL2 attack threshold	4	T2[31:0] (9.23 format)	0x0074 0000
0x44	AGL4 attack threshold	4	T1[31:0] (9.23 format)	0x0074 0000
0x45	AGL4 attack rate	8		0x0008 0000
	AGL4 release rate			0xFFF8 0000
0x46	AGL control	4	Description shown in subsequent section	0x0002 0000
0x47	AGL3 softening filter alpha	8	u[31:26], ae[25:0]	0x0008 0000
	AGL3 softening filter omega		u[31:26], oe[25:0]	0x0078 0000
0x48	AGL4 softening filter alpha	8	u[31:26], ae[25:0]	0x0008 0000
	AGL4 softening filter omega		u[31:26], oe[25:0]	0x0078 0000
0x49	Reserved	4	Reserved (1)	
0x4A		4		0x1212 1010 E1FF FFFF F95E 1212
0x4B		4		0x0000 296E
0x4C		4		0x0000 5395
0x4D		4		0x0000 0000
0x4E		4		0x0000 0000
0x4F	PWM switching rate control	4	u[31:4], src[3:0]	0x0000 0008
0x50	Bank switch control	4	Description shown in subsequent section	0x0F70 8000
0x51	Ch 1 output mixer	12	Ch 1 output mix1[2]	0x0080 0000
			Ch 1 output mix1[1]	0x0000 0000
			Ch 1 output mix1[0]	0x0000 0000
0x52	Ch 2 output mixer	12	Ch 2 output mix2[2]	0x0080 0000
			Ch 2 output mix2[1]	0x0000 0000
			Ch 2 output mix2[0]	0x0000 0000
0x53		16	Reserved (1)	0x0080 0000 0000 0000 0000 0000
0x54		16	Reserved (1)	0x0080 0000 0000 0000 0000 0000
0x56	Output post-scale	4	u[31:26], post[25:0]	0x0080 0000
0x57	Output pre-scale	4	u[31:26], pre[25:0] (9.17 format)	0x0002 0000
0x58	ch1_bq[10]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Register Maps (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x59	ch1_cross_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			ch1_cross_bq[1]	0x0000 0000
			ch1_cross_bq[2]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5A	ch1_cross_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5B	ch1_cross_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5C	ch1_cross_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5D	ch2_bq[10]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5E	ch2_cross_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5F	ch2_cross_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x60	ch2_cross_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x61	ch2_cross_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x62	IDF post scale	4	Description shown in subsequent section	0x0000 0080

Register Maps (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x63–0x69	Reserved	4	Reserved(1)	0x0000 0000
0x6A		4		0x0000 8312
0x6B	Left channel PWM level meter	4	Data[31:0]	0x007F 7CED
0x6C	Right channel PWM level meter	4	Data[31:0]	0x0000 0000
0x6D	Reserved	8	Reserved(1)	0x0000 0000 0000 0000
0x6E–0x6F		4		0x0000 0000
0x70	ch1 inline mixer	4	u[31:26], in_mix1[25:0]	0x0080 0000
0x71	inline_AGL_en_mixer_ch1	4	u[31:26], in_mixagl_1[25:0]	0x0000 0000
0x72	ch1 right_channel mixer	4	u[31:26], right_mix1[25:0]	0x0000 0000
0x73	ch1 left_channel_mixer	4	u[31:26], left_mix_1[25:0]	0x0080 0000
0x74	ch2 inline mixer	4	u[31:26], in_mix2[25:0]	0x0080 0000
0x75	inline_AGL_en_mixer_ch2	4	u[31:26], in_mixagl_2[25:0]	0x0000 0000
0x76	ch2 left_chanel mixer	4	u[31:26], left_mix1[25:0]	0x0000 0000
0x77	ch2 right_channel_mixer	4	u[31:26], right_mix_1[25:0]	0x0080 0000
0x78–0xF7			Reserved(1)	0x0000 0000
0xF8	Update device address key	4	Dev Id Update Key[31:0] (Key = 0xF9A5A5A5)	0x0000 0054
0xF9	Update device address	4	u[31:8],New Dev Id[7:0] (New Dev Id = 0x54 for TAS5751M)	0x0000 0054
0xFA–0xFF		4	Reserved(1)	0x0000 0000

All DAP coefficients are 3.23 format unless specified otherwise.

Registers 0x3B through 0x46 should be altered only during the initialization phase.

7.7.2 Detailed Register Descriptions

7.7.2.1 Clock Control Register (0x00)

The clocks and data rates are automatically determined by the TAS5751M. The clock control register contains the autodetected clock status. Bits D7–D5 reflect the sample rate. Bits D4–D2 reflect the MCLK frequency.

Table 5. Clock Control Register (0x00)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	–	–	–	–	–	f_S = 32-kHz sample rate
0	0	1	–	–	–	–	–	Reserved
0	1	0	–	–	–	–	–	Reserved
0	**1**	**1**	**–**	**–**	**–**	**–**	**–**	**f_S = 44.1/48-kHz sample rate**(1)
1	0	0	–	–	–	–	–	f_S = 16-kHz sample rate
1	0	1	–	–	–	–	–	f_S = 22.05/24-kHz sample rate
1	1	0	–	–	–	–	–	f_S = 8-kHz sample rate
1	1	1	–	–	–	–	–	f_S = 11.025/12-kHz sample rate
–	–	–	0	0	0	–	–	MCLK frequency = 64 × f_S(2)
–	–	–	0	0	1	1	–	MCLK frequency = 128 × f_S(2)
0	0	0	0	1	0	0	0	MCLK frequency = 192 × f_S(3)
–	**–**	**–**	**0**	**1**	**1**	**–**	**–**	**MCLK frequency = 256 × f_S**(1)(4)

(1) Default values are in **bold**.
(2) Only available for 44.1-kHz and 48-kHz rates
(3) Rate only available for 32/44.1/48-KHz sample rates
(4) Not available at 8 kHz

Table 5. Clock Control Register (0x00) (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	1	0	0	–	–	MCLK frequency = 384 × f_S
–	–	–	1	0	1	–	–	MCLK frequency = 512 × f_S
–	–	–	1	1	0	–	–	Reserved
–	–	–	1	1	1	–	–	Reserved
–	**–**	**–**	**–**	**–**	**–**	**0**	**–**	**Reserved**
–	**–**	**–**	**–**	**–**	**–**	**–**	**0**	**Reserved**

7.7.2.2 Device ID Register (0x01)

The device ID register contains the ID code for the firmware revision.

Table 6. General Status Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Identification code** (1)

(1) Default values are in **bold**.

7.7.2.3 Error Status Register (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error definitions:

- MCLK error: MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
- SCLK error: The number of SCLKs per LRCLK is changing.
- LRCLK error: LRCLK frequency is changing.
- Frame slip: LRCLK phase is drifting with respect to internal frame sync.

Table 7. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	-	–	–	–	–	–	–	MCLK error
–	1	–	–	–	–	–	–	PLL autolock error
–	–	1	–	–	–	–	–	SCLK error
–	–	–	1	–	–	–	–	LRCLK error
–	–	–	–	1	–	–	–	Frame slip
–	–	–	–	–	1	–	–	Clip indicator
–	–	–	–	–	–	1	–	Overcurrent, overtemperature, overvoltage, or undervoltage error
0	0	0	0	0	0	0	0	Reserved
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**No errors** (1)

(1) Default values are in **bold**.

7.7.2.4 System Control Register 1 (0x03)

System control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.
If 1, the dc-blocking filter (–3 dB cutoff <1 Hz) for each channel is enabled.

Bit D5: If 0, use soft unmute on recovery from a clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E.
If 1, use hard unmute on recovery from clock error. This is a fast recovery, a single-step volume ramp.

Bits D1–D0: Select de-emphasis

Table 8. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	PWM high-pass (dc blocking) disabled
1	–	–	–	–	–	–	–	**PWM high-pass (dc blocking) enabled** (1)
–	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	**1**	–	–	–	–	–	**Soft unmute on recovery from clock error** (1)
–	–	1	–	–	–	–	–	Hard unmute on recovery from clock error
–	–	–	**0**	–	–	–	–	**Reserved** (1)
–	–	–	–	**0**	–	–	–	**Reserved** (1)
–	–	–	–	–	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	**0**	**0**	**No de-emphasis** (1)
–	–	–	–	–	–	0	1	De-emphasis for f_S = 32 kHz
–	–	–	–	–	–	1	0	De-emphasis for f_S = 44.1 kHz
–	–	–	–	–	–	1	1	De-emphasis for f_S = 48 kHz

(1) Default values are in **bold**.

7.7.2.5 Serial Data Interface Register (0x04)

As shown in Table 9, the TAS5751M supports nine serial data modes. The default is 24-bit, I^2S mode.

Table 9. Serial Data Interface Control Register (0x04) Format

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTH	D7–D4	D3	D2	D1	D0
Right-justified	16	0000	0	0	0	0
Right-justified	20	0000	0	0	0	1
Right-justified	24	0000	0	0	1	0
I^2S	16	000	0	0	1	1
I^2S	20	0000	0	1	0	0
I^2S (1)	**24**	**0000**	**0**	**1**	**0**	**1**
Left-justified	16	0000	0	1	1	0
Left-justified	20	0000	0	1	1	1
Left-justified	24	0000	1	0	0	0
Reserved		0000	1	0	0	1
Reserved		0000	1	0	1	0
Reserved		0000	1	0	1	1
Reserved		0000	1	1	0	0
Reserved		0000	1	1	0	1
Reserved		0000	1	1	1	0
Reserved		0000	1	1	1	1

(1) Default values are in **bold**.

7.7.2.6 System Control Register 2 (0x05)

When bit D6 is set low, the system exits all-channel shutdown and starts playing audio; otherwise, the outputs are shut down (hard mute).

Table 10. System Control Register 2 (0x05)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Mid-Z ramp disabled** (1)
1	–	–	–	–	–	–	–	Mid-Z ramp enabled
–	0	–	–	–	–	–	–	Exit all-channel shutdown (normal operation)
–	**1**	–	–	–	–	–	–	**Enter all-channel shutdown (hard mute)** (1)
–	–	**0**	**0**	–	**–**	**–**	–	**Reserved** (1)
				0	**–**	**–**	–	**Ternary modulation disabled** (1)
–	–	–	–	1	–	–	–	Ternary modulation enabled
–	–	–	–	–	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	**0**	–	configured as input
–	–	–	–	–	–	1	–	configured configured as output to function as fault output pin.
–	–	–	–	–	–	–	**0**	**Reserved** (1)

(1) Default values are in **bold**.

Ternary modulation is disabled by default. To enable ternary modulation, the following writes are required before bringing the system out of shutdown:

1. Set bit D3 of register 0x05 to 1.
2. Write the following ICD settings:
   a. 0x11= 80
   b. 0x12= 7C
   c. 0x13= 80
   d. 0x14 =7C
3. Set the input mux register as follows:
   a. 0x20 = 00 89 77 72

7.7.2.7 Soft Mute Register (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

Table 11. Soft Mute Register (0x06)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	–	–	–	**Reserved** (1)
–	–	–	–	–	1	–	–	Soft mute channel 3
–	–	–	–	–	**0**	–	–	**Soft unmute channel 3** (1)
–	–	–	–	–	–	1	–	Soft mute channel 2
–	–	–	–	–	–	**0**	–	**Soft unmute channel 2** (1)
–	–	–	–	–	–	–	1	Soft mute channel 1
–	–	–	–	–	–	–	**0**	**Soft unmute channel 1** (1)

(1) Default values are in **bold**.

7.7.2.8 Volume Registers (0x07, 0x08, 0x09)

The volume register 0x07, 0x08, and 0x09 correspond to master volume, channel 1 volume, and channel 2 volume, respectively. Step size is 0.125 dB and volume registers are 2 bytes.

Master volume – 0x07 (default is mute, 0x03FF)

Channel-1 volume – 0x08 (default is 0 dB, 0x00C0)

Channel-2 volume – 0x09 (default is 0 dB, 0x00C0)

Table 12. Master Volume Table

Value	Level
0x0000	24.000
0x0001	23.875
...	(0.125 dB steps)
0x03FE	–103.750
0x03FF	Mute

7.7.2.9 Volume Configuration Register (0x0E)

Bits D2–D0: Volume slew rate (used to control volume change and MUTE ramp rates). These bits control the number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the I^2S data as follows:

Sample rate (kHz)	Approximate ramp rate
8/16/32	125 μs/step
11.025/22.05/44.1	90.7 μs/step
12/24/48	83.3 μs/step

In two-band AGL, register 0x0A should be set to 0x30 and register 0x0E bits 6 and 5 should be set to 1.

Table 13. Volume Configuration Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	**Reserved** (1)
–	0	–	–	–	–	–	–	AGL2 volume 1 (ch4) from I^2C register 0x08
–	**1**	–	–	–	–	–	–	**AGL2 volume 1 (ch4) from I^2C register 0x0A** (1)
–	–	0	–	–	–	–	–	AGL2 volume 2 (ch3) from I^2C register 0x09
–	–	**1**	–	–	–	–	–	**AGL2 volume 2 (ch3) from I^2C register 0x0A** (1)
–	–	–	**1**	**0**	–	–	–	**Reserved** (1)
–	–	–	–	–	**0**	**0**	**0**	**Volume slew 512 steps (43 ms volume ramp time at 48 kHz)** (1)
–	–	–	–	–	0	0	1	Volume slew 1024 steps (85-ms volume ramp time at 48 kHz)
–	–	–	–	–	0	1	0	Volume slew 2048 steps (171-ms volume ramp time at 48 kHz)
–	–	–	–	–	0	1	1	Volume slew 256 steps (21-ms volume ramp time at 48 kHz)
–	–	–	–	–	1	X	X	Reserved

(1) Default values are in **bold**.

7.7.2.10 Modulation Limit Register (0x10)

Table 14. Modulation Limit Register (0x10)

D7	D6	D5	D4	D3	D2	D1	D0	MODULATION LIMIT
0	**0**	**0**	**0**	**0**	–	–	–	Reserved
–	–	–	–	–	0	0	0	Reserved
–	–	–	–	–	**0**	**0**	**1**	**98.4%**(1)
–	–	–	–	–	0	1	0	97.7%
–	–	–	–	–	0	1	1	96.9%
–	–	–	–	–	1	0	0	96.1%
–	–	–	–	–	1	0	1	95.3%
–	–	–	–	–	1	1	0	94.5%
–	–	–	–	–	1	1	1	93.8%

(1) Default values are in **bold**.

7.7.2.11 Interchannel Delay Registers (0x11, 0x12, 0x13, and 0x14)

Internal PWM channels 1, 2, $\overline{1}$, and $\overline{2}$ are mapped into registers 0x11, 0x12, 0x13, and 0x14.

Table 15. Channel Interchannel Delay Register Format

BITS DEFINITION	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	–	–	Minimum absolute delay, 0 DCLK cycles
	0	1	1	1	1	1	–	–	Maximum positive delay, 31 × 4 DCLK cycles
	1	0	0	0	0	0	–	–	Maximum negative delay, –32 × 4 DCLK cycles
							0	0	Reserved
SUBADDRESS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Delay = (value) × 4 DCLKs**
0x11	**1**	**0**	**1**	**0**	**1**	**1**	–	–	**Default value for channel 1** (1)
0x12	**0**	**1**	**0**	**1**	**0**	**1**	–	–	**Default value for channel 2** (1)
0x13	**1**	**0**	**1**	**0**	**1**	**1**	–	–	**Default value for $\overline{\text{channel 1}}$** (1)
0x14	**0**	**1**	**0**	**1**	**0**	**1**	–	–	**Default value for $\overline{\text{channel 2}}$** (1)

(1) Default values are in **bold**.

ICD settings have high impact on audio performance (e.g., dynamic range, THD, crosstalk, etc.) Therefore, appropriate ICD settings must be used. By default, the device has ICD settings for the AD mode. If used in BD mode, then update these registers before coming out of all-channel shutdown.

MODE	AD MODE	BD MODE
0x11	AC	B8
0x12	54	60
0x13	AC	A0
0x14	54	48

7.7.2.12 PWM Shutdown Group Register (0x19)

Settings of this register determine which PWM channels are active. The functionality of this register is tied to the state of bit D5 in the system control register.

This register defines which channels belong to the shutdown group. If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D5 is set to 0 in system control register 2, 0x05).

Table 16. PWM Shutdown Group Register (0x19)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Reserved** (1)
–	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	**1**	–	–	–	–	–	**Reserved** (1)
–	–	–	**1**	–	–	–	–	**Reserved** (1)
–	–	–	–	**0**	–	–	–	**PWM channel 4 does not belong to shutdown group.** (1)
–	–	–	–	1	–	–	–	PWM channel 4 belongs to shutdown group.
–	–	–	–	–	**0**	–	–	**PWM channel 3 does not belong to shutdown group.** (1)
–	–	–	–	–	1	–	–	PWM channel 3 belongs to shutdown group.
–	–	–	–	–	–	**0**	–	**PWM channel 2 does not belong to shutdown group.** (1)
–	–	–	–	–	–	1	–	PWM channel 2 belongs to shutdown group.
–	–	–	–	–	–	–	**0**	**PWM channel 1 does not belong to shutdown group.** (1)
–	–	–	–	–	–	–	1	PWM channel 1 belongs to shutdown group.

(1) Default values are in **bold**.

7.7.2.13 Start/Stop Period Register (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all-channel shutdown command or change in the $\overline{\text{PDN}}$ state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I^2S clock stability.

Table 17. Start/Stop Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**–**	**–**	–	–	–	–	–	**SSTIMER enabled** (1)
1	–	–	–	–	–	–	–	SSTIMER disabled
–	**1**	**1**	–	–	–	–	–	**Reserved** (1)
–	–	–	0	0	–	–	–	No 50% duty cycle start/stop period
–	**–**	**–**	**0**	**1**	**0**	**0**	**0**	**16.5-ms 50% duty cycle start/stop period**
–	–	–	0	1	0	0	1	23.9-ms 50% duty cycle start/stop period
–	–	–	0	1	0	1	0	31.4-ms 50% duty cycle start/stop period
–	–	–	0	1	0	1	1	40.4-ms 50% duty cycle start/stop period
–	–	–	0	1	1	0	0	53.9-ms 50% duty cycle start/stop period
–	–	–	0	1	1	0	1	70.3-ms 50% duty cycle start/stop period
–	–	–	0	1	1	1	0	94.2-ms 50% duty cycle start/stop period
–	–	–	0	1	1	1	1	125.7-ms 50% duty cycle start/stop period (1)
–	–	–	1	0	0	0	0	164.6-ms 50% duty cycle start/stop period
–	–	–	1	0	0	0	1	239.4-ms 50% duty cycle start/stop period
–	–	–	1	0	0	1	0	314.2-ms 50% duty cycle start/stop period
–	–	–	1	0	0	1	1	403.9-ms 50% duty cycle start/stop period
–	–	–	1	0	1	0	0	538.6-ms 50% duty cycle start/stop period
–	–	–	1	0	1	0	1	703.1-ms 50% duty cycle start/stop period
–	–	–	1	0	1	1	0	942.5-ms 50% duty cycle start/stop period
–	–	–	1	0	1	1	1	1256.6-ms 50% duty cycle start/stop period
–	–	–	1	1	0	0	0	1728.1-ms 50% duty cycle start/stop period
–	–	–	1	1	0	0	1	2513.6-ms 50% duty cycle start/stop period
–	–	–	1	1	0	1	0	3299.1-ms 50% duty cycle start/stop period
–	–	–	1	1	0	1	1	4241.7-ms 50% duty cycle start/stop period
–	–	–	1	1	1	0	0	5655.6-ms 50% duty cycle start/stop period
–	–	–	1	1	1	0	1	7383.7-ms 50% duty cycle start/stop period

(1) Default values are in **bold**.

Table 17. Start/Stop Period Register (0x1A) (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	1	1	1	1	0	9897.3-ms 50% duty cycle start/stop period
–	–	–	1	1	1	1	1	13,196.4-ms 50% duty cycle start/stop period

7.7.2.14 Oscillator Trim Register (0x1B)

The TAS5751M PWM processor contains an internal oscillator to support autodetect of I^2S clock rates. This reduces system cost because an external reference is not required. A reference resistor must be connected between pin 16 and 17, as shown in Table 18.

Writing 0x00 to register 0x1B enables the trim that was programmed at the factory.

Note that trim must always be run following reset of the device.

Table 18. Oscillator Trim Register (0x1B)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	**Reserved** (1)
–	**0**	–	–	–	–	–	–	**Oscillator trim not done (read-only)** (1)
–	1	–	–	–	–	–	–	Oscillator trim done (read only)
–	–	**0**	**0**	**0**	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	0	–	Select factory trim (Write a 0 to select factory trim; default is 1.)
–	–	–	–	–	–	**1**	–	**Factory trim disabled** (1)
–	–	–	–	–	–	–	**0**	**Reserved** (1)

(1) Default values are in **bold**.

7.7.2.15 BKND_ERR Register (0x1C)

When a back-end error signal is received from the internal power stage, the power stage is reset, stopping all PWM activity. Subsequently, the modulator waits approximately for the time listed in Table 19 before attempting to re-start the power stage.

Table 19. BKND_ERR Register (0x1C)(1)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**1**	**0**	**1**	**x**	**x**	**x**	**X**	**Reserved**
–	–	–	–	0	0	1	0	Set back-end reset period to 299 ms(2)
–	–	–	–	0	0	1	1	Set back-end reset period to 449 ms
–	–	–	–	0	1	0	0	Set back-end reset period to 598 ms
–	–	–	–	0	1	0	1	Set back-end reset period to 748 ms
–	–	–	–	0	1	1	0	Set back-end reset period to 898 ms
–	–	–	–	0	1	1	1	Set back-end reset period to 1047 ms
–	–	–	–	1	0	0	0	Set back-end reset period to 1197 ms
–	–	–	–	1	0	0	1	Set back-end reset period to 1346 ms
–	–	–	–	1	0	1	X	Set back-end reset period to 1496 ms
–	**–**	**–**	**–**	**1**	**1**	**1**	**X**	**Set back-end reset period to 1496 ms**

(1) This register can be written only with a non-reserved value. The RSTz pin must be toggled between subsequent writes to this register.
(2) Default values are in **bold**.

7.7.2.16 Input Multiplexer Register (0x20)

This register controls the modulation scheme (AD or BD mode) as well as the routing of I^2S audio to the internal channels.

Table 20. Input Multiplexer Register (0x20)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	–	–	–	–	–	–	–	**Channel-1 AD mode** (1)
1	–	–	–	–	–	–	–	Channel-1 BD mode
–	**0**	**0**	**0**	–	–	–	–	**SDIN-L to channel 1** (1)
–	0	0	1	–	–	–	–	SDIN-R to channel 1
–	0	1	0	–	–	–	–	Reserved
–	0	1	1	–	–	–	–	Reserved
–	1	0	0	–	–	–	–	Reserved
–	1	0	1	–	–	–	–	Reserved
–	1	1	0	–	–	–	–	Ground (0) to channel 1
–	1	1	1	–	–	–	–	Reserved
–	–	–	–	**0**	–	–	–	**Channel 2 AD mode** (1)
–	–	–	–	1	–	–	–	Channel 2 BD mode
–	–	–	–	–	0	0	0	SDIN-L to channel 2
–	–	–	–	–	**0**	**0**	**1**	**SDIN-R to channel 2** (1)
–	–	–	–	–	0	1	0	Reserved
–	–	–	–	–	0	1	1	Reserved
–	–	–	–	–	1	0	0	Reserved
–	–	–	–	–	1	0	1	Reserved
–	–	–	–	–	1	1	0	Ground (0) to channel 2
–	–	–	–	–	1	1	1	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**Reserved** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**Reserved** (1)

(1) Default values are in **bold**.

7.7.2.17 PWM Output MUX Register (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21–D20: Selects which PWM channel is output to AMP_OUT_A

Bits D17–D16: Selects which PWM channel is output to AMP_OUT_B

Bits D13–D12: Selects which PWM channel is output to AMP_OUT_C

Bits D09–D08: Selects which PWM channel is output to AMP_OUT_D

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 4 = 0x03.

Table 21. PWM Output MUX Register (0x25)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**Reserved** (1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	–	–	–	–	–	–	**Reserved** (1)
–	**–**	**0**	**0**	–	–	–	–	**Multiplex channel 1 to AMP_OUT_A** (1)
–	–	0	1	–	–	–	–	Multiplex channel 2 to AMP_OUT_A
–	–	1	0	–	–	–	–	Multiplex $\overline{\text{channel 1}}$ to AMP_OUT_A
–	–	1	1	–	–	–	–	Multiplex $\overline{\text{channel 2}}$ to AMP_OUT_A
–	–	–	–	**0**	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	0	0	Multiplex channel 1 to AMP_OUT_B
–	–	–	–	–	–	0	1	Multiplex channel 2 to AMP_OUT_B
–	–	–	–	–	–	**1**	**0**	**Multiplex $\overline{\text{channel 1}}$ to AMP_OUT_B** (1)
–	–	–	–	–	–	1	1	Multiplex $\overline{\text{channel 2}}$ to AMP_OUT_B
D15	**D14**	**D13**	**D12**	**D11**	**D 10**	**D9**	**D8**	**FUNCTION**
0	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	0	0	–	–	–	–	Multiplex channel 1 to AMP_OUT_C
–	–	**0**	**1**	–	–	–	–	**Multiplex channel 2 to AMP_OUT_C** (1)
–	–	1	0	–	–	–	–	Multiplex $\overline{\text{channel 1}}$ to AMP_OUT_C
–	–	1	1	–	–	–	–	Multiplex $\overline{\text{channel 2}}$ to AMP_OUT_C
–	–	–	–	**0**	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	0	0	Multiplex channel 1 to AMP_OUT_D
–	–	–	–	–	–	0	1	Multiplex channel 2 to AMP_OUT_D
–	–	–	–	–	–	1	0	Multiplex $\overline{\text{channel 1}}$ to AMP_OUT_D
–	–	–	–	–	–	**1**	**1**	**Multiplex $\overline{\text{channel 2}}$ to AMP_OUT_D** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**Reserved** (1)

(1) Default values are in **bold**.

7.7.2.18 AGL Control Register (0x46)

Table 22. AGL Control Register (0x46)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	**–**	**–**	–	–	–	–	**Reserved** (1)
–	–	0	–	–	–	–	–	Reserved
–	**–**	**1**	**–**	**–**	**–**	**–**	**–**	**Reserved**
–	–	–	**0**	–	–	–	–	**Reserved** (1)
–	–	–	–	**0**	–	–	–	**AGL4 turned OFF** (1)
–	–	–	–	1	–	–	–	AGL4 turned ON
–	–	–	–	–	**0**	–	–	**AGL3 turned OFF** (1)
–	–	–	–	–	1	–	–	AGL3 turned ON
–	–	–	–	–	–	**0**	–	**AGL2 turned OFF** (1)
–	–	–	–	–	–	1	–	AGL2 turned ON
–	–	–	–	–	–	–	**0**	**AGL1 turned OFF** (1)
–	–	–	–	–	–	–	1	AGL1 turned ON

(1) Default values are in **bold**.

7.7.2.19 PWM Switching Rate Control Register (0x4F)

PWM switching rate should be selected through the register 0x4F before coming out of all-channnel shutdown.

Table 23. PWM Switching Rate Control Register (0x4F)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
–	–	**0**	**0**	–	–	–	–	**Reserved**(1)
–	–	–	–	0	1	1	0	SRC = 6
–	–	–	–	0	1	1	1	SRC = 7
–	**–**	**–**	**–**	**1**	**0**	**0**	**0**	**SRC = 8**(1)
–	–	–	–	1	0	0	1	SRC = 9
–	–	–	–	1	0	1	0	Reserved
–	–	–	–	1	1	–	–	Reserved

(1) Default values are in **bold**.

7.7.2.20 Bank Switch and EQ Control (0x50)

Table 24. Bank Switching Command (0x50)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**Reserved** (1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**Reserved** (1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0								**EQ ON** (1)
1	–	–	–	–	–	–	–	EQ OFF (bypass BQ 1–11 of channels 1 and 2)
–	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	**0**	–	–	–	–	–	**Ignore bank-mapping in bits D31–D8. Use default mapping.** (1)
		1						Use bank-mapping in bits D31–D8.
–	–	–	**0**	–	–	–	–	**L and R can be written independently.** (1)
–	–	–	1	–	–	–	–	L and R are ganged for EQ biquads; a write to the left-channel biquad is also written to the right-channel biquad. (0x29–0x2F is ganged to 0x30–0x36. Also, 0x58–0x5B is ganged to 0x5C–0x5F.
–	–	**–**	**–**	**0**	–	–	–	**Reserved** (1)
–	–	–	–	–	**0**	**0**	**0**	**No bank switching. All updates to DAP** (1)
–	–	–	–	–	0	0	1	Configure bank 1 (32 kHz by default)
–	–	–	–	–	0	1	X	Reserved
–	–	–	–	–	1	X	X	Reserved

(1) Default values are in **bold**.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

As mentioned previously, the TAS5751M device can be used in stereo and mono mode. This section describes the information required to configure the device for several popular configurations and for integrating the TAS5751M device into the larger system.

8.1.1 External Component Selection Criteria

The Supporting Component Requirements table in each application description section lists the details of the supporting required components in each of the System Application Schematics. Where possible, the supporting component requirements have been consolidated to minimize the number of unique components which are used in the design. Component list consolidation is a method to reduce the number of unique part numbers in a design. Consolidation is done to ease inventory management and reduce the manufacturing steps during board assembly. For this reason, some capacitors are specified at a higher voltage than what would normally be required. An example of this is a 50-V capacitor can be used for decoupling of a 3.3-V power supply net.

In this example, a higher voltage capacitor can be used even on the lower voltage net to consolidate all caps of that value into a single component type. Similarly, several unique resistors, all having the same size and value but different power ratings can be consolidated by using the highest rated power resistor for each instance of that resistor value.

While this consolidation can seem excessive, the benefits of having fewer components in the design can far outweigh the trivial cost of a higher voltage capacitor. If lower voltage capacitors are already available elsewhere in the design, they can be used instead of the higher voltage capacitors. In all situations, the voltage rating of the capacitors must be at least 1.45 times the voltage of the voltage which appears across them. The power rating of the capacitors should be 1.5 times to 1.75 times the power dissipated in the capacitors during normal use case.

8.1.1.1 Component Selection Impact on Board Layout, Component Placement, and Trace Routing

Because the layout is important to the overall performance of the circuit, the package size of the components shown in the component list were intentionally chosen to allow for proper board layout, component placement, and trace routing. In some cases, traces are passed in between two surface mount pads or ground plane extends from the TAS5751M device between two pads of a surface mount component and into to the surrounding copper for increased heat-sinking of the device. While components can be offered in smaller or larger package sizes, the package size should remain identical to that used in the application circuit as shown. This consistency ensures that the layout and routing can be matched very closely, optimizing thermal, electromagnetic, and audio performance of the TAS5751M device in circuit in the final system.

8.1.1.2 Amplifier Output Filtering

The TAS5751M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter. The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that do not have other circuits which are sensitive to EMI, a simple ferrite bead or ferrite bead and capacitor can replace the traditional large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be preferred due to audio characteristics. Refer to the application report *Class-D Filter Design* (SLOA119) for a detailed description of proper component selection and design of an L-C filter based upon the desired load and response.

8.2 Typical Applications

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases. Each of these configurations can be realized using the Evaluation Module (EVM) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

8.2.1 Stereo Bridge Tied Load Application

A stereo system generally refers to a system inside which are two full range speakers without a separate amplifier path for the speakers that reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

The Stereo BTL Configuration is shown in 図 67.

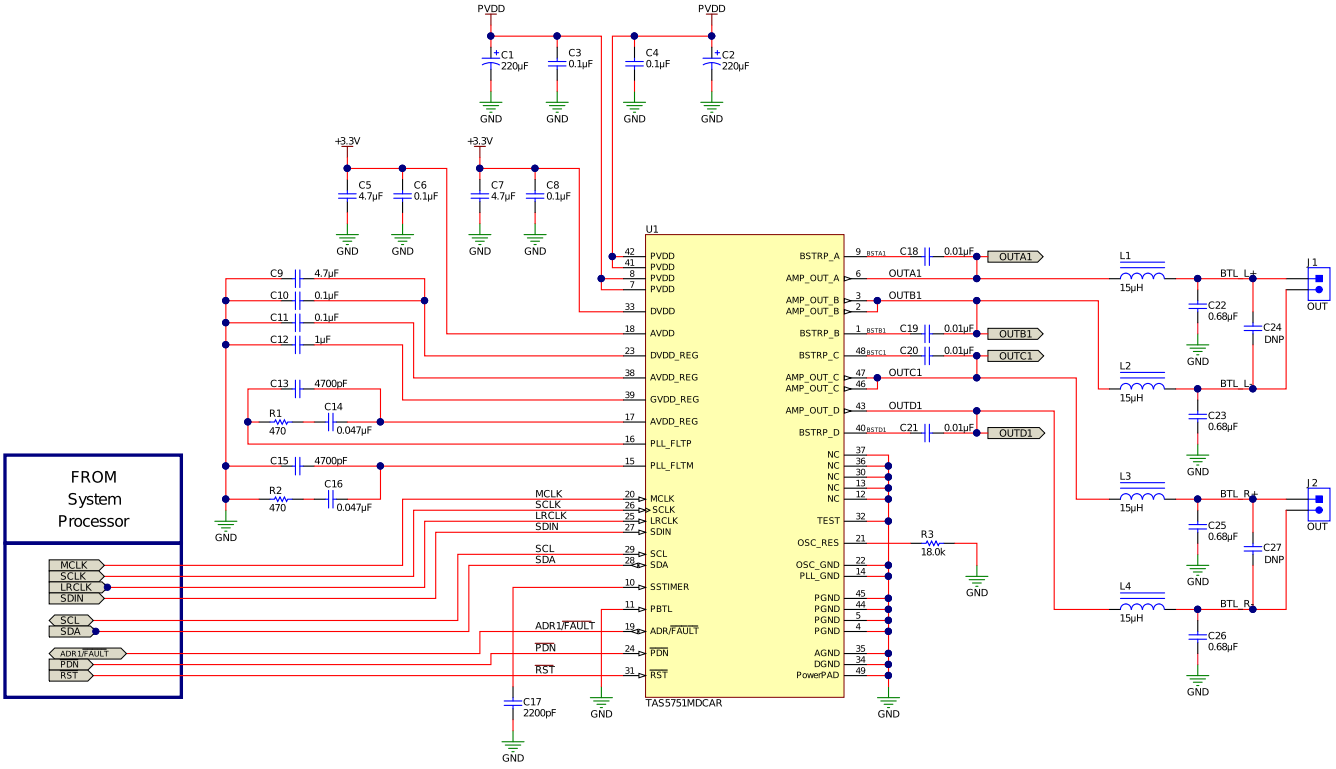


図 67. Stereo Bridge Tied Load Application

Typical Applications (continued)

8.2.1.1 Design Requirements

The design requirements for the Stereo Bridge Tied Load Application of the TAS5751M device is found in 表 25

表 25. Design Requirements for Stereo Bridge Tied Load Application

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	8 V to 24 V
Digital	I²S Compliant Master
	I²C Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter (1)
Speaker	4 Ω minimum.

(1) Refer to SLOA119 for a detailed description on the filter design.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Component Selection and Hardware Connections

The typical connections required for proper operation of the device can be found on the TAS5751M User's Guide. The device was tested with this list of components, deviation from this typical application components unless recommended by this document can produce unwanted results, which could range from degradation of audio performance to destructive failure of the device. The application report *Class-D Filter Design* (SLOA119) offers a detailed description of proper component selection and design of the output filter based upon the modulation used, desired load and response.

8.2.1.2.2 Control and Software Integration

The TAS5751M device has a bidirectional I²C used to program the registers of the device and to read device status. The TAS5751MEVM and the PurePath Console GUI are powerful tools that allow the TAS5751M evaluation, control and configuration. The Register Dump feature of the PurePath Console software can be used to generate a custom configuration file for any end-system operating mode. Prior approval is required to download PurePath Console GUI. Please request access at http://www.ti.com/tool/purepathconsole.

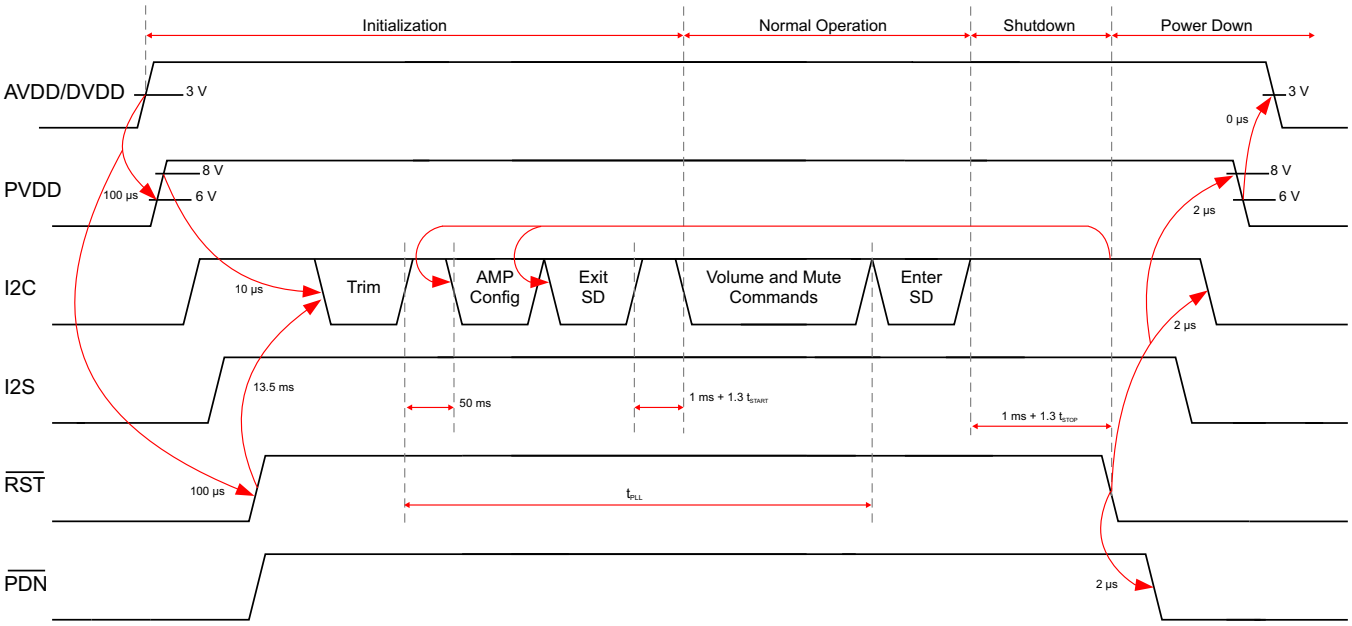
8.2.1.2.3 I²C Pullup Resistors

Customary pullup resistors are required on the SCL and SDA signal lines. They are not shown in the Typical Application Circuits, because they are shared by all of the devices on the I²C bus and are considered to be part of the associated passive components for the System Processor. These resistor values should be chosen per the guidance provided in the I²C Specification.

8.2.1.2.4 Digital I/O Connectivity

The digital I/O lines of the TAS5751M are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be HIGH or LOW) is required to be pulled HIGH, it should be connected to DVDD through a pull-up resistor to control the slew rate of the voltage presented to the digital I/O pins. However, having a separate pull-up resistor for each static digital I/O line is not necessary. Instead, a single resistor can be used to tie all static I/O lines HIGH to reduce BOM count.

8.2.1.2.5 Recommended Startup and Shutdown Procedures



t_{PLL} has to be greater than 240 ms + 1.3 t_{START}, after the first trim command following AVDD/DVDD power-up. It does not apply to trim commands following subsequent resets.
t_{START}/t_{STOP} = PWM start/stop time as defined in register 0x1A

図 68. Recommended Start-Up and Shutdown Sequence

8.2.1.2.5.1 Start-Up Sequence

Use the following sequence to power up and initialize the device:

1. Hold all digital inputs low and ramp up AVDD/DVDD to at least 3 V.
2. Initialize digital inputs and PVDD supply as follows:
   - Drive $\overline{RST}$ = 0, $\overline{PDN}$ = 1, and other digital inputs to their desired state. Wait at least 100 µs, drive $\overline{RST}$ high
   - Wait ≥ 13.5 ms.
   - Ramp up PVDD to at least 8 V while ensuring that it remains below 6 V for at least 100 µs after AVDD/DVDD reaches 3 V.
   - Wait ≥ 10 µs.
3. Trim oscillator (write 0x00 to register 0x1B) and wait at least 50 ms.
4. Configure the Digital Audio Processor of the Amplifier via I²C, refer to Section 8.5 Register Maps for more information.
5. Configure remaining registers.
6. Exit shutdown (sequence defined in Shutdown Sequence).

8.2.1.2.5.2 Normal Operation

The following are the only events supported during normal operation:

1. Writes to master/channel volume registers.
2. Writes to soft-mute register.
3. Enter and exit shutdown (sequence defined in Shutdown Sequence).

注

Event 3 is not supported for 240 ms + 1.3 × t_{start} after trim following AVDD/DVDD power-up ramp (where t_{start} is specified by register 0x1A).

8.2.1.2.5.3 Shutdown Sequence

Enter:

1. Write 0x40 to register 0x05.
2. Wait at least 1 ms + 1.3 × t_{stop} (where t_{stop} is specified by register 0x1A).
3. If desired, reconfigure by returning to step 4 of initialization sequence.

Exit:

1. Write 0x00 to register 0x05 (exit shutdown command can not be serviced for as much as 240 ms after trim following AVDD/DVDD power-up ramp).
2. Wait at least 1 ms + 1.3 × t_{start} (where t_{start} is specified by register 0x1A).
3. Proceed with normal operation.

8.2.1.2.5.4 Power-Down Sequence

Use the following sequence to power down the device and its supplies:

1. If time permits, enter shutdown (sequence defined in Shutdown Sequence); else, in case of sudden power loss, assert $\overline{PDN}$ = 0 and wait at least 2 ms.
2. Assert $\overline{RST}$ = 0.
3. Drive digital inputs low and ramp down PVDD supply as follows:
   - Drive all digital inputs low after $\overline{RST}$ has been low for at least 2 µs.
   - Ramp down PVDD while ensuring that it remains above 8 V until $\overline{RST}$ has been low for at least 2 µs.
4. Ramp down AVDD/DVDD while ensuring that it remains above 3 V until PVDD is below 6 V.

8.2.1.3 Application Performance Plots

CURVE TITLE	FIGURE
Output Power Vs Supply Voltage Stereo BTL Mode	図 5
Total Harmonic Distortion + Noise Vs Output Power Stereo BTL Mode	図 22
Total Harmonic Distortion + Noise Vs Frequency Stereo BTL Mode	図 13
Power Efficiency Vs Output Power Stereo BTL Mode	図 25
Crosstalk Vs Frequency Stereo BTL Mode	図 31

8.2.2 Mono Parallel Bridge Tied Load Application

A mono system refers to a system in which the amplifier is used to drive a single loudspeaker. Parallel Bridge Tied Load (PBTL) indicates that the two full-bridge channels of the device are placed in parallel and drive the loudspeaker simultaneously using an identical audio signal. The primary benefit of operating this device in PBTL operation is to reduce the power dissipation and increase the current sourcing capabilities of the amplifier output. In this mode of operation, the current limit of the audio amplifier is approximately doubled while the on-resistance is approximately halved.

The loudspeaker can be a full-range transducer or one that only reproduces the low-frequency content of an audio signal, as in the case of a powered subwoofer. Often in this use case, two stereo signals are mixed together and sent through a low-pass filter to create a single audio signal which contains the low-frequency information of the two channels.

The Mono PBTL Configuration is shown in 図 69.

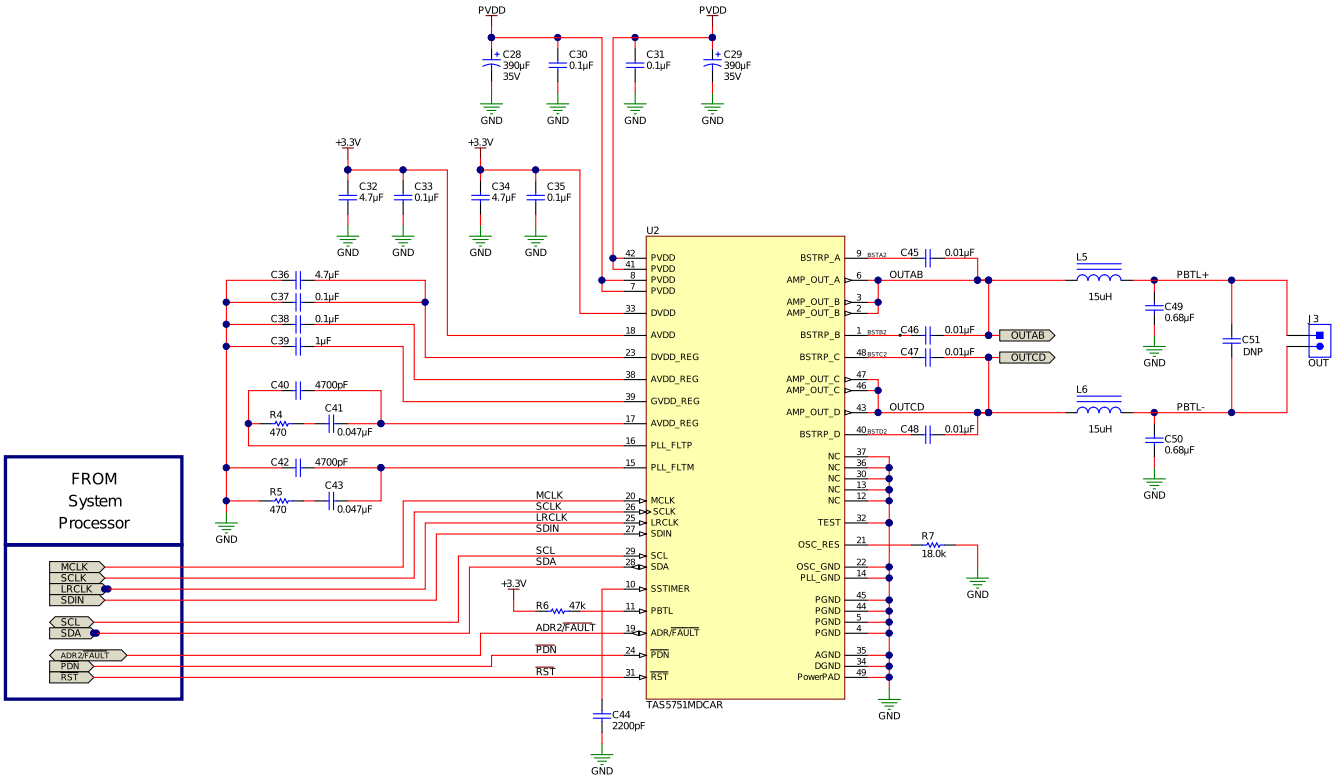


図 69. Mono Parallel Bridge Tied Load Application

8.2.2.1 Design Requirements

The design requirements for the Mono Parallel Bridge Tied Load Appliction of the TAS5751M device is found in 表 26

表 26. Design Requirements for Mono Parallel Bridge Tied Load Application

PARAMETER	EXAMPLE
Low Power Supply	3.3 V
High Power Supply	8 V to 24 V
Digital	I²S Compliant Master
	I²C Compliant Master
	GPIO Control
Output Filters	Inductor-Capacitor Low Pass Filter (1)
Speaker	2 Ω minimum.

(1) Refer to the application report *Class-D Filter Design* (SLOA119) for a detailed description on the filter design.

8.2.2.2 Detailed Design Procedure

Refer to the Detailed Design Procedure section.

8.2.2.3 Application Performance Plots

CURVE TITLE	FIGURE
Output Power Vs Supply Voltage Mono PBTL Mode	図 33
Total Harmonic Distortion + Noise Vs Output Power Mono PBTL Mode	図 34
Total Harmonic Distortion + Noise Vs Frequency Mono PBTL Mode	図 37
Power Efficiency Vs Output Power Mono PBTL Mode	図 40

9 Power Supply Recommendations

To facilitate system design, the TAS5751M device requires only a 3.3-V supply in addition to the PVDD power-stage supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

To provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BSTRP_x), and power-stage supply pins (PVDD). The gate-drive voltage (GVDD_REG) is derived from the PVDD voltage. Place all decoupling capacitors as close to their associated pins as possible. In addition, avoid inductance between the power-supply pins and the decoupling capacitors.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BSTRP_x) to the power-stage output pin (AMP_OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD_REG) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. The capacitors shown in *Typical Applications* ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power-stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD). For optimal electrical performance, EMI compliance, and system reliability, each PVDD pin should be decoupled with a 100-nF, X7R ceramic capacitor placed as close as possible to each supply pin.

The TAS5751M device is fully protected against erroneous power-stage turn-on due to parasitic gate charging.

10 Layout

10.1 Layout Guidelines

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout. Ideally, the guidance provided in the *Application Information* section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in 図 70. The examples represent exemplary baseline balance of the engineering trade-offs involved with laying out the device. The designs can be modified slightly as needed to meet the needs of a given application. For example, in some applications, solution size can be compromised to improve thermal performance through the use of additional contiguous copper near the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components.

10.1.1 Decoupling Capacitors

Placing the bypassing and decoupling capacitors close to supply has been long understood in the industry. The placement of the capacitors applies to AVDD and PVDD. However, the capacitors on the PVDD net for the TAS5751M device deserve special attention. The small bypass capacitors on the PVDD lines of the DUT must be placed as close the PVDD pins as possible. Not only does placing these devices far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5751M device may cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the Absolute Maximum Ratings table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Example* section.

10.1.2 Thermal Performance and Grounding

Follow the layout examples shown in the *Layout Example* section of this document to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance may be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat-producing components or structures near the amplifier (including above or below in the end equipment).
- Use a higher layer count PCB if possible to provide more heat sinking capability for the TAS5751M device and to prevent traces of copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5751M device away from the edge of the PCB when possible to ensure that heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5751M device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5751M device. Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

10.2 Layout Example

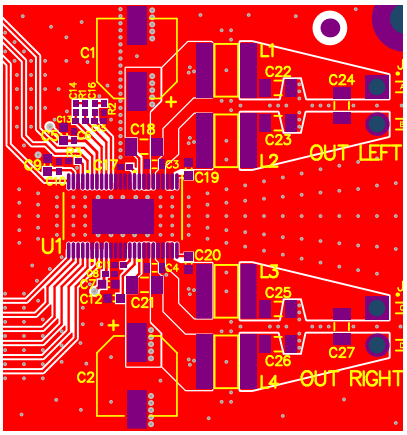


図 70. Layout Example (Stereo) - Top View Composite

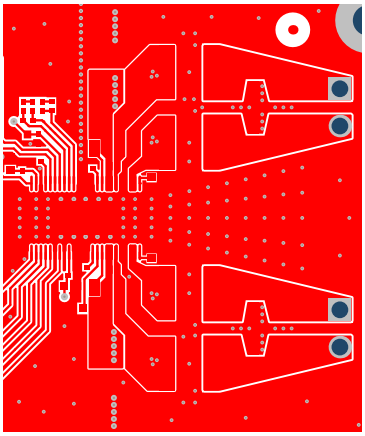


図 71. Layout Example (Stereo) - Top Layer

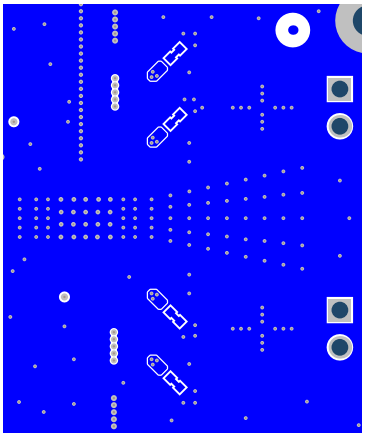


図 72. Layout Example (Stereo) - Bottom Layer

Layout Example (continued)

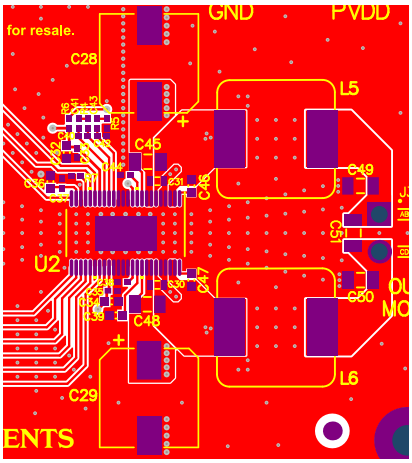


図 73. Layout Example (Mono) - Top View Composite

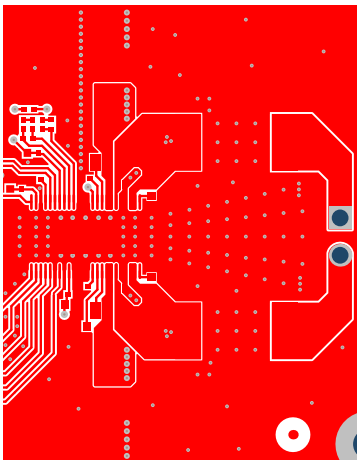


図 74. Layout Example (Mono) - Top Layer

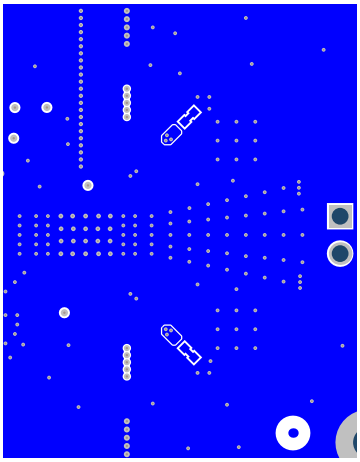


図 75. Layout Example (Mono) - Bottom Layer

11 デバイスおよびドキュメントのサポート

11.1 商標

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5751MDCA	ACTIVE	HTSSOP	DCA	48	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5751M	Samples
TAS5751MDCAR	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5751M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

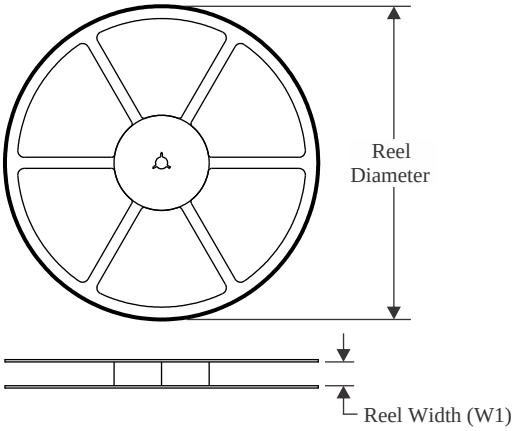
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

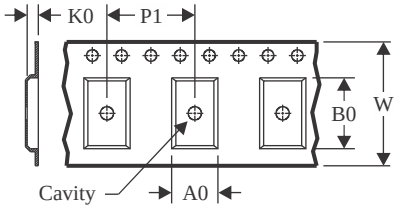
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

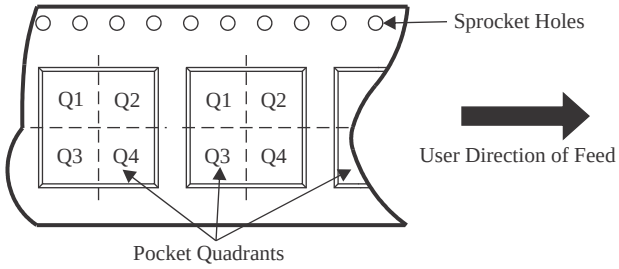


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

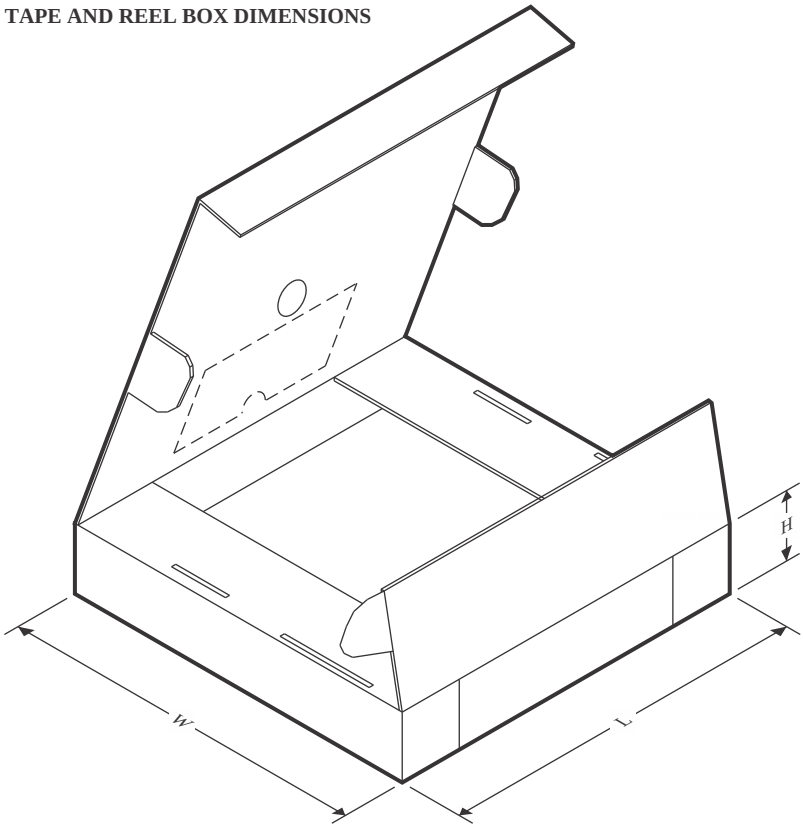
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5751MDCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

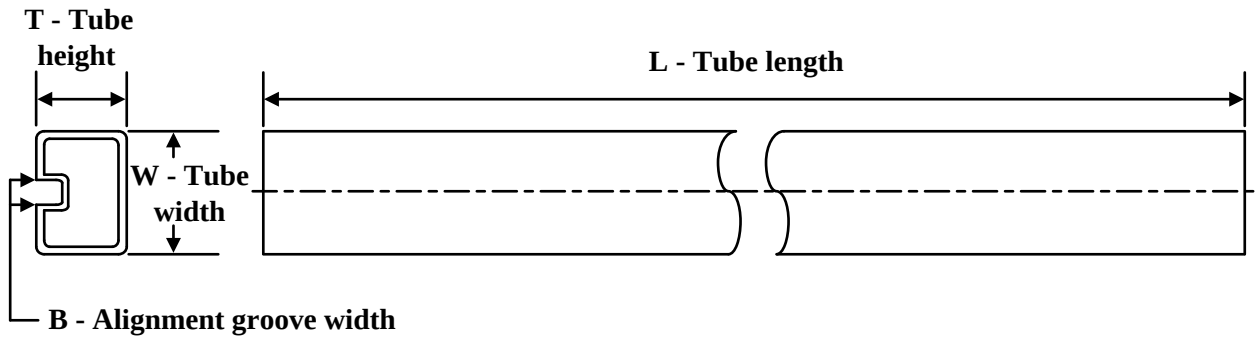
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5751MDCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5751MDCA	DCA	HTSSOP	48	40	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

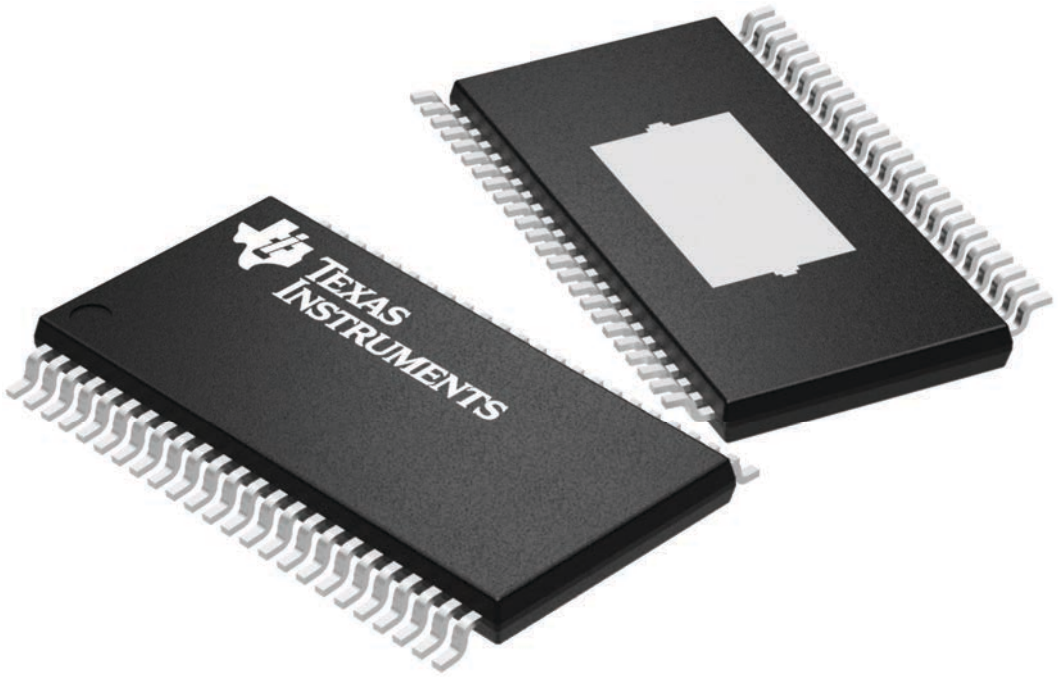
DCA 48

HTSSOP - 1.2 mm max height

12.5 x 6.1, 0.5 mm pitch

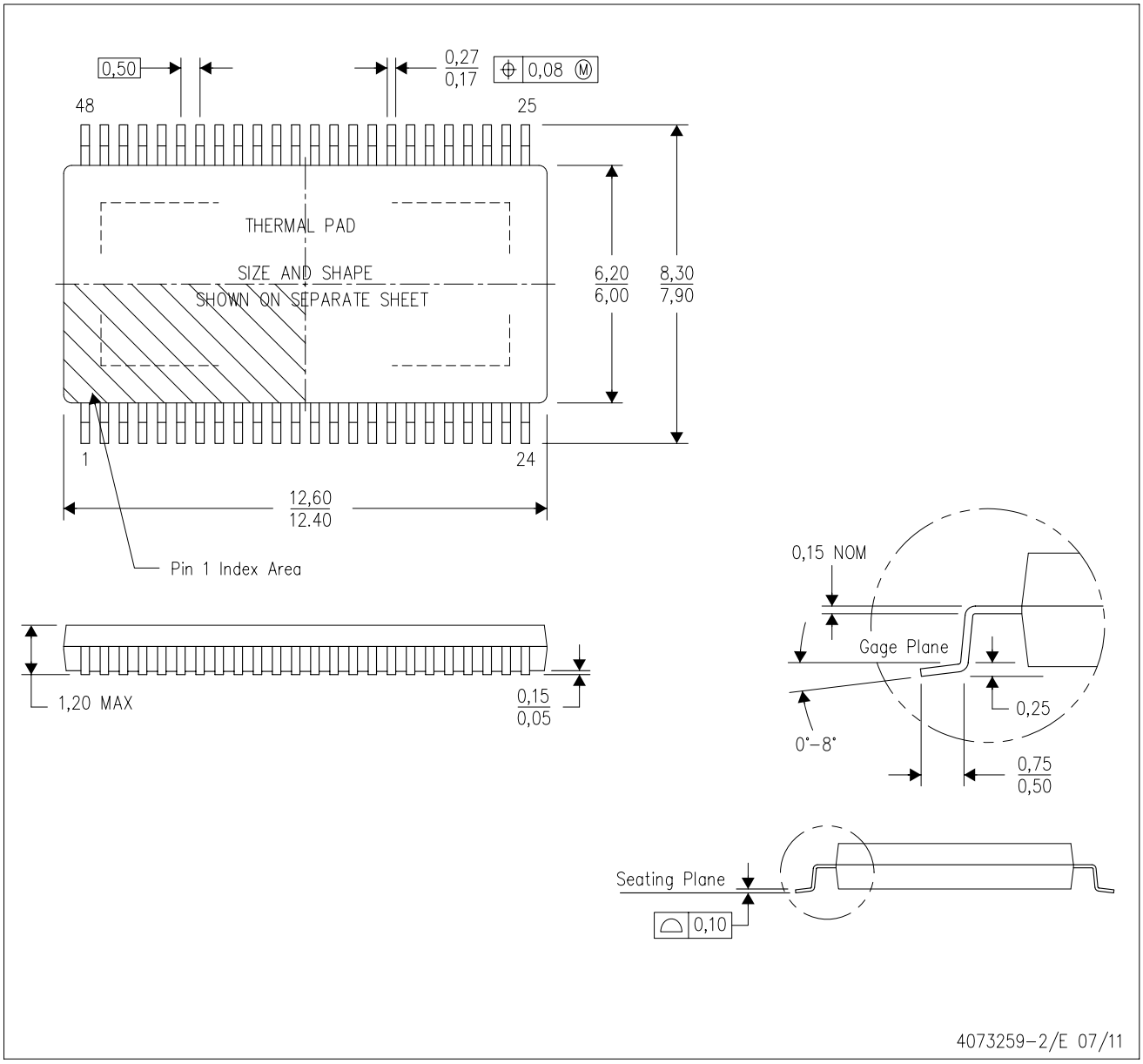
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224608/A

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

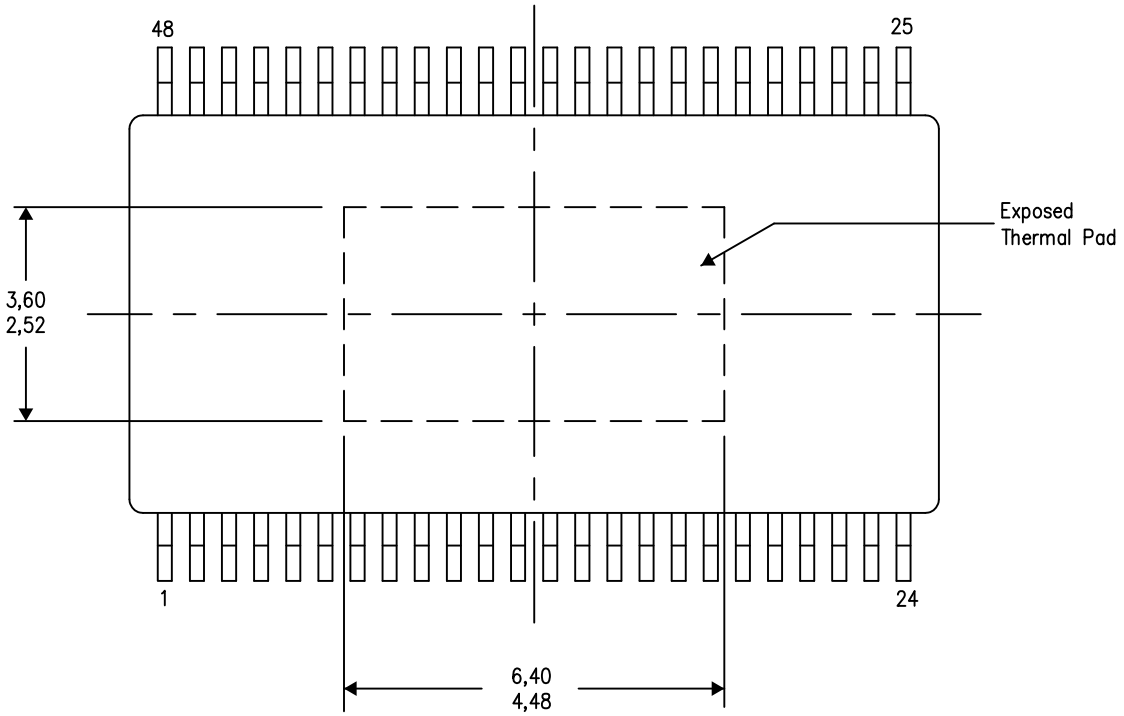
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

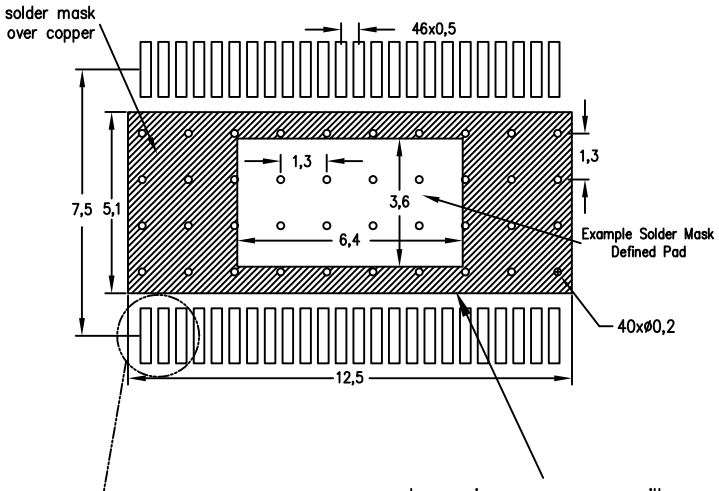
4206320–4/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

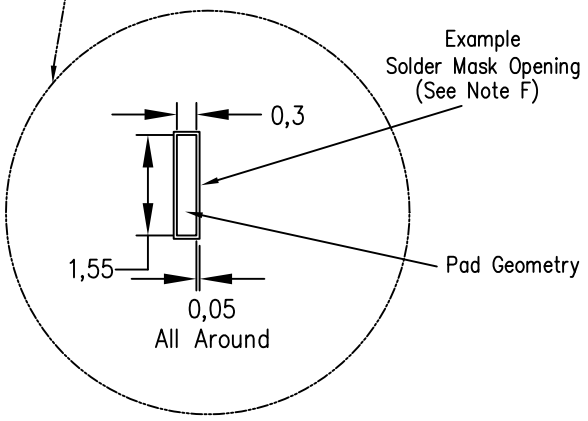
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

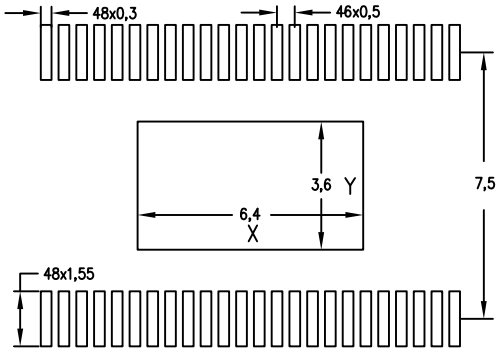


Increasing copper area will
enhance thermal performance
(See Note D)

Example
Non Soldermask Defined Pad



Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



(See Note E)

Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.21	4.06
0.127mm	6.40	3.60
0.152mm	5.85	3.29
0.178mm	5.41	3.04

4208546–3/H 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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