TAA5242 119dB のダイナミック レンジを備えたハードウェア制御の高性能ステレオ オーディオ ADC

1 特長

- ステレオ高性能オーディオ ADC
  - 性能:
    - ライン / マイクロフォン差動入力のダイナミック レンジ:119dB
    - 差動入力 THD+N:-98 dB
  - 入力電圧:
    - 差動、$2V_{RMS}$ フルスケール入力
    - シングルエンド、$1V_{RMS}$ フルスケール入力
  - サンプル レート (f_S) = 8kHz～192kHz
- 主な特長
  - ピンまたはハードウェア制御
  - オーディオ シリアル インターフェイス
    - フォーマット:TDM、I^2S、左揃え (LJ)
    - バス コントローラおよびターゲット モード
    - TDM モードのデイジーチェーン
    - ワード長:24 ビットまたは 32 ビットを選択可能
  - カットオフ周波数を選択可能なデジタル HPF:
    - 48kHz のサンプリング レートで 1Hz または 12Hz
  - ピンで選択可能なデジタル デシメーションフィルタ オプション:
    - リニア位相
    - 低レイテンシ
  - PLL およびマイクロフォン バイアスを内蔵
  - 自動クロック検出
  - 自動サンプル レート検出
  - クロック エラー時の割り込み出力
  - 単一電源動作 AVDD:1.8V または 3.3V
  - I/O 電源動作:1.8V または 3.3V
  - 温度グレード 1:-40°C ≤ T_A ≤ +125°C

2 アプリケーション

- テレビ会議システム
- IP ネットワーク カメラ
- IP 電話
- スマート スピーカ
- 業務用マイクとワイヤレス システム

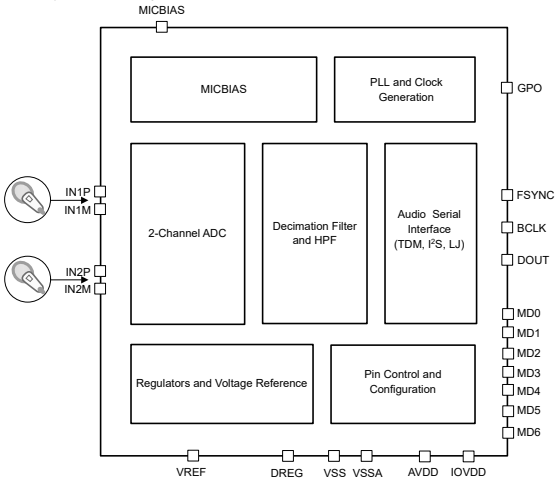
3 概要

TAA5242 は、$2V_{RMS}$ の差動入力と 119dB のダイナミック レンジを備えた高性能 ステレオ オーディオ ADC です。TAA5242 は、AC または DC 結合構成のオプションにより、差動とシングルエンドの両方のライン / マイクロフォン入力信号をサポートします。TAA5242 は、低ジッタの位相ロック ループ (PLL)、ピンでカットオフを選択できるデジタル ハイパス フィルタ (HPF) を内蔵しており、最高 192kHz のサンプル レートをサポートします。TAA5242 は、コントローラおよびターゲット モードで時分割多重化 (TDM)、I^2S、または左揃え (LJ) オーディオ フォーマットをサポートし、ピン / ハードウェア制御で制御されます。このように高性能な機能、ピン制御、そして単一電源動作であるため、TAA5242 はスペースに制約のあるオーディオ アプリケーションに最適な選択肢となっています。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ (公称) (2)
TAA5242	VQFN (24)	4mm × 4mm、0.5mm ピッチ

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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4 Pin Configuration and Functions

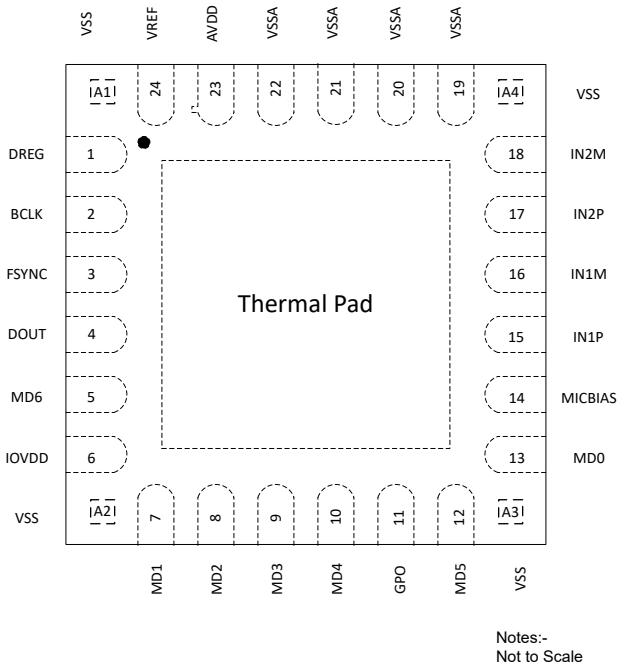


図 4-1. 24-Pin QFN Package with Exposed Thermal Pad and Corner Pins, Top View

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VSS	A1	Ground	Ground Pin. Short directly to board ground plane.
DREG	1	Digital Supply	Digital on-chip regulator output voltage for digital supply (1.55V, nominal)
BCLK	2	Digital I/O	Audio serial data interface bus bit clock
FSYNC	3	Digital I/O	Audio serial data interface bus frame synchronization signal
DOUT	4	Digital Output	Audio serial data interface bus output
MD6	5	Digital Input	TDM Mode: Daisy chain input
			I2S/LJ Mode: Mono/Stereo ADC channels selection
IOVDD	6	Digital Supply	Digital I/O power supply (1.8V or 3.3V, nominal)
VSS	A2	Ground	Ground pin. Short directly to board ground plane.
MD1	7	Digital Input	Controller Mode: Frame rate and BCLK frequency selection
			Target Mode: AVDD supply, word length, and decimation filter type selection
MD2	8	Digital Input	Controller Mode: Frame rate and BCLK frequency selection
			Target Mode: AVDD supply, word length, and decimation filter type selection
MD3	9	Digital Input	Controller Mode: Controller clock input
			TDM Target Mode: Daisy chain enable/disable
			I2S/LJ Target Mode: Digital HPF cut-off frequency and input cap quick charge setting
MD4	10	Digital Input	ADC input configuration selection

表 4-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
GPO	11	Digital Output	Interrupt Output (latched)
MD5	12	Digital Input	ADC input configuration selection
VSS	A3	Ground	Ground pin. Short directly to board ground plane.
MD0	13	Analog Input	Multi-Level analog input for Controller/Target and I^2S/TDM/LJ selection
MICBIAS	14	Analog	MICBIAS Output
IN1P	15	Analog Input	Analog input 1P Pin
IN1M	16	Analog Input	Analog input 1M Pin
IN2P	17	Analog Input	Analog input 2P Pin
IN2M	18	Analog Input	Analog input 2M Pin
VSS	A4	Ground	Ground pin. Short directly to board ground plane.
VSSA	19	Ground	Short directly to board ground plane
VSSA	20	Ground	Short directly to board ground plane
VSSA	21	Ground	Short directly to board ground plane
VSSA	22	Ground	Short directly to board ground plane
AVDD	23	Analog Supply	Analog power supply (1.8V or 3.3V, nominal)
VREF	24	Analog	Analog reference voltage filter output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to VSS (thermal pad)	–0.3	3.9	V
Supply voltage	IOVDD to VSS (thermal pad)	–0.3	3.9	V
Ground voltage differences	VSSA to VSS (thermal pad)	–0.3	0.3	V
Analog input voltage	Analog input pins voltage to VSS (thermal pad)	–0.3	AVDD + 0.3	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Functional ambient, T_A	–55	125	°C
	Operating ambient, T_A	–40	125	
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER					
AVDD(1)	Analog supply voltage to VSS (thermal pad) - AVDD 3.3V operation	3.0	3.3	3.6	V
	Analog supply voltage to VSS (thermal pad) - AVDD 1.8V operation	1.65	1.8	1.95	
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8V operation	1.65	1.8	1.95	
INPUTS					
INxx	Analog input pins voltage to VSS (thermal pad)	0		AVDD	V
IO	Digital input pins (MD1 to MD6) voltage to VSS (thermal pad)	0		IOVDD	V
MD0	MD0 pin w.r.t VSS (thermal pad)	0		AVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
OTHERS					
CCLK	MD3 controller mode clock frequency (CCLK) - IOVDD 3.3V operation			36.864(2)	MHz
	MD3 controller mode clock frequency (CCLK) - IOVDD 1.8V operation			24.576(2)	
C_L	Digital output load capacitance		20	50	pF

(1) VSSA and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2V.
(2) CCLK input rise time (V_{IL} to V_{IH}) and fall time (V_{IH} to V_{IL}) must be less than 5ns. For better audio noise performance, CCLK input must be used with low jitter.

5.4 Thermal Information

THERMAL METRIC(1)		TAA5242 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear phase decimation filter; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC PERFORMANCE FOR INPUT RECORDING						
	Differential input full-scale AC signal voltage	AC-coupled input		2		V_{RMS}
	Single-ended input full-scale AC signal voltage	AC-coupled input		1		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	INx differential AC-coupled input and AC signal shorted to ground		119		dB
SNR	Signal-to-noise ratio, A-weighted(1) (2)	INx differential DC-coupled input and AC signal shorted to ground, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)		112		dB
SNR	Signal-to-noise ratio, A-weighted(1) (2)	INx differential AC-coupled input and AC signal shorted to ground, AVDD = 1.8V		113		dB
		INx differential DC-coupled input and AC signal shorted to ground, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01), AVDD = 1.8V		105		
DR	Dynamic range, A-weighted(2)	INx differential AC-coupled input and –60dBFS AC signal input		119		dB
		INx differential DC-coupled input and –60dBFS AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)		112		

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear phase decimation filter; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DR	Dynamic range, A-weighted(2)	INx differential AC-coupled input and –60dBFS AC signal input, AVDD = 1.8V		113		dB
		INx differential DC-coupled input and –60dBFS AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01), AVDD = 1.8V		105		
THD+N	Total harmonic distortion(2)	INx differential AC-coupled input and –1dBFS AC signal input		–98		dB
		INx differential DC-coupled input and –1dB full-scale AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)		–98		
ADC OTHER PARAMETERS						
	AC Input impedance	Input pins INxP or INxM		5		kΩ
	Output data sample rate		8		192	kHz
	Output data sample word length	Pin Selectable	24		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter, – 3dB point (Pin Selectable)	1		12	Hz
	Interchannel isolation	–1dBFS AC signal line-in differential input to non-measurement channel		–134		dB
	Interchannel gain mismatch	–6dBFS AC signal line-in differential input, 1kHz sinusoidal signal		±0.1		dB
	Interchannel phase mismatch	–6dBFS AC signal line-in differential input, 1kHz sinusoidal signal		±0.01		Degrees
PSRR	Power-supply rejection ratio	100mV_{PP}, 1kHz sinusoidal signal on AVDD, differential input		120		dB
MICROPHONE BIAS						
	MICBIAS noise	Bandwidth = 20Hz to 20kHz, A-weighted, 1µF capacitor between MICBIAS and VSS (thermal pad)		2		$µV_{RMS}$
	MICBIAS voltage	AVDD = 1.8V		1.375		V
		AVDD = 3.3V		2.75		
DIGITAL I/O						
V_{IL}	Low-level digital input logic voltage threshold	All digital pins, IOVDD 1.8V operation	–0.3		0.35 × IOVDD	V
		All digital pins, IOVDD 3.3V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins, IOVDD 1.8V operation	0.65 × IOVDD		IOVDD + 0.3	V
		All digital pins, IOVDD 3.3V operation	2		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins, I_{OL} = –2 mA, IOVDD 1.8V operation			0.45	V
		All digital pins, I_{OL} = –2 mA, IOVDD 3.3V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins, I_{OH} = 2 mA, IOVDD 1.8V operation	IOVDD – 0.45			V
		All digital pins, I_{OH} = 2 mA, IOVDD 3.3V operation	2.4			
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, Input = 0V	–5	0.1	5	µA

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear phase decimation filter; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, Input = IOVDD	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in sleep mode or low power mode	All external clocks stopped with MD3 pin grounded, AVDD = 3.3V		1.37		mA
I_{IOVDD}		All external clocks stopped with MD3 pin grounded, IOVDD = 3.3V		0.6		µA
I_{IOVDD}		All external clocks stopped with MD3 pin grounded, IOVDD = 1.8V		0.3		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 16kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3 V		9.3		mA
I_{IOVDD}		IOVDD = 3.3 V		0.05		
I_{IOVDD}		IOVDD = 1.8 V		0.02		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 48kHz, I^2S Target Mode, BCLK = 64 × f_S	AVDD = 3.3 V		12		mA
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		

(1) Ratio of output level with 1kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(2) All performance measurements done with a 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter can result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

5.6 Timing Requirements: TDM, I^2S or LJ Interface

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see for timing diagram where DIN refers to Daisy Chain Input when applicable

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period	IOVDD = 1.8V	80			ns
		IOVDD = 3.3V	40			
$t_{H(BCLK)}$	BCLK high pulse duration(1)	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{L(BCLK)}$	BCLK low pulse duration(1)	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{SU(FSYNC)}$	FSYNC setup time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{HLD(FSYNC)}$	FSYNC hold time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{SU(DIN)}$	DIN setup time	IOVDD = 1.8V	8			ns
		IOVDD = 3.3V	8			
$t_{HLD(DIN)}$	DIN hold time	IOVDD = 1.8V	16			ns
		IOVDD = 3.3V	8			
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time (IOVDD = 1.8V)			10	ns
		10% - 90% rise time (IOVDD = 3.3V)			10	

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see for timing diagram where DIN refers to Daisy Chain Input when applicable

			MIN	NOM	MAX	UNIT
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time (IOVDD = 1.8V)			10	ns
		90% - 10% fall time (IOVDD = 3.3V)			10	

(1) To meet the timing specifications, the BCLK minimum high or low pulse duration must be higher than 25ns, if the DOUT data line is latched on the opposite BCLK edge polarity from the one used by the device to transmit the DOUT data at IOVDD = 3.3V.

5.7 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see Figure 5-1 for timing diagram where DIN refers to Daisy Chain Input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(DOUT-BCLK)}$	BCLK to DOUT delay	50% of BCLK to 50% of DOUT, IOVDD = 1.8V			26	ns
		50% of BCLK to 50% of DOUT, IOVDD = 3.3V			19	
$t_{d(DOUT-FSYNC)}$	FSYNC to DOUT delay in TDM or LJ mode	50% of FSYNC to 50% of DOUT, IOVDD = 1.8V			26	ns
		50% of FSYNC to 50% of DOUT, IOVDD = 3.3V			19	
$f_{(BCLK)}$	BCLK output clock frequency; controller mode(1)	IOVDD = 1.8V			12.288	MHz
		IOVDD = 3.3V			24.576	
$t_{d(FSYNC)}$	BCLK to FSYNC delay; controller mode	50% of BCLK to 50% of FSYNC, IOVDD = 1.8V			26	ns
		50% of BCLK to 50% of FSYNC, IOVDD = 3.3V			19	
$t_{H(BCLK)}$	BCLK high pulse duration; controller mode	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{L(BCLK)}$	BCLK low pulse duration; controller mode	IOVDD = 1.8V	36			ns
		IOVDD = 3.3V	18			
$t_{r(BCLK)}$	BCLK rise time; controller mode	10% - 90% rise time, IOVDD = 1.8V			10	ns
		10% - 90% rise time, IOVDD = 3.3V			10	
$t_{f(BCLK)}$	BCLK fall time; controller mode	90% - 10% fall time, IOVDD = 1.8V			10	ns
		90% - 10% fall time, IOVDD = 3.3V			10	

(1) To meet the timing specifications, the BCLK output clock frequency must be lower than 18.5MHz, if the DOUT data line is latched on the opposite BCLK edge polarity from the one used by the device to transmit DOUT data at IOVDD = 3.3V.

5.8 Timing Diagrams

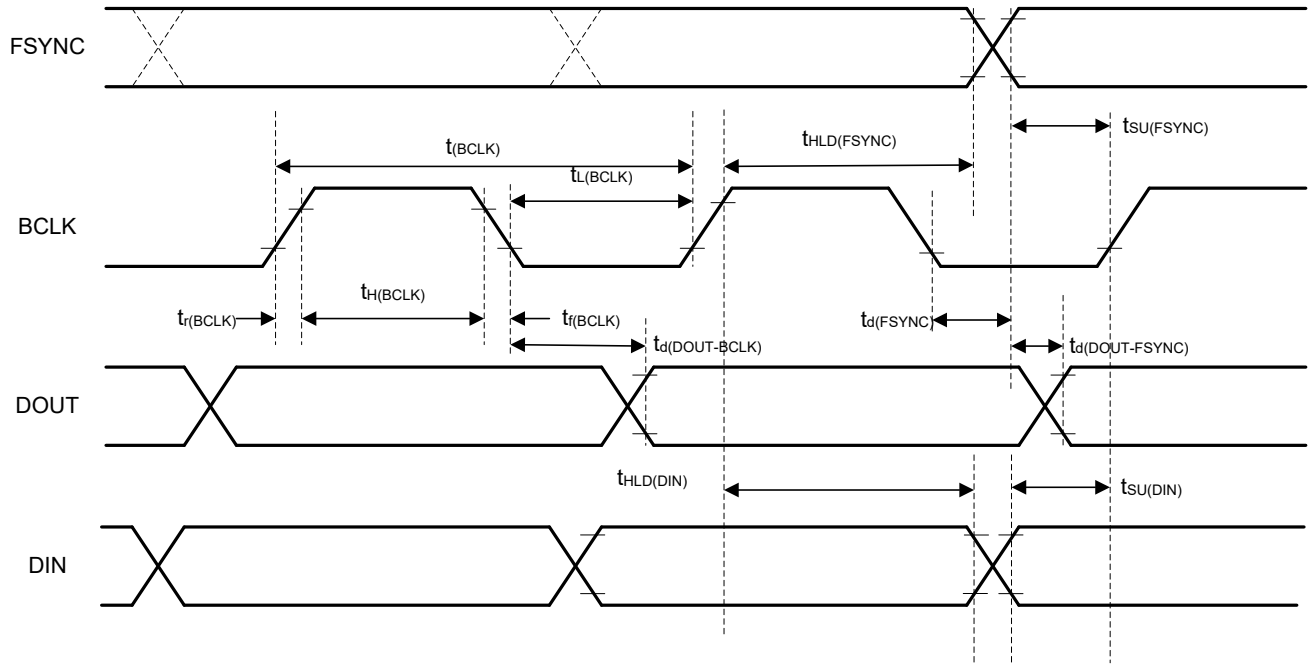
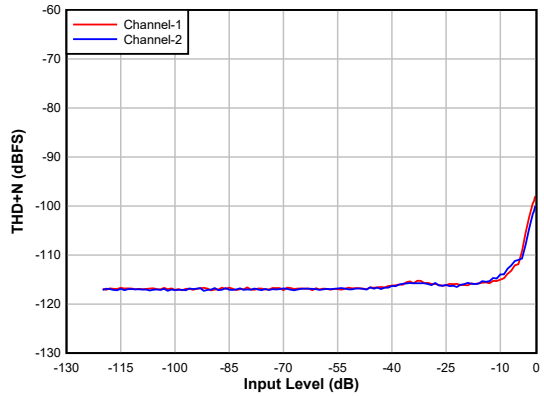


図 5-1. TDM, I²S, and LJ Interface Timing Diagram

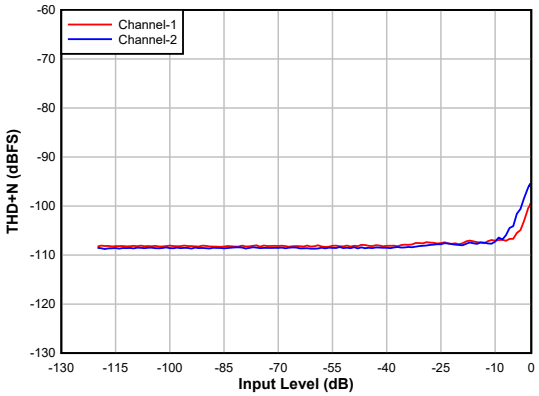
5.9 Typical Characteristics

at T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode, linear phase decimation filter; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted banwidth, unless otherwise noted



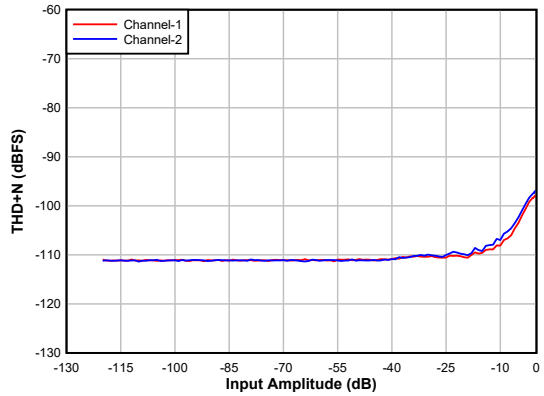
AC-coupled differential line input

図 5-2. ADC THD+N Level vs Input



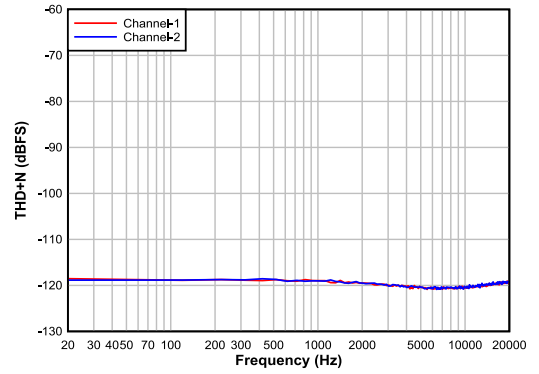
AC-coupled single-ended line input

図 5-3. ADC THD+N Level vs Input



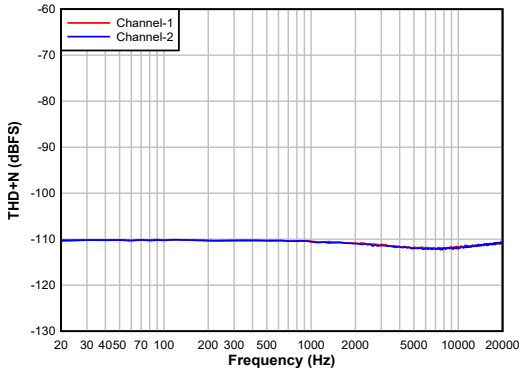
AC-coupled differential line input, AVDD=1.8V

図 5-4. ADC THD+N Level vs Input



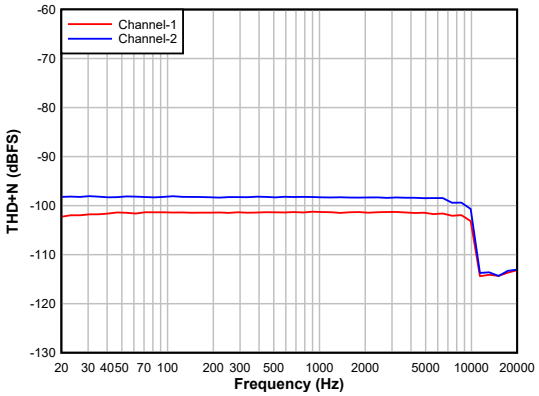
AC-coupled differential line input (-60dBFS)

図 5-5. ADC A-weighted DR vs Frequency



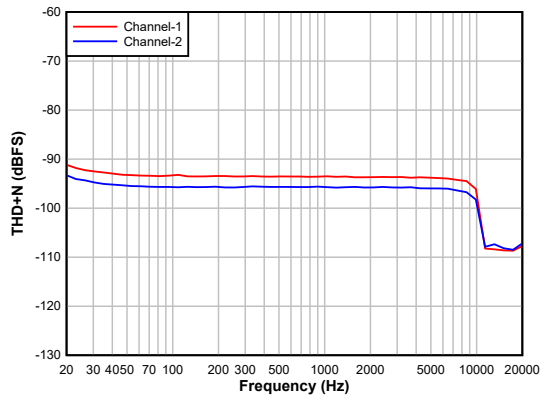
AC-coupled single-ended line input (-60dBFS)

図 5-6. ADC A-weighted DR vs Frequency



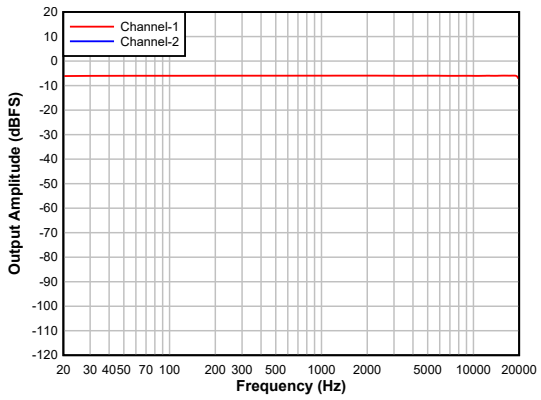
AC-coupled differential line input (-1dBFS)

図 5-7. ADC THD+N vs Frequency



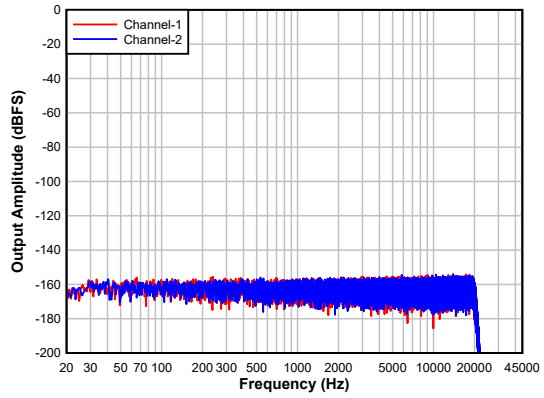
AC-coupled single-ended line input (-1dBFS)

図 5-8. ADC THD+N vs Frequency



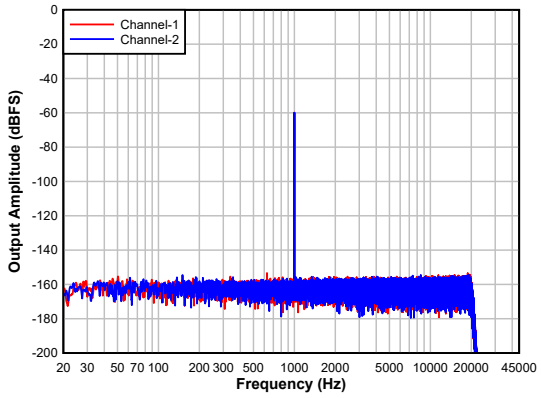
AC-coupled differential line input (-6dBFS)

図 5-9. ADC Frequency Response



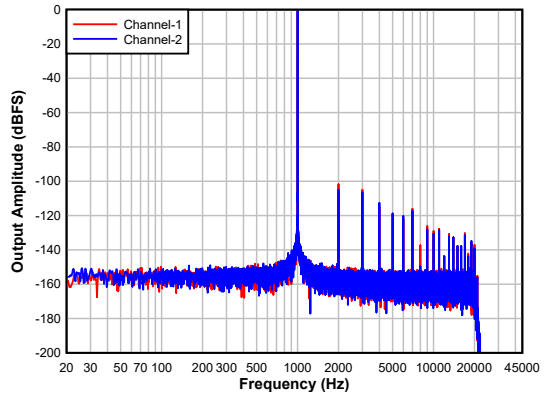
AC-coupled differential line input

図 5-10. ADC FFT with Idle Channel Input



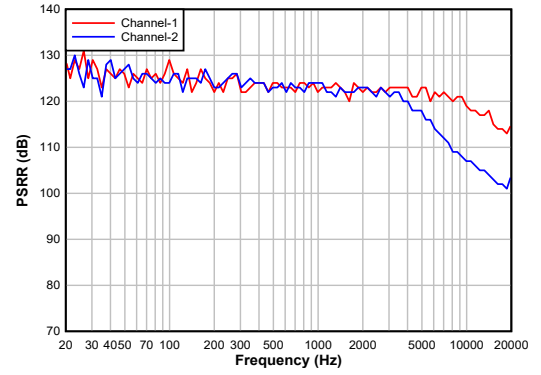
AC-coupled differential line input

図 5-11. ADC FFT with -60dBFS Input



AC-coupled differential line input

図 5-12. ADC FFT with -1dBFS Input



AC-coupled differential line input

図 5-13. ADC PSRR vs Frequency

6 Detailed Description

6.1 Overview

The TAA5242 is a high-performance, low-power, stereo, audio analog-to-digital converter (ADC). This device is intended for broad market applications such as ruggedized communication equipment, IP network camera, professional audio and multimedia applications. The high dynamic range of this device enables far-field audio recording with high fidelity. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained system designs. Package, performance, and compatible configuration across extended family make this device well suited for scalable system designs.

The TAA5242 consists of the following blocks:

- 2-channel, multibit, high-performance delta-sigma (ΔΣ) ADCs
- Pin or Hardware controlled device configurations
- Configurable single-ended or differential audio inputs
- Low-noise microphone bias output
- Linear-phase or Low-latency digital decimation filters
- High-pass filter (HPF) with selectable cut-off frequency options
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

The device supports a flexible audio serial interface [time-division multiplexing (TDM), I^2S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

6.2 Functional Block Diagram

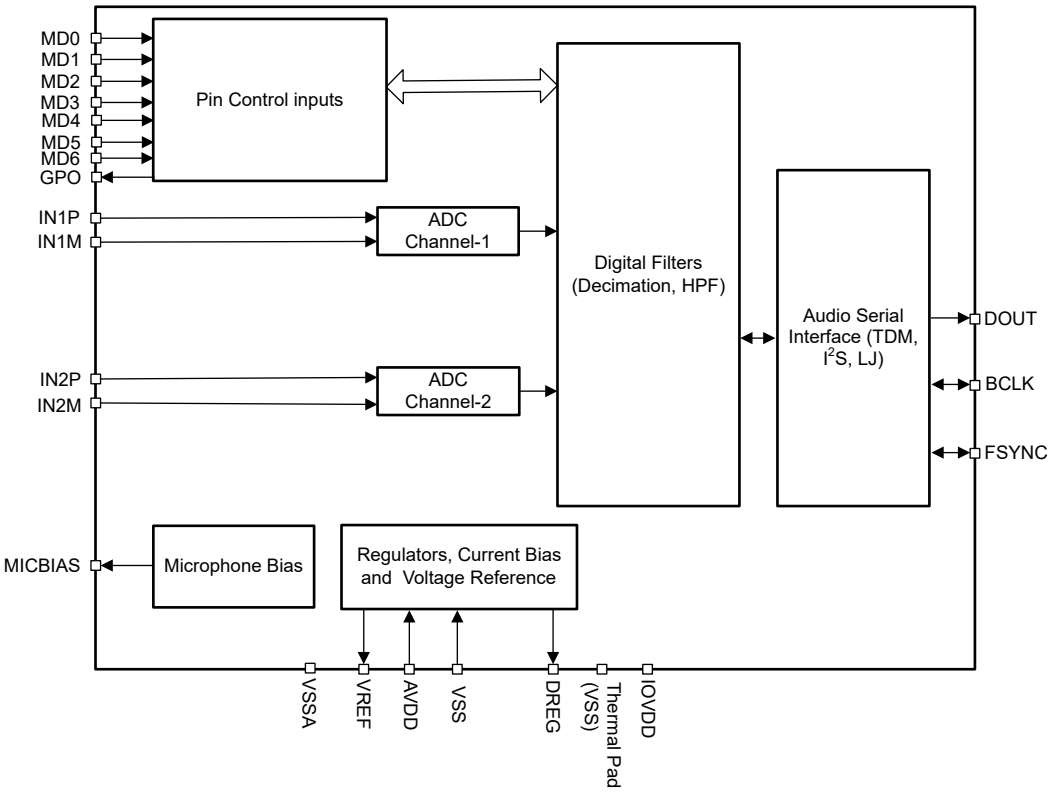


図 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Hardware Control

The device supports simple hardware-pin-controlled options to select a specific mode of operation and audio interface for a given system as summarized in 表 6-1. The MD1 to MD6 pins are connected to either logic low (VSS) or logic high (IOVDD), and the MD0 pin can be connected to AVDD or VSS through different pull-up or pull-down resistors.

表 6-1. Pin Selectable Configurations Summary

PIN	TARGET MODE	CONTROLLER MODE
MD0	Multi-level analog input for controller/target mode and I2S/TDM/LJ mode selection	
MD1	AVDD supply, word length, and decimation filter type selection	Frame rate and BCLK frequency selection
MD2		
MD3	I^2S/LJ Mode: HPF Cut-off and Input Cap Quick Charge Selection TDM Mode: Daisy Chain Enable/Disable	CCLK Input
MD4	ADC Input Configuration (Differential/Single-ended, AC/DC Coupled)	
MD5		
MD6	I^2S/LJ Mode: Mono/Stereo selection TDM Mode: Daisy chain input	

6.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAA5242 on the digital audio serial interface (ASI), or audio bus. This bus can be operated in target or controller mode through pin control. The ASI supports TDM mode for multichannel operation, I^2S and Left-Justified (LJ) bus protocols. The data is in MSB-first, two's-complement pulse code modulation (PCM) format, with pin-selectable word-length configuration.

The device supports an audio bus controller or target mode of operation using the hardware pin MD0. In target mode, FSYNC and BCLK work as input pins whereas in controller mode, FSYNC and BCLK work as output pins generated by the device. 表 6-2 shows the controller and target mode selection using the MD0 pin.

表 6-2. Controller and Target Mode Selection

MD0	CONTROLLER AND TARGET SELECTION
Short to Ground	Target I^2S Mode
Short to Ground with 4.7K Ohms	Target TDM Mode
Short to AVDD	Controller I^2S Mode
Short to AVDD with 4.7K Ohms	Controller TDM Mode
Short to AVDD with 22K Ohms	Target LJ Mode

The word length for audio serial interface (ASI) in TAA5242 can be selected through MD1 and MD2 Pins in target mode of operation. In controller mode, fixed word length of 32 bits is supported. The TAA5242 also supports 1.8V AVDD operation in target mode with 32-bit word length. 表 6-3 shows the configuration table for setting word length, AVDD supply voltage and decimation filter type applicable in Target Mode. In controller mode, AVDD supply mode is 3.3V, word length of 32-bits is supported, decimation filter is configured in the linear-phase and the MD1 and MD2 Pins control the system clock configuration described in 表 6-9.

表 6-3. Word Length, Supply Mode and Decimation Filter Selection

MD2	MD1	WORD LENGTH, SUPPLY MODE, AND INTERPOLATION FILTER SELECTION (Valid for Target Mode only)
Low	Low	AVDD = 3.3V, Word Length = 32, Linear-phase decimation filter
Low	High	AVDD = 1.8V, Word Length = 32, Linear-phase decimation filter

表 6-3. Word Length, Supply Mode and Decimation Filter Selection (続き)

MD2	MD1	WORD LENGTH, SUPPLY MODE, AND INTERPOLATION FILTER SELECTION (Valid for Target Mode only)
High	Low	AVDD = 3.3V, Word Length = 24, Linear-phase decimation filter
High	High	AVDD = 3.3V, Word Length = 32, Low-latency decimation filter

The TAA5242 also offers daisy chain configuration for target TDM mode of operation. This can be selected through MD3 pin when MD0 is configured in target TDM mode. In this mode, MD6 can be used as Daisy chain data input. 表 6-4 shows the daisy chain configuration in Target TDM mode of operation based on MD3 pin. When enabled, for a TDM with N slots, the device plays the audio present on the last 2 slots, and the remaining slots are shifted to the right and sent on the MD6 pin. An example for this is shown in 図 6-2.

表 6-4. Daisy Chain Selection for Target TDM Mode

MD3	DAISY CHAIN
Low	Disable
High	Enable

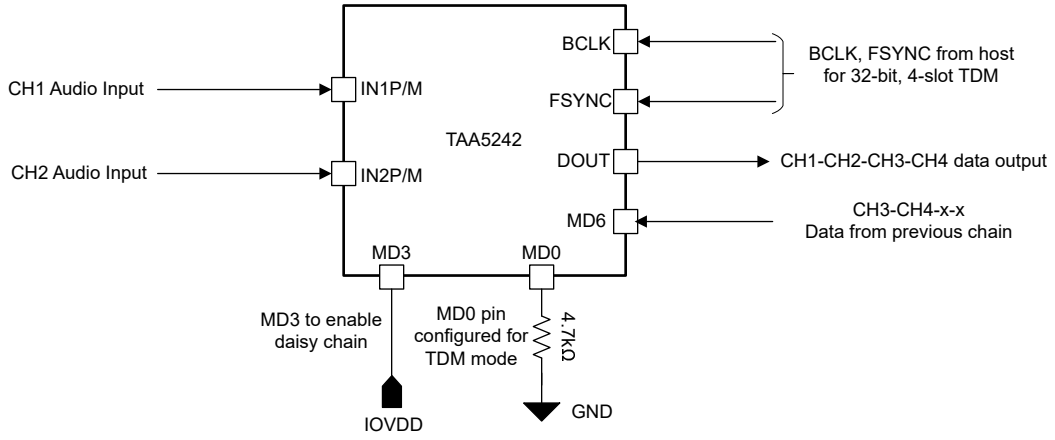


図 6-2. Daisy Chain in TDM Mode Block Diagram

The MD3 pin acts as the controller clock (CCLK) input when the device is configured in controller mode through MD0 pin to set the system clocks as described in セクション 6.3.3.

6.3.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit is transmitted on the rising edge of BCLK and received on the falling edge of the BCLK. 図 6-3 and 図 6-4 show the protocol timing for TDM operation with various configurations. DIN refers to the Daisy Chain Input.

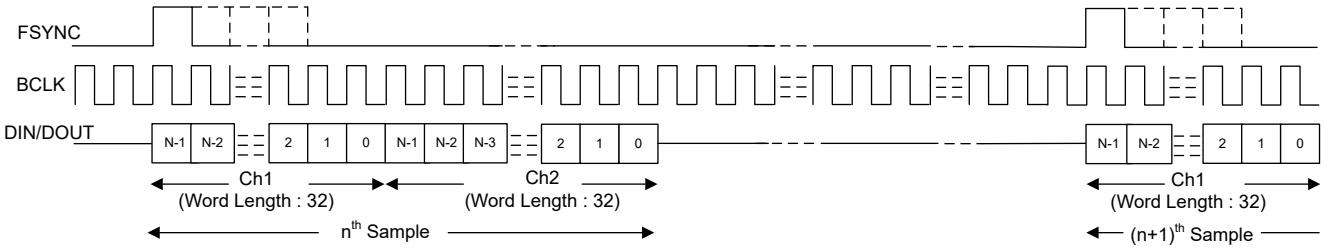


図 6-3. TDM Mode Protocol Timing (MD0 shorted to ground with 4.7K Ohms) In Target Mode

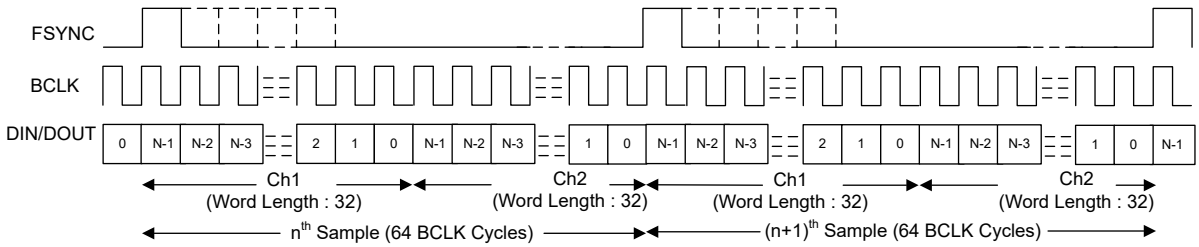


図 6-4. TDM Mode Protocol Timing (MD0 shorted to AVDD with 4.7K Ohms) In Controller Mode

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active input and output channels times the word length of the input and output channel data. The DOUT pin is in a Hi-Z state for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well.

6.3.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. In controller mode, FSYNC is transmitted on the falling edge of BCLK. 図 6-5 and 図 6-6 show the protocol timing for I^2S operation in target and controller mode of operation.

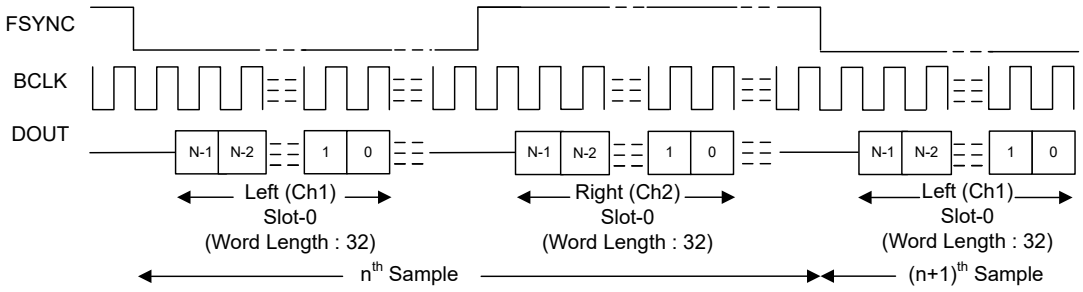


図 6-5. I^2S Mode Protocol Timing (MD0 shorted to ground) in Target Mode

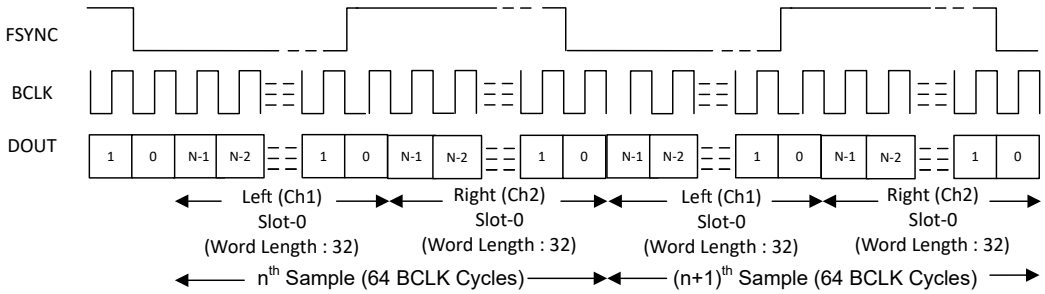


図 6-6. I^2S Protocol Timing (MD0 shorted to AVDD) In Controller Mode

For proper operation of the audio bus in I^2S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the word length of the output channel data.

6.3.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. The MSB of the right slot 0 is transmitted in

the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. 図 6-7 illustrates the protocol timing for LJ operation. in target mode.

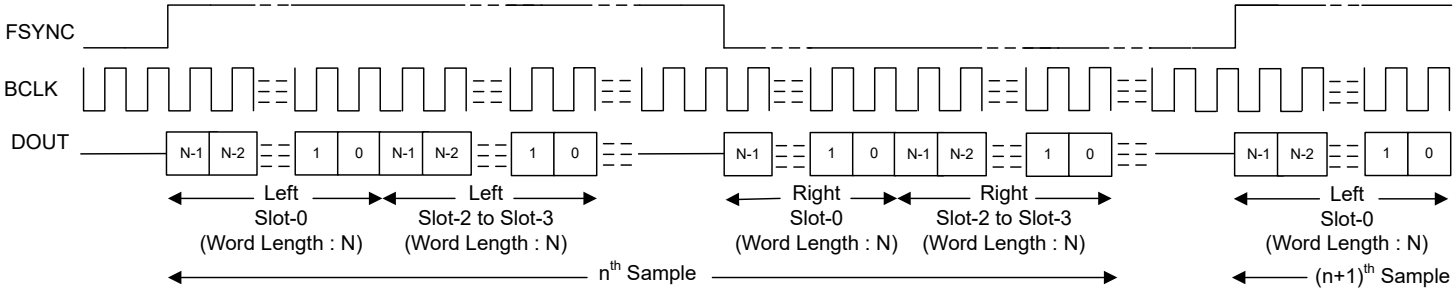


図 6-7. LJ Mode Standard Protocol Timing (MD0 shorted to AVDD with 22 kOhm) in Target Mode

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the word length of the output channel data.

6.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC modulators and digital filter engine, as well as other control blocks.

In target mode of operation, the device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. 表 6-5 to 表 6-8 list the supported FSYNC and BCLK frequencies depending on the IOVDD Supply.

表 6-5. Supported FSYNC (Multiples or Submultiples of 48kHz) and BCLK Frequencies (IOVDD - 3.3V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8kHz)	FSYNC (16kHz)	FSYNC (24kHz)	FSYNC (32kHz)	FSYNC (48kHz)	FSYNC (96kHz)	FSYNC (192kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**

表 6-6. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies (IOVDD - 3.3V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35kHz)	FSYNC (14.7kHz)	FSYNC (22.05kHz)	FSYNC (29.4kHz)	FSYNC (44.1kHz)	FSYNC (88.2kHz)	FSYNC (176.4kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**

表 6-7. Supported FSYNC (Multiples or Submultiples of 48kHz) and BCLK Frequencies (IOVDD - 1.8V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8kHz)	FSYNC (16kHz)	FSYNC (24kHz)	FSYNC (32kHz)	FSYNC (48kHz)	FSYNC (96kHz)	FSYNC (192kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	**Reserved**
128	1.024	2.048	3.072	4.096	6.144	12.288	**Reserved**
192	1.536	3.072	4.608	6.144	9.216	**Reserved**	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	**Reserved**	**Reserved**
384	3.072	6.144	9.216	12.288	**Reserved**	**Reserved**	**Reserved**
512	4.096	8.192	12.288	**Reserved**	**Reserved**	**Reserved**	**Reserved**

表 6-8. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies (IOVDD - 1.8V Operation)

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35kHz)	FSYNC (14.7kHz)	FSYNC (22.05kHz)	FSYNC (29.4kHz)	FSYNC (44.1kHz)	FSYNC (88.2kHz)	FSYNC (176.4kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	**Reserved**
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	**Reserved**
192	1.4112	2.8224	4.2336	5.6448	8.4672	**Reserved**	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	**Reserved**	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	**Reserved**	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	**Reserved**	**Reserved**	**Reserved**	**Reserved**

In the controller mode of operation, the device uses the MD3 pin, as the system clock, CCLK for the reference input clock source. In target mode of operation, the MD3 pin function described in 表 6-4and 表 6-3.

The device provides flexibility in FSYNC selection with a supported system clock frequency option of either 256 × f_S or 128 × f_S or a fixed 48/44.1kHz or 96/88.2kHz as configured using the MD1 and MD2 pins. 表 6-9 shows the FSYNC and BCLK selection for the controller mode using the MD1 and MD2 pins. In controller mode of operation, AVDD = 3.3V and Word-Length = 32 and linear-phase decimation filter is applicable.

表 6-9. System Clock Selection for the Controller Mode

MD2	MD1	SYSTEM CLOCK SELECTION (Valid for Controller Mode only)		
		FSYNC	BCLK TO FSYNC RATIO	
			I²S MODE	TDM MODE
Low	Low	CCLK/256	64	256 for FSYNC ≤ 48kHz, 128 for 48kHz < FSYNC ≤ 96kHz, and 64 for FSYNC > 96kHz
Low	High	CCLK/128		
High	Low	96/88.2 kHz		128
High	High	48/44.1 kHz		256

6.3.4 Analog Input Configurations

The device supports simultaneous recording of up to two channels using the high-performance stereo ADC. The device consists of two pairs of analog input pins (INxP and INxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for the analog pins can be from electret-condenser analog microphones, micro electrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board.

The voice or audio signal inputs can be capacitively coupled (AC-coupled) or DC-coupled to the device. For best distortion performance, use of low-voltage coefficient capacitors for AC-coupling is recommended. The typical input impedance for the TAA5242 is 5 kΩ for the INxP or INxM pins with ±20% variation. The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. To enable quick charging, the device has a quick charge scheme to speed up the charging of the coupling capacitor at power-up when operating in I²S/LJ target mode. This input cap quick charge setting can be enabled by configuring the MD3 pin. The MD3 pin also configures the digital HPF cut-off frequency when the device is operating in I²S/LJ target mode.

For optimal performance, the common-mode variation at the device input should be limited to less than 100mVpp for AC-coupled settings. For applications that cannot avoid large common-mode fluctuations, the device offers the modes to configure the device for higher common-mode tolerance. 表 6-11 shows the analog input configuration modes available with MD4 and MD5 configuration.

表 6-10. Input Cap Quick-Charge and HPF Selection in Target I²S/LJ Mode

MD3	INPUT CAP QUICK CHARGE	HPF CUT-OFF FREQUENCY
Low	Disabled	1Hz @ 48kHz sampling rate
High	Enabled	12Hz @ 48kHz sampling rate

表 6-11. Analog Input Configurations

MD5	MD4	ANALOG INPUT CONFIGURATION
Low	Low	Differential input; AC-Coupled only
Low	High	Differential input; AC or DC-Coupled with High Common Mode Tolerance
High	Low	Single-Ended input on INxP; AC-Coupled only
High	High	Single-Ended input on INxP; AC or DC-Coupled with High Common Mode Tolerance

図 6-8 to 図 6-11 show the typical configuration diagrams for the various input configuration modes.

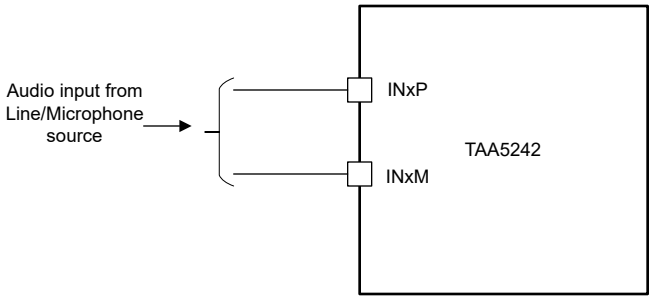


図 6-8. DC-Coupled Microphone or Line Differential Input Connection

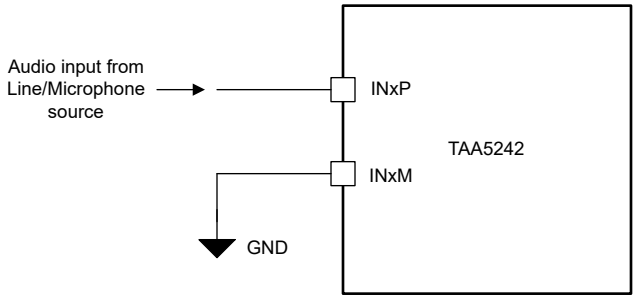


図 6-9. DC-Coupled Microphone or Line Single-Ended Input Connection

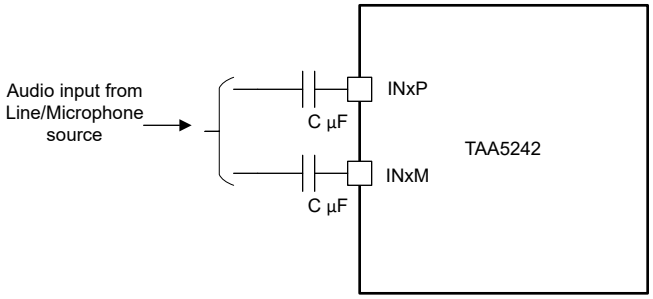


図 6-10. AC-Coupled Microphone or Line Differential Input Connection

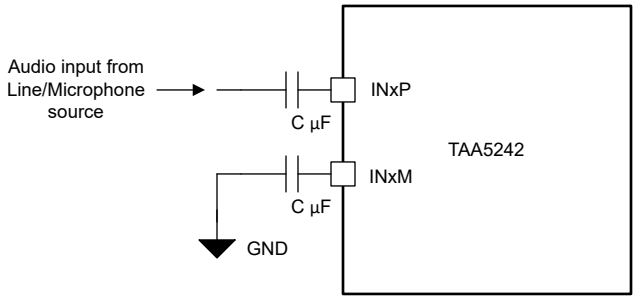


図 6-11. AC-Coupled Microphone or Line Single-Ended Input Connection

The device also supports channel select configurations to enable mono or stereo input in I^2S and LJ Modes. This can be configured by setting MD6 pin. 表 6-12 shows the control for this feature with MD6 configuration. ADC Channel-2 is disabled when MD6 pin is set to High. In TDM mode, MD6 pin function is as described in 図 6-2.

表 6-12. Input Channel Select configuration in I^2S and LJ Modes

MD6	ANALOG INPUT CONFIGURATION
Low	Stereo ADC

表 6-12. Input Channel Select configuration in I²S and LJ Modes (続き)

MD6	ANALOG INPUT CONFIGURATION
High	Mono 1-Channel ADC (IN1x enabled, IN2x disabled)

6.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The TAA5242 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1µF capacitor connected from the VREF pin to analog ground (VSS). The value of this reference voltage, VREF, is set to 2.75V, which in turn supports a $2V_{RMS}$ differential full-scale input to the device. The required minimum AVDD voltage for this VREF voltage is 3V. When the device is configured for 1.8V AVDD supply voltage, the voltage on the VREF pin is 1.375V, which in turn supports a $1V_{RMS}$ differential full-scale input to the device. Do not connect any external load to a VREF pin.

6.3.6 Integrated Microphone Bias

The device integrates a built-in, low-noise microphone bias pin that outputs a high PSRR, low noise output voltage equal to VREF that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphones. The integrated bias amplifier supports up to 5mA of load current that can be used for multiple microphones. When using this MICBIAS pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones.

6.3.7 Signal-Chain Processing

図 6-12 shows the key components of the record-path signal chain.

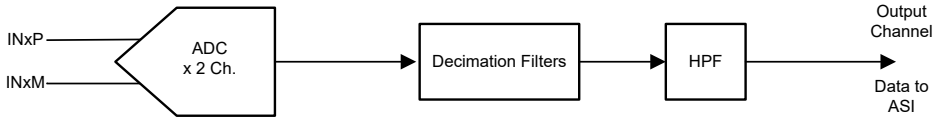


図 6-12. ADC Signal-Chain Processing Flowchart

The TAA5242 signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and flexible digital processing blocks. The high performance and flexibility combined with a compact package makes the TAA5242 optimized for a variety of end-equipments and applications that require multichannel audio capture. The ADC signal-chain integrates high-performance multi-stage digital decimation filter followed by a high-pass filter (HPF) with configurable cut-off frequency described further.

6.3.7.1 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. The decimation filters in the device can be selected to linear-phase or low-latency filters based on the state of the MD2 and MD1 pins according to 表 6-3. This makes them suitable for a wide variety of audio applications. Following section describes the filter response for different samples rates.

6.3.7.1.1 Linear-phase filters

The linear-phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

6.3.7.1.1.1 Sampling Rate: 8kHz or 7.35kHz

図 6-13 and 図 6-14 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 8kHz or 7.35kHz, 表 6-13 and lists its specifications.

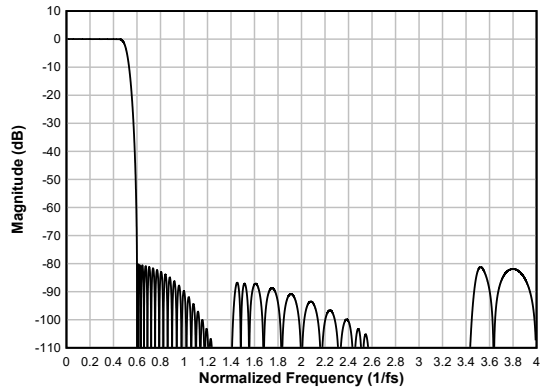


図 6-13. Linear-phase Decimation Filter Magnitude Response

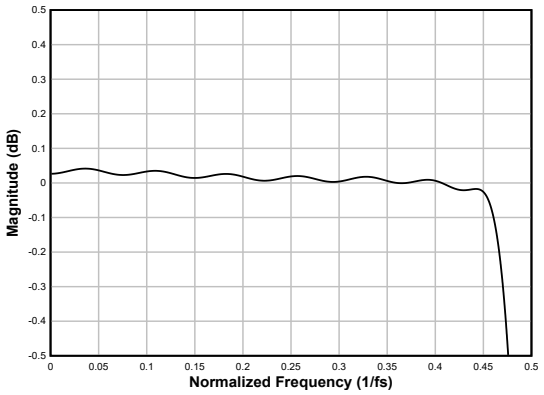


図 6-14. Linear-phase Decimation Filter Pass-Band Ripple

表 6-13. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.2			dB
	Frequency range is 4 × f_S onwards	84.7			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.1		1/f_S

6.3.7.1.1.2 Sampling Rate: 16kHz or 14.7kHz

図 6-15 and 図 6-16 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 16kHz or 14.7kHz, and 表 6-14 lists its specifications.

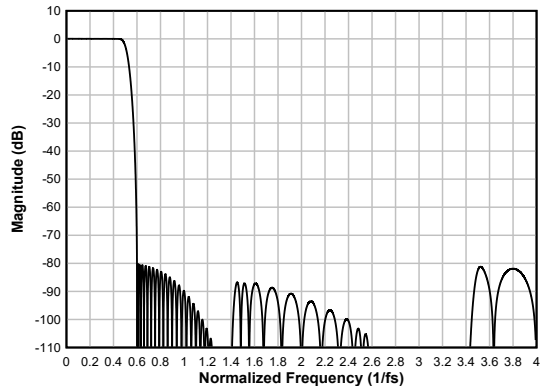


図 6-15. Linear-phase Decimation Filter Magnitude Response

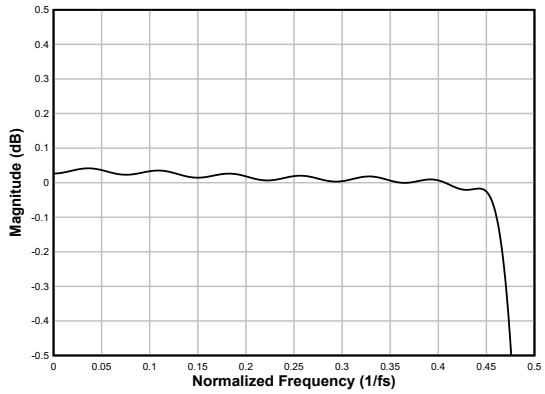


図 6-16. Linear-phase Decimation Filter Pass-Band Ripple

表 6-14. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.2			dB
	Frequency range is 4 × f_S onwards	84.7			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.1		1/f_S

6.3.7.1.1.3 Sampling Rate: 24kHz or 22.05kHz

図 6-17 and 図 6-18 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 24kHz or 22.05kHz, and 表 6-16 lists its specifications.

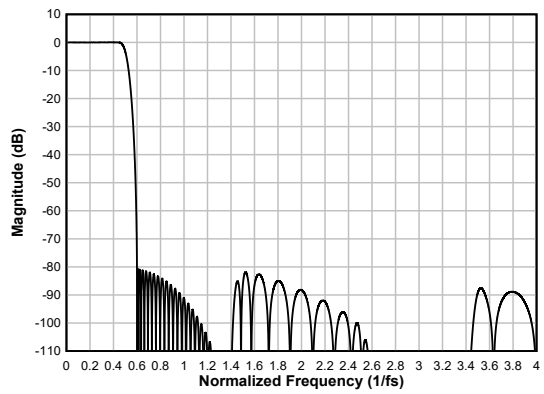


図 6-17. Linear-phase Decimation Filter Magnitude Response

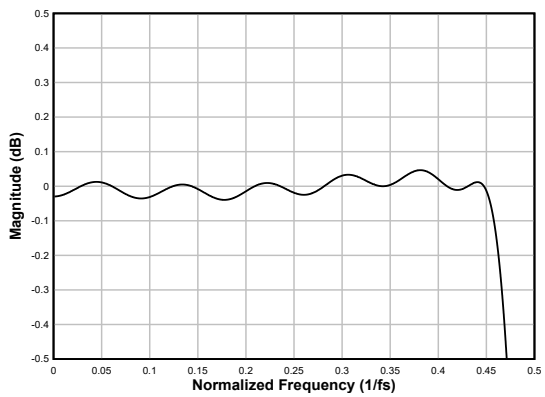


図 6-18. Linear-phase Decimation Filter Pass-Band Ripple

表 6-15. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.6			dB
	Frequency range is 4 × f_S onwards	93			

表 6-15. Linear-phase Decimation Filter Specifications (続き)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay or latency	Frequency range is 0 to 0.455 × f_S		14.7		$1/f_S$

6.3.7.1.1.4 Sampling Rate: 32kHz or 29.4kHz

図 6-20 and 図 6-21 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 32kHz or 29.4kHz, and 表 6-17 lists its specifications.

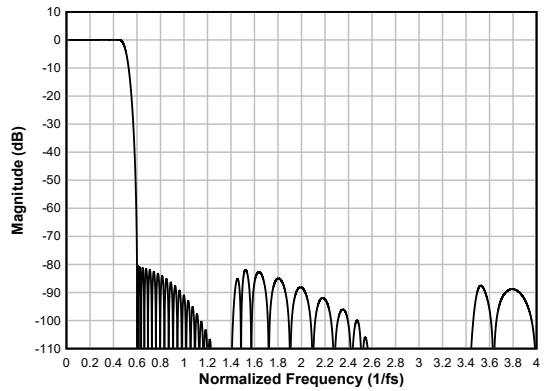


図 6-19. Linear-phase Decimation Filter Magnitude Response

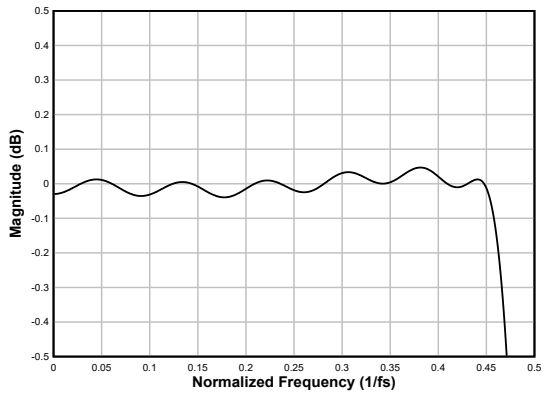


図 6-20. Linear-phase Decimation Filter Pass-Band Ripple

表 6-16. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.6			dB
	Frequency range is 4 × f_S onwards	92.9			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		14.7		$1/f_S$

6.3.7.1.1.5 Sampling Rate: 48kHz or 44.1kHz

図 6-21 and 図 6-22 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 48kHz or 44.1kHz, and 表 6-17 lists its specifications.

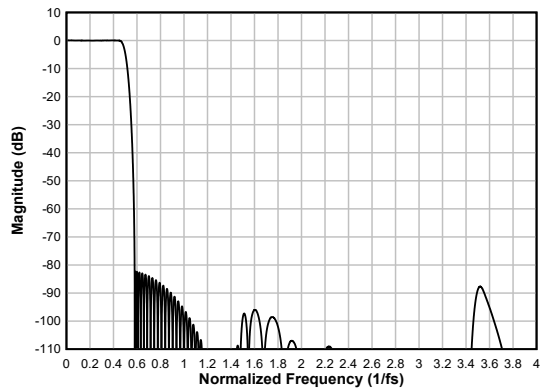


図 6-21. Linear-phase Decimation Filter Magnitude Response

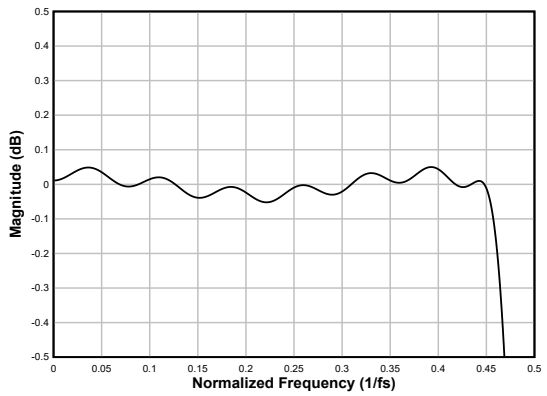


図 6-22. Linear-phase Decimation Filter Pass-Band Ripple

表 6-17. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82.2			dB
	Frequency range is 4 × f_S onwards	98			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17		1/f_S

6.3.7.1.1.6 Sampling Rate: 96kHz or 88.2kHz

図 6-23 and 図 6-24 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 96kHz or 88.2kHz, and 表 6-18 lists its specifications.

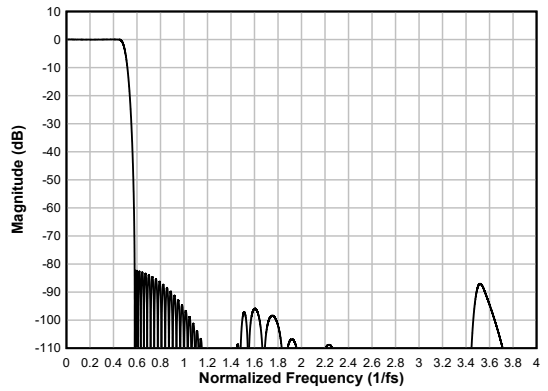


図 6-23. Linear-phase Decimation Filter Magnitude Response

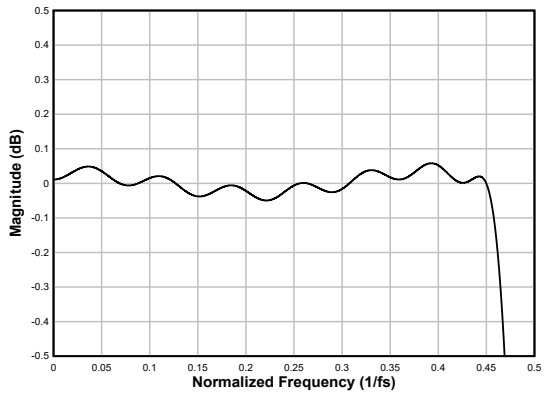


図 6-24. Linear-phase Decimation Filter Pass-Band Ripple

表 6-18. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.455 × f_S	–0.05		0.06	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82.2			dB
	Frequency range is 4 × f_S onwards	87			
Group delay or latency	Frequency range is 0 to 0.455 × f_S		16.9		1/f_S

6.3.7.1.1.7 Sampling Rate: 192kHz or 176.4kHz

図 6-25 and 図 6-26 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 192kHz or 176.4kHz, and 表 6-19 lists its specifications.

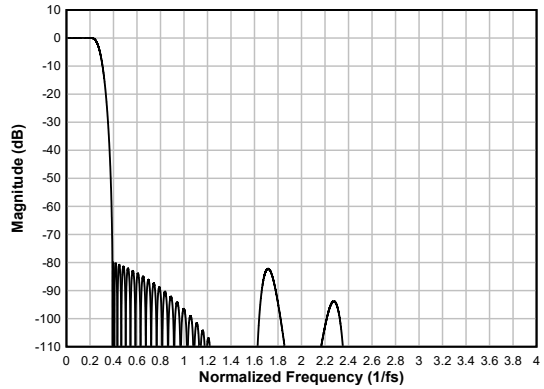


図 6-25. Linear-phase Decimation Filter Magnitude Response

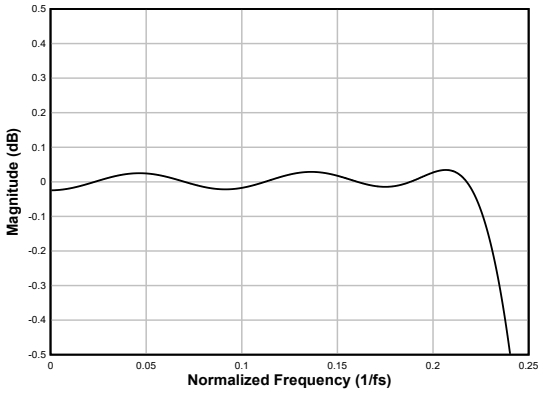


図 6-26. Linear-phase Decimation Filter Pass-Band Ripple

表 6-19. Linear-phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.223 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.391 × f_S to 4 × f_S	80			dB
	Frequency range is 4 × f_S onwards	82.2			
Group delay or latency	Frequency range is 0 to 0.258 × f_S		11.6		1/f_S

6.3.7.1.2 Low-latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the TAA5242 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.376 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

6.3.7.1.2.1 Sampling Rate: 24kHz or 22.05kHz

図 6-27 shows the magnitude response and 図 6-28 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 24kHz or 22.05kHz. 表 6-20 lists its specifications.

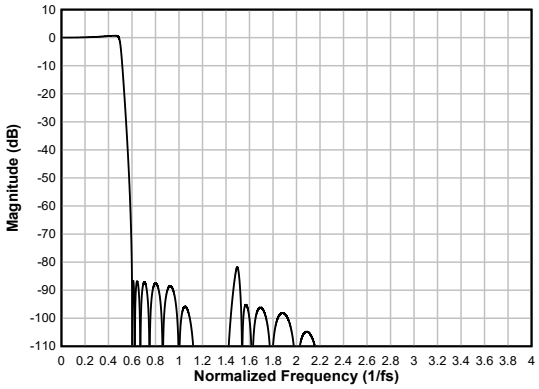


図 6-27. Low-latency Decimation Filter Magnitude Response

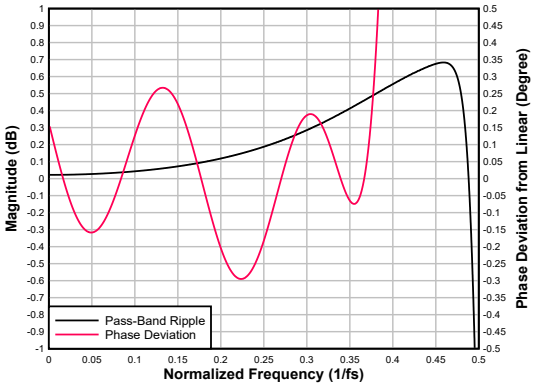


図 6-28. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-20. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.492 × f_S	–0.67		–0.67	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	81.8			dB
	Frequency range is 4 × f_S onwards	115			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.5		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.092		0.029	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.3		0.27	Degrees

6.3.7.1.2.2 Sampling Rate: 32kHz or 29.4kHz

図 6-29 shows the magnitude response and 図 6-30 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 32kHz or 29.4kHz. 表 6-21 lists its specifications.

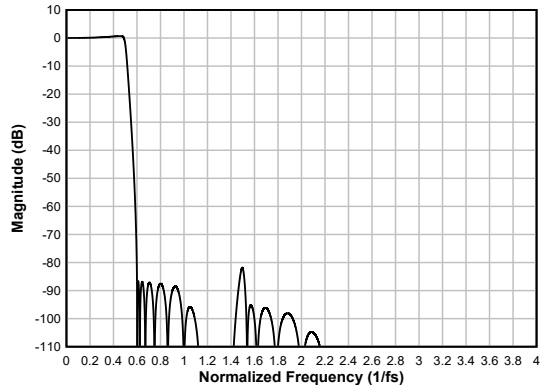


図 6-29. Low-latency Decimation Filter Magnitude Response

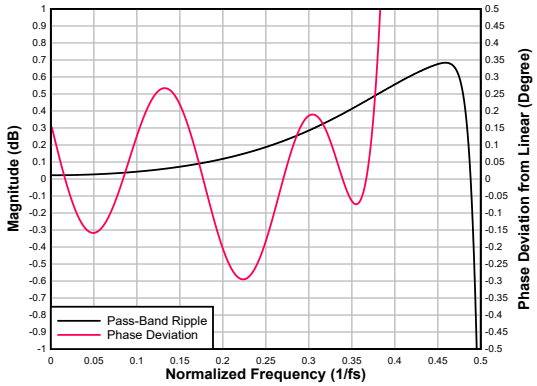


図 6-30. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-21. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.492 × f_S	–0.67		–0.67	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	81.8			dB
	Frequency range is 4 × f_S onwards	115			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.5		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.092		0.029	$1/f_S$
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.3		0.27	Degrees

6.3.7.1.2.3 Sampling Rate: 48kHz or 44.1kHz

図 6-31 shows the magnitude response and 図 6-32 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 48kHz or 44.1kHz. 表 6-22 lists its specifications.

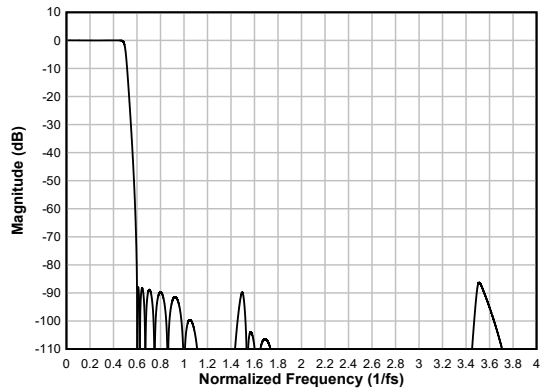


図 6-31. Low-latency Decimation Filter Magnitude Response

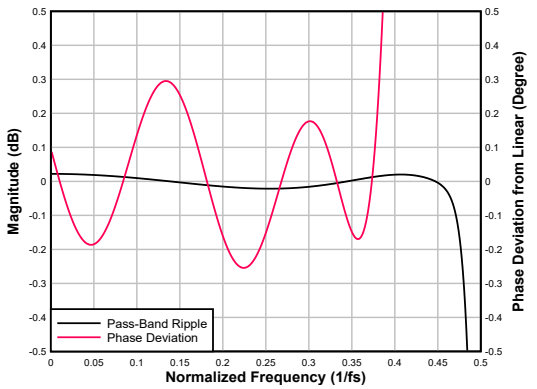


図 6-32. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-22. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.456 × f_S	–0.02		–0.02	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	86.3			dB
	Frequency range is 4 × f_S onwards	96.8			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.6		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.086		0.027	$1/f_S$

表 6-22. Low-latency Decimation Filter Specifications (続き)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.25		0.3	Degrees

6.3.7.1.2.4 Sampling Rate: 96kHz or 88.2kHz

図 6-33 shows the magnitude response and 図 6-34 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 96kHz or 88.2kHz. 表 6-23 lists its specifications.

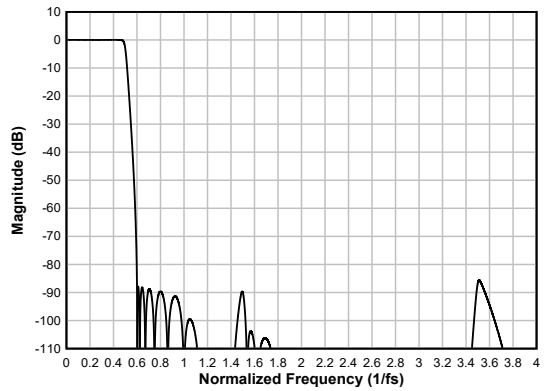


図 6-33. Low-latency Decimation Filter Magnitude Response

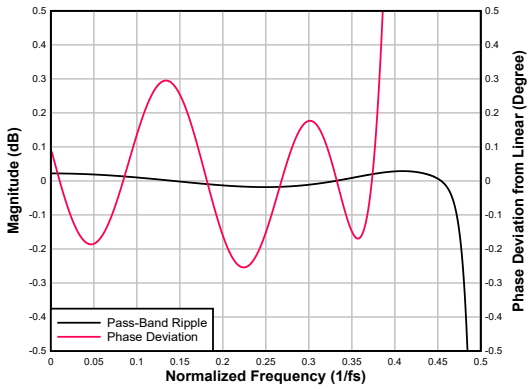


図 6-34. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-23. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.456 × f_S	–0.02		0.03	dB
Stop-band attenuation	Frequency range is 0.599 × f_S to 4 × f_S	85.6			dB
	Frequency range is 4 × f_S onwards	95.7			
Group delay or latency	Frequency range is 0 to 0.376 × f_S		6.6		1/f_S
Group delay deviation	Frequency range is 0 to 0.376 × f_S	-0.086		0.022	1/f_S
Phase deviation	Frequency range is 0 to 0.376 × f_S	-0.25		0.022	Degrees

6.3.7.1.2.5 Sampling Rate: 192kHz or 176.4kHz

図 6-35 shows the magnitude response and 図 6-36 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 192kHz or 176.4kHz. 表 6-24 lists its specifications.

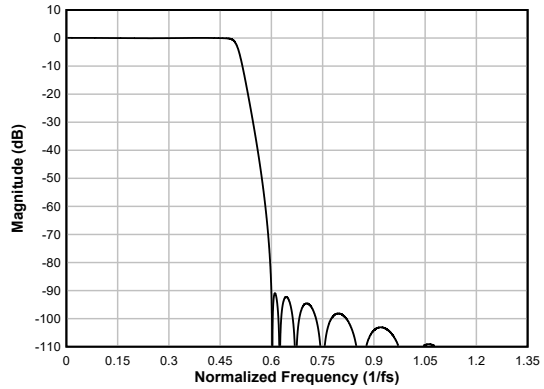


図 6-35. Low-latency Decimation Filter Magnitude Response

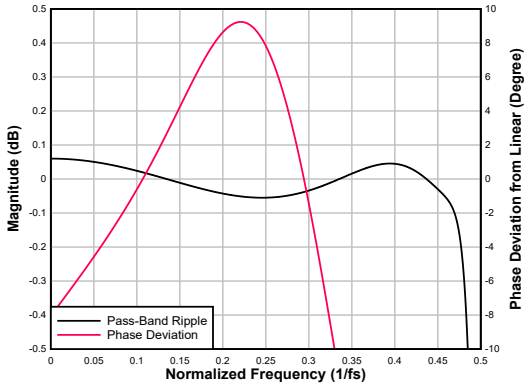


図 6-36. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation

表 6-24. Low-latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.456 × f_S	–0.06		0.06	dB
Stop-band attenuation	Frequency range is 0.571 × f_S to 1.35 × f_S	90.5			dB
	Frequency range is 1 × f_S onwards	86.9			
Group delay or latency	Frequency range is 0 to 0.327 × f_S		6.8		1/f_S
Group delay deviation	Frequency range is 0 to 0.327 × f_S	-0.296		0.829	1/f_S
Phase deviation	Frequency range is 0 to 0.327 × f_S	-9.24		9.24	Degrees

6.3.7.2 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a high-pass filter (HPF). This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. The default cut-off frequency for this HPF is set to 1Hz at 48kHz sampling frequency and in Target I^2S/LJ Mode, it is selectable between 1Hz and 12Hz at 48kHz sampling frequency as mentioned in 表 6-10. This is not a channel-independent filter setting but is globally applicable for all ADC channels. セクション 6.3.7.2 shows the frequency response for the HPF with the two settings.

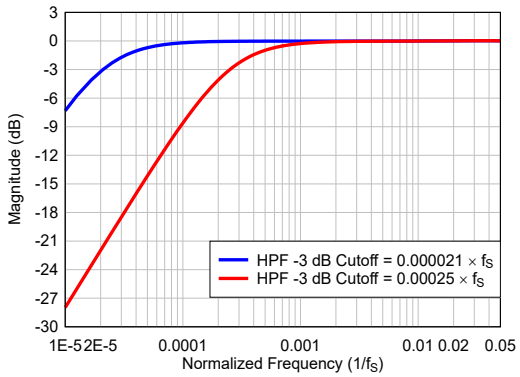


図 6-37. HPF Filter Frequency Response Plot

6.4 Device Functional Modes

6.4.1 Active Mode

The device wakes up in active mode when AVDD and IOVDD are available. MD0 pin sets the type of audio serial interface and should be configured along with the supplies. Further, configure all other hardware control mode pins (MD1, MD2, MD3, MD4,MD5 and MD6) for the desired mode of operation before enabling the clocks for the device.

In active mode, when the audio clocks are available, the device automatically powers up all ADC channels and starts transmitting and playing data over the audio serial interface as per the configurations. If the clocks are stopped, then the device auto powers down the ADC channels.

Stopping the clocks or clock-error triggers an interrupt on the GPO pin. This is a latched interrupt that can be cleared by power-cycling the device supplies.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TAA5242 is a pin or hardware controlled stereo, high-performance audio ADC that supports sample rates of up to 192 kHz. The device can be configured by controlling the Mode pins MD0 to MD6 and can support 1.8V or 3.3V AVDD analog power supply along with flexible digital audio interfaces of I²S/TDM/LJ. The device has differential and single-ended input capabilities and can support both line-in and microphone inputs for stereo recording with high dynamic range.

7.2 Typical Application

7.2.1 Application

図 7-1 shows a typical configuration of the TAA5242 for an application using 2-channel differential AC-coupled microphone operation with a Target Mode I²S audio serial data interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

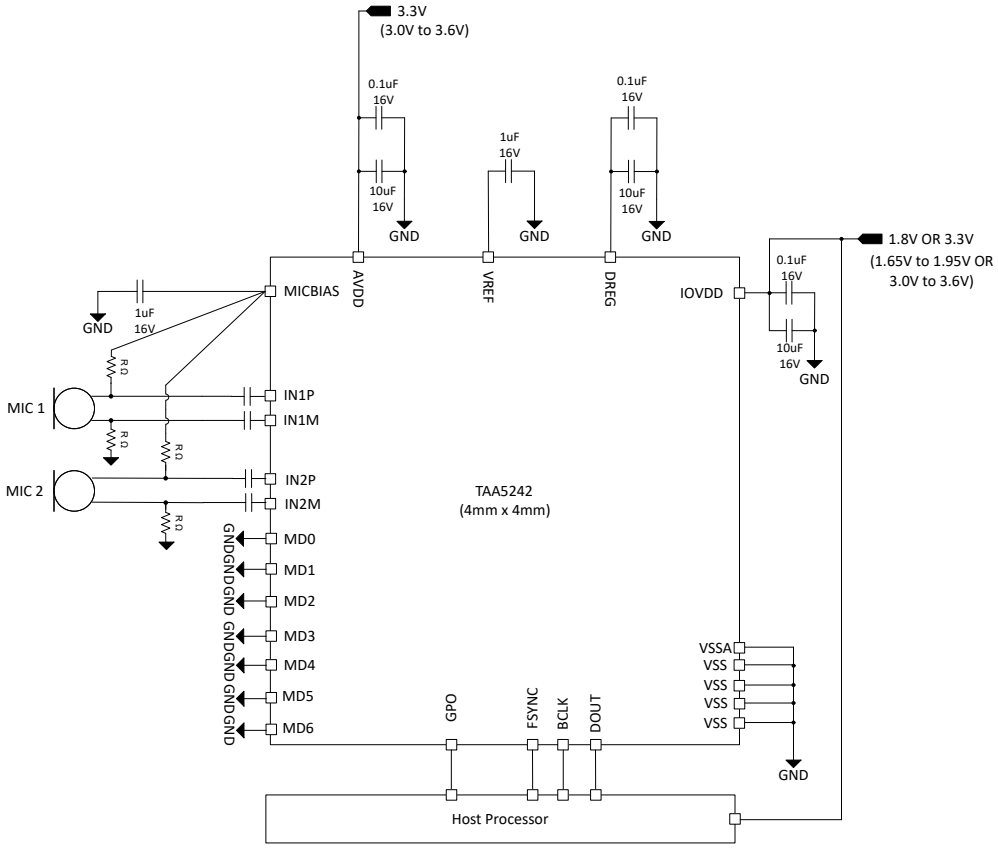


図 7-1. Stereo Differential AC-Coupled Microphone in Target I²S Mode, Block Diagram

7.2.2 Design Requirements

表 7-1 lists the design parameters for this application.

表 7-1. Design Parameters

PARAMETER	VALUE
AVDD	1.8V or 3.3V
IOVDD	1.8V or 3.3V
AVDD supply current consumption	12mA, with AVDD = 3.3V
IOVDD supply current consumption	0.1mA, with IOVDD = 3.3V
Maximum MICBIAS current	5mA

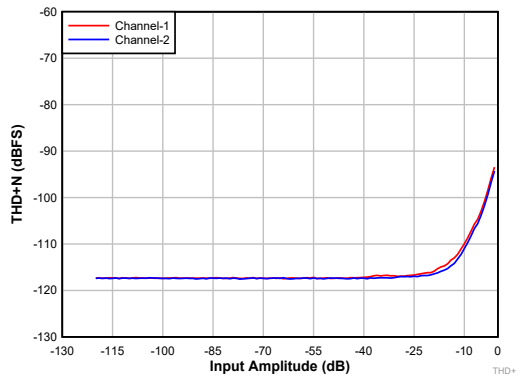
7.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAA5242 for this specific application.

1. Audio Serial Interface (ASI) Mode is configured based on the MD0 pin setting which needs to be provided along with the power supplies. Configure MD0 to be to be either pulled up to AVDD or down to VSS with appropriate resistor values. MD0 is to be grounded for this application case.
2. Apply power to the device:
   a. Power up the AVDD and IOVDD supplies.
   b. Ensure that MD0 pin setting is stable as soon as power supplies are up and wait for at least 2ms to allow the device to initialize for this mode of operation.
   c. The device is now in sleep mode (low power mode <1.5mA).
3. Configure the Mode pins MD1 to MD6 as per the system requirements:
   a. Pull up to IOVDD or pull down to VSS on MD1 to MD6 pins as per the required configuration. The MD1 to MD6 pins are grounded for this application's use-case.
4. Apply the ASI clocks (BCLK and FSYNC) to wake up the device.
5. To put the device back in sleep mode, stop the clocks:
   a. Wait at least 100ms to allow the device to complete shutdown sequence.
   b. Change the device configurations by changing MD1 to MD6 pin settings as per requirement.
6. To change the ASI mode, re-configure MD0 pin and power-cycle the device.
7. Repeat steps 1-6 as required for mode transitions.

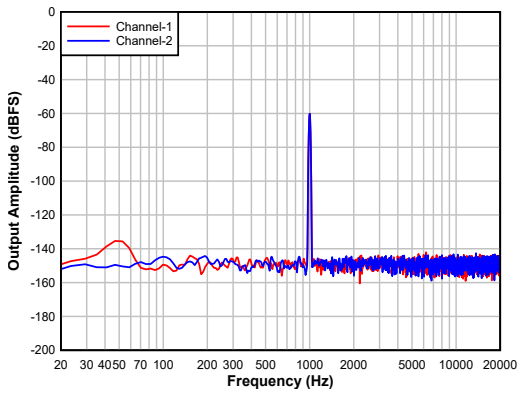
7.2.4 Application Performance Plots

At T_A = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f_{IN} = 1kHz sinusoidal signal, f_S = 48kHz, 32-bit audio data, BCLK = 256×f_S, TDM target mode, and linear phase decimation filter, with differential AC-coupled line-input configuration; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted



AC-coupled differential line input

図 7-2. ADC THD+N Level vs Input



Differential output, -60dBFS input

図 7-3. ADC FFT with -60dBFS Input

7.3 Power Supply Recommendations

The power supply sequence between the IOVDD and AVDD rails can be applied in any order. MD0 pin should be provided along with the power supplies and should be stable as soon as the supplies are settled to the recommended operating voltage levels. Only initiate the clocks to initialize the device after all the other Mode pins (MD1 to MD6) are also stable.

For the supply power-up requirement, t_1, t_2 and t_3 must be at least 2ms to allow the device to initialize the internal settings. See the *セクション 6.3.1* section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, t_4, t_5 and t_6 must be at least 10ms. This timing (as shown in 図 7-4) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into a low power mode.

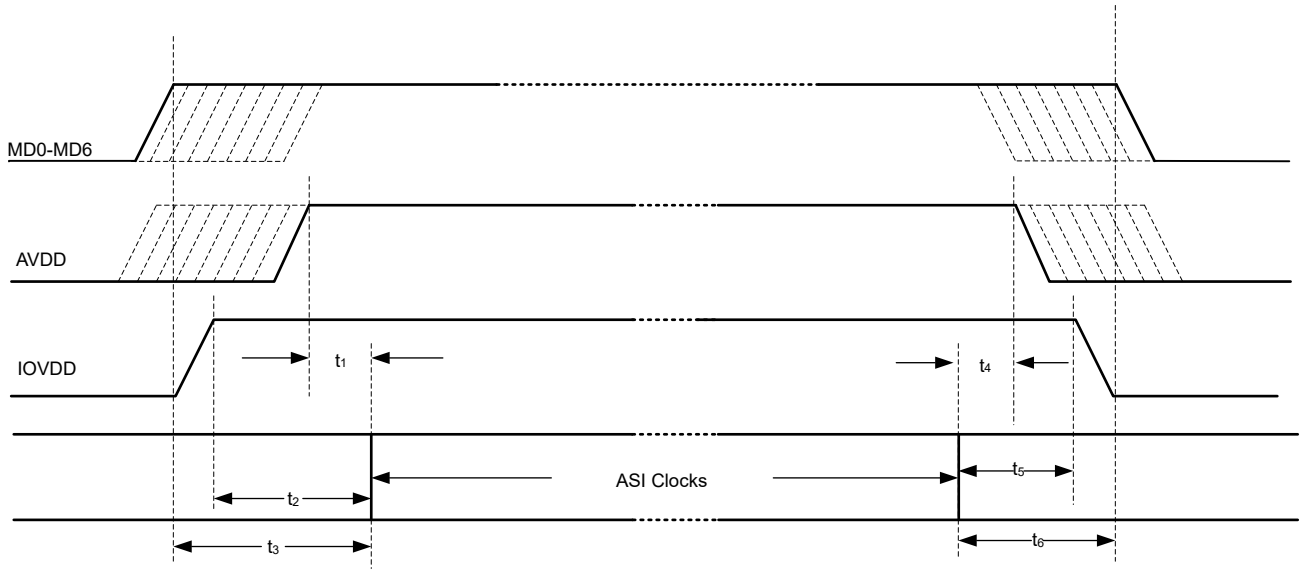


図 7-4. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 0.1V/µs and that the wait time between a power-down and a power-up event is at least 100 ms.

The TAA5242 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG and integrated internal analog regulator.

7.4 Layout

7.4.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- Use the same ground between VSS and VSSA to avoid any potential voltage difference between them.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- Avoid running high-frequency clock and control signals near INxx pins where possible.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for good performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply traces for multiple microphones to avoid coupling across microphones.
- Provide a direct connection from the VREF and MICBIAS external capacitor ground terminal to the VSS pin.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

7.4.2 Layout Example

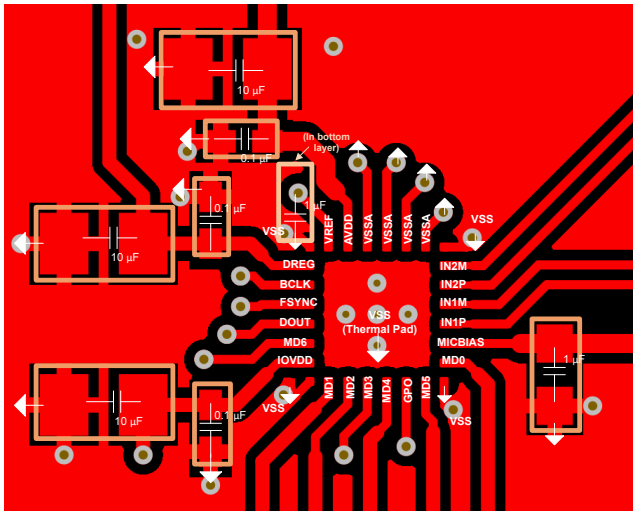


図 7-5. Example Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TAx5x42EVM-K Hardware Control Evaluation Module* User's Guide

8.2 ドキュメントの更新通知を受け取る方法

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2024) to Revision A (April 2024)	Page
• デバイスのステータスを「量産データ」に更新。	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAA5242IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TAA5242	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

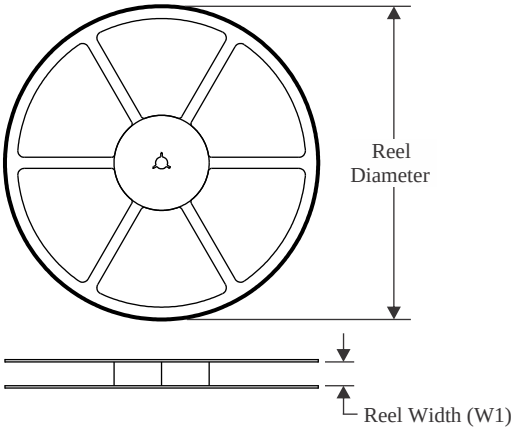
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

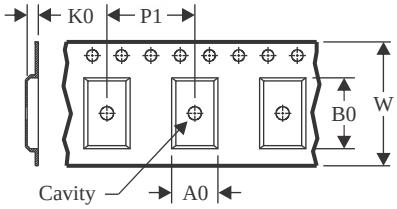
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

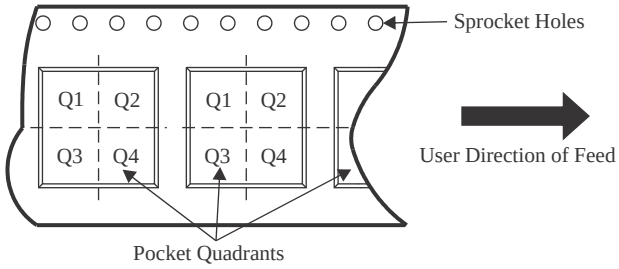


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

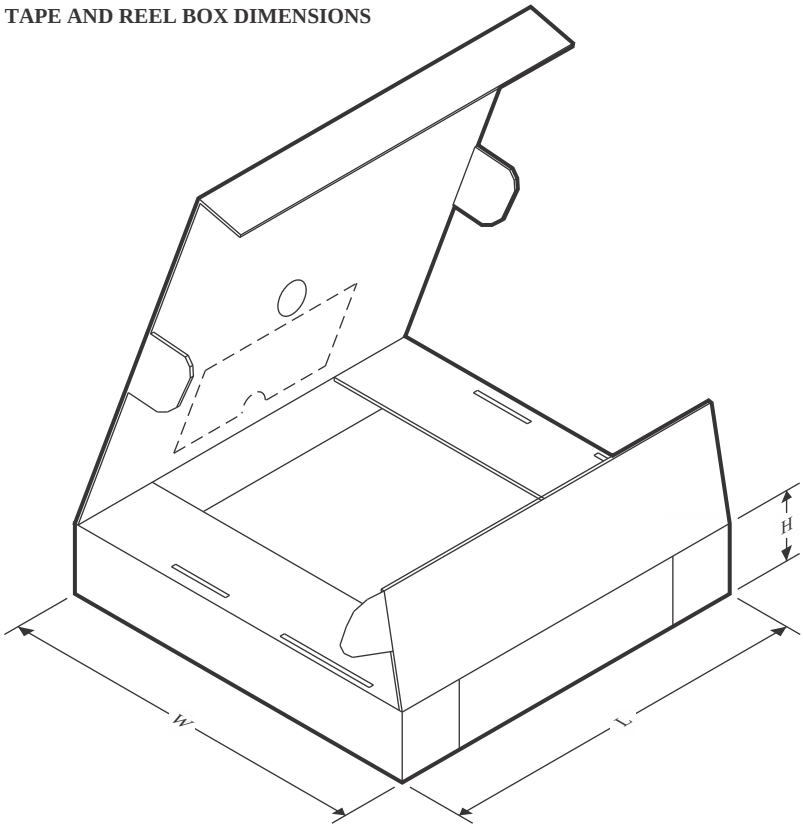
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAA5242IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



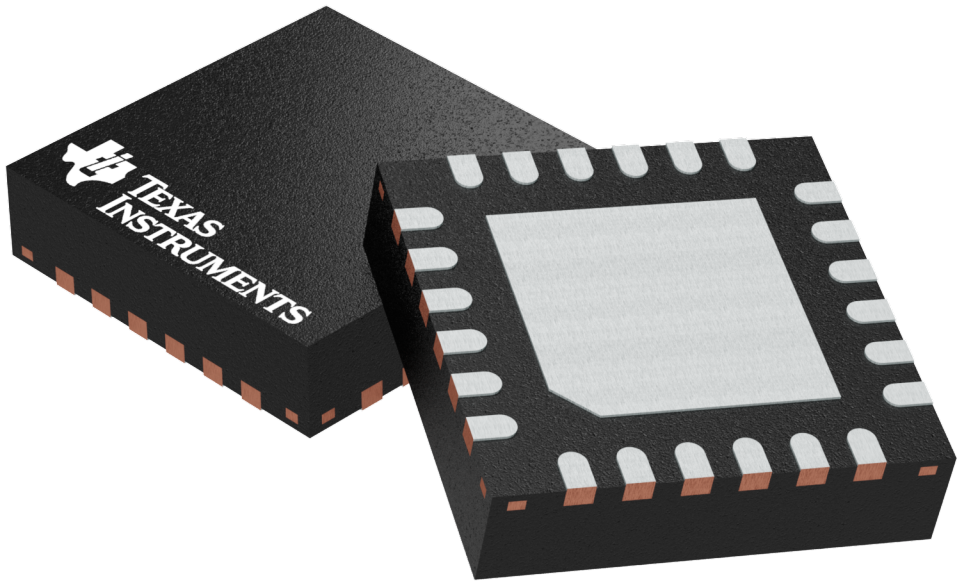
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAA5242IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

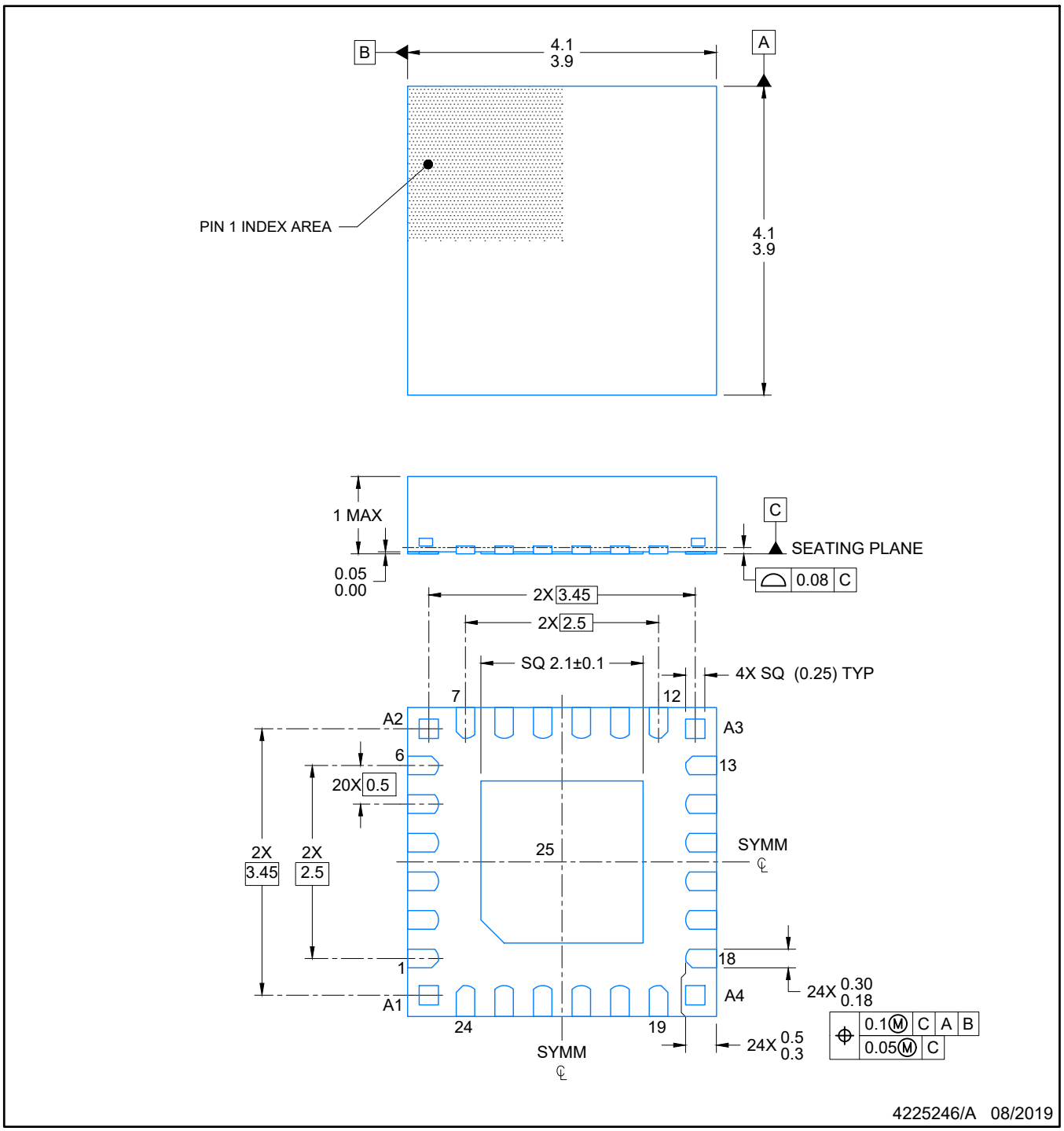
4204104/H

PACKAGE OUTLINE

RGE0024R

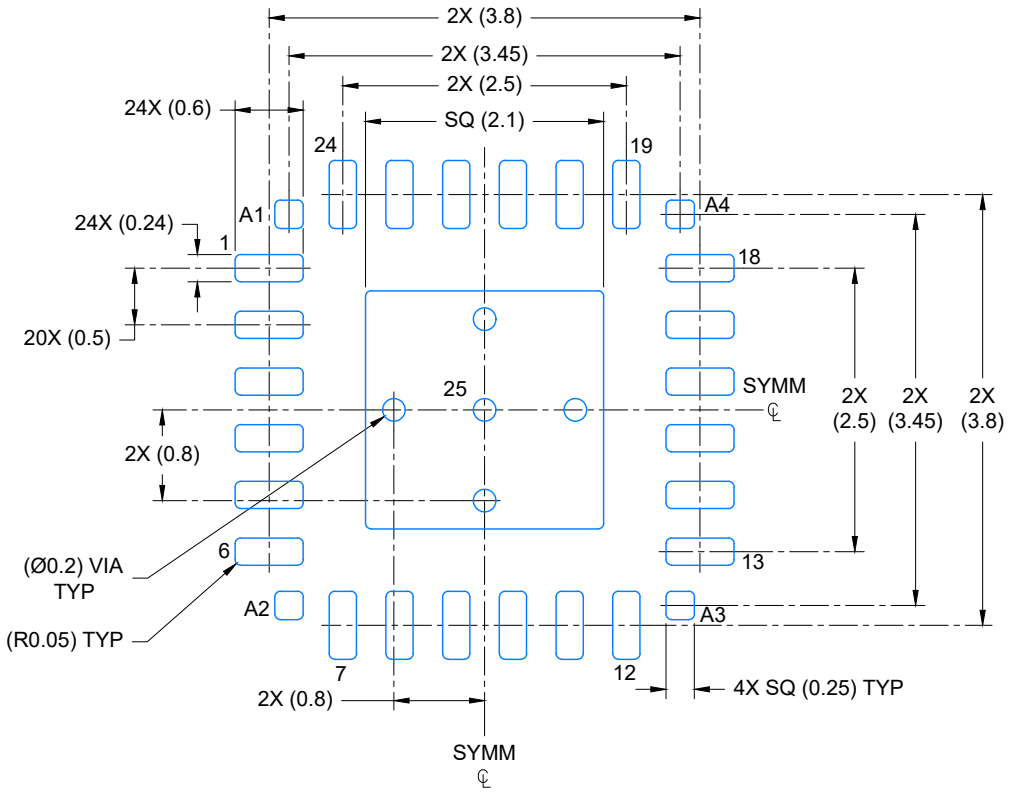
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

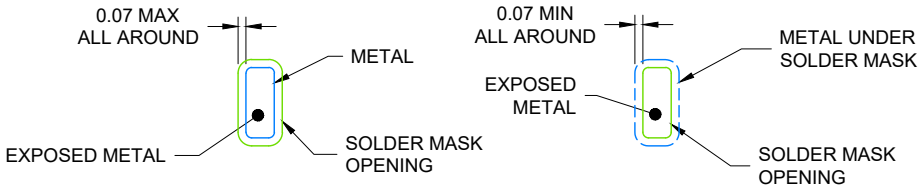


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

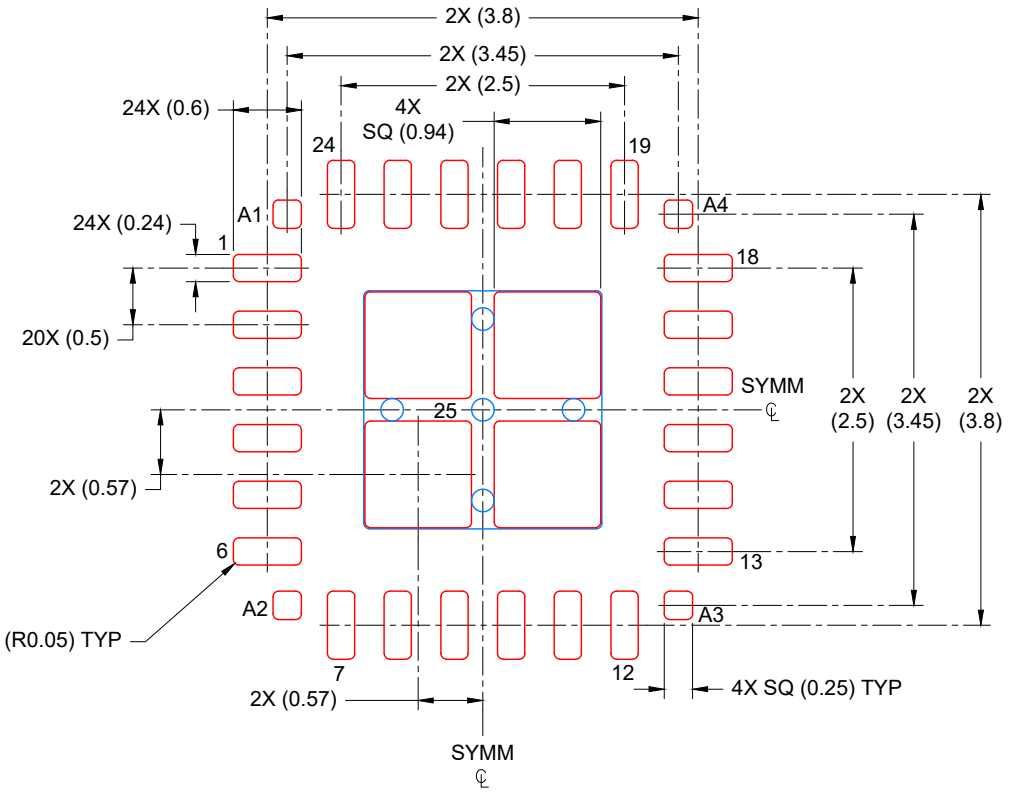
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4225246/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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