

## SN74TVC3306 デュアル電圧クランプ

### 1 特長

- 電圧制限アプリケーションで使用できるように設計
- ポート A と B の間は  $3.5\Omega$  のオン状態接続
- フロースルー・ピン配置によりプリント基板の配線を簡素化
- GTL+ レベルとのダイレクト・インターフェイス
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護:
  - 人体モデルで 2000V
  - マシン・モデルで 200V
  - 荷電デバイス・モデルで 1000V

### 2 アプリケーション

- 電圧レベル変換
- 信号スイッチング
- バス絶縁

### 3 概要

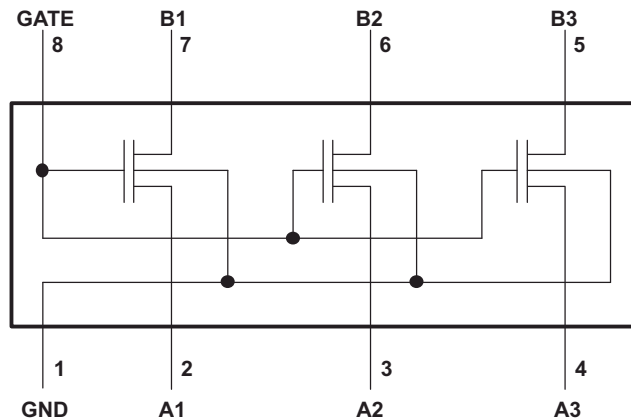
**SN74TVC3306** このデバイスには、共通のバッファなしゲートを持つ 3 個の並列 NMOS パス・トランジスタが搭載されています。スイッチのオン状態の抵抗が低いため、最小の伝播遅延で接続が可能です。

このデバイスは、リファレンス・トランジスタにゲートをカスケード接続したデュアル・スイッチとして使用できます。各パス・トランジスタの低電圧側は、リファレンス・トランジスタによって設定された電圧に制限されます。これは、High 状態の電圧レベルのオーバーシュートに敏感な入力を持つ部品を保護するためです。

#### パッケージ情報

部品番号	パッケージ <sup>(1)</sup>	パッケージ・サイズ <sup>(2)</sup>
SN74TVC3306	DCT (SSOP, 8)	2.95mm × 4mm
	DCU (VSSOP, 8)	2mm × 3.1mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



この SN74TVC3306 デバイスは、多くの電圧レベルにわたって双方向機能を備えています。このデータシートに記載されている電圧レベルは例です。

概略回路図

## Table of Contents

<b>1 特長</b> .....	1	<b>7 Parameter Measurement Information</b> .....	7
<b>2 アプリケーション</b> .....	1	<b>8 Detailed Description</b> .....	8
<b>3 概要</b> .....	1	8.1 Overview.....	8
<b>4 Revision History</b> .....	2	8.2 Functional Block Diagram.....	8
<b>5 Pin Configuration and Functions</b> .....	3	8.3 Feature Description.....	8
<b>6 Specifications</b> .....	4	8.4 Device Functional Modes.....	8
6.1 Absolute Maximum Ratings.....	4	<b>9 Application and Implementation</b> .....	9
6.2 ESD Ratings.....	4	9.1 Application Information.....	9
6.3 Recommended Operating Conditions.....	4	9.2 Typical Application.....	9
6.4 Thermal Information.....	4	9.3 Power Supply Recommendations.....	10
6.5 Electrical Characteristics.....	5	9.4 Layout.....	10
6.6 Switching Characteristics (AC, $V_{GATE} = 3.3\text{ V}$ , Translating Down).....	5	<b>10 Device and Documentation Support</b> .....	12
6.7 Switching Characteristics (AC, $V_{GATE} = 2.5\text{ V}$ , Translating Down).....	5	10.1 ドキュメントの更新通知を受け取る方法.....	12
6.8 Switching Characteristics (AC, $V_{GATE} = 3.3\text{ V}$ , Translating Up).....	5	10.2 サポート・リソース.....	12
6.9 Switching Characteristics (AC, $V_{GATE} = 2.5\text{ V}$ , Translating Up).....	6	10.3 Trademarks.....	12
6.10 Typical Characteristics.....	6	10.4 静電気放電に関する注意事項.....	12
		10.5 用語集.....	12
		<b>11 Mechanical, Packaging, and Orderable Information</b> .....	12

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision D (December 2014) to Revision E (September 2023)</b>	<b>Page</b>
• ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....	1
• Changed the thermal values to reflect device performance.....	4
• Changed the switching characteristics to reflect device performance.....	5

<b>Changes from Revision C (March 2002) to Revision D (December 2014)</b>	<b>Page</b>
• 「アプリケーション」セクション、「製品情報」表、「ピン機能」表、「取り扱いに関する定格」表、「熱に関する情報」表、「代表的特性」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• 「注文情報」表を削除.....	1
• Changed the $R_{ON}$ parameter in the <i>Electrical Characteristics</i> table.....	5

## 5 Pin Configuration and Functions

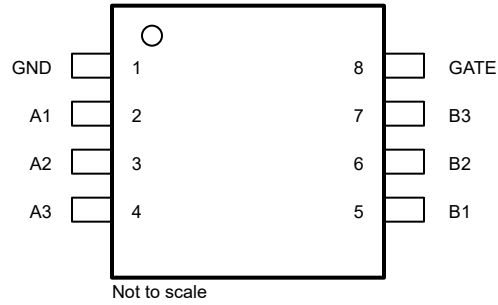


图 5-1. DCT or DCU Package, 8-Pin SOP or VSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A1	2	I/O	I/O of gate 1
A2	3	I/O	I/O of gate 1
A3	4	I/O	I/O of gate 1
B1	5	I/O	I/O of gate 2
B2	6	I/O	I/O of gate 2
B3	7	I/O	I/O of gate 2
GATE	8	I	Gate pin. Set high to enable the switches. Connect to B1 ( $V_{BIAS}$ ) for translation application.
GND	1	—	Ground

(1) I = input, O = output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_{I/O}$	Input/output voltage range <sup>(2)</sup>	-0.5	7	V
	Continuous channel current		128	mA
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	2000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5	V
$V_{GATE}$	GATE voltage	0	5	V
$I_{PASS}$	Pass transistor current		64	mA
$T_A$	Operating free-air temperature	-40	85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74TVC3306		UNIT	
	DCT	DCU		
	8 PINS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	254.1	275.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.6	127.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	168.8	186.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	70.1	65.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	167.4	185.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	$I_I = -18$ mA,	$V_{GATE} = 0$			-1.2	V
$I_{IH}$	$V_I = 5$ V,	$V_{GATE} = 0$			5	$\mu$ A
$C_{i(GATE)}$	$V_I = 3$ V or 0			11		pF
$C_{io(off)}$	$V_O = 3$ V or 0,	$V_{GATE} = 0$		4	6	pF
$C_{io(on)}$	$V_O = 3$ V or 0,	$V_{GATE} = 3$ V		10.5	12.5	pF
$R_{on}$ <sup>(2)</sup>	$V_I = 0$ ,	$I_O = 64$ mA	$V_{GATE} = 4.5$ V	3.5	5.5	$\Omega$
			$V_{GATE} = 3$ V	4.7	7	
			$V_{GATE} = 2.3$ V	6.3	9.5	
	$V_I = 2.4$ V,	$I_O = 15$ mA	$V_{GATE} = 4.5$ V	4.8	7.5	
	$V_I = 1.8$ V,	$I_O = 15$ mA	$V_{GATE} = 4.5$ V	4.5	5	

(1) All typical values are at  $T_A = 25^\circ\text{C}$ .

(2) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

## 6.6 Switching Characteristics (AC, $V_{GATE} = 3.3$ V, Translating Down)

over recommended operating free-air temperature range,  $V_{GATE} = 3.3$  V,  $V_{IH} = 3.3$  V,  $V_{IL} = 0$ , and  $V_M = 1.15$  V (unless otherwise noted) (see [7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	0	0.8	0	0.6	0	0.3	ns
$t_{PHL}$			0	1.2	0	1	0	0.75	

## 6.7 Switching Characteristics (AC, $V_{GATE} = 2.5$ V, Translating Down)

over recommended operating free-air temperature range,  $V_{GATE} = 2.5$  V,  $V_{IH} = 2.5$  V,  $V_{IL} = 0$ , and  $V_M = 0.75$  V (unless otherwise noted) (see [7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	0	1	0	0.7	0	0.4	ns
$t_{PHL}$			0	1.3	0	1	0	0.75	

## 6.8 Switching Characteristics (AC, $V_{GATE} = 3.3$ V, Translating Up)

over recommended operating free-air temperature range,  $V_{GATE} = 3.3$  V,  $V_{IH} = 2.3$  V,  $V_{IL} = 0$ ,  $V_T = 3.3$  V,  $V_M = 1.15$  V, and  $R_L = 300$   $\Omega$  (unless otherwise noted) (see [7-1](#))

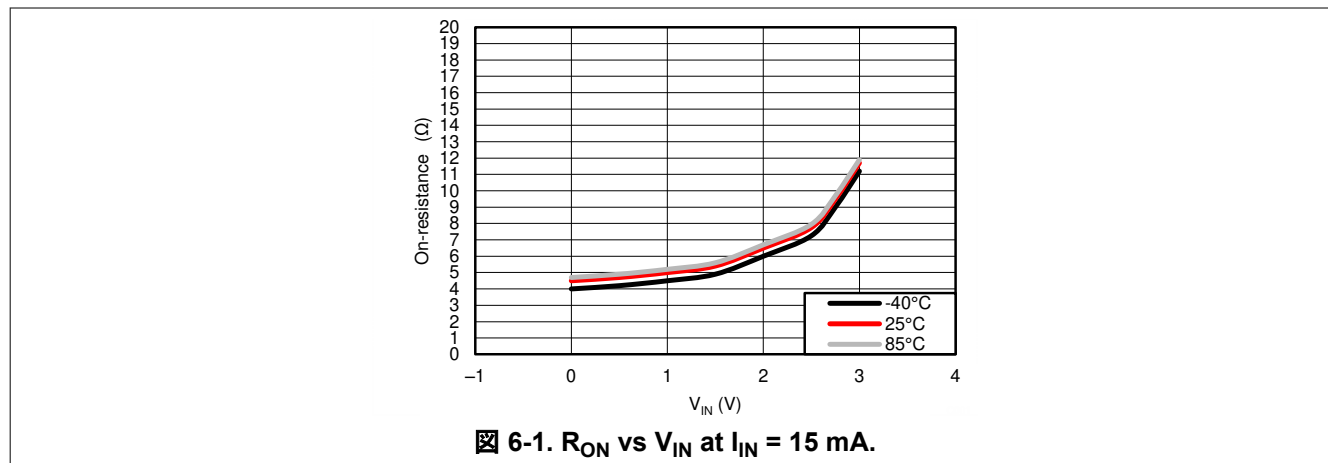
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	0	0.9	0	0.6	0	0.4	ns
$t_{PHL}$			0	1.4	0	1.1	0	1.0	

### 6.9 Switching Characteristics (AC, $V_{GATE} = 2.5\text{ V}$ , Translating Up)

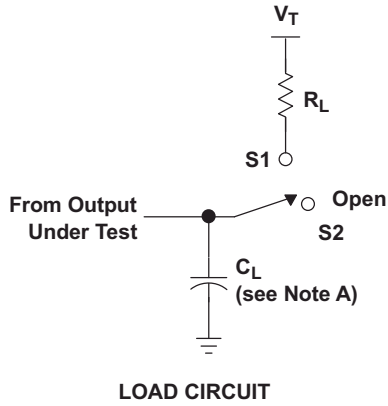
over recommended operating free-air temperature range,  $V_{GATE} = 2.5\text{ V}$ ,  $V_{IH} = 1.5\text{ V}$ ,  $V_{IL} = 0$ ,  $V_T = 2.5\text{ V}$ ,  $V_M = 0.75\text{ V}$ , and  $R_L = 300\ \Omega$  (unless otherwise noted) (see [7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	0	1	0	0.6	0	0.4	ns
$t_{PHL}$			0	1.3	0	1.3	0	1.3	

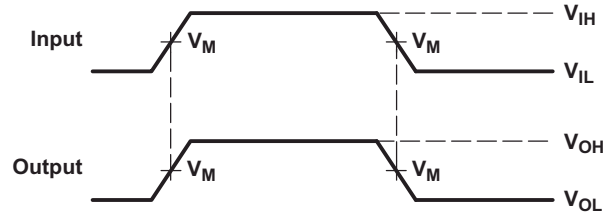
### 6.10 Typical Characteristics



## 7 Parameter Measurement Information



USAGE	SWITCH
Translating up	S1
Translating down	S2



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.  
 C. The outputs are measured one at a time, with one transition per measurement.

**7-1. Load Circuit for Outputs**

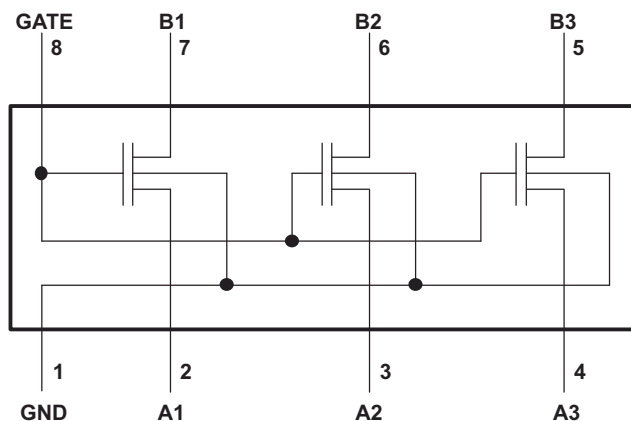
## 8 Detailed Description

### 8.1 Overview

The SN74TVC3306 device provides three parallel NMOS pass transistors with a common unbuffered gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a dual switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots.

### 8.2 Functional Block Diagram



The SN74TVC3306 device has bidirectional capability across many voltage levels. The voltage levels documented in this data sheet are examples.

### 8.3 Feature Description

#### 8.3.1 Voltage Clamping

The internal NMOS transistors allow the SN74TVC3306 device to act as a voltage clamp and be configured as a voltage level translator. For more information, see [Application and Implementation](#).

### 8.4 Device Functional Modes

#### 8.4.1 Voltage Clamping

Whenever the signal on the inputs on the side with  $V_{REF}$  goes higher than  $V_{REF}$ , the voltage clamps on the opposite side to the value of  $V_{DPU}$  due to the pullup resistors. In this case, the voltage is translating up. For more information, see [Application and Implementation](#).

#### 8.4.2 Voltage Passing

Whenever the signal on the inputs on the VREF side is lower than VREF, the signal will pass to the other side as intended. In this case, the low pulse is staying low (no translation). For more information, see [Application and Implementation](#).



## 9 Application and Implementation

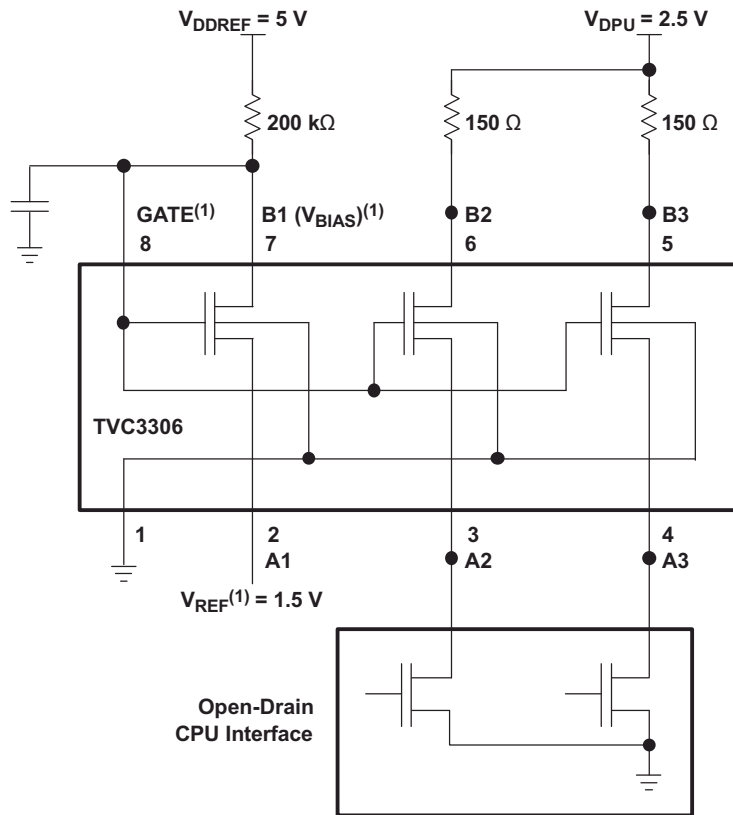
### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

Because of the voltage-clamping mechanism, the SN74TVC3306 device performs best as a level translator for signals that have sharp edges (as opposed to analog audio signals).

### 9.2 Typical Application



$V_{REF}$  and  $V_{BIAS}$  can be applied to any one of the pass transistors. GATE must be connected externally to  $V_{BIAS}$

☒ 9-1. Typical Application Circuit

## 9.2.1 Design Requirements

### 9.2.1.1 Application Operating Conditions

#### Application Operating Conditions (See [Figure 9-1](#))

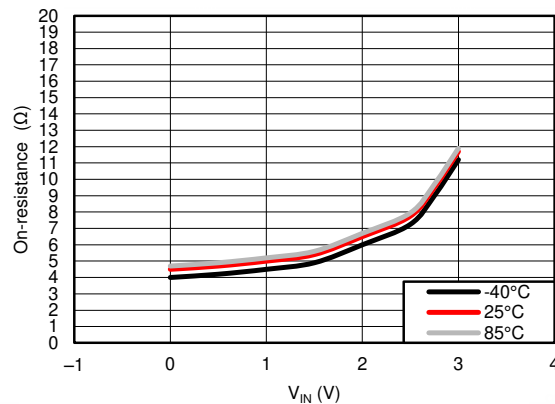
		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>BIAS</sub>	BIAS voltage	V <sub>REF</sub> + 0.6	2.1	5	V
V <sub>GATE</sub>	GATE voltage	V <sub>REF</sub> + 0.6	2.1	5	V
V <sub>REF</sub>	Reference voltage	0	1.5	4.4	V
V <sub>DPU</sub>	Drain pullup voltage	2.36	2.5	2.64	V
I <sub>PASS</sub>	Pass-transistor current		14		mA
I <sub>REF</sub>	Reference-transistor current		5		μA
T <sub>A</sub>	Operating free-air temperature	-40		85	°C

(1) All typical values are at T<sub>A</sub> = 25°C.

### 9.2.2 Detailed Design Procedure

For the clamping configuration, the common GATE input must be connected to one side (An or Bn) of any one of the pass transistors, making that the V<sub>BIAS</sub> connection of the reference transistor and the opposite side (Bn or An) the V<sub>REF</sub> connection. When V<sub>BIAS</sub> is connected through a 200-kΩ resistor to a 3-V to 5.5-V V<sub>CC</sub> supply and V<sub>REF</sub> is set to 0 V to V<sub>CC</sub> – 0.6 V, the output of each switch has a maximum clamp voltage equal to V<sub>REF</sub>. A filter capacitor on V<sub>BIAS</sub> is recommended.

### 9.2.3 Application Curves



**Figure 9-2. On-Resistance vs VIN (A to B, 15 mA Current)**

## 9.3 Power Supply Recommendations

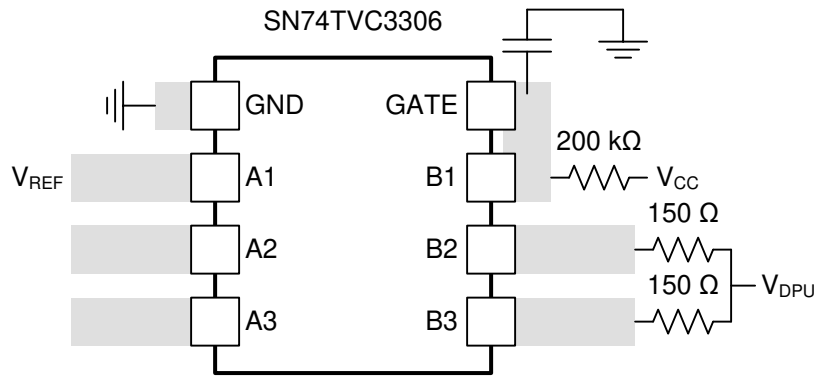
A 200-kΩ resistor is recommended from the input to V<sub>CC</sub> when the device is being used as a voltage clamp. A filter capacitor is recommended on B1 as well.

## 9.4 Layout

### 9.4.1 Layout Guidelines

If used, the filter capacitor should be placed as close to the input of the device as possible.

### 9.4.2 Layout Example



 **9-3. Layout Example for Voltage-Clamp Configuration**

## 10 Device and Documentation Support

### 10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.2 サポート・リソース

**TI E2E™ サポート・フォーラム**は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74TVC3306DCTR	ACTIVE	SSOP	DCT	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	FA6 (S, Y)	<a href="#">Samples</a>
SN74TVC3306DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	(FA6, FA6P, FA6S)	<a href="#">Samples</a>
SN74TVC3306DCURG4	NRND	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA6S	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74TVC3306DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74TVC3306DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74TVC3306DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74TVC3306DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74TVC3306DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74TVC3306DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0





4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

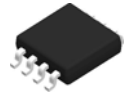


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

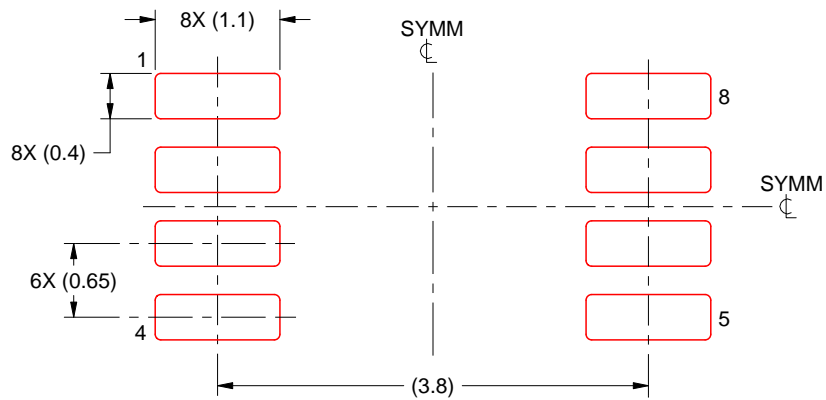
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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