

SN74LVC1G14-Q1 シングル・シュミット・トリガ・インバータ

1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
 - デバイス温度グレード 1: -40°C ~ +125°C の動作時 周囲温度範囲
 - デバイス人体モデル (HBM) ESD 分類レベル 2
 - デバイス帯電モデル (CDM) ESD 分類レベル C5
- 5V V_{CC} 動作をサポート
- 5.5V までの入力電圧に対応
- 最大 t_{pd} 4.6ns (3.3V 時)
- 低い消費電力、最大 I_{CC} : 10 μ A
- 3.3V において ± 24 mA の出力駆動能力
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- 車体制御モジュール
- エンジン制御モジュール
- インフォテインメント・システム
- テレマティクス

3 概要

このシングル・シュミット・トリガ・インバータは、1.65V ~ 5.5V の V_{CC} で動作するように設計されています。

SN74LVC1G14-Q1 デバイスは 1 個のインバータを内蔵しており、ブール関数 $Y = \bar{A}$ を実行します。このデバイスは独立した 1 個のインバータとして機能しますが、シュミット動作によって、正方向の (V_{T+}) 信号と負方向の (V_{T-}) 信号に対する入力スレッショルド・レベルが異なることがあります。

このデバイスは、 I_{off} を使用する部分的パワーダウン・アプリケーション用の動作が完全に規定されています。 I_{off} 回路が出力をディセーブルにするので、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

製品情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
SN74LVC1G14-Q1	SC70 (5)	2.10mm × 2.00mm
	SON (6)	1.45mm × 1.00mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



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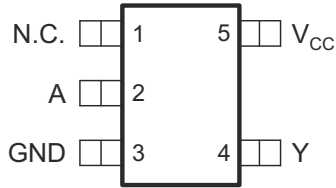
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4 Revision History

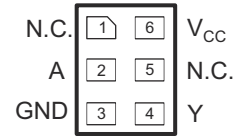
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2019) to Revision C (August 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Updated the pin numbers for V_{CC} and N.C. in the <i>Pin Functions</i> table for the DRY package to match the pin configuration.....	3
• Updated the <i>TPD Across Temperature at 3.3 V V_{CC}</i> image in the <i>Typical Characteristics</i>	6
Changes from Revision A (March 2017) to Revision B (August 2019)	Page
• 「製品情報」表に SON (6) DRY パッケージを追加.....	1
• Added DRY package pinout to <i>Pin Configurations and Functions</i> section	3
Changes from Revision * (February 2015) to Revision A (March 2017)	Page
• 「製品情報」表で、パッケージ・タイプを DCK (SC70) に変更し、本体サイズを訂正.....	1
• Deleted θ_{JA} from <i>Absolute Maximum Ratings</i> table.....	4

5 Pin Configuration and Functions



✎ 5-1. DCK Package 5-Pin SC70 (Top View)



N.C. – No internal connection
See mechanical drawings for dimensions.

✎ 5-2. DRY Package 6-Pin SON Transparent Top View

Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DCK (SC70) NO.	DRY (SON) NO.		
A	2	2	I	Input
GND	3	3	—	Ground
N.C.	1	1, 5	—	No internal connection.
V _{CC}	5	6	—	Supply or power pin
Y	4	4	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	6.5	V
V _I	Input voltage ⁽²⁾	-0.53	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ^{(2) (3)}	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

See⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4
		V _{CC} = 2.3 V		-8
		V _{CC} = 3 V		-16
				-24
V _{CC} = 4.5 V		-32		
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4
		V _{CC} = 2.3 V		8
		V _{CC} = 3 V		16
				24
V _{CC} = 4.5 V		32		
T _A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G14-Q1		UNIT
		DCK (SC70)	DRY (SON)	
		5 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	280	264	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	66	167	°C/W
R _{θJB}	Junction-to-board thermal resistance	67	142	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2	26	°C/W
ψ _{JB}	Junction-to-board characterization parameter	66	142	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#)

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{T+} Positive-going input threshold voltage		1.65 V	0.79		1.16	V
		2.3 V	1.11		1.56	
		3 V	1.5		1.87	
		4.5 V	2.16		2.74	
		5.5 V	2.61		3.33	
V _{T-} Negative-going input threshold voltage		1.65 V	0.39		0.64	V
		2.3 V	0.58		0.89	
		3 V	0.84		1.16	
		4.5 V	1.41		1.79	
		5.5 V	1.87		2.29	
ΔV _T Hysteresis (V _{T+} – V _{T-})		1.65 V	0.37		0.62	V
		2.3 V	0.48		0.77	
		3 V	0.56		0.87	
		4.5 V	0.71		1.04	
		5.5 V	0.71		1.11	
V _{OH}	I _{OL} = –100 μA	1.65 V to 4.5 V	V _{CC} – 0.1			V
	I _{OL} = –4 mA	1.65 V	1.2			
	I _{OL} = –8 mA	2.3 V	1.9			
	I _{OL} = –16 mA	3 V	2.4			
	I _{OL} = –24 mA		2.3			
	I _{OL} = –32 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 100 μA	1.65 V to 4.5 V			0.1	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.3	
	I _{OL} = 16 mA	3 V			0.4	
	I _{OL} = 24 mA				0.55	
	I _{OL} = 32 mA	4.5 V			0.70	
I _I	A input	V _I = 5.5 V or GND	0 to 5.5 V		±5	μA
I _{off}		V _I or V _O = 5.5 V	0		±10	μA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V		10	μA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500	μA

6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
C _i	V _I = V _{CC} or GND	3.3 V		4.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range (unless otherwise noted) (see [7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2.8	9.9	1.6	5.5	1.5	4.6	0.9	4.4	ns

6.7 Switching Characteristics, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range (unless otherwise noted) (see [7-2](#))

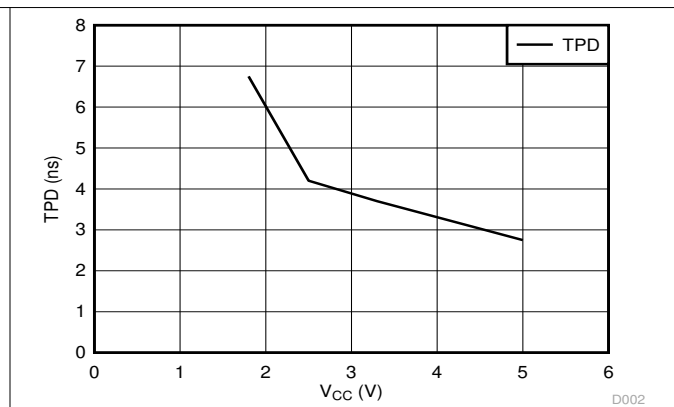
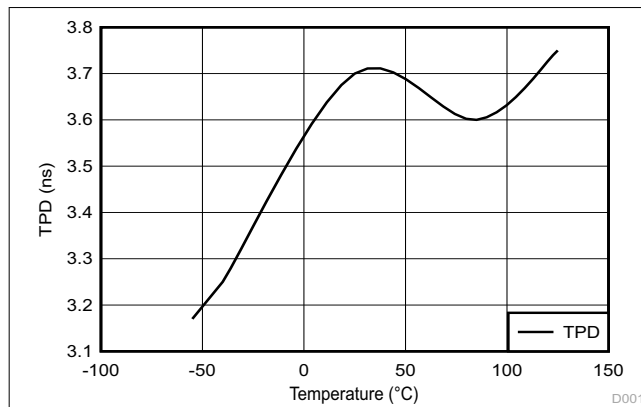
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	3.8	13	2	8	1.8	6.5	1.2	6	ns

6.8 Operating Characteristics

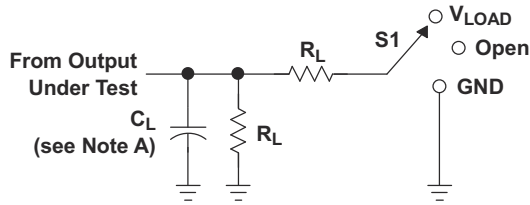
T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	20	21	22	25	pF

6.9 Typical Characteristics



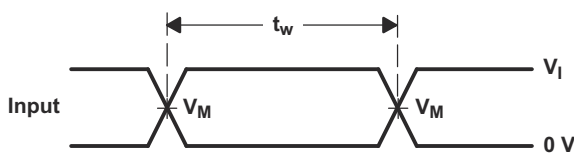
7 Parameter Measurement Information



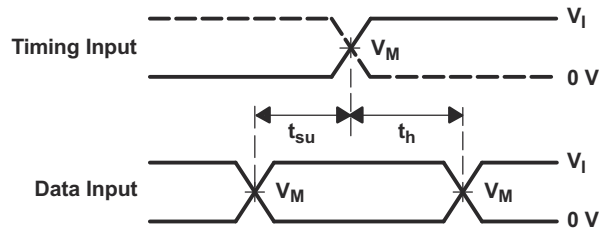
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

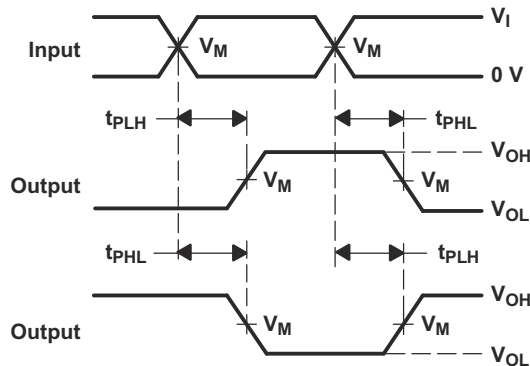
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



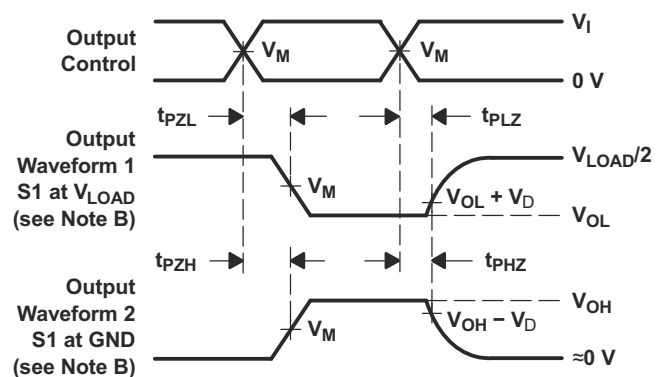
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



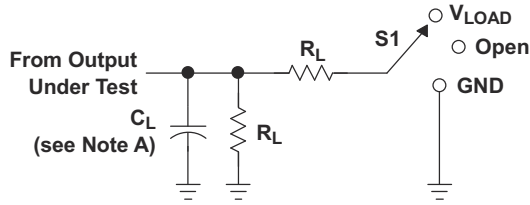
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

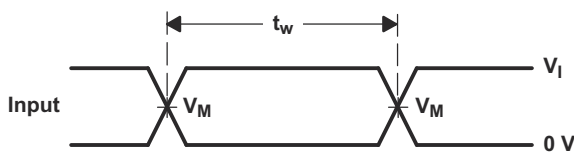
7-1. Load Circuit and Voltage Waveforms



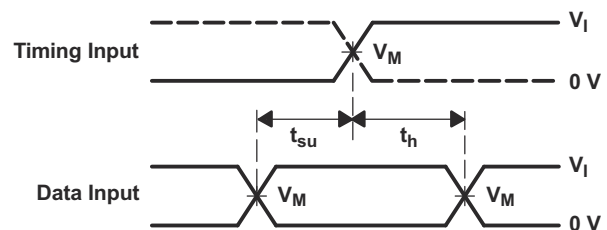
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

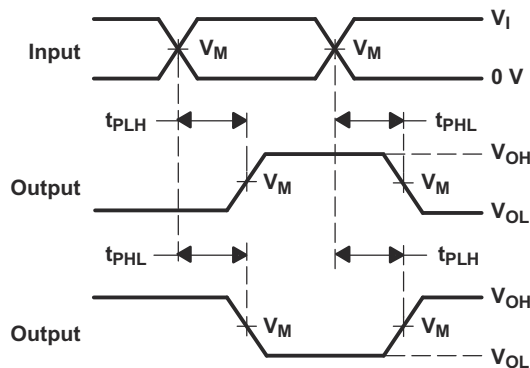
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



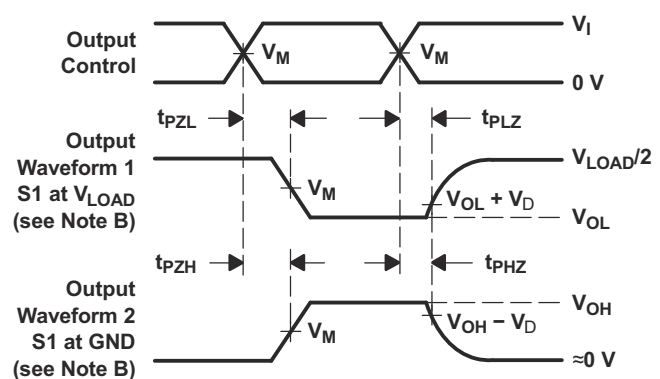
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

7-2. Load Circuit and Voltage Waveforms

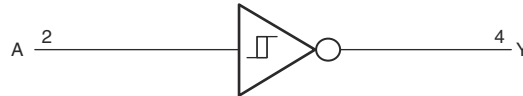
8 Detailed Description

8.1 Overview

The SN74LVC1G14-Q1 device contains one Schmitt Trigger Inverter and performs the Boolean function $Y = \bar{A}$. The device functions as an independent inverter, but because of Schmitt Trigger action, it will have different input threshold levels for a positive-going (V_{t+}) and negative-going (V_{t-}) signals.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuit disables the output, preventing damaging current back-flow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range
- Operates from 1.65 V to 5 V V_{CC} and Input Operation
- Inputs Accept Voltages to 5.5 V
- Allows down voltage translation
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation which allows voltages on the inputs and outputs, when V_{CC} is 0 V

8.4 Device Functional Modes

表 8-1 shows the functional modes of the SN74LVC1G14-Q1 device.

表 8-1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

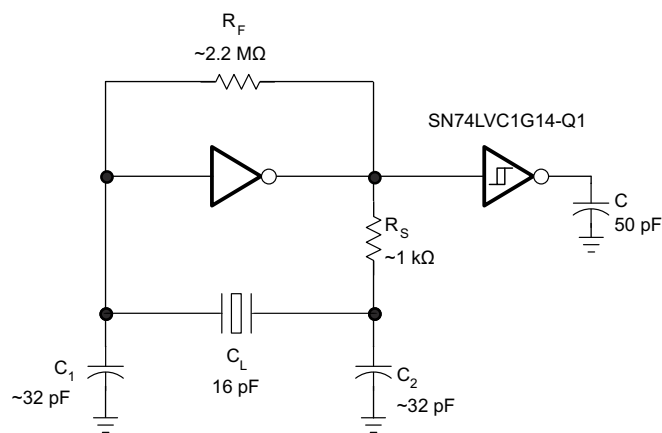
Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74LVC1G14-Q1 is a high drive CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC} .

9.2 Typical Application



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図 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

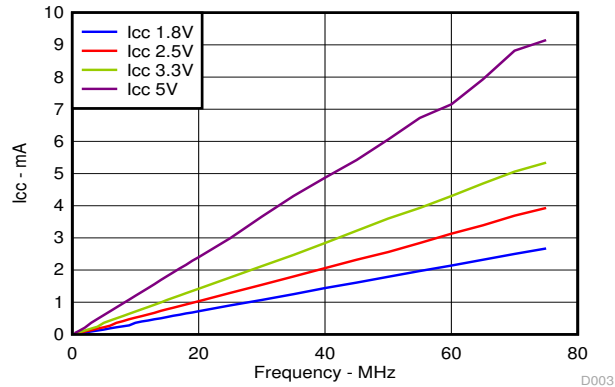
1. Recommended Input Conditions

- Rise time and fall time specs. See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
- Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the [Recommended Operating Conditions](#) table at any valid V_{CC} .

2. Recommended Output Conditions

- Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above V_{CC} .

9.2.3 Application Curve



9-2. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

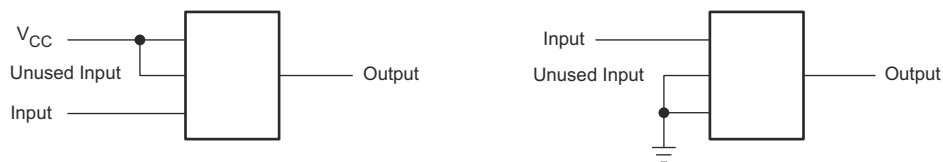
Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1- μF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01- μF or 0.022- μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input terminals should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

11.2 Layout Example



11-1. Layout Schematic

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G14QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(SJJ, SJM)	Samples
SN74LVC1G14QDRYRQ1	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FE	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G14-Q1 :

- Catalog : [SN74LVC1G14](#)
- Enhanced Product : [SN74LVC1G14-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G14QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G14QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G14QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
SN74LVC1G14QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

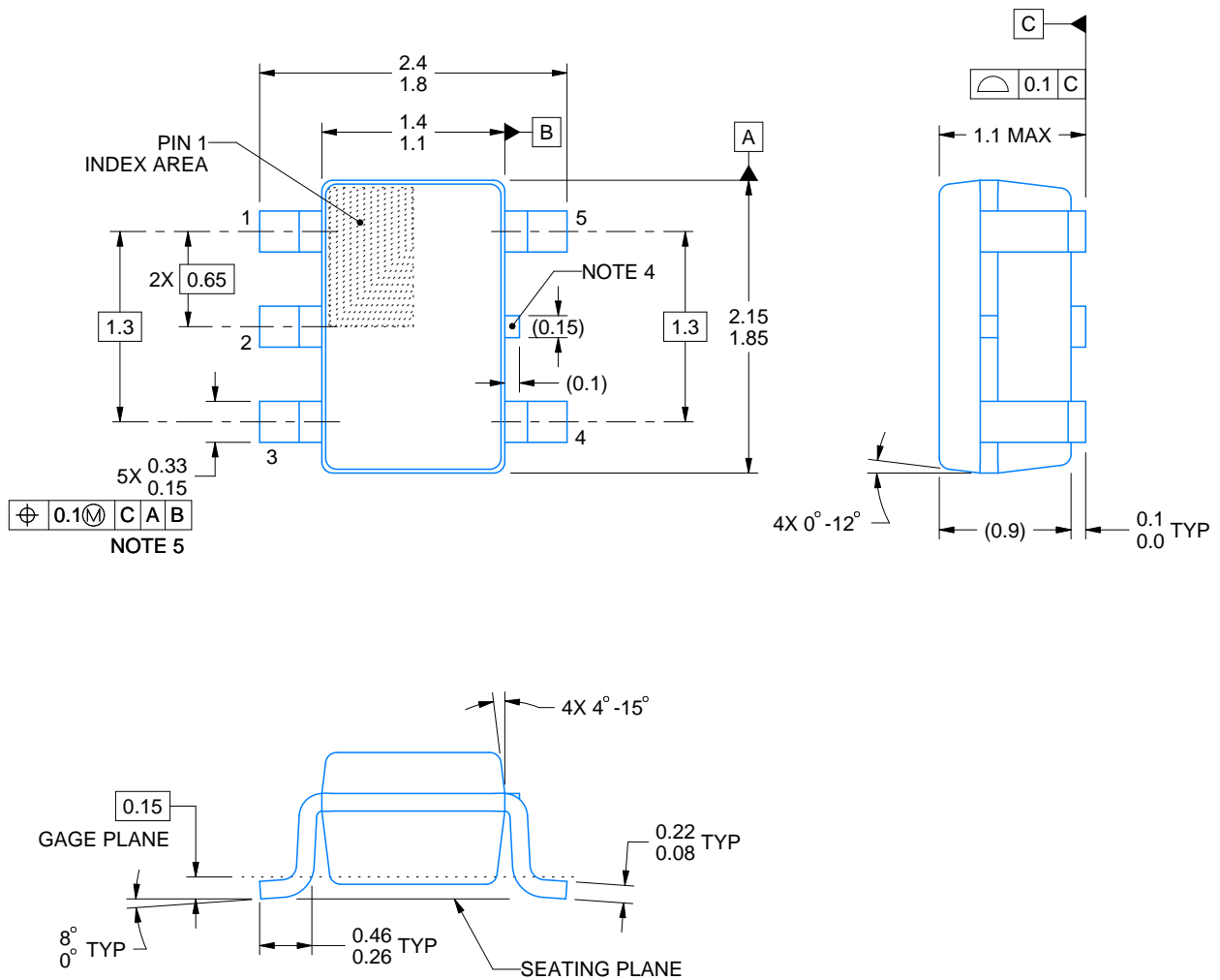


PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

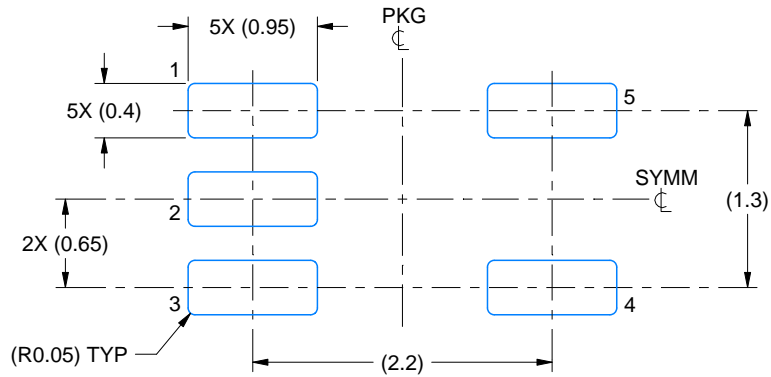
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Reference JEDEC MO-203.
- Support pin may differ or may not be present.
- Lead width does not comply with JEDEC.
- Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

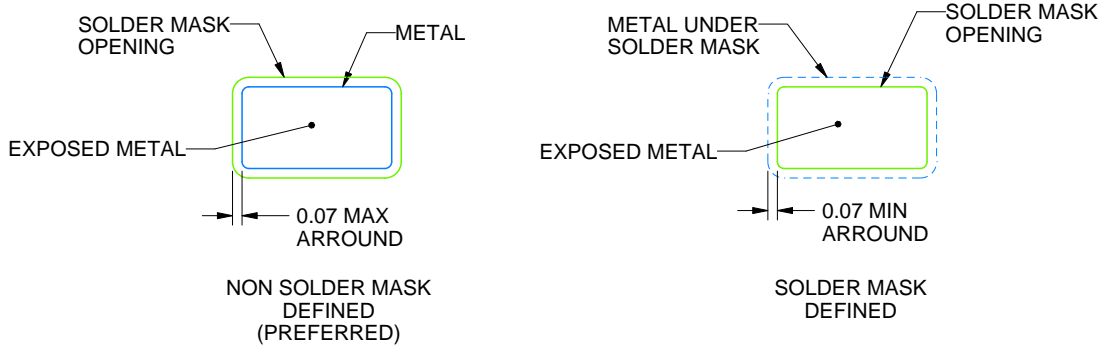
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

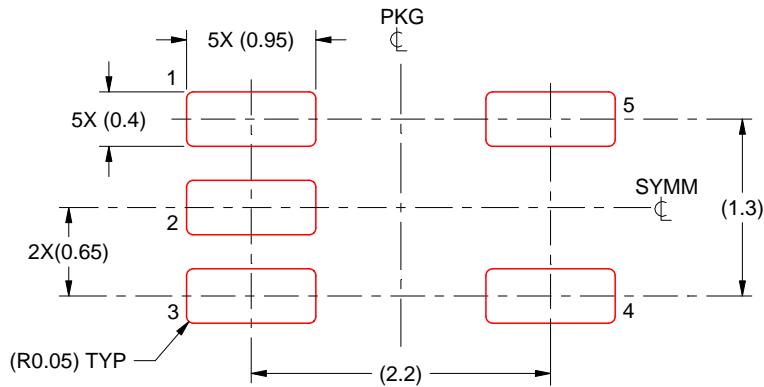
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

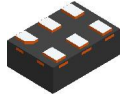
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

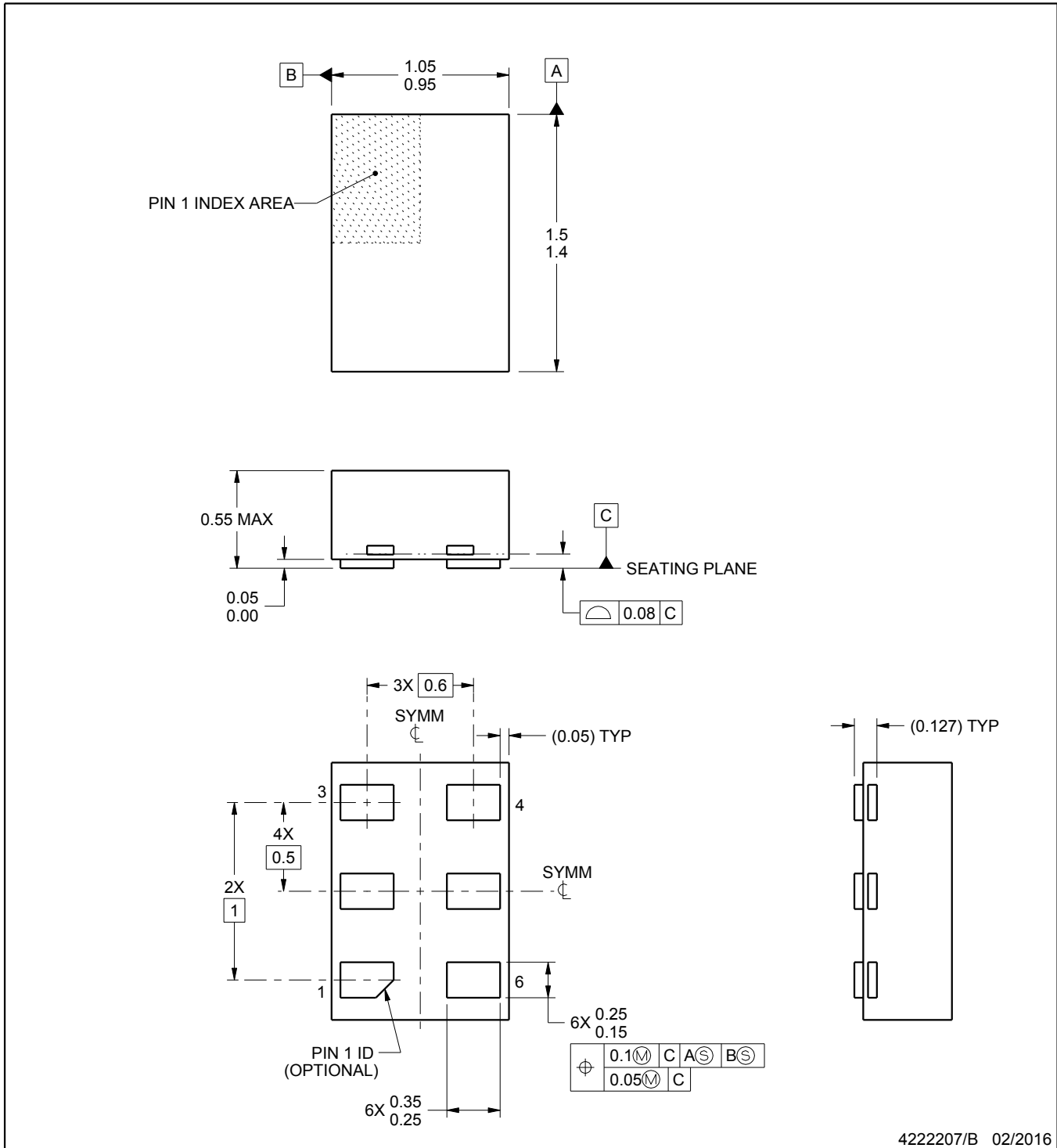
DRY0006B



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222207/B 02/2016

NOTES:

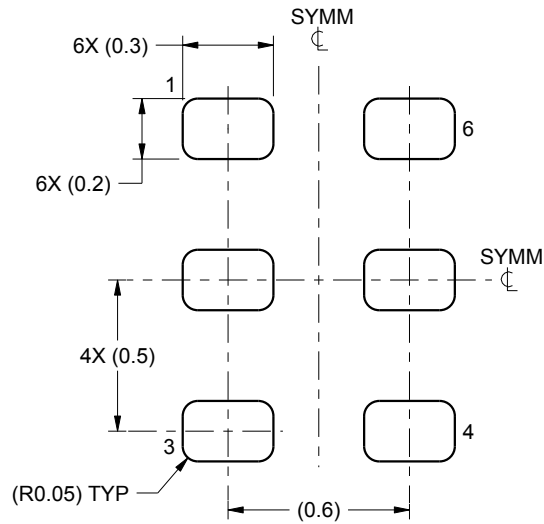
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

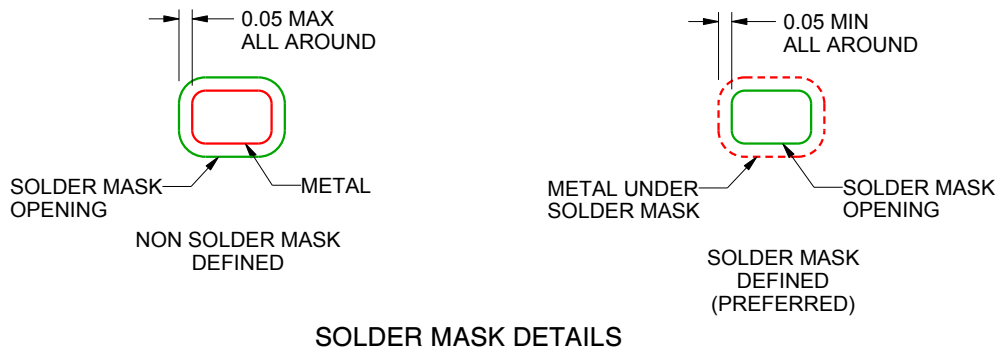
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

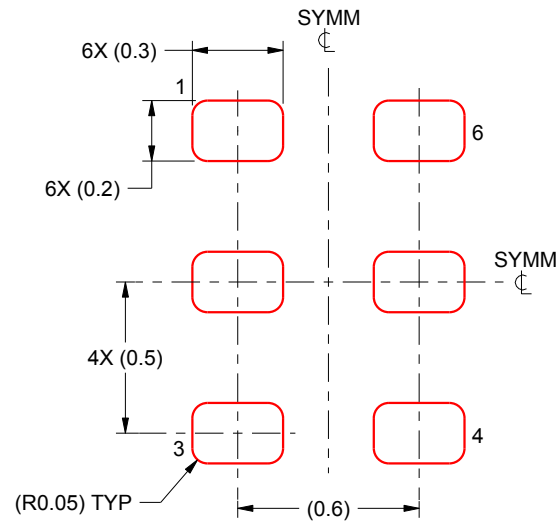
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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