

# SN74HCS86-Q1 車載用、シュミット・トリガ入力採用クワッド 2 入力 XOR ゲート

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - デバイス温度グレード 1:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ ,  $T_A$
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- 広い動作電圧範囲: 2V~6V
- シュミット・トリガ入力により低速の信号またはノイズの多い信号に対応
- 低消費電力
  - $I_{CC}$ : 100nA (標準値)
  - 入力リーク電流:  $\pm 100\text{nA}$  (標準値)
- 6V で  $\pm 7.8\text{mA}$  の出力駆動能力

## 2 アプリケーション

- 複数の入力信号の位相差を検出
- 選択可能なインバータ/バッファの作成

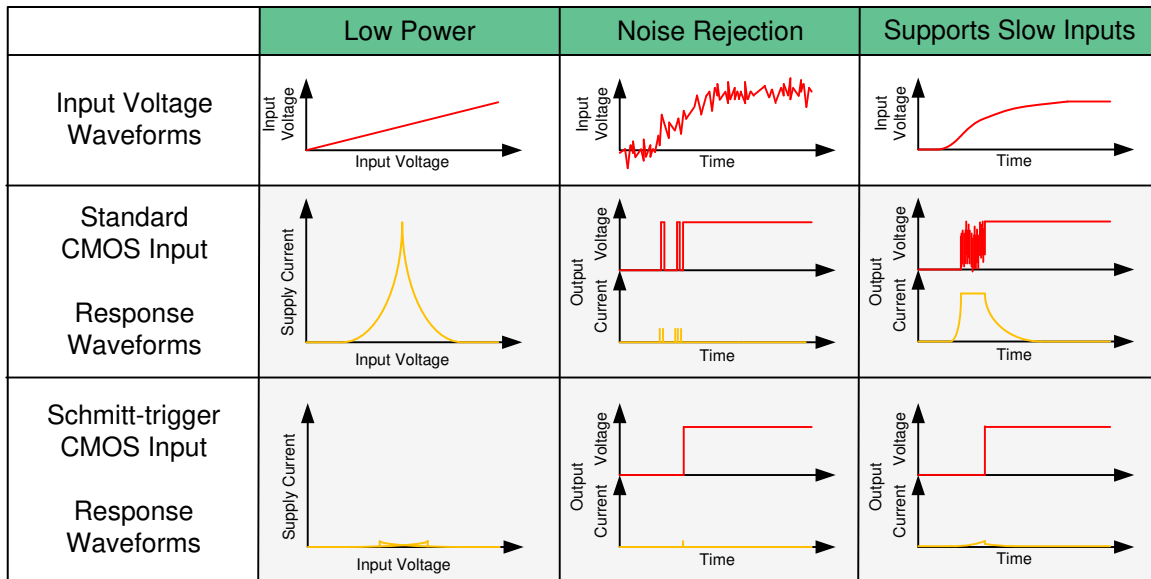
## 3 概要

このデバイスには、シュミット・トリガ入力採用の 4 つの独立した 2 入力 XOR ゲートが内蔵されています。各ゲートはブール関数  $Y = A \oplus B$  を正論理で実行します。

### デバイス情報

部品番号	パッケージ (1)	本体サイズ (公称)
SN74HCS86PW-Q1	TSSOP (14)	5.00mm × 4.40mm
SN74HCS86D-Q1	SOIC (14)	9.90mm × 3.90mm
SN74HCS86BQA-Q1	WQFN (14)	3.00mm × 2.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



シュミット・トリガ入力の利点



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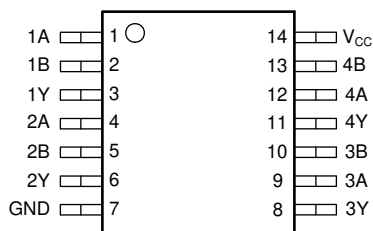
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## 4 Revision History

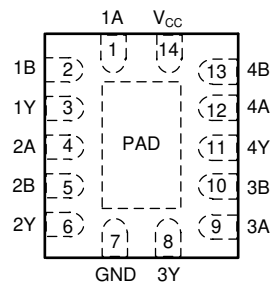
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (September 2019) to Revision C (March 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• 「デバイス情報」表に BQA パッケージの情報を追加.....	1
• Added BQA package information to <i>Pin Configuration and Functions</i> .....	3
• Added BQA package information to <i>Thermal Information</i> table.....	5
Changes from Revision A (August 2019) to Revision B (September 2019)	Page
• 「デバイス情報」表に D パッケージを追加.....	1
• Added D package information to <i>Pin Configuration and Functions</i> .....	3
• Added D package column to <i>Thermal Information</i> table.....	5
Changes from Revision * (July 2019) to Revision A (August 2019)	Page
• Deleted "I <sub>CC</sub> " and "output" from "Continuous current through V <sub>CC</sub> or GND" row for clarity.....	4

## 5 Pin Configuration and Functions



**5-1. D or PW Package  
14-Pin SOIC or TSSOP  
Top View**



**5-2. BQA Package  
14-Pin WQFN  
Top View**

## Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V <sub>CC</sub>	14	—	Positive Supply

1. BQA Package only.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±35 mA
	Continuous current through V <sub>CC</sub> or GND			±70 mA
T <sub>J</sub>	Junction temperature <sup>(3)</sup>			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 2	±4000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise and fall rate			Unlimited	ns/V
T <sub>A</sub>	Ambient temperature	-40		125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74HCS86-Q1			UNIT
		PW (TSSOP)	D (SOIC)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	109.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89.0	111.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	77.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	25.2	45.5	20.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	94.1	89.1	77.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	56.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{T+}$	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7	3.15		
				6 V	2.1	4.2		
$V_{T-}$	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9	2.2		
				6 V	1.2	3.0		
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ )			2 V	0.2		1.0	V
				4.5 V	0.4	1.4		
				6 V	0.6	1.6		
$V_{OH}$	High-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2 V to 6 V	$V_{CC} - 0.1$	$V_{CC} - 0.002$		V
			$I_{OH} = -6 \text{ mA}$	4.5 V	4.0	4.3		
			$I_{OH} = -7.8 \text{ mA}$	6 V	5.4	5.75		
$V_{OL}$	Low-level output voltage	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2 V to 6 V		0.002	0.1	V
			$I_{OL} = 6 \text{ mA}$	4.5 V		0.18	0.30	
			$I_{OL} = 7.8 \text{ mA}$	6 V		0.22	0.33	
$I_I$	Input leakage current	$V_I = V_{CC}$ or 0		6 V		$\pm 100$	$\pm 1000$	nA
$I_{CC}$	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V		0.1	2	$\mu\text{A}$
$C_i$	Input capacitance			2 V to 6 V			5	pF
$C_{pd}$	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

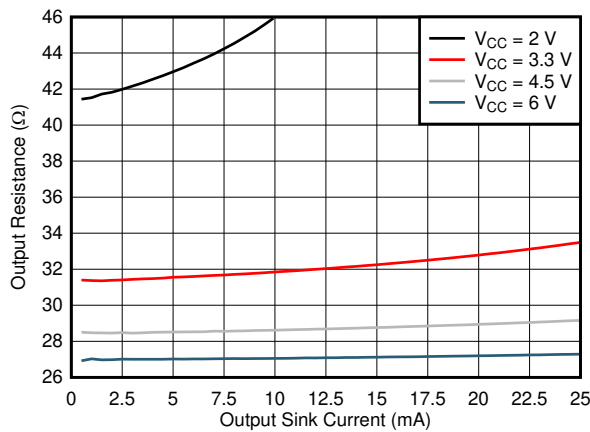
### 6.6 Switching Characteristics

$C_L = 50$  pF; over operating free-air temperature range; typical ratings measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted). See [Parameter Measurement Information](#).

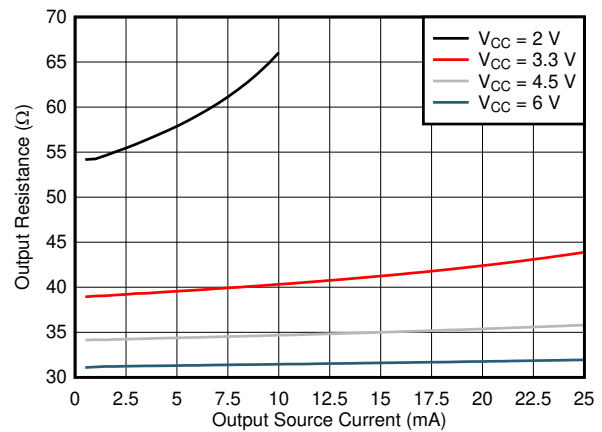
PARAMETER		FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	MIN	TYP	MAX	UNIT
$t_{pd}$	Propagation delay	A or B	Y	2 V		15	36	ns
				4.5 V		7	13	
				6 V		6	12	
$t_t$	Transition-time		Y	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

### 6.7 Typical Characteristics

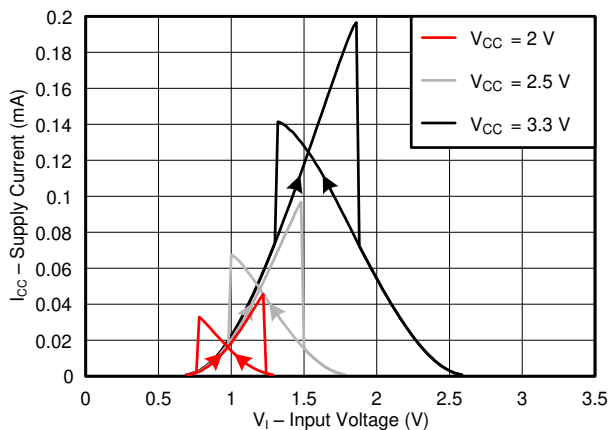
$T_A = 25^\circ\text{C}$



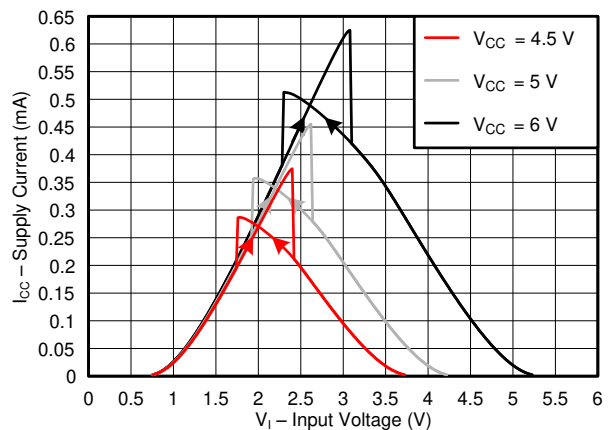
**6-1. Output driver resistance in LOW state.**



**6-2. Output driver resistance in HIGH state.**



**6-3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply**



**6-4. Supply current across input voltage, 4.5-, 5-, and 6-V supply**

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 2.5 \text{ ns}$ .

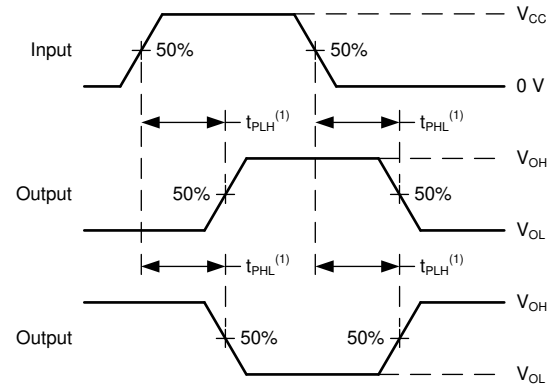
For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



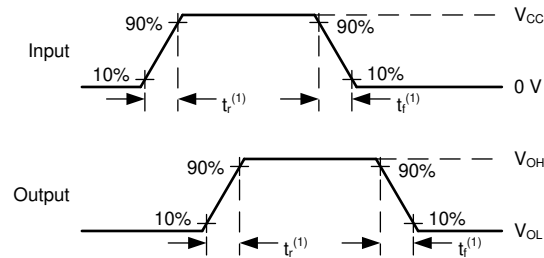
(1)  $C_L$  includes probe and test-fixture capacitance.

### 7-1. Load Circuit for Push-Pull Outputs



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

### 7-2. Voltage Waveforms Propagation Delays



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

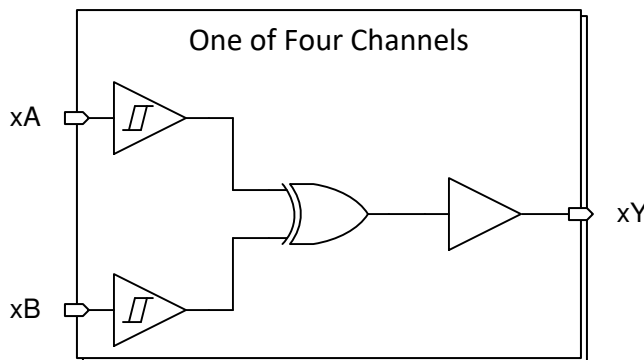
### 7-3. Voltage Waveforms, Input and Output Transition Times

## 8 Detailed Description

### 8.1 Overview

This device contains four independent 2-input XOR Gates with Schmitt-trigger inputs. Each gate performs the Boolean function  $Y = A \oplus B$  in positive logic.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

#### 8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ( $R = V \div I$ ).

The Schmitt-trigger input architecture provides hysteresis as defined by  $\Delta V_T$  in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

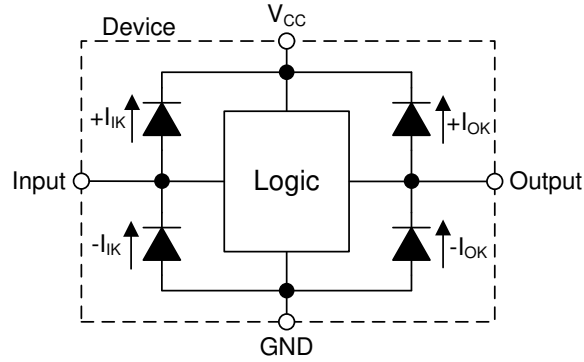
#### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Electrical Placement of Clamping Diodes for Each Input and Output](#).

#### 注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.






**8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.4 Device Functional Modes

Function Table lists the functional modes of the SN74HCS86-Q1.

**表 8-1. Function Table**

INPUTS <sup>(1)</sup>		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

(1) H = High Voltage Level, L = Low Voltage Level

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

In this application, a 2-input XOR gate is used as a phase difference detector as shown in [Typical application block diagram](#). The remaining three gates can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

The SN74HCS86-Q1 is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

Typically, clock signals have fast transition rates, but additional filtering can be added to the clock signals which can lead to slower transitions rates. This makes the SN74HCS86-Q1 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

### 9.2 Typical Application

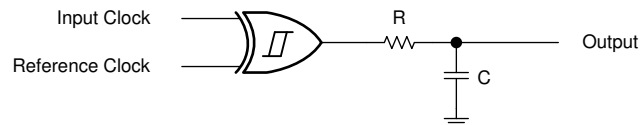


图 9-1. Typical application block diagram

#### 9.2.1 Design Requirements

##### 9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS86-Q1 plus the maximum static supply current,  $I_{CC}$ , listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS86-Q1 plus the maximum supply current,  $I_{CC}$ , listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS86-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS86-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### 注意

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.1.2 Input Considerations

Input signals must cross  $V_{t-(min)}$  to be considered a logic LOW, and  $V_{t+(max)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS86-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74HCS86-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the  $\Delta V_{T(min)}$  in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than  $V_{CC}$  or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

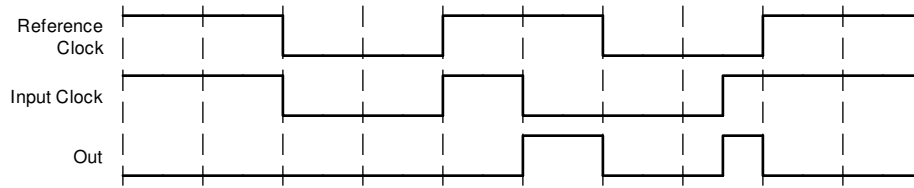
Refer to *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS86-Q1 to the receiving device(s).
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.2.3 Application Curves



☒ 9-2. Application timing diagram

## 10 Power Supply Recommendations

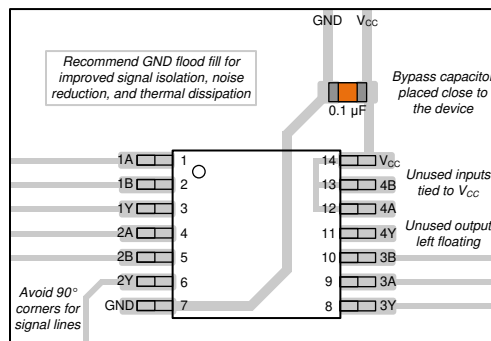
The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example



✎ 11-1. Example layout for the SN74HCS86-Q1

## 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [HCMOS Design Considerations application report \(SCLA007\)](#)
- Texas Instruments, [CMOS Power Consumption and  \$C\_{pd}\$  Calculation application report \(SDYA009\)](#)
- Texas Instruments, [Designing With Logic application report](#)

### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 12.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.6 用語集

TI 用語集 この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS86QBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS86Q	<a href="#">Samples</a>
SN74HCS86QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS86Q1	<a href="#">Samples</a>
SN74HCS86QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS86Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74HCS86-Q1 :**

- Catalog : [SN74HCS86](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS86QBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74HCS86QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS86QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS86QBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74HCS86QDRQ1	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCS86QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**BQA 14**

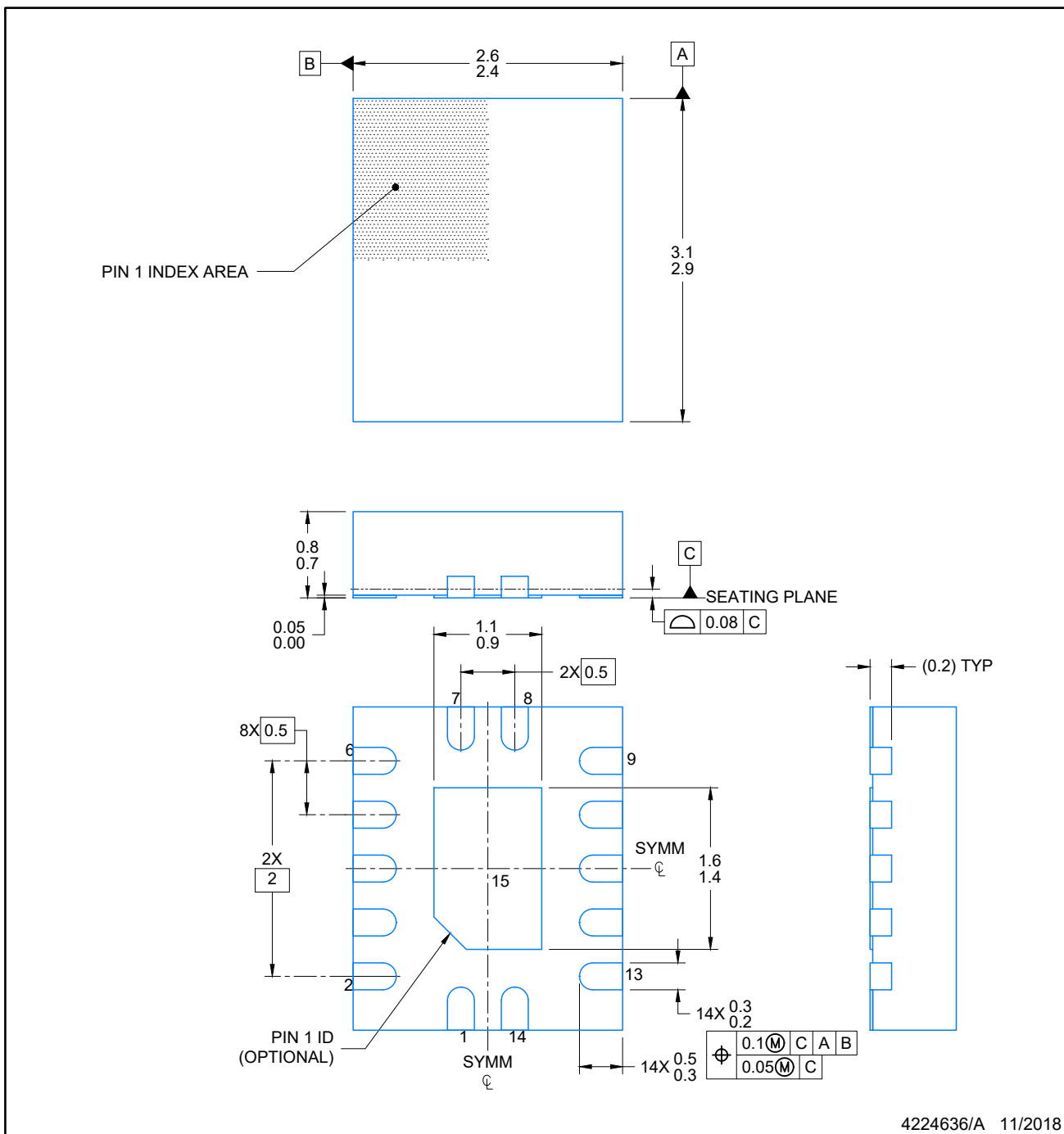
**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



# EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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