

## SN74CBTLV3126 低電圧クワッド FET バス・スイッチ

### 1 特長

- 標準の 126 タイプのピン配置
- 2 つのポート間を  $5\Omega$  スイッチで接続
- データ I/O ポートのレール・ツー・レール・スイッチング
- $I_{off}$  により部分的パワーダウン・モードでの動作をサポート
- JESD 78, Class II 準拠で 100mA 超のラッチアップ性能

### 2 アプリケーション

- データセンターおよびエンタープライズ・コンピューティング
- ブロードバンド固定回線アクセス
- ビル・オートメーション
- 有線ネットワーク
- モーター・ドライブ

### 3 概要

SN74CBTLV3126 クワッド FET バス・スイッチには、独立のライン・スイッチが搭載されています。各スイッチは、対応する出力イネーブル (OE) 入力が LOW のときディセーブルになります。

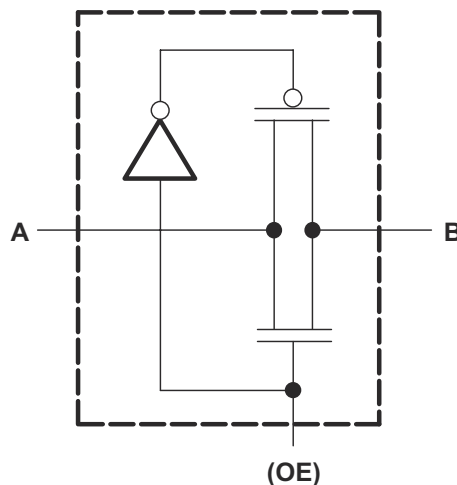
このデバイスは、 $I_{off}$  を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。 $I_{off}$  機能により、電源オフ時に損傷を引き起こすような電流がデバイスに逆流しないことが保証されます。SN74CBTLV3126 デバイスは、電源オフ時には絶縁されます。

電源オンまたは電源オフ時に高インピーダンス状態を保証するため、OE はプルダウン抵抗経路で GND に接続します。この抵抗の最小値は、ドライバの電流シンク能力によって決定されます。

#### パッケージ情報<sup>(1)</sup>

部品番号	パッケージ	本体サイズ (公称)
SN74CBTLV3126	SOIC (D) (14)	8.65mm × 3.91mm
	TVSOP (DGV) (14)	3.60mm × 4.40mm
	TSSOP (PW) (14)	5.00mm × 4.40mm
	VQFN (RGY) (14)	4.00mm × 3.50mm
	SSOP (DBQ) (16)	4.90mm × 3.90mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



概略回路図、各 FET スイッチ



## Table of Contents

1 特長.....	1	8.4 Device Functional Modes.....	8
2 アプリケーション.....	1	<b>9 Application and Implementation.....</b>	<b>10</b>
3 概要.....	1	9.1 Application Information.....	10
<b>4 Revision History.....</b>	<b>2</b>	9.2 Typical Application.....	10
<b>5 Pin Configuration and Functions.....</b>	<b>3</b>	<b>10 Power Supply Recommendations.....</b>	<b>11</b>
<b>6 Specifications.....</b>	<b>5</b>	<b>11 Layout.....</b>	<b>11</b>
6.1 Absolute Maximum Ratings.....	5	11.1 Layout Guidelines.....	11
6.2 ESD Ratings.....	5	11.2 Layout Example.....	12
6.3 Recommended Operating Conditions.....	5	<b>12 Device and Documentation Support.....</b>	<b>13</b>
6.4 Thermal Information.....	5	12.1 Receiving Notification of Documentation Updates..	13
6.5 Electrical Characteristics.....	6	12.2 サポート・リソース.....	13
6.6 Switching Characteristics.....	6	12.3 Trademarks.....	13
<b>7 Parameter Measurement Information.....</b>	<b>7</b>	12.4 Electrostatic Discharge Caution.....	13
<b>8 Detailed Description.....</b>	<b>8</b>	12.5 Glossary.....	13
8.1 Overview.....	8	<b>13 Mechanical, Packaging, and Orderable</b>	
8.2 Functional Block Diagram.....	8	<b>Information.....</b>	<b>13</b>
8.3 Feature Description.....	8		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision K (June 2021) to Revision L (August 2022)	Page
• Updated the <i>Overview</i> section.....	8
Changes from Revision J (January 2019) to Revision K (June 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Changed <i>active low</i> to <i>active high</i> in the <i>Pin Configurations and Functions</i> section to reflect logic description change.....	3
Changes from Revision I (October 2003) to Revision J (January 2019)	Page
• 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• Added $V_{IH}$ MAX values in the <i>Recommended Operating Conditions</i> table.....	5

## 5 Pin Configuration and Functions

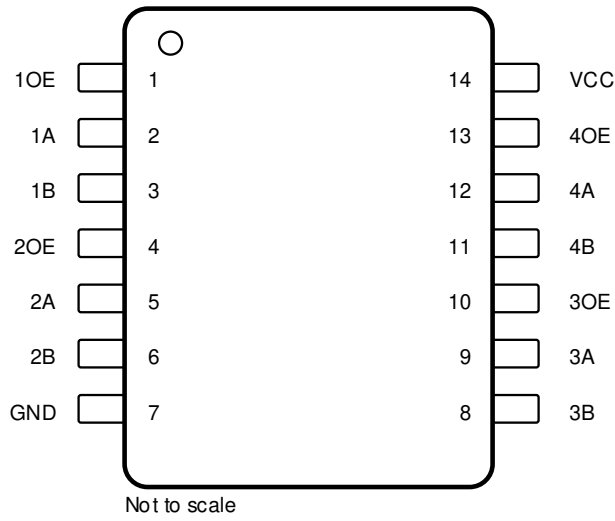


图 5-1. D, DGV, and PW Package, 14 Pin SOIC, TVSOP, and TSSOP (Top View)

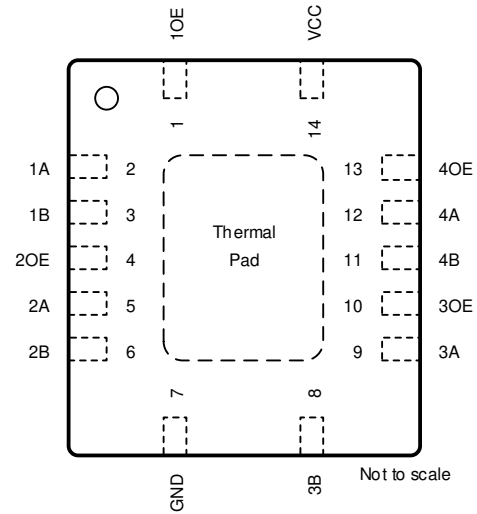


图 5-2. RGY Package, 14 Pin VQFN (Top View)

表 5-1. Pin Functions, D, DGV, PW, RGY

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	2	I/O	Channel 1 input or output
1B	3	I/O	Channel 1 input or output
1OE	1	I	Output enable, active high
2A	5	I/O	Channel 2 input or output
2B	6	I/O	Channel 2 input or output
2OE	4	I	Output enable, active high
3A	9	I/O	Channel 3 input or output
3B	8	I/O	Channel 3 input or output
3OE	10	I	Output enable, active high
4A	12	I/O	Channel 4 input or output
4B	11	I/O	Channel 4 input or output
4OE	13	I	Output enable, active high
GND	7	—	Ground
V <sub>CC</sub>	14	P	Power supply
Thermal Pad		—	Exposed thermal pad. There is no requirement to solder this pad; if connected, it should be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power

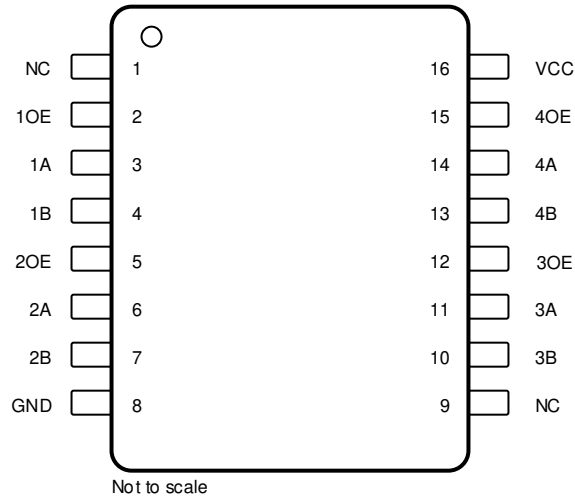


图 5-3. DBQ Package, 16 Pin SSOP (Top View)

表 5-2. Pin Functions, DBQ

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	3	I/O	Channel 1 input or output
1B	4	I/O	Channel 1 input or output
1OE	2	I	Output enable, active high
2A	6	I/O	Channel 2 input or output
2B	7	I/O	Channel 2 input or output
2OE	5	I	Output enable, active high
3A	11	I/O	Channel 3 input or output
3B	10	I/O	Channel 3 input or output
3OE	12	I	Output enable, active high
4A	14	I/O	Channel 4 input or output
4B	13	I/O	Channel 4 input or output
4OE	15	I	Output enable, active high
GND	8	—	Ground
NC	9	—	No internal connection
V <sub>CC</sub>	16	P	Power supply

(1) I = input, O = output, I/O = input and output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
I <sub>I/O</sub>	Continuous channel current		128	mA
I <sub>IK</sub>	Input clamp current	V <sub>I/O</sub> < 0	-50	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	V <sub>CC</sub>
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	V <sub>CC</sub>
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74CBTLV3126					UNIT
		D (SOIC)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	DBQ (SSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	16 Pins	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	100.6	154.8	123.3	59.6	118.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	55.5	64.5	53.0	71.3	66.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	56.8	88.4	66.3	35.6	62.2	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	17.0	11.1	9.3	4.2	20.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	56.4	87.4	65.7	35.7	61.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	16.1	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	$V_{CC} = 3\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$I_I$	$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}$ or GND			$\pm 1$	$\mu\text{A}$
$I_{off}$	$V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 3.6 V			10	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ ,	$I_O = 0$ , $V_I = V_{CC}$ or GND			10	$\mu\text{A}$
$\Delta I_{CC}$ <sup>(2)</sup>	Control inputs $V_{CC} = 3.6\text{ V}$ ,	One input at 3 V, Other inputs at $V_{CC}$ or GND			300	$\mu\text{A}$
$C_i$	Control inputs $V_I = 3\text{ V}$ or 0			2.5		pF
$C_{io(OFF)}$	$V_O = 3\text{ V}$ or 0, OE = GND			7		pF
$r_{on}$ <sup>(3)</sup>	$V_{CC} = 2.3\text{ V}$ , TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	8	$\Omega$
			$I_I = 24\text{ mA}$	5	8	
		$V_I = 1.7\text{ V}$ ,	$I_I = 15\text{ mA}$	27	40	
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	7	
			$I_I = 24\text{ mA}$	5	7	
		$V_I = 2.4\text{ V}$ ,	$I_I = 15\text{ mA}$	10	15	

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(2) This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

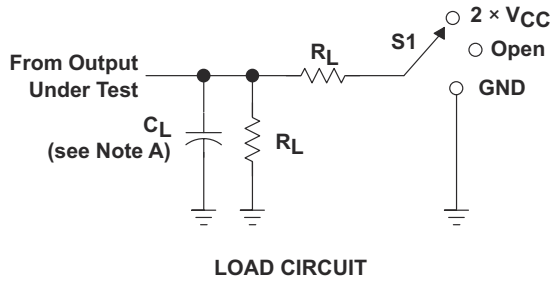
## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$ <sup>(1)</sup>	A or B	B or A		0.15		0.25	ns
$t_{en}$	OE	A or B	1.6	4.5	1.9	4.2	ns
$t_{dis}$	OE	A or B	1.3	4.7	1	4.8	ns

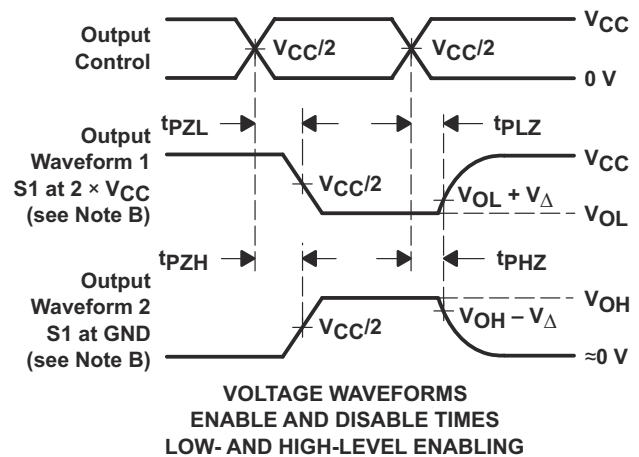
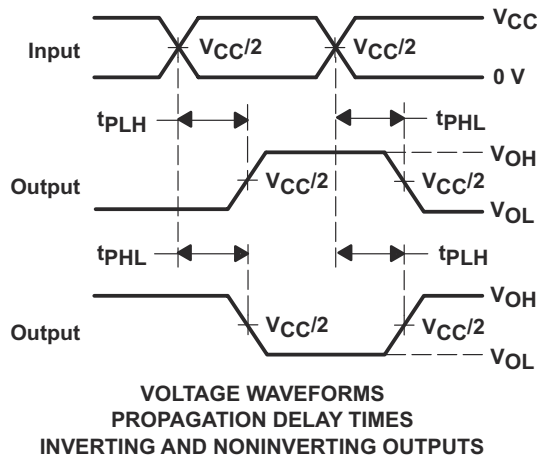
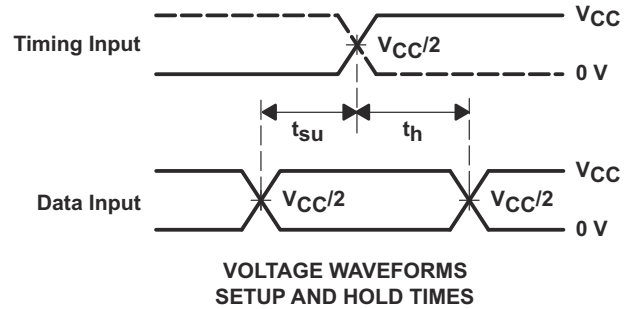
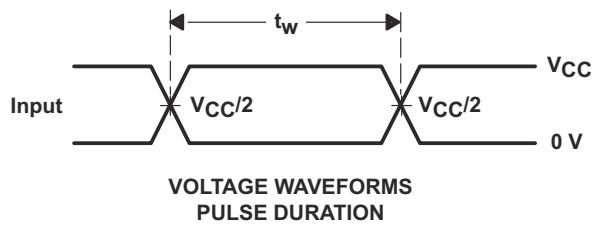
(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## 7 Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 $\Omega$	0.3 V



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

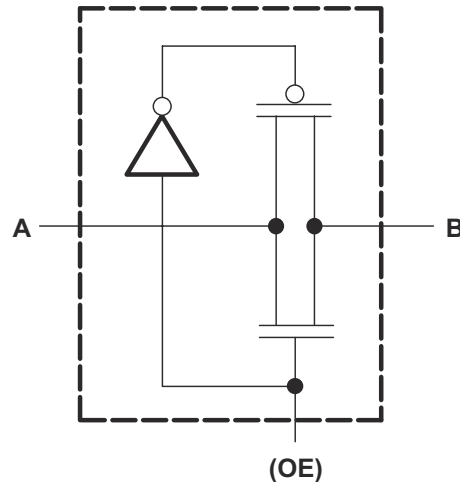
7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low. This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CBTLV3126 device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The SN74CBTLV3126 features 5- $\Omega$  switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs.  $I_{off}$  supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on. Latch-up performance exceeds 100 mA per JESD 78, Class II.

### 8.4 Device Functional Modes

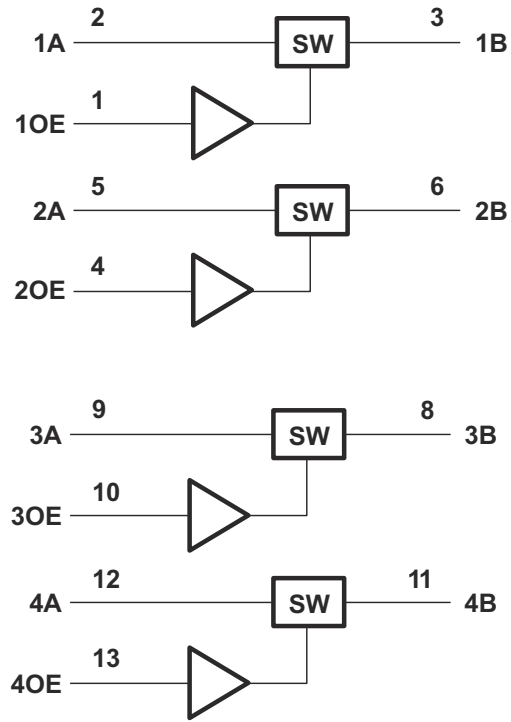
#### 8.4.1 Function Table (Each Bus Switch)

表 8-1 provides the truth table for the SN74CBTLV3126.

表 8-1. Truth Table

INPUT OE	FUNCTION
L	Disconnect
H	A port = B port





8-1. Logic Diagram (Positive Logic)

## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

One useful application to take advantage of the SN74CBTLV3126 features is isolating various protocols from a processor or MCU such as JTAG, SPI, or standard GPIO signals. The device provides excellent isolation performance when the device is powered. The added benefit of powered-off protection allows a system to minimize complexity by eliminating the need for power sequencing in hot-swap and live insertion applications.

### 9.2 Typical Application

#### 9.2.1 Protocol and Signal Isolation

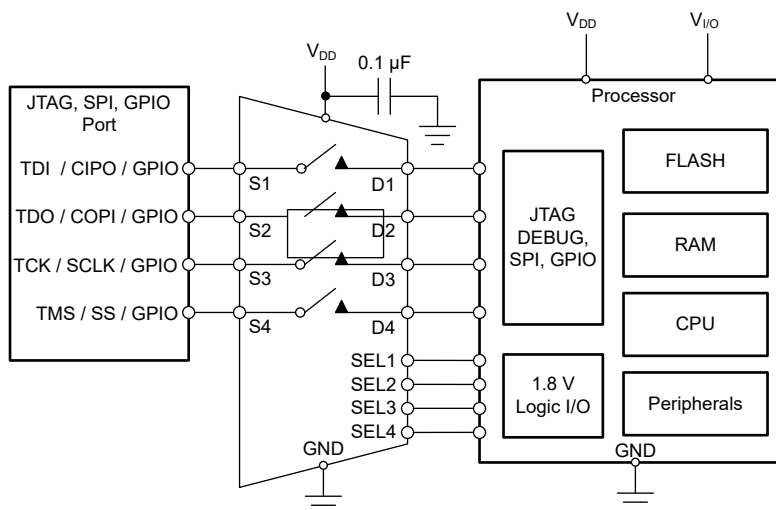


図 9-1. Typical Application

#### 9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Supply ( $V_{DD}$ )	3.3 V
Input or output signal range	0 V to 3.3 V
Control logic thresholds	1.8 V compatible

### 9.2.1.2 Detailed Design Procedure

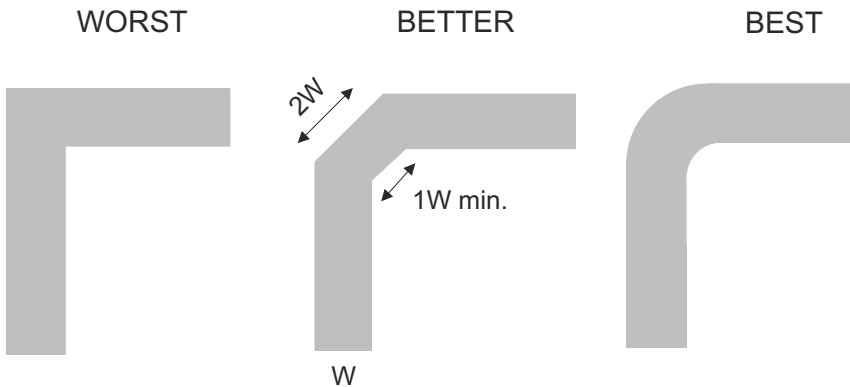
The SN74CBTLV3126 can operate without any external components except for the supply decoupling capacitors. TI recommends that the digital control pins (OE) be pulled up to  $V_{CC}$  or down to GND to avoid an undesired switch state that could result from the floating pin. All input signals passing through the switch must fall within the *Recommend Operating Conditions* of the SN74CBTLV3126 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. This example can also utilize the Powered-off Protection feature, and the inputs can range from 0 V to 3.3 V when  $V_{DD} = 0$  V.

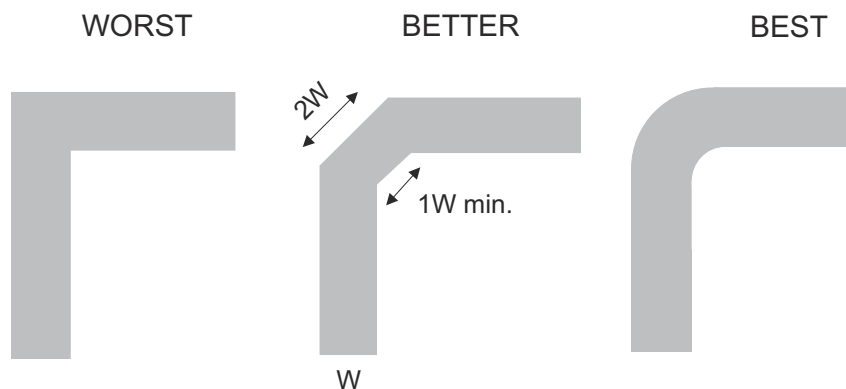
## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu$ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight, and therefore; some traces must turn corners.  11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.



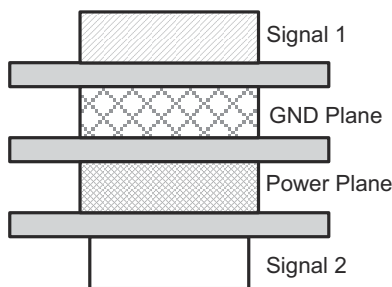
 11-1. Trace Example

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

- Avoid stubs on the high-speed signals traces because they cause signal reflections.
- Route all high-speed signal traces over continuous GND planes, with no interruptions.
- Avoid crossing over anti-etch, commonly found with plane splits.

- When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [Figure 11-2](#).



**Figure 11-2. Example Layout**

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

[Figure 11-3](#) shows an example of a PCB layout with the SN74CBTLV3126. Some key considerations are:

Decouple the  $V_{DD}$  pin with a 0.1- $\mu\text{F}$  capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the  $V_{DD}$  supply.

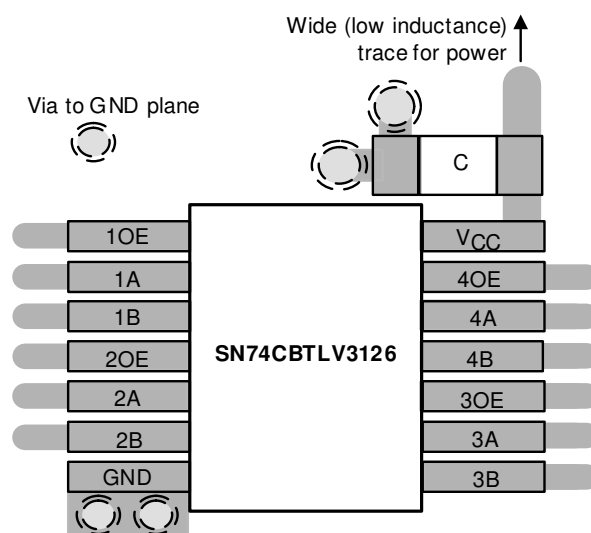
High-speed switches require proper layout and design procedures for optimum performance.

Keep the input lines as short as possible.

Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

## 11.2 Layout Example



**Figure 11-3. Example Layout**

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTLV3126D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	CBTLV3126	
SN74CBTLV3126DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126	Samples
SN74CBTLV3126DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126	Samples
SN74CBTLV3126DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126	Samples
SN74CBTLV3126PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	CL126	
SN74CBTLV3126PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126	Samples
SN74CBTLV3126RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3126DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3126RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3126DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CBTLV3126DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74CBTLV3126DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74CBTLV3126PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74CBTLV3126RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

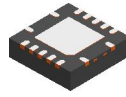
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A

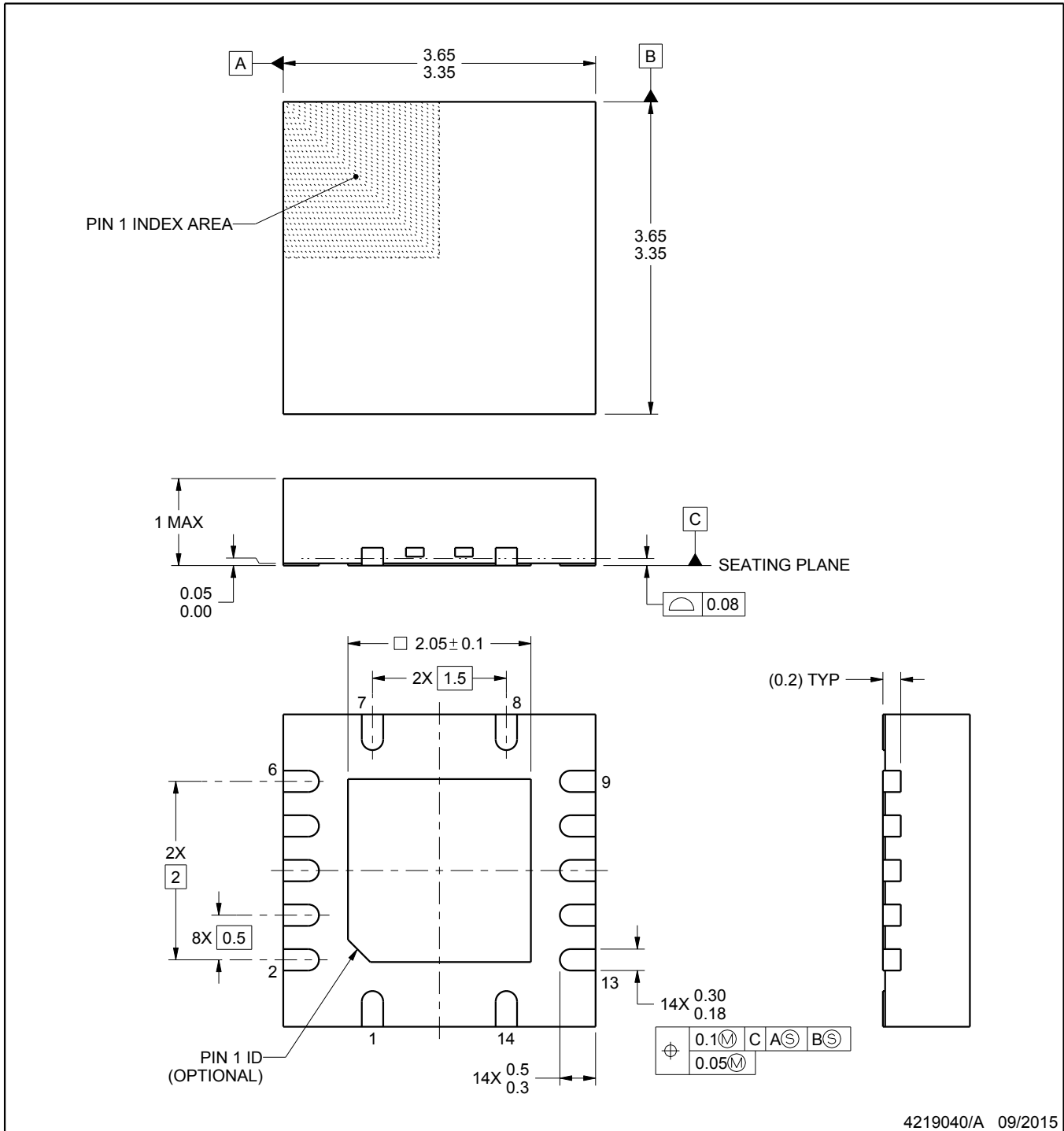
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

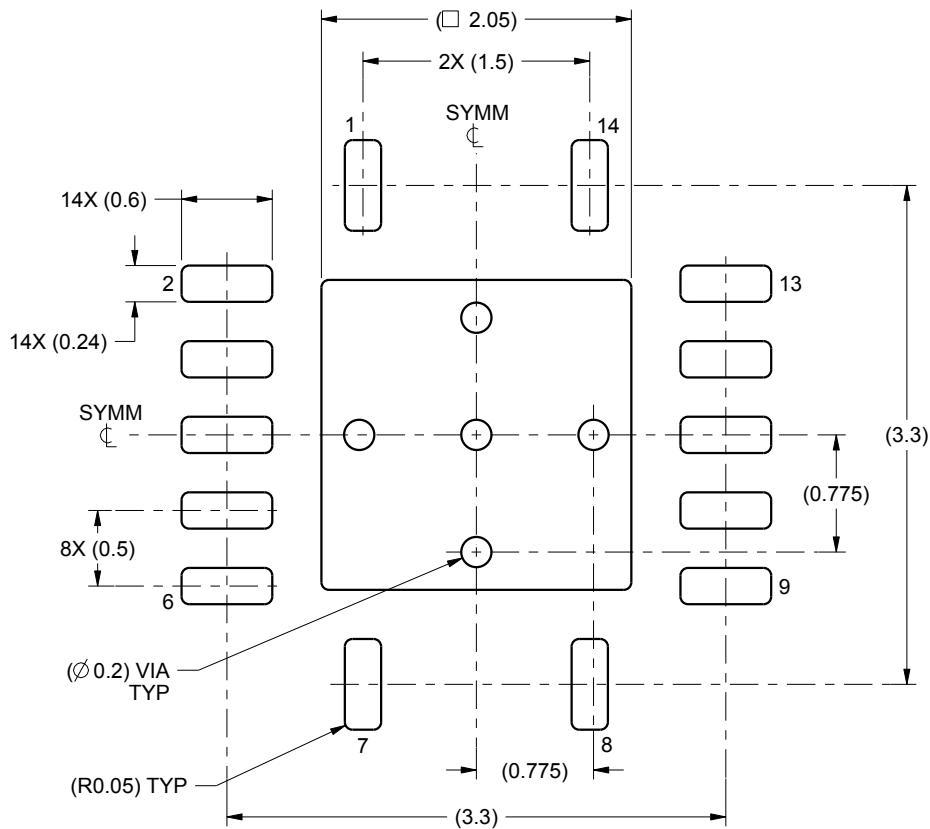
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

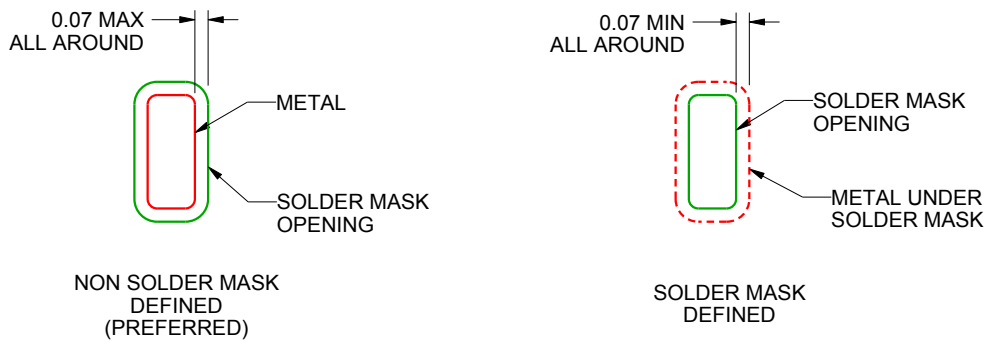
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

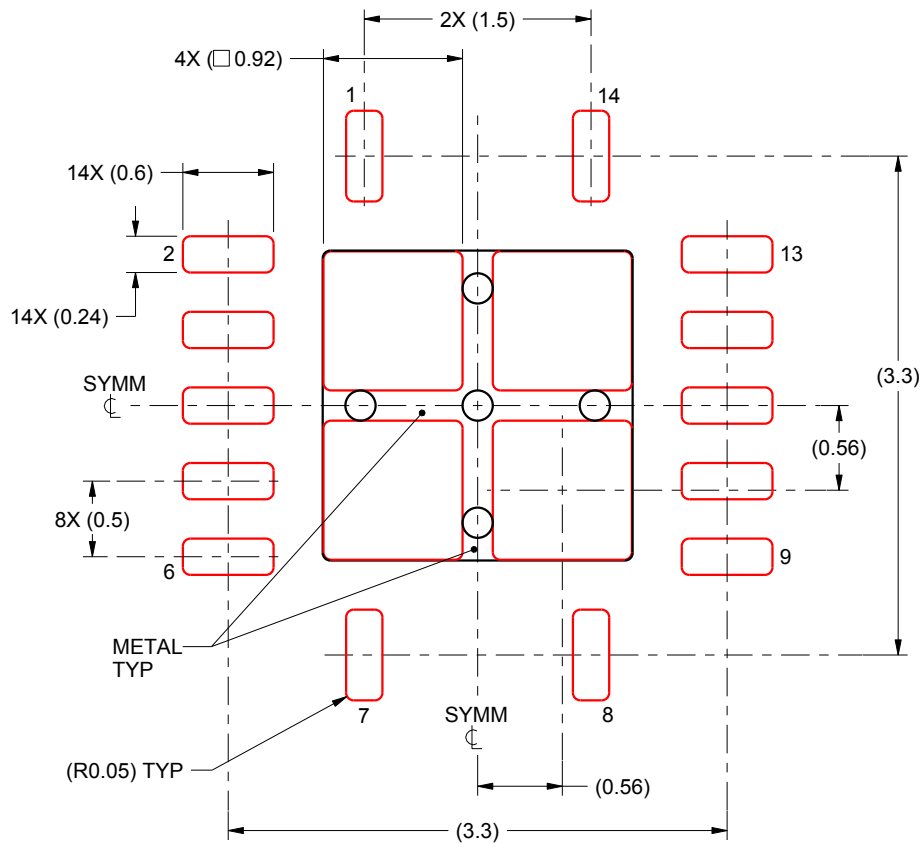
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

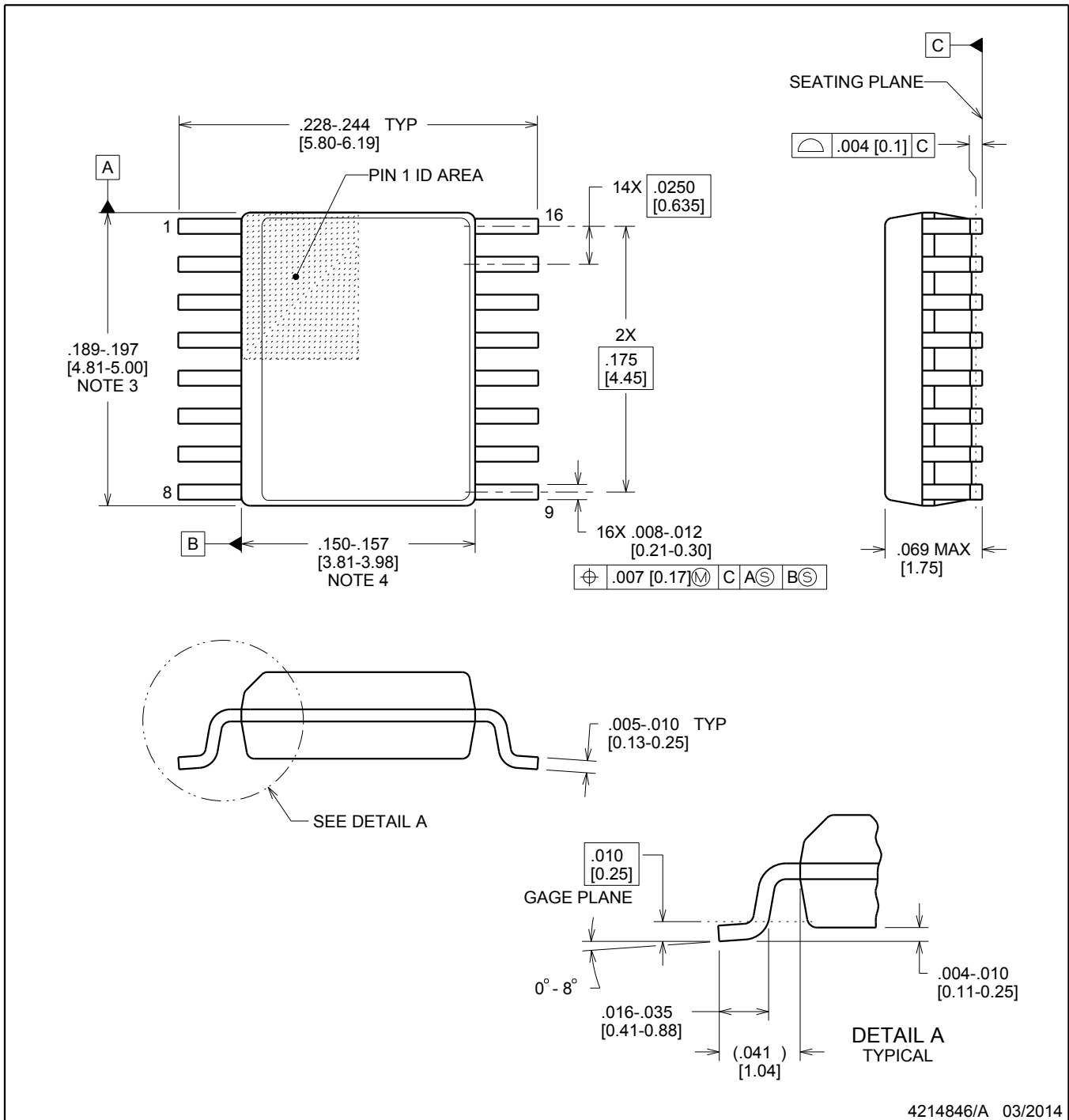


# PACKAGE OUTLINE

## DBQ0016A

### SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



#### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、ます。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated