

SN74CB3T3245 2.5Vおよび3.3V、低電圧、8ビットFETバス・スイッチ、5V許容のレベル・シフト搭載

1 特長

- 標準の245タイプのピン配置
- 出力電圧変換は V_{CC} に追従
- すべてのデータI/Oポートで混在モード信号動作をサポート
 - 3.3V V_{CC} により、5V入力を3.3V出力にレベル・シフト
 - 2.5V V_{CC} により、5V/3.3V入力を2.5V出力にレベル・シフト
- デバイスの電源オン時とオフ時の両方で5V許容のI/O
- 伝播遅延がゼロに近い双方向データ・フロー
- 低いオン抵抗(r_{on})特性($r_{on} = 5\Omega$: 標準値)
- 低い入力/出力容量により負荷が最小化($C_{io(OFF)} = 5pF$: 標準値)
- データおよび制御入力にアンダーシュート・クランプ・ダイオードを搭載
- 低い消費電力($I_{CC} = 40\mu A$: 最大値)
- 2.3V~3.6Vの範囲の V_{CC} で動作
- データI/Oは0~5Vの信号レベルに対応 (0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V)
- 制御入力をTTLまたは5V/3.3V CMOS出力で駆動可能
- I_{off} により部分的パワーダウン・モード動作をサポート

- JESD 17準拠で250mA超のラッチアップ性能
- ESD性能はJESD 22に準拠シテスト済み
 - 人体モデルで2000V (A114-B、クラス II)
 - 荷電デバイス・モデルで1000V (C101)
- 低消費電力の携帯用機器に理想的

2 アプリケーション

- デジタル・アプリケーションをサポート: レベル変換、PCIインターフェイス、USBインターフェイス、メモリ・インターリーピング、バス絶縁

3 概要

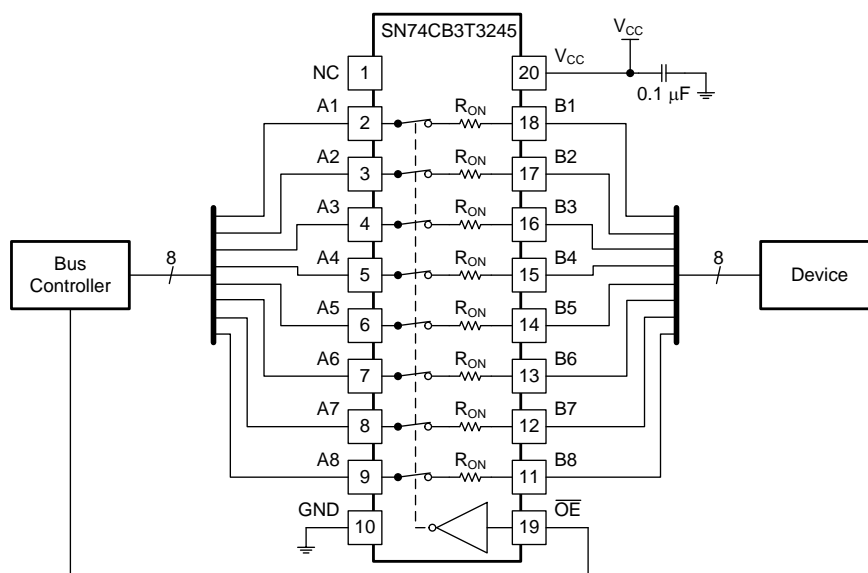
SN74CB3T3245デバイスは高速のTTL互換8ビットFETバス・スイッチで、オン抵抗(r_{on})が低く、伝播遅延が最小限です。このデバイスは、 V_{CC} に追従した電圧変換を行うことで、すべてのデータI/Oポートにおいて混在モード信号動作を完全にサポートします。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
SN74CB3T3245DBQ	SSOP (20)	8.65mm×3.90mm
SN74CB3T3245DGV	TVSOP (20)	5.00mm×4.40mm
SN74CB3T3245DW	SOIC (20)	12.80mm×7.50mm
SN74CB3T3245PW	TSSOP (20)	6.50mm×4.40mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーションの機能図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

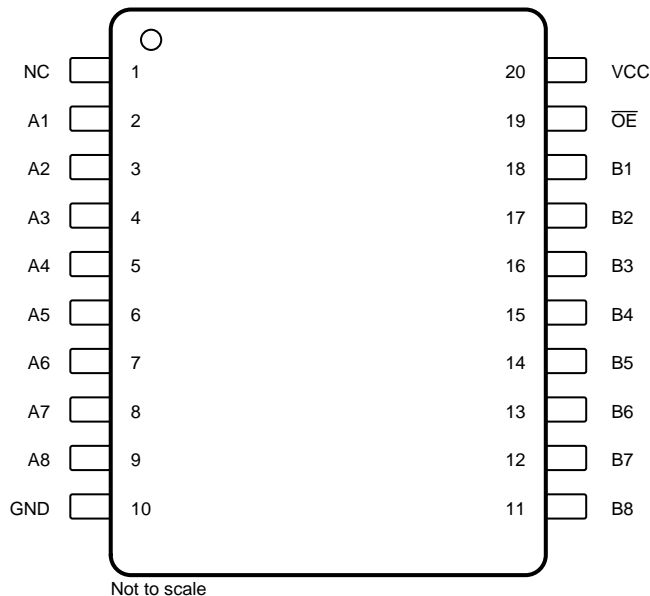
Revision B (June 2015) から Revision C に変更	Page
• Changed the pin out image appearance	3
• Changed $I_O = 1\text{ mA}$ To: $I_O = 1\text{ }\mu\text{A}$ in Figure 9 and Figure 10	11

Revision A (August 2012) から Revision B に変更	Page
• 「アプリケーション」セクション、「製品情報」表、「ピン構成および機能」セクション、「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 「注文情報」表を削除	1

2005年3月発行のものから更新	Page
• Updated graphic note and picture in Figure 1 .	8

5 Pin Configuration and Functions

**DBQ, DGV, DW, and PW Package
20-Pin SSOP, TVSOP, SOIC, TSSOP
Top View**



NC — No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC	—	Not internally connected
2	A1	I/O	Switch 1 A terminal
3	A2	I/O	Switch 2 A terminal
4	A3	I/O	Switch 3 A terminal
5	A4	I/O	Switch 4 A terminal
6	A5	I/O	Switch 5 A terminal
7	A6	I/O	Switch 6 A terminal
8	A7	I/O	Switch 7 A terminal
9	A8	I/O	Switch 8 A terminal
10	GND	—	Ground
11	B8	I/O	Switch 8 B terminal
12	B7	I/O	Switch 7 B terminal
13	B6	I/O	Switch 6 B terminal
14	B5	I/O	Switch 5 B terminal
15	B4	I/O	Switch 4 B terminal
16	B3	I/O	Switch 3 B terminal
17	B2	I/O	Switch 2 B terminal
18	B1	I/O	Switch 1 B terminal
19	\overline{OE}	I	Output enable, active low
20	V _{CC}	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾	-0.5	7	V
V _{IN}	Control input voltage ⁽²⁾⁽³⁾	-0.5	7	V
V _{I/O}	Switch I/O voltage ⁽²⁾⁽³⁾⁽⁴⁾	-0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		-50 mA
I _{I/O}	I/O port clamp current	V _{I/O} < 0		-50 mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±128 mA
Continuous current through V _{CC} or GND				±100 mA
T _J	Junction temperature			150 °C
T _{stg}	Storage temperature	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	5.5
		V _{CC} = 2.7 V to 3.6 V	2	5.5
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0	0.7
		V _{CC} = 2.7 V to 3.6 V	0	0.8
V _{I/O}	Data input/output voltage	0	5.5	V
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74CB3T3245				UNIT	
	DBQ (SSOP)	DGV (TVSOP)	DW (SOIC)	PW (TSSOP)		
	20 PINS	20 PINS	20 PINS	20 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	68	92	58	83	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT	
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V	
V_{OH}		See and Figure 1					
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_{IN} = 3.6\text{ V to } 5.5\text{ V or GND}$			± 10	μA	
I_I		$V_{CC} = 3.6\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7\text{ V to } 5.5\text{ V}$		± 20	μA	
			$V_I = 0.7\text{ V to } V_{CC} - 0.7\text{ V}$		-40		
			$V_I = 0\text{ to } 0.7\text{ V}$		± 5		
I_{OZ} ⁽³⁾		$V_{CC} = 3.6\text{ V}$, $V_O = 0\text{ to } 5.5\text{ V}$, $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND			± 10	μA	
I_{off}		$V_{CC} = 0$, $V_O = 0\text{ to } 5.5\text{ V}$, $V_I = 0$,			10	μA	
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND		40	μA	
			$V_I = 5.5\text{ V}$		40		
ΔI_{CC} ⁽⁴⁾	Control inputs	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND			300	μA	
C_{in}	Control inputs	$V_{CC} = 3.3\text{ V}$, $V_{IN} = V_{CC}$ or GND		4		pF	
$C_{iO(OFF)}$		$V_{CC} = 3.3\text{ V}$, $V_{I/O} = 5.5\text{ V}$, 3.3 V , or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND		5		pF	
$C_{iO(ON)}$		$V_{CC} = 3.3\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5\text{ V or } 3.3\text{ V}$		5	pF	
			$V_{I/O} = \text{GND}$		13		
r_{on} ⁽⁵⁾		$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$, $V_I = 0$	$I_O = 24\text{ mA}$		5	8.5	Ω
			$I_O = 16\text{ mA}$		5	8.5	
		$V_{CC} = 3\text{ V}$, $V_I = 0$	$I_O = 64\text{ mA}$		5	7	
			$I_O = 32\text{ mA}$		5	7	

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd} ⁽¹⁾	A or B	B or A		0.15		0.25	ns
t_{en}	\overline{OE}	A or B	1	10.5	1	8	ns
t_{dis}	\overline{OE}	A or B	1	5.5	1	7.5	ns

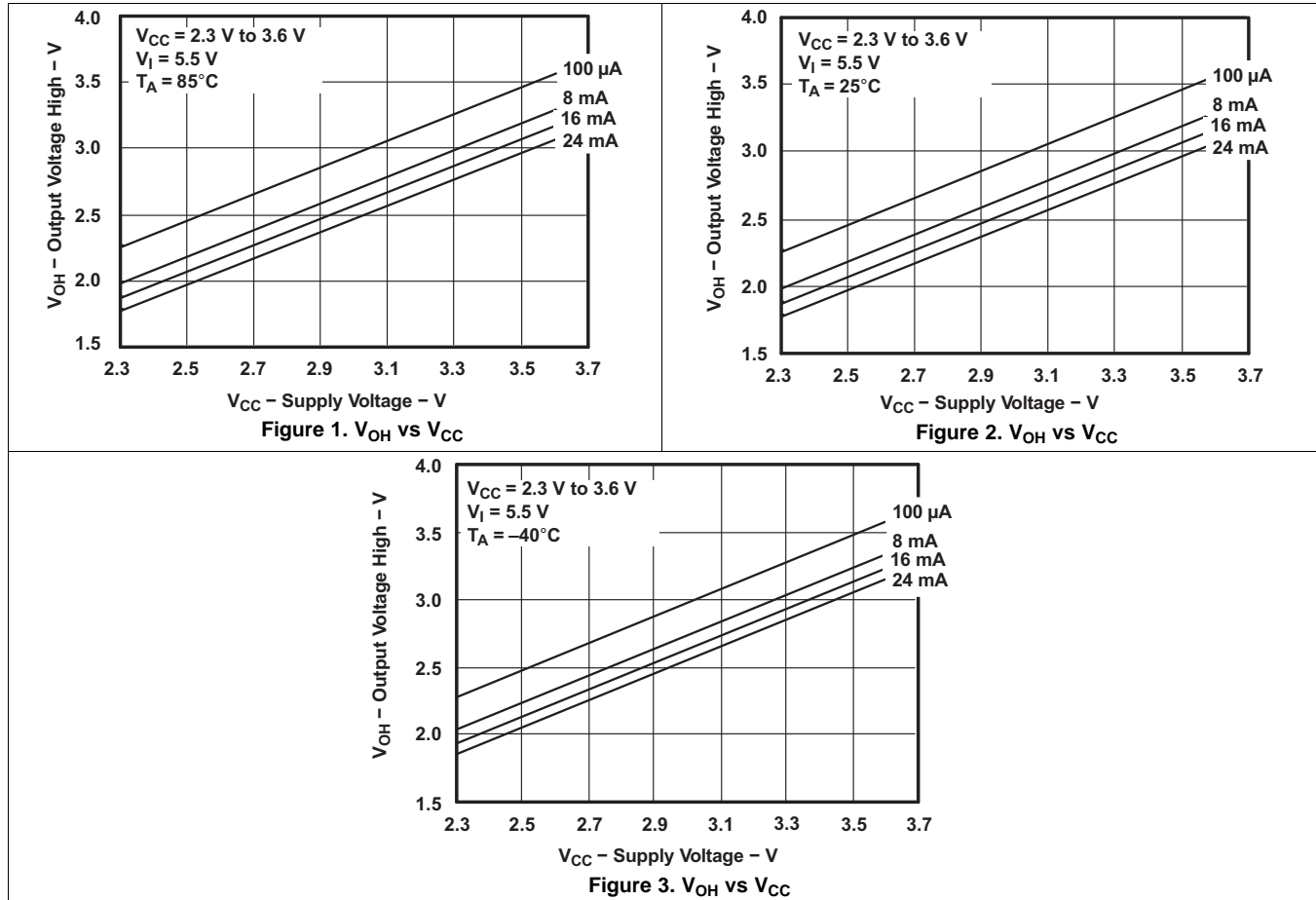
(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

SN74CB3T3245

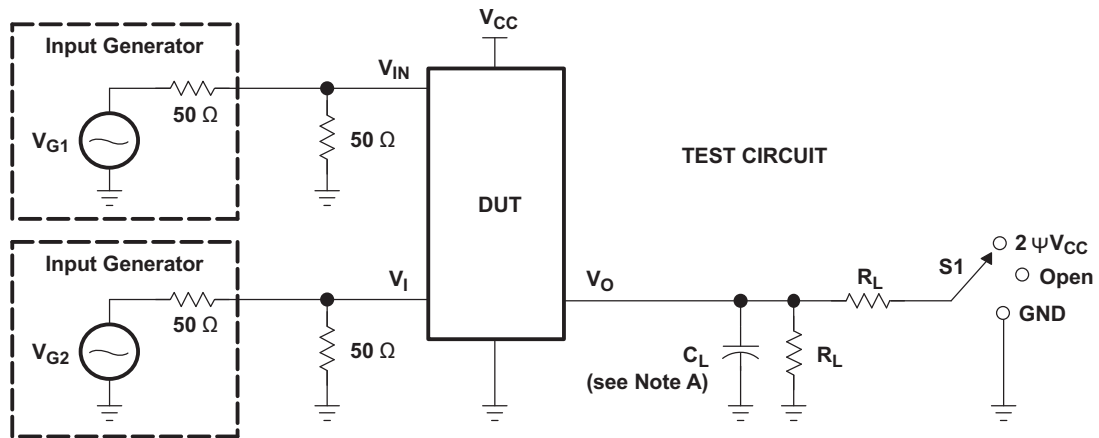
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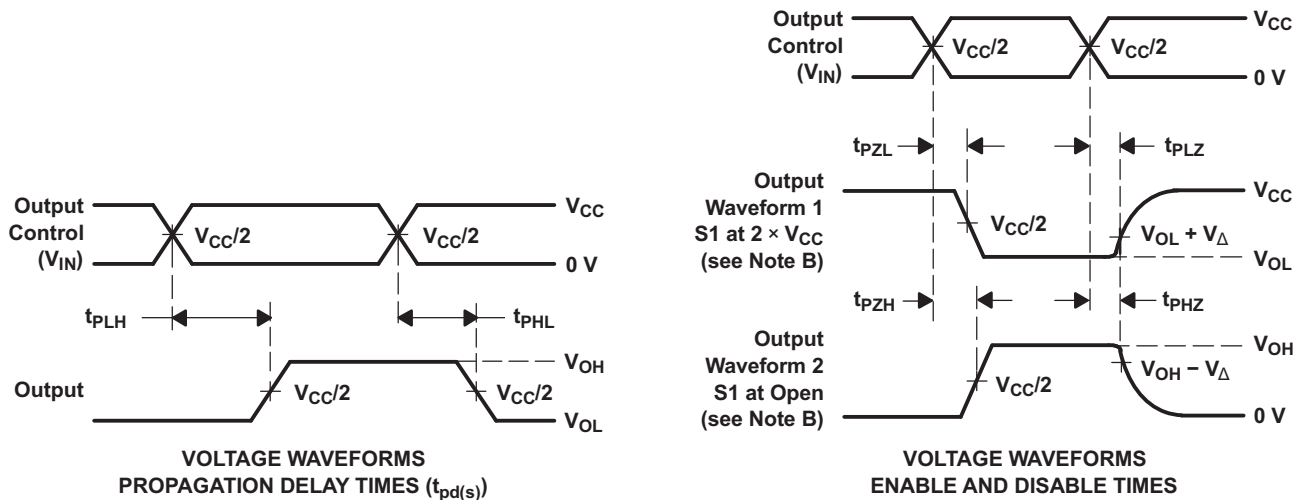
6.7 Typical Characteristics



7 Parameter Measurement Information



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V	Open	500 Ω	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × V _{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V _{CC}	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	Open	500 Ω	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V	50 pF	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - H. All parameters and waveforms are not applicable to all devices.

Figure 4. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

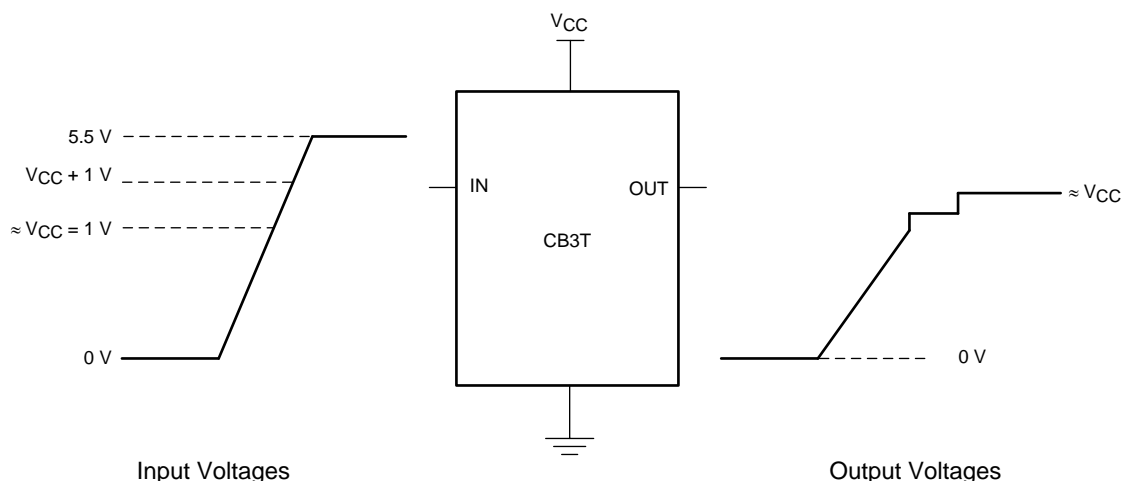
The SN74CB3T3245 device is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T3245 device supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 5).

The SN74CB3T3245 device is an 8-bit bus switch with a single output-enable (\overline{OE}) input and a standard '245 pinout. When \overline{OE} is low, the 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} + 1V$, and less than or equal to 5.5V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 5. Typical DC Voltage Translation Characteristics

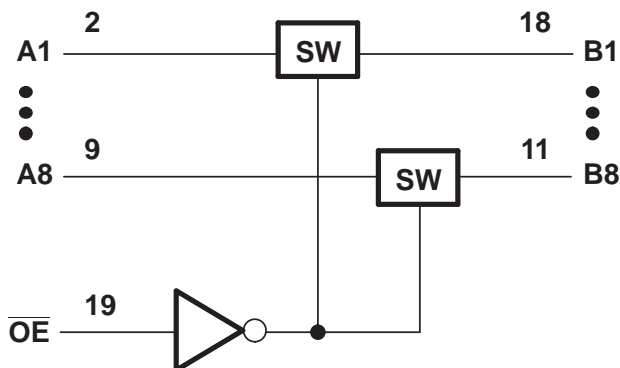
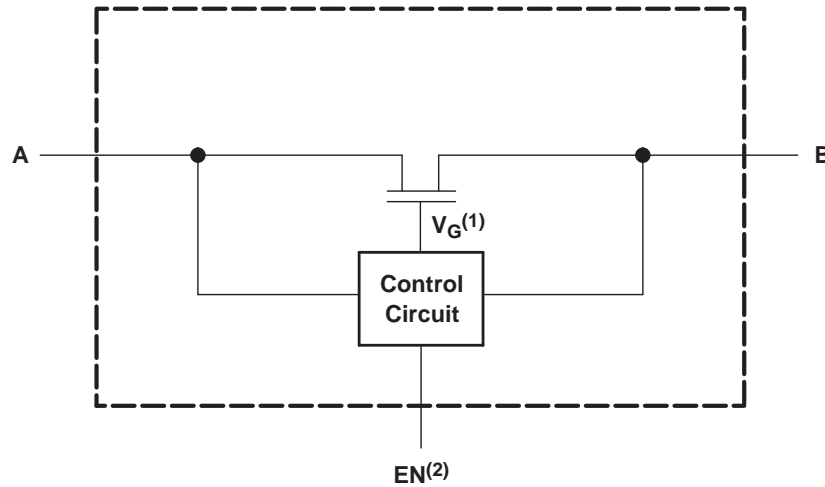


Figure 6. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



- 1) Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > (V_{CC} + V_T)$.
- 2) EN is the internal enable signal applied to the switch.

Figure 7. Simplified Schematic, Each FET Switch (SW)

8.3 Feature Description

The SN74CB3T3245 device uses the standard '245-type pinout. The output voltage tracks V_{CC} , allowing for easy down-translation. The device is ideal for low-power portable equipment.

Mixed-mode signal operation is supported on all data I/O ports. 5-V input down to 3.3-V output level shift with 3.3-V V_{CC} and 5-V/3.3-V input down to 2.5-V output level shift With 2.5-V V_{CC} are possible due to overvoltage tolerant inputs.

This part is friendly to partial power down systems. The I/Os are 5-V-tolerant with the device powered up or powered down and I_{off} supports partial-power-down mode operation

The SN74CB3T3245 has a bidirectional data flow with near-zero propagation delay.

The SN74CB3T3245 has low ON-state resistance (r_{on}) characteristics ($r_{on} = 5 \Omega$ Typical)

The SN74CB3T3245 has both low input and output capacitance minimizes loading ($C_{io(OFF)} = 5 \text{ pF}$ Typical)

Data and control inputs provide undershoot clamp diodes.

The SN74CB3T3245 has low power consumption ($I_{CC} = 40 \mu\text{A}$ Maximum)

The SN74CB3T3245 has a V_{CC} operating range from 2.3 V to 3.6 V.

The data I/Os support 0- to 5-V signaling levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)

Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74CB3T3245.

Table 1. Function Table

INPUT OE	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This application is specifically to connect a 5-V bus to a 3.3-V device. It is assumed that communication in this particular application is one-directional, going from the bus controller to the device.

9.2 Typical Application

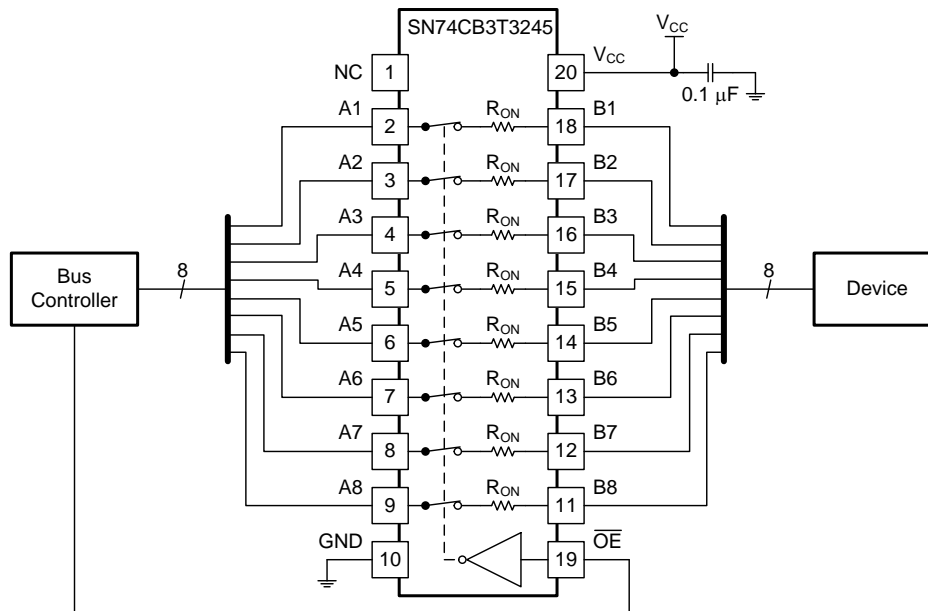


Figure 8. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

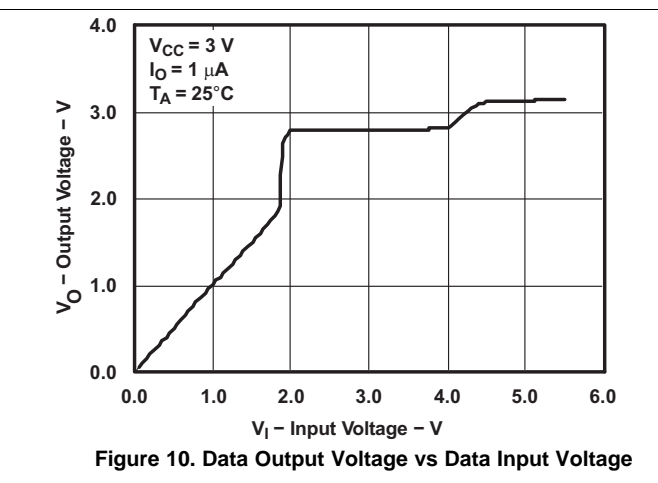
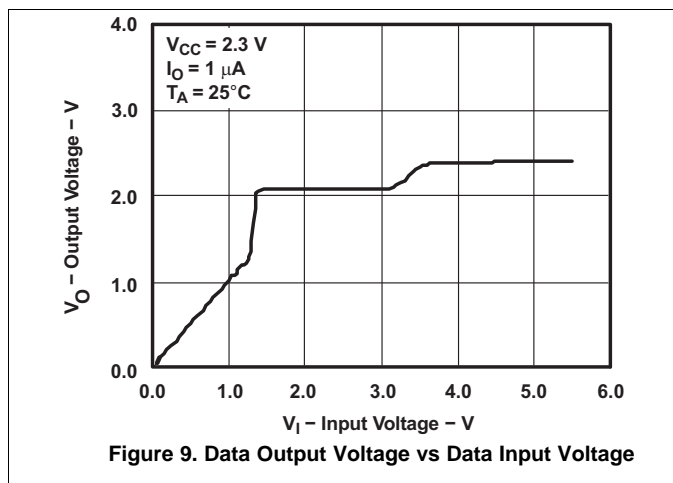
Because this design is for down-translating voltage, no pullup resistors are required.

9.2.2 Detailed Design Procedure

1. Recommended Input conditions
 - Specified high and low levels. See (V_{IH} and V_{IL}) in [Recommended Operating Conditions](#)
 - Inputs are overvoltage tolerant allowing them to go as high as 7 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 128 mA on each channel

Typical Application (continued)

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μF or 0.022- μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 11](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

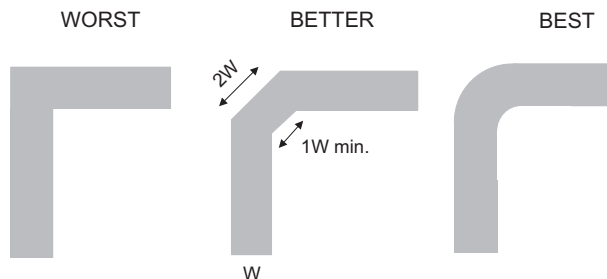


Figure 11. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

『低速またはフローティングCMOS入力の影響』、[SCBA004](#)

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer)* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.

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12.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3T3245DBQR	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245	Samples
SN74CB3T3245DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	KS245	
SN74CB3T3245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3T3245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74CB3T3245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	356.0	356.0	35.0
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74CB3T3245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74CB3T3245PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CB3T3245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CB3T3245DWG4	DW	SOIC	20	25	507	12.83	5080	6.6

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

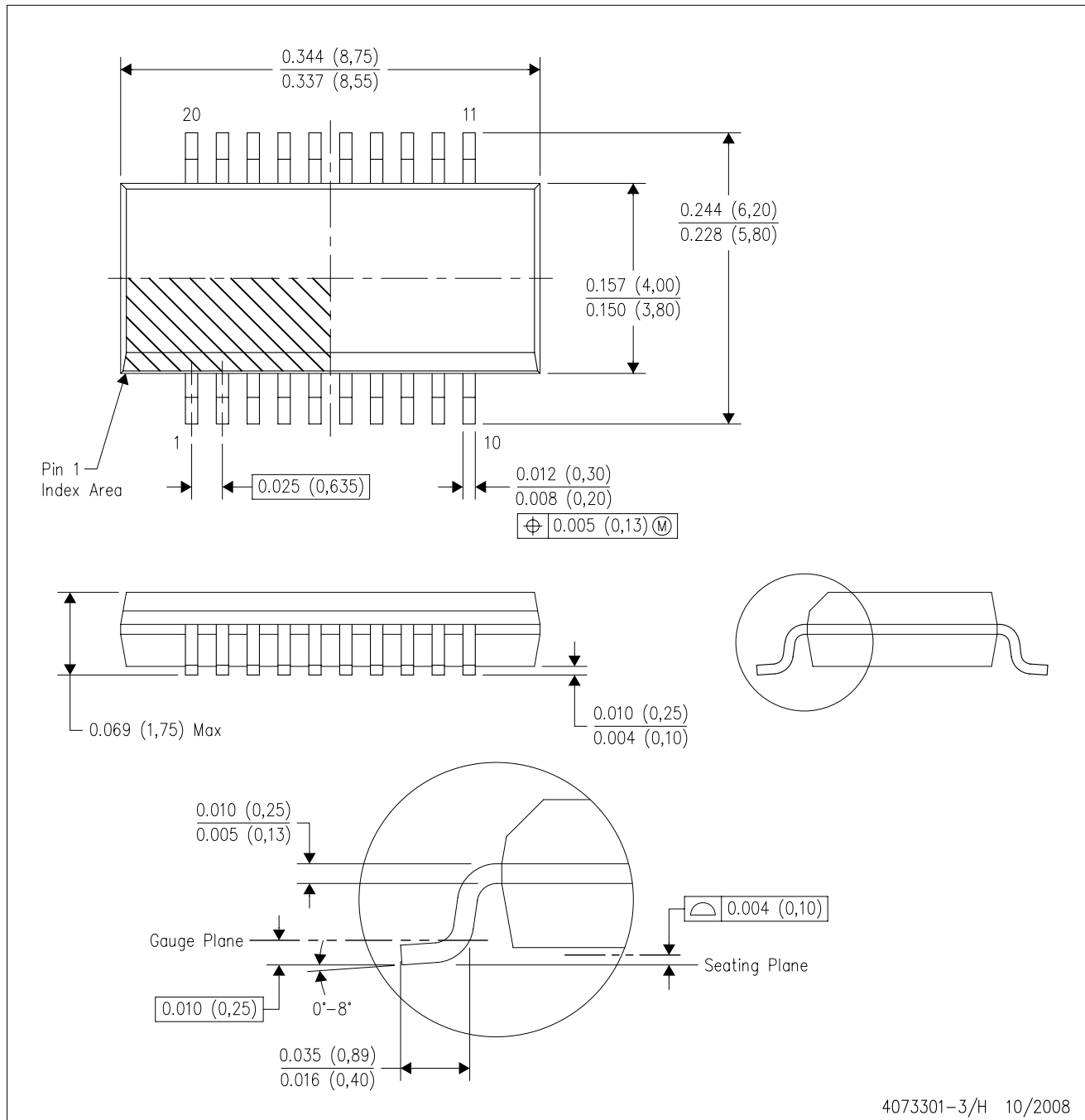
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AD.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

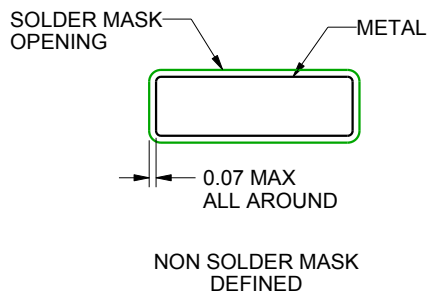
DW0020A

SOIC - 2.65 mm max height

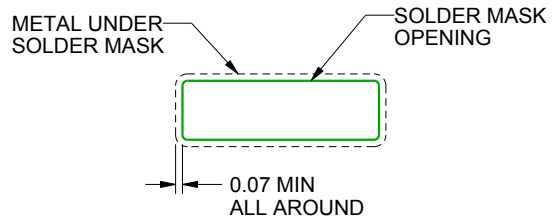
SOIC



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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