TEXAS INSTRUMENTS
SN74AVC4T234
JAJSJB8B – JUNE 2011 – REVISED JULY 2020

SN74AVC4T234 4 ビット、デュアル電源、単方向、非反転電圧トランスレータ

1 特長

- 広い動作 V_{CC} 範囲:0.9V～3.6V
- 3.6V I/O 許容で、混在モードの信号動作をサポート
- 最大 t_{pd}:3.7ns (3.3V 時)
- バランスが取れた伝播遅延:$t_{PLH} = t_{PHL}$
- 小さい静的消費電力、I_{CC}:5μA 以下
- どちらかの V_{CC} が 0V になると出力を無効化
- 1.8V で ±3mA の出力駆動能力
- 26Ω の直列抵抗 (A 側出力)
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- 入力ヒステリシスにより、低速な入力遷移と、入力のスイッチング・ノイズ耐性強化を実現
- 最大データ・レート
  - 380Mbps (1.8V から 3.3V に変換)
  - 200Mbps (1.8V 未満から 3.3V に変換)
  - 200Mbps (2.5V または 1.8V に変換)
  - 150Mbps (1.5V に変換)
  - 100Mbps (1.2V に変換)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 人体モデルで 2000V (A114-A)
  - デバイス帯電モデルで 500V (C101)

2 アプリケーション

- パーソナル・エレクトロニクス
- 産業用
- エンタープライズ
- 通信機器

3 概要

この 4 ビット非反転バス・トランシーバは、2 つの独立した構成可能な電源レールを使用して B ポート入力と A ポート出力の間の非同期通信を実現します。A ポートは V_{CCA} に追従し、B ポートは V_{CCB} に追従するように設計されており、V_{CCA} と V_{CCB} はどちらも 0.9V～3.6V に設定できます。

SN74AVC4T234 ソリューションは、0.9V～3.6V の V_{CC} 範囲全体にわたって非常に小さい静的および動的消費電力を達成しバッテリ寿命を延ばすことで、バッテリ駆動の携帯型アプリケーションにおける業界の低消費電力要求を満たします。また、この製品はシグナル・インテグリティを良好に維持します。

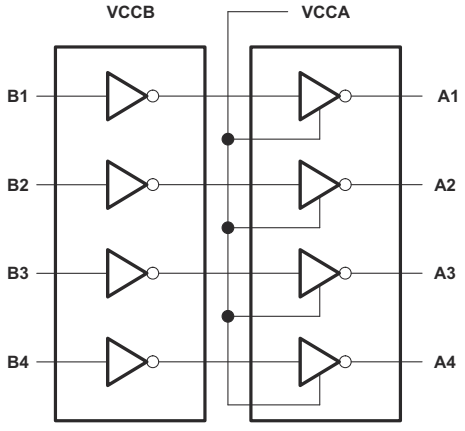
このデバイスは、I_{off} を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off} 回路が出力をディスエーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

V_{CC} 絶縁機能は、どちらかの V_{CC} 入力が GND レベルになると、A 側ポートを確実に高インピーダンス状態にします。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN74AVC4T234ZSU	uCSP (11)	2.00mm × 1.40mm
SN74AVC4T234ZWA	NFBGA (11)	2.00mm × 1.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 6
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics, V_{CCB} = 1.1 V ... 7
6.7 Switching Characteristics, V_{CCB} = 1.4 V ... 7
6.8 Switching Characteristics, V_{CCB} = 1.65 V ... 7
6.9 Switching Characteristics, V_{CCB} = 2.3 V ... 8
6.10 Switching Characteristics, V_{CCB} = 3 V ... 8
6.11 Operating Characteristics ... 8
7 Parameter Measurement Information ... 9
7.1 Load Circuit and Voltage Waveforms ... 9
8 Detailed Description ... 10
8.1 Overview ... 10
8.2 Functional Block Diagram ... 10
8.3 Feature Description ... 10
8.4 Device Functional Modes ... 10
9 Application and Implementation ... 11
9.1 Application Information ... 11
9.2 Typical Application ... 11
10 Power Supply Recommendations ... 12
11 Layout ... 12
11.1 Layout Guidelines ... 12
11.2 Layout Example ... 12
12 Device and Documentation Support ... 13
12.1 サポート・リソース ... 13
12.2 Trademarks ... 13
12.3 静電気放電に関する注意事項 ... 13
12.4 用語集 ... 13
13 Mechanical, Packaging, and Orderable Information ... 13

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (June 2011) to Revision B (July 2020)	Page
• 全体のフォーマットを、追加情報付きの新しい TI データシート標準に変更	1
• 「特長」の「入力ディスエーブル機能によりフローティング入力条件が可能」を削除	1
• 「特長」の「どちらかの V_{CC} が 0V になると出力を無効化」を追加	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「*注文情報*」表を削除	1
• 注文可能製品として ZWA パッケージを追加	1
• Added *ESD Ratings* table	4
• Added Thermal Information table	6
• Added Feature Description section.	10
• Added Device Functional Modes section	10
• Added Application and Implementation section	11
• Added Power Supply Recommendations section	12
• Added Layout section	12
• Added Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections.	13

5 Pin Configuration and Functions

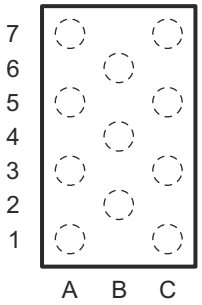


図 5-1. ZSU/ZWA Package 11-Pin uCSP Transparent Top View

Pin Functions

PIN	NO.	TYPE	DESCRIPTION
NAME	ZSU, ZWA		
B1	C7	I	Channel 1 Data input port
B2	C5	I	Channel 2 Data input port
B3	C3	I	Channel 3 Data input port
B4	C1	I	Channel 4 Data input port
A1	A7	O	Channel 1 Data output port
A2	A5	O	Channel 2 Data output port
A3	A3	O	Channel 3 Data output port
A4	A1	O	Channel 4 Data output port
V_{CCA}	B6	—	A-side output port power supply voltage (0.9 V to 3.6 V)
V_{CCB}	B4	—	B-side input port power supply voltage (0.9 V to 3.6 V)
GND	B2	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	Output ports (A port)	–0.5	4.6	V
		Input ports (B port)	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			V_{CCI} (1) (3)	V_{CCO} (2)	MIN	MAX	UNIT
V_{CCA}	Supply voltage				0.9	3.6	V
V_{CCB}	Supply voltage				0.9	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	0.9 V to 1.1 V		V_{CCI} × 0.8	3.6	V
			1.1 V to 1.4 V		V_{CCI} × 0.8	3.6	
			1.4 V to 1.95 V		V_{CCI} × 0.65	3.6	
			2.3 V to 2.7 V		V_{CCI} × 0.65	3.6	
			3 V to 3.6 V		V_{CCI} × 0.65	3.6	
V_{IL}	Low-level input voltage	Data inputs(4)	0.9 V to 1.1 V		0	V_{CCI} × 0.2	V
			1.1 V to 1.4 V		0	V_{CCI} × 0.2	
			1.1 V to 1.95 V		0	V_{CCI} × 0.35	
			2.3 V to 2.7 V		0	V_{CCI} × 0.35	
			3 V to 3.6 V		0	V_{CCI} × 0.35	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
I_{OH}	High-level output current			0.9 V to 1.1 V		–0.1	mA
				1.1 V to 1.3 V		–1	
				1.4 V to 1.6 V		–2	
				1.65 V to 1.95 V		–3	
				2.3 V to 2.7 V		–6	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			0.9 V to 1.1 V		0.1	mA
				1.1 V to 1.3 V		1	
				1.4 V to 1.6 V		2	
				1.65 V to 1.95 V		3	
				2.3 V to 2.7 V		6	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate			3 V to 3.6 V		10	ns/V
				2.3 V to 2.7 V		20	
				1.65 V to 1.95 V		50	
				1.4 V to 1.6 V		100	
				1.1 V to 1.3 V		100	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CCB} input port.
(2) V_{CCO} is the V_{CCA} output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V

6.4 Thermal Information

THERMAL METRIC[1]		SN74AVC4T234 ZSU (uCSP) 11 PINS	SN74AVC4T234 ZWA (NFBGA) 11 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	165.9	181.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.8	136.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	123.2	137.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.4	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	122.9	137.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-5.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER[1] [2]		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	0.9 V	0.9 V to 3.6 V	T_A = –40°C to 85°C	V_{CCA} – 0.1			V
		I_{OH} = –1 mA		1.1 V		T_A = –40°C to 85°C	0.88			
		I_{OH} = –2 mA		1.4 V		T_A = –40°C to 85°C	1.05			
		I_{OH} = –3 mA		1.65 V		T_A = –40°C to 85°C	1.2			
		I_{OH} = –6 mA		2.3V		T_A = –40°C to 85°C	1.75			
		I_{OH} = –12 mA		3 V		T_A = –40°C to 85°C	2.3			
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	0.9 V	0.9 V to 3.6 V	T_A = –40°C to 85°C			0.1	V
		I_{OL} = 1 mA		1.1 V		T_A = –40°C to 85°C			0.2	
		I_{OL} = 2 mA		1.4 V		T_A = –40°C to 85°C			0.2	
		I_{OL} = 3 mA		1.65 V		T_A = –40°C to 85°C			0.25	
		I_{OL} = 6 mA		2.3V		T_A = –40°C to 85°C			0.3	
		I_{OL} = 12 mA		3 V		T_A = –40°C to 85°C			0.55	
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V	T_A = 25°C		±0.1	±1	µA
						T_A = –40°C to 85°C			±5	
				0 V to 3.6 V	0 V	T_A = 25°C		±0.1	±1	
						T_A = –40°C to 85°C			±5	
I_{CCA}		V_{CCB} or GND, I_O = 0		0.8 V to 3.6 V	0.8 V to 3.6 V	T_A = –40°C to 85°C			8	µA
				0 V	0 V to 3.6 V	T_A = –40°C to 85°C			8	
				0 V to 3.6 V	0 V	T_A = –40°C to 85°C			8	
I_{CCB}		V_{CCB} or GND, I_O = 0		0.8 V to 3.6 V	0.8 V to 3.6 V	T_A = –40°C to 85°C			8	µA
				0 V	0 V to 3.6 V	T_A = –40°C to 85°C			8	
				0 V to 3.6 V	0 V	T_A = –40°C to 85°C			8	
I_{CCA} + I_{CCB}		V_{CCB} or GND, I_O = 0		0.8 V to 3.6 V	0.8 V to 3.6 V	T_A = –40°C to 85°C			16	µA
C_i	V_{CCB}	V_{CCB} = 3.3 V or GND		3.3 V	3.3 V	T_A = 25°C		22		pF
C_{io}	A or B port	V_{CCA} = 3.3 V or GND		3.3 V	3.3 V	T_A = 25°C		5		pF
						T_A = –40°C to 85°C			7	

(1) V_{CCI} is the V_{CCB} input port.
(2) V_{CCO} is the V_{CCA} output port.

6.6 Switching Characteristics, V_{CCB} = 1.1 V

over recommended operating free-air temperature range, V_{CCB} = 1.1 V (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	TYP	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V	5.5	ns
			V_{CCA} = 1.4 V	4.6	
			V_{CCA} = 1.65 V	4.2	
			V_{CCA} = 2.3 V	3.7	
			V_{CCA} = 3 V	3.9	
t_{PHL}	B	A	V_{CCA} = 1.1 V	4.7	ns
			V_{CCA} = 1.4 V	3.9	
			V_{CCA} = 1.65 V	3.4	
			V_{CCA} = 2.3 V	3	
			V_{CCA} = 3 V	3.1	

6.7 Switching Characteristics, V_{CCB} = 1.4 V

over recommended operating free-air temperature range, V_{CCB} = 1.4 V (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	MIN	TYP	MAX	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V		4.7		ns
			V_{CCA} = 1.4 V	2		5	
			V_{CCA} = 1.65 V	1.5		3.8	
			V_{CCA} = 2.3 V	1.2		3.8	
			V_{CCA} = 3 V	1		3.8	
t_{PHL}	B	A	V_{CCA} = 1.1 V		4.2		ns
			V_{CCA} = 1.4 V	2		5	
			V_{CCA} = 1.65 V	1.5		3.9	
			V_{CCA} = 2.3 V	1.2		3	
			V_{CCA} = 3 V	1		3	

6.8 Switching Characteristics, V_{CCB} = 1.65 V

over recommended operating free-air temperature range, V_{CCB} = 1.65 V (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	MIN	TYP	MAX	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V		4.3		ns
			V_{CCA} = 1.4 V	2		4.2	
			V_{CCA} = 1.65 V	1.5		4.1	
			V_{CCA} = 2.3 V	1.2		3.8	
			V_{CCA} = 3 V	1		3.7	
t_{PHL}	B	A	V_{CCA} = 1.1 V		2.6		ns
			V_{CCA} = 1.4 V	2		4.2	
			V_{CCA} = 1.65 V	1.5		4.1	
			V_{CCA} = 2.3 V	1.2		3.8	
			V_{CCA} = 3 V	1		3.7	

6.9 Switching Characteristics, V_{CCB} = 2.3 V

over recommended operating free-air temperature range, V_{CCB} = 2.3 V (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	MIN	TYP	MAX	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V		2.7		ns
			V_{CCA} = 1.4 V	2		3.5	
			V_{CCA} = 1.65 V	1.5		3.1	
			V_{CCA} = 2.3 V	1.2		2.8	
			V_{CCA} = 3 V	0.2		4.1	
t_{PHL}	B	A	V_{CCA} = 1.1 V		2.4		ns
			V_{CCA} = 1.4 V	2		3.7	
			V_{CCA} = 1.65 V	1.5		3.7	
			V_{CCA} = 2.3 V	1.2		2.8	
			V_{CCA} = 3 V	0.2		3.5	

6.10 Switching Characteristics, V_{CCB} = 3 V

over recommended operating free-air temperature range, V_{CCB} = 3 V (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA}	MIN	TYP	MAX	UNIT
t_{PLH}	B	A	V_{CCA} = 1.1 V		3.9		ns
			V_{CCA} = 1.4 V	2		3.8	
			V_{CCA} = 1.65 V	1.5		3.6	
			V_{CCA} = 2.3 V	0.5		3.6	
			V_{CCA} = 3 V	0.2		3.6	
t_{PHL}	B	A	V_{CCA} = 1.1 V		3.9		ns
			V_{CCA} = 1.4 V	2		3.7	
			V_{CCA} = 1.65 V	1.5		3.1	
			V_{CCA} = 2.3 V	0.5		3.5	
			V_{CCA} = 3 V	0.2		3	

6.11 Operating Characteristics

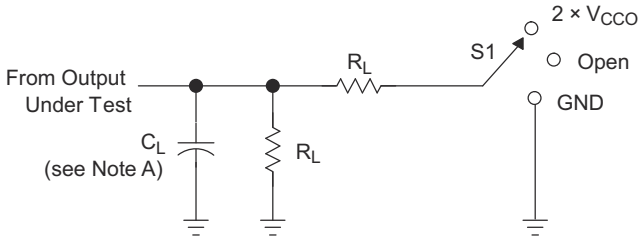
T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA}, V_{CCB}	TYP	UNIT
C_{pdA} (1)	B to A	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.1 V	18.5	pF
				V_{CCA} = V_{CCB} = 1.4 V		
				V_{CCA} = V_{CCB} = 1.65 V		
				V_{CCA} = V_{CCB} = 2.3 V		
				V_{CCA} = V_{CCB} = 3 V		

(1) Power dissipation capacitance per transceiver

7 Parameter Measurement Information

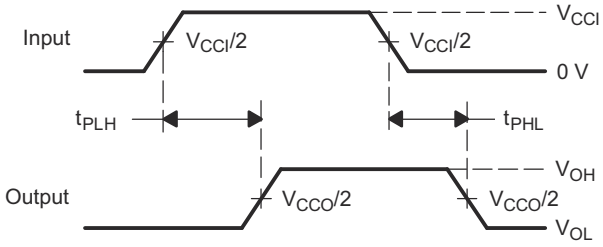
7.1 Load Circuit and Voltage Waveforms



LOAD CIRCUIT

TEST	S1
t_{pd}	Open

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	30 pF	0.5 kΩ	0.1 V
1.5 V ± 0.1 V	30 pF	0.5 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	0.5 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	0.5 kΩ	0.15 V
3.3 V ± 0.3 V	30 pF	0.5 kΩ	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is V_{CCB}.
F. V_{CCO} is V_{CCA}.

図 7-1. Load and Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AVC4T234 is a 4-bit, dual-supply noninverting voltage level translation device. The B input port pins are referenced to the V_{CCB} supply, and the A output port pins are referenced to the V_{CCA}. The B port is able to accept I/O voltages ranging from 0.9 V to 3.6 V.

8.2 Functional Block Diagram

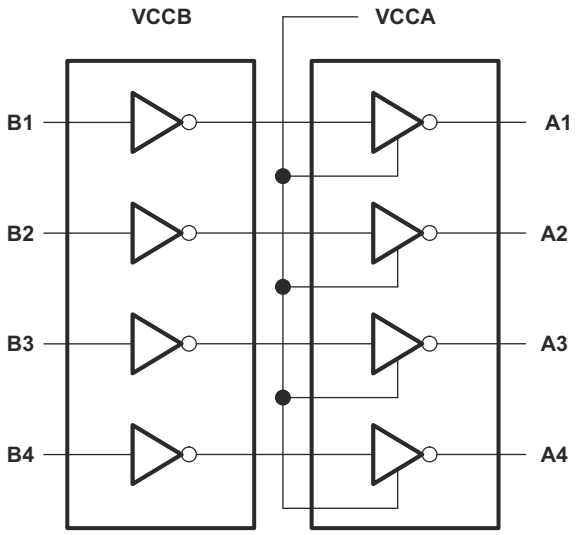


図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 0.9-V to 3.6-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 0.9 V and 3.6 V; thus, making the device suitable for translating between any of the low voltage nodes (0.9, 1.05 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Supports High Speed Translation

The SN74AVC4T234 device can support high data rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

8.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS	OUTPUTS
Bx	**Ax**
L	L
H (referenced to V_{CCB})	H (referenced to V_{CCA})

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74AVC4T234 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T234 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

9.2 Typical Application

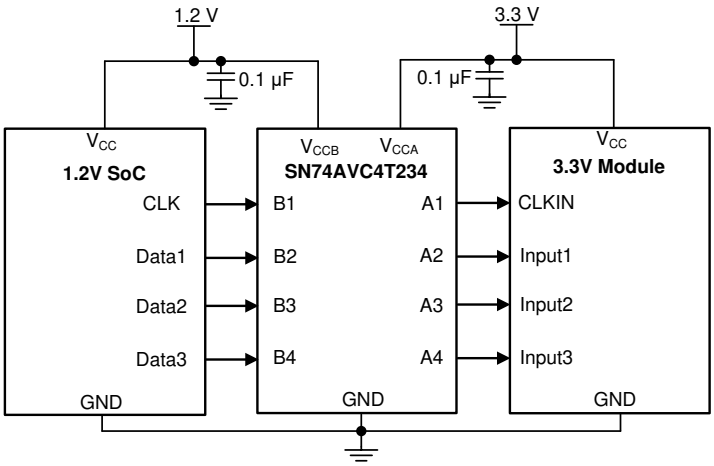


図 9-1. Typical Application Diagram

9.2.1 Design Requirements

For the design example shown in *Typical Application,* use the parameters listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	0.9 V to 3.6 V
Output voltage range	0.9 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T234 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T234 device is driving to determine the output voltage range.

9.2.3 Application Curves

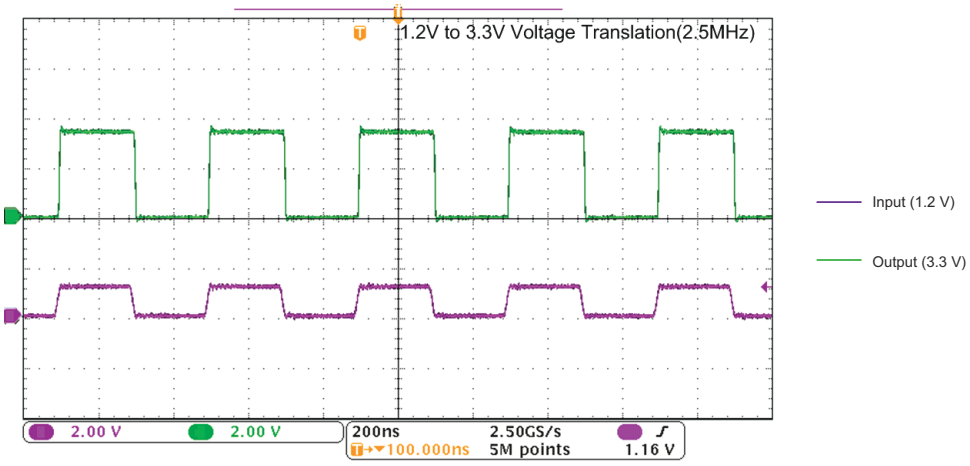


図 9-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

10 Power Supply Recommendations

The SN74AVC4T234 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 0.9 V to 3.6 V and V_{CCB} accepts any supply voltage from 0.9 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 0.9-V, 1.05-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes.

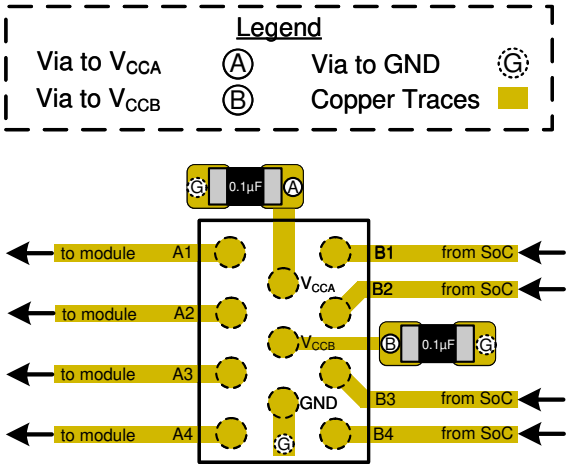
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

11.2 Layout Example



12 Device and Documentation Support

12.1 サポート・リソース

TI E2E™ サポート・フォーラムは、検証済みの迅速な回答と設計支援をエンジニアがエキスパートから直接得るための頼れる情報源です。既存の回答を検索し、または新たに質問することで、必要とする設計支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.3 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.4 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC4T234ZWAR	ACTIVE	NFBGA	ZWA	11	2500	RoHS & Green	SN98.5/AG1/CU0.5	Level-2-260C-1 YEAR	-40 to 85	1G2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

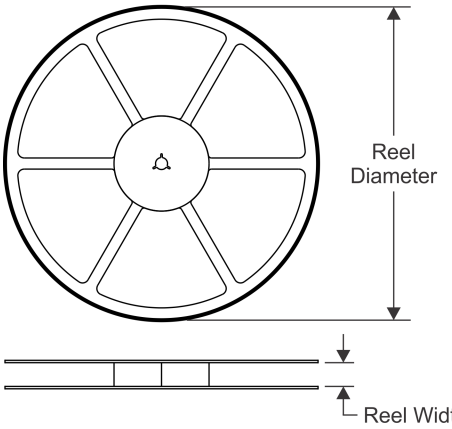
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

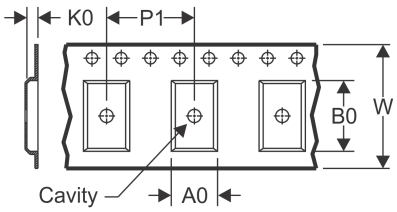
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

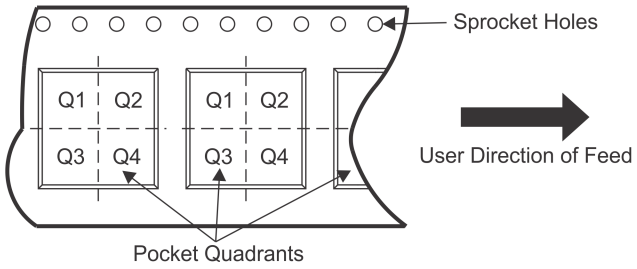


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

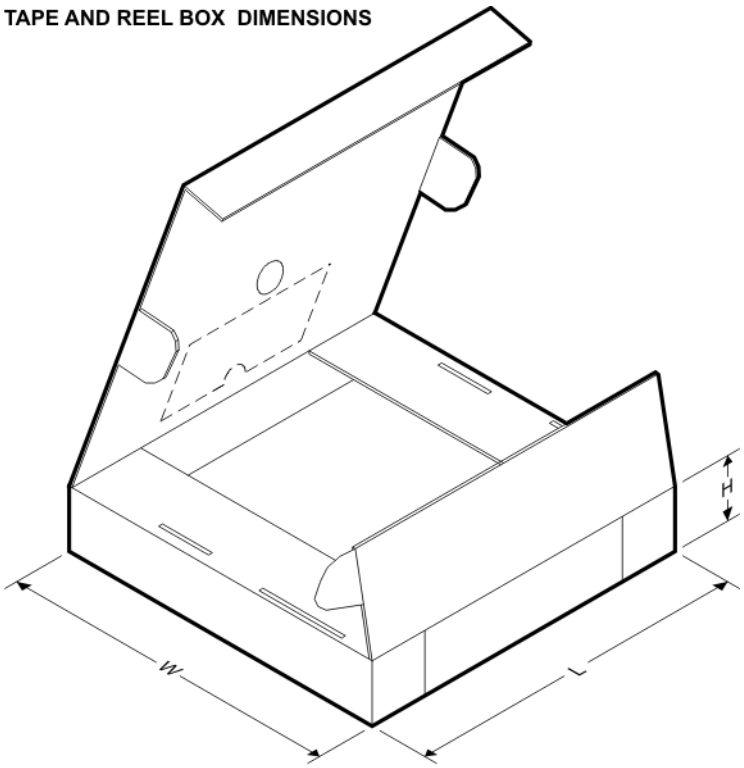
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC4T234ZWAR	NFBGA	ZWA	11	2500	330.0	8.4	1.6	2.2	0.55	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

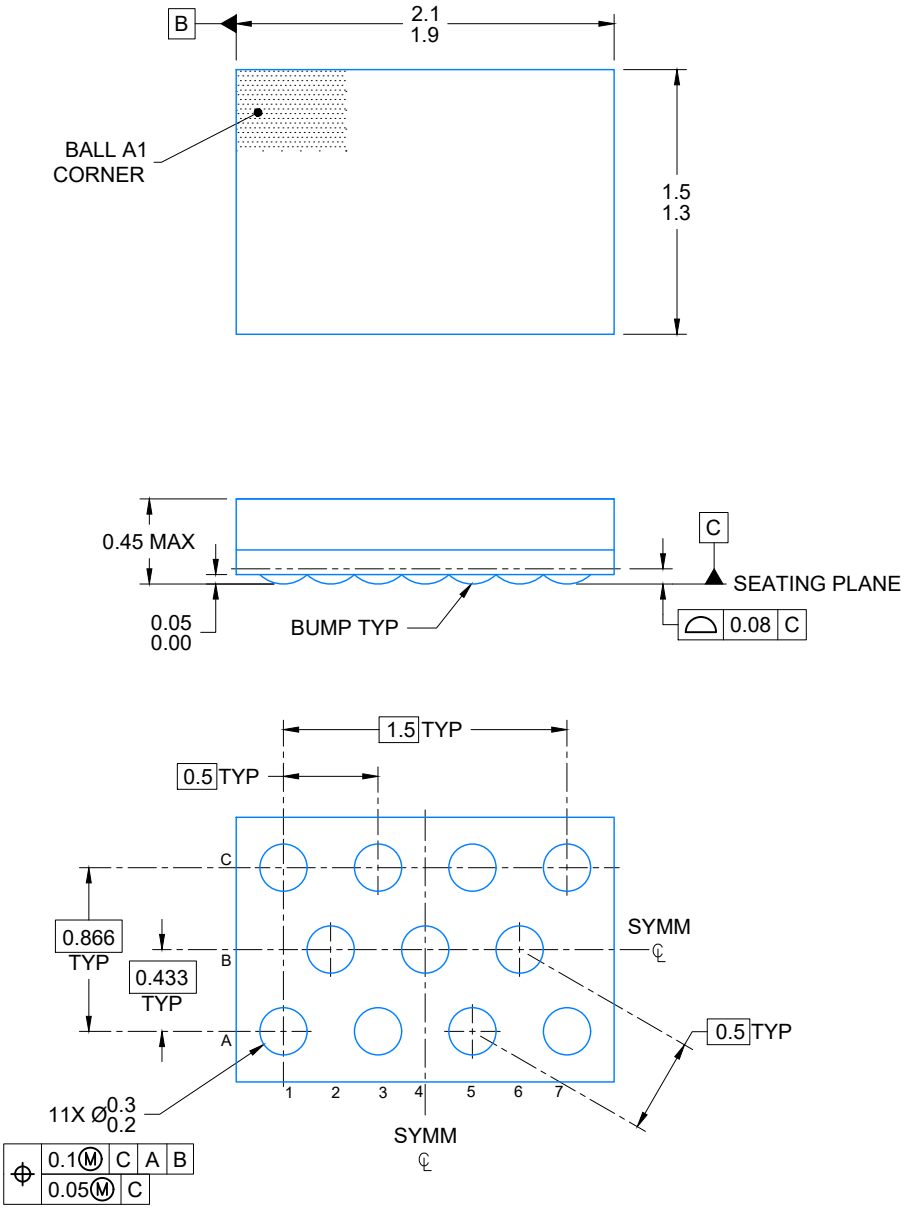
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC4T234ZWAR	NFBGA	ZWA	11	2500	338.1	338.1	20.6

PACKAGE OUTLINE

ZWA0011A

NFBGA - 0.45 mm max height

MICRO CHIP SCALE PACKAGE

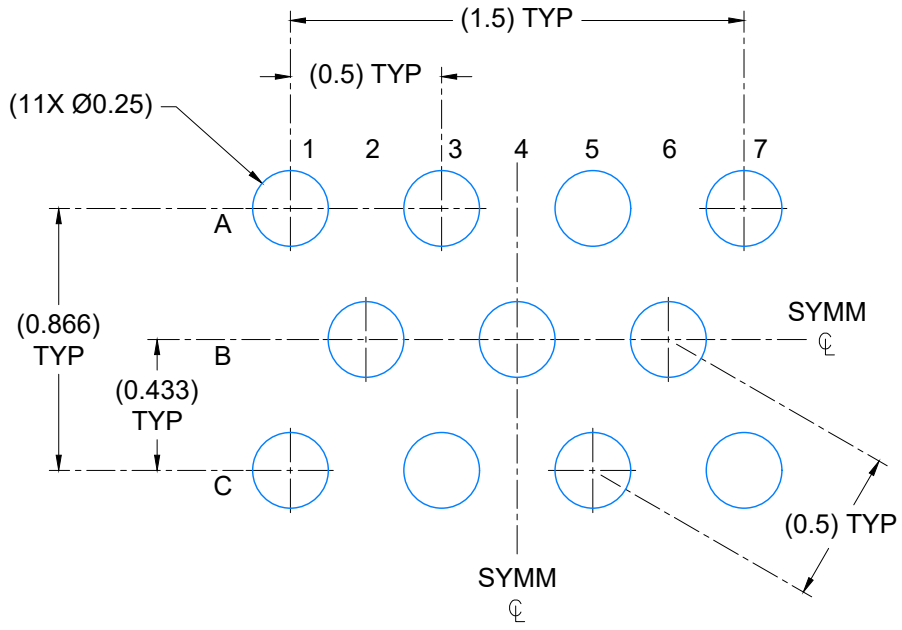


4224717/A 12/2018

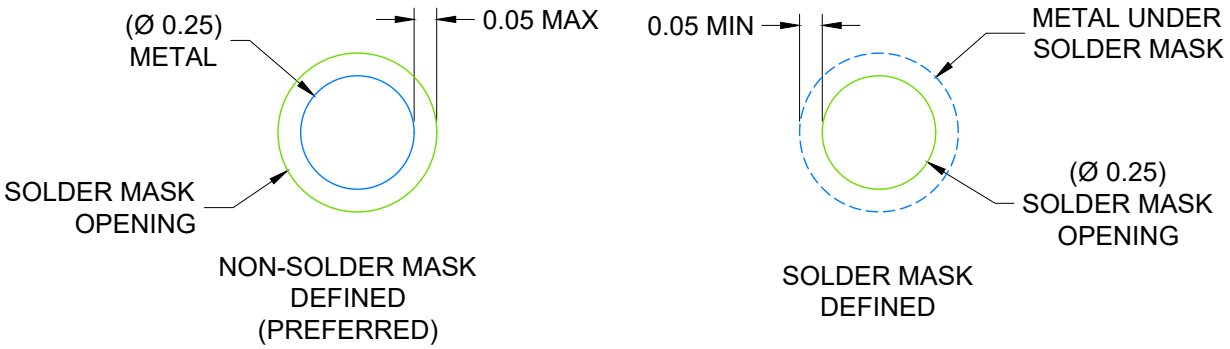
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224717/A 12/2018

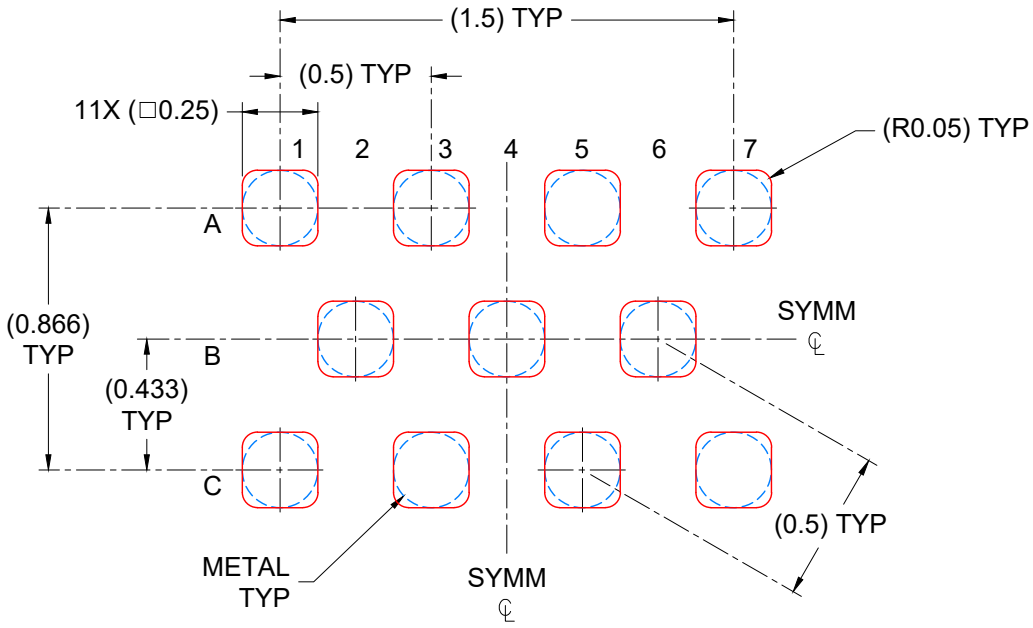
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

NFBGA - 0.45 mm max height

MICRO CHIP SCALE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4224717/A 12/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265