# SN74AUP1T34 1ビット単方向電圧レベル変換器

## 1 特長

- 広い動作VCC範囲: 0.9V～3.6V
- 平衡化された伝播遅延: $t_{PLH}$ = $t_{PHL}$ (1.8Vから3.3Vへの変換の標準値)
- 低い静的消費電力: 最大値5µA ICC
- 3Vにおいて±6mAの出力駆動能力
- $I_{off}$により部分的パワーダウン・モード動作をサポート
- VCC絶縁機能 - $V_{CCA}$入力がGNDのとき、Bポートは高インピーダンス状態
- 入力ヒステリシスにより、低速な入力遷移と、入力のスイッチング・ノイズ耐性強化を実現
- JESD 22を超えるESD保護
- 5000V、人体モデル(A114-A)
- JESD 78, Class II準拠で100mA超のラッチアップ性能

## 2 アプリケーション

- エンタープライズ
- 産業用
- パーソナル・エレクトロニクス
- テレコミュニケーション

## 3 概要

SN74AUP1T34デバイスは、1ビットの非反転変換器で、2つの独立に構成可能な電源レールを使用します。AからBへの単方向変換器として動作し、Aポートは$V_{CCA}$をトラッキングするよう設計されています。$V_{CCA}$は0.9V～3.6Vの電源電圧を受け付けます。Bポートは$V_{CCB}$をトラッキングするよう設計されています。$V_{CCB}$は0.9V～3.6Vの電源電圧を受け付けます。これにより、1V、1.2V、1.5V、1.8V、2.5V、3.3Vの電圧ノード間で低電圧の変換が可能になります。また、SN74AUP1T34は$I_{off}$を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。$I_{off}$回路が出力をディスエーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

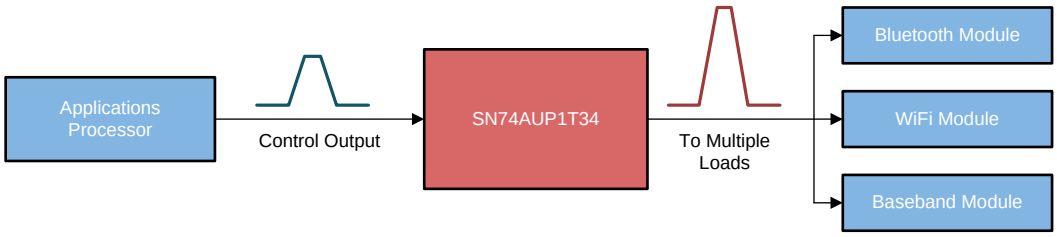
VCC絶縁機能により、$V_{CCA}$入力がGNDのとき、Bポートは高インピーダンス状態です。$V_{CCB}$入力がGNDのとき、A側へのどの入力も、たとえフローティングであっても、リーク電流は引き起こしません。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| SN74AUP1T34DCK | SC70 (5) | 2.00mm×1.25mm |
| SN74AUP1T34DRY | SON (6) | 1.45mm×1.00mm |
| SN74AUP1T34DSF | SON (6) | 1.00mm×1.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**サンプル・アプリケーション**



# 目次



## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Revision E (June 2016)** から **Revision F** に変更 **Page**

- Added operating junction temperature to *Absolute Maximum Ratings* table ... 5
- Updated *Recommended Operating Conditions* table ... 6
- Updated the $V_{CCB}$ value for the parameter 'high-level input voltage' in the *Recommended Operating Conditions* table ... 6
- Updated the $V_{CCB}$ value for the parameter 'low-level input voltage' in the *Recommended Operating Conditions* table ... 6
- Added *Electrical Characteristics: DC* table ... 7

**Revision D (April 2016)** から **Revision E** に変更 **Page**

- Changed pin A number From: 3 To: 2 and GND From: 2 To: 3 for the SC70 package in the *Pin Configuration and Functions* section ... 4

**Revision C (May 2013)** から **Revision D** に変更 **Page**

- 「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。... 1
- 「*注文情報*」表を削除 ... 1

**Revision B (July 2012)** から **Revision C** に変更 **Page**

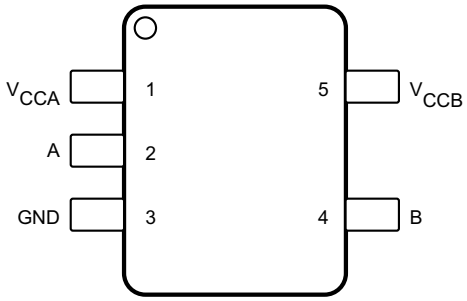
- 「特長」に「VCC絶縁機能 - $V_{CCA}$入力がGNDのとき、Bポートは高インピーダンス状態」を追加 ... 1
- Updated *Pin Functions* table. ... 4
- Deleted $I_{OZ}$ PARAMETER from RECOMMENDED OPERATION CONDITIONS. ... 6
- Added $V_{MI}$ and $V_{MO}$ equations to Wavefrom 1 graphic. ... 10
- 追加 FUNCTION TABLE. ... 12

**Revision A (June 2012) から Revision B に変更** **Page**

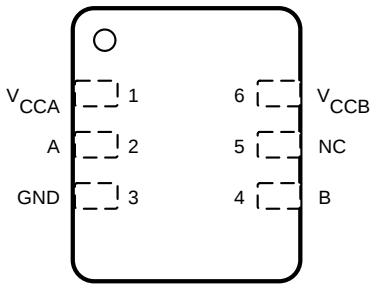
- 「特長」から「出力イネーブル機能により、ユーザーが出力をディセーブルして消費電力を削減可能」を削除..... 1

# 5 Pin Configuration and Functions

**DCK Package**
**5-Pin SC70**
**Top View**




**DRY or DSF Package**
**6-Pin SON**
**Top Through View**




**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SC70 | SON | | |
| A | 2 | 2 | I | Input Port |
| B | 4 | 4 | O | Output Port |
| GND | 3 | 3 | — | Ground |
| $V_{CCA}$ | 1 | 1 | — | Input Port DC Power Supply |
| $V_{CCB}$ | 5 | 6 | — | Output Port DC Power Supply |
| NC | — | 5 | — | No Connect. Leave floating. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CCA}$ and $V_{CCB}$ | | –0.3 | 4 | V |
| Input voltage, $V_I$ | | –0.5 | 4.6 | V |
| | | –0.5 | 4.6 | |
| | | –0.5 | 4.6 | |
| Voltage applied to any output in the high-impedance or power-off state, $V_O$ | | –0.5 | 4.6 | V |
| | | –0.5 | 4.6 | |
| Voltage applied to any output in the high or low state, $V_O$ | | –0.5 | 4.6 | V |
| | | –0.5 | 4.6 | |
| Input clamp current, $I_{IK}$ | $V_I$ < 0 V | | –50 | mA |
| Output clamp current, $I_{OK}$ | $V_O$ < 0 V | | –50 | mA |
| Continuous output current, $I_O$ | | | ±50 | mA |
| Continuous current through $V_{CCA}$ or GND | | | ±100 | mA |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |
| Operating junction temperature, $T_J$ | | | 150 | °C |

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | 5000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | 750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | 0.9 | | 3.6 | V |
| $V_{CCB}$ | Supply voltage | | | 0.9 | | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CCA}$ = 0.9 V to 1.95 V | $V_{CCB}$ = 0.9 V to 3.6 V | 0.65 × $V_{CCA}$ | | | V |
| | | $V_{CCA}$ = 2.3 V to 2.7 V | $V_{CCB}$ = 0.9 V to 3.6 V | 1.6 | | | |
| | | $V_{CCA}$ = 3 V to 3.6 V | $V_{CCB}$ = 0.9 V to 3.6 V | 2 | | | |
| $V_{IH}$ | Low-level input voltage | $V_{CCA}$ = 0.9 V | $V_{CCB}$ = 0.9 V to 3.6 V | | | 0.3 × $V_{CCA}$ | V |
| | | $V_{CCA}$ = 1 V to 1.95 V | $V_{CCB}$ = 0.9 V to 3.6 V | | | 0.35 × $V_{CCA}$ | |
| | | $V_{CCA}$ = 2.3 V to 2.7 V | $V_{CCB}$ = 0.9 V to 3.6 V | | | 0.7 | |
| | | $V_{CCA}$ = 3 V to 3.6 V | $V_{CCB}$ = 0.9 V to 3.6 V | | | 0.9 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CCA}$ = 3 V to 3.6 V | $V_{CCB}$ = 0.9 V to 3.6 V | | | 200 | ns/V |
| $T_A$ | Operating free-air temperature | | | –40 | | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74AUP1T34 | | | UNIT |
|---|---|---|---|---|---|
| | | DCK (SC70) | DRY (SON) | DSF (SON) | |
| | | 5 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 300.8 | 338.5 | 367.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 141.3 | 240.4 | 188.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 77.3 | 224.6 | 274.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 12.6 | 86.8 | 24.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 76.5 | 221.4 | 273.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics: DC

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_I = V_{IH}$ | $I_{OH}$ = –100 µA | 0.9 V to 3.6 V | 0.9 V to 3.6 V | $V_{CCB}$ – 0.2 | | V |
| | | | $I_{OH}$ = –0.25 mA | 0.9 V to 1 V | 0.9 V to 1 V | 0.75 × $V_{CCB}$ | | |
| | | | $I_{OH}$ = –1.5 mA | 1.2 V | 1.2 V | 1 | | |
| | | | $I_{OH}$ = –2 mA | 1.65 V | 1.65 V | 1.32 | | |
| | | | $I_{OH}$ = –3 mA | 2.3 V | 2.3 V | 1.9 | | |
| | | | $I_{OH}$ = –6 mA | 3 V | 3 V | 2.72 | | |
| $V_{OL}$ | Low-level output voltage | $V_I = V_{IL}$ | $I_{OL}$ = 100 µA | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | 0.1 | V |
| | | | $I_{OL}$ = 0.25 mA | 0.9 V to 1 V | 0.9 V to 1 V | | 0.1 | |
| | | | $I_{OL}$ = 1.5 mA | 1.2 V | 1.2 V | | 0.3 × $V_{CCB}$ | |
| | | | $I_{OL}$ = 2 mA | 1.65 V | 1.65 V | | 0.31 | |
| | | | $I_{OL}$ = 3 mA | 2.3 V | 2.3 V | | 0.31 | |
| | | | $I_{OL}$ = 6 mA | 3 V | 3 V | | 0.31 | |
| $I_I$ | Input leakage current | $V_I$ = VCCA or GND | | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | ±1 | µA |
| $I_{off}$ | Off-state current | A or B port: $V_I$ or $V_O$ = 0 to 3.6 V | | 0 V | 0 V to 3.6 V | | ±5 | µA |
| | | | | 0 V to 3.6 V | 0 V | | ±5 | |
| $I_{CCA}$ | $V_{CCA}$ supply current | $V_I$ = VCCI or GND, $I_O$ = 0 mA | | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | 5 | µA |
| | | | | 0.9 V to 3.6 V | $V_{CCA}$ | | 2 | |
| | | | | 0 V | 0 V to 3.6 V | | 1 | |
| | | | | 0 V to 3.6 V | 0 V | | 1 | |
| $I_{CCB}$ | $V_{CCB}$ supply current | $V_I$ = VCCI or GND, $I_O$ = 0 mA | | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | 5 | µA |
| | | | | 0.9 V to 3.6 V | $V_{CCA}$ | | 2 | |
| | | | | 0 V | 0 V to 3.6 V | | 1 | |
| | | | | 0 V to 3.6 V | 0 V | | 1 | |
| $I_{CCA}$ + $I_{CCB}$ | Combined supply current | $V_I$ = VCCI or GND, $I_O$ = 0 mA | | 0.9 V to 3.6 V | 0.9 V to 3.6 V | | 5.2 | µA |
| $C_I$ | Input capacitance | $V_I$ = 3.3 V or GND | | 3.3 V | 3.3 V | | 4 | pF |
| $C_{I/O}$ | Input-to-output internal capacitance | A or B port: $V_O$ = 3.3 V or GND | | 0 V | 3.3 V | | 7 | pF |

## 6.6 Electrical Characteristics: AC

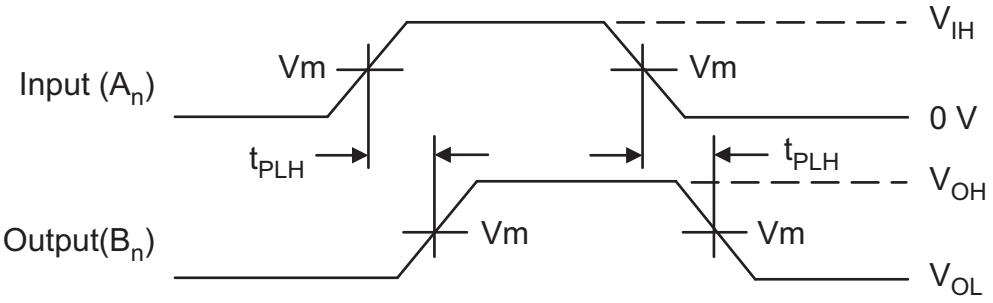
over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}/t_{PHL}$ | Propagation delay time low-to-high output / high-to-low output | $C_L$ = 5 pF | 0.9 V | 0.9 V | | 25 | | ns |
| | | | | 1.2 V | | 18 | | |
| | | | | 1.65 V | | 16.2 | | |
| | | | | 2.3 V | | 16.3 | | |
| | | | | 3 V | | 16.8 | | |
| | | $C_L$ = 5 pF | 1.2 V | 0.9 V | | | 42.5 | |
| | | | | 1.2 V | | | 24.9 | |
| | | | | 1.65 V | | | 23.2 | |
| | | | | 2.3 V | | | 22.6 | |
| | | | | 3 V | | | 22.5 | |
| | | $C_L$ = 5 pF | 1.65 V | 0.9 V | | | 40 | |
| | | | | 1.2 V | | | 10.7 | |
| | | | | 1.65 V | | | 8.84 | |
| | | | | 2.3 V | | | 8.08 | |
| | | | | 3 V | | | 7.88 | |
| | | $C_L$ = 5 pF | 2.3 V | 0.9 V | | | 41.3 | |
| | | | | 1.2 V | | | 8.02 | |
| | | | | 1.65 V | | | 5.73 | |
| | | | | 2.3 V | | | 4.92 | |
| | | | | 3 V | | | 4.2 | |
| | | $C_L$ = 5 pF | 3 V | 0.9 V | | | 42.5 | |
| | | | | 1.2 V | | | 7.61 | |
| | | | | 1.65 V | | | 4.5 | |
| | | | | 2.3 V | | | 3.65 | |
| | | | | 3 V | | | 3.39 | |
| $t_{PLH}/t_{PHL}$ | Propagation delay time low-to-high output / high-to-low output | $C_L$ = 10 pF | 0.9 V | 0.9 V | | 28.9 | | ns |
| | | | | 1.2 V | | 19.8 | | |
| | | | | 1.65 V | | 17.9 | | |
| | | | | 2.3 V | | 18 | | |
| | | | | 3 V | | 18.5 | | |
| | | $C_L$ = 10 pF | 1.2 V | 0.9 V | | | 43.22 | |
| | | | | 1.2 V | | | 12.33 | |
| | | | | 1.65 V | | | 9.57 | |
| | | | | 2.3 V | | | 8.81 | |
| | | | | 3 V | | | 8.61 | |
| | | $C_L$ = 10 pF | 1.65 V | 0.9 V | | | 40.44 | |
| | | | | 1.2 V | | | 9.21 | |
| | | | | 1.65 V | | | 6.57 | |
| | | | | 2.3 V | | | 5.5 | |
| | | | | 3 V | | | 4.73 | |
| | | $C_L$ = 10 pF | 2.3 V | 0.9 V | | | 41.56 | |
| | | | | 1.2 V | | | 8.3 | |
| | | | | 1.65 V | | | 5.54 | |
| | | | | 2.3 V | | | 4.42 | |
| | | | | 3 V | | | 4.01 | |
| | | $C_L$ = 10 pF | 3 V | 0.9 V | | | 42.81 | |
| | | | | 1.2 V | | | 7.87 | |
| | | | | 1.65 V | | | 4.55 | |
| | | | | 2.3 V | | | 3.8 | |
| | | | | 3 V | | | 3.36 | |

## Electrical Characteristics: AC (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}/t_{PHL}$ | Propagation delay time low-to-high output / high-to-low output | $C_L$ = 15 pF | 0.9 V | 0.9 V | | 30.6 | | ns |
| | | | | 1.2 V | | 21.6 | | |
| | | | | 1.65 V | | 19.6 | | |
| | | | | 2.3 V | | 19.7 | | |
| | | | | 3 V | | 20.3 | | |
| | | $C_L$ = 15 pF | 1.2 V | 0.9 V | | | 43.87 | |
| | | | | 1.2 V | | | 12.98 | |
| | | | | 1.65 V | | | 10.3 | |
| | | | | 2.3 V | | | 9.54 | |
| | | | | 3 V | | | 9.34 | |
| | | $C_L$ = 15 pF | 1.65 V | 0.9 V | | | 40.78 | |
| | | | | 1.2 V | | | 9.59 | |
| | | | | 1.65 V | | | 6.95 | |
| | | | | 2.3 V | | | 5.87 | |
| | | | | 3 V | | | 5.07 | |
| | | $C_L$ = 15 pF | 2.3 V | 0.9 V | | | 41.79 | |
| | | | | 1.2 V | | | 8.55 | |
| | | | | 1.65 V | | | 5.8 | |
| | | | | 2.3 V | | | 4.68 | |
| | | | | 3 V | | | 4.27 | |
| | | $C_L$ = 15 pF | 3 V | 0.9 V | | | 43.09 | |
| | | | | 1.2 V | | | 8.16 | |
| | | | | 1.65 V | | | 4.84 | |
| | | | | 2.3 V | | | 4.09 | |
| | | | | 3 V | | | 3.65 | |
| $t_{PLH}/t_{PHL}$ | Propagation delay time low-to-high output / high-to-low output | $C_L$ = 30 pF | 0.9 V | 0.9 V | | 32.1 | | ns |
| | | | | 1.2 V | | 21.3 | | |
| | | | | 1.65 V | | 18.7 | | |
| | | | | 2.3 V | | 18 | | |
| | | | | 3 V | | 18.3 | | |
| | | $C_L$ = 30 pF | 1.2 V | 0.9 V | | | 45.65 | |
| | | | | 1.2 V | | | 14.76 | |
| | | | | 1.65 V | | | 12.37 | |
| | | | | 2.3 V | | | 11.61 | |
| | | | | 3 V | | | 11.41 | |
| | | $C_L$ = 30 pF | 1.65 V | 0.9 V | | | 41.72 | |
| | | | | 1.2 V | | | 10.65 | |
| | | | | 1.65 V | | | 8.01 | |
| | | | | 2.3 V | | | 6.94 | |
| | | | | 3 V | | | 5.99 | |
| | | $C_L$ = 30 pF | 2.3 V | 0.9 V | | | 42.44 | |
| | | | | 1.2 V | | | 9.26 | |
| | | | | 1.65 V | | | 6.51 | |
| | | | | 2.3 V | | | 5.39 | |
| | | | | 3 V | | | 4.97 | |
| | | $C_L$ = 30 pF | 3 V | 0.9 V | | | 43.69 | |
| | | | | 1.2 V | | | 8.8 | |
| | | | | 1.65 V | | | 5.48 | |
| | | | | 2.3 V | | | 4.72 | |
| | | | | 3 V | | | 4.28 | |




$V_{MI}$ =$V_{IH}$/2; $V_{MO}$= $V_{CCB}$/2

$t_R$ = $t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns

**Figure 1. Waveform 1 – Propagation Delays**

## 6.7 Typical Characteristics

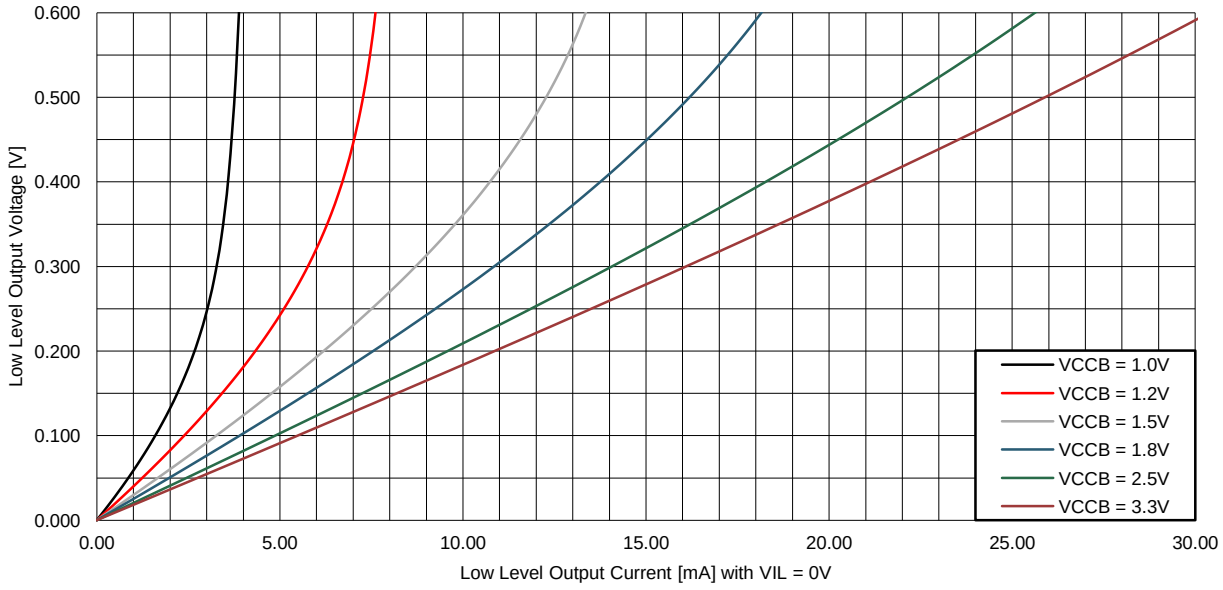
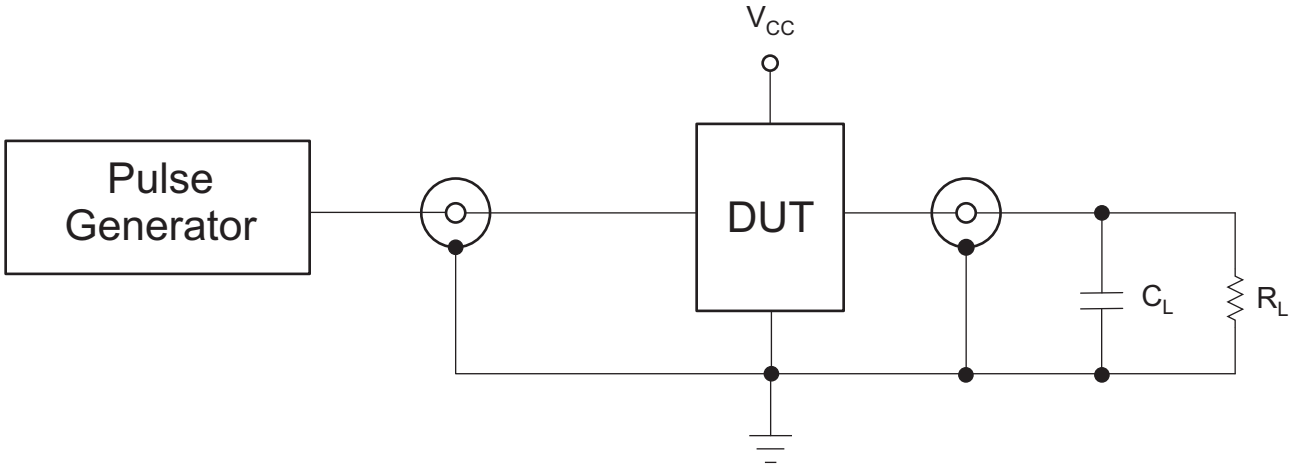



**図 2. Low Level Output Voltage vs Low Level Output Current**

## 7 Parameter Measurement Information




**TEST**

$t_{PLH}$, $t_{PHL}$

$C_L$ = 5 pF, 10 pF, 15 pF, 30 pF or equivalent (includes probe and jig capacitance)

$R_L$ = 1 MΩ or equivalent

$Z_{OUT}$ of pulse generator = 50 Ω

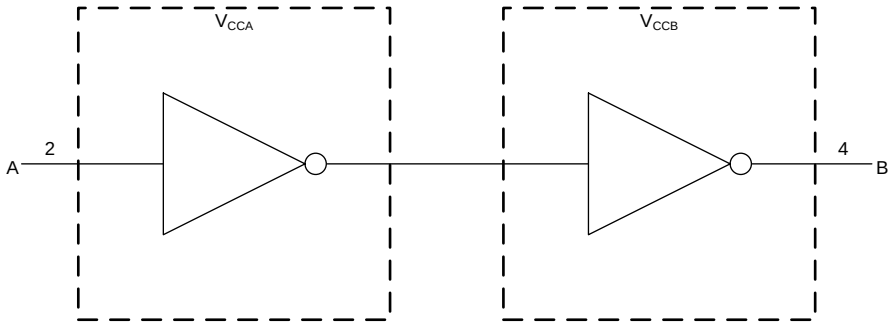
**図 3. AC (Propagation Delay) Test Circuit**

# 8 Detailed Description

## 8.1 Overview

The SN74AUP1T34 is a unidirectional, single-bit, dual-supply, noninverting voltage-level translator. Pin A, which is referenced to $V_{CCA}$, receives the signal that is to be level translated. Pin B, which is referenced to $V_{CCB}$, transmits the level translated signal. Both supply pins $V_{CCA}$ and $V_{CCB}$ support a voltage range from 0.9 V to 3.6 V.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Fully Configurable Dual-Rail Design

Both $V_{CCA}$ and $V_{CCB}$ can be supplied at any voltage from 0.9 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (1 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

### 8.3.2 Partial-Power-Down Mode Operation

$I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the SN74AUP1T34 when it is powered down. This can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

### 8.3.3 $V_{CC}$ Isolation

The $V_{CC}$ isolation feature ensures that if either $V_{CCA}$ or $V_{CCB}$ are at GND (or < 0.4 V), both ports A and B are set to a high-impedance state, preventing false logic levels from being presented to either bus.

### 8.3.4 Input Hysteresis

Input hysteresis allows the input to support slew rates as slow as 200 ns/V, improving switching noise immunity.

## 8.4 Device Functional Modes

表 1 lists the functional modes of the SN74AUP1T34.

**表 1. Function Table**

| INPUT | OUTPUT |
|---|---|
| **A PORT** | **B PORT** |
| L | L |
| H | H |

# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74AUP1T34 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

## 9.2 Typical Application

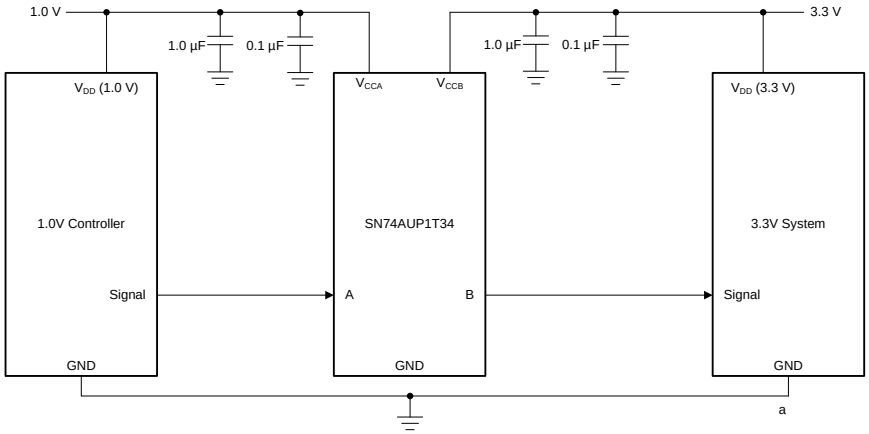



**図 4. Typical Application Example**

### 9.2.1 Design Requirements

表 2 lists the design requirements of the SN74AUP1T34.

**表 2. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input Voltage Range | 0.9 V to 3.6 V |
| Output Voltage Range | 0.9 V to 3.6 V |

### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AUP1T34 device to determine the input voltage range. For a valid logic-high, the value must exceed the $V_{IH}$ of the input port. For a valid logic low the value must be less than the $V_{IL}$ of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AUP1T34 device is driving to determine the output voltage range.

### 9.2.3 Application Curve

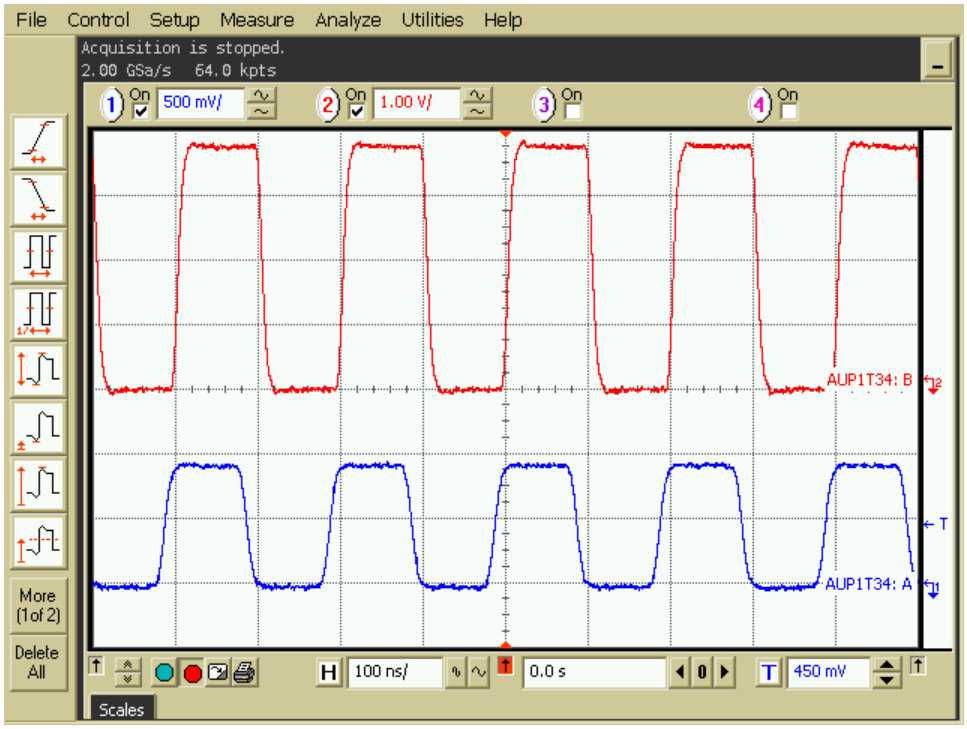



**図 5. 10-MHz Up Translation (0.9 V to 3.6 V)**

## 10 Power Supply Recommendations

Connect ground before applying either $V_{CCA}$ or $V_{CCB}$. There is no specific power sequence requirement for the SN74AUP1T34. $V_{CCA}$ or $V_{CCB}$ may be powered up first, and $V_{CCA}$ or $V_{CCB}$ may be powered down first.

## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

### 11.2 Layout Example

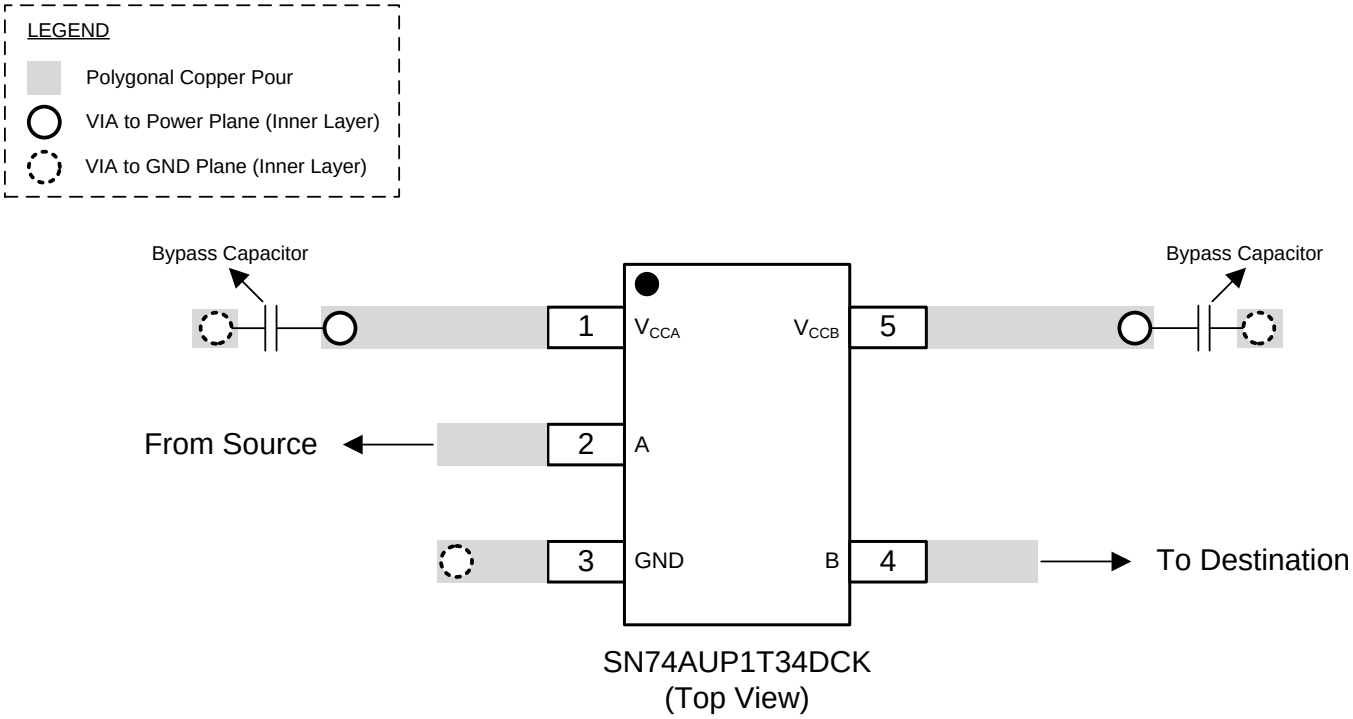



**図 6. Example Layout**

# 12 デバイスおよびドキュメントのサポート

## 12.1 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™オンライン・コミュニティ** ***TIのE2E ( Engineer-to-Engineer ) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

**設計サポート** ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

## 12.2 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.3 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

## 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1T34DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | U2E | Samples |
| SN74AUP1T34DRYR | ACTIVE | SON | DRY | 6 | 5000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U2 | Samples |
| SN74AUP1T34DSFR | ACTIVE | SON | DSF | 6 | 5000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U2 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AUP1T34 :**

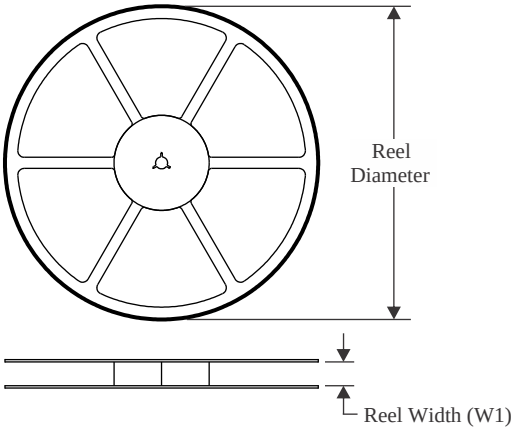
- Automotive : SN74AUP1T34-Q1

NOTE: Qualified Version Definitions:

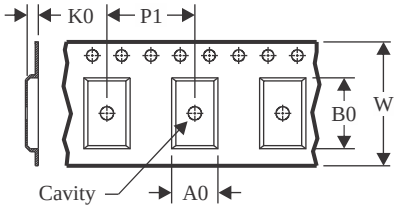
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

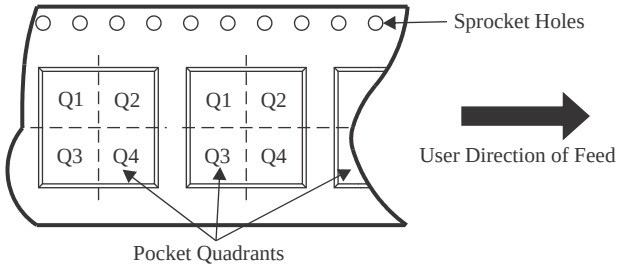



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

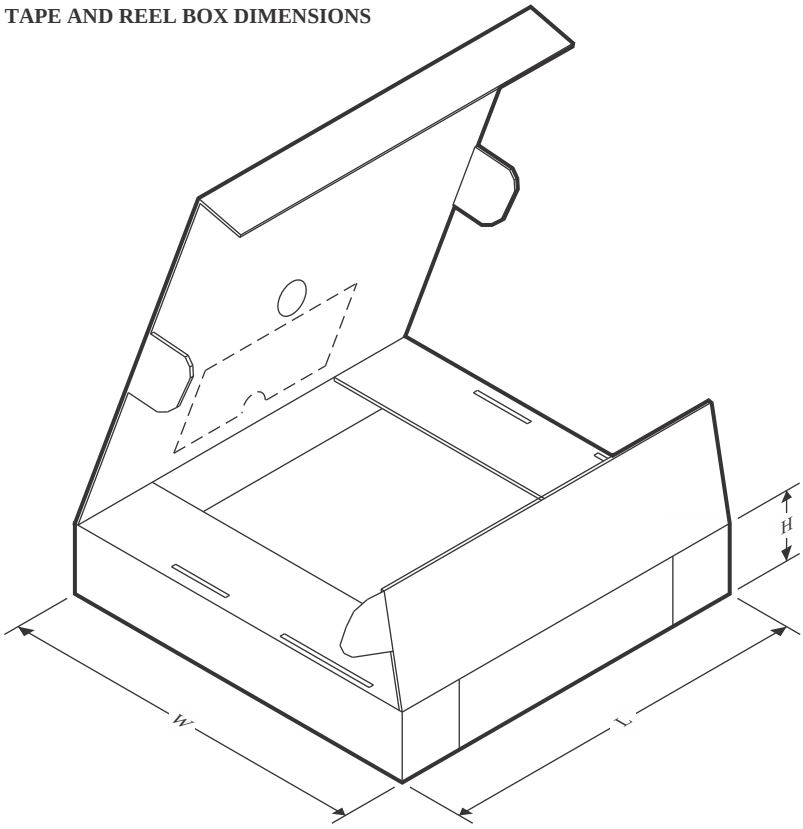
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1T34DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1T34DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1T34DSFR | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

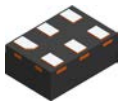
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUP1T34DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1T34DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1T34DSFR | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |

# DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

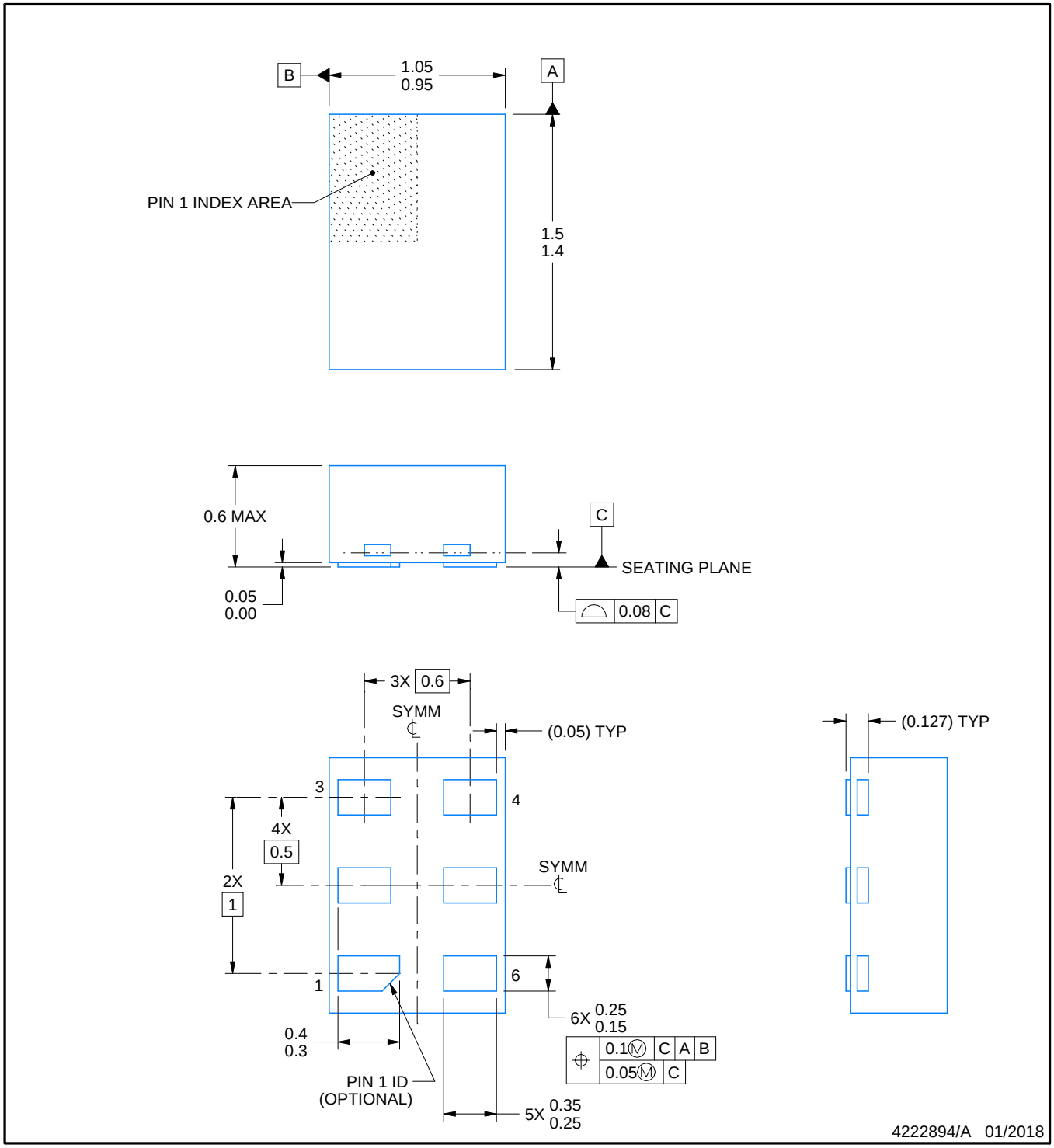
# DRY0006A



# PACKAGE OUTLINE

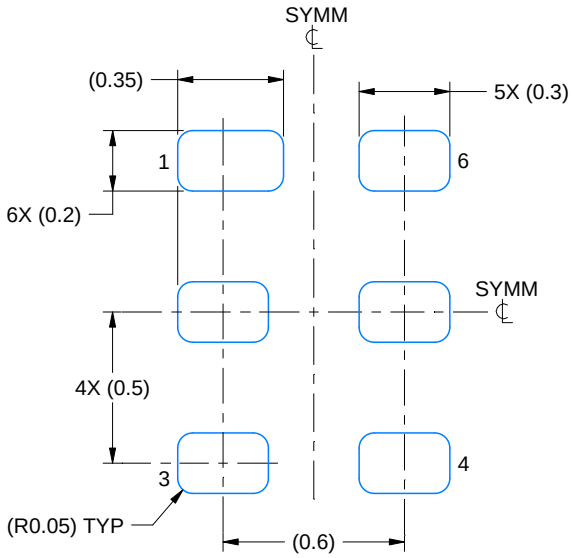
## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

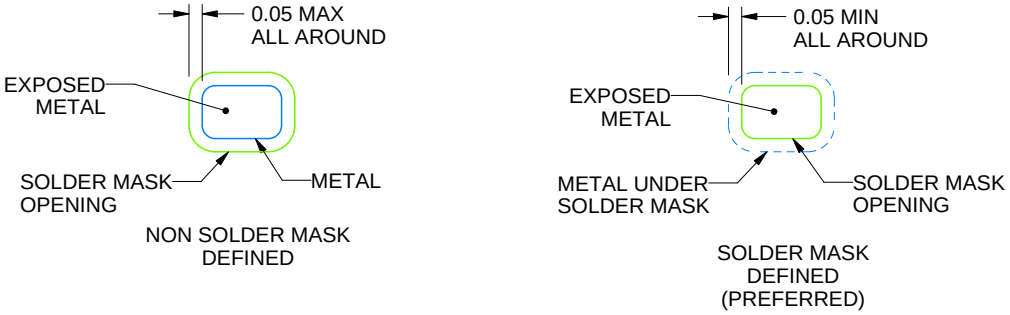



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

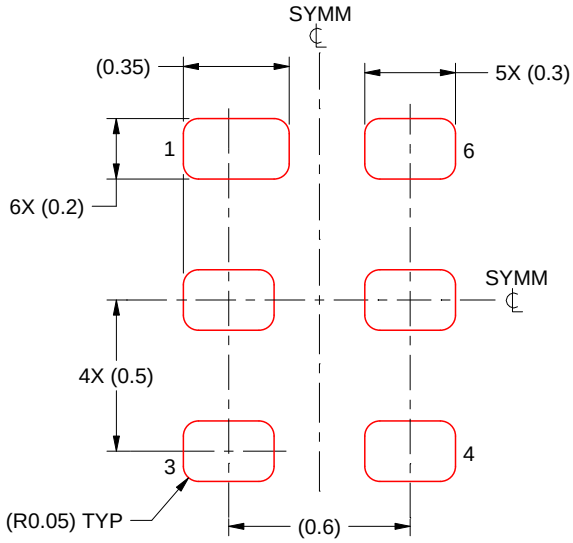
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DRY0006A

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

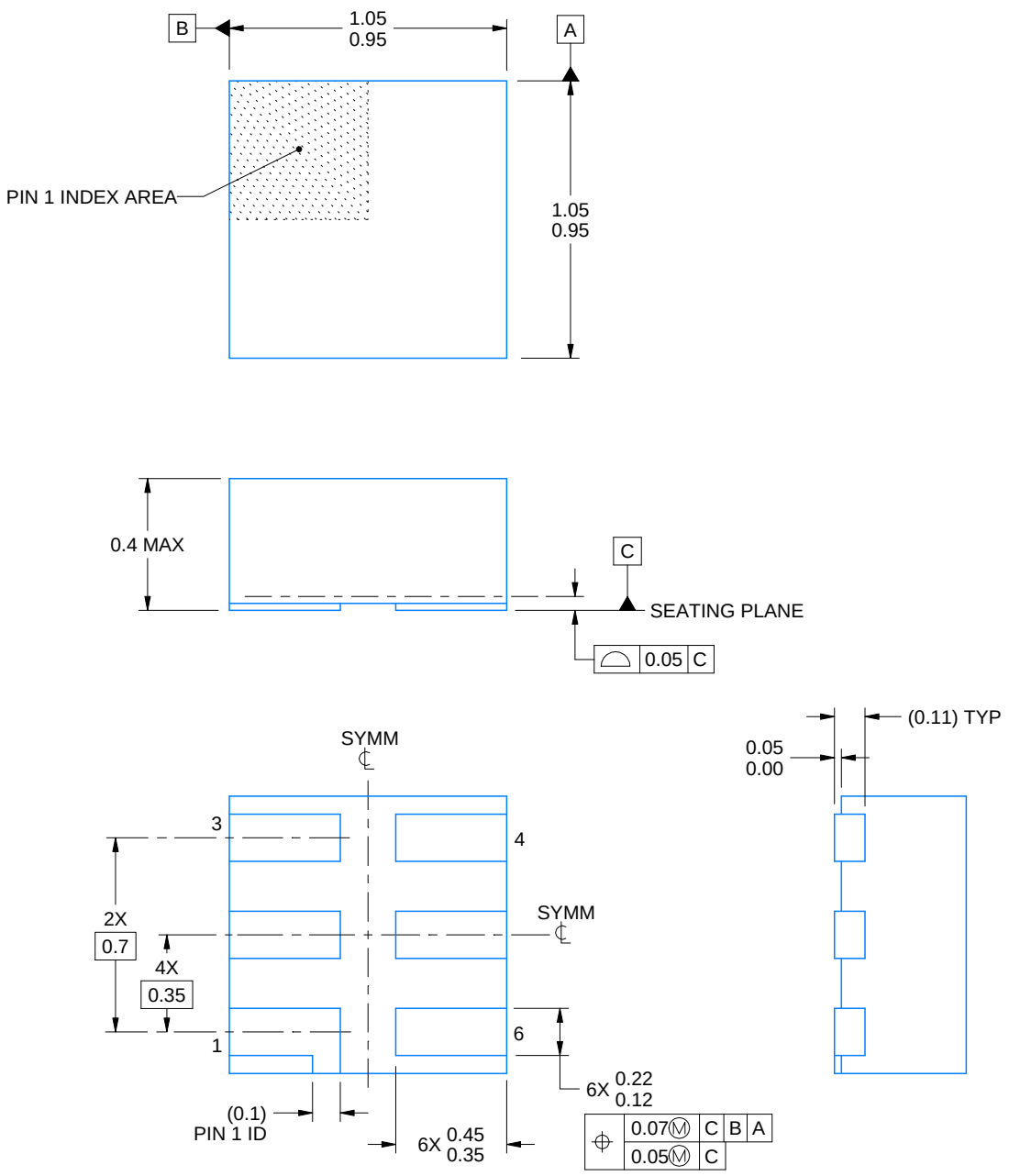
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DSF0006A

## X2SON - 0.4 mm max height

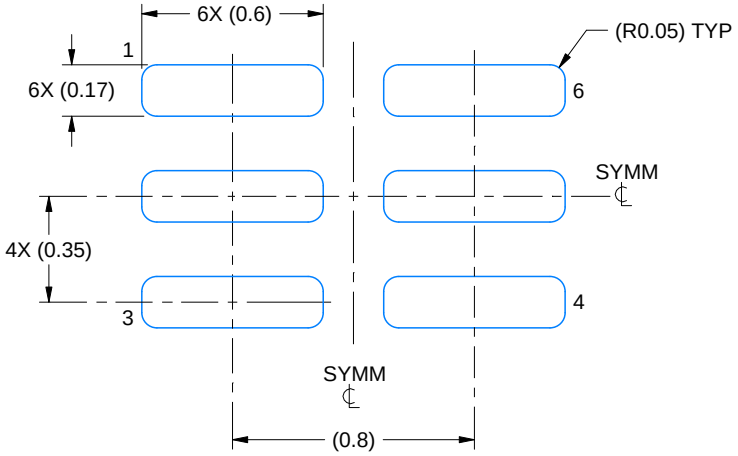
PLASTIC SMALL OUTLINE - NO LEAD



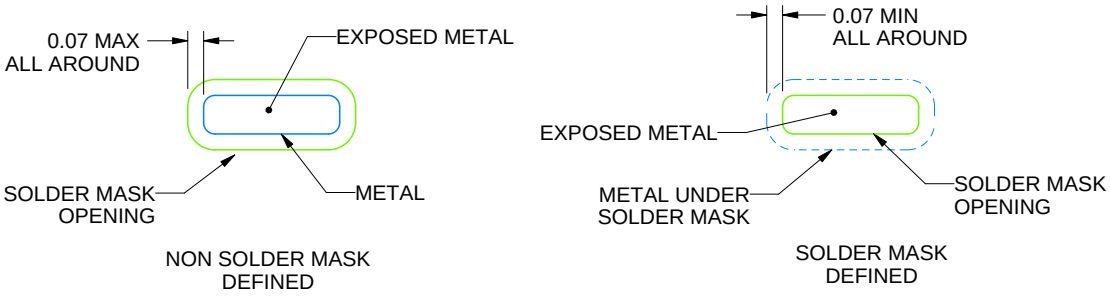

4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

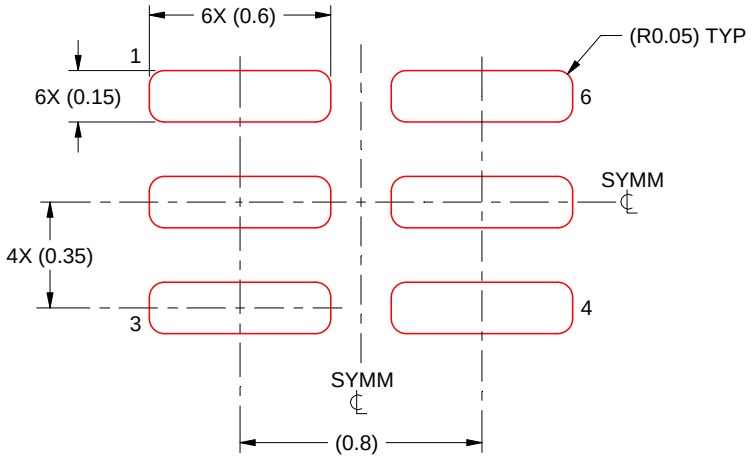
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

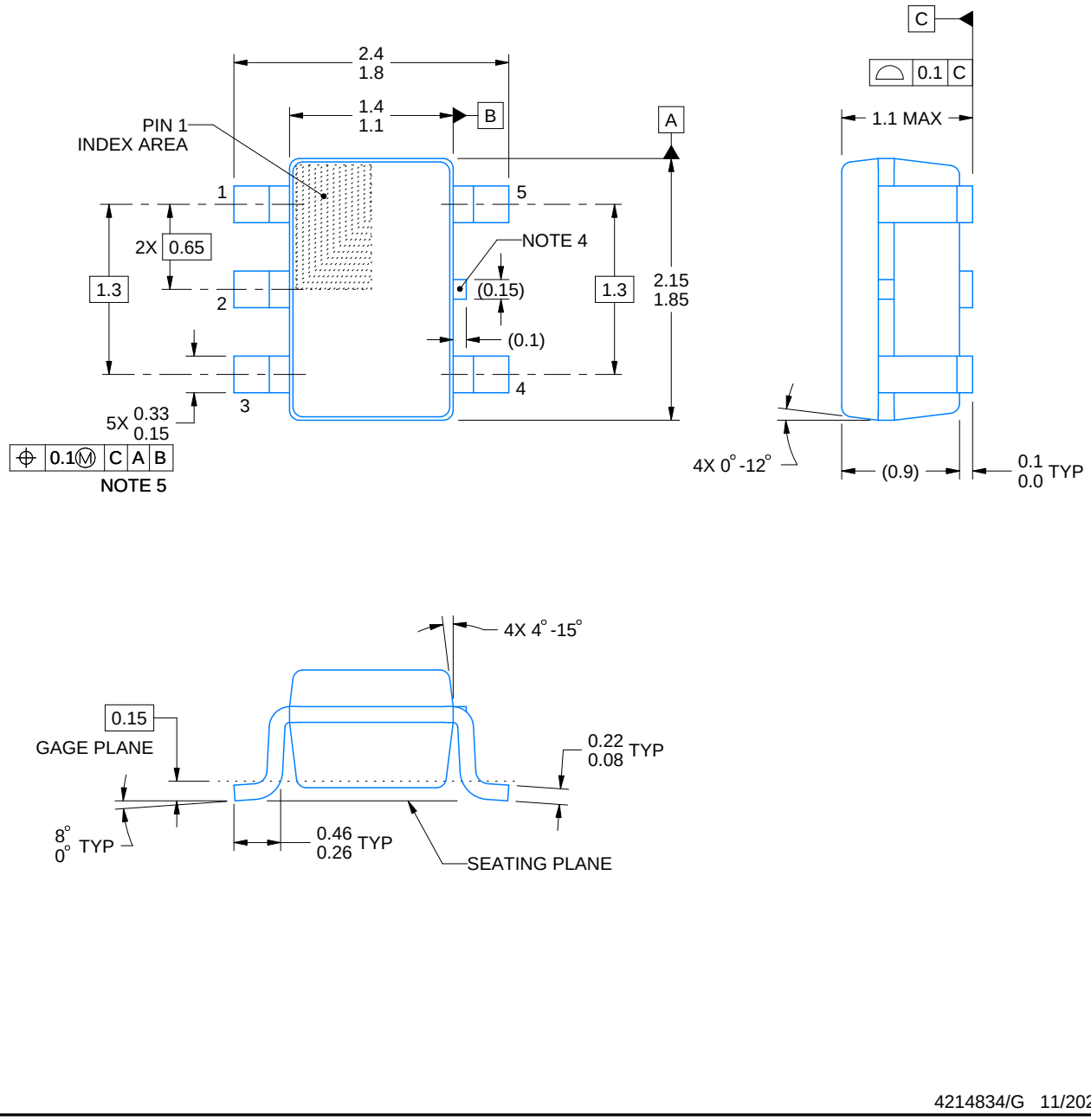
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

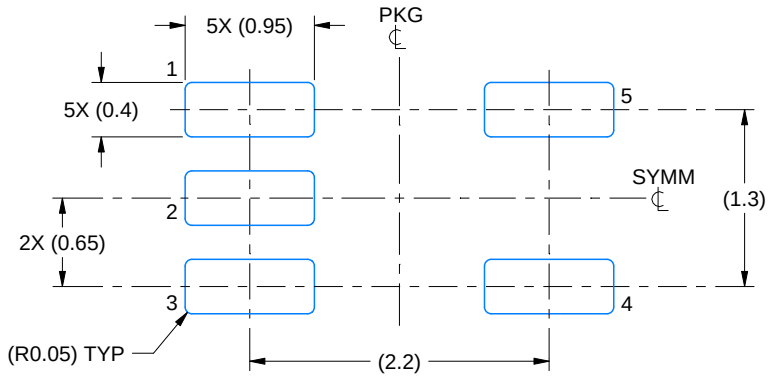
SMALL OUTLINE TRANSISTOR



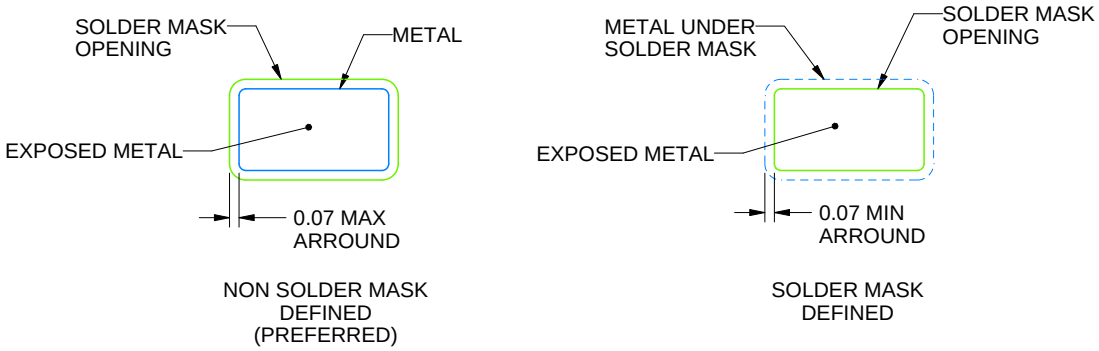

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

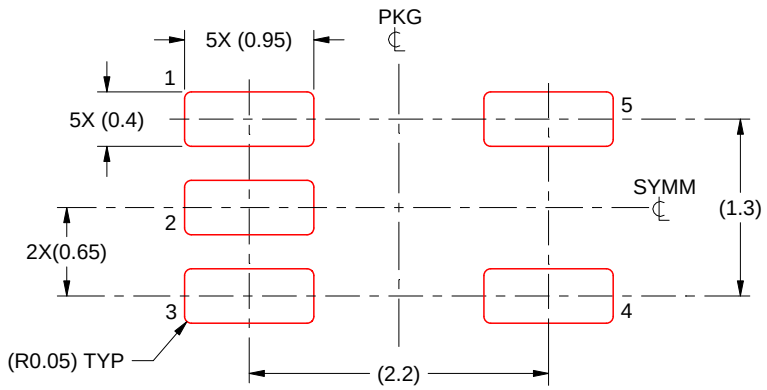



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265