

SN74AHC125Q 車載用、3 ステート出力、クワッドバスバッファゲート

1 特長

- Q デバイスは、車載性能要件を満たしています
- お客様固有の構成の管理は、大幅変更承認によって対応可能
- EPIC™ (Enhanced-Performance Implanted CMOS) プロセス
- 2V~5.5V の V_{CC} で動作
- JESD 17 準拠で 250mA 超のラッチアップ性能

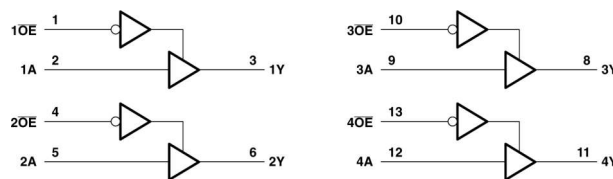
2 概要

SN74AHC125Q は、3 ステート出力の独立ラインドライバを備えたクワッドバスバッファゲートです。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージサイズ ⁽²⁾	本体サイズ ⁽³⁾
SN74AHC125Q	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



論理図 (正論理)



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3 Pin Configuration and Functions

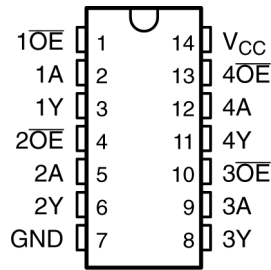


図 3-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

表 3-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1 OE	1	I	Output enable
1A	2	I	Input
1Y	3	O	Output
2 OE	4	I	Output enable
2A	5	I	Input
2Y	6	O	Output
3 OE	8	I	Output enable
3A	9	I	Input
3Y	10	I	Output
4 OE	13	I	Output enable
4A	12	I	Input
4Y	11	O	Output
GND	7	—	Ground
V _{CC}	14	I	Supply voltage

(1) I = input, O = output

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I ⁽²⁾	Input voltage range	-0.5	7	V
V _O ⁽²⁾	Output voltage range	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current (V _I < 0)		-20	mA
I _{OK}	Output clamp current (V _O < 0 or V _O > V _{CC})		±20	mA
I _O	Continuous output current (V _O = 0 to V _{CC})		±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 3 V	2.1	
		V _{CC} = 5.5 V	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 3 V	0.9	
		V _{CC} = 5.5 V	1.65	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	μA
		V _{CC} = 3.3 V ± 0.3 V	-4	mA
		V _{CC} = 5 V ± 0.5 V	-8	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 3.3 V ± 0.3 V	4	mA
		V _{CC} = 5 V ± 0.5 V	8	
Δt/Δv	input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	ns/V
		V _{CC} = 5 V ± 0.5 V	20	
T _A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC	SN74AHC125Q		UNIT	
	D (SOIC)	PW (TSSOP)		
	14 PINS	14 PINS		
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	86	113	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA		2 V	1.9	2		1.9	V	
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
	I _{OH} = -4 mA		3 V	2.58		2.48			
	I _{OH} = -8 mA		4.5 V	3.94		3.8			
V _{OL}	I _{OL} = 50 μA		2 V			0.1	0.1	V	
			3 V			0.1	0.1		
			4.5 V			0.1	0.1		
	I _{OL} = 4 mA		3 V			0.36	0.5		
	I _{OL} = 8 mA		4.5 V			0.36	0.5		
I _I	V _I = 5.5 V or GND		0 V to 5.5 V			±0.1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND		5.5 V			±0.25	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0		5.5 V			4	40	μA	
C _i	V _I = V _{CC} or GND		5 V		4	10		pF	

4.5 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15 pF		5.6	8	1	9.5	ns
t _{PHL}					5.6	8	1	9.5	
t _{PZH}	OE	Y	C _L = 15 pF		5.4	8	1	9.5	ns
t _{PZL}					5.4	8	1	9.5	
t _{PHZ}	OE	Y	C _L = 15 pF		7	9.7	1	11.5	ns
t _{PLZ}					7	9.7	1	11.5	
t _{PLH}	A	Y	C _L = 50 pF		8.1	11.5	1	13	ns
t _{PHL}					8.1	11.5	1	13	
t _{PZH}	OE	Y	C _L = 50 pF		7.9	11.5	1	13	ns
t _{PZL}					7.9	11.5	1	13	
t _{PHZ}	OE	Y	C _L = 50 pF		9.5	13.2	1	15	ns
t _{PLZ}					9.5	13.2	1	15	

4.6 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15 pF		3.8	5.5	1	6.5	ns
t _{PHL}					3.8	5.5	1	6.5	
t _{PZH}	OE	Y	C _L = 15 pF		3.6	5.1	1	6	ns
t _{PZL}					3.6	5.1	1	6	

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 over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PHZ}	OE	Y	$C_L = 15\text{ pF}$		4.6	6.8	1	8	ns
t_{PLZ}					4.6	6.8	1	8	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	
t_{PZH}	OE	Y	$C_L = 50\text{ pF}$		5.1	7.1	1	8	ns
t_{PZL}					5.1	7.1	1	8	
t_{PHZ}	OE	Y	$C_L = 50\text{ pF}$		6.1	8.8	1	10	ns
t_{PLZ}					6.1	8.8	1	10	

4.7 Noise Characteristics

 $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (1)

PARAMETER		MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

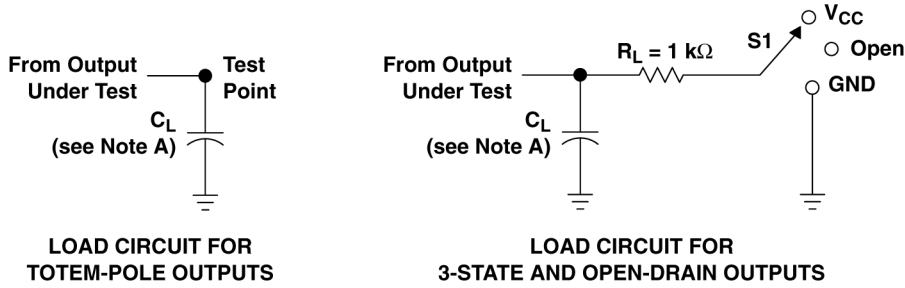
(1) Characteristics are for surface-mount packages only.

4.8 Operating Characteristics

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

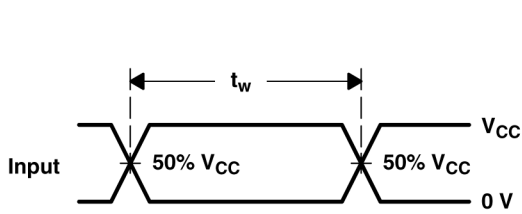
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	No load, $f = 1\text{ MHz}$	14	pF

5 Parameter Measurement Information

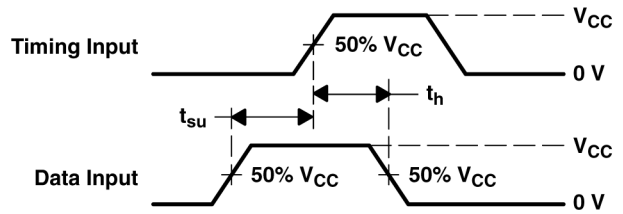


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

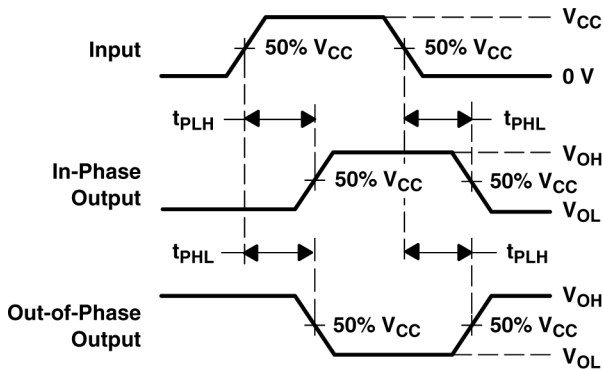
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



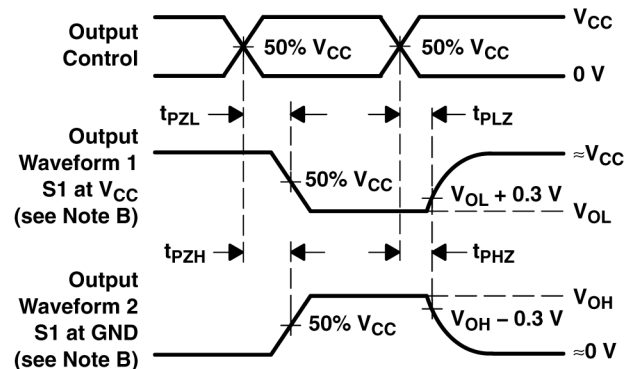
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

5-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

6 Detailed Description

6.1 Overview

Each output is disabled when the associated output-enable (\overline{OE}) input is high. When \overline{OE} is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6.2 Functional Block Diagram

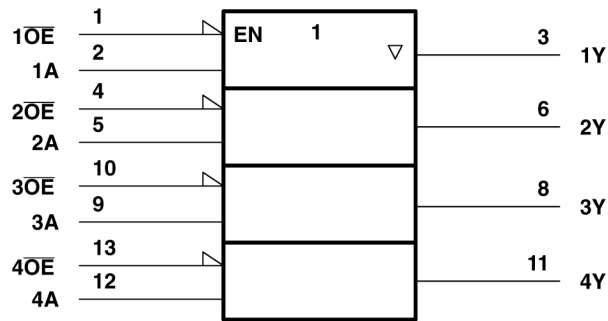


图 6-1. Logic Symbol

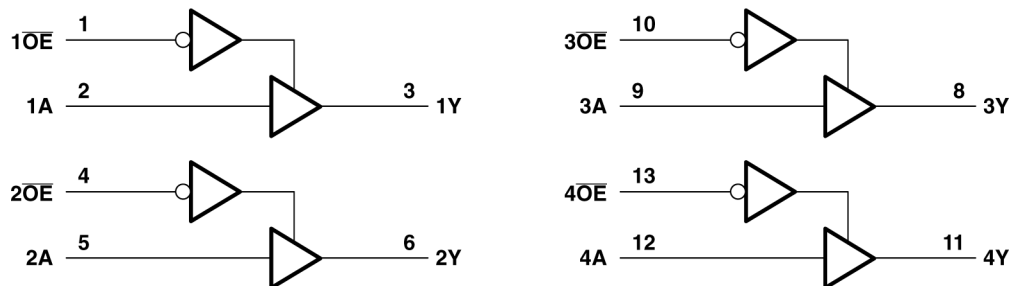


图 6-2. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

表 6-1. Function Table
(Each Buffer)

INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

7 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツはその正確性も完全性も保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.2.2 Layout Example

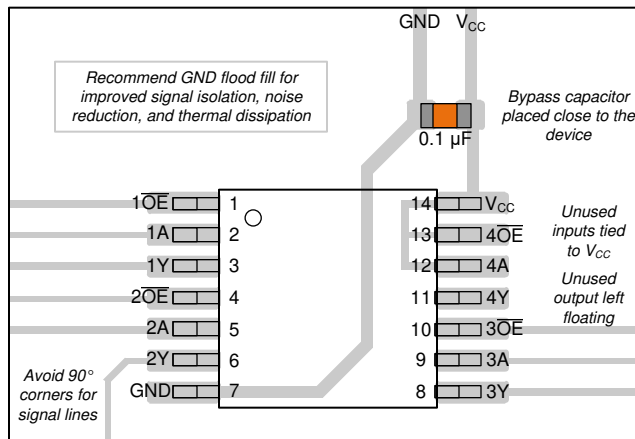


図 7-1. Example Layout for the SN74AHC125Q

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC125Q	Click here	Click here	Click here	Click here	Click here

8.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.3 Trademarks

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8.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2002) to Revision A (December 2024)

Page

<ul style="list-style-type: none"> 「パッケージ情報」の表、「ピンの機能」の表、「熱に関する情報」の表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加 	1
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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC125QPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125Q	Samples
SN74AHC125QPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC125QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125QPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC125QPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC125QPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC125QPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

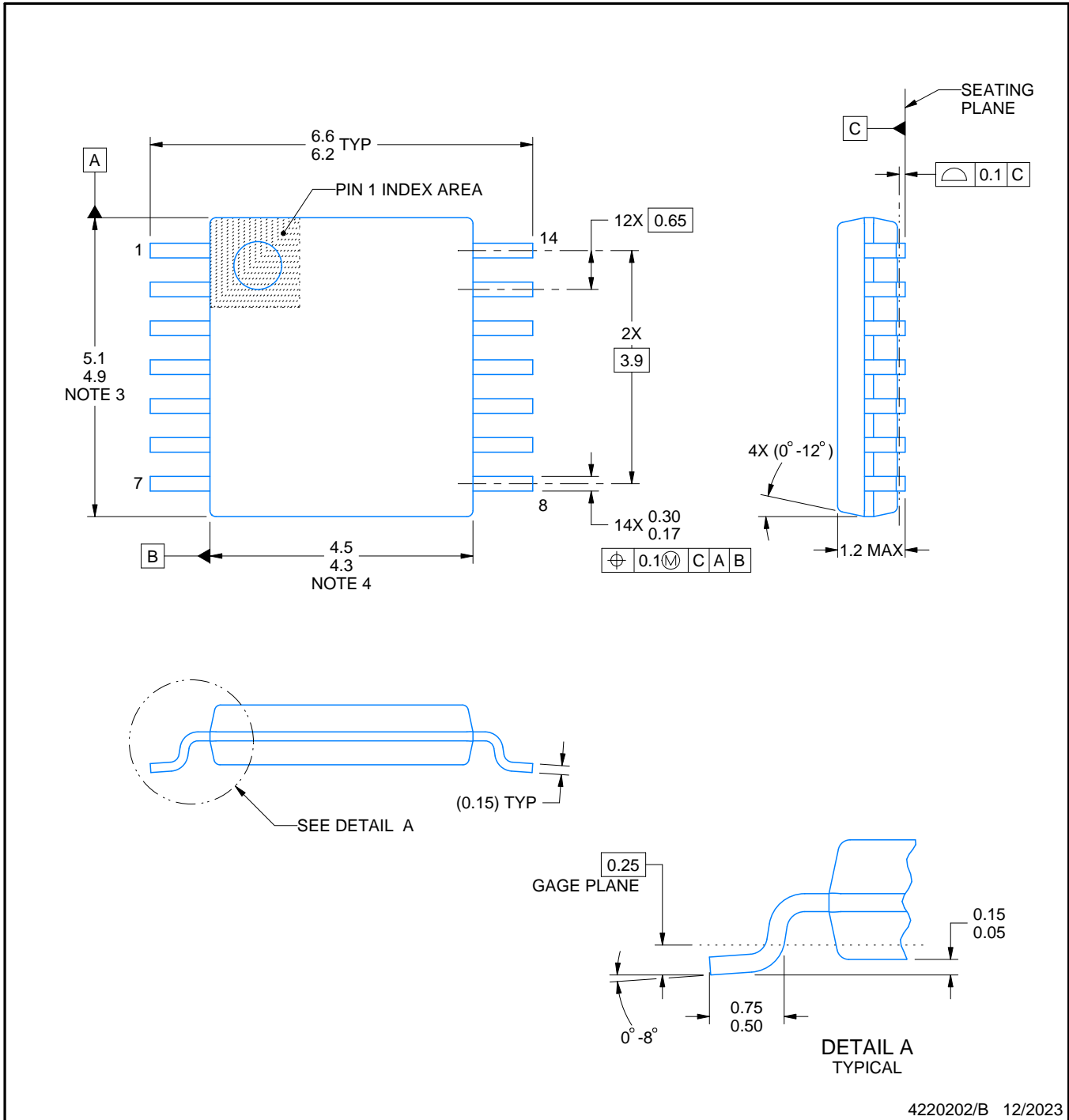
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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