

SN65C1168E-SEP $\pm 12\text{kV}$ ESD 保護機能搭載、デュアル差動ドライバ / レシーバ

1 特長

- VID V62/19606
- 放射線耐性を強化
 - シングル・イベント・ラッチアップ (SEL) 耐性: 125°C で $43\text{MeV}\cdot\text{cm}^2/\text{mg}$ まで
 - $30\text{krad}(\text{Si})$ まで ELDRS なし
 - すべてのウェハー・ロットについて、 $20\text{krad}(\text{Si})$ までの吸収線量 (TID) RLAT (Radiation Lot Acceptance Test)
- 宇宙向けに強化されたプラスチック
 - 管理されたベースライン
 - 金線
 - NiPdAu リード仕上げ
 - 単一のアセンブリ/テスト施設
 - 単一の製造施設
 - 軍用温度範囲 ($-55^\circ\text{C}\sim 125^\circ\text{C}$) で利用可能
 - 長い製品ライフ・サイクル
 - 製品変更通知期間の延長
 - 製品のトレーサビリティ
 - モールド・コンパウンドの改良による低いガス放出
- TIA/EIA-422-B および ITU Recommendation V.11 適合以上の性能
- 5V 単一電源で動作
- RS-422 バス・ピン用 ESD 保護機能
 - $\pm 12\text{kV}$ 人体モデル (HBM)
 - $\pm 8\text{kV}$ IEC 61000-4-2、接触放電
 - $\pm 8\text{kV}$ IEC 61000-4-2、エアギャップ放電

- 低パルス・スキュー
- レシーバ入力インピーダンス: $17\text{k}\Omega$ (標準値)
- レシーバ入力感度: $\pm 200\text{mV}$
- レシーバ同相入力電圧範囲: $-7\text{V}\sim 7\text{V}$
- グリッチ・フリーのパワーアップ / パワーダウン 保護機能

2 アプリケーション

- 低軌道衛星用途のサポート
- 衛星通信
- AC / サーボ・モータ・ドライブ

3 概要

SN65C1168E-SEP はデュアル・ドライバとデュアル・レシーバで構成されており、RS-422 バス・ピンを $\pm 12\text{kV}$ の ESD (HBM) と $\pm 8\text{kV}$ の ESD (IEC61000-4-2 エアギャップ放電および接触放電) から保護できます。このデバイスは、TIA/EIA-422-B および ITU Recommendation V.11 の要件を満たしていますが、TID で $20\text{krad}(\text{Si})$ 照射後には、すべてのパラメータが TIA/EIA-422-B および ITU Recommendation V.11 のすべての要件を満たしているわけではありません。

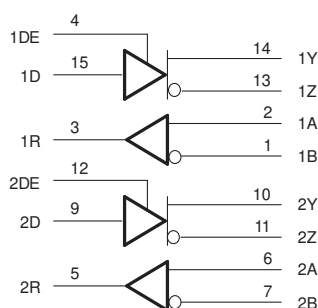
製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
SN65C1168EMPWTSEP	TSSOP (16)	5.00mmx4.40mm
SN65C1168EMPWSEP		

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図

SN65C1168E-SEP



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4 改訂履歴

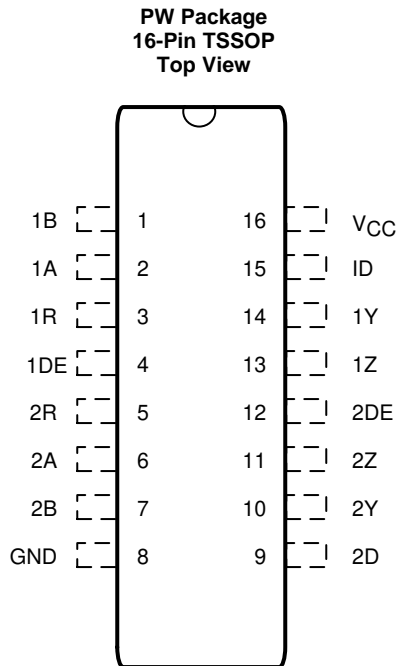
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2019年7月	*	初版

5 Description

SN65C1168E-SEP のドライバは、それぞれアクティブ HIGH イネーブルを備えています。

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	RS422 differential input (noninverting) to receiver 1
2A	6	I	RS422 differential input (noninverting) to receiver 2
1B	1	I	RS422 differential input (inverting) to receiver 1
2B	7	I	RS422 differential input (inverting) to receiver 2
1D	15	I	Logic data input to RS422 driver 1
2D	9	I	Logic data input to RS422 driver 2
1DE	4	I	Driver 1 enable (active high)
2DE	12	I	Driver 2 enable (active high)
GND	8	—	Device ground
1R	3	O	Logic data output of RS422 receiver 1
2R	5	O	Logic data output of RS422 receiver 2
V _{CC}	16	—	Power supply
1Y	14	O	RS-422 differential (noninverting) driver output 1
2Y	10	O	RS-422 differential (noninverting) driver output 2
1Z	13	O	RS-422 differential (noninverting) driver output 1
2Z	11	O	RS-422 differential (noninverting) driver output 2

7 Specifications

7.1 Absolute Maximum Ratings

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage ⁽²⁾	-0.5	7	V	
V _I	Input voltage	Driver, DE, RE	-0.5	7	V
		A or B, Receiver	-14	14	
V _{ID}	Differential input voltage ⁽³⁾	Receiver	-14	14	V
V _O	Output voltage	Driver	-0.5	7	V
		Receiver	-0.5	V _{CC} + 0.5	
I _{IK}	Input clamp current	Driver, V _I < 0		-20	mA
I _{OK}	Output clamp current	Driver, V _O < 0		-20	mA
		Receiver	-20	20	
I _O	Output current	Driver	-150	150	mA
		Receiver	-25	25	
I _{CC}	Supply current		200	mA	
	GND current		-200	mA	
T _J	Operating virtual junction temperature		150	°C	
T _{stg}	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential input voltage are with respect to the network GND.
- (3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.

7.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±12000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
		IEC 61000-4-2, air-gap discharge	±8000	
		IEC 61000-4-2, contact discharge	±8000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IC}	Common-mode input voltage ⁽¹⁾	Receiver			±7	V
V _{ID}	Differential input voltage	Receiver			±7	V
V _I	Input voltage	Except A, B	0		5.5	V
V _O	Output voltage	Receiver	0		V _{CC}	V
V _{IH}	High-level input voltage	Except A, B	2			V
V _{IL}	Low-level input voltage	Except A, B			0.8	V
I _{OH}	High-level output current	Receiver			-6	mA
		Driver			-20	
I _{OL}	Low-level output current	Receiver			6	mA
		Driver			20	
T _A	Operating free-air temperature		-55		125	°C

(1) Refer to TIA/EIA-422-B for exact conditions.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN65C1168E-SEP		UNIT
	PW (TSSOP)		
	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	102.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	32.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	48.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	48.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Driver Section Electrical Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
V_{OH}	High-level output voltage	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -20 \text{ mA}$		2.4	3.5		V
V_{OL}	Low-level output voltage	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$			0.2	0.4	V
$ V_{OD1} $	Differential output voltage 1	$I_O = 0 \text{ mA}$		2		6	V
$ V_{OD2} $	Differential output voltage 2	$R_L = 100 \Omega$, see Figure 1 ⁽²⁾		2	3.7		V
$\Delta V_{OD} $	Change in magnitude of differential output voltage	$R_L = 100 \Omega$, see Figure 1 ⁽²⁾		-0.4		0.4	V
V_{OC}	Common-mode output voltage	$R_L = 100 \Omega$, see Figure 1 ⁽²⁾		-3		3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage	$R_L = 100 \Omega$, see Figure 1 ⁽²⁾		-0.4		0.4	V
$I_{O(OFF)}$	Output current with power off	$V_{CC} = 0 \text{ V}$	$V_O = 6 \text{ V}$			100	μA
			$V_O = -0.25 \text{ V}$			100	
$I_{O(OFF)}$	Output current with power off ⁽³⁾	$V_{CC} = 0 \text{ V}$	$V_O = 6 \text{ V}$			3	mA
			$V_O = -0.25 \text{ V}$			3	
I_{OZ}	High-impedance-state output current		$V_O = 2.5 \text{ V}$			20	μA
			$V_O = 5 \text{ V}$			-20	
I_{OZ}	High-impedance-state output current ⁽³⁾		$V_O = 2.5 \text{ V}$			2	mA
			$V_O = 5 \text{ V}$			-2	
I_{IH}	High-level input current	$V_I = V_{CC}$ or V_{IH}				1	μA
I_{IL}	Low-level input current	$V_I = \text{GND}$ or V_{IL}				-36	μA
I_{OS}	Short-circuit output current	$V_O = V_{CC}$ or GND ⁽⁴⁾		-30		-160	mA
I_{CC}	Supply current (total package)	No load, Enabled	$V_I = V_{CC}$ or GND		4	6	mA
			$V_I = 2.4$ or 0.5 V ⁽⁵⁾		5	9	
I_{CC}	Supply current (total package) ⁽³⁾	No load, Enabled	$V_I = V_{CC}$ or GND			17	mA
			$V_I = 2.4$ or 0.5 V ⁽⁵⁾			16	
C_i	Input capacitance				6		pF

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) Refer to TIA/EIA-422-B for exact conditions.

(3) 25°C only. Post 20-krad(Si) HDR TID using worst case static biasing.

(4) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

(5) This parameter is measured per input, while the other inputs are at V_{CC} or GND .

7.6 Receiver Section Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IT+}	Positive-going input threshold voltage, differential input				0.2	V	
V_{IT-}	Negative-going input threshold voltage, differential input		-0.2 ⁽²⁾			V	
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			60		mV	
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -6$ mA	3.8	4.2		V	
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = 6$ mA		0.1	0.3	V	
I_I	Line input current	Other input at 0 V	$V_I = 10$ V		1.5	mA	
			$V_I = -10$ V		-2.5		
r_I	Input resistance	$V_{IC} = -7$ V to 7 V, other input at 0 V	4	17		k Ω	
I_{CC}	Supply current (total package)	No load, Enabled	$V_I = V_{CC}$ or GND		4	6	mA
			$V_I = 2.4$ V or 0.5 V ⁽³⁾		5	9	
I_{CC}	Supply current (total package) ⁽⁴⁾	No load	$V_I = V_{CC}$ or GND		17	mA	
			$V_I = 2.4$ or 0.5 V ⁽⁵⁾		16		

(1) All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$.

(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) Refer to TIA/EIA-422-B for exact conditions.

(4) 25°C only. Post 20-krad(Si) HDR TID using worst case static biasing.

(5) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

7.7 Driver Section Switching Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R1 = R2 = 50 Ω , R3 = 500 Ω , C1 = C2 = C3 = 40 pF, S1 is open, see Figure 2		8	16	ns
t_{PLH}	Propagation delay time, low- to high-level output			8	16	ns
$t_{sk(p)}$	Pulse skew			1.5	4	ns
t_r	Rise time	R1 = R2 = 50 Ω , R3 = 500 Ω , C1 = C2 = C3 = 40 pF, S1 is open, see Figure 3		5	8	ns
t_f	Fall time			5	8	ns
t_{PZH}	Output-enable time to high level	R1 = R2 = 50 Ω , R3 = 500 Ω , C1 = C2 = C3 = 40 pF, S1 is closed, see Figure 4		10	19	ns
t_{PZL}	Output-enable time to low level			10	19	ns
t_{PHZ}	Output-disable time from high level	R1 = R2 = 50 Ω , R3 = 500 Ω , C1 = C2 = C3 = 40 pF, S1 is closed, see Figure 4		7	16	ns
t_{PLZ}	Output-disable time from low level			7	16	ns
f_{SW}	Maximum switching frequency	R1 = R2 = 50 Ω , R3 = 500 Ω , C1 = C2 = C3 = 40 pF, S1 is open, see Figure 3	20			MHz

(1) All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$.

7.8 Receiver Section Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 5	9	15	27	ns
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 5	9	15	27	ns
t_{TLH}	Transition time, low- to high-level output	$V_{IC} = 0\text{ V}$, see Figure 5		4	9	ns
t_{PHL}	Transition time, high- to low-level output			4	9	ns

- (1) Measured per input while the other inputs are at V_{CC} or GND.
 (2) All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

8 Parameter Measurement Information

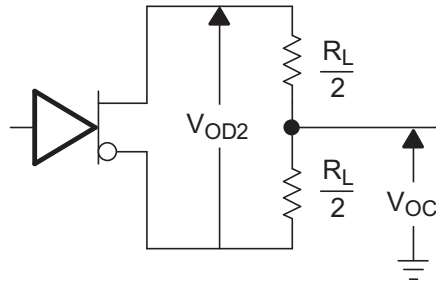
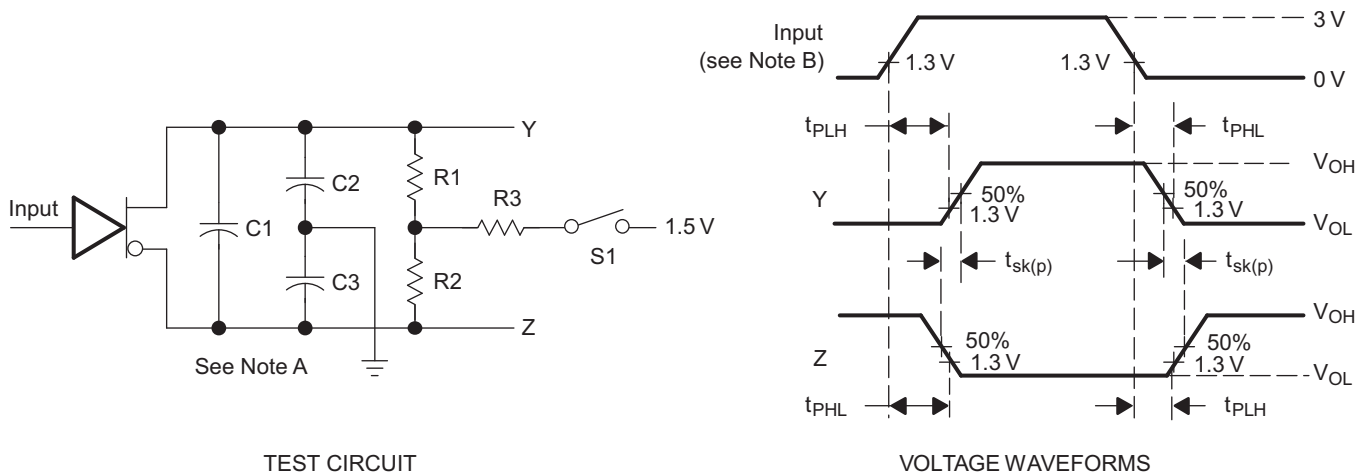
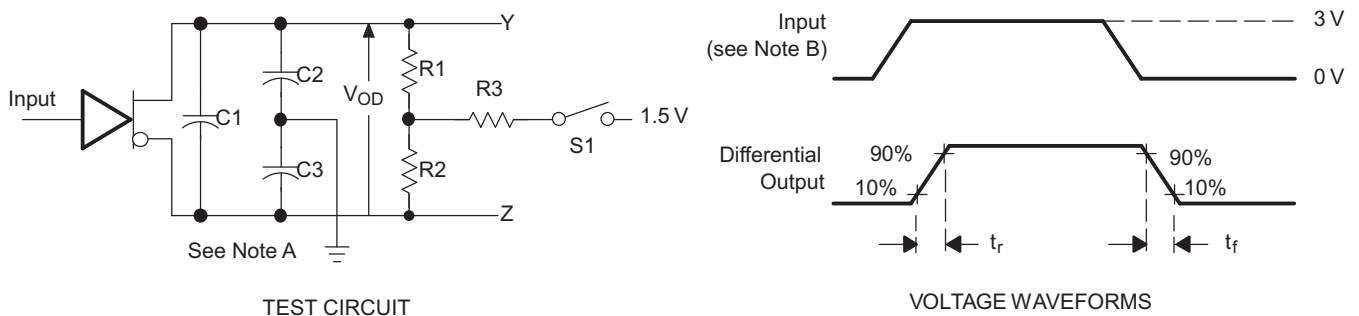


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

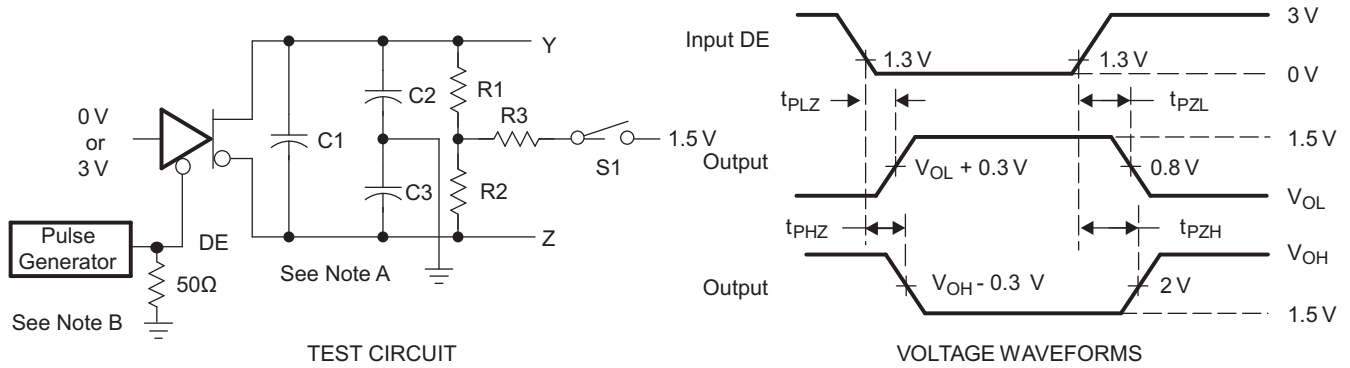
Figure 2. Driver Test Circuit and Voltage Waveforms



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

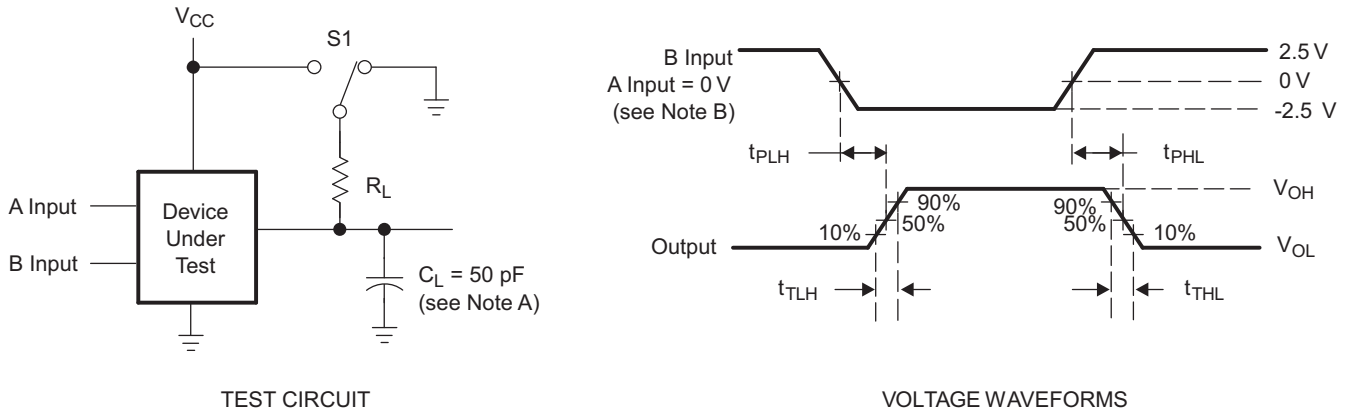
Figure 3. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

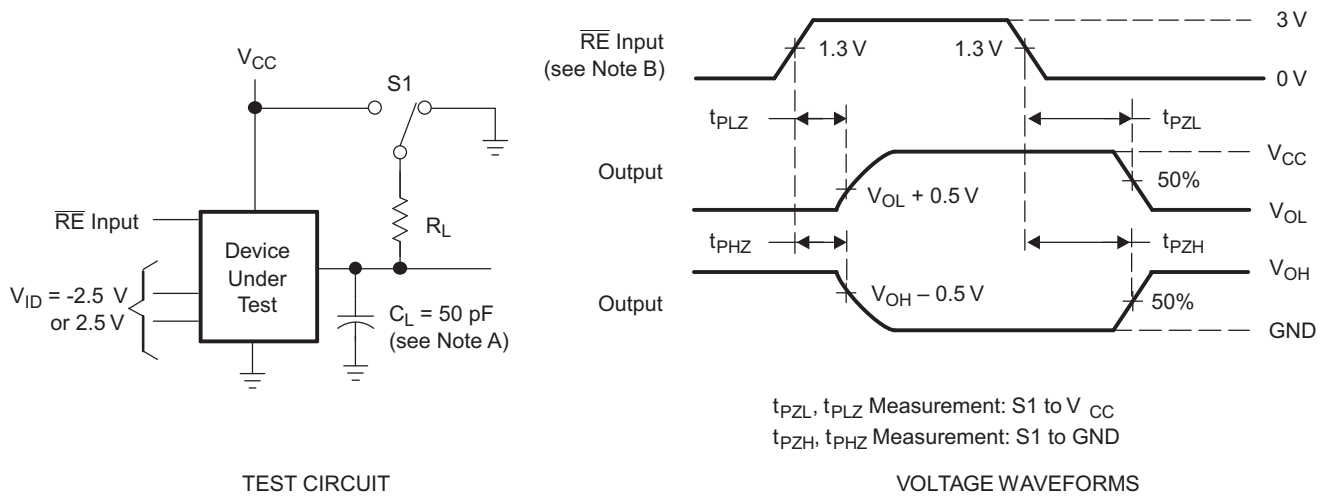
Figure 4. Driver Test Circuit and Voltage Waveforms



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 5. Receiver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

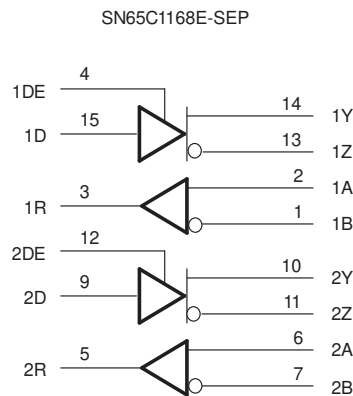
Figure 6. Receiver Test Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN65C1168E-SEP consist of dual drivers and dual receivers powered from a single 5-V supply. This device meets the requirements of TIA/EIA-422-B and ITU recommendation V.11.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Active High Driver Output Enables

SN65C1168E-SEP drivers can be configured individually by 1DE and 2DE logic inputs. Both drivers are set at high-impedance when disabled.

9.4 Device Functional Modes

Table 1 and Table 2 lists the functional modes of SN65C1168E-SEP.

Table 1. Each Driver⁽¹⁾

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = High level, L = Low level, X = Irrelevant, Z = High impedance (off)

Table 2. Each Receiver⁽¹⁾

DIFFERENTIAL INPUTS A-B	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$?
$V_{ID} \leq -0.2 \text{ V}$	L
Open	H

(1) H = High level, L = Low level, ? = Indeterminate

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Figure 7 shows a typical RS-422 application. One transmitter is able to broadcast to multiple receiving nodes connected together over a shared differential bus. Twisted-pair cabling with a controlled differential impedance is used, and a termination resistance is placed at the farthest receive end of the cable in order to match the transmission line impedance and minimize signal reflections.

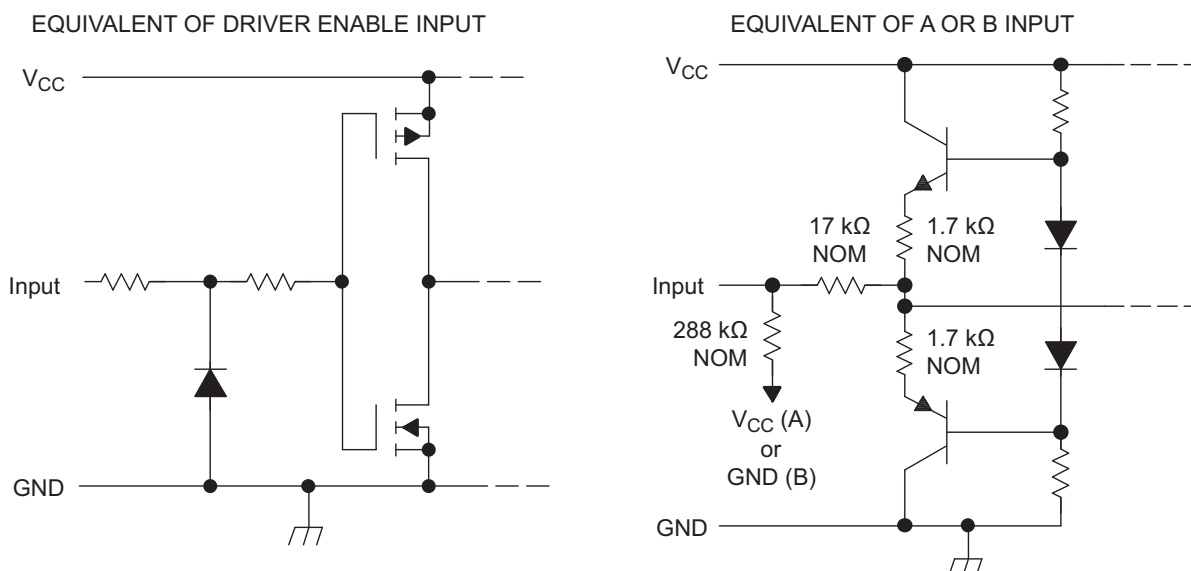


Figure 7. Schematic of Inputs

Application Information (continued)

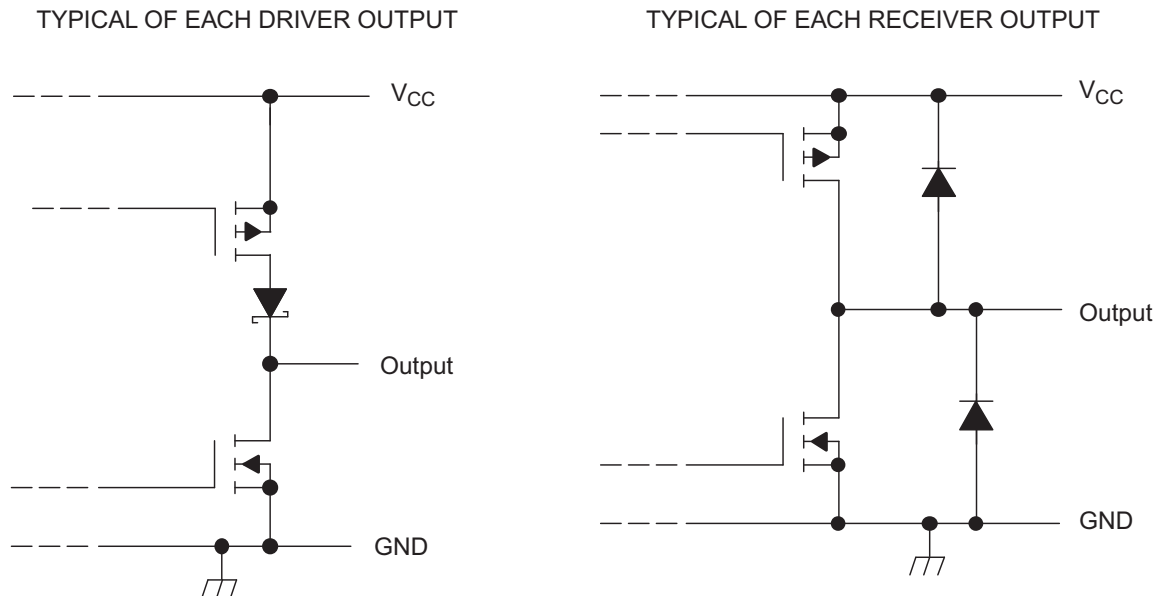


Figure 8. Schematic of Outputs

10.2 Typical Application

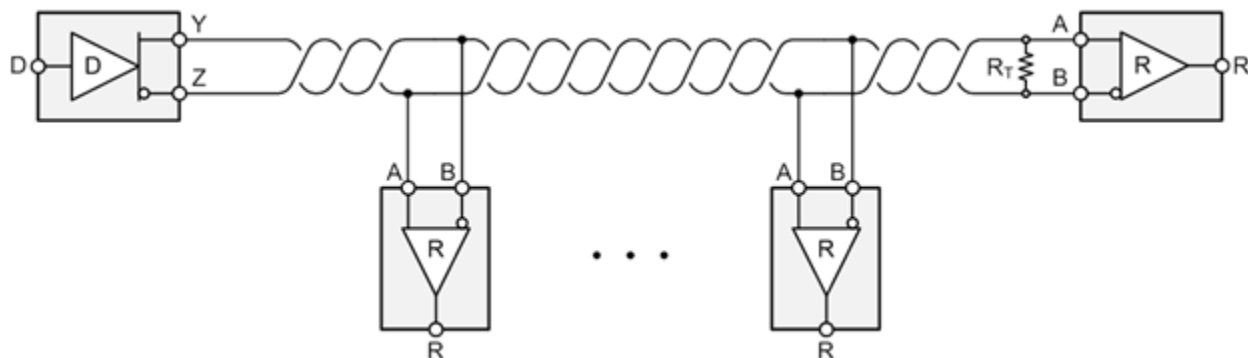


Figure 9. Typical RS-422 Application

10.2.1 Design Requirements

A typical RS-422 implementation using SN65C116xE requires the following:

- 5-V power source.
- Connector that ensures the correct polarity for port pins.
- Cabling that supports the desired operating rate and transmission distance.

10.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure ± 200 mV on the A-B port when the driver circuit is disabled.

11 Power Supply Recommendations

Use a 5-V power supply for V_{CC} place 0.1- μ F bypass capacitors close to the power supply pins to reduce errors coupling in from noisy or high impedance power supplies.

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

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12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C1168EMPWSEP	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	1168SEP	Samples
SN65C1168EMPWTSEP	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	1168SEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C1168EMPWTSEP	TSSOP	PW	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C1168EMPWTSEP	TSSOP	PW	16	250	210.0	185.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C1168EMPWSEP	PW	TSSOP	16	90	530	10.2	3600	3.5



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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