

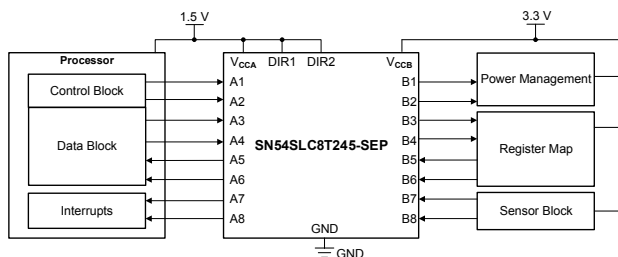
# SN54SLC8T245-SEP 8 ビット、デュアル電源バス・トランシーバ、構成可能な電圧変換およびトリステート出力搭載

## 1 特長

- VID V62/22604
- 耐放射線特性:
  - 125°Cにおいて 43MeV-cm<sup>2</sup>/mg のシングル・イベント・ラッチアップ (SEL) 耐性
  - すべてのウェハー・ロットについて、20krad(Si) までの吸収線量 (TID) RLAT (Radiation Lot Acceptance Test)
- 認定済みの完全に構成可能なデュアル・レール設計により、各ポートは 0.65V~3.6V の範囲の電源電圧で動作可能
- 動作温度範囲: -55°C~+125°C
- 複数の方向制御ピンにより、昇圧と降圧の変換を同時に実行
- 1.8V から 3.3V への変換時に最高 380Mbps をサポート
- 電源オフ時に 2 つのバスを実質的に絶縁する V<sub>CC</sub> 絶縁機能
- 部分的パワーダウン・モードにより、電源オフ時に電流の逆流を制限
- JESD 78, Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 人体モデルで 8000V
  - デバイス帯電モデルで 1000V

## 2 アプリケーション

- 低軌道 (LEO) 衛星用途のサポート
- 宇宙用レーダーおよび通信
- 人工衛星のペイロード



代表的なアプリケーション回路図

## 3 概要

SN54SLC8T245-SEP デバイスは、8 ビットの非反転バス・トランシーバで、最新の電圧ノード (0.7V、0.8V、0.9V) で動作しているデバイスと、業界標準の電圧ノード (1.8V、2.5V、3.3V) で動作しているデバイスとの間で、電圧レベル不一致の問題を双方向に解決できます。

このデバイスは、2 つの独立した電源レール (V<sub>CCA</sub> および V<sub>CCB</sub>) を使用し、最低 0.65V で動作します。データ・ピン A1 から A8 までは V<sub>CCA</sub> に追従するように設計されており、0.65V~3.6V の任意の電源電圧を受け付けます。データ・ピン B1 から B8 までは V<sub>CCB</sub> に追従するように設計されており、0.65V~3.6V の任意の電源電圧を受け付けます。

SN54SLC8T245-SEP は、データ・バス間の非同期通信用に設計されています。このデバイスは、方向制御入力 (DIR1 および DIR2) のロジック・レベルに応じて、A バスから B バスへ、または B バスから A バスへデータを転送します。出力イネーブル ( $\overline{OE}$ ) 入力を使用すると、出力をディセーブルにして、バスを実質的に絶縁できます。

SN54SLC8T245-SEP デバイスは、制御ピン (DIR および  $\overline{OE}$ ) が V<sub>CCA</sub> を基準とするよう設計されています。

このデバイスは、I<sub>off</sub> を使用する部分的パワーダウン・アプリケーション用の動作が完全に規定されています。I<sub>off</sub> 回路は、デバイスの電源がオフになったとき、出力をディセーブルにします。これによってデバイスへの電流の逆流を阻止し、デバイスを損傷から保護します。

V<sub>CC</sub> 絶縁機能により、いずれかの V<sub>CC</sub> 入力電圧が 100mV 未満になると、すべてのレベル シフタ出力がディセーブルされ、高インピーダンス状態になるように設計されています。

電源投入または電源オフの間にレベル シフタ I/O を高インピーダンス状態にするには、 $\overline{OE}$  をプルアップ抵抗を介して V<sub>CC</sub> に接続します。この抵抗の最小値は、ドライバの電流シンク能力によって決まります。

### パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
SN54SLC8T245-SEP	PW (TSSOP, 24)	7.8mm × 6.4mm

- (1) 詳細については、[セクション 11](#) を参照してください。
- (2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



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## 4 Pin Configuration and Functions

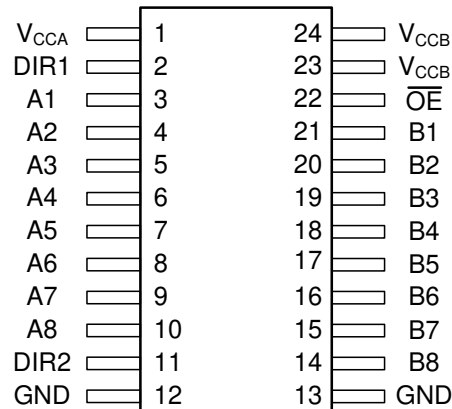


図 4-1. PW Package, 24-Pin TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A1	3	I/O	Input/output A1. Referenced to $V_{CCA}$ .
A2	4	I/O	Input/output A2. Referenced to $V_{CCA}$ .
A3	5	I/O	Input/output A3. Referenced to $V_{CCA}$ .
A4	6	I/O	Input/output A4. Referenced to $V_{CCA}$ .
A5	7	I/O	Input/output A5. Referenced to $V_{CCA}$ .
A6	8	I/O	Input/output A6. Referenced to $V_{CCA}$ .
A7	9	I/O	Input/output A7. Referenced to $V_{CCA}$ .
A8	10	I/O	Input/output A8. Referenced to $V_{CCA}$ .
B1	21	I/O	Input/output B1. Referenced to $V_{CCB}$ .
B2	20	I/O	Input/output B2. Referenced to $V_{CCB}$ .
B3	19	I/O	Input/output B3. Referenced to $V_{CCB}$ .
B4	18	I/O	Input/output B4. Referenced to $V_{CCB}$ .
B5	17	I/O	Input/output B5. Referenced to $V_{CCB}$ .
B6	16	I/O	Input/output B6. Referenced to $V_{CCB}$ .
B7	15	I/O	Input/output B7. Referenced to $V_{CCB}$ .
B8	14	I/O	Input/output B8. Referenced to $V_{CCB}$ .
DIR1	2	I	Direction-control signal 1. Referenced to $V_{CCA}$ .
DIR2	11	I	Direction-control signal 2. Referenced to $V_{CCA}$ . Tie to GND to maintain backward compatibility with SN74AVC8T245 device.
GND	12	—	Ground
	13	—	Ground
OE	22	I	Output Enable. Pull to GND to enable all outputs. Pull to $V_{CCA}$ to place all outputs in high-impedance mode. Referenced to $V_{CCA}$ .
$V_{CCA}$	1	—	A-port supply voltage. $0.65\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$
$V_{CCB}$	23	—	B-port supply voltage. $0.65\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$
	24	—	B-port supply voltage. $0.65\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_{CCA}$		-0.5	4.2	V
Supply voltage, $V_{CCB}$		-0.5	4.2	V
Input voltage, $V_I$ <sup>(2)</sup>	I/O ports (A port)	-0.5	4.2	V
	I/O ports (B port)	-0.5	4.2	
	Control inputs	-0.5	4.2	
Voltage applied to any output in the high-impedance or power-off state, $V_O$ <sup>(2)</sup>	A port	-0.5	4.2	V
	B port	-0.5	4.2	
Voltage applied to any output in the high or low state, $V_O$ <sup>(2) (3)</sup>	A port	-0.5	$V_{CCA} + 0.2$	V
	B port	-0.5	$V_{CCB} + 0.2$	
Input clamp current, $I_{IK}$	$V_I < 0$	-50		mA
Output clamp current, $I_{OK}$	$V_O < 0$	-50		mA
Continuous output current, $I_O$		-50	50	mA
Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND		-100	100	mA
Junction Temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±8000	V
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

		MIN	MAX	UNIT	
V <sub>CCA</sub>	Supply voltage	0.65	3.6	V	
V <sub>CCB</sub>	Supply voltage	0.65	3.6	V	
V <sub>IH</sub>	High-level input voltage	Data inputs	V <sub>CCI</sub> = 0.65 V – 0.75 V	V <sub>CCI</sub> × 0.70	V
			V <sub>CCI</sub> = 0.76 V – 1 V	V <sub>CCI</sub> × 0.70	
			V <sub>CCI</sub> = 1.1 V – 1.95 V	V <sub>CCI</sub> × 0.65	
			V <sub>CCI</sub> = 2.3 V – 2.7 V	1.6	
			V <sub>CCI</sub> = 3 V – 3.6 V	2	
	Control inputs (DIR, $\overline{OE}$ ) Referenced to V <sub>CCA</sub>		V <sub>CCA</sub> = 0.65 V – 0.75 V	V <sub>CCA</sub> × 0.70	
			V <sub>CCA</sub> = 0.76 V – 1 V	V <sub>CCA</sub> × 0.70	
			V <sub>CCA</sub> = 1.1 V – 1.95 V	V <sub>CCA</sub> × 0.65	
			V <sub>CCA</sub> = 2.3 V – 2.7 V	1.6	
			V <sub>CCA</sub> = 3 V – 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	Data inputs	V <sub>CCI</sub> = 0.65 V – 0.75 V	V <sub>CCI</sub> × 0.30	V
			V <sub>CCI</sub> = 0.76 V – 1 V	V <sub>CCI</sub> × 0.30	
			V <sub>CCI</sub> = 1.1 V – 1.95 V	V <sub>CCI</sub> × 0.35	
			V <sub>CCI</sub> = 2.3 V – 2.7 V	0.7	
			V <sub>CCI</sub> = 3 V – 3.6 V	0.8	
	Control inputs (DIR, $\overline{OE}$ ) Referenced to V <sub>CCA</sub>		V <sub>CCA</sub> = 0.65 V – 0.75 V	V <sub>CCA</sub> × 0.30	
			V <sub>CCA</sub> = 0.76 V – 1 V	V <sub>CCA</sub> × 0.30	
			V <sub>CCA</sub> = 1.1 V – 1.95 V	V <sub>CCA</sub> × 0.35	
			V <sub>CCA</sub> = 2.3 V – 2.7 V	0.7	
			V <sub>CCA</sub> = 3 V – 3.6 V	0.8	
V <sub>I</sub>	Input voltage <sup>(3)</sup>	0	3.6	V	
V <sub>O</sub>	Output voltage	Active state	0	V <sub>CCO</sub> <sup>(2)</sup>	V
		Tri-state	0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V	
T <sub>A</sub>	Operating free-air temperature	–55	125	°C	

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(3) All unused data inputs of the device must be held at V<sub>CCI</sub> or GND for proper device operation. See the [Implications of Slow or Floating CMOS Inputs](#) application report.

### 5.4 Thermal Information

THERMAL METRIC		SN54SLC8T245-SEP	UNIT
		PW (TSSOP)	
		24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	45.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	58.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	57.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

## 5.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage V <sub>I</sub> = V <sub>IH</sub>	I <sub>OH</sub> = -100 μA	0.7 V – 3.6 V	0.7 V – 3.6 V	V <sub>CCO</sub> – 0.1		V
		I <sub>OH</sub> = -50 μA	0.65 V	0.65 V	0.55		
		I <sub>OH</sub> = -200 μA	0.76 V	0.76 V	0.58		
		I <sub>OH</sub> = -500 μA	0.85 V	0.85 V	0.65		
		I <sub>OH</sub> = -3 mA	1.1 V	1.1 V	0.85		
		I <sub>OH</sub> = -6 mA	1.4 V	1.4 V	1.05		
		I <sub>OH</sub> = -8 mA	1.65 V	1.65 V	1.2		
		I <sub>OH</sub> = -9 mA	2.3 V	2.3 V	1.75		
		I <sub>OH</sub> = -12 mA	3 V	3 V	2.3		
V <sub>OL</sub>	Low-level output voltage V <sub>I</sub> = V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	0.7 V – 3.6 V	0.7 V – 3.6 V			0.1
		I <sub>OL</sub> = 50 μA	0.65 V	0.65 V			0.1
		I <sub>OL</sub> = 200 μA	0.76 V	0.76 V			0.18
		I <sub>OL</sub> = 500 μA	0.85 V	0.85 V			0.2
		I <sub>OL</sub> = 3 mA	1.1 V	1.1 V			0.25
		I <sub>OL</sub> = 6 mA	1.4 V	1.4 V			0.35
		I <sub>OL</sub> = 8 mA	1.65 V	1.65 V			0.45
		I <sub>OL</sub> = 9 mA	2.3 V	2.3 V			0.55
		I <sub>OL</sub> = 12 mA	3 V	3 V			0.7
I <sub>I</sub>	Input leakage current	Control Inputs (DIR, $\overline{OE}$ ): V <sub>I</sub> = V <sub>CCA</sub> or GND	0.65 V – 3.6 V	0.65 V – 3.6 V	-1	1	μA
I <sub>off</sub>	Partial power down current	A Port: V <sub>I</sub> or V <sub>O</sub> = 0 V – 3.6 V	0 V	0 V – 3.6 V	-35	55	μA
		B Port: V <sub>I</sub> or V <sub>O</sub> = 0 V – 3.6 V	0 V – 3.6 V	0 V	-35	55	
I <sub>OZ</sub>	High-impedance state output current	A Port: V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND, $\overline{OE}$ = V <sub>IH</sub>	3.6 V	3.6 V	-8	8	μA
		B Port: V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND, $\overline{OE}$ = V <sub>IH</sub>	3.6 V	3.6 V	-8	8	
I <sub>CCA</sub>	V <sub>CCA</sub> supply current	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0 mA	0.65 V – 3.6 V	0.65 V – 3.6 V			40
			0 V	3.6 V			-12
			3.6 V	0 V			35
I <sub>CCB</sub>	V <sub>CCB</sub> supply current	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0 mA	0.65 V – 3.6 V	0.65 V – 3.6 V			38
			0 V	3.6 V			35
			3.6 V	0 V			-12
I <sub>CCA</sub> + I <sub>CCB</sub>	Combined supply current	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0 mA	0.65 V – 3.6 V	0.65 V – 3.6 V			70
C <sub>i</sub>	Input capacitance	Control Inputs (DIR, $\overline{OE}$ ): V <sub>I</sub> = 3.3 V or GND	3.3 V	3.3 V			4.5
C <sub>io</sub>	Data I/O capacitance	Ports A and B: $\overline{OE}$ = V <sub>CCA</sub> , V <sub>O</sub> = 1.65 V DC + 1 MHz -16 dBm sine wave	3.3 V	3.3 V			5.7

(1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(2) All typical values are for T<sub>A</sub> = 25°C

## 5.6 Switching Characteristics, $V_{CCA} = 0.7\text{ V}$

See [6-1](#) and [6-2](#) for test circuit and loading conditions. See [6-3](#) and [6-4](#) for measurement waveforms.

PARAMETER	TEST CONDITIONS	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )									UNIT
		0.7 V ± 0.05 V	0.8 V ± 0.04 V	0.9 V ± 0.045 V	1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$t_{pd}$	Propagation delay	From input A to output B	68	47	34	23	21	21	23	27	ns
		From input B to output A	67	55	46	32	28	26	25	25	
$t_{dis}$	Disable time	From input $\overline{OE}$ to output A	100	100	100	100	100	100	100	100	ns
		From input $\overline{OE}$ to output B	111	86	73	38	34	34	33	36	
$t_{en}$	Enable time	From input $\overline{OE}$ to output A	105	105	105	105	105	105	105	105	ns
		From input $\overline{OE}$ to output B	127	78	56	39	36	36	39	47	

## 5.7 Switching Characteristics, $V_{CCA} = 0.8\text{ V}$

See [6-1](#) and [6-2](#) for test circuit and loading conditions. See [6-3](#) and [6-4](#) for measurement waveforms.

PARAMETER	TEST CONDITIONS	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )									UNIT
		0.7 V ± 0.05 V	0.8 V ± 0.04 V	0.9 V ± 0.045 V	1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$t_{pd}$	Propagation delay	From input A to output B	55	38	26	16	14	13	13	14	ns
		From input B to output A	47	38	32	21	17	15	14	14	
$t_{dis}$	Disable time	From input $\overline{OE}$ to output A	71	71	71	71	71	71	71	71	ns
		From input $\overline{OE}$ to output B	105	79	66	32	28	27	25	26	
$t_{en}$	Enable time	From input $\overline{OE}$ to output A	64	64	64	64	64	64	64	64	ns
		From input $\overline{OE}$ to output B	118	69	47	30	27	26	26	28	

## 5.8 Switching Characteristics, $V_{CCA} = 0.9\text{ V}$

See [6-1](#) and [6-2](#) for test circuit and loading conditions. See [6-3](#) and [6-4](#) for measurement waveforms.

PARAMETER	TEST CONDITIONS	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )									UNIT
		0.7 V ± 0.05 V	0.8 V ± 0.04 V	0.9 V ± 0.045 V	1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$t_{pd}$	Propagation delay	From input A to output B	45	31	21	13	10	9	9	9	ns
		From input B to output A	35	27	23	15	11	10	9	8	
$t_{dis}$	Disable time	From input $\overline{OE}$ to output A	55	55	55	55	55	55	55	55	ns
		From input $\overline{OE}$ to output B	99	74	61	26	23	22	20	20	
$t_{en}$	Enable time	From input $\overline{OE}$ to output A	41	41	41	41	41	41	41	41	ns
		From input $\overline{OE}$ to output B	108	63	41	24	20	19	18	19	

## 5.9 Switching Characteristics, $V_{CCA} = 1.2\text{ V}$

See [6-1](#) and [6-2](#) for test circuit and loading conditions. See [6-3](#) and [6-4](#) for measurement waveforms.

PARAMETER	TEST CONDITIONS	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )									UNIT
		0.7 V ± 0.05 V	0.8 V ± 0.04 V	0.9 V ± 0.045 V	1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$t_{pd}$	Propagation delay	From input A to output B	33	21	14	8	6	5	5	5	ns
		From input B to output A	24	16	13	8	6	5	4	4	
$t_{dis}$	Disable time	From input $\overline{OE}$ to output A	19	19	19	19	19	19	19	19	ns
		From input $\overline{OE}$ to output B	92	66	53	20	17	16	14	14	
$t_{en}$	Enable time	From input $\overline{OE}$ to output A	19	19	19	19	19	19	19	19	ns
		From input $\overline{OE}$ to output B	96	53	33	17	12	11	10	10	

## 5.10 Switching Characteristics, $V_{CCA} = 1.5\text{ V}$

See [6-1](#) and [6-2](#) for test circuit and loading conditions. See [6-3](#) and [6-4](#) for measurement waveforms.

PARAMETER	TEST CONDITIONS	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )									UNIT
		0.7 V ± 0.05 V	0.8 V ± 0.04 V	0.9 V ± 0.045 V	1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$t_{pd}$	Propagation delay	From input A to output B	29	17	11	6	5	4	4	3	ns
		From input B to output A	23	14	10	6	5	4	3	3	
$t_{dis}$	Disable time	From input $\overline{OE}$ to output A	15	15	15	15	15	15	15	15	ns
		From input $\overline{OE}$ to output B	89	64	50	18	15	15	12	13	
$t_{en}$	Enable time	From input $\overline{OE}$ to output A	12	12	12	12	12	12	12	12	ns
		From input $\overline{OE}$ to output B	92	49	29	14	10	8	7	7	

## 5.11 Switching Characteristics, $V_{CCA} = 1.8\text{ V}$

See [6-1](#) and [6-2](#) for test circuit and loading conditions. See [6-3](#) and [6-4](#) for measurement waveforms.

PARAMETER	TEST CONDITIONS	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )									UNIT
		0.7 V ± 0.05 V	0.8 V ± 0.04 V	0.9 V ± 0.045 V	1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$t_{pd}$	Propagation delay	From input A to output B	28	15	9	5	4	4	3	3	ns
		From input B to output A	23	13	9	5	4	4	3	2	
$t_{dis}$	Disable time	From input $\overline{OE}$ to output A	14	14	14	14	14	14	14	14	ns
		From input $\overline{OE}$ to output B	89	63	49	17	15	14	12	12	
$t_{en}$	Enable time	From input $\overline{OE}$ to output A	9	9	9	9	9	9	9	9	ns
		From input $\overline{OE}$ to output B	91	47	28	13	9	7	6	6	



### 5.12 Switching Characteristics, $V_{CCA} = 2.5\text{ V}$

See [6-1](#) and [6-2](#) for test circuit and loading conditions. See [6-3](#) and [6-4](#) for measurement waveforms.

PARAMETER	TEST CONDITIONS	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )									UNIT
		0.7 V ± 0.05 V	0.8 V ± 0.04 V	0.9 V ± 0.045 V	1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$t_{pd}$	Propagation delay	From input A to output B	27	14	8	4	3	3	2	2	ns
		From input B to output A	26	13	8	5	4	3	2	2	
$t_{dis}$	Disable time	From input $\overline{OE}$ to output A	11	11	11	11	11	11	11	11	ns
		From input $\overline{OE}$ to output B	88	62	48	16	13	13	11	11	
$t_{en}$	Enable time	From input $\overline{OE}$ to output A	6	6	6	6	6	6	6	6	ns
		From input $\overline{OE}$ to output B	89	46	26	12	8	7	5	5	

### 5.13 Switching Characteristics, $V_{CCA} = 3.3\text{ V}$

See [6-1](#) and [6-2](#) for test circuit and loading conditions. See [6-3](#) and [6-4](#) for measurement waveforms.

PARAMETER	TEST CONDITIONS	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )									UNIT
		0.7 V ± 0.05 V	0.8 V ± 0.04 V	0.9 V ± 0.045 V	1.2 V ± 0.1 V	1.5 V ± 0.1 V	1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$t_{pd}$	Propagation delay	From input A to output B	27	13	8	4	3	2	2	2	ns
		From input B to output A	31	14	9	5	3	3	2	2	
$t_{dis}$	Disable time	From input $\overline{OE}$ to output A	11	11	11	11	11	11	11	11	ns
		From input $\overline{OE}$ to output B	87	61	48	16	13	12	11	11	
$t_{en}$	Enable time	From input $\overline{OE}$ to output A	5	5	5	5	5	5	5	5	ns
		From input $\overline{OE}$ to output B	89	45	26	11	8	6	5	4	

### 5.14 Operating Characteristics

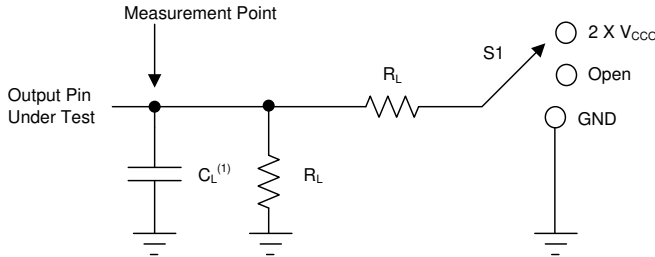
$T_A = 25^\circ\text{C}$ ,  $C_L = 0$ ,  $R_L = \text{Open}$ ,  $f = 1\text{ MHz}$ ,  $t_r = t_f = 1\text{ ns}$

PARAMETER	TEST CONDITIONS	SUPPLY VOLTAGE ( $V_{CCA} = V_{CCB}$ )									UNIT
		0.7 V	0.8 V	0.9 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP		
$C_{pdA}$	$V_{CCA}$ Power dissipation capacitance per transceiver	A to B: Outputs Enabled	1.2	1.8	1.8	1.7	1.7	1.7	2	2.5	pF
	A to B: Outputs Disabled	1.1	1.8	1.8	1.7	1.7	1.7	2	2.1	pF	
	B to A: Outputs Enabled	9.3	11.8	11.8	12	12.2	13	16.4	18.1	pF	
	B to A: Outputs Disabled	2.6	1.2	1.1	1.2	1.2	1.3	1.6	3.9	pF	
$C_{pdB}$	$V_{CCB}$ Power dissipation capacitance per transceiver	A to B: Outputs Enabled	9.3	11.7	11.8	11.9	12.2	12.9	16.3	18	pF
	A to B: Outputs Disabled	2.6	11.7	11.8	11.9	12.2	12.9	16.3	3.9	pF	
	B to A: Outputs Enabled	1.2	1.8	1.8	1.7	1.7	1.7	2	2.5	pF	
	B to A: Outputs Disabled	1.1	1.8	1.8	1.7	1.7	1.7	2	2.1	pF	

## 6 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- $f = 1 \text{ MHz}$
- $Z_0 = 50 \Omega$
- $dv / dt \leq 1 \text{ ns/V}$



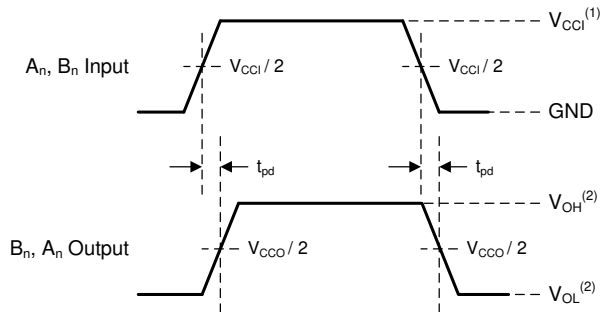
A.  $C_L$  includes probe and jig capacitance.

图 6-1. Load Circuit

Parameter	$V_{CCO}$	$R_L$	$C_L$	S1	$V_{TP}$
$t_{pd}$	1.1 V - 3.6 V	2 kΩ	15 pF	Open	N/A
	0.65 V - 0.95 V	20 kΩ	15 pF	Open	N/A
$t_{en}^{(1)}, t_{dis}^{(1)}$	3 V - 3.6 V	2 kΩ	15 pF	2 X $V_{CCO}$	0.3 V
	1.65 V - 2.7 V	2 kΩ	15 pF	2 X $V_{CCO}$	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	2 X $V_{CCO}$	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	2 X $V_{CCO}$	0.1 V
$t_{en}^{(2)}, t_{dis}^{(2)}$	3 V - 3.6 V	2 kΩ	15 pF	GND	0.3 V
	1.65 V - 2.7 V	2 kΩ	15 pF	GND	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	GND	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	GND	0.1 V

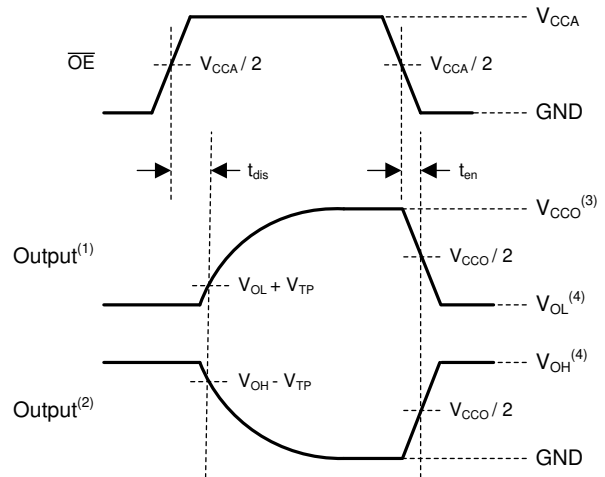
- A. Output waveform on the conditions that input is driven to a valid Logic Low.
- B. Output waveform on the condition that input is driven to a valid Logic High.

图 6-2. Load Circuit Conditions



- A.  $V_{CC1}$  is the supply pin associated with the input port.
- B.  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels with specified  $R_L$ ,  $C_L$ , and  $S_1$ .

图 6-3. Propagation Delay



- A. Output waveform on the condition that input is driven to a valid Logic Low.
- B. Output waveform on the condition that input is driven to a valid Logic High.
- C.  $V_{CCO}$  is the supply pin associated with the output port.
- D.  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels with specified  $R_L$ ,  $C_L$ , and  $S_1$ .

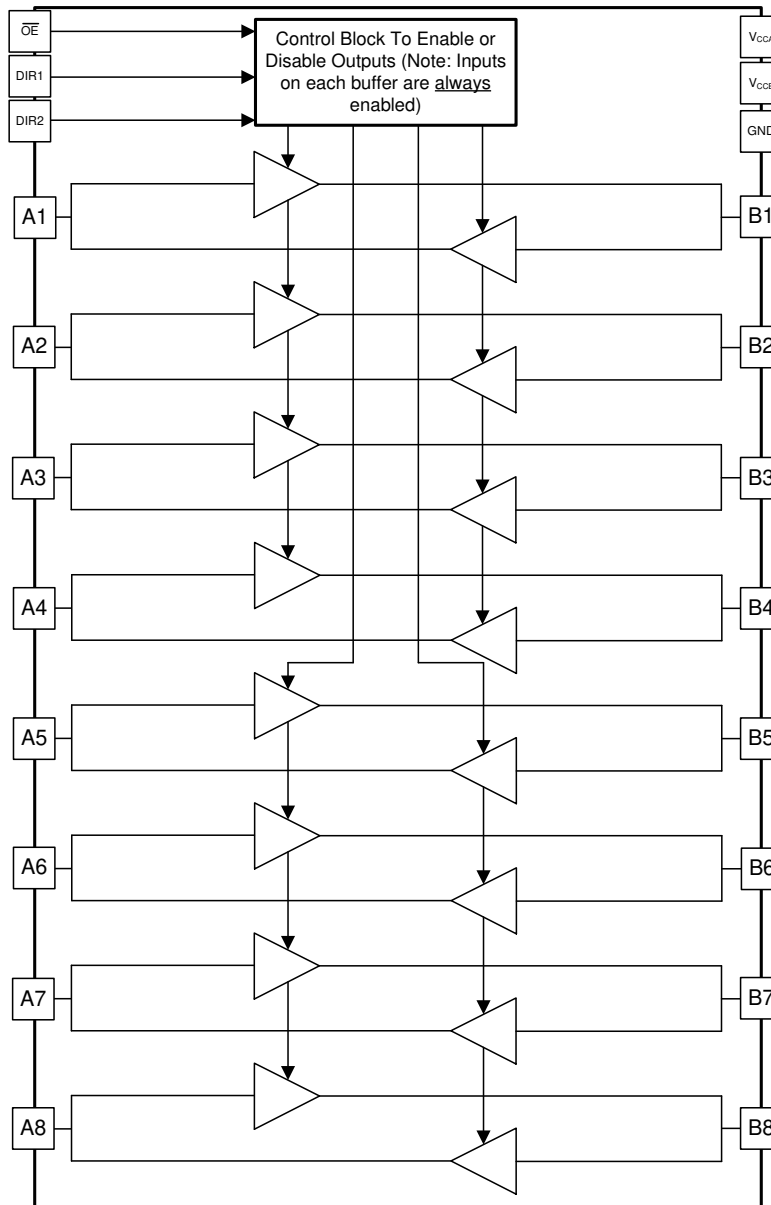
图 6-4. Enable Time And Disable Time

## 7 Detailed Description

### 7.1 Overview

The SN54SLC8T245-SEP device is an 8-bit, dual-supply non-inverting transceiver with bidirectional voltage level translation. The I/O pins labeled with A and the control pins (DIR1, DIR2, and  $\overline{OE}$ ) are supported by  $V_{CCA}$ , and the I/O pins labeled with B are supported by  $V_{CCB}$ . The A port and the B port are able to accept I/O voltages ranging from 0.65 V to 3.6 V.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Up-Translation and Down-Translation From 0.65 V to 3.6 V

Both supply pins are configured from 0.65 V to 3.6 V, which makes the device suitable for translating between any of the low voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

### 7.3.2 Multiple Direction Control Pins

Two control pins are used to configure the 8 data I/Os. I/O channels 1 through 4 are grouped together and I/O channels 5 through 8 are banked together. The benefit of this is to permit simultaneous up-translation and down-translation within one device. This eliminates the need for multiple devices, where each device can only provide up-translation or down-translation sequentially. Simultaneous up and down translation is supported when both  $V_{CCA}$  and  $V_{CCB}$  are at least 1.40 V.

### 7.3.3 $I_{off}$ Supports Partial-Power-Down Mode Operation

This feature is to limit the leakage current of an I/O pin being driven to a voltage as large as 3.6 V while having its corresponding power supply rail powered down. This is represented by the  $I_{off}$  parameter in the [Electrical Characteristics](#) table.

## 7.4 Device Functional Modes

All control inputs are referenced to  $V_{CCA}$  and must be driven to a valid Logic High or Logic Low (that is, not floating) for proper device operation and to prevent excessive power consumption. [表 7-1](#) summarizes the possible modes of device operation based on the configuration of the control inputs.

**表 7-1. Function Table**

CONTROL INPUTS <sup>(1)</sup>			SIGNAL DIRECTION	
OE	DIR1	DIR2	Bits 1:4	Bits 5:8
H	X	X	Disabled (Hi-Z)	
L	L	L	B to A	
L	L	H	B to A	A to B
L	H	L	A to B	
L	H	H	A to B	B to A

(1) Input circuits of the data I/Os are always active and must be driven to a valid logic level.

## 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The SN54SLC8T245-SEP device can be used in level-translation applications for interfacing devices or systems operating at different voltage nodes. [Figure 8-1](#) depicts an application in which the SN54SLC8T245-SEP device is up-translating a 0.7 V input to a 3.3 V output to interface between a system controller and a peripheral device.

### 8.2 Typical Application

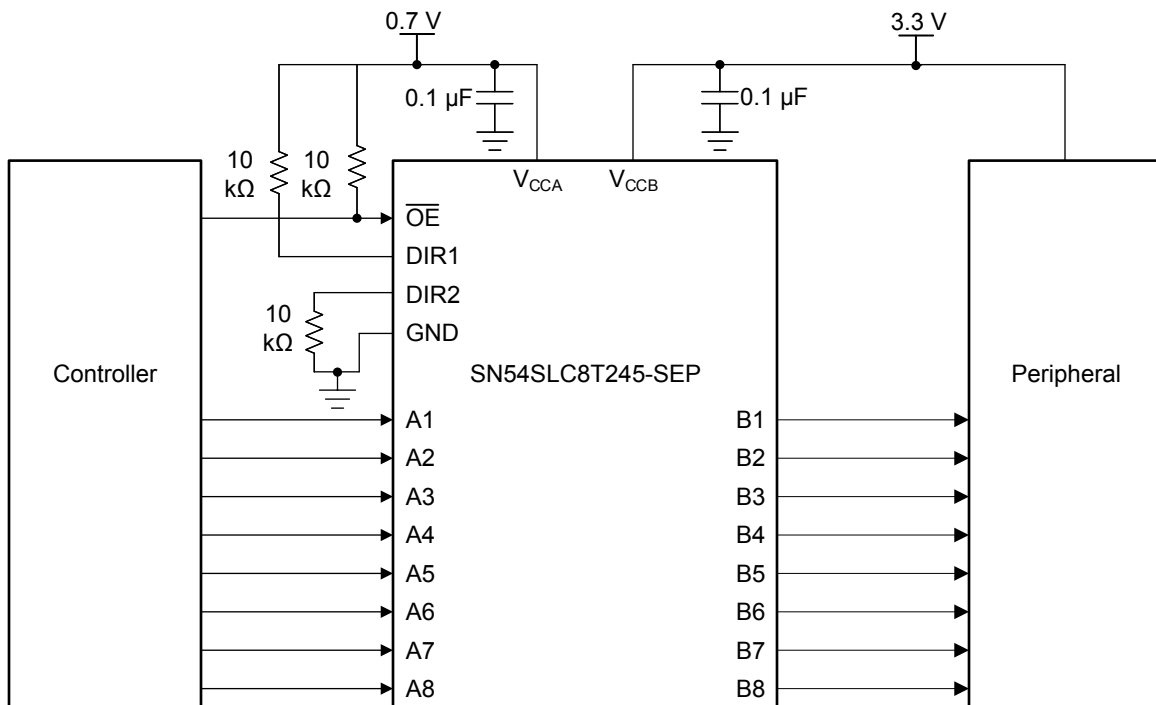


Figure 8-1. Typical Application Schematic

## 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

## 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN54SLC8T245-SEP device to determine the input voltage range. For a valid logic high, the value must exceed the  $V_{IH}$  of the input port. For a valid logic low, the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN54SLC8T245-SEP device is driving to determine the output voltage range.

## 8.2.3 Application Curve

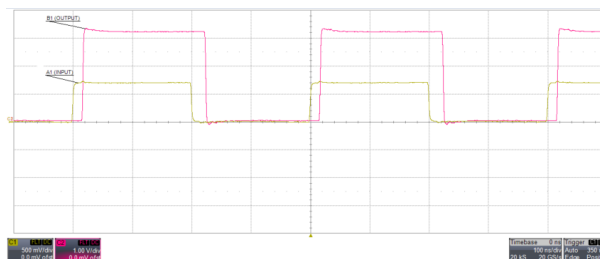


図 8-2. Translation Up (0.7 V to 3.3 V) at 2.5 MHz

## 8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. There are no additional requirements for power supply sequencing.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of level translators, see the [Power Sequencing for AXC Family of Devices](#) application report.

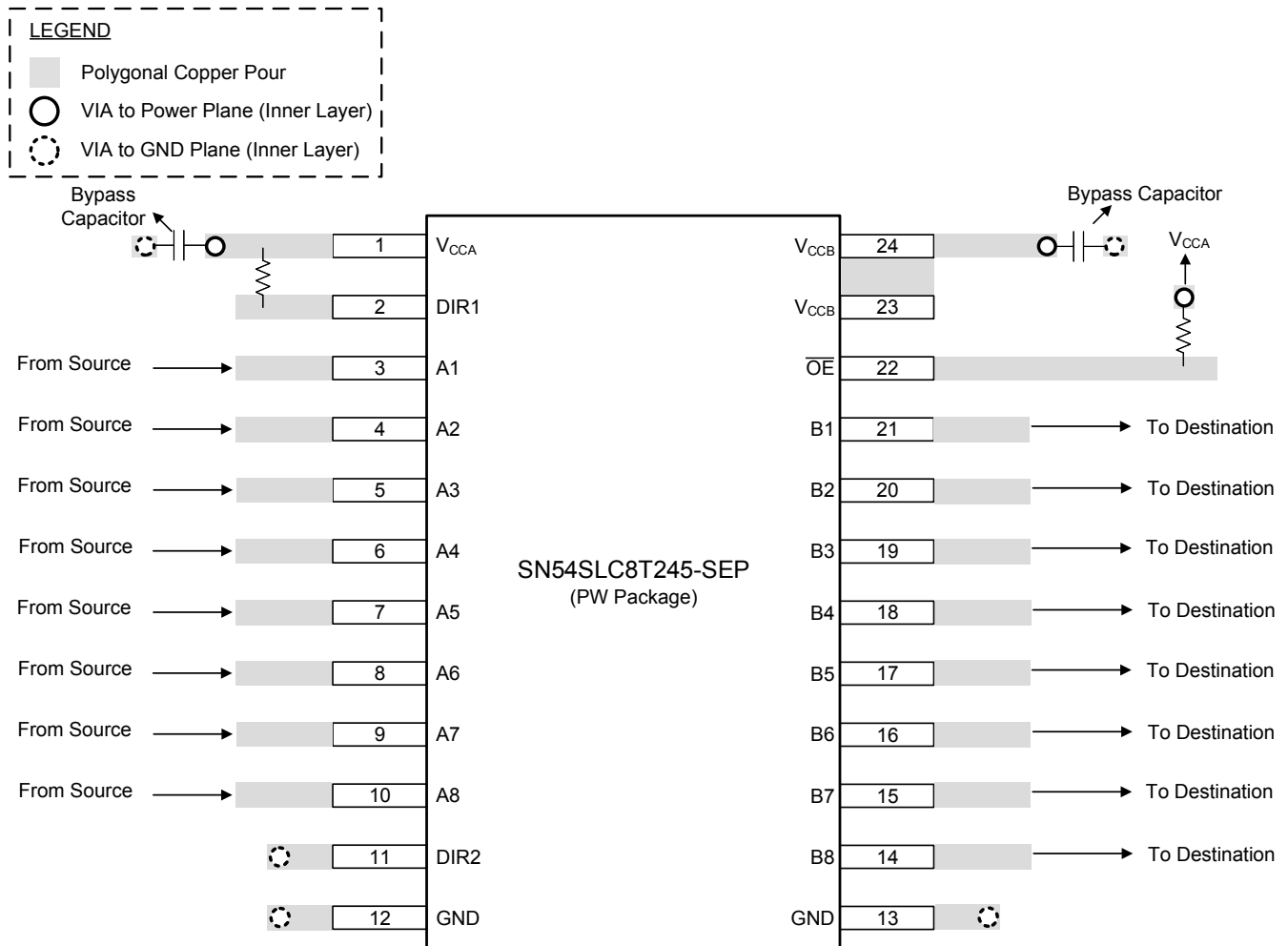
## 8.4 Layout

### 8.4.1 Layout Guidelines

To device reliability, follow common printed-circuit board layout guidelines:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

### 8.4.2 Layout Example



**図 8-3. SN54SLC8T245-SEP Device Layout Example**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application report](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2022) to Revision B (December 2023)	Page
• パッケージ・リード・サイズを含めるよう「パッケージ情報」表を更新 .....	1
• Updated the <i>Translation Up (0.7 V to 3.3 V) at 2.5 MHz</i> figure.....	14

Changes from Revision * (February 2022) to Revision A (September 2022)	Page
• データシートのステータスを以下のように変更:「事前情報」から「量産データ」.....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN54SLC8T245PWTSEP	ACTIVE	TSSOP	PW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SLC8T245E	<a href="#">Samples</a>
V62/22604-01XE	ACTIVE	TSSOP	PW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		SLC8T245E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN54SLC8T245PWTSEP	TSSOP	PW	24	250	180.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN54SLC8T245PWTSEP	TSSOP	PW	24	250	210.0	185.0	35.0

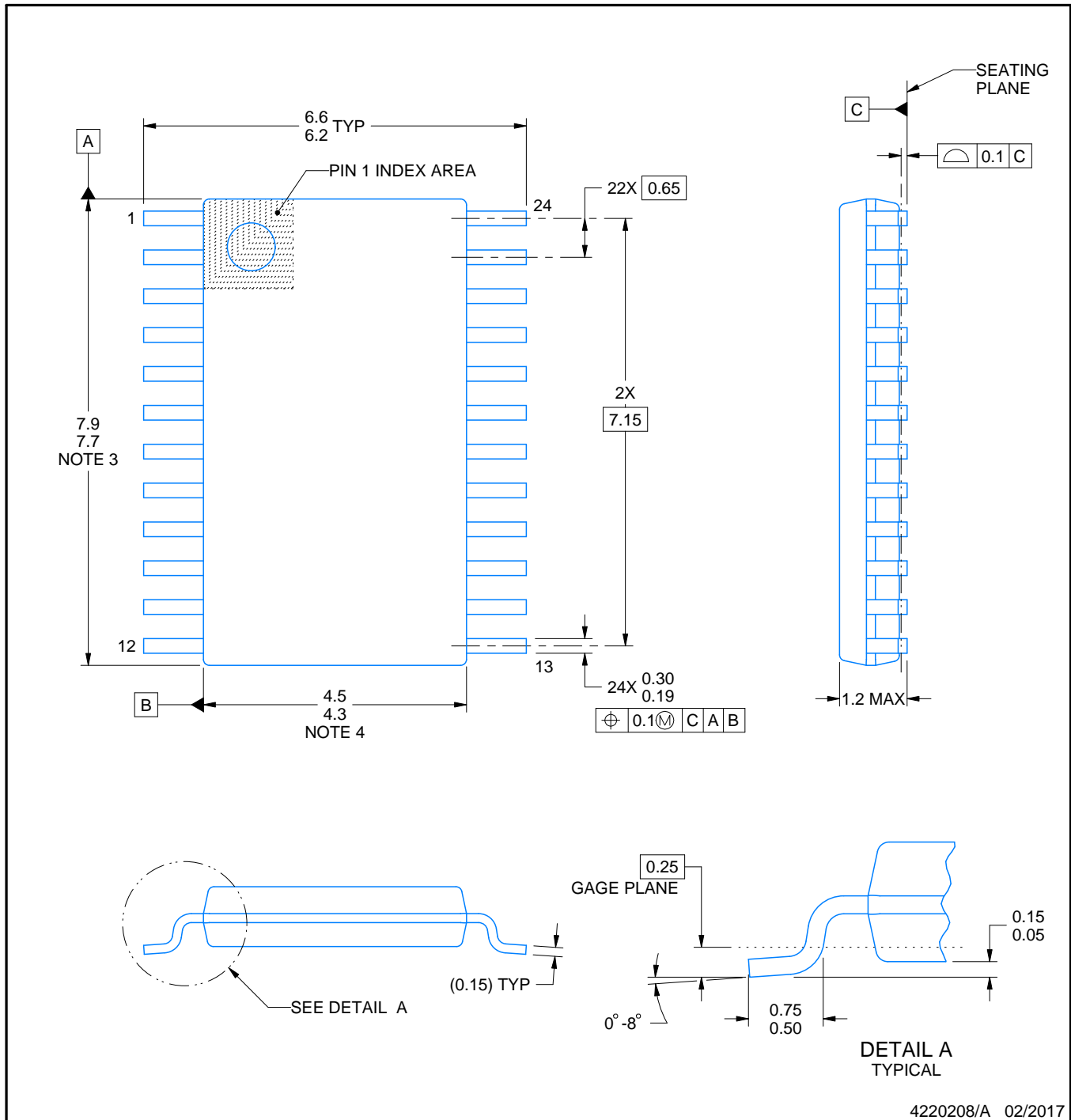
# PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

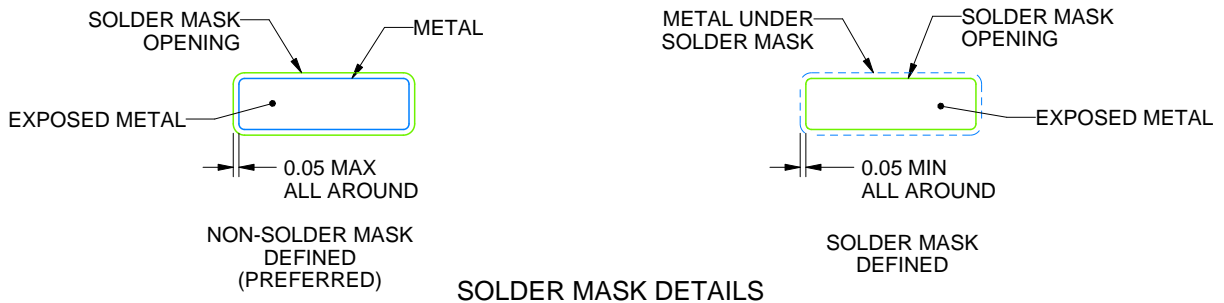
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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