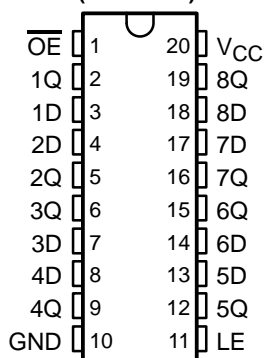


# SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

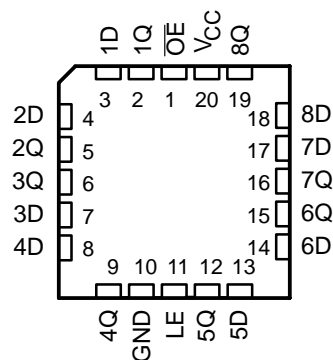
SCBS016D – SEPTEMBER 1988 – REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- Full Parallel Access for Loading
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)

SN54BCT373 . . . J OR W PACKAGE  
SN74BCT373 . . . DB, DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54BCT373 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'BCT373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT373N	SN74BCT373N
	SOIC – DW	Tube	SN74BCT373DW	BCT373
		Tape and reel	SN74BCT373DWR	
	SOP – NS	Tape and reel	SN74BCT373NSR	BCT373
SSOP – DB	Tape and reel	SN74BCT373DBR	BT373	
–55°C to 125°C	CDIP – J	Tube	SNJ54BCT373J	SNJ54BCT373J
	CFP – W	Tube	SNJ54BCT373W	SNJ54BCT373W
	LCCC – FK	Tube	SNJ54BCT373FK	SNJ54BCT373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS016D – SEPTEMBER 1988 – REVISED MARCH 2003

## description/ordering information (continued)

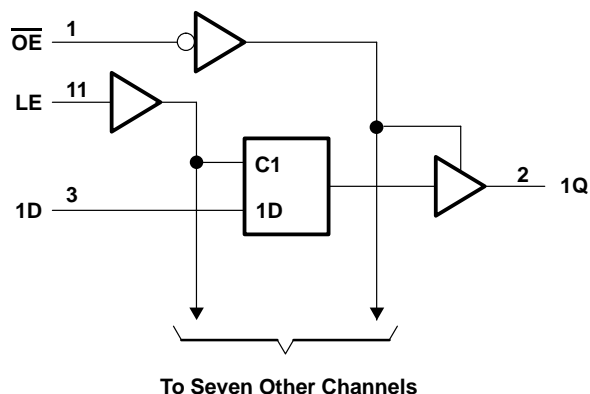
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



# SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS016D – SEPTEMBER 1988 – REVISED MARCH 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ .....	–0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ .....	–30 mA
Current into any output in the low state: SN54BCT373 .....	96 mA
SN74BCT373 .....	128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54BCT373			SN74BCT373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			48			64	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54BCT373, SN74BCT373**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

SCBS016D – SEPTEMBER 1988 – REVISED MARCH 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		SN54BCT373			SN74BCT373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	2.4	3.3		2.4	3.3		V
		I <sub>OH</sub> = -12 mA	2	3.2					
		I <sub>OH</sub> = -15 mA				2	3.1		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA		0.38	0.55				V
		I <sub>OL</sub> = 64 mA				0.42	0.55		
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			0.4			0.4	mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V			-0.6			-0.6	mA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-100		-225	-100		-225	mA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50			50	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50			-50	μA
I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V			37	60		37	60	mA
I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V			2	5		2	5	mA
I <sub>CCZ</sub>	V <sub>CC</sub> = 5.5 V			5	8		5	8	mA
C <sub>i</sub>	V <sub>CC</sub> = 5 V,	V <sub>I</sub> = 2.5 V or 0.5 V		6			6		pF
C <sub>o</sub>	V <sub>CC</sub> = 5 V,	V <sub>O</sub> = 2.5 V or 0.5 V		11			11		pF

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54BCT373		SN74BCT373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	7.5		7.5		7.5		ns
t <sub>su</sub>	Setup time, data before LE↓	2		2		2		ns
t <sub>h</sub>	Hold time, data after LE↓	5.5		5.5		5.5		ns



# SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS016D – SEPTEMBER 1988 – REVISED MARCH 2003

## switching characteristics (see Figure 1)

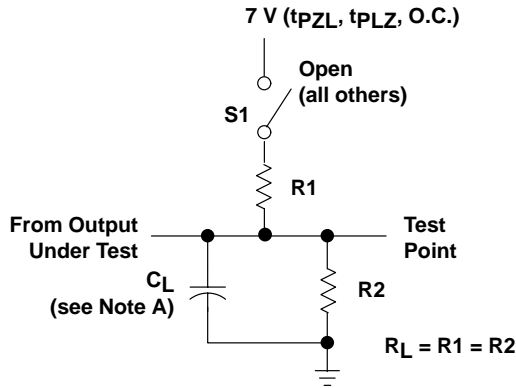
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V},$ $C_L = 50\text{ pF},$ $R_1 = 500\ \Omega,$ $R_2 = 500\ \Omega,$ $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R_1 = 500\ \Omega,$ $R_2 = 500\ \Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT
			'BCT373			SN54BCT373		SN74BCT373		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	2	5.9	7.7	1.5	10.1	2	9.3	ns
$t_{PHL}$			2	6.7	8.5	1	10.3	1.5	9.5	
$t_{PLH}$	LE	Q	2	6.2	8.2	2	10.1	2	9.3	ns
$t_{PHL}$			2	5.9	7.8	2	9.2	2	8.8	
$t_{PZH}$	$\overline{OE}$	Q	1	7.8	9.6	1	12.3	1	11.8	ns
$t_{PZL}$			1	8.2	10.2	1	12.5	1	12	
$t_{PHZ}$	$\overline{OE}$	Q	1	4.9	6.6	1	7.4	1	7	ns
$t_{PLZ}$			1	5	6.7	1	8.1	1	7.4	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

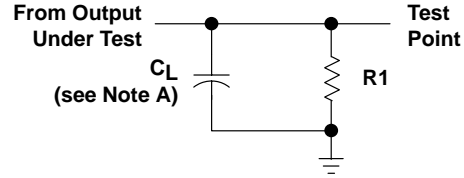
# SN54BCT373, SN74BCT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS016D – SEPTEMBER 1988 – REVISED MARCH 2003

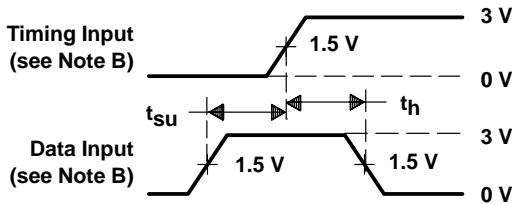
## PARAMETER MEASUREMENT INFORMATION



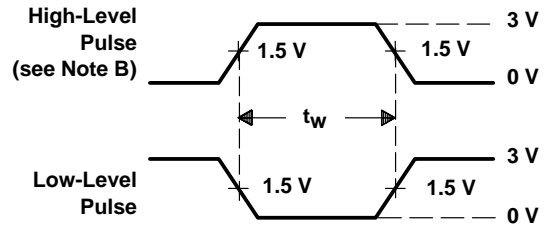
LOAD CIRCUIT FOR  
3-STATE AND OPEN-COLLECTOR OUTPUTS



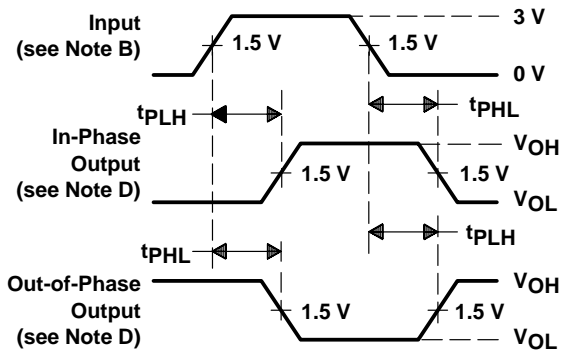
LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS



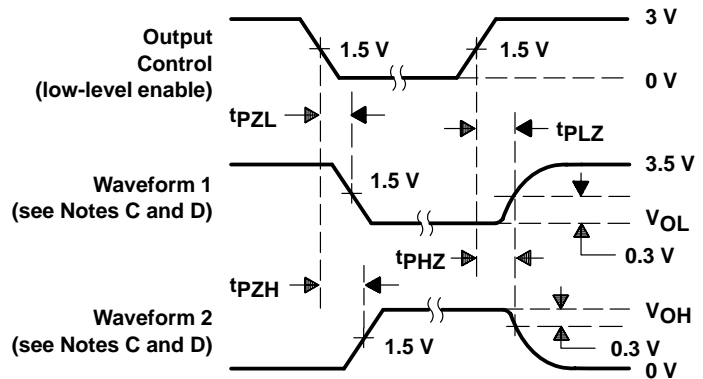
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
 F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9074601M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9074601M2A SNJ54BCT 373FK	<a href="#">Samples</a>
5962-9074601MRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9074601MR A SNJ54BCT373J	<a href="#">Samples</a>
SNJ54BCT373FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9074601M2A SNJ54BCT 373FK	<a href="#">Samples</a>
SNJ54BCT373J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9074601MR A SNJ54BCT373J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TUBE**

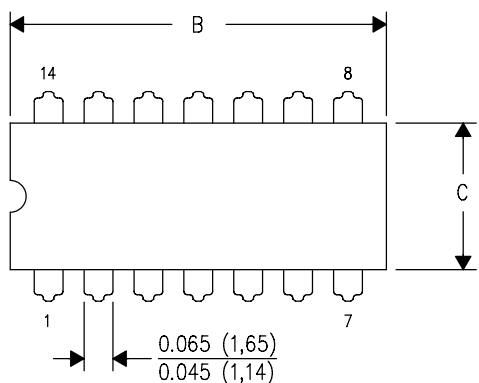

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9074601M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT373FK	FK	LCCC	20	55	506.98	12.06	2030	NA

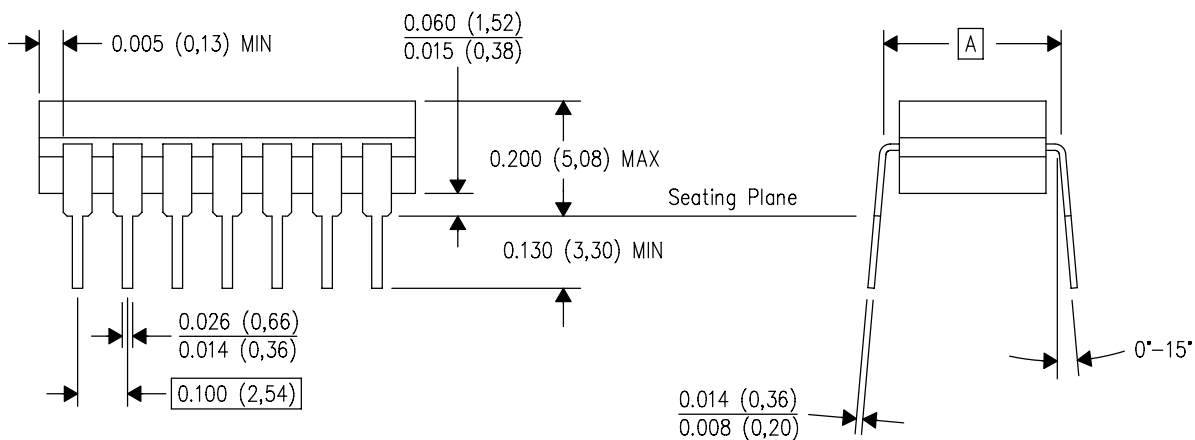
# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated