

SNx4AC74 デュアル ポジティブ エッジ トリガ D タイプ フリップ フロップ、クリア/プリセット搭載

1 特長

- 2V~6V の V_{CC} で動作
- 6V までの入力電圧に対応
- 最大 t_{pd} 10 ns (5V 時)

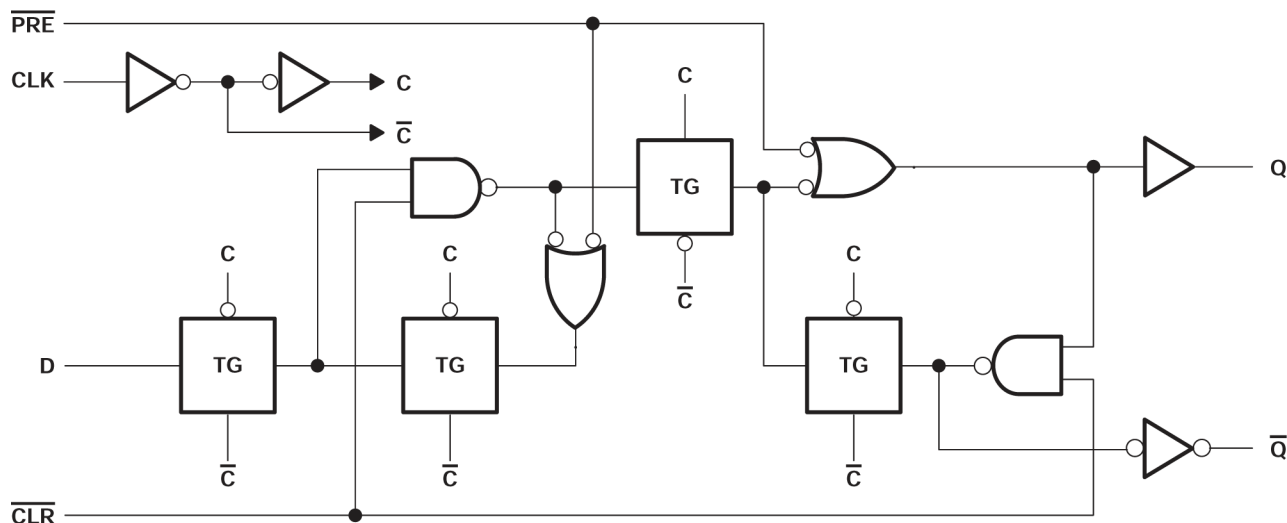
2 概要

'AC74 デバイスは、デュアル ポジティブ エッジ トリガ D タイプ フリップ フロップです。

製品情報

部品番号	パッケージ (1)	パッケージサイズ (2)	本体サイズ (3)
SNx4AC74	PW (TSSOP, 14)	5 mm × 6.4 mm	5 mm × 4.40 mm
	D (SOIC, 14)	8.65 mm × 6 mm	8.65 mm × 3.9 mm
	DB (SSOP, 14)	6.2 mm × 7.8 mm	6.2 mm × 5.3 mm
	N (PDIP, 14)	19.3 mm × 9.4 mm	19.3 mm × 6.35 mm
	NS (SOP, 14)	10.2 mm × 7.8 mm	10.3 mm × 5.3 mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



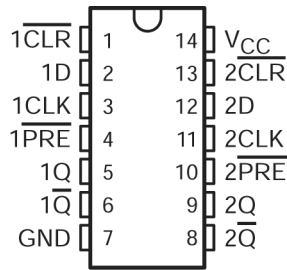
各フリップフロップの論理図 (正論理)



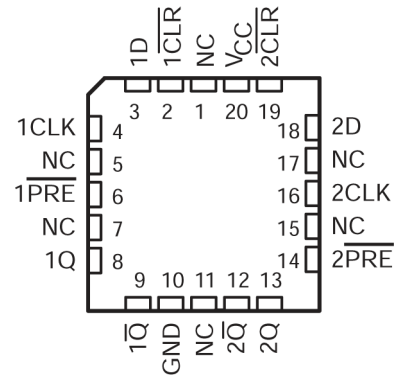
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3 Pin Configuration and Functions



☒ 3-1. SN54AC74 J or W Package; SN74AC74 D, DB, N, NS, or PW Package (Top View)



NC - No internal connection

☒ 3-2. SN54AC74 FK Package (Top View)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1 CLR	1	Input	Channel 1, Clear Input, Active Low
1D	2	Input	Channel 1, Data Input
1CLK	3	Input	Channel 1, Positive edge triggered clock input
1 PRE	4	Input	Channel 1, Preset Input, Active Low
1Q	5	Output	Channel 1, Output
1 Q̄	6	Output	Channel 1, Inverted Output
GND	7	—	Ground
2 Q̄	8	Output	Channel 2, Inverted Output
2Q	9	Output	Channel 2, Output
2 PRE	10	Input	Channel 2, Preset Input, Active Low
2CLK	11	Input	Channel 2, Positive edge triggered clock input
2D	12	Input	Channel 2, Data Input
2 CLR	13	Input	Channel 2, Clear Input, Active Low
V _{CC}	14	—	Positive Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I ⁽²⁾	Input voltage range	-0.5	V _{CC} + 0.5	V
V _O ⁽²⁾	Output voltage range	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0 or V _I > V _{CC})		±20 mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})		±20 mA
I _O	Continuous output current	(V _O = 0 to V _{CC})		±50 mA
	Continuous current through V _{CC} or GND			±200 mA
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AC74		SN74AC74		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	6	2	6	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1	2.1		V
		V _{CC} = 4.5 V	3.15	3.15		
		V _{CC} = 5.5 V	3.85	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 3 V	0.9		V	
		V _{CC} = 4.5 V	1.35			
		V _{CC} = 5.5 V	1.65			
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V	-12		mA	
		V _{CC} = 4.5 V	-24			
		V _{CC} = 5.5 V	-24			
I _{OL}	Low-level output current	V _{CC} = 3 V	12		mA	
		V _{CC} = 4.5 V	24			
		V _{CC} = 5.5 V	24			
Δt/Δv	Input transition rise or fall rate	8		8		ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC ⁽¹⁾	SNx4AC74					UNIT
	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA} Junction-to-ambient thermal resistance	119.9	96	80	76	145.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9	4.49		2.9		2.9	V	
		4.5 V	4.4	5.49		4.4		4.4		
		5.5 V	5.4	5.49		5.4		5.4		
	I _{OH} = -12 mA	3 V	2.56			2.4		2.46		
		I _{OH} = -24 mA	4.5 V	3.86			3.7			3.76
			5.5 V	4.86			4.7			4.76
		I _{OH} = -50 mA ⁽¹⁾	5.5 V				3.85			
I _{OH} = -75 mA ⁽¹⁾	5.5 V						3.85			
V _{OL}	I _{OL} = 50 μA	3 V		0.002	0.1		0.1	0.1	V	
		4.5 V		0.001	0.1		0.1	0.1		
		5.5 V		0.001	0.1		0.1	0.1		
	I _{OL} = 12 mA	3 V			0.36		0.5	0.44		
		4.5 V			0.36		0.5	0.44		
	I _{OL} = 24 mA		5.5 V			0.36		0.5		0.44
		I _{OL} = 50 mA ⁽¹⁾	5.5 V				1.65			
I _{OL} = 75 mA ⁽¹⁾	5.5 V						1.65			
I _I	Data pins	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA
	Control pins					±0.1		±1	±1	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		40	20	μA	
C _i	V _I = V _{CC} or GND	5 V		3					pF	

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

4.5 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

			T _A = 25°C		SN54AC74		SN74AC74		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency			100			70		95	MHz
t _w	Pulse duration	PRE or CLR low		5.5			8		7	ns
		CLK		5.5			8		7	
t _{su}	Setup time, data before CLK ↑	Data		4			5		4.5	ns
		PRE or CLR inactive		0			0.5		0	

SN54AC74, SN74AC74

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 over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		$T_A = 25^\circ\text{C}$		SN54AC74		SN74AC74		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_h	Hold time, data after CLK \uparrow	0.5		0.5		0.5		ns

4.6 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

 over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		$T_A = 25^\circ\text{C}$		SN54AC74		SN74AC74		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	140		95		125		MHz
t_w	Pulse duration	PRE or CLR low	4.5	5.5	5			ns
		CLK	4.5	5.5	5			
t_{su}	Setup time, data before CLK \uparrow	Data	3	4	3			ns
		PRE or CLR inactive	0	0.5	0			
t_h	Hold time, data after CLK \uparrow	0.5		0.5		0.5		ns

4.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

 over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		70		95	MHz	
t_{PLH}	PRE or CLR	Q or \bar{Q}	3.5	8	12	1	13	2.5	13	ns
t_{PHL}			4	10.5	12	1	14	3.5	13.5	
t_{PLH}	CLK	Q or \bar{Q}	4.5	8	13.5	1	17.5	4	16	ns
t_{PHL}			3.5	8	14	1	13.5	3.5	14.5	

4.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

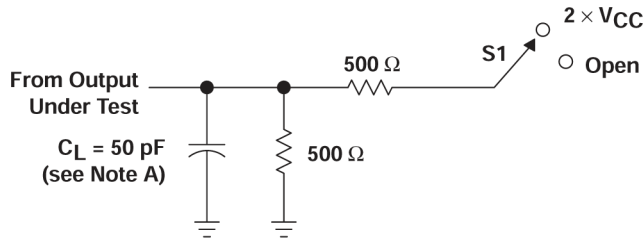
 over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			140	160		95		125	MHz	
t_{PLH}	PRE or CLR	Q or \bar{Q}	2.5	6	9	1	9.5	2	10	ns
t_{PHL}			3	8	9.5	1	10.5	2.5	10.5	
t_{PLH}	CLK	Q or \bar{Q}	3.5	6	10	1	12	3	10.5	ns
t_{PHL}			2.5	6	10	1	10	2.5	10.5	

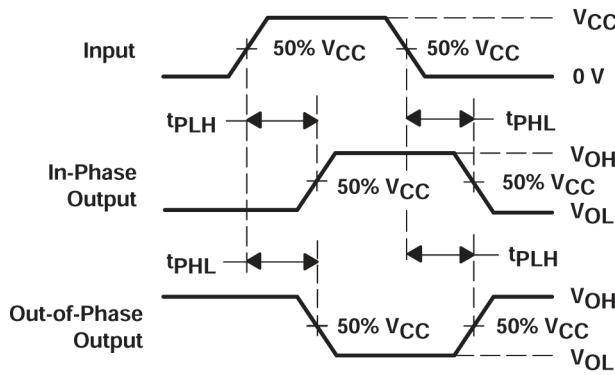
4.9 Operating Characteristics
 $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$,	$f = 1\text{ MHz}$	45	pF

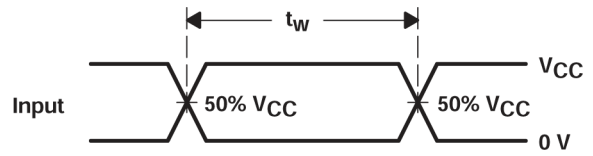
5 Parameter Measurement Information



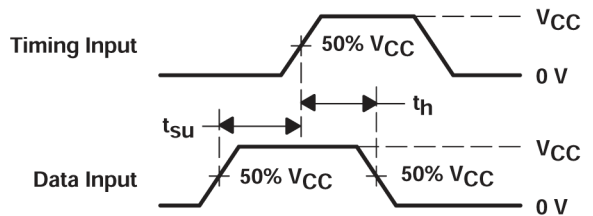
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- C. The outputs are measured one at a time with one input transition per measurement.

图 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open

6 Detailed Description

6.1 Overview

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

6.2 Functional Block Diagram

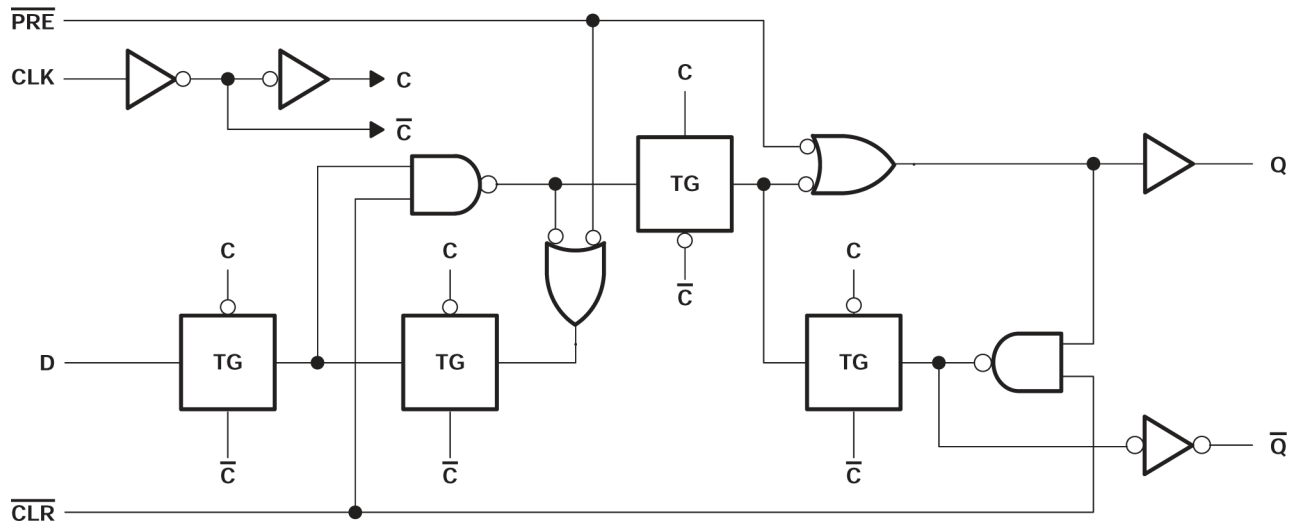


図 6-1. Logic Diagram, Each Flip-flop (Positive Logic)

6.3 Device Functional Modes

表 6-1. Function Table

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\overline{Q}_0

- (1) This configuration is unstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

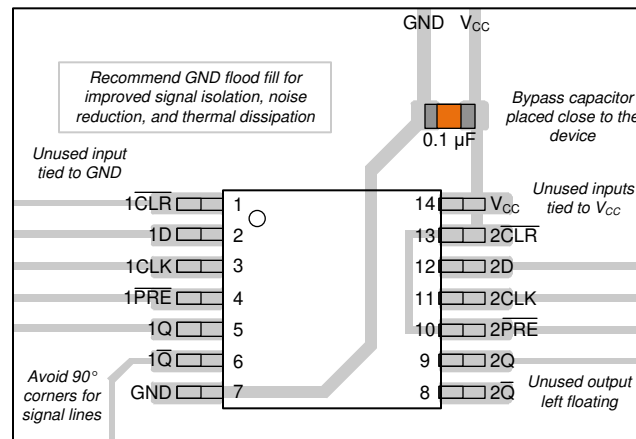
7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

7.2 Layout

7.2.1 Layout Guidelines

7.2.2 Layout Example



☒ 7-1. Example Layout for the in the SNx4AC74 Package

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AC74	Click here	Click here	Click here	Click here	Click here
SN74AC74	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.4 Trademarks

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8.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (October 2003) to Revision G (July 2024)	Page
<ul style="list-style-type: none"> 製品情報の表、ピンの機能の表、熱に関する情報の表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加..... Updated RθJA values: D = 86 to 119.9, PW = 113 to 145.7, all values in °C/W..... 	<p>1</p> <p>5</p>

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88520012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-88520012A SNJ54AC 74FK	Samples
5962-8852001CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8852001CA SNJ54AC74J	Samples
5962-8852001DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8852001DA SNJ54AC74W	Samples
5962-8852001VDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8852001VD A SNV54AC74W	Samples
SN74AC74D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	AC74	
SN74AC74DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC74N	Samples
SN74AC74NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC74N	Samples
SN74AC74NSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	AC74	
SN74AC74PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SN74AC74PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC74	Samples
SNJ54AC74FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-88520012A SNJ54AC 74FK	Samples
SNJ54AC74J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8852001CA SNJ54AC74J	Samples
SNJ54AC74W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8852001DA SNJ54AC74W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AC74, SN54AC74-SP, SN74AC74 :

- Catalog : [SN74AC74](#), [SN54AC74](#)
- Enhanced Product : [SN74AC74-EP](#), [SN74AC74-EP](#)
- Military : [SN54AC74](#)

- Space : [SN54AC74-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC74DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC74NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AC74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC74PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC74PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC74DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AC74DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AC74DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AC74DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AC74NSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74AC74PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AC74PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AC74PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AC74PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-88520012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8852001DA	W	CFP	14	25	506.98	26.16	6220	NA
5962-8852001VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AC74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AC74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AC74FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC74W	W	CFP	14	25	506.98	26.16	6220	NA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

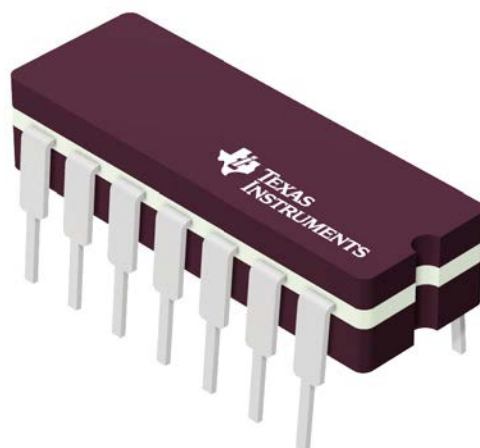
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

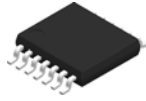
PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

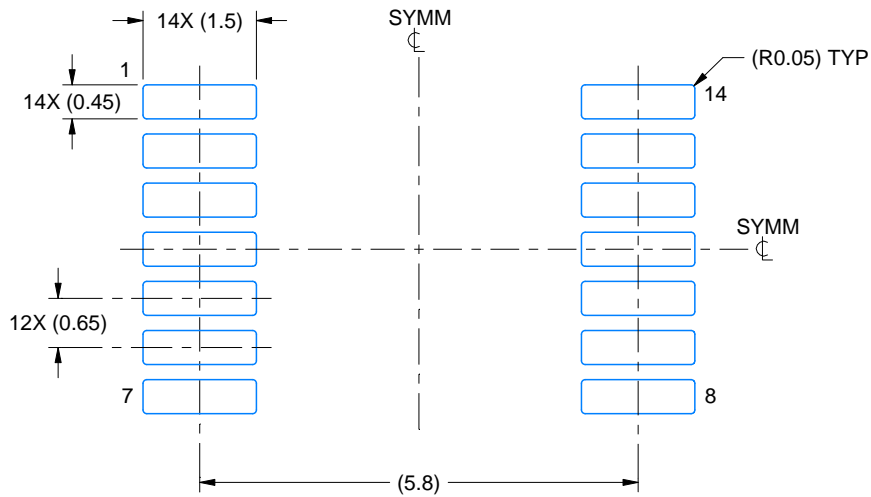
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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