SN4599-Q1 車載用 5V、2:1 (SPDT)、1 チャネル アナログ スイッチ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲:-40℃～125℃
  - デバイス HBM 分類レベル H1C
  - デバイス CDM 分類レベル C3
- レール ツー レールの動作
- 双方向の信号パス
- 低いオン抵抗:7Ω
- 幅広い電源電圧範囲:2V～5.5V
- –40℃～+125℃の動作温度
- ブレイク ビフォー メイクのスイッチング動作
- SN4599-Q1 NLAS4599-Q1 の直接代替品

2 アプリケーション

- アナログおよびデジタル スイッチング
- I2C および SPI バスの多重化
- 先進運転支援システム (ADAS)
- ボディ エレクトロニクスおよび照明
- インフォテインメントおよびクラスタ
- ゾーン アーキテクチャ
- 車体制御モジュール
- バッテリ管理システム
- テレマティクス
- 車載用ヘッド ユニット

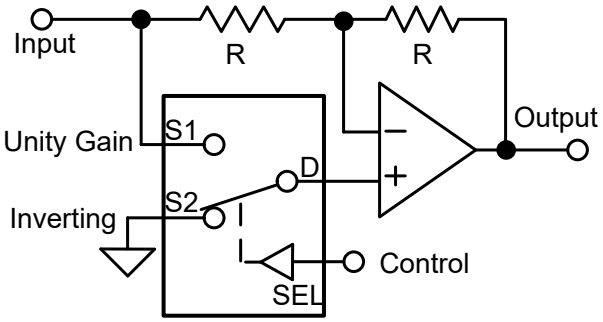
3 概要

SN4599-Q1 は、汎用の CMOS (相補型金属酸化膜半導体) 単極双投 (SPDT) スイッチです。SN4599-Q1 は、SEL ピンの状態に基づいて、2 つのソース入力間のスイッチングを行います。2V～5.5V の広い動作電源電圧範囲で、幅広い車載用アプリケーションに使用可能です。このデバイスは、ソース (Sx) およびドレイン (D) ピンで、GND から V_{DD} までの範囲の双方向アナログおよびデジタル信号をサポートします。

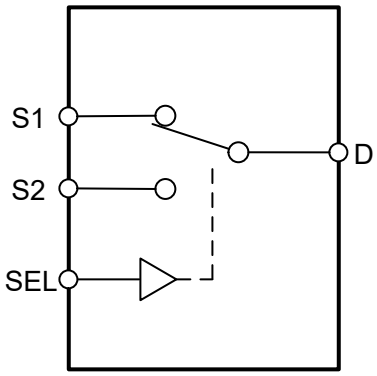
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
SN4599-Q1	DBV (SOT-23、6)	2.9mm × 2.8mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーションの例



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4 Pin Configuration and Functions

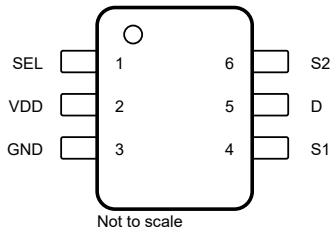


図 4-1. DBV Package 6-Pin SOT-23 (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SEL	1	I	Select pin: controls state of the switch according to 表 7-1. (Logic Low = S1 to D, Logic High = S2 to D)
VDD	2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
GND	3	P	Ground (0V) reference
S1	4	I/O	Source pin 1. Can be an input or output.
D	5	I/O	Drain pin. Can be an input or output.
S2	6	I/O	Source pin 2. Can be an input or output.

(1) I = input, O = output, I/O = input and output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	-0.5	6	V
V_{IN}	Control input voltage(2)	-0.5	6	V
$V_{I/O}$	Voltage range applied to any output in the high-impedance or power-off state(2) (3)	-0.5	V_{DD} + 0.5	V
I_{IK}	Control input clamp current V_{IN} < 0		-50	mA
$I_{I/O}$	I/O port diode current $V_{I/O}$ < 0 or $V_{I/O}$ > V_{DD}	-50	50	mA
$I_{I/O}$	On-state switch current(4) $V_{I/O}$ = 0 to V_{DD}	I_{DC} ± 10 %(7)	I_{DC} ± 10 %(7)	mA
P_{tot}	Total power dissipation		300	mW
T_j	Junction temperature		150	C
Storage temperature, T_{stg}		-65	150	C

(1) Operation outside the Absolute Maximum Rating may cause permanent device damage. Absolute Maximum Rating do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Condition. If used outside the Recommended Operating Condition but within the Absolute Maximum Rating, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground unless otherwise specified.
(3) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for $V_{I/O}$.
(4) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for $I_{I/O}$.
(5) Refer to *Source or Drain Current* table for I_{DC} specifications.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-002 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2		5.5	V
$V_{I/O}$	Switch input or output voltage (Max of V_{DD})		0		V_{DD}	V
V_{IN}	Control input voltage		0		5.5	V
V_{IH}	High-level input voltage	V_{DD} = 2V to 2.29V	V_{DD} x 0.75			V
		V_{DD} = 2.3V to 5.5V	V_{DD} x 0.7			
V_{IL}	Low-level input voltage	V_{DD} = 2V to 2.29V			V_{DD} x 0.25	V
		V_{DD} = 2.3V to 2.9V			V_{DD} x 0.3	
		V_{DD} = 3V to 5V			0.85	

5.4 Thermal Information

THERMAL METRIC (1)		SN4599-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	212.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	96.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	80.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	96.	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Source or Drain Current through Switch

Current through the Switch	T_J = 25°C	T_J = 85°C	T_J = 125°C	T_J = 130°C	UNIT
I_{DC} (1)	150	120	60	50	mA
I_{peak} (2)	300	300	180	160	mA

(1) See ***Thermal Considerations*** section for more details
(2) Pulse current of 1ms with 10% Duty Cycle

5.6 Electrical Characteristics

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SN4599-Q1									
		V_{DD} V	$V_{I/o}$ V	I_O mA	T_A				
r_{ON}	ON-state switch resistance	2 V	V_I = 0 V	I_O = 4 mA	25°C		11		Ω
					–40°C to +85°C			20	
					–40°C to +125°C			20	
			V_I = 1.65	I_O = -4 mA	25°C		15		
					–40°C to +85°C			50	
					–40°C to +125°C			50	
		2.3 V	V_I = 0 V	I_O = 8 mA	25°C		8		
					–40°C to +85°C			12	
					–40°C to +125°C			12	
			V_I = 2.3 V	I_O = -8 mA	25°C		11		
					–40°C to +85°C			30	
					–40°C to +125°C			30	
		3 V	V_I = 0 V	I_O = 24 mA	25°C		7		
					–40°C to +85°C			9	
					–40°C to +125°C			9	
			V_I = 3 V	I_O = -24 mA	25°C		9		
					–40°C to +85°C			20	
					–40°C to +125°C			20	
		4.5 V	V_I = 0 V	I_O = 30 mA	25°C		6		
					–40°C to +85°C			7	
					–40°C to +125°C			7	
			V_I = 2.4 V	I_O = 30 mA	25°C		7		
					–40°C to +85°C			12	
					–40°C to +125°C			12	
			V_I = 4.5 V	I_O = -30 mA	25°C		7		
					–40°C to +85°C			15	
					–40°C to +125°C			15	
r_{range}	ON-state switch resistance over signal range	2 V	$0 \le V_{Sn} \le V_{DD}$	I_D = -4 mA	25°C			210	Ω
					–40°C to +85°C			210	
					–40°C to +125°C			210	
		2.3 V		I_D = -8 mA	25°C			85	
					–40°C to +85°C			85	
					–40°C to +125°C			85	
		3 V		I_D = -24 mA	25°C			30	
					–40°C to +85°C			30	
					–40°C to +125°C			30	
		4.5 V		I_D = -30 mA	25°C			18	
					–40°C to +85°C			18	
					–40°C to +125°C			18	

5.6 Electrical Characteristics (続き)

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
Δr_{ON}	Maximum ON resistance between any two channels	2 V	V_{Sn} = 1.15 V	I_D = -4 mA	25°C		0.5		Ω
					–40°C to +85°C		0.5		
					–40°C to +125°C		0.5		
		2.3 V	V_{Sn} = 1.6 V	I_D = -8 mA	25°C		0.1		
					–40°C to +85°C		0.1		
					–40°C to +125°C		0.3		
		3 V	V_{Sn} = 2.1 V	I_D = -24 mA	25°C		0.1		
					–40°C to +85°C		0.1		
					–40°C to +125°C		0.3		
		4.5 V	V_{Sn} = 3.15 V	I_D = -30 mA	25°C		0.1		
					–40°C to +85°C		0.1		
					–40°C to +125°C		0.2		
$r_{on(flat)}$	ON resistance flatness	2 V	0 ≤ V_{Sn} ≤ V_{DD}	I_D = -4 mA	25°C		110		Ω
					–40°C to +85°C		110		
					–40°C to +125°C		110		
		2.3 V		I_D = -8 mA	25°C		26		
					–40°C to +85°C		26		
					–40°C to +125°C		40		
		3 V		I_D = -24 mA	25°C		9		
					–40°C to +85°C		9		
					–40°C to +125°C		10		
		4.5 V		I_D = -30 mA	25°C		4		
					–40°C to +85°C		4		
					–40°C to +125°C		5		
Ioff	Switch OFF leakage current	2 V	V_S = 1 V / 1.62 V V_D = 1.62 V / 1 V		25°C		±5		nA
					–40°C to +85°C			±25	
					–40°C to +125°C			±100	
		5.5 V	V_S = 4.5 V / 1.5 V V_D = 1.5 V / 4.5 V		25°C		±5		
					–40°C to +85°C			±25	
					–40°C to +125°C			±100	
$I_{S(on)}$	ON-state switch leakage current	5.5	V_I = V_{DD} or GND, V_O = Open		25°C		±15		nA
					–40°C to +85°C			±50	
					–40°C to +125°C			±100	
I_{IN}	Control input current	0 V to 5.5 V	0 ≤ V_{IN} ≤ V_{DD}		25°C		±0.05	±0.1	μA
					–40°C to +85°C			±1	
					–40°C to +125°C			±1	
I_{DD}	Supply current	5.5 V	SEL = V_{DD} or GND		25°C		1		μA
					–40°C to +85°C			10	
					–40°C to +125°C			35	
C_I	Control input capacitance	5 V	SEL (V_{DD}/2)		25°C		2.7		pF
					–40°C to +85°C		2.7		
					–40°C to +125°C		2.7		

5.6 Electrical Characteristics (続き)

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$C_{io(off)}$	Switch input/output capacitance	5 V	Sn (V_{DD}/2)	25°C		5.2		pF
				–40°C to +85°C		5.2		
				–40°C to +125°C		5.2		
$C_{io(on)}$	Switch input/output capacitance	5 V	Sn (V_{DD}/2)	25°C		21		pF
				–40°C to +85°C		21		
				–40°C to +125°C		21		
			D (V_{DD}/2)	25°C		21		
				–40°C to +85°C		21		
				–40°C to +125°C		21		

(1) T_A = 25C

5.7 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{DD}	MIN	NOM	MAX	UNIT
Frequency response (switch on)	D or Sn	Sn or D	R_L = 50 Ω, f_{in} = sine wave	2 V		250		MHz
				2.3 V		250		
				3 V		250		
				4.5 V		250		
Crosstalk (between switches)	S1 or S2	S2 or S1	R_L = 50 Ω, f_{in} = 1MHz sine wave	2 V		-54		dB
				2.3 V		-54		
				3 V		-54		
				4.5 V		-54		
Feed through attenuation (switch off)	D or Sn	Sn or D	C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave)	2 V		-57		dB
				2.3 V		-57		
				3 V		-57		
				4.5 V		-57		
Charge injection	SEL (Vs = V_{DD}/2)	D	C_L = 0.1 nF, R_L = 1 MΩ	3.3 V		3		pC
				5 V		7		
Total harmonic distortion	D or Sn	Sn or D	V_I = 4.0 V_{p-p}, Vbias = V_{DD}/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	4.5 V		0.01		%

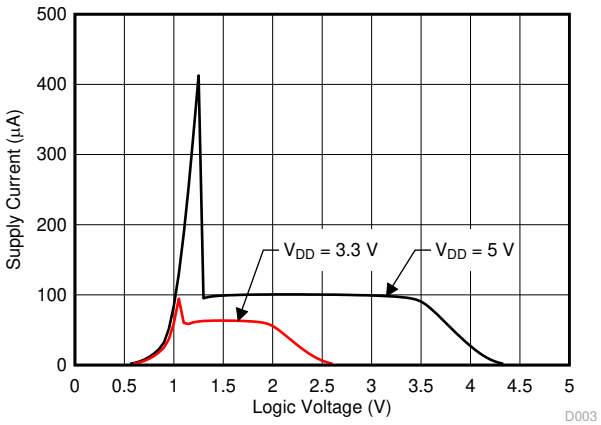
5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

Parameter		FROM (INPUT)	TO (OUTPUT)	V_{DD}	MIN	NOM	MAX	UNIT
t_{tran}	R_L = 200Ω, C_L = 15pF, V_S = 1V	D or Sn	Sn or D	2 V ± 0.15 V		28		ns
							44	
							44	
	R_L = 200Ω, C_L = 15pF, V_S = 2V	D or Sn	Sn or D	3.3 V ± 0.3 V		14		ns
							20	
							21	
	R_L = 200Ω, C_L = 15pF, V_S = 3V	D or Sn	Sn or D	5 V ± 0.5 V		12		ns
							18	
							19	
T_{B-M}	Break before make time			2 V ± 0.15 V	0.5			ns
				2.5 V ± 0.2 V	0.5			
				3.3 V ± 0.3 V	0.5			
				5 V ± 0.5 V	0.5			

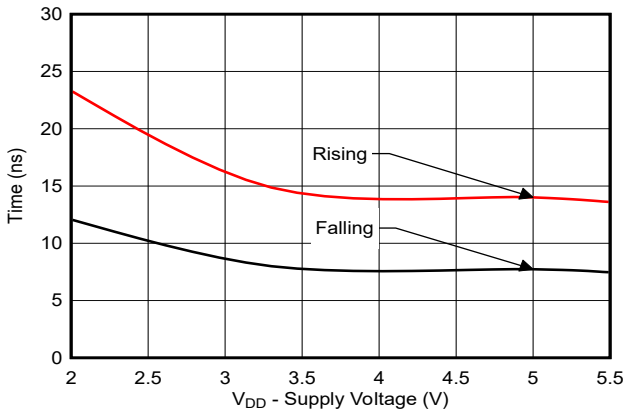
5.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



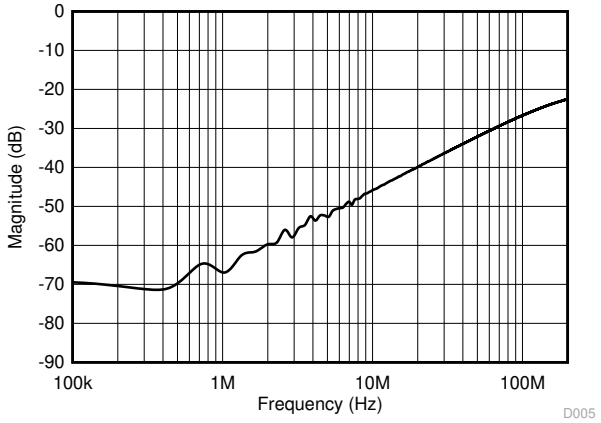
T_A = 25°C

図 5-1. Supply Current vs Logic Voltage



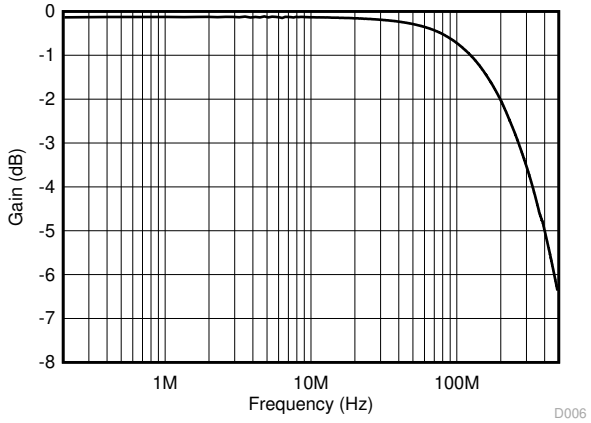
T_A = 25°C

図 5-2. $T_{transition}$ vs Supply Voltage



T_A = 25°C

図 5-3. Crosstalk and Off-Isolation vs Frequency



T_A = 25°C

図 5-4. Frequency Response

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 6-1. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

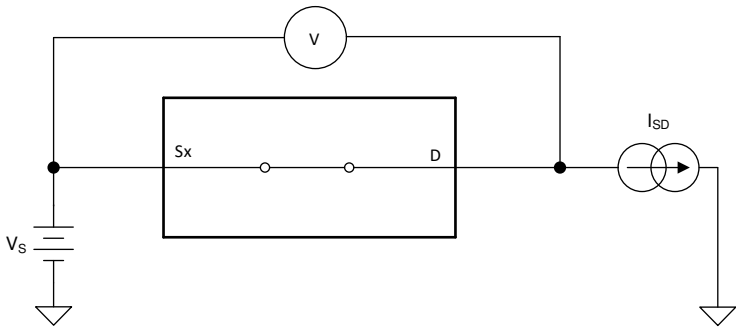


図 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

The setup used to measure off-leakage current is shown in 図 6-2.

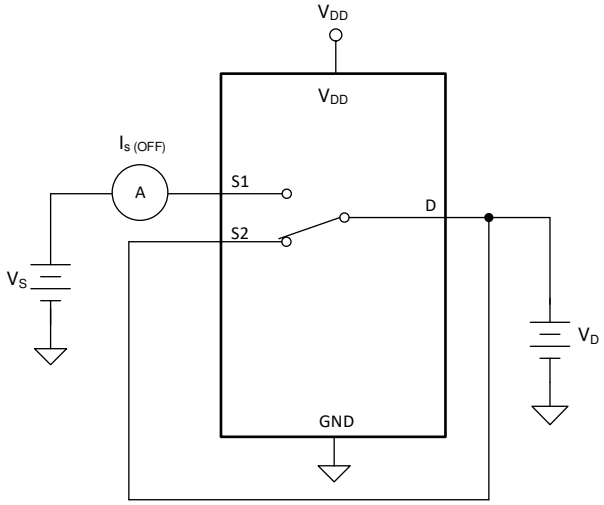


図 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 図 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

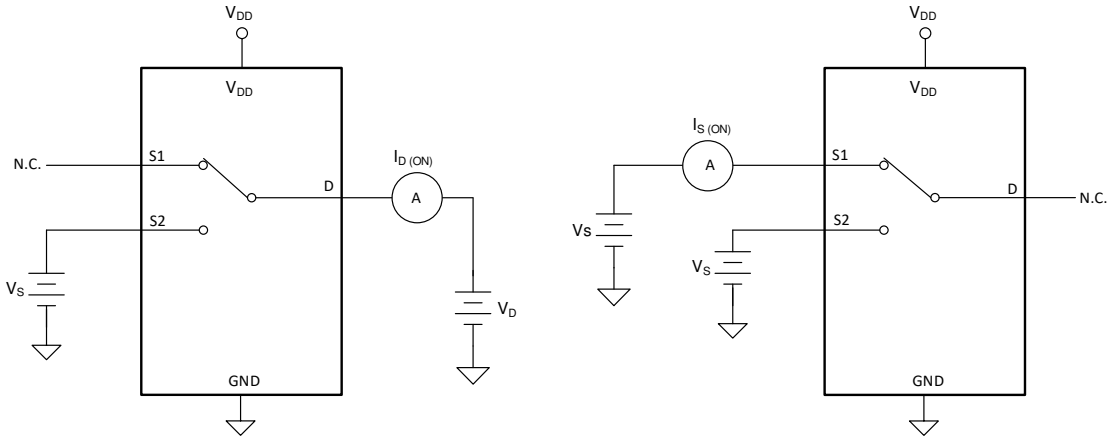


図 6-3. On-Leakage Measurement Setup

6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the logic control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 図 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

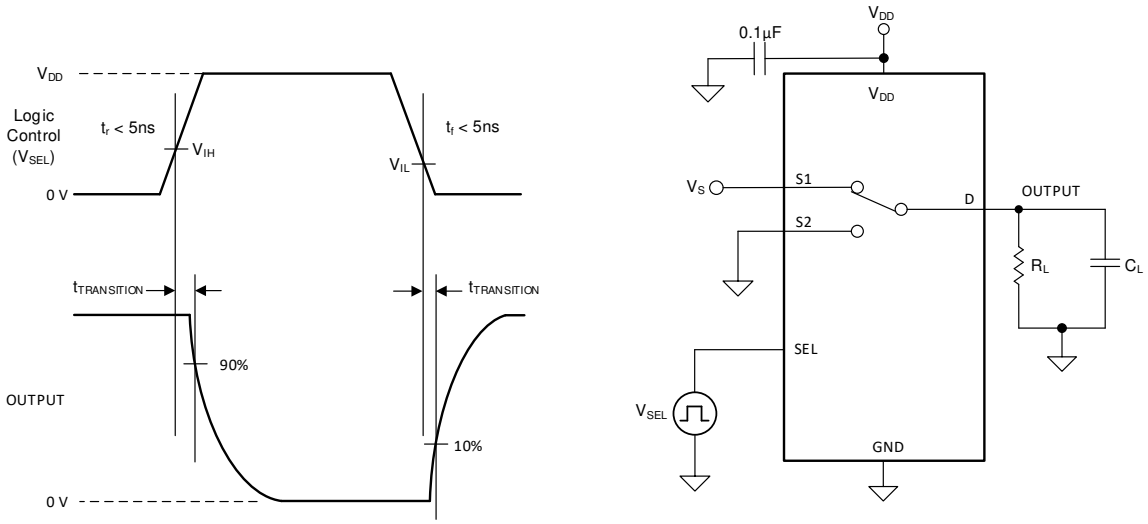


図 6-4. Transition-Time Measurement Setup

6.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 図 6-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

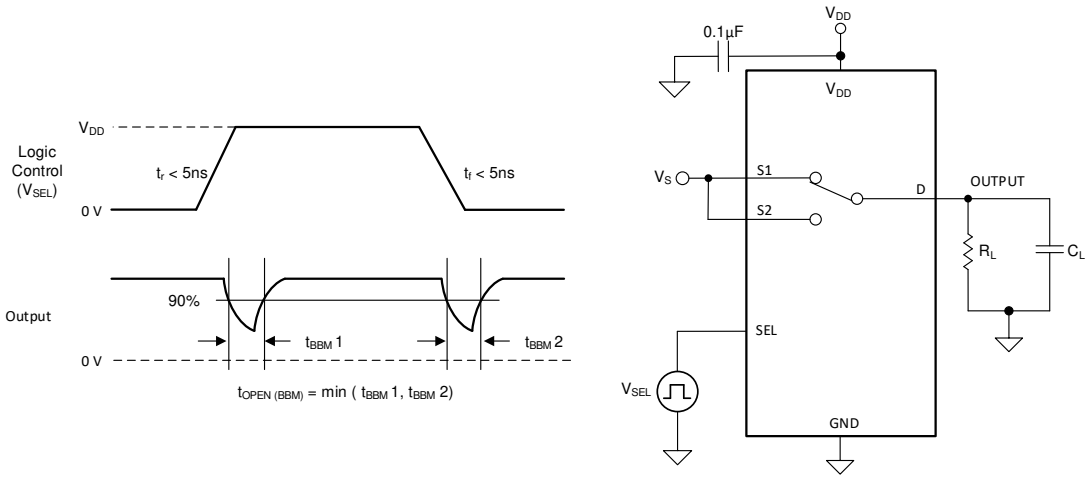


図 6-5. Break-Before-Make Delay Measurement Setup

6.6 Charge Injection

The SN4599-Q1 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 図 6-6 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

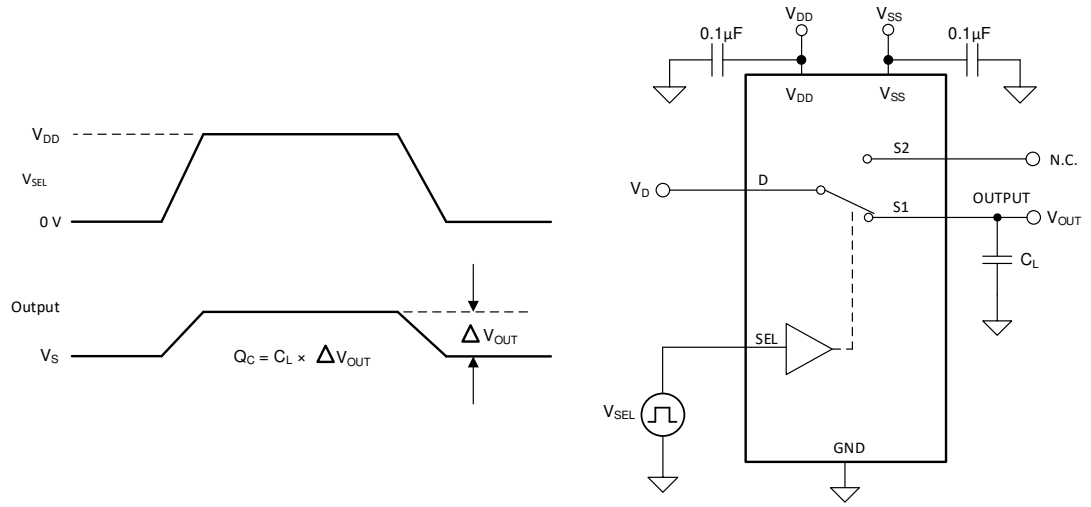


図 6-6. Charge-Injection Measurement Setup

6.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 図 6-7 shows the setup used to measure, and the equation used to calculate off isolation.

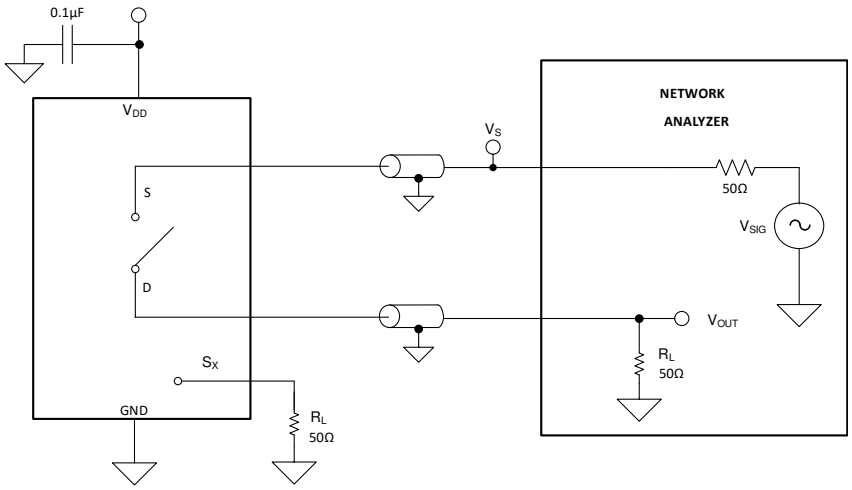


図 6-7. Off Isolation Measurement Setup

$$Off\ Isolation\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

6.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 図 6-8 shows the setup used to measure, and the equation used to calculate crosstalk.

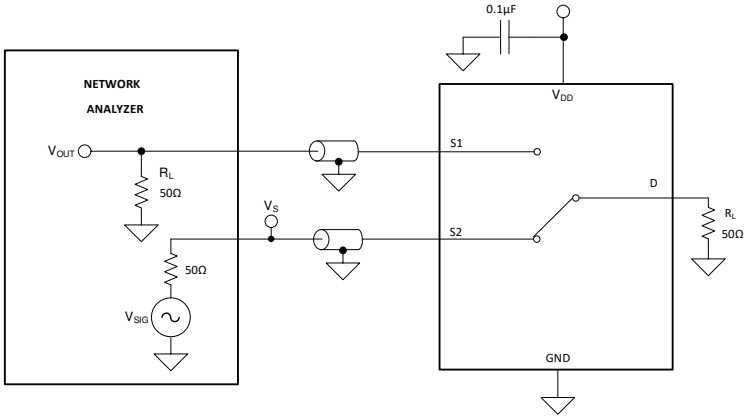


図 6-8. Crosstalk Measurement Setup

$$Channel-to-Channel\ Crostalk\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

6.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 図 6-9 shows the setup used to measure bandwidth.

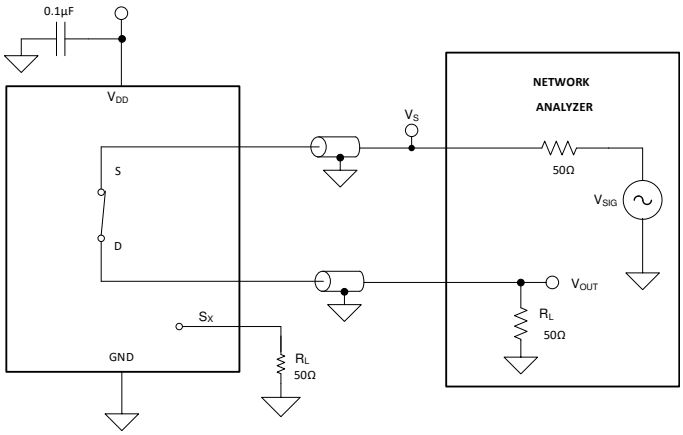


図 6-9. Bandwidth Measurement Setup

7 Detailed Description

7.1 Functional Block Diagram

The SN4599-Q1 is an 2:1 (SPDT), 1-channel switch where the input is controlled with a single select (SEL) control pin.

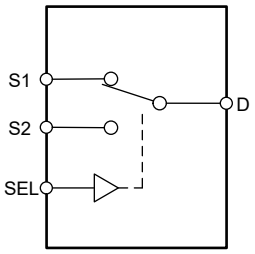


図 7-1. SN4599-Q1 Functional Block Diagram

7.2 Feature Description

7.2.1 Bidirectional Operation

The SN4599-Q1 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

7.2.2 Rail to Rail Operation

The valid signal path input/output voltage for SN4599-Q1 ranges from GND to V_{DD}.

7.2.3 Fail-Safe Logic

The SN4599-Q1 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the SN4599-Q1 to be ramped to 5.5V while V_{DD} = 0V. Additionally, the feature enables operation of the SN4599-Q1 with V_{DD} = 2V while allowing the select pin to interface with a logic level of another device up to 5.5V.

7.3 Device Functional Modes

The select (SEL) pin of the SN4599-Q1 controls which source channel is connected to the drain of the device. When a signal path is not selected, that source pin is in high impedance mode (HI-Z). The control pin can be as high as 5.5V.

7.4 Truth Tables

表 7-1. SN4599-Q1 Truth Table

CONTROL LOGIC (SEL)	Selected Source (Sx) Connected To Drain (D) Pin
0	S1
1	S2

8 Application and Implementation

注

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8.1 Application Information

SN4599-Q1 offers good system performance across a wide operating supply (2V to 5.5V). Additionally, the control input pin supports Fail-Safe Logic which allows for operation up to 5.5V, regardless of the state of the supply pin. This protection stops the logic pins from back-powering the supply rail. These features of the SN4599-Q1 general purpose multiplexer, reduce system complexity, board size, and overall system cost.

8.2 Typical Application

8.2.1 Switchable Operational Amplifier Gain Setting

One example application of the SN4599-Q1 is to change an Op Amp from unity gain setting to an inverting amplifier configuration. Utilizing a switch allows a system to have a configurable gain and allows the same architecture to be utilized across the board for various inputs to the system. 図 8-1 shows the SN4599-Q1 configured for gain setting application.

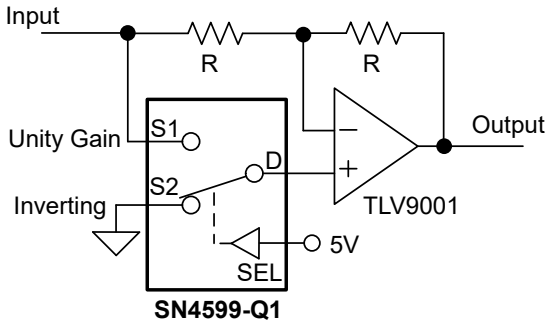


図 8-1. Switchable Op Amp Gain Setting

8.2.1.1 Design Requirements

This design example uses the parameters listed in 表 8-1.

表 8-1. Design Parameters

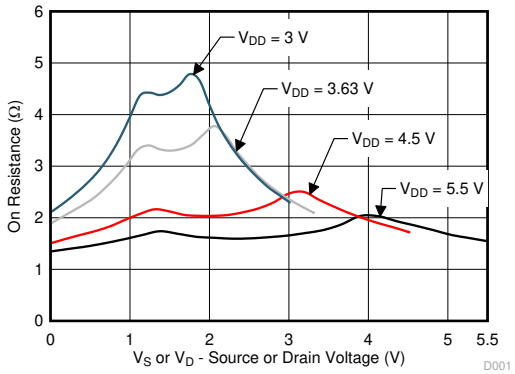
PARAMETERS	VALUES
Input Signal	0V to 3.3V
Mux Supply (V_{DD})	3.3V
Op Amp Supply (V_+/ V_-)	±3.3V
Mux I/O signal range	0V to V_{DD} (Rail to Rail)
Control logic thresholds	2.31V up to 5.5V

8.2.1.2 Detailed Design Procedure

The application shown in 図 8-1 demonstrates how to use a single control input and toggle between gain settings of -1 and +1. If switching between inverting and unity gain is not required, then the SN4599-Q1 can be utilized in the feedback path to select different feedback resistors and provide scalable gain settings for configurable signal conditioning.

The SN4599-Q1 can operate without any external components except for the supply decoupling capacitors. It is recommended to have a weak pull-down or pull-up resistor so that the input of the select pin is in a known state. All inputs to the switch must fall within the recommend operating conditions of the SN4599-Q1 including signal range and continuous current. For this design with a supply of 3.3V, the signal range can be 0V to 3.3V and the maximum continuous current can be 30mA.

8.2.1.3 Application Curve



T_A = 25°C

図 8-2. On-Resistance vs Source or Drain Voltage

8.2.2 Input Control for Power Amplifier

Another application of the SN4599-Q1 is for input control of a power amplifier. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate to GND. 図 8-3 shows the SN4599-Q1 configured for control of the power amplifier.

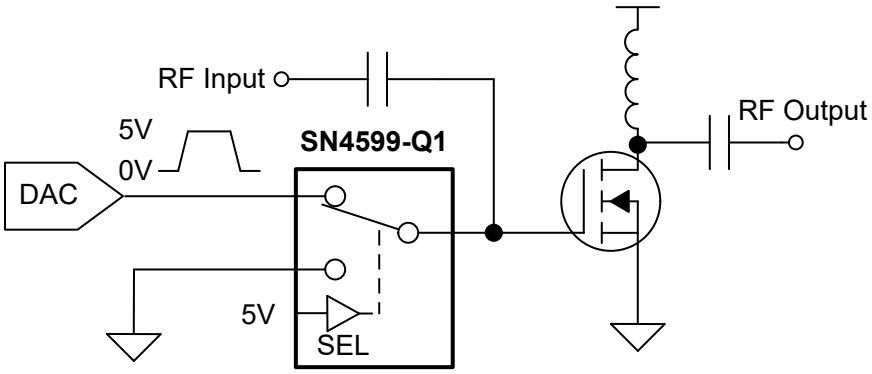


図 8-3. Input Control of Power Amplifier

8.2.2.1 Design Requirements

This design example uses the parameters listed in 表 8-1.

表 8-2. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	5V
Mux I/O signal range	0V to V_{DD} (Rail to Rail)
Control logic thresholds	Up to 5.5V

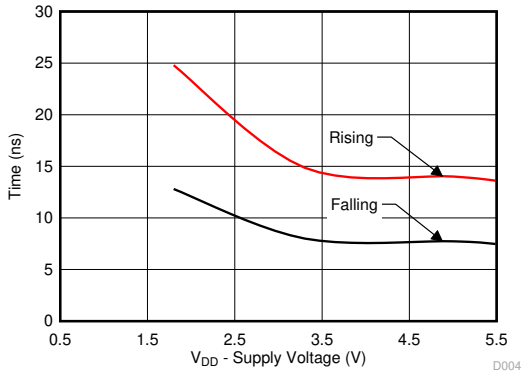
8.2.2.2 Detailed Design Procedure

The application shown in 図 8-3 demonstrates how to toggle between the DAC output and GND to control a power amplifier using a single control input. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pin of the switch.

The SN4599-Q1 can operate without any external components except for the supply decoupling capacitors. It is recommended to have a weak pull-down or pull-up resistor so that the input of the select pin is in a known state. All inputs to the switch must fall within the recommend operating conditions of the SN4599-Q1 including signal range and continuous current. For this design with a supply of 5V, the signal range can be 0V to 5V and the maximum continuous current can be 30mA.

8.2.2.3 Application Curve

A key parameter for this application is the transition time of the device. Faster transition time allows the system to toggle between input sources at a faster rate and allows the output to settle to the final value. The SN4599-Q1 has a transition time that varies with supply voltage and is shown in 図 8-4



T_A = 25°C

図 8-4. $T_{transition}$ vs Supply Voltage

8.3 Power Supply Recommendations

The SN4599-Q1 operates across a wide supply range of 2V to 5.5V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must

turn corners. 図 8-5 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

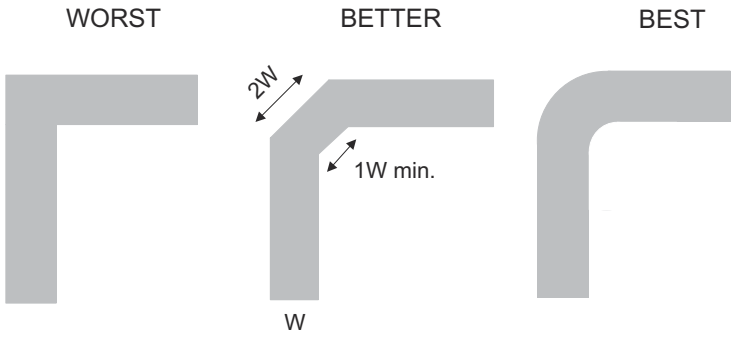


図 8-5. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

図 8-6 shows an example of a PCB layout with the SN4599-Q1. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

8.4.2 Layout Example

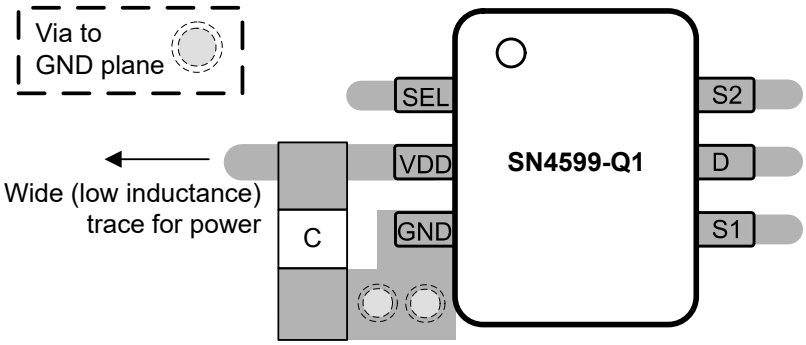


図 8-6. SN4599-Q1 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* .
- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches* .
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* .

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

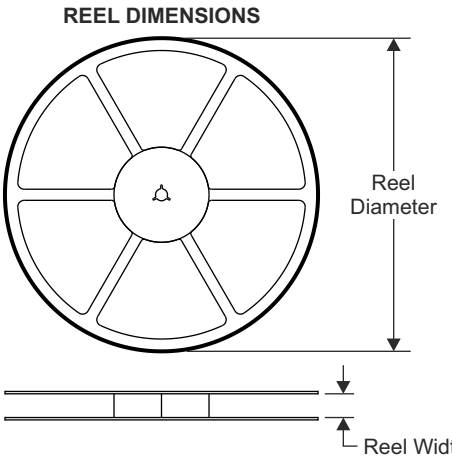
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

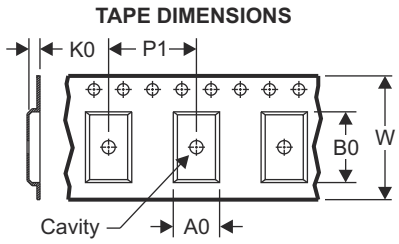
Changes from Revision * (April 2024) to Revision A (July 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

11 Mechanical, Packaging, and Orderable Information

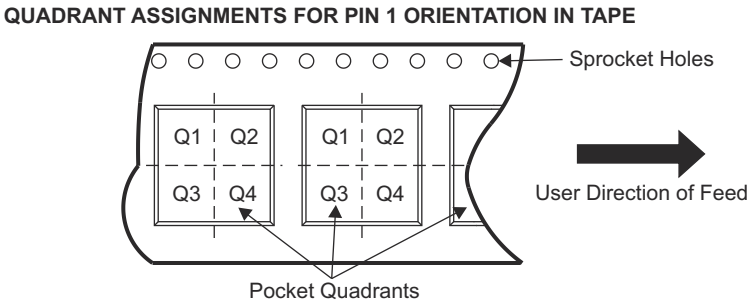
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information



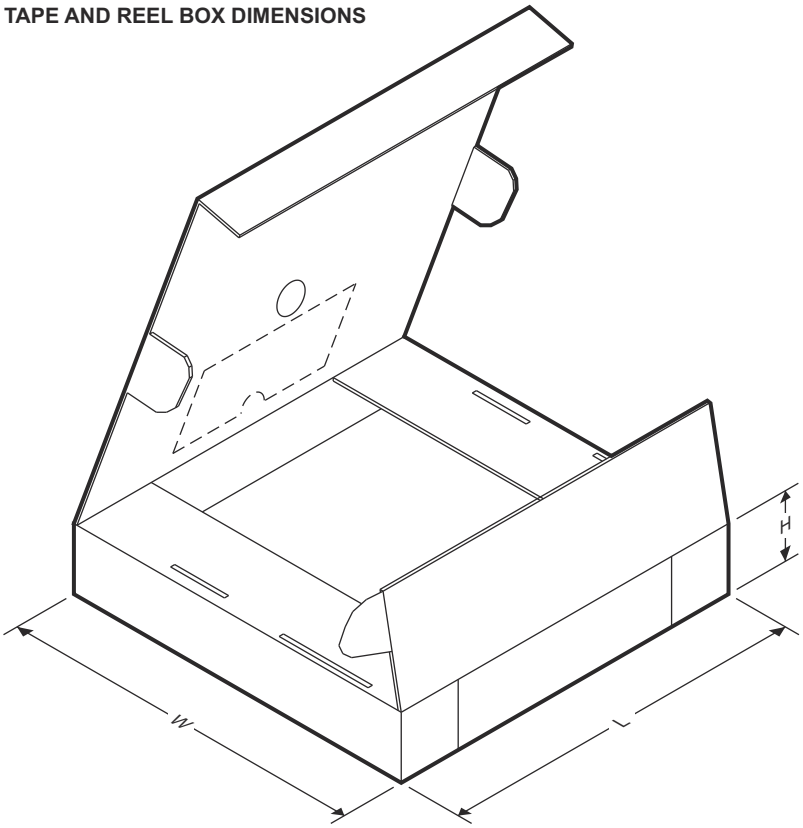


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN4599DBVRQ1	SOT-23	DBV	6	3000	178	9	2.4	2.5	1.2	4	8	Q3

TAPE AND REEL BOX DIMENSIONS



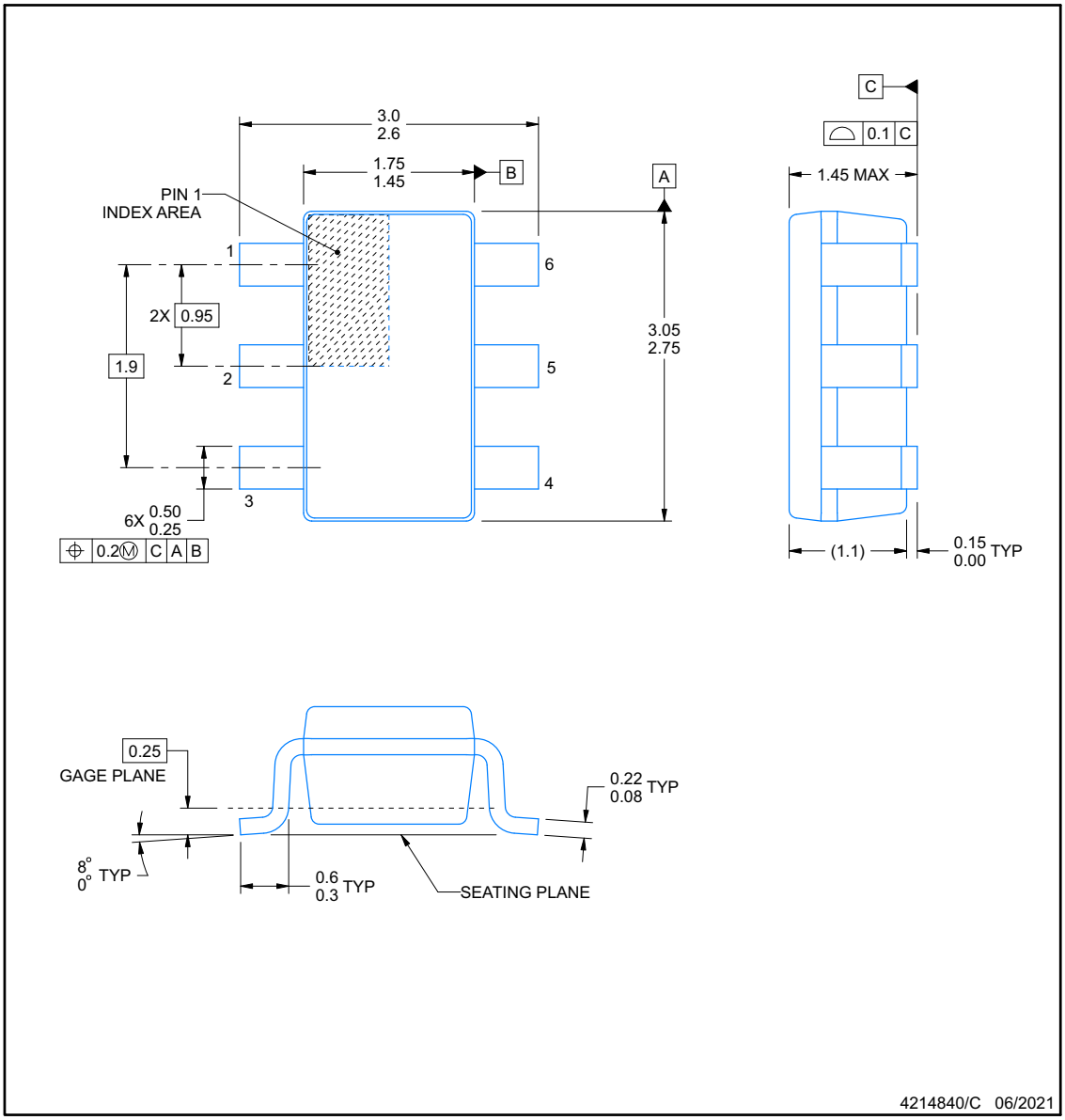
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN4599DBVRQ1	SOT-23	DBV	6	3000	180	180	18

11.2 Mechanical Data

PACKAGE OUTLINE

DBV0006A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



NOTES:

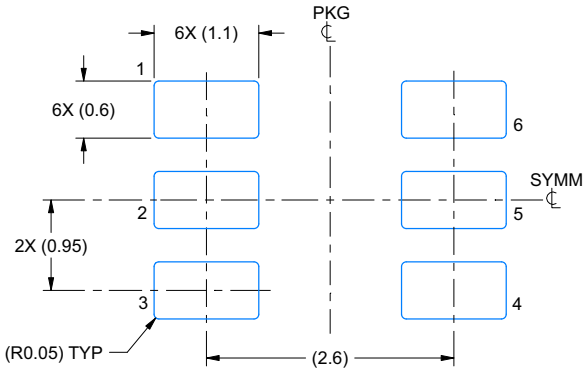
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

EXAMPLE BOARD LAYOUT

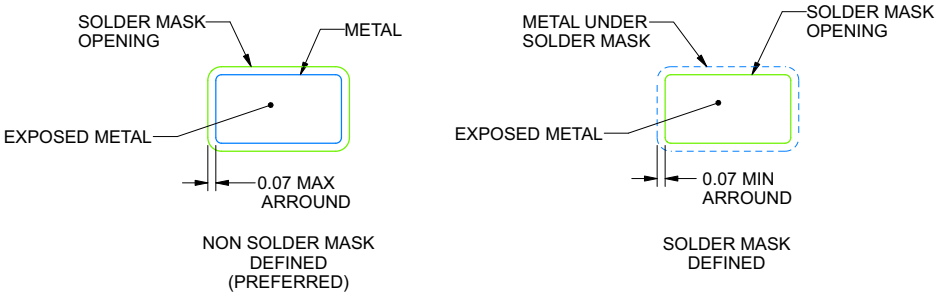
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

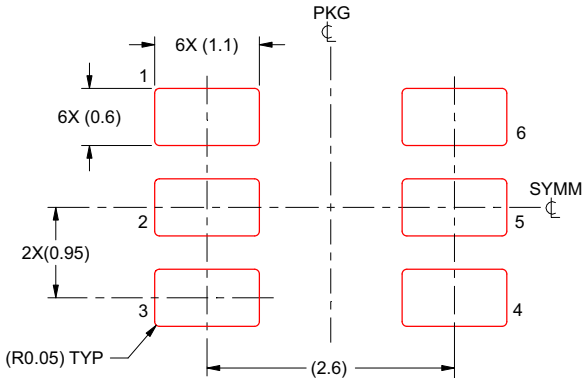
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN4599DBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3GTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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