

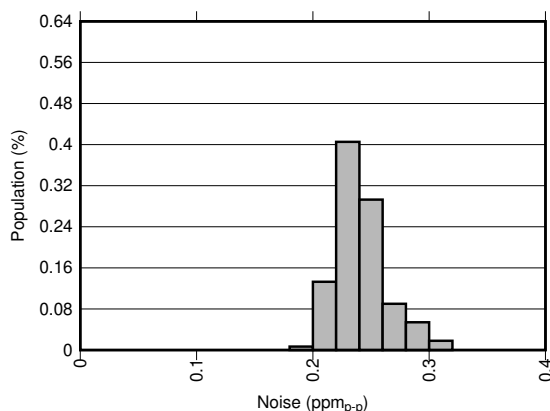
REF70 ドリフト係数 2ppm/°C以下、1/f ノイズ 0.23ppm_{p-p} の高精度電圧リファレンス

1 特長

- 高精度測定を可能にする低ノイズ
 - 1/f ノイズ (0.1Hz~10Hz): 0.23ppm_{p-p}
 - 10Hz~1kHz: 0.35ppm_{rms}
- 低温度ドリフト係数:
 - 2ppm/°C以下 (-40°C~125°C)
- 高精度: ±0.025% 以下
- 耐湿性に優れた気密セラミック・パッケージ (LCCC)
- 優れた長期安定性 (1k 時間): 35ppm
- 低ドロップアウト: 400mV
- 多様なアプリケーションに適した設計:
 - 最大入力電圧: 18V
 - 出力電流: ±10mA
 - 電圧オプション: 1.25V、2.5V、3V、3.3V、4.096V、5V
- 非常に柔軟なソリューション:
 - 1μF~100μF の出力低 ESR コンデンサで安定
 - 高 PSRR: 1kHz 時に 107dB
 - 動作温度範囲: -40°C~+125°C

2 アプリケーション

- 半導体試験用機器
- 高精度データ・アキュイジション・システム
- 高精度重量計
- 超音波スキャナ
- X 線システム
- 産業用計測機器
- PLC アナログ I/O モジュール
- フィールド・トランスミッタ
- 電力監視



0.1Hz~10Hz の電圧ノイズの分布

3 概要

REF70 は、業界最小のノイズ (0.23ppm_{p-p})、非常に小さい温度ドリフト係数 (2ppm/°C)、高い精度 (±0.025%) を特長とする高精度シリーズ電圧リファレンスのファミリです。厳しい過渡要件を満たせるように、REF70 は高 PSRR、低ドロップアウト電圧、優れた負荷 / ライン・レギュレーションを実現しています。この精度と機能の組み合わせは、高精度、高分解能データ・コンバータ (ADS8900B、ADS127L01、DAC11001A など) と一緒に高精度リファレンスを使って信号チェーン性能を最適化する必要があるテスト / 測定などのアプリケーションのために設計されています。REF70 は、アナログ・フロント・エンドによる低ノイズ測定が必要な、ノイズに敏感な医療用アプリケーション (超音波、X 線など) にも適しています。

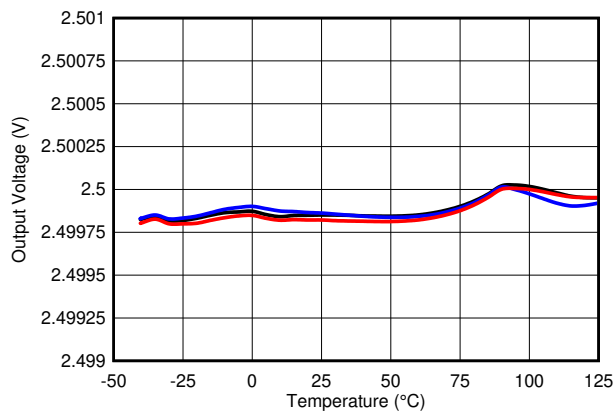
REF70 ファミリは VSSOP および LCCC パッケージ・オプションで供給されます。LCCC (FKH) パッケージは、キャリブレーションなしで長期間安定して動作するリファレンスを必要とするアプリケーションのために小さい長期ドリフトを実現できる気密封止セラミック・パッケージです。

REF70 は、-40°C~+125°Cの広い温度範囲で動作が規定されています。この広い温度範囲により各種産業用アプリケーションでの動作が可能になっています。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
REF70	LCCC (8)	5.00mm × 5.00mm
	VSSOP (8)	3.00mm × 3.00mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



出力電圧と周囲温度との関係



Table of Contents

1 特長	1	8.4 Noise Performance.....	22
2 アプリケーション	1	8.5 Temperature Drift.....	25
3 概要	1	8.6 Power Dissipation.....	25
4 Revision History	2	9 Detailed Description	26
5 Device Comparison Table	4	9.1 Overview.....	26
6 Pin Configuration and Functions	5	9.2 Functional Block Diagram.....	26
7 Specifications	6	9.3 Feature Description.....	26
7.1 Absolute Maximum Ratings.....	6	9.4 Device Functional Modes.....	26
7.2 ESD Ratings.....	6	10 Application and Implementation	28
7.3 Recommended Operating Conditions.....	6	10.1 Application Information.....	28
7.4 Thermal Information.....	6	10.2 Typical Applications.....	28
7.5 REF7012 Electrical Characteristics.....	7	10.3 Power Supply Recommendation.....	33
7.6 REF7025 Electrical Characteristics.....	8	10.4 Layout.....	33
7.7 REF7030 Electrical Characteristics.....	9	11 Device and Documentation Support	35
7.8 REF7033 Electrical Characteristics.....	10	11.1 Documentation Support.....	35
7.9 REF7040 Electrical Characteristics.....	11	11.2 ドキュメントの更新通知を受け取る方法.....	35
7.10 REF7050 Electrical Characteristics.....	13	11.3 サポート・リソース.....	35
7.11 Typical Characteristics.....	15	11.4 Trademarks.....	35
8 Parameter Measurement Information	20	11.5 静電気放電に関する注意事項.....	35
8.1 Solder Heat Shift.....	20	11.6 用語集.....	35
8.2 Long-Term Stability.....	21	12 Mechanical, Packaging, and Orderable Information	35
8.3 Thermal Hysteresis.....	21		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (March 2023) to Revision G (September 2023)	Page
• Update table to highlight REF7025 and REF7040 release in VSSOP package.....	4
• Added performance parameters for VSSOP package.....	8
• Added performance parameters for VSSOP package.....	11
• Changed 図 7-25 to longer duration (10000 hours).....	15
• Added 図 7-27	15
• Changed 図 8-4 and 図 8-4 , to longer duration (10000 hours).....	21
• Changed 図 8-10 , to highlight performance at different supply voltages.....	22
• Changed minimum ESR value from 10 mΩ to 1 mΩ.....	26
• Changed minimum ESR value from 10 mΩ to 1 mΩ.....	29

Changes from Revision E (July 2022) to Revision F (March 2023)	Page
• 読みやすさの向上のため、電圧オプション機能に改訂を追加.....	1
• VSSOP パッケージのプレビューの脚注を削除.....	1
• Added footnote to indicate VSSOP package preview material.....	4
• Added performance parameters for VSSOP package.....	7
• Added performance graphs for VSSOP package devices.....	15
• Added solder shift histogram for VSSOP package.....	20
• Added long term stability details for VSSOP package.....	21
• Added thermal hysteresis details for VSSOP package.....	21
• Added layout details for VSSOP package.....	34

Changes from Revision D (November 2021) to Revision E (July 2022)	Page
ドキュメントのフィードバックに基づいて長期安定性機能のテキストを更新し、追加のテストを実施して数値を 28ppm から 35ppm に更新。.....	1
VSSOP パッケージの「製品情報」表の脚注を追加。.....	1
Updated Long-term stability numbers to reflect latest evaluation results.....	8
Changed 図 7-25 to longer duration (4000 hours).....	15
Changed 図 8-4 , to longer duration (4000 hours).....	21

Changes from Revision C (September 2021) to Revision D (November 2021)	Page
Changed REF7012 status from Preproduction device to Released device.....	4
Changed REF7012 status to Released Device. Updated specifications to meet production release device.....	7
Added REF7030 Electrical Characteristics table.....	9
Added REF7033 Electrical Characteritics table.....	10
Added REF7012 Thermal Hysteresis figure.....	15
Added JEDEC standard details to follow for solder reflow profiles. Updated solder shift histogram plot.....	20
Added Thermal Hysteresis plots for REF7012 device	21

Changes from Revision B (April 2021) to Revision C (September 2021)	Page
ページ 1 の「特長」に 1.25V のバリエントを追加.....	1
In the Device Comparison Table, added the 1.25V variant and added foot notes to indicate which devices are released vs pre-production	4
Changed Dropout voltage to min VIN = 2.75 V for VOUT < 2.5 V.	6
Added Electrical Characteristics table for REF7012 (Product Preview).....	7
Changed VINMIN from 3 V to VOUT + VDO	8
Added Electrical Characteristics table for REF7040 (Product Preview).....	11
Added Electrical Characteristics table for REF7050 (Product Preview).....	13
Added to the notes above the Typical Characteristics plots, Vref = 2.5 V to the default conditions.....	15
Under Temperature Drift section of the Parameter Measurement Information, corrected the figure from Long Term Drift plot to Temperature Drift.....	25

Changes from Revision A (December 2020) to Revision B (April 2021)	Page
見出しと製品情報の REF7025 をより一般的な REF70 シリーズに変更。ADC コンパニオン製品を追加。.....	1
Changed Figures 7-2 and 7-20, <i>Long-Term Stability (First 1000 Hours)</i> , to longer duration (2000 hours).....	15
Corrected typical shift from 0.021% to 0.009%.....	20
Changed Figure 8-3, <i>Long-Term Stability LCCC -1000 hours</i> , to longer duration (2000 hours).....	21
Corrected Figure 8-5, <i>Thermal Hysteresis Distribution Cycle 2 (-40°C to 125°C)</i> , data and title.....	21
Reordered figures and paragraphs for better flow.....	24
Changed VREF to VREF(25°C) in Equation 2.....	25
Added missing supply bypass capacitor value (10-μF).....	26
Clarified piezoelectric contribution to noise and added links to resources.....	29
Added clarification on how to connect OUTF and OUTS in specific load current condition.....	30
Corrected part numbers and added links in Table 10-2, <i>Reference Op Amp Options</i>	31

Changes from Revision * (October 2020) to Revision A (December 2020)	Page
APL から RTM へのリリース.....	1

5 Device Comparison Table

PRODUCT		V _{out}
LCC package	VSSOP package	
REF7012QFKHT ⁽¹⁾	REF7012QDGKR ⁽¹⁾	1.25 V
REF7025QFKHT ⁽¹⁾	REF7025QDGKR ⁽¹⁾	2.5 V
REF7030QFKHT ⁽¹⁾	REF7030QDGKR ²	3.0 V
REF7033QFKHT ⁽¹⁾	REF7033QDGKR ²	3.3 V
REF7040QFKHT ⁽¹⁾	REF7040QDGKR ⁽¹⁾	4.096 V
REF7050QFKHT ⁽¹⁾	REF7050QDGKR ²	5.0 V

- (1) This orderable is released to market.
 (2) Samples available for the orderable upon request.

6 Pin Configuration and Functions

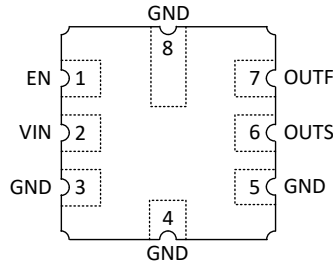


図 6-1. FKH Package
8-Pin LCCC
Top View

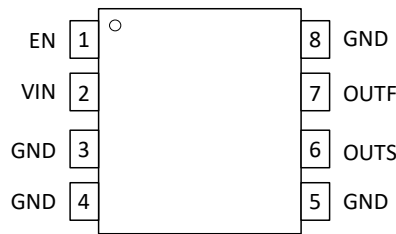


図 6-2. DGK Package
8-Pin VSSOP
Top View

表 6-1. Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	FKH	DGK		
EN	1	1	Input	Device enable control. Low level input disables the reference output and device enters shutdown mode. Device can be enabled by driving voltage > 1.6V. If the pin is left floating, the internal pull up will enable the device.
VIN	2	2	Power	Input supply voltage connection. Connect a minimum 0.1- μ F decoupling capacitor to ground for the best performance.
GND	3	3	Ground	Ground connection.
GND	4	4	Ground	Ground connection.
GND	5	5	Ground	Ground connection
OUTS	6	6	Input	Reference voltage output sense connection.
OUTF	7	7	Output	Reference voltage output force connection. Connect a output capacitor between 1- μ F to 100- μ F for the best performance.
GND	8	8	Ground	Ground connection.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	V _{IN}	-0.3	20	V
Enable voltage	EN	-0.3	V _{IN} + 0.3	V
Output voltage	V _{OUT}	-0.3	6	V
Output short circuit current	I _{SC}		25	mA
Operating temperature range	T _A	-55	150	°C
Storage temperature range	T _{stg}	-65	170	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	V _{OUT} + V _{DO} ⁽¹⁾		18	V
EN	Enable voltage	0		V _{IN}	V
I _L	Output current	-10		10	mA
T _A	Operating temperature	-40	25	125	°C

- (1) V_{DO} = Dropout voltage. For V_{OUT} < 2.5 V minimum V_{IN} = 2.75 V

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF70xx		UNIT
		FKH (CERAMIC)	DGK (MSOP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	95.8	201.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	59.0	85.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	58.3	122.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	48.2	21.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	58.1	121.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	28.5	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 REF7012 Electrical Characteristics

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = 3\text{ V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	$T_A = 25^\circ\text{C}$	-0.025		0.025	%
	Output voltage accuracy	$T_A = 25^\circ\text{C}$; DGK package	-0.05		0.05	%
	Output voltage temperature coefficient	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			2	ppm/ $^\circ\text{C}$
	Output voltage temperature coefficient	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$; DGK package			2	ppm/ $^\circ\text{C}$
	Output voltage temperature coefficient	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$; DGK package			4.2	ppm/ $^\circ\text{C}$
LINE AND LOAD REGULATION						
$\Delta V_O / \Delta V_{IN}$	Line regulation	$2.75\text{ V} \leq V_{IN} \leq 18\text{ V}$		4		ppm/V
		$2.75\text{ V} \leq V_{IN} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			30	
$\Delta V_O / \Delta I_L$	Load regulation	$I_L = 0\text{ mA to }10\text{ mA}$		5		ppm/mA
		$I_L = 0\text{ mA to }10\text{ mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			15	
		$I_L = 0\text{ mA to }-10\text{ mA}$		15		
		$I_L = 0\text{ mA to }-10\text{ mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			30	
NOISE						
e_{np-p}	Low frequency noise	$f = 0.1\text{ Hz to }10\text{ Hz}$		0.25		ppm _{p-p}
e_n	Output voltage noise	$f = 10\text{ Hz to }1\text{ kHz}$		0.35		ppm _{rms}
HYSTERESIS AND LONG-TERM STABILITY						
	Long-term stability	0 to 250h at 35°C – FKH package		15		ppm
		0 to 1000h at 35°C – FKH package		35		
	Long-term stability	0 to 250h at 35°C – DGK package		27		ppm
		0 to 1000h at 35°C – DGK package		37		
	Output voltage hysteresis (cycle 1)	25°C , -40°C , 125°C , 25°C – FKH package		18		ppm
		25°C , -40°C , 85°C , 25°C – FKH package		11		
		25°C , 0°C , 70°C , 25°C – FKH package		11		
	Output voltage hysteresis (cycle 1)	25°C , -40°C , 125°C , 25°C – DGK package		410		ppm
		25°C , -40°C , 85°C , 25°C – DGK package		35		
		25°C , 0°C , 70°C , 25°C – DGK package		33		
TURN ON TIME						
t_{ON}	Turn-on time	0.1% settling, $C_{OUT} = 1\ \mu\text{F}$		0.5		ms
CAPACITIVE LOAD						
C_{IN}	Stable input capacitor range	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.1		μF
C_{OUT}	Stable output capacitor range ⁽¹⁾	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		1	100	μF
POWER SUPPLY						
V_{IN}	Input voltage		2.75		18	V
I_Q	Quiescent current	$T_A = 25^\circ\text{C}$	Active mode	4	6.5	mA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			7.5	mA
		$T_A = 25^\circ\text{C}$	Shutdown mode	5	10	μA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			12	μA

7.5 REF7012 Electrical Characteristics (続き)

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = 3\text{ V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{EN}	Enable pin voltage	Active mode (EN=1)	1.6		V
		Shutdown mode (EN=0)		0.5	V
I_{EN}	Enable pin current	$V_{IN} = V_{EN} = 18\text{V}$	3.2	4	μA
		$V_{IN} = V_{EN} = 18\text{V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		5	μA
I_{SC}	Short circuit current	$V_{OUT} = 0\text{V}$	30		mA

(1) ESR for the capacitor can range from 1 m Ω to 400 m Ω

7.6 REF7025 Electrical Characteristics

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT					
	Output voltage accuracy	$T_A = 25^\circ\text{C}$	-0.025	0.025	%
	Output voltage temperature coefficient	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		2	ppm/ $^\circ\text{C}$
LINE AND LOAD REGULATION					
$\Delta V_O / \Delta V_{IN}$	Line regulation	$V_{OUT} + V_{DO} \leq V_{IN} \leq 18\text{ V}$		4	ppm/V
		$V_{OUT} + V_{DO} \leq V_{IN} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		30	
$\Delta V_O / \Delta I_L$	Load regulation	$I_L = 0\text{ mA to }10\text{ mA}$, $V_{IN} = V_{OUT} + V_{DO}$		5	ppm/mA
		$I_L = 0\text{ mA to }10\text{ mA}$, $V_{IN} = V_{OUT} + V_{DO}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		10	
		$I_L = 0\text{ mA to }-10\text{ mA}$, $V_{IN} = V_{OUT} + V_{DO}$		5	
		$I_L = 0\text{ mA to }-10\text{ mA}$, $V_{IN} = V_{OUT} + V_{DO}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		15	
NOISE					
e_{np-p}	Low frequency noise	$f = 0.1\text{ Hz to }10\text{ Hz}$		0.23	ppm _{p-p}
e_n	Output voltage noise	$f = 10\text{ Hz to }1\text{ kHz}$		0.35	ppm _{rms}
HYSTERESIS AND LONG-TERM STABILITY					
	Long-term stability	0 to 250h at 35°C - FKH package		15	ppm
		0 to 1000h at 35°C - FKH package		35	
	Long-term stability	0 to 250h at 35°C - DGK package		35	ppm
		0 to 1000h at 35°C - DGK package		75	ppm
	Output voltage hysteresis (cycle 1)	25°C , -40°C , 125°C , 25°C - FKH package		180	ppm
		25°C , -40°C , 85°C , 25°C - FKH package		100	
		25°C , 0°C , 70°C , 25°C - FKH package		40	
	Output voltage hysteresis (cycle 1)	25°C , -40°C , 125°C , 25°C - DGK package		290	ppm
		25°C , -40°C , 85°C , 25°C - DGK package		50	
		25°C , 0°C , 70°C , 25°C - DGK package		45	
TURN ON TIME					
t_{ON}	Turn-on time	0.1% settling, $C_{OUT} = 1\ \mu\text{F}$		0.5	ms
CAPACITIVE LOAD					
C_{IN}	Stable input capacitor range	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.1	μF

7.6 REF7025 Electrical Characteristics (続き)

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
C_{OUT}	Stable output capacitor range (1)	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		1		100	μF
POWER SUPPLY							
V_{IN}	Input voltage			$V_{OUT} + V_{DO}$		18	V
I_Q	Quiescent current	$T_A = 25^\circ\text{C}$	Active mode		4	6	mA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				6.5	mA
		$T_A = 25^\circ\text{C}$	Shutdown mode		5	10	μA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				12	μA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	$V_{IN} = V_{EN} = 18\text{V}$			3.2	4	μA
		$V_{IN} = V_{EN} = 18\text{V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				5	μA
V_{DO}	Dropout voltage	$I_L = 5\text{mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				250	mV
		$I_L = 10\text{mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				400	mV
I_{SC}	Short circuit current	$V_{OUT} = 0\text{V}$			25		mA

(1) ESR for the capacitor can range from 1 m Ω to 400 m Ω

7.7 REF7030 Electrical Characteristics

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	$T_A = 25^\circ\text{C}$		-0.025		0.025	%
	Output voltage temperature coefficient	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				2	ppm/ $^\circ\text{C}$
LINE AND LOAD REGULATION							
$\Delta V_O / \Delta V_{IN}$	Line regulation	$3.2\text{ V} \leq V_{IN} \leq 18\text{ V}$			4		ppm/V
		$3.2\text{ V} \leq V_{IN} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				30	
$\Delta V_O / \Delta I_L$	Load regulation	$I_L = 0\text{ mA to } 10\text{ mA}$, $V_{IN} = 3.5\text{ V}$			5		ppm/mA
		$I_L = 0\text{ mA to } 10\text{ mA}$, $V_{IN} = 3.5\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				10	
		$I_L = 0\text{ mA to } -10\text{ mA}$, $V_{IN} = 3.5\text{ V}$			5		
		$I_L = 0\text{ mA to } -10\text{ mA}$, $V_{IN} = 3.5\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				15	
NOISE							
e_{np-p}	Low frequency noise	$f = 0.1\text{ Hz to } 10\text{ Hz}$			0.23		ppm _{p-p}
e_n	Output voltage noise	$f = 10\text{ Hz to } 1\text{ kHz}$			0.35		ppm _{rms}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 250h at 35°C - FKH package			15		ppm
		0 to 1000h at 35°C - FKH package				35	
	Output voltage hysteresis (cycle 1)	25°C , -40°C , 125°C , 25°C – FKH package			180		ppm
		25°C , -40°C , 85°C , 25°C – FKH package				100	
		25°C , 0°C , 70°C , 25°C – FKH package				40	

7.7 REF7030 Electrical Characteristics (続き)

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, $C_{OUT} = 1\ \mu\text{F}$			0.5		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.1			μF
C_{OUT}	Stable output capacitor range (1)	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		1		100	μF
POWER SUPPLY							
V_{IN}	Input voltage			$V_{OUT} + V_{DO}$		18	V
I_Q	Quiescent current	$T_A = 25^\circ\text{C}$	Active mode		4	6	mA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				7	mA
		$T_A = 25^\circ\text{C}$	Shutdown mode		5	10	μA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				12	μA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	$V_{IN} = V_{EN} = 18\text{V}$			3.2	4	μA
		$V_{IN} = V_{EN} = 18\text{V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				5	μA
V_{DO}	Dropout voltage	$I_L = 5\text{mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				250	mV
		$I_L = 10\text{mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				400	mV
I_{SC}	Short circuit current	$V_{OUT} = 0\text{V}$			25		mA

(1) ESR for the capacitor can range from 1 m Ω to 400 m Ω

7.8 REF7033 Electrical Characteristics

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	$T_A = 25^\circ\text{C}$		-0.025		0.025	%
	Output voltage temperature coefficient	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				2	ppm/ $^\circ\text{C}$
LINE AND LOAD REGULATION							
$\Delta V_O / \Delta V_{IN}$	Line regulation	$3.5\text{ V} \leq V_{IN} \leq 18\text{ V}$			4		ppm/V
		$3.5\text{ V} \leq V_{IN} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				30	
$\Delta V_O / \Delta I_L$	Load regulation	$I_L = 0\text{ mA to } 10\text{mA}$, $V_{IN} = 3.8\text{ V}$			5		ppm/mA
		$I_L = 0\text{ mA to } 10\text{mA}$, $V_{IN} = 3.8\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				10	
		$I_L = 0\text{ mA to } -10\text{mA}$, $V_{IN} = 3.8\text{ V}$			5		
		$I_L = 0\text{ mA to } -10\text{mA}$, $V_{IN} = 3.8\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				15	
NOISE							
e_{np-p}	Low frequency noise	$f = 0.1\text{ Hz to } 10\text{ Hz}$			0.23		ppm _{p-p}
e_n	Output voltage noise	$f = 10\text{ Hz to } 1\text{ kHz}$			0.35		ppm _{rms}
HYSTERESIS AND LONG-TERM STABILITY							

7.8 REF7033 Electrical Characteristics (続き)

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
	Long-term stability	0 to 250h at 35°C - FKH package			15		ppm
		0 to 1000h at 35°C - FKH package			35		
	Output voltage hysteresis (cycle 1)	25°C , -40°C , 125°C , 25°C – FKH package			180		ppm
		25°C , -40°C , 85°C , 25°C – FKH package			100		
		25°C , 0°C , 70°C , 25°C – FKH package			40		
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, $C_{OUT} = 1\ \mu\text{F}$			0.5		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.1			μF
C_{OUT}	Stable output capacitor range (1)	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		1		100	μF
POWER SUPPLY							
V_{IN}	Input voltage			$V_{OUT} + V_{DO}$		18	V
I_Q	Quiescent current	$T_A = 25^\circ\text{C}$	Active mode		4	6	mA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				7	mA
		$T_A = 25^\circ\text{C}$	Shutdown mode		5	10	μA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				12	μA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	$V_{IN} = V_{EN} = 18\text{V}$			3.2	4	μA
		$V_{IN} = V_{EN} = 18\text{V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				5	μA
V_{DO}	Dropout voltage	$I_L = 5\text{mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				250	mV
		$I_L = 10\text{mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				400	mV
I_{SC}	Short circuit current	$V_{OUT} = 0\text{V}$			25		mA

(1) ESR for the capacitor can range from 1 m Ω to 400 m Ω

7.9 REF7040 Electrical Characteristics

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	$T_A = 25^\circ\text{C}$		-0.025		0.025	%
	Output voltage temperature coefficient	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				2	ppm/ $^\circ\text{C}$
LINE AND LOAD REGULATION							
$\Delta V_O / \Delta V_{IN}$	Line regulation	$V_{OUT} + V_{DO} \leq V_{IN} \leq 18\text{V}$			4		ppm/V
		$V_{OUT} + V_{DO} \leq V_{IN} \leq 18\text{V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				30	

7.9 REF7040 Electrical Characteristics (続き)

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
$\Delta V_O / \Delta I_L$	Load regulation	$I_L = 0\text{ mA to }10\text{ mA}$, $V_{IN} = V_{OUT} + V_{DO}$			5		ppm/mA
		$I_L = 0\text{ mA to }10\text{ mA}$, $V_{IN} = V_{OUT} + V_{DO}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				10	
		$I_L = 0\text{ mA to }-10\text{ mA}$, $V_{IN} = V_{OUT} + V_{DO}$			5		
		$I_L = 0\text{ mA to }-10\text{ mA}$, $V_{IN} = V_{OUT} + V_{DO}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				15	
NOISE							
e_{np-p}	Low frequency noise	$f = 0.1\text{ Hz to }10\text{ Hz}$			0.23		ppm _{p-p}
e_n	Output voltage noise	$f = 10\text{ Hz to }1\text{ kHz}$			0.35		ppm _{rms}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 250h at 35°C - FKH package			15		ppm
		0 to 1000h at 35°C - FKH package			35		
	Long-term stability	0 to 250h at 35°C - DGK package			35		ppm
		0 to 1000h at 35°C - DGK package			75		
	Output voltage hysteresis (cycle 1)	25°C , -40°C , 125°C , 25°C - FKH package			180		ppm
		25°C , -40°C , 85°C , 25°C - FKH package			100		
		25°C , 0°C , 70°C , 25°C - FKH package			40		
	Output voltage hysteresis (cycle 1)	25°C , -40°C , 125°C , 25°C (cycle 1) - DGK package			290		ppm
		25°C , -40°C , 85°C , 25°C (cycle 1) - DGK package			50		
		25°C , 0°C , 70°C , 25°C (cycle 1) - DGK package			45		
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, $C_{OUT} = 1\ \mu\text{F}$			0.5		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			0.1		μF
C_{OUT}	Stable output capacitor range (1)	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			1	100	μF
POWER SUPPLY							
V_{IN}	Input voltage			$V_{OUT} + V_{DO}$		18	V
I_Q	Quiescent current	$T_A = 25^\circ\text{C}$		Active mode	4	6	mA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				6.5	mA
		$T_A = 25^\circ\text{C}$		Shutdown mode	5	10	μA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				12	μA
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	$V_{IN} = V_{EN} = 18\text{V}$		3.2		4	μA
		$V_{IN} = V_{EN} = 18\text{V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				5	μA
V_{DO}	Dropout voltage	$I_L = 5\text{ mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				250	mV
		$I_L = 10\text{ mA}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				400	mV
I_{SC}	Short circuit current	$V_{OUT} = 0\text{V}$				25	mA

(1) ESR for the capacitor can range from 1 m Ω to 400 m Ω

7.10 REF7050 Electrical Characteristics

Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	$T_A = 25^\circ\text{C}$		-0.025		0.025	%
	Output voltage temperature coefficient	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				2	ppm/ $^\circ\text{C}$
LINE AND LOAD REGULATION							
$\Delta V_O / \Delta V_{IN}$	Line regulation	$V_{OUT} + V_{DO} \leq V_{IN} \leq 18\text{ V}$			4		ppm/V
		$V_{OUT} + V_{DO} \leq V_{IN} \leq 18\text{ V}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				30	
$\Delta V_O / \Delta I_L$	Load regulation	$I_L = 0\text{ mA to } 10\text{ mA}, V_{IN} = V_{OUT} + V_{DO}$			5		ppm/mA
		$I_L = 0\text{ mA to } 10\text{ mA}, V_{IN} = V_{OUT} + V_{DO}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				10	
		$I_L = 0\text{ mA to } -10\text{ mA}, V_{IN} = V_{OUT} + V_{DO}$			5		
		$I_L = 0\text{ mA to } -10\text{ mA}, V_{IN} = V_{OUT} + V_{DO}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				15	
NOISE							
e_{np-p}	Low frequency noise	$f = 0.1\text{ Hz to } 10\text{ Hz}$			0.23		ppm _{p-p}
e_n	Output voltage noise	$f = 10\text{ Hz to } 1\text{ kHz}$			0.35		ppm _{rms}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 250h at 35°C - FKH package			15		ppm
		0 to 1000h at 35°C - FKH package				35	
	Output voltage hysteresis (cycle 1)	$25^\circ\text{C}, -40^\circ\text{C}, 125^\circ\text{C}, 25^\circ\text{C}$ – FKH package			180		ppm
		$25^\circ\text{C}, -40^\circ\text{C}, 85^\circ\text{C}, 25^\circ\text{C}$ – FKH package				100	
		$25^\circ\text{C}, 0^\circ\text{C}, 70^\circ\text{C}, 25^\circ\text{C}$ – FKH package				40	
TURN ON TIME							
t_{ON}	Turn-on time	0.1% settling, $C_{OUT} = 1\ \mu\text{F}$			0.5		ms
CAPACITIVE LOAD							
C_{IN}	Stable input capacitor range	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.1			μF
C_{OUT}	Stable output capacitor range (1)	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		1		100	μF
POWER SUPPLY							
V_{IN}	Input voltage			$V_{OUT} + V_{DO}$		18	V
I_Q	Quiescent current	$T_A = 25^\circ\text{C}$	Active mode		4	6	mA
				$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			6.5
		$T_A = 25^\circ\text{C}$	Shutdown mode		5	10	μA
				$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			12
V_{EN}	Enable pin voltage	Active mode (EN=1)		1.6			V
		Shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	$V_{IN} = V_{EN} = 18\text{V}$			3.2	4	μA
		$V_{IN} = V_{EN} = 18\text{V}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				5	μA
V_{DO}	Dropout voltage	$I_L = 5\text{ mA}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				250	mV
		$I_L = 10\text{ mA}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				400	mV

7.10 REF7050 Electrical Characteristics (続き)

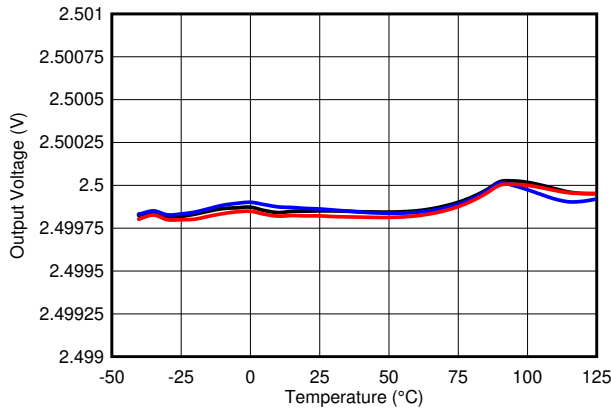
Specifications are tested at $T_A = 25^\circ\text{C}$, $I_L = 0\text{ mA}$, $C_{IN} = 0.1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{IN} = V_{OUT} + 0.5\text{V}$, OUTS connected to OUTF, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{sc}	Short circuit current	$V_{OUT} = 0\text{V}$		25		mA

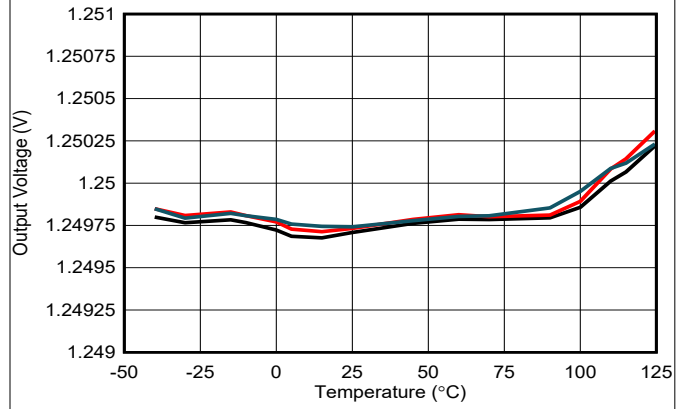
(1) ESR for the capacitor can range from 1 m Ω to 400 m Ω

7.11 Typical Characteristics

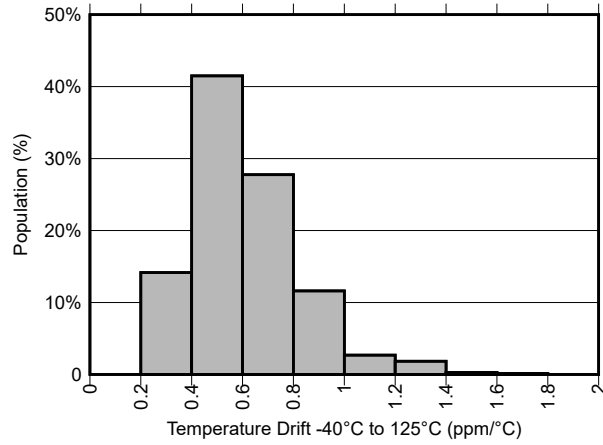
at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{REF} + 0.5\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\text{ }\mu\text{F}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $V_{REF} = 2.5\text{ V}$ (unless otherwise noted)



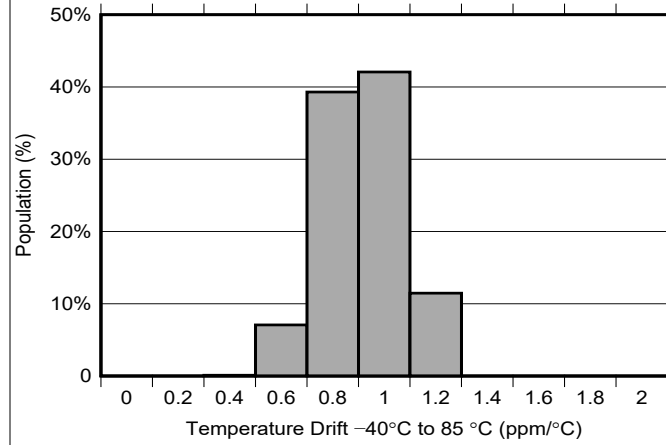
7-1. Output Voltage Vs Free-Air Temperature (REF7025QFKHR)



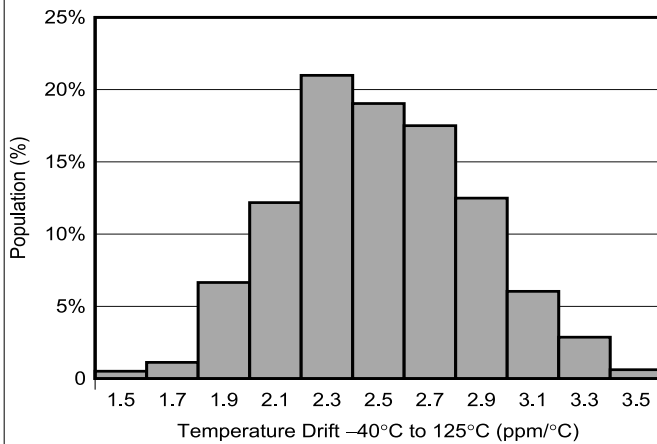
7-2. Output Voltage Vs Free-Air Temperature (REF7012QDGKR)



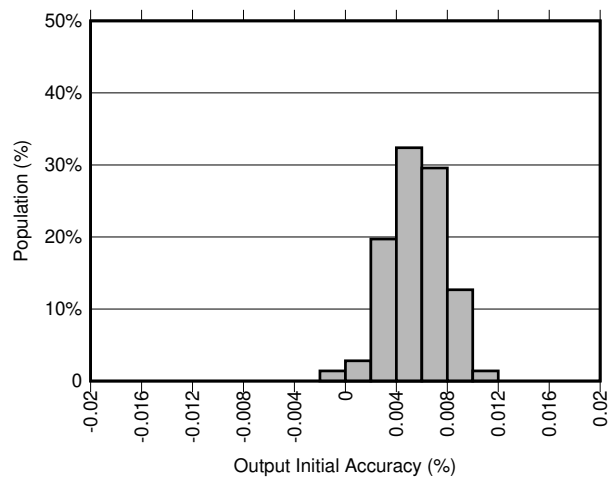
7-3. Temperature Drift Distribution (REF7025QFKHR)



7-4. Temperature Drift Distribution (REF7012QDGKR)



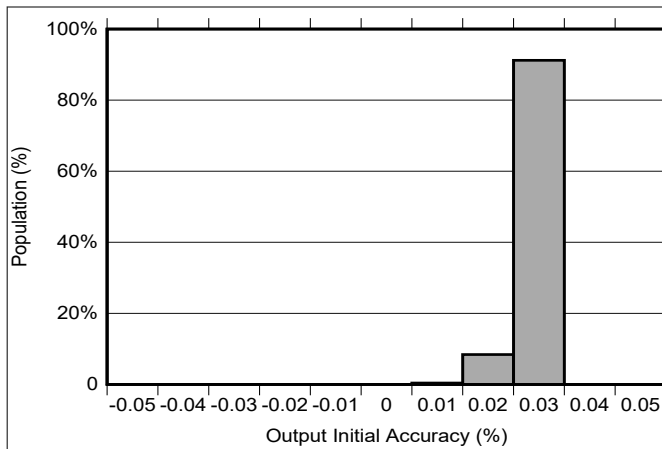
7-5. Temperature Drift Distribution (REF7012QDGKR)



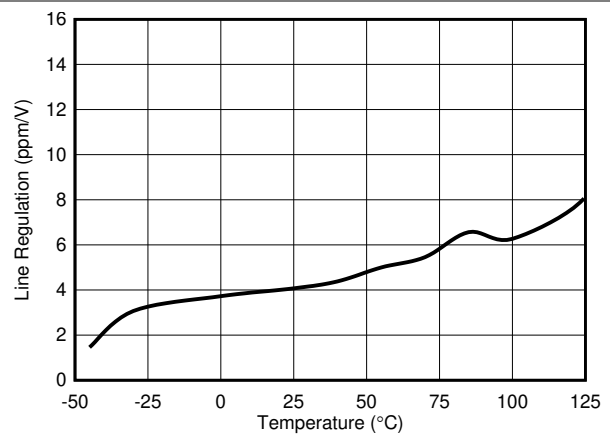
7-6. Accuracy Distribution (REF7025QFKHR)

7.11 Typical Characteristics (continued)

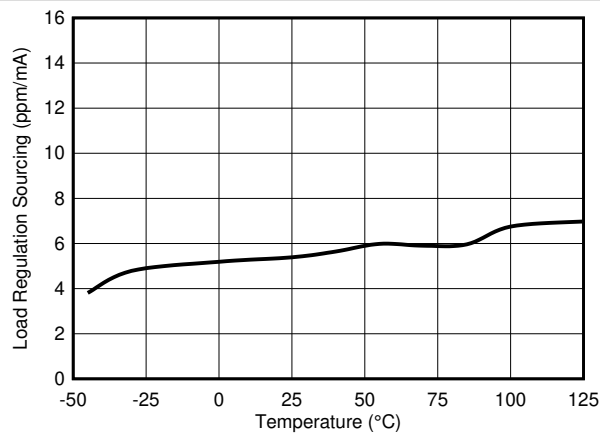
at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{REF} + 0.5\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\ \mu\text{F}$, $C_{IN} = 0.1\ \mu\text{F}$, $V_{REF} = 2.5\text{ V}$ (unless otherwise noted)



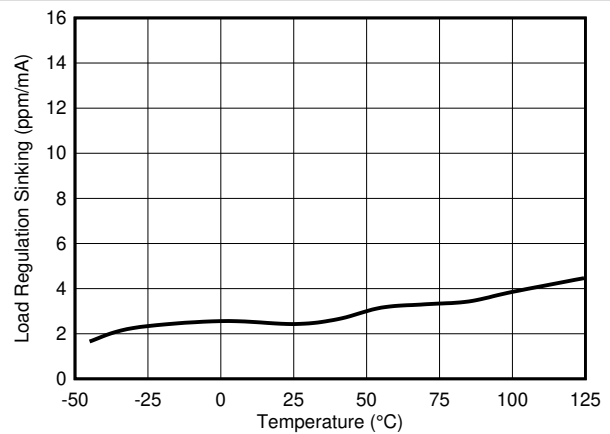
7-7. Accuracy Distribution (REF7012QDGKR)



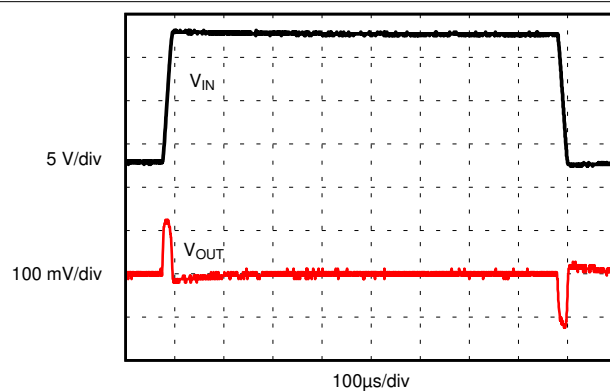
7-8. Line Regulation vs Temperature



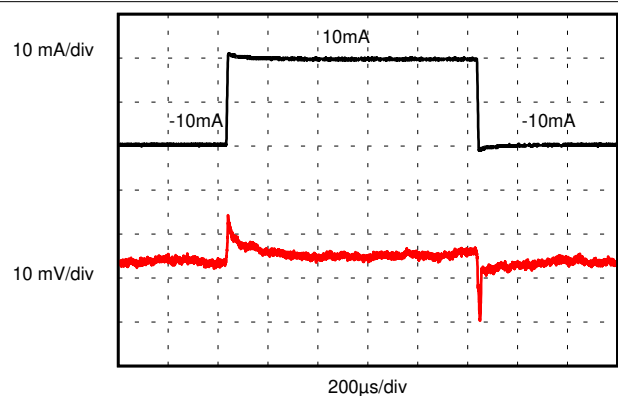
7-9. Load Regulation (Sourcing) vs Temperature



7-10. Load Regulation (Sinking) vs Temperature



7-11. Line Regulation Response



7-12. Load Transient Response ($C_L = 1\ \mu\text{F}$)

7.11 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{REF} + 0.5\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\ \mu\text{F}$, $C_{IN} = 0.1\ \mu\text{F}$, $V_{REF} = 2.5\text{ V}$ (unless otherwise noted)

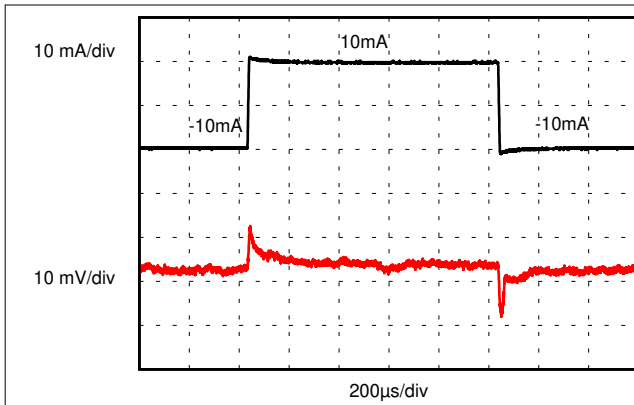


Figure 7-13. Load Transient Response ($C_L = 10\ \mu\text{F}$)

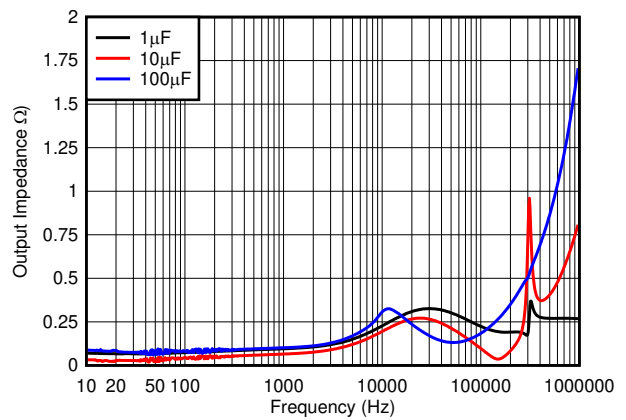


Figure 7-14. Output Impedance

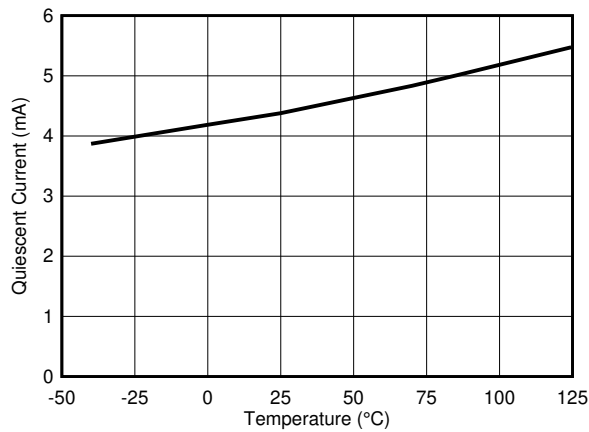


Figure 7-15. Quiescent Current vs Temperature

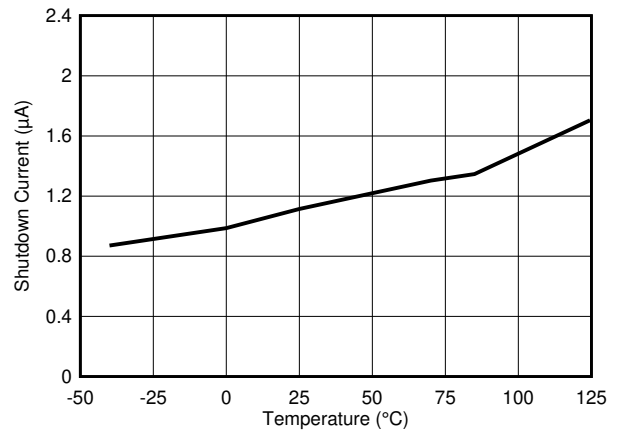


Figure 7-16. Shutdown Current vs Temperature

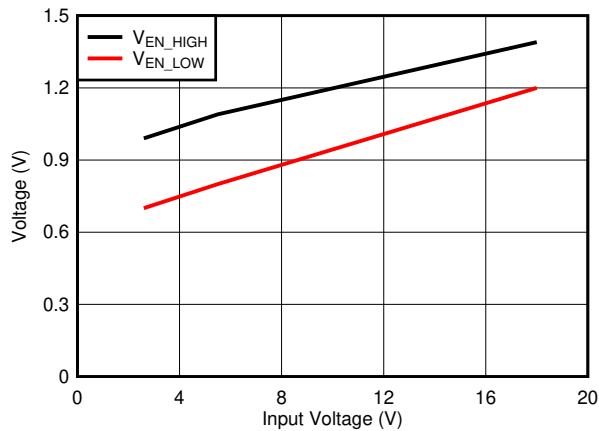


Figure 7-17. Enable Threshold vs V_{IN}

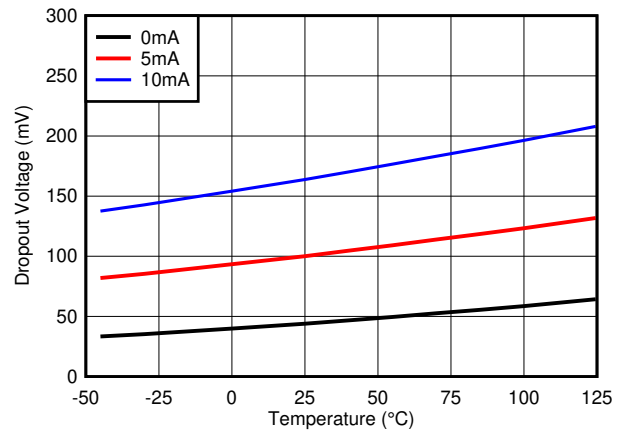
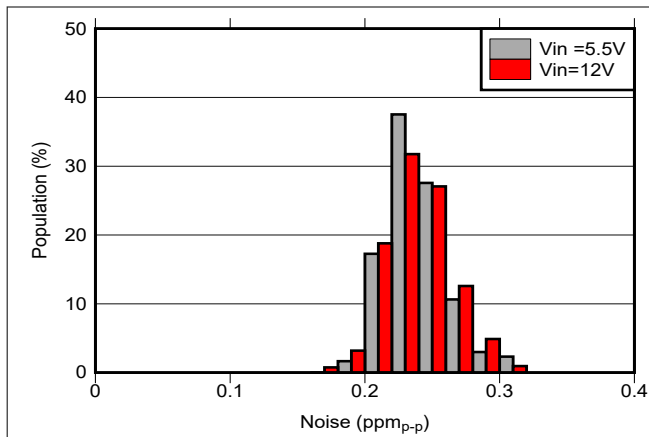


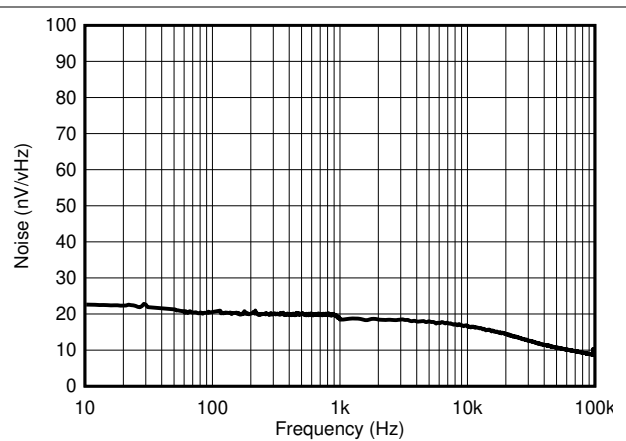
Figure 7-18. Dropout Voltage vs Temperature

7.11 Typical Characteristics (continued)

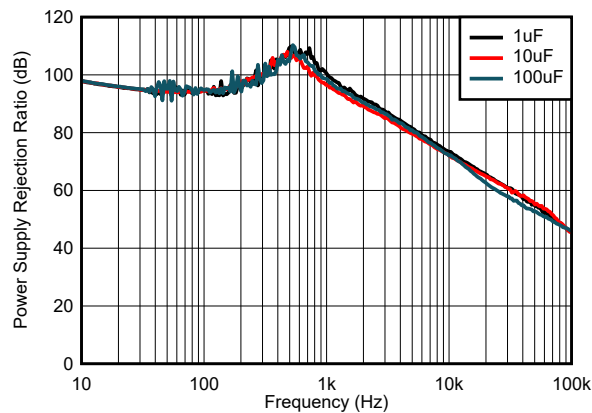
at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{REF} + 0.5\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\text{ }\mu\text{F}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $V_{REF} = 2.5\text{ V}$ (unless otherwise noted)



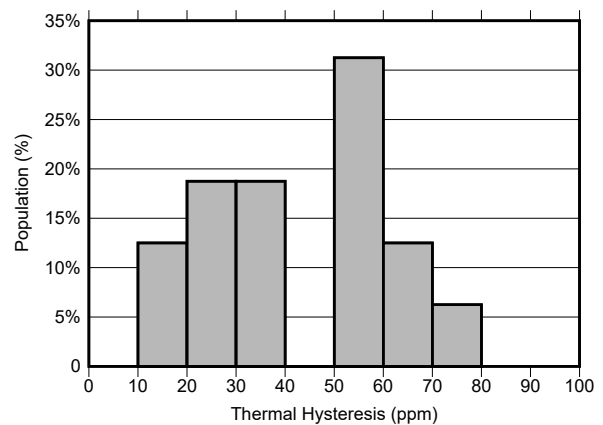
7-19. 0.1-Hz to 10-Hz Voltage Noise Distribution (300 units)



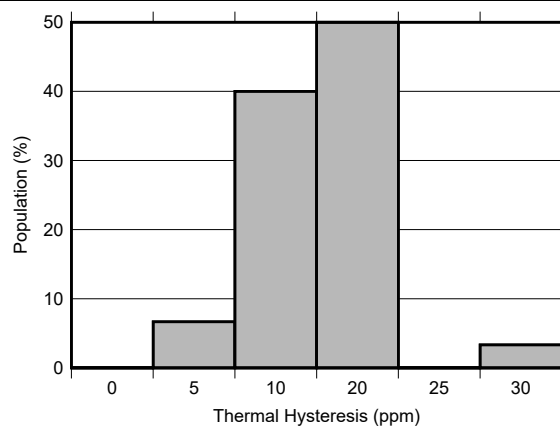
7-20. Noise Performance 10 Hz to 100 kHz



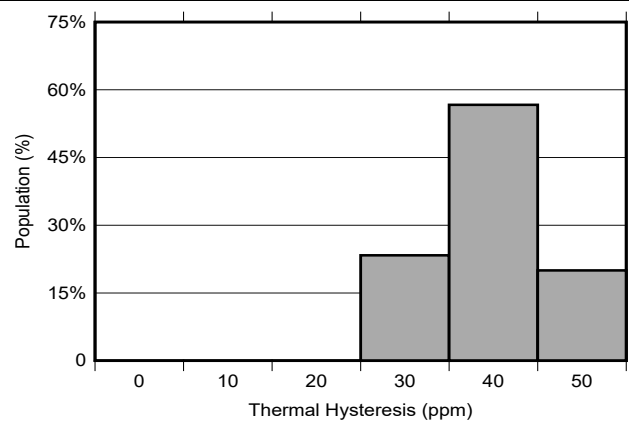
7-21. Power-Supply Rejection Ratio vs Frequency



7-22. REF7025QFKHR Thermal Hysteresis Distribution (0°C to 70°C)



7-23. REF7012QFKHR Thermal Hysteresis Distribution (0°C to 70°C)



7-24. REF7012QDGKR Thermal Hysteresis Distribution (0°C to 70°C)

7.11 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{REF} + 0.5\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\text{ }\mu\text{F}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $V_{REF} = 2.5\text{ V}$ (unless otherwise noted)

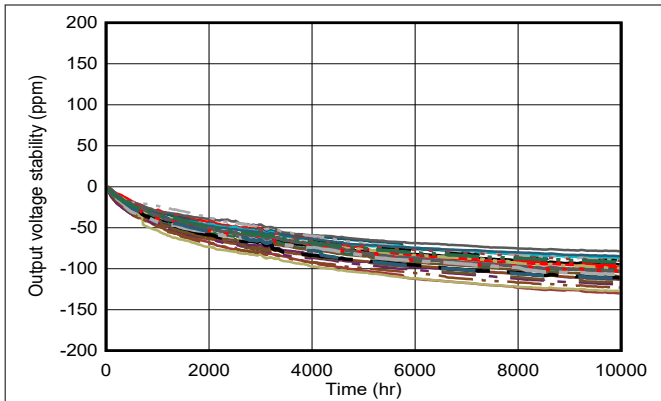


图 7-25. Long-Term Stability LCCC package (First 10000 Hours)

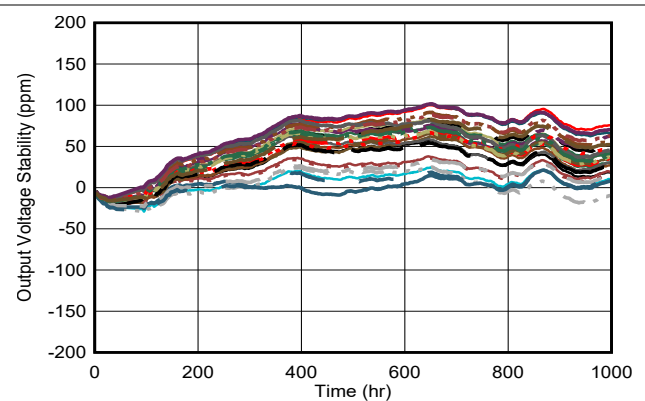


图 7-26. Long-Term Stability VSSOP package REF7012 (First 1000 Hours)

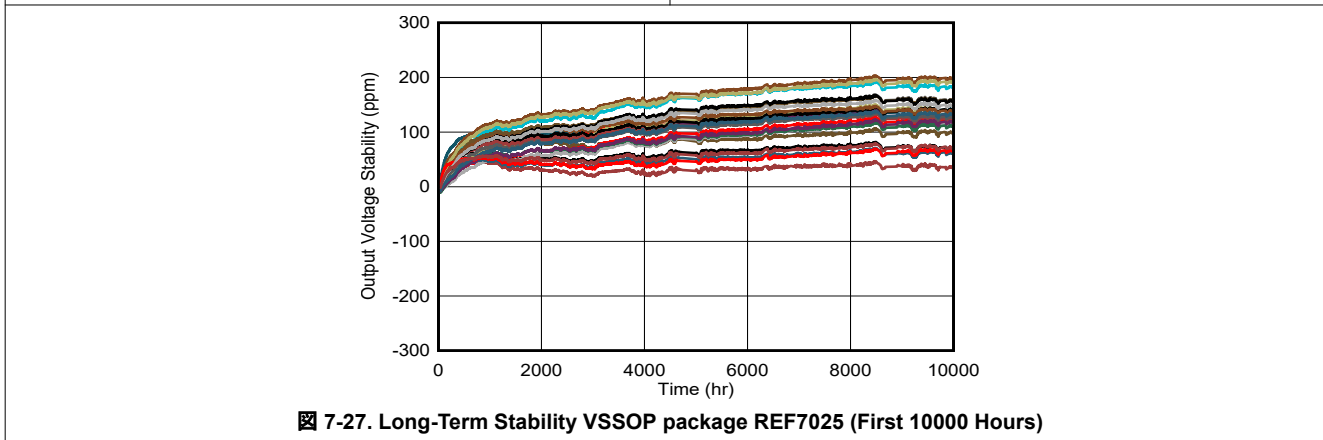


图 7-27. Long-Term Stability VSSOP package REF7025 (First 10000 Hours)

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF70 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated during soldering process. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error. In order to illustrate this effect, a total of 32 devices were soldered on two printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in [Figure 8-1](#). The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm.

For recommended reflow profiles using 'Sn-Pb Eutectic Assembly' or 'Pb-Free Assembly' please refer JEDEC J-STD-020 standard.

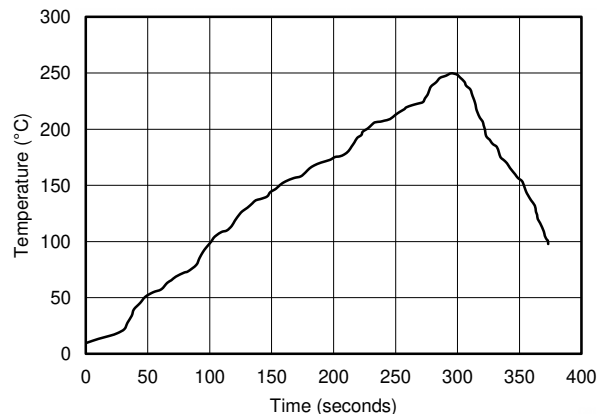


Figure 8-1. Reflow Profile

The reference output voltage is measured before and after the reflow process. Although all tested units exhibit very low shifts, higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the [Figure 8-2](#) and [Figure 8-3](#) display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize its exposure to thermal stress.

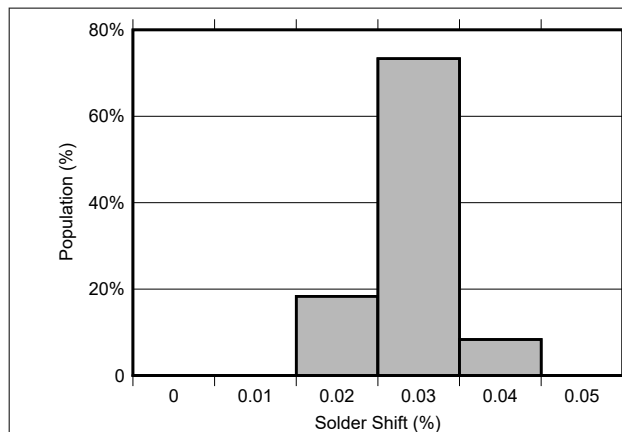


Figure 8-2. Solder Shift (LCCC Package)

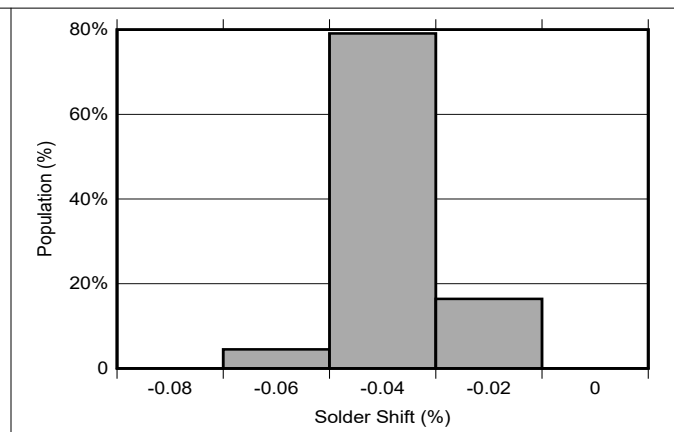



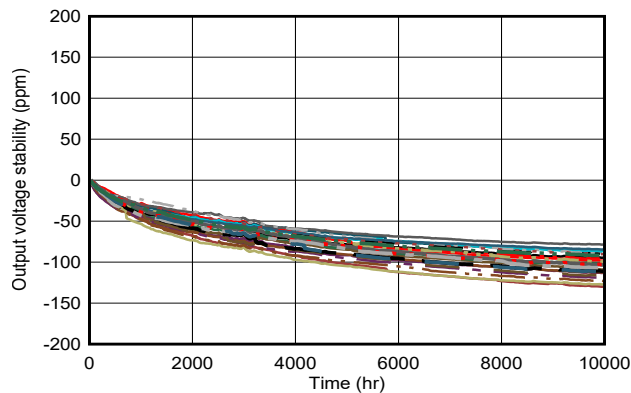
Figure 8-3. Solder Shift (VSSOP Package)

8.2 Long-Term Stability


One of the key parameters of the REF70 references is long-term stability also known as long-term drift. The long-term stability value was tested in a typical setup that reflects standard PCB board manufacturing practices. The boards are made of standard FR4 material and the board does not have special cuts or grooves around the devices to relieve the mechanical stress of the PCB. The devices and boards in this test do not undergo high temperature burn in post-soldering prior to testing. These conditions reflect a real world use case scenario and common manufacturing techniques.

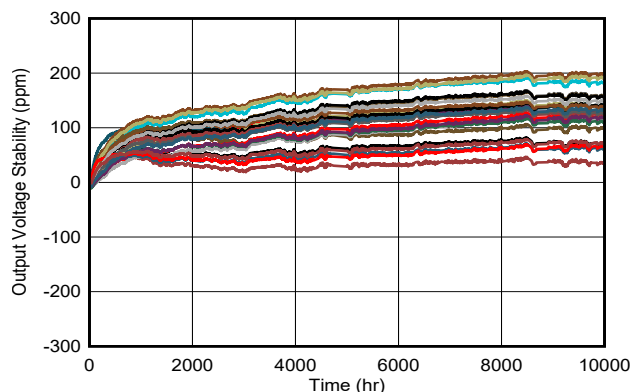
During the long-term stability testing, precautions are taken to ensure that only the long-term stability drift is being measured. The boards are maintained at 35°C in an oil bath. The oil bath ensures that the temperature is constant across the device over time compared to an air oven. The measurements are captured every 30 minutes with a calibrated 8.5 digit multimeter.

Typical long-term stability characteristic is expressed as a deviation over time.  8-4 shows the typical drift value for the REF70 in LCCC (FKH) package is 35 ppm from 0 to 1000 hours. It is important to understand that long-term stability is not ensured by design and that the value is typical. The REF70 will experience the highest drift in the initial 1000 hr. Subsequent deviation is typically lower than previous 1000 hr.



 8-4. Long Term Stability LCCC -10000 hours (V_{OUT})

 8-5 shows the typical drift value for the REF70 in VSSOP (DGK) package is 75 ppm from 0 to 1000 hours. It is important to understand that long-term stability is not ensured by design and that the value is typical. The REF70 will experience the highest drift in the initial 1000 hr.



 8-5. Long Term Stability VSSOP -10000 hours (V_{OUT})

8.3 Thermal Hysteresis

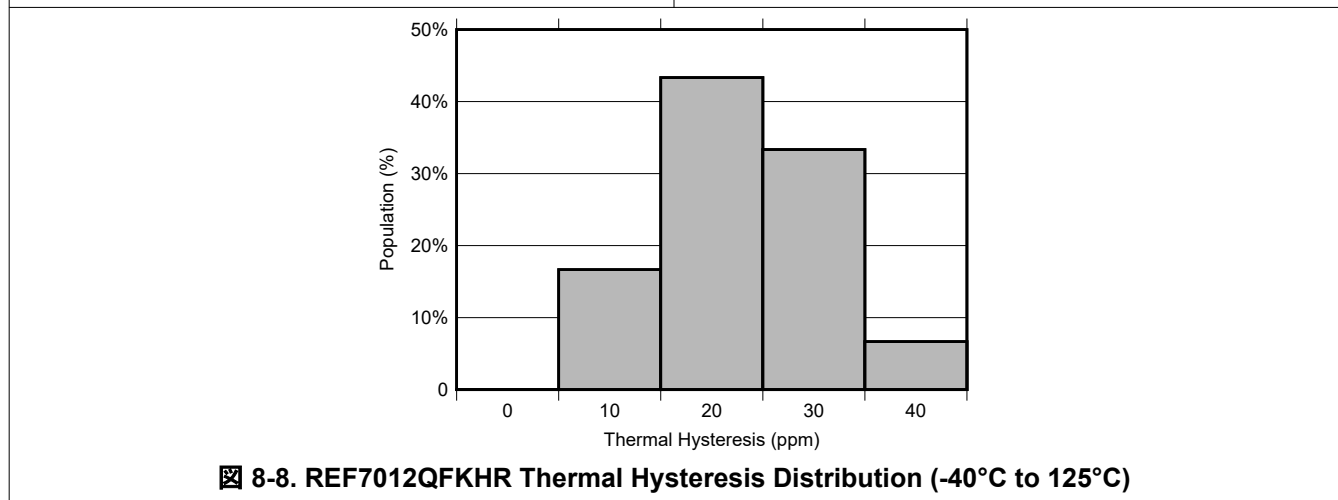
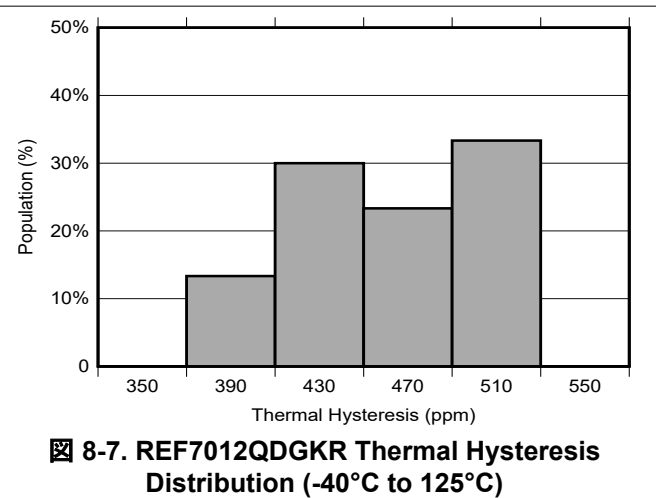
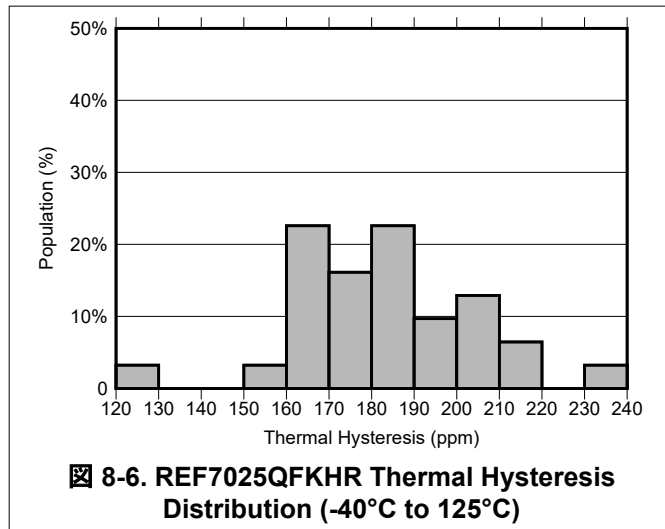
Thermal hysteresis is measured with the REF70 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling

the device through the specified temperature range, and returning to 25°C. This can be seen in [Figure 8-6](#) to [Figure 8-8](#). Hysteresis can be expressed by [Equation 1](#):

$$V_{\text{HYST}} = \left(\frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \times 10^6 \text{ (ppm)} \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of -40°C to +125°C and returns to 25°C.

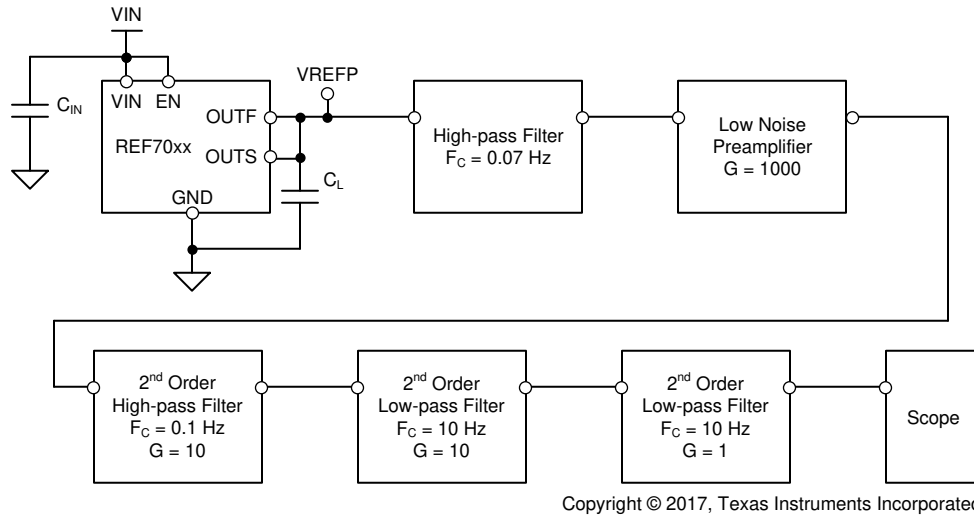


8.4 Noise Performance

8.4.1 1/f Noise

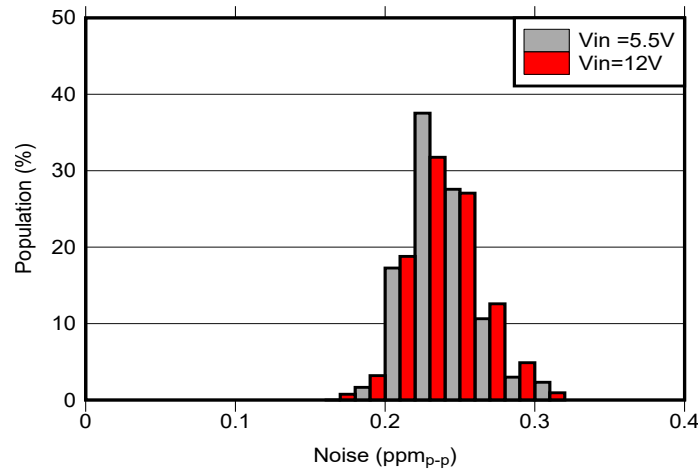
1/f noise, also known as flicker noise, is a low frequency noise that affects the device output voltage which can affect precision measurements in ADCs. This noise increases proportionally with output voltage and operating temperature. It is measured by filtering the output from 0.1-Hz to 10-Hz. Since the 1/f noise is an extremely low

value, the frequency of interest needs to be amplified and band-pass filtered. This is done by using a high-pass filter to block the DC voltage. The resulting noise is then amplified by a gain of 1000. The bandpass filter is created by a series of high-pass and low-pass filter that adds additional gain to make it more visible on a oscilloscope as shown in [8-9](#). 1/f noise must be tested in a Faraday cage enclosure to block environmental noise.



8-9. 1/f Noise Test Setup

Typical 1/f noise (0.1-Hz to 10-Hz) distribution can be seen in [8-10](#). The noise is measured at two different supply voltages. The REF70 noise performance is not impacted by supply voltage.



8-10. 0.1-Hz to 10-Hz Voltage Noise Distribution

The 1/f noise is in such a low frequency range that it is not practical to filter out which makes it a key parameter for ultra-low noise measurements. Noise sensitive designs must use the lowest 1/f noise for the highest precision measurements. [8-11](#) shows the effect of 1/f noise over 10s.

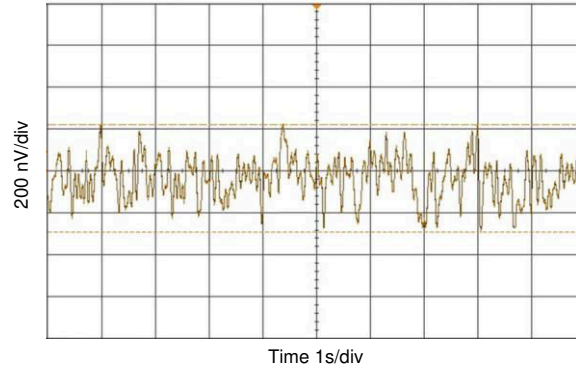


図 8-11. 0.1-Hz to 10-Hz Voltage Noise

8.4.2 Broadband Noise

Broadband noise is a noise that appears at higher frequency compared to $1/f$ noise. The broadband noise is usually flat and uniform over frequency as shown in 図 8-13. The broadband noise is measured by high-pass filtering the output of the REF70 and measuring the result on a spectrum analyzer as shown in 図 8-12. The DC component of the REF70 is removed by using a high-pass filter and then amplified. When measuring broadband noise, it is not necessary to have high gain in order to achieve maximum bandwidth.

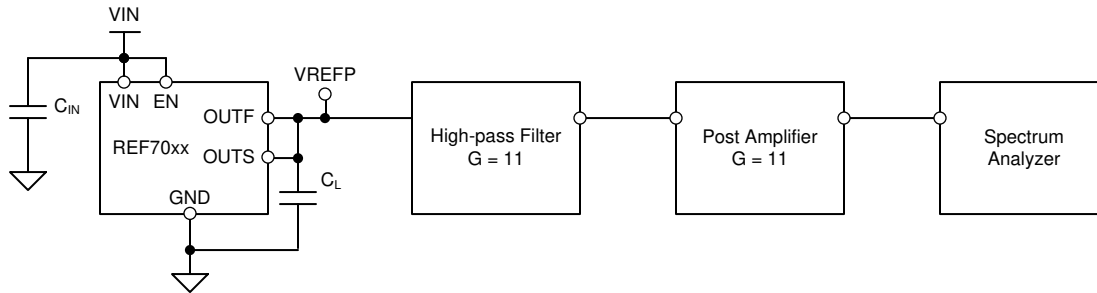


図 8-12. Broadband Noise Test Setup

For noise sensitive designs, a low-pass filter can be used to reduce broadband noise output noise levels by removing the high frequency components. When designing a low-pass filter special care must be taken to ensure the output impedance of the filter does not degrade ac performance. This can occur in RC low-pass filters where a large series resistance can impact the load transients due to output current fluctuations.

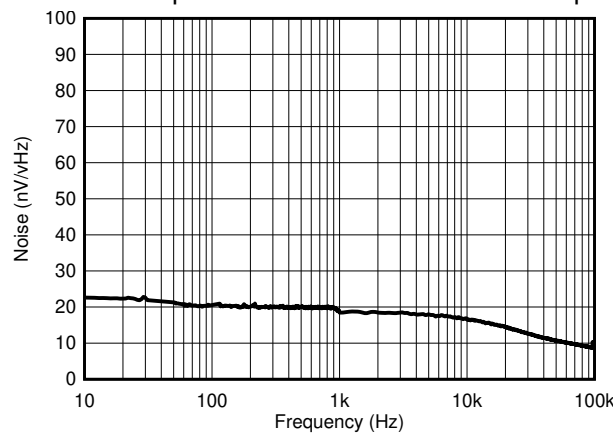


図 8-13. Noise Performance 10 Hz to 100 kHz

8.5 Temperature Drift

The REF70 is designed and tested for a minimal output voltage temperature drift, which is defined as the change in output voltage over temperature. Every unit shipped is tested at multiple temperatures to ensure that the product meets data sheet specifications. The temperature coefficient is calculated using the box method in which a box is formed by the min/max limits for the nominal output voltage over the operating temperature range. REF70 has a low maximum temperature coefficient of 2 ppm/°C from –40°C to +125°C. This method corresponds more accurately to the method of test and provides a closer estimate of actual error than the other methods. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Due to temperature curvature correction to achieve low-temperature drift, the temperature drift is expected to be non-linear. See [SLYT183](#) for more information on the box method. The box method equation is shown in 式 2:

$$\text{Drift} = \left(\frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF(25°C)}} \times \text{Temperature Range}} \right) \times 10^6 \quad (2)$$

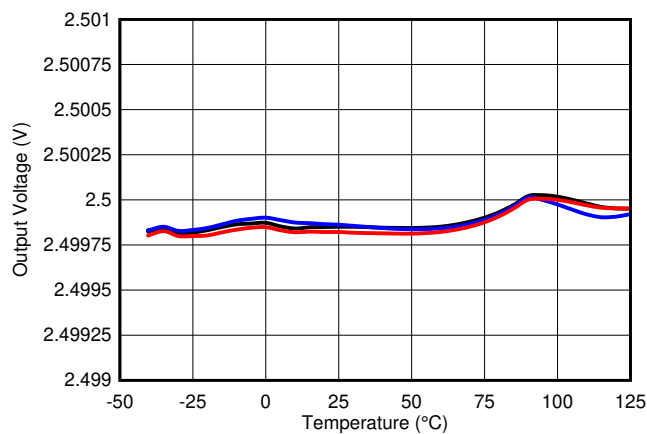


図 8-14. Output Voltage Vs Free-Air Temperature

8.6 Power Dissipation

The REF70 voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceed its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with 式 3:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (3)$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

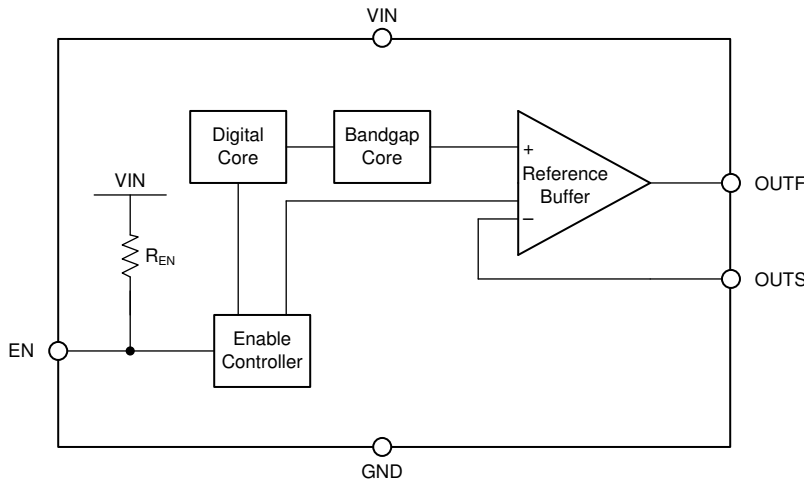
Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

9 Detailed Description

9.1 Overview

The REF70 is family of ultra low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The [セクション 9.2](#) is a simplified block diagram of the REF70 showing basic band-gap topology.

9.2 Functional Block Diagram




9.3 Feature Description

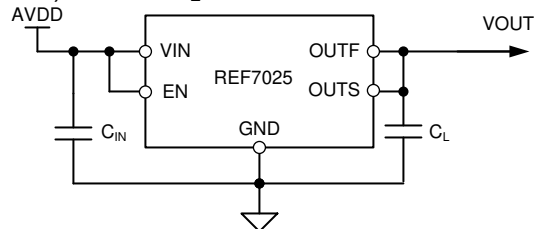
9.3.1 EN Pin

The EN pin of the REF70 has an internal 16 M Ω pull-up resistor (R_{EN}) to VIN. This allows the EN pin of the REF70 to be left floating. When the EN pin of the REF70 is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF70 can be placed in shutdown mode by pulling the EN pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 12 μ A in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the [セクション 7.6](#) for logic high and logic low voltage levels.

9.4 Device Functional Modes

9.4.1 Basic Connections


 [9-1](#) shows the typical connections for the REF70. TI recommends a supply bypass capacitor (C_{IN}) ranging from 0.1- μ F to 10- μ F. A 1- μ F to 100- μ F output capacitor (C_L) must be connected from OUTF to GND. The equivalent series resistance (ESR) value of C_L must be 1 m Ω to 400 m Ω to ensure output stability.



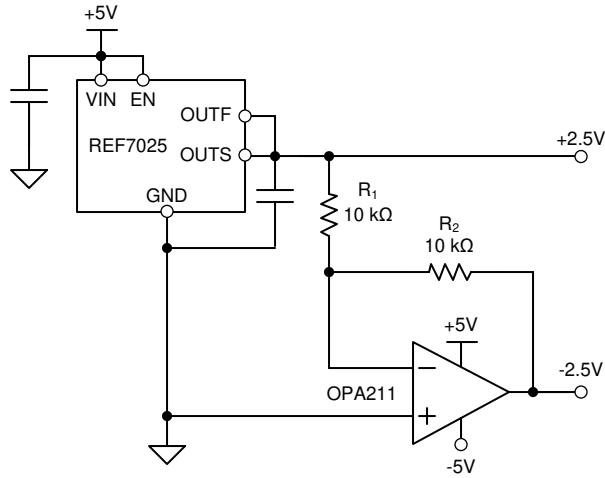
Copyright © 2020, Texas Instruments Incorporated

9-1. Basic Connections

9.4.2 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF70 and OPA211 can be used to provide a dual-supply reference from a 5-V supply.  [9-2](#) shows the REF70 used to provide a 2.5-V supply reference voltage and -2.5V negative reference voltage. The low noise performance of the REF70 complements

the low noise of the OPA211 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.



Copyright © 2020, Texas Instruments Incorporated

9-2. The REF70 and OPA211 Create Positive and Negative Reference Voltages

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

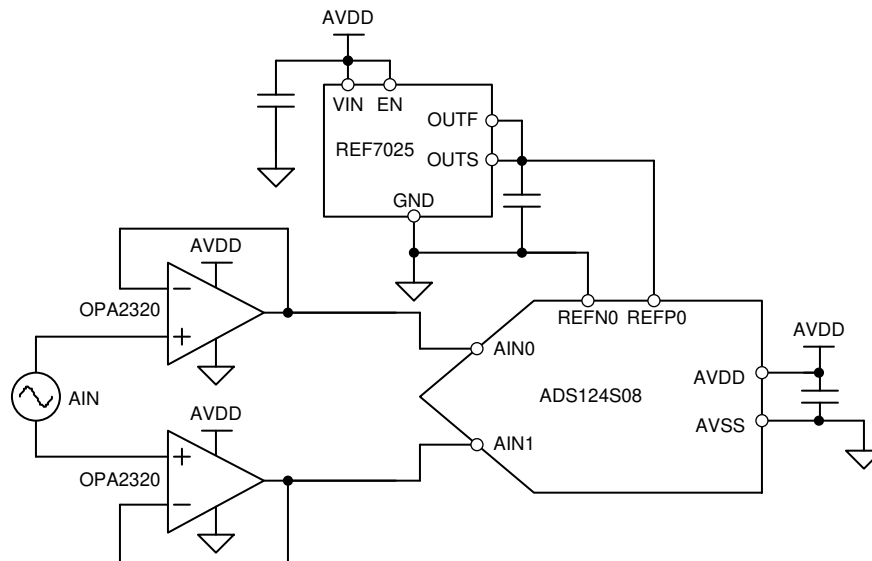
This device is a natural fit for many precision applications and it can be connected to system components in various ways and thus there are many situations that this data sheet can not characterize in detail. Basic applications include positive/negative voltage reference and data acquisition systems. The table below shows the typical applications of REF70 and its companion data converters.

APPLICATION	DATA CONVERTER
Precision Data Acquisition	ADS124S08, ADS8900B, ADS1278, ADS1262, DAC80501, DAC8562
Industrial Instrumentation	ADS127L01, ADS8699, ADS1256, ADS1251, DAC9881, DAC8811, DAC1220, DAC80508
Semiconductor Test	ADS8598H, ADS131M08, ADS8686S, ADS8881, DAC11001A, DAC91001A, DAC7744
Power Monitoring, PLC Analog I/O	ADS131E04, ADS131A02,
Field Transmitters	ADS1247, ADS1220

10.2 Typical Applications

10.2.1 Typical Application: Basic Voltage Reference Connection

The circuit shown in [図 10-1](#) shows the basic configuration for the REF70 references. Connect bypass capacitors according to the guidelines in [セクション 10.2.1.2.1](#).



Copyright © 2020, Texas Instruments Incorporated

図 10-1. Basic Reference Connection

10.2.1.1 Design Requirements

A detailed design procedure is based on a design example. For this design example, use the parameters listed in [表 10-1](#) as the input parameters.

表 10-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	5.5 V
Output voltage V_{OUT}	2.5 V
REF7025 input capacitor	10- μ F
REF7025 output capacitor	10- μ F

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Input and Output Capacitors

A 1 μ F to 10 μ F bypass capacitor should be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1 μ F capacitor in parallel to reduce high frequency supply noise.

A low ESR capacitor of 1 μ F to 100 μ F must be connected to the output to improve stability and help filter out high frequency noise. Best performance and stability is attained with low-ESR output capacitors with an ESR from 1 m Ω to 400 m Ω . For very low noise applications, special care must be taken with X7R and other MLCC capacitors due to their piezoelectric effect. Mechanical vibration can transduce to voltage via the piezoelectric effect which appears as noise in the μ V range, potentially dominating the noise of the REF70. More information on how the piezoelectric effect can be explored in systems can be found in [Stress-induced outbursts: Microphonics in ceramic capacitors \(Part 1\)](#) and [Stress-induced outbursts: Microphonics in ceramic capacitors \(Part 2\)](#). It is recommended that to use film capacitors for noise sensitive applications.

The transient startup response of the REF70 is shown in [図 10-2](#). The startup response of the REF70 family is dependent on the output capacitor. While larger capacitors will decrease the output noise, they will increase the startup response.

10.2.1.2.1.1 Application Curve

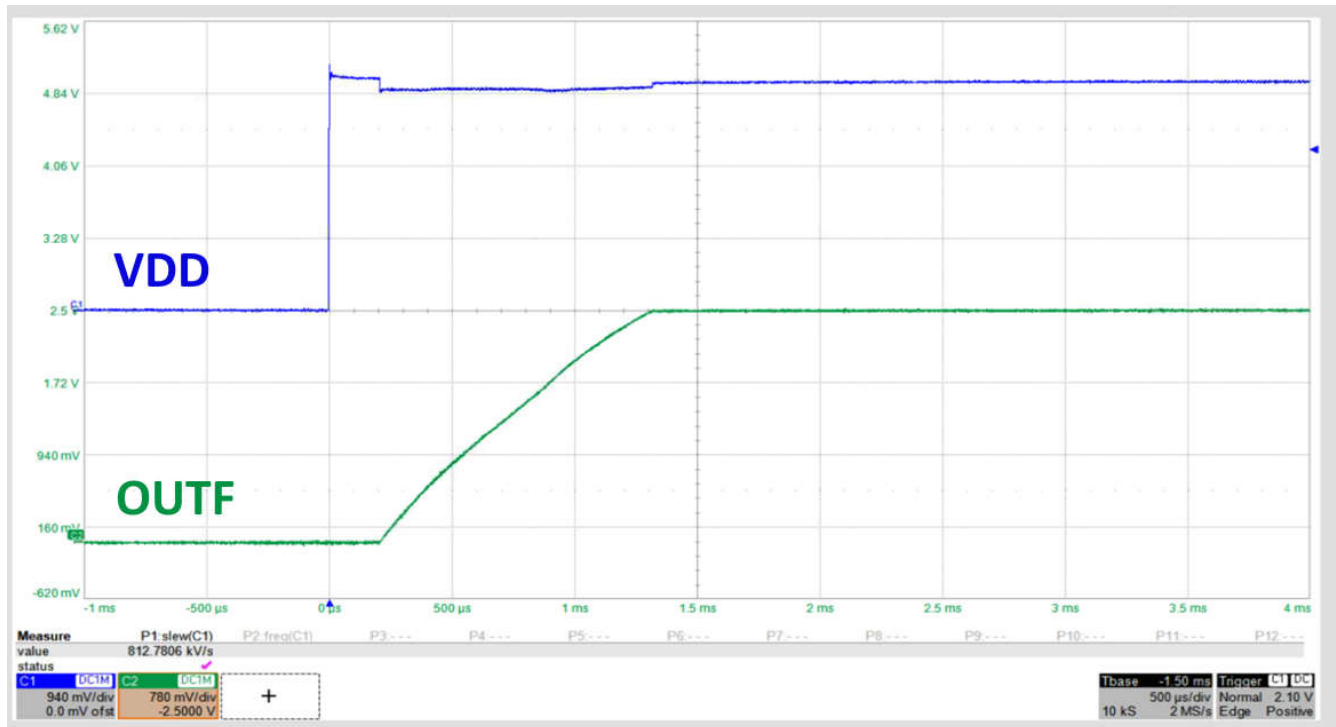


図 10-2. REF7025 Startup (C = 10 μF)

10.2.1.2.2 Force and Sense Connection

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this drop can reach several millivolts or more, introducing a considerable error into the output voltage of the reference. A 3000-mil long, 15-mil wide trace of 1-ounce copper has a resistance of approximately 100 mΩ at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error. In an ideal board layout, the reference must be mounted as close as possible to the load to minimize the length of the output traces, and, therefore, the error introduced by voltage drop. However, in applications where this is not possible or convenient, force and sense connections (sometimes referred to as Kelvin sensing connections) are provided as a means of minimizing the IR drop and improving accuracy.

Kelvin connections work by providing a set of high impedance voltage-sensing lines to the output and ground nodes. Because very little current flows through these connections, the IR drop across their traces is negligible, and the output and ground. The REF70 has kelvin connection capabilities due to its output force (OUTF) and input sense (OUTS) connection as shown in [Basic Reference Connection](#). The output force voltage will vary upwards from the internal V_{REF} voltage to ensure that at V_{OUT} , which is where the OUTF and OUTS connect at the point-of-load, the voltage will be precisely V_{REF} . The sense connection on the REF70 requires 4 mA due to its architecture.

It is always advantageous to use Kelvin connections whenever possible. However, in applications where the IR drop is negligible or an extra set of traces cannot be routed to the load, the force and sense pins for V_{OUT} can simply be tied together close to the pins, and the device can be used in the same fashion as a normal 3-terminal reference.

10.2.2 Typical Application: DAC Force and Sense Reference Drive Circuit

Certain DACs require external voltage references to operate properly. There are DACs that only require a positive voltage for operating in which the basic connection will work. For other DACs there can be a need a positive and negative reference voltage due to their bipolar output.

The circuit shown in [Figure 10-3](#) shows a DAC force and sense reference drive circuit for the DACx1001 using the REF70. This circuit takes advantage of the DACx1001 RCM circuit to remove the need of additional external resistors to make a negative reference due to the integrated precision resistors. This circuit requires additional buffers due to undesired series resistance on the reference input of the DAC.

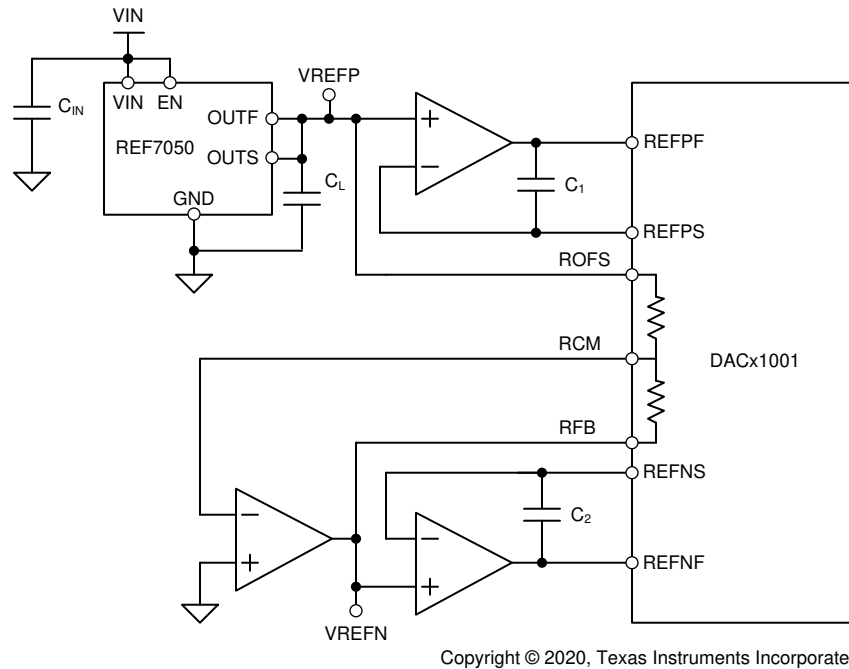


Figure 10-3. Basic Force and Sense Reference Drive Circuit Connections with DACx1001

10.2.2.1 Design Requirements

For this design example, use the reference op amp recommendation listed in [Table 10-2](#) for the buffer circuit.

Table 10-2. Reference Op Amp Options

SELECTION PARAMETERS	OP AMPS
Low voltage and current noise	OPA211, OPA827, OPA828
Low offset and drift	OPA189

The REF70 turn-on time is dependent on the output capacitor. In certain applications that require a fast turn-on can require a smaller output capacitor as shown in [Figure 10-4](#)

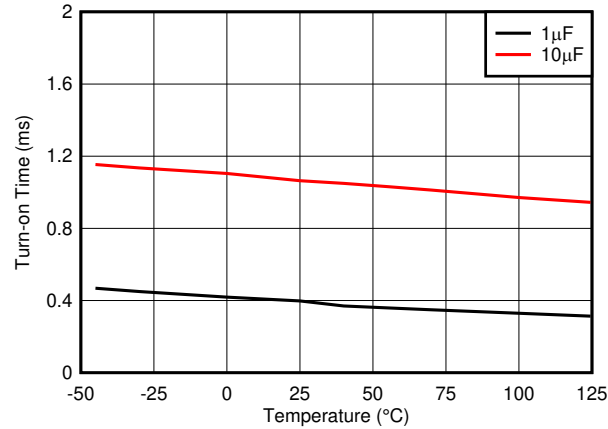
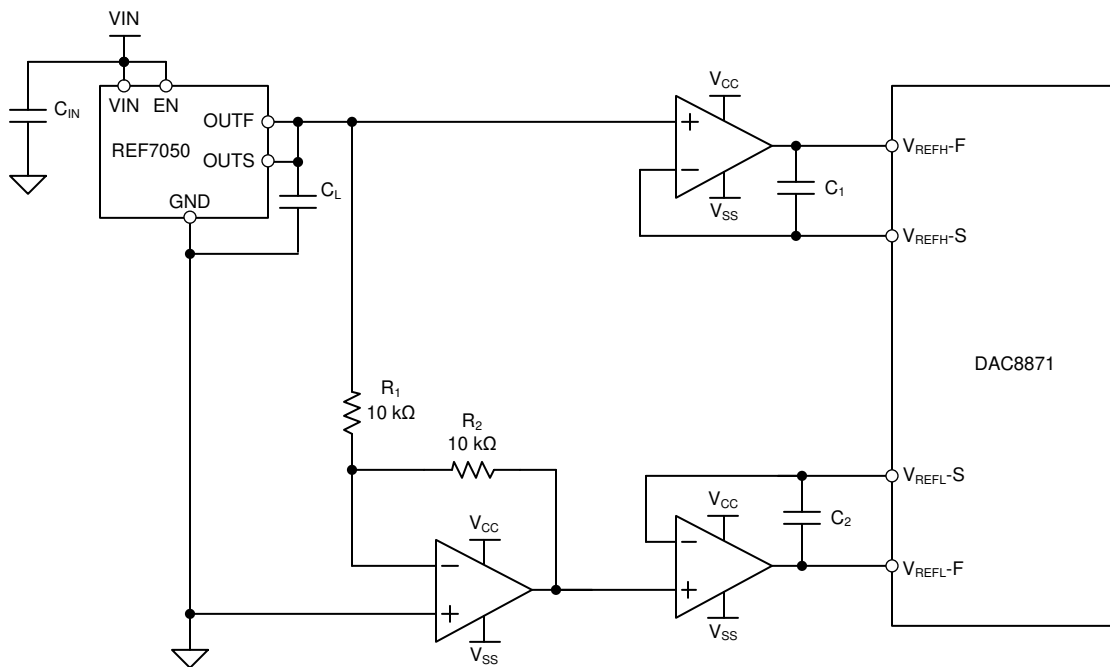


Figure 10-4. REF70 Turn-on Time

For DAC designs that do not have the RCM feature, use Figure 10-5 as it generates the negative reference circuit to create the VREFN. More details on this type of design can be found in SBAA322.



Copyright © 2020, Texas Instruments Incorporated

Figure 10-5. Basic Force and Sense Reference Drive Circuit Connections

10.3 Power Supply Recommendation

The REF70 family of references features a low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage for 0-mA output current conditions. The dropout voltage will vary with the output current so refer to the dropout voltage to see typical dropout voltage requirements. TI recommends a supply bypass capacitor ranging between 0.1 μF to 10 μF .

During start-up the REF70 can experience moments of high input current due to the output capacitors. The input current can momentarily rise to I_{SC} .

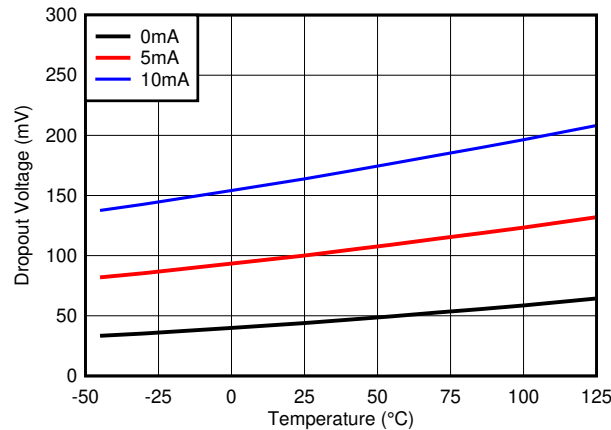


FIG 10-6. Dropout Voltage vs Temperature

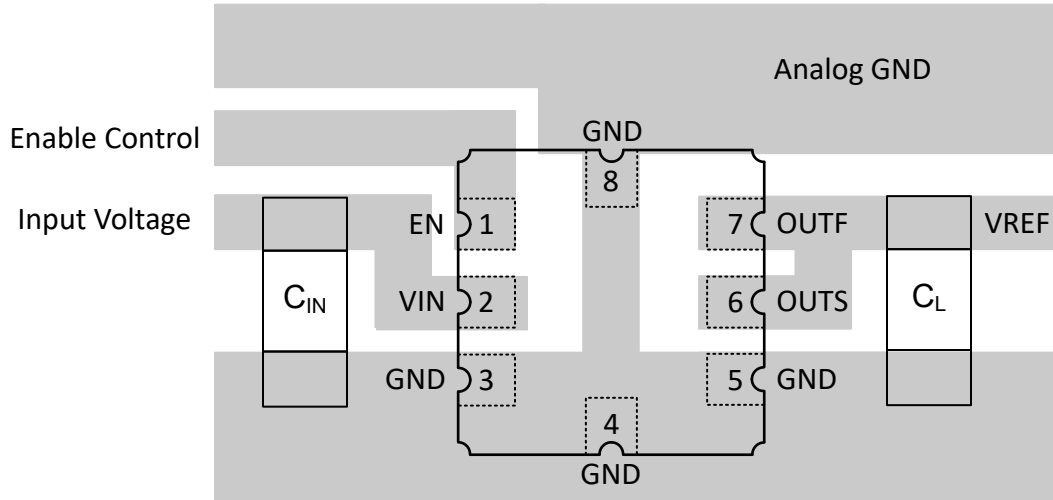
10.4 Layout

10.4.1 Layout Guidelines

FIG 10-7 and FIG 10-8 illustrate an example of a PCB layout for a data acquisition system using the REF70. Some key considerations are:

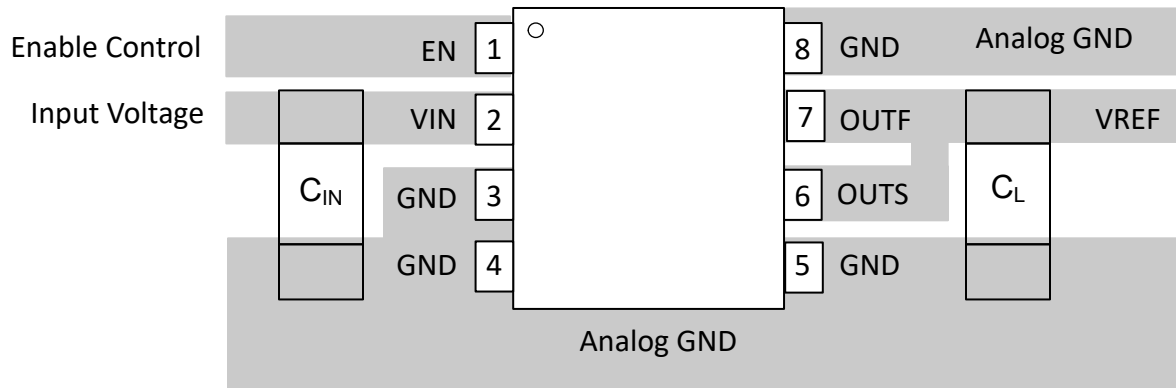
- Connect low-ESR, 0.1- μF ceramic bypass capacitors at V_{IN} of the REF70.
- Connect low-ESR, 1- μF to 100- μF capacitor at $OUTF$ of the REF70.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

10.4.2 Layout Example



Copyright © 2020, Texas Instruments Incorporated

☒ 10-7. Layout Example FKH Package



Copyright © 2023, Texas Instruments Incorporated

☒ 10-8. Layout Example DGK Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Voltage Reference Design Tips For Data Converters](#)
- Texas Instruments, [Voltage Reference Selection Basics](#)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF7012QDGKR	ACTIVE	VSSOP	DGK	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2L1S	Samples
REF7012QFKHT	ACTIVE	LCCC	FKH	8	250	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-40 to 125	REF12FKH	Samples
REF7025QDGKR	ACTIVE	VSSOP	DGK	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TAS	Samples
REF7025QFKHT	ACTIVE	LCCC	FKH	8	250	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-40 to 125	REF25FKH	Samples
REF7030QFKHT	ACTIVE	LCCC	FKH	8	250	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-40 to 125	REF30FKH	Samples
REF7033QFKHT	ACTIVE	LCCC	FKH	8	250	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-40 to 125	REF33FKH	Samples
REF7040QDGKR	ACTIVE	VSSOP	DGK	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TDS	Samples
REF7040QFKHT	ACTIVE	LCCC	FKH	8	250	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-40 to 125	REF40FKH	Samples
REF7050QDGKR	ACTIVE	VSSOP	DGK	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2TES	Samples
REF7050QFKHT	ACTIVE	LCCC	FKH	8	250	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-40 to 125	REF50FKH	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

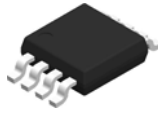
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF7012QDGKR	VSSOP	DGK	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF7012QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7025QDGKR	VSSOP	DGK	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF7025QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7030QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7033QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7040QDGKR	VSSOP	DGK	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF7040QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2
REF7050QDGKR	VSSOP	DGK	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF7050QFKHT	LCCC	FKH	8	250	180.0	12.4	5.35	5.35	1.57	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF7012QDGKR	VSSOP	DGK	8	3000	356.0	356.0	35.0
REF7012QFKHT	LCCC	FKH	8	250	210.0	185.0	35.0
REF7025QDGKR	VSSOP	DGK	8	3000	356.0	356.0	35.0
REF7025QFKHT	LCCC	FKH	8	250	210.0	185.0	35.0
REF7030QFKHT	LCCC	FKH	8	250	210.0	185.0	35.0
REF7033QFKHT	LCCC	FKH	8	250	210.0	185.0	35.0
REF7040QDGKR	VSSOP	DGK	8	3000	356.0	356.0	35.0
REF7040QFKHT	LCCC	FKH	8	250	210.0	185.0	35.0
REF7050QDGKR	VSSOP	DGK	8	3000	356.0	356.0	35.0
REF7050QFKHT	LCCC	FKH	8	250	210.0	185.0	35.0

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



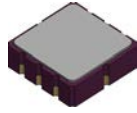
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

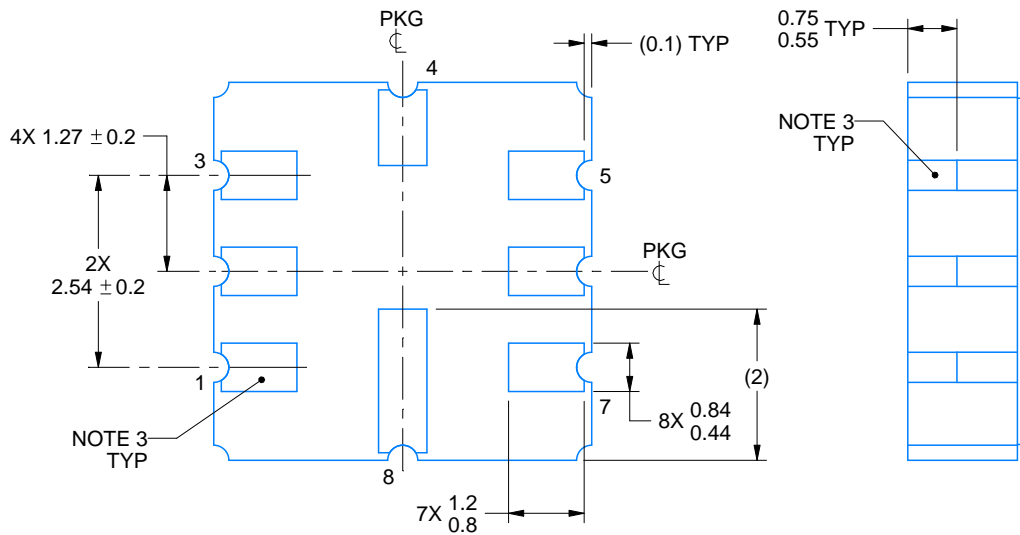
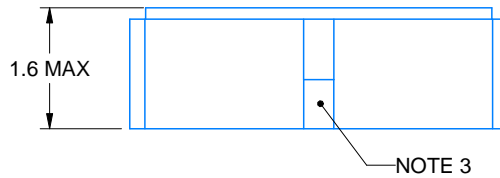
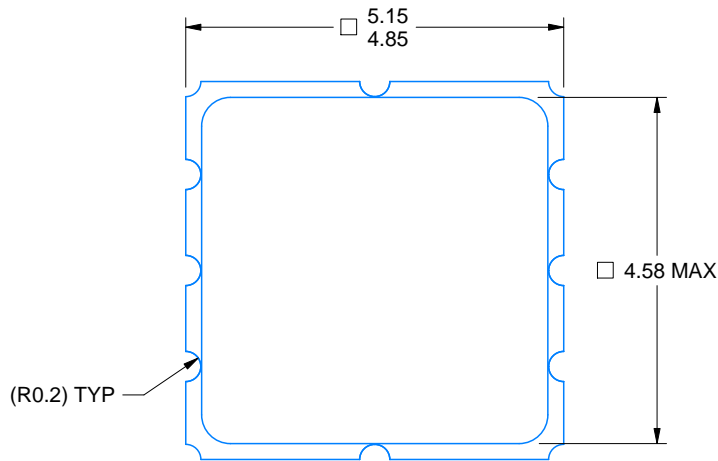
FKH0008A



PACKAGE OUTLINE

LCCC - 1.6 mm max height

LEADLESS CERAMIC CHIP CARRIER



4222330/E 04/2023

NOTES:

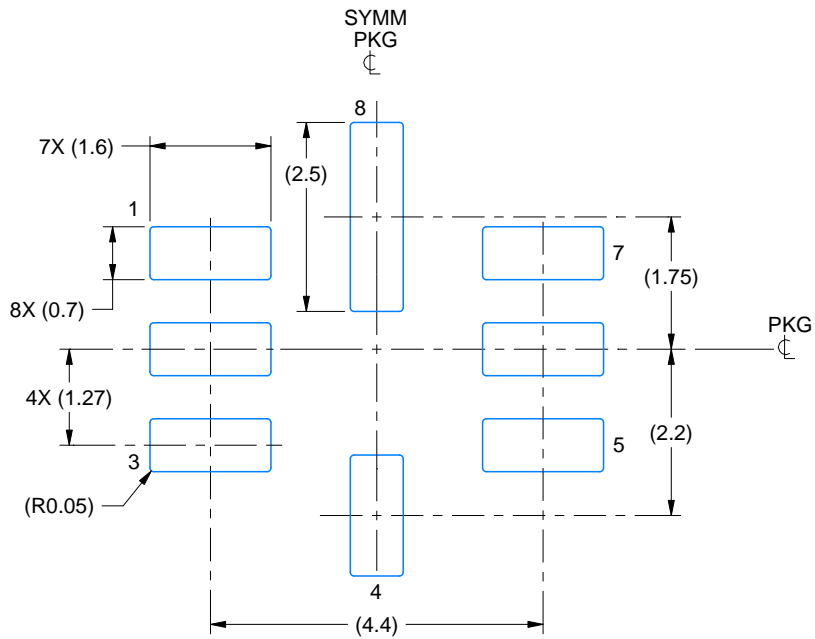
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. Terminals are gold plated.

EXAMPLE BOARD LAYOUT

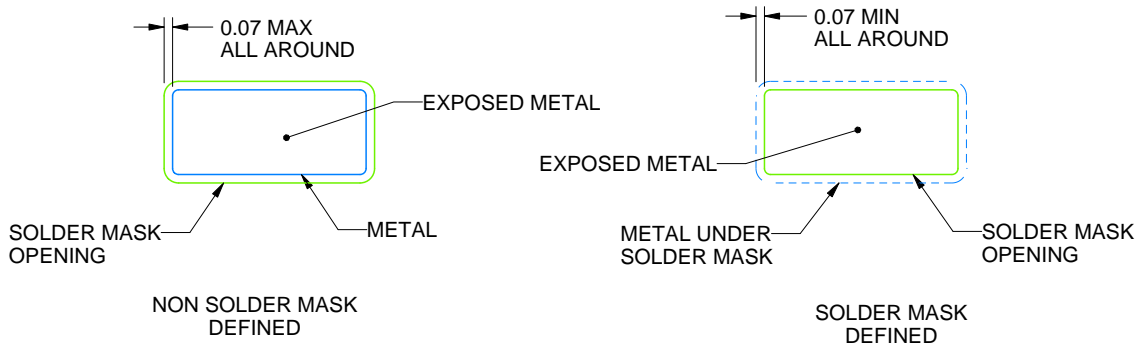
FKH0008A

LCCC - 1.6 mm max height

LEADLESS CERAMIC CHIP CARRIER



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS

4222330/E 04/2023

NOTES: (continued)

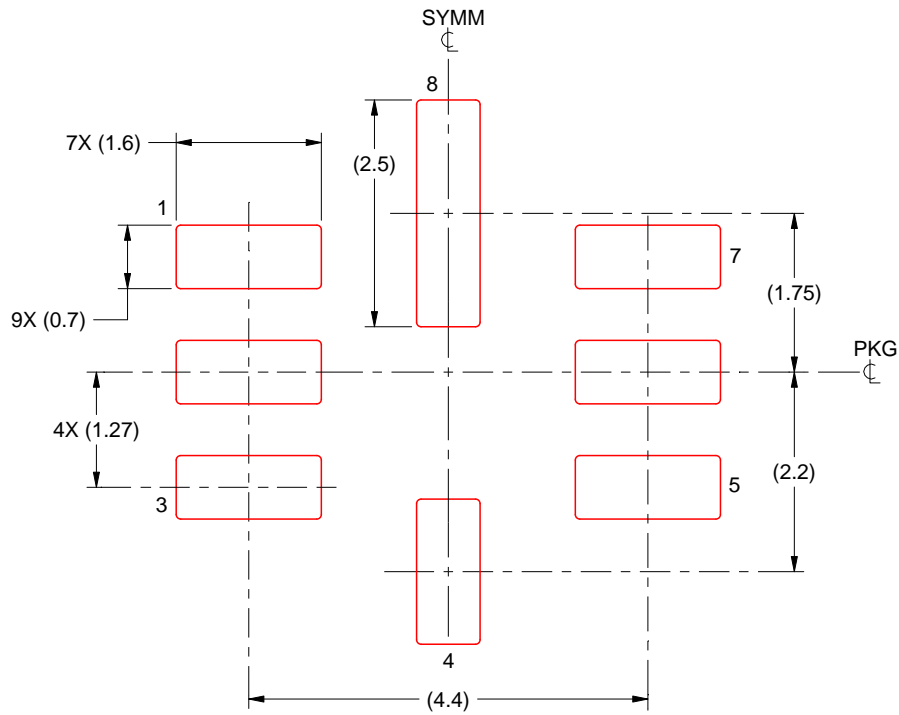
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

FKH0008A

LCCC - 1.6 mm max height

LEADLESS CERAMIC CHIP CARRIER



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:12X

4222330/E 04/2023

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated