RC4580 デュアル オーディオ オペアンプ

1 特長

- 動作電圧±2V～±18V
- 低いノイズ電圧:0.8μVrms
- ゲイン帯域幅積:12MHz
- 全高調波歪み:0.0005%
- スルーレート:5V/μs
- NJM4580 のドロップイン代替品
- LM833、NE5532、NJM4558/9、NJM4560/2/5 デバイスとピンおよび機能が互換

2 アプリケーション

- オーディオ プリアンプ
- アクティブ フィルタ
- ヘッドホン アンプ
- 産業用の測定機器

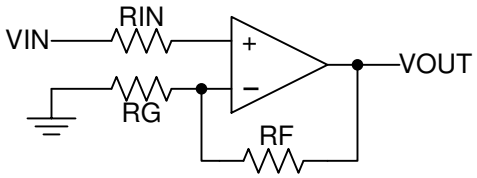
3 概要

RC4580 デバイスは、トーン制御の改善など、オーディオ アプリケーション向けに最適化された設計のデュアル オペアンプです。このデバイスはノイズが低く、ゲイン帯域幅が高く、高調波歪みが小さく、出力電流が大きくて、プリアンプ、アクティブ フィルタ、産業用測定機器などのオーディオ エレクトロニクス用に設計されています。大きな出力電流が必要な場合、RC4580 デバイスをヘッドフォン アンプとして使用できます。RC4580 デバイスはデバイスの動作電源電圧範囲が広いため、低電圧アプリケーションでも使用できます。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (2)
RC4580	D (SOIC、8)	3.9mm × 4.9mm
	P (PDIP、8)	9.81mm × 9.43mm
	PW (TSSOP、8)	3.0mm × 4.4mm
	DGK (VSSOP、8)	3.0mm × 3.0mm
	DDF (SOT-23、8)	1.6mm × 2.9mm

(1) 供給されているすべてのパッケージについては、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



非反転アンプの回路図

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4 Pin Configuration and Functions

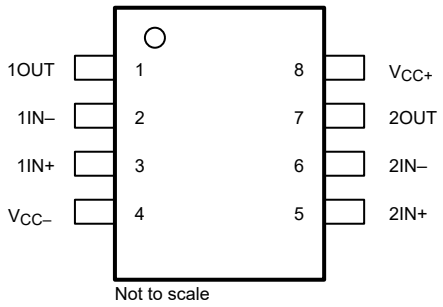


図 4-1. D, PW, and DGK Packages 8-Pin SOIC, TSSOP, and VSSOP (Top View)

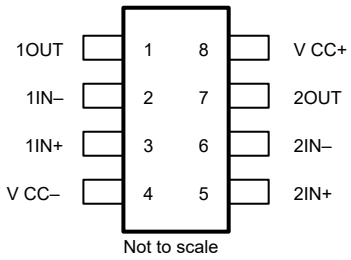


図 4-2. DDF Package 8-Pin SOT-23 (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN–	2	I	Inverting input
1OUT	1	O	Output
2IN+	5	I	Noninverting input
2IN–	6	I	Inverting input
2OUT	7	O	Output
V_{CC+}	8	—	Positive supply
$V_{CC–}$	4	—	Negative supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		±18	V
V_I	Input voltage (any input)		±15	V
V_{ID}	Differential input voltage		±30	V
I_O	Output current		±50	mA
T_A	Ambient temperature range	–40	125	°C
T_{stg}	Storage temperature range	–60	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	2	16	V
$V_{CC–}$		–2	–16	
V_{ICR}	Input common-mode voltage range	–13.5	13.5	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		RC4580					UNIT
		D (SOIC)	P (PDIP)	PW (TSSOP)	DGK (VSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109	99.2	163	160.5	177.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.7	78.8	38	70.2	96.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	49	61.9	90.6	95.6	95.2	
ψ_{JT}	Junction-to-top characterization parameter	10.6	44.8	1.3	8.8	9.5	
ψ_{JB}	Junction-to-board characterization parameter	48.6	61.2	88.9	94.0	95.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

$V_{CC±}$ = ±15 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S = < 10kΩ		0.5	3	mV
I_{IO}	Input offset current			5	200	nA
I_{IB}	Input bias current			100	500	nA
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ, V_O = ±10V	90	110		dB
V_{CM}	Output voltage swing	R_L ≥ 2kΩ	±12	±13.5		V
V_{ICR}	Common-mode input voltage		±12	±13.5		V
CMRR	Common-mode rejection ratio	R_S ≤ 10kΩ	80	110		dB
k_{SVR}	Supply-voltage rejection ratio(1)	R_S ≤ 10kΩ	80	110		dB
I_{CC}	Total supply current (all amplifiers)			6	9	mA

(1) Measured with $V_{CC±}$ varied simultaneously

5.6 Operating Characteristics

$V_{CC±}$ = ±15 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	R_L ≥ 2kΩ	5	V/µs
GBW	Gain-bandwidth product	f = 10kHz	12	MHz
THD	Total harmonic distortion	V_O = 5V, R_L = 2kΩ, f = 1kHz, A_{VD} = 20dB	0.0005%	
V_n	Equivalent input noise voltage	RIAA, R_S ≤ 2.2kΩ, 30kHz LPF	0.8	µVrms

5.7 Typical Characteristics

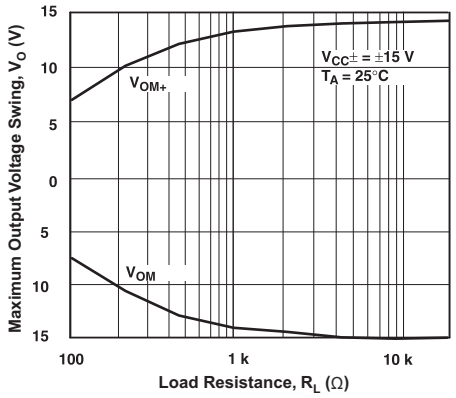


図 5-1. Maximum Output Voltage Swing vs Load Resistance

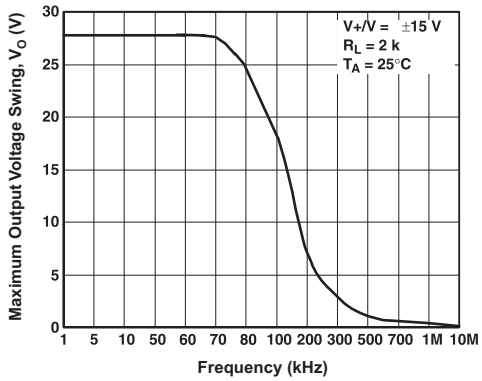


図 5-2. Maximum Ouput Voltage Swing vs Frequency

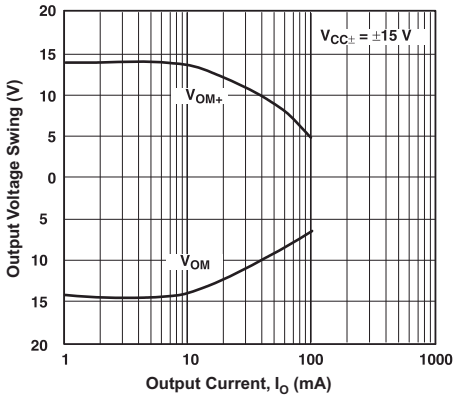


図 5-3. Output Voltage Swing vs Output Current

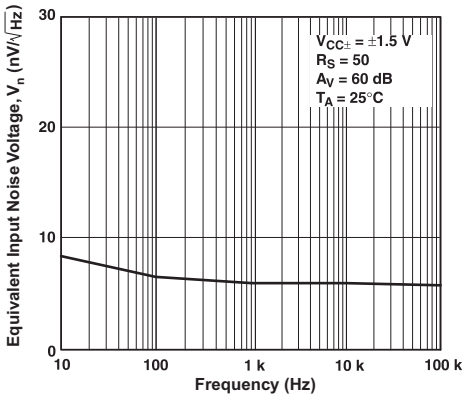


図 5-4. Equivalent Input Noise Voltage vs Frequency

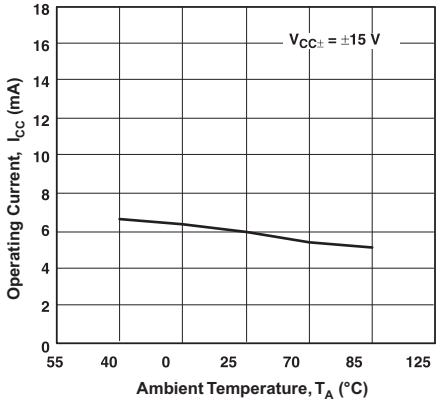


図 5-5. Operating Current vs Temperature

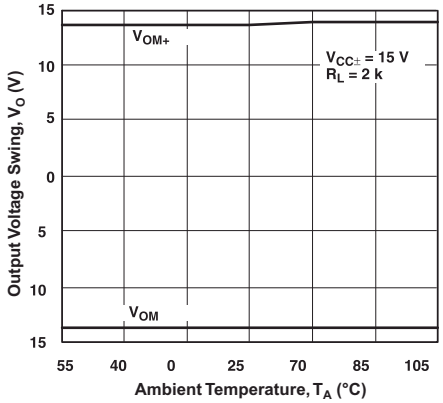


図 5-6. Output Voltage Swing vs Temperature

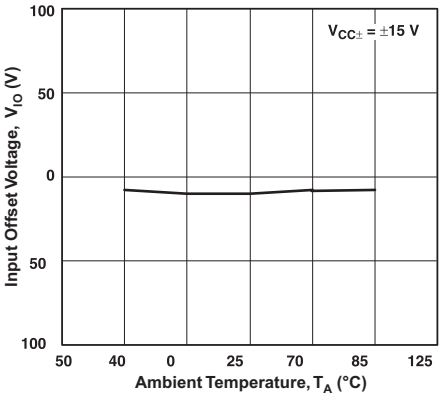


図 5-7. Input Offset Voltage vs Temperature

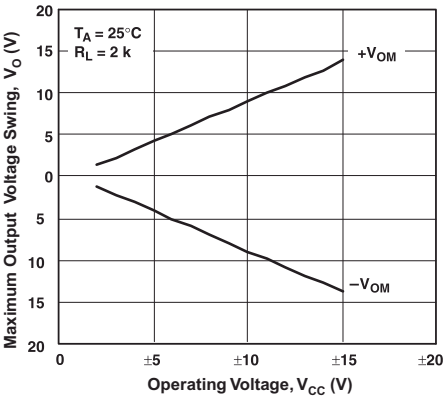


図 5-8. Input Bias Current vs Temperature

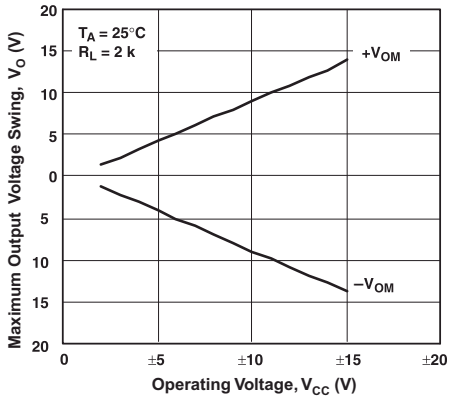


図 5-9. Maximum Output Voltage Swing vs Operating Voltage

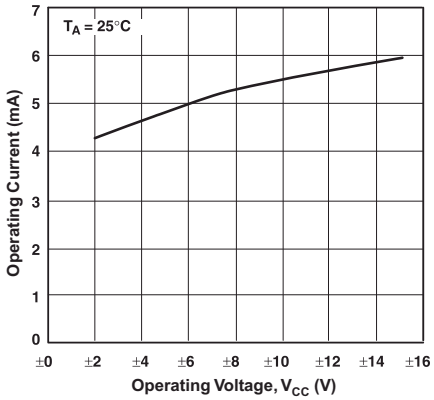


図 5-10. Operating Current vs Operating Voltage

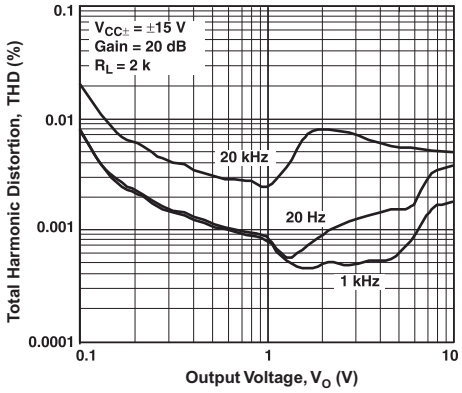


図 5-11. Total Harmonic Distortion vs Output Voltage

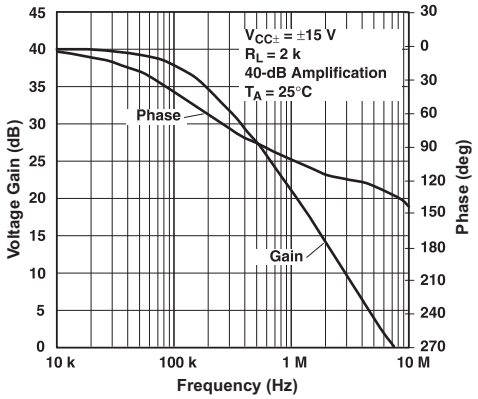


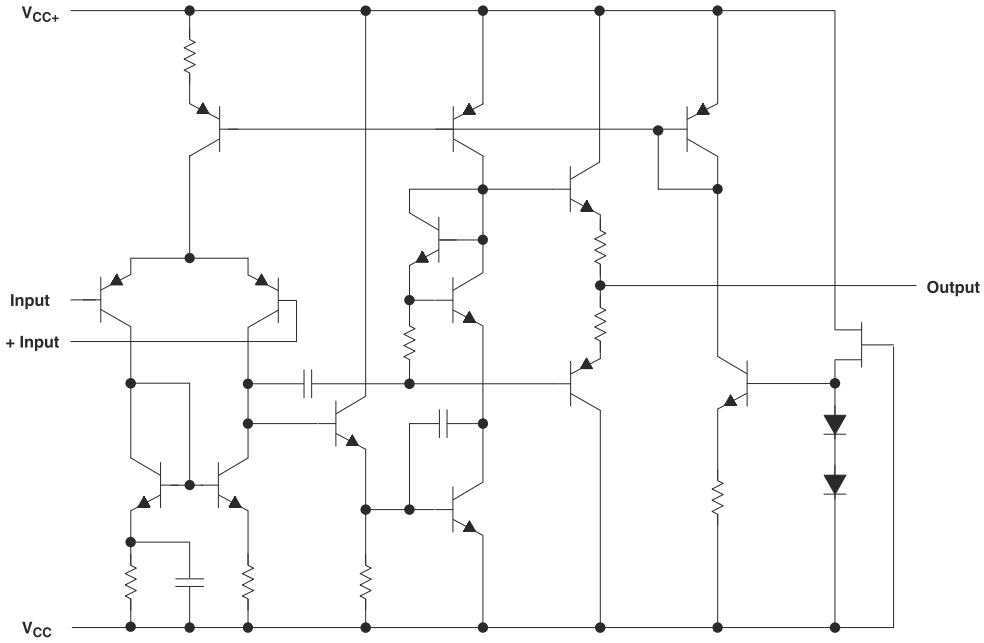
図 5-12. Voltage Gain, Phase vs Frequency

6 Detailed Description

6.1 Overview

The RC4580 device is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. The device offers low noise, high gain bandwidth, low harmonic distortion, and high output current. When high output current is required, the RC4580 device can be used as a headphone amplifier. Due to the wide operating supply voltage of the device, the RC4580 device can also be used in low-voltage applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The RC4580 device has a 12MHz unity-gain bandwidth.

6.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. The CMRR is found by taking the ratio of the change in input offset voltage to the change in the input voltage, then converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have the CMRR as high as possible. The CMRR of the RC4580 device is 110dB.

6.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change the op amp output when there is a change on the input. The RC4580 device has a 5V/µs slew rate.

6.4 Device Functional Mode

The RC4580 device is powered on when the supply is connected. Each device can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Typical Application

Some applications require differential signals. 図 7-1 shows a simple circuit to convert a single-ended input of 2V to 10V into differential output of ±8V on a single 15V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 2V to 10V. The difference, V_{DIFF}, is the difference between V_{OUT+} and $V_{OUT–}$.

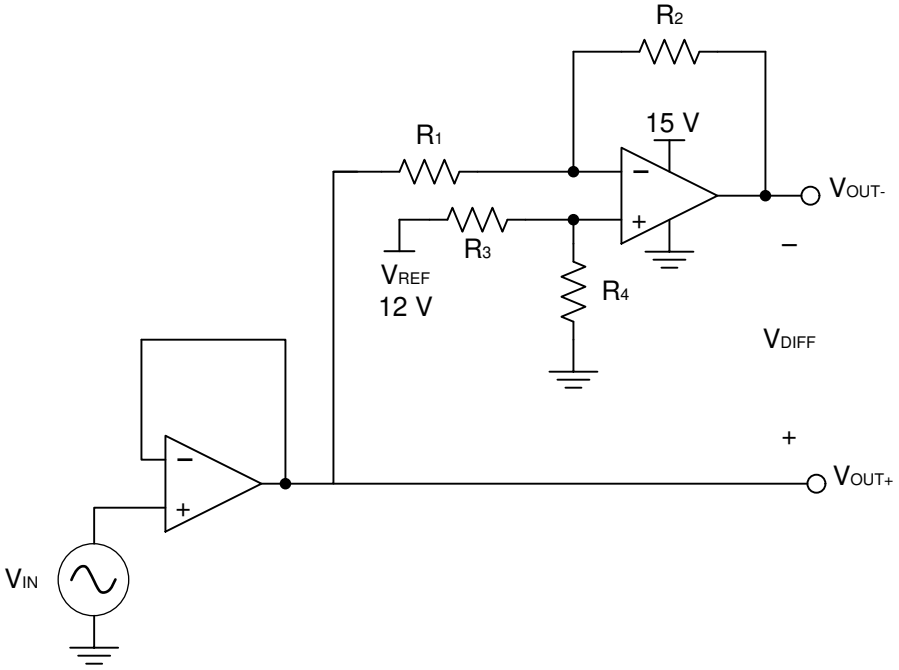


図 7-1. Schematic for Single-Ended Input to Differential Output Conversion

7.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15V
- Reference voltage: 12V
- Input: 2V to 10V
- Output differential: ±8V

7.1.2 Detailed Design Procedure

The circuit in 図 7-1 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and $V_{OUT–}$ using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see 式 1). $V_{OUT–}$ is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for $V_{OUT–}$ is 式 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT–} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) – V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and $V_{OUT–}$. 式 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into 式 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common-mode voltage is one half of V_{REF} (see 式 7).

$$V_{DIFF} = V_{OUT+} – V_{OUT–} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) – V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT–} = V_{REF} – V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} – V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT–}}{2}\right) = \frac{1}{2} V_{REF} \tag{7}$$

7.1.2.1 Amplifier Selection

Linearity over the input range is key for good DC accuracy. The common-mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. The RC4580 device has a bandwidth of 12MHz, therefore this circuit is only be able to process signals with frequencies of less than 12MHz.

7.1.2.2 Passive Component Selection

Because the transfer function of $V_{OUT–}$ is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36kΩ with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

7.1.3 Application Curves

The measured transfer functions in 図 7-2, 図 7-3, and 図 7-4 were generated by sweeping the input voltage from 0V to 12V. However, this design should only be used between 2V and 10V for optimum linearity.

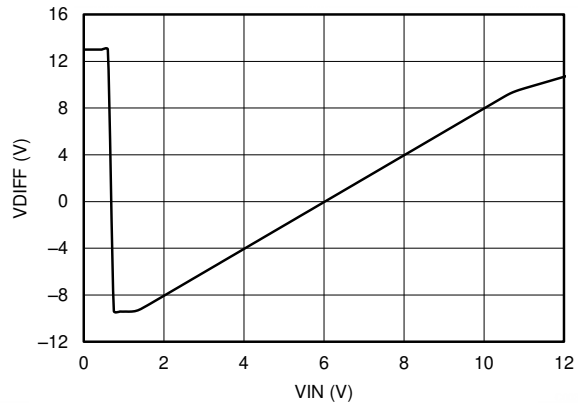


図 7-2. Differential Output Voltage vs Input Voltage

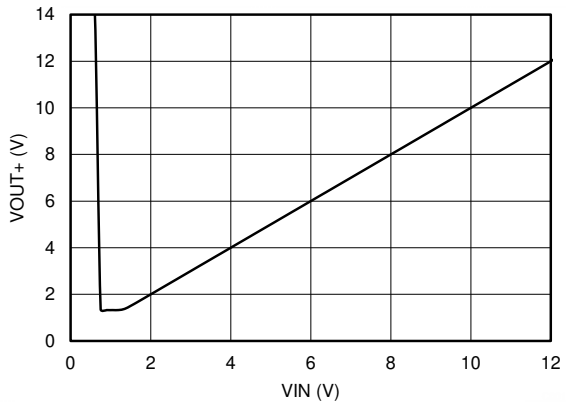


図 7-3. Positive Output Voltage vs Input Voltage

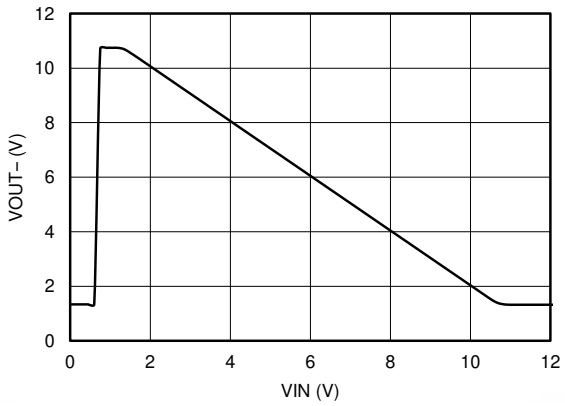


図 7-4. Positive Output Voltage vs Input Voltage

7.2 Power Supply Recommendations

The RC4580 device is specified for operation over the range of ±2V to ±16V; many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

> **注意**
>
> Supply voltages outside of the ±18V range can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

7.3 Layout

7.3.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.3.2 Layout Example

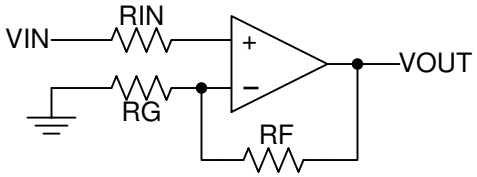


図 7-5. Operational Amplifier Schematic for Noninverting Configuration

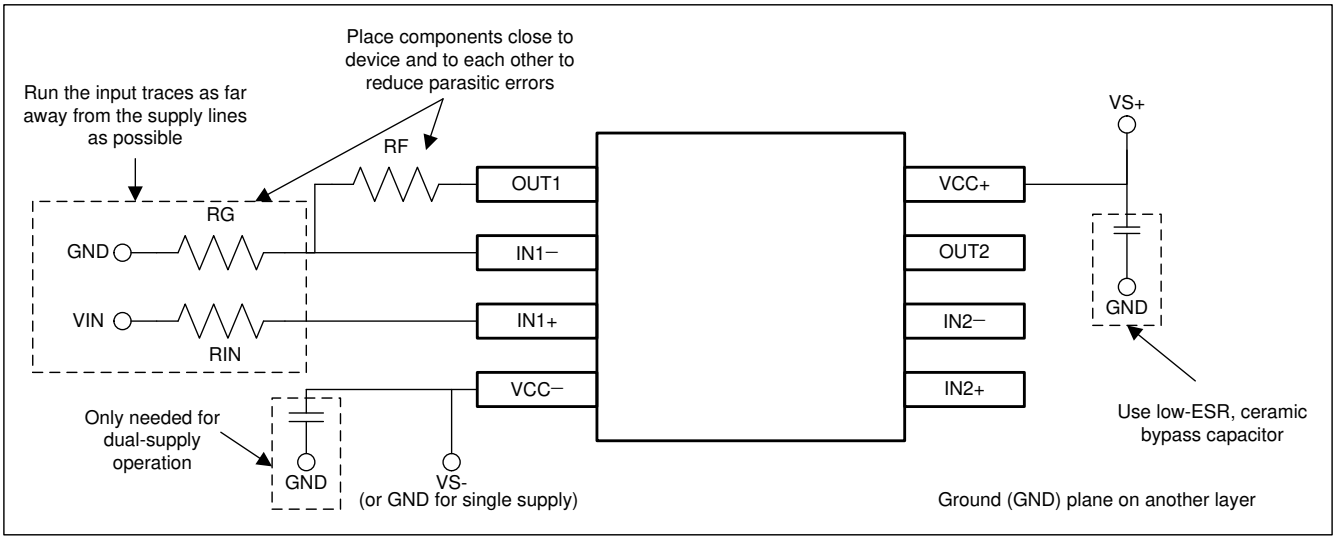


図 7-6. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision D (November 2014) to Revision E (November 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- P (PDIP、8)、DGK (VSSOP、8)、DDF (SOT-23、8) パッケージをデータシートに追加 1
- Changed the slew rate value listed in the *Slew Rate* section from: 5V/ms to: 5V/µs to match the slew rate values listed in the *Features* section and *Electrical Characteristics* table 8
- Deleted references to the *Circuit Board Layout Techniques* application note 11

Changes from Revision C (March 2004) to Revision D (November 2014) **Page**

- 「アプリケーション」、「デバイス情報」表、「ピンの機能」表、「取り扱い定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 1
- 「注文情報」表を削除。 1
- Changed T_A = 25°C to T_A = –40°C to 125°C in condition statement for *Electrical Characteristics* table and *Operational Characteristics* table 5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

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上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4580ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	R4580I	
RC4580IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580F	Samples
RC4580IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580	Samples
RC4580IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I	Samples
RC4580IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	RC4580IP	Samples
RC4580IPW	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 125	R4580I	
RC4580IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF RC4580 :

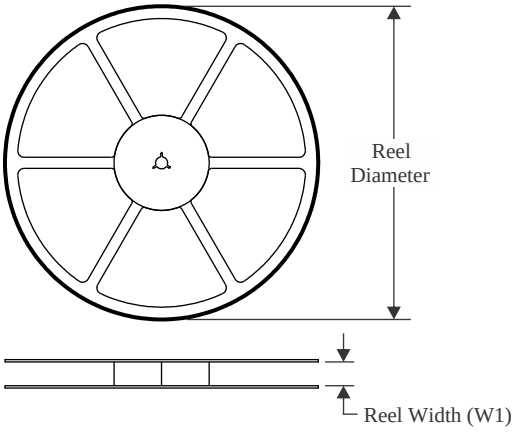
- Automotive : RC4580-Q1

NOTE: Qualified Version Definitions:

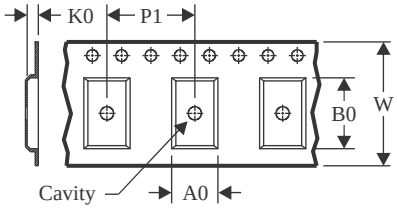
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

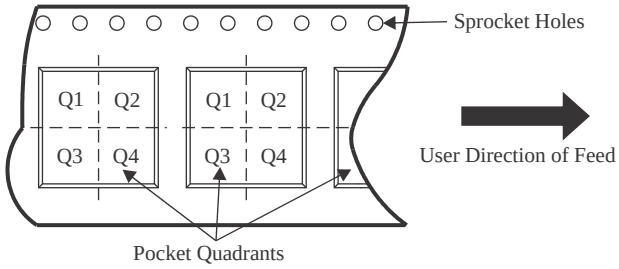


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

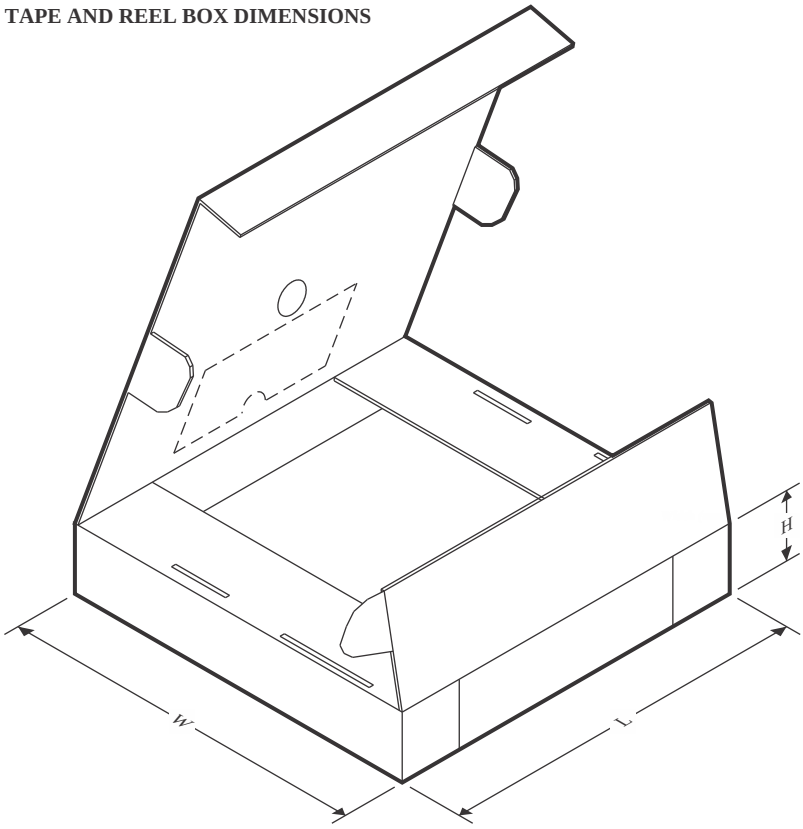
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4580IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
RC4580IDGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

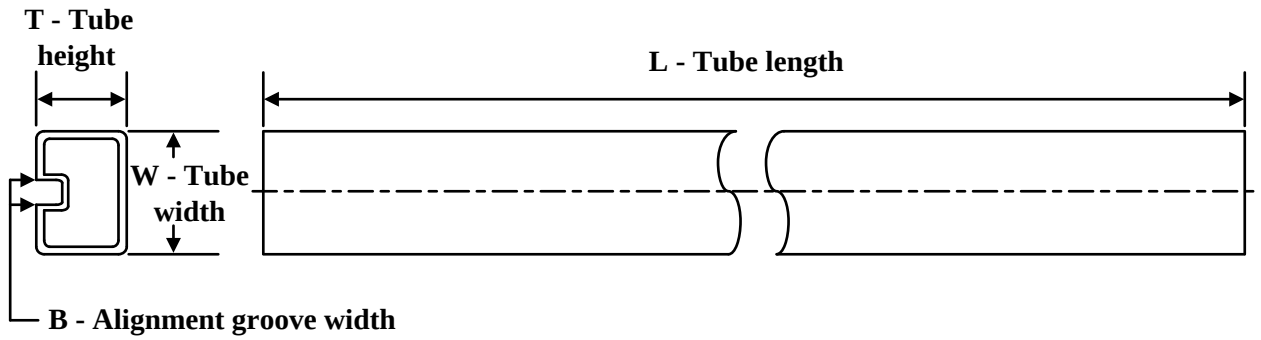
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4580IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
RC4580IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
RC4580IDR	SOIC	D	8	2500	353.0	353.0	32.0
RC4580IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

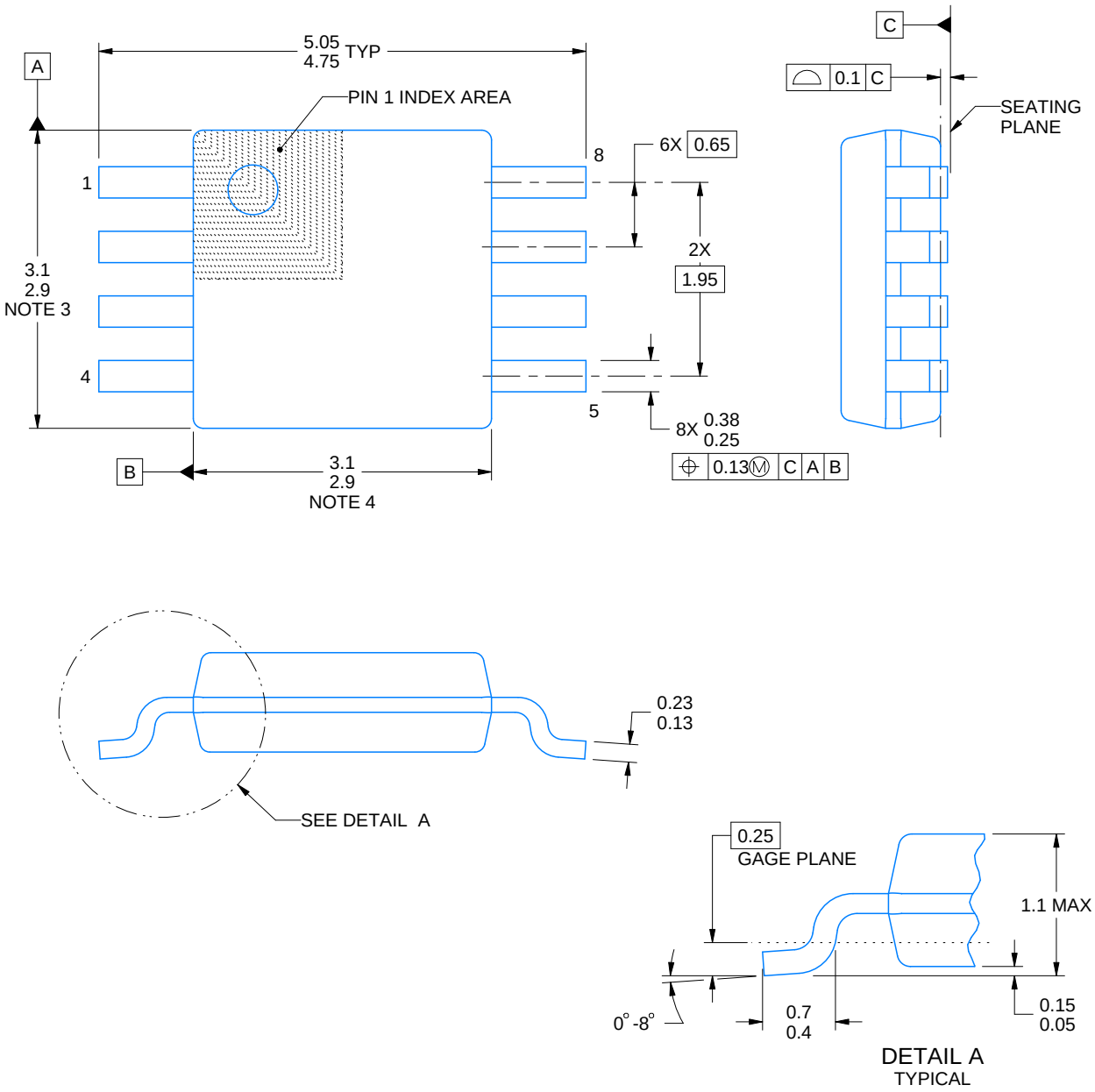
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
RC4580IP	P	PDIP	8	50	506	13.97	11230	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

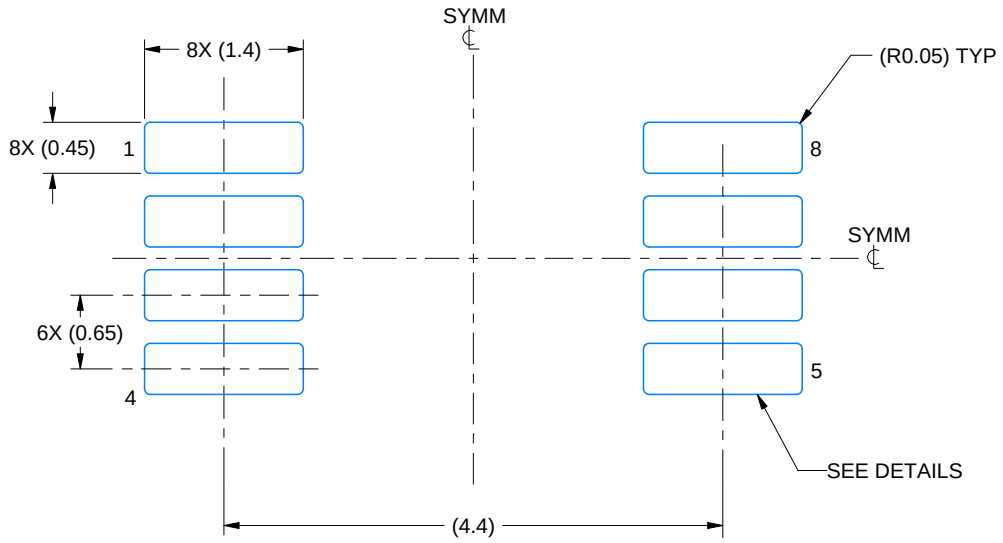
SMALL OUTLINE PACKAGE



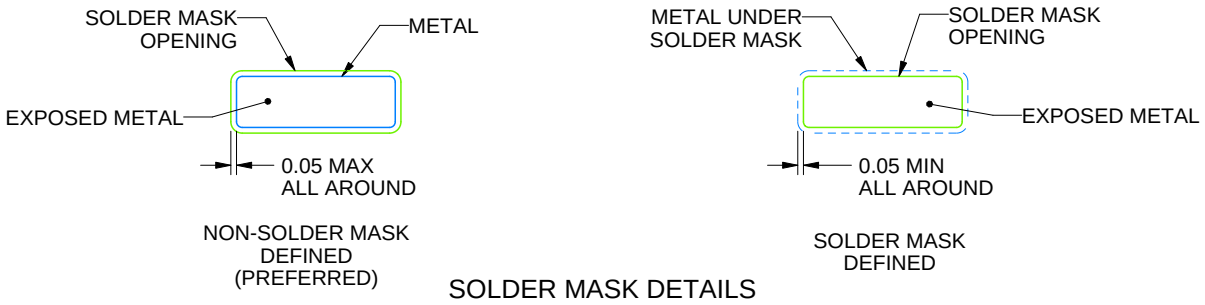
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

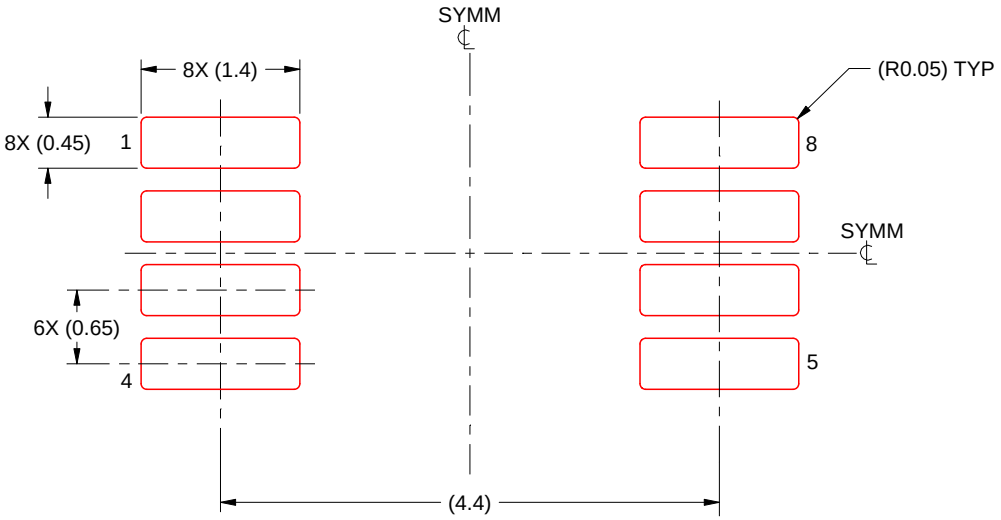


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

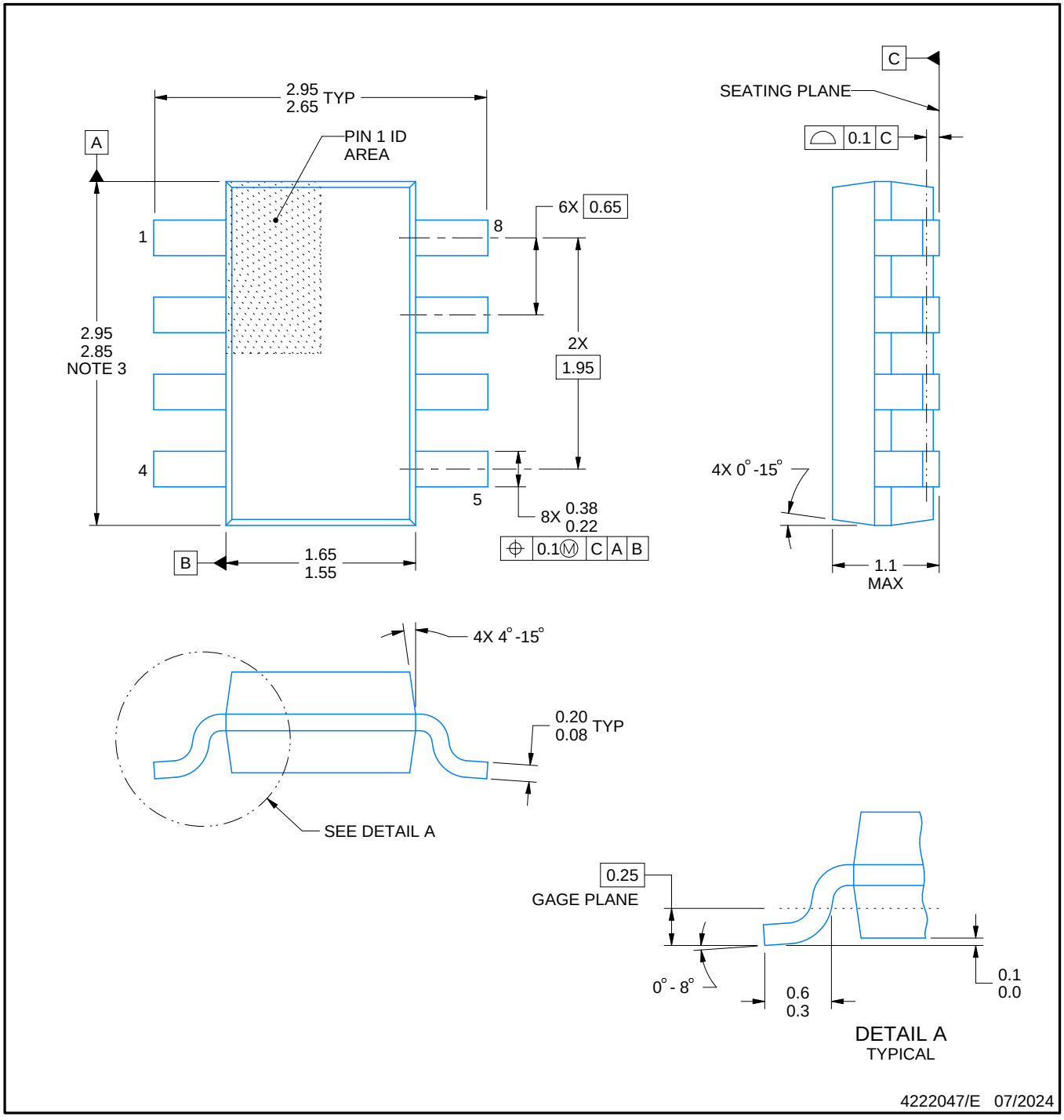
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

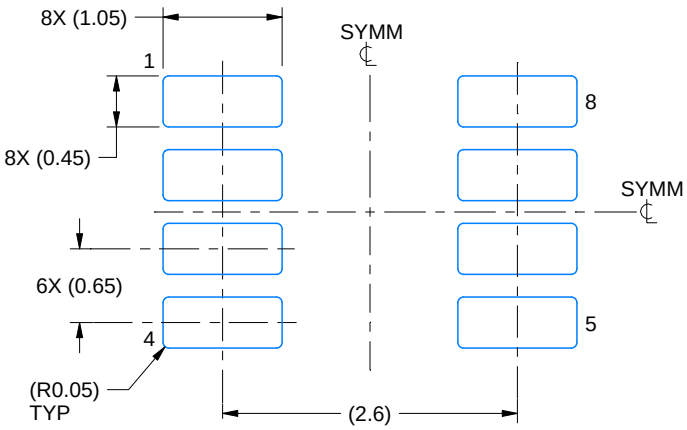
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

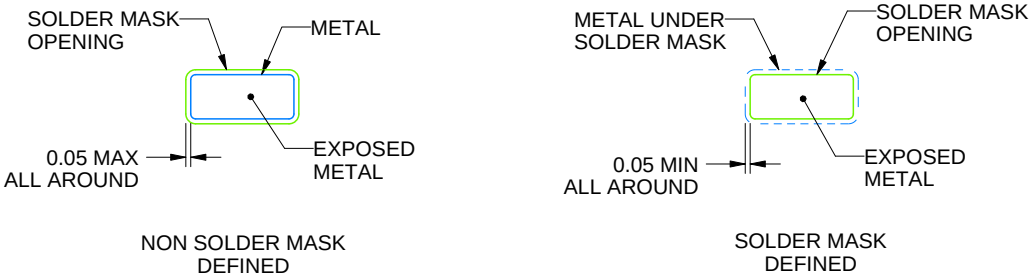


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

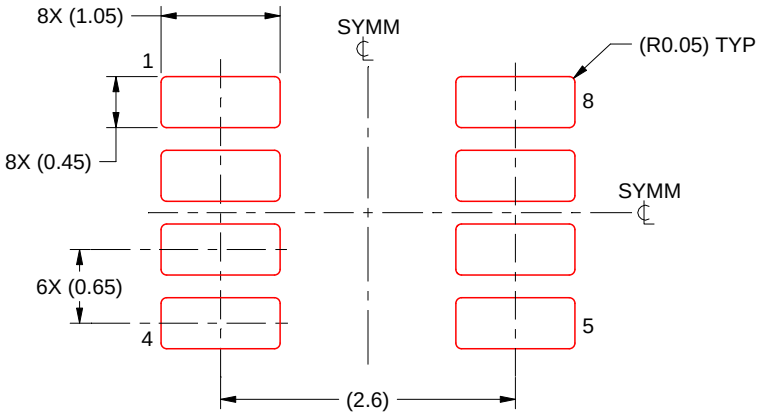
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

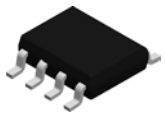


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

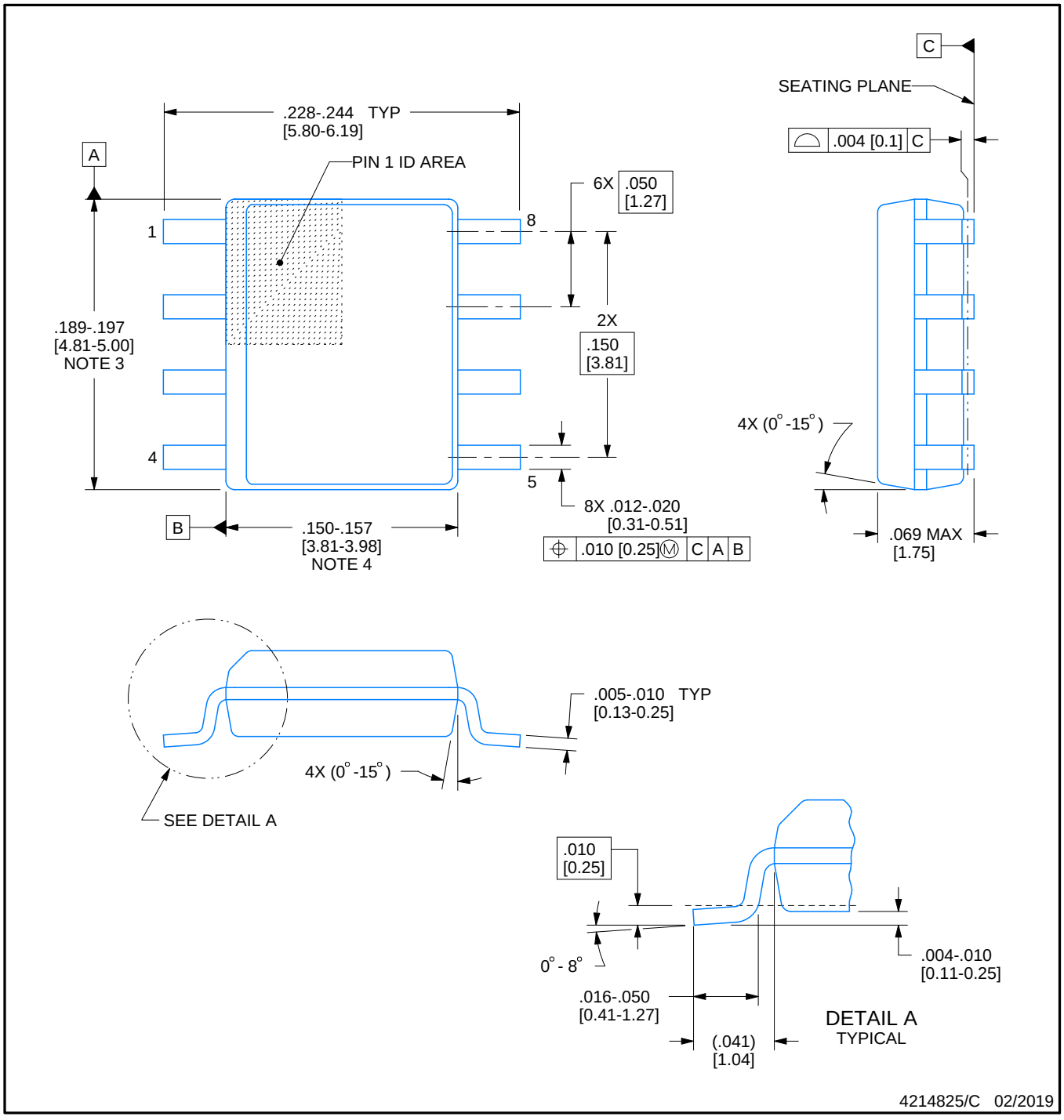


PACKAGE OUTLINE

D0008A

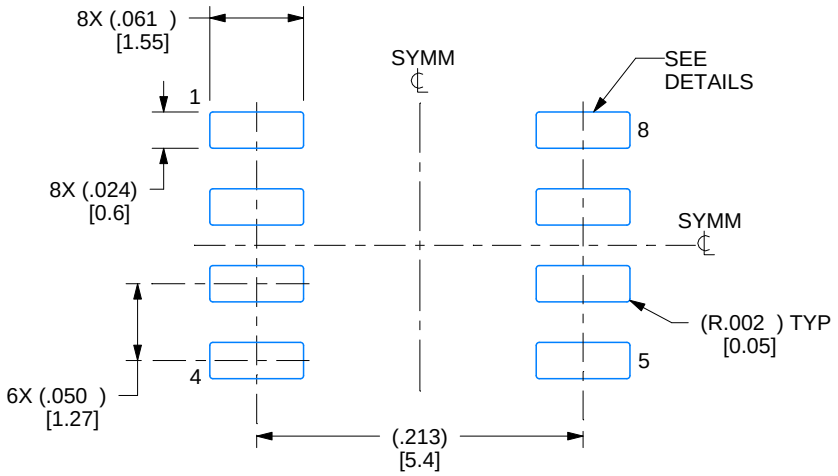
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

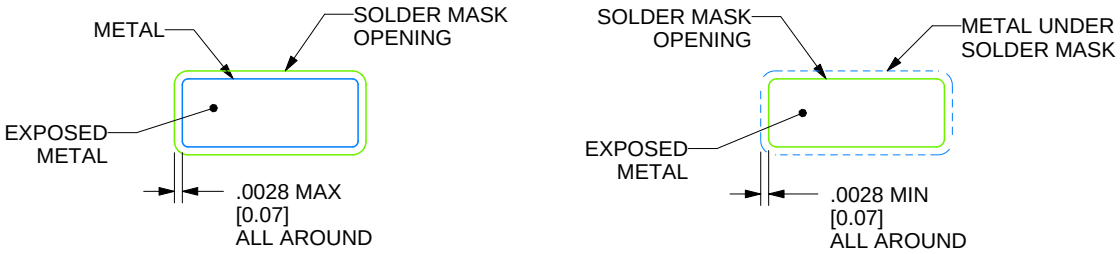


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

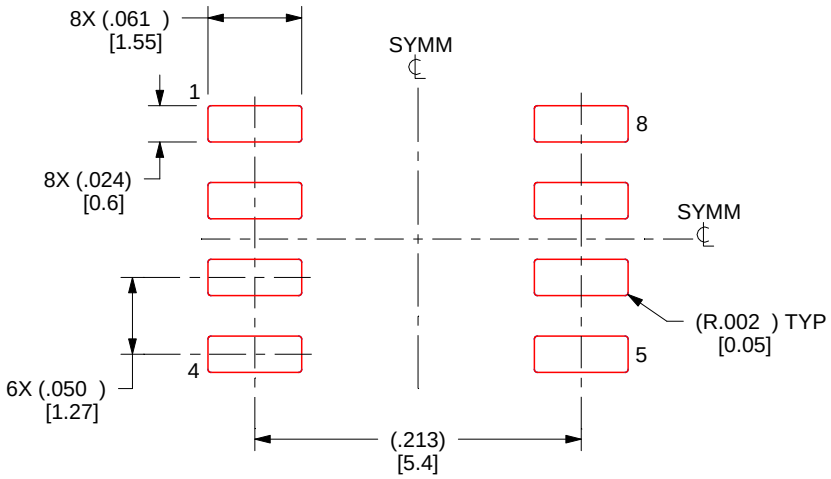
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



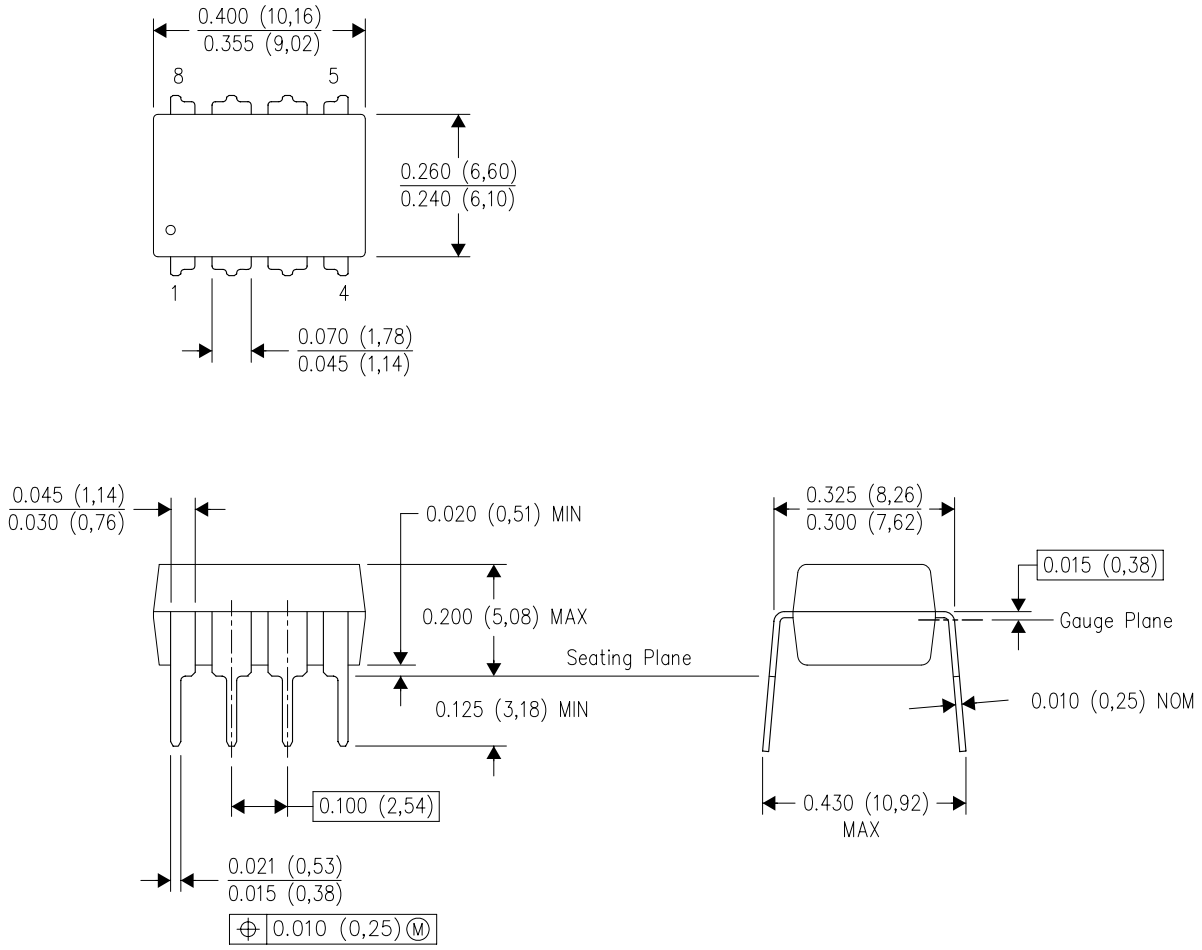
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



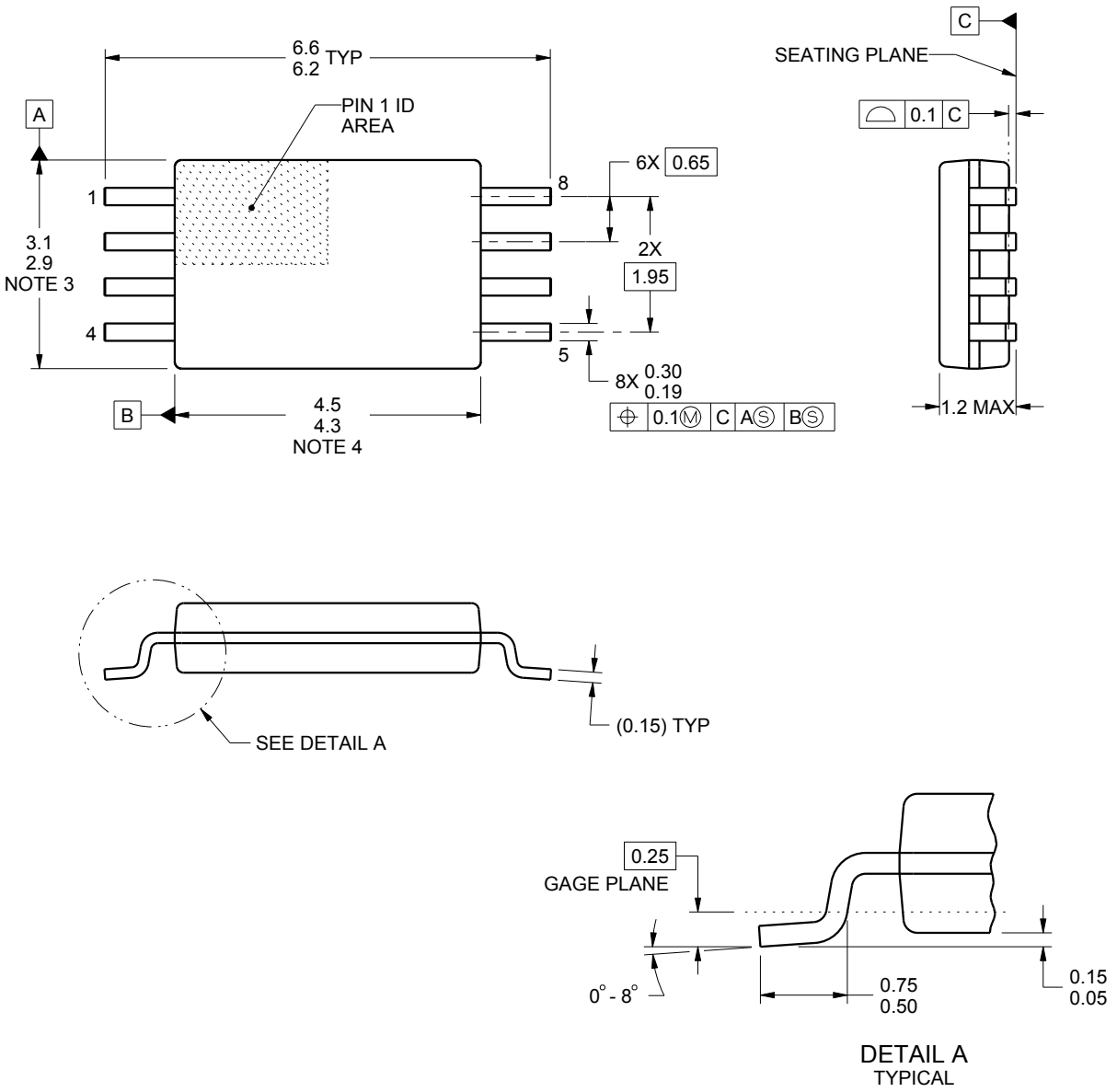
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

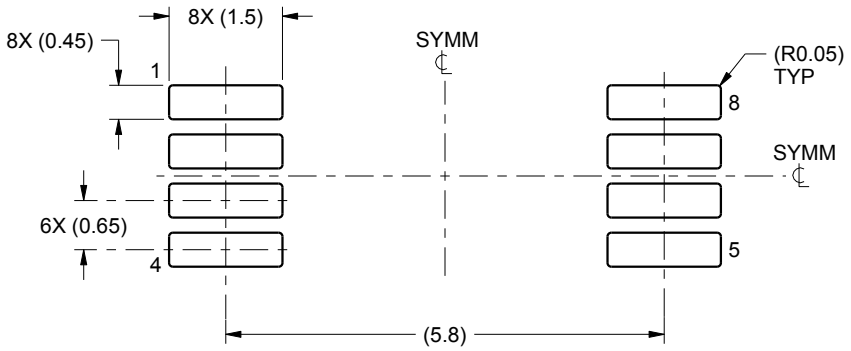
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

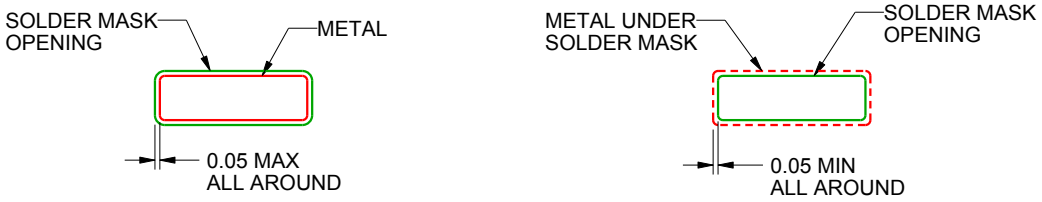


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

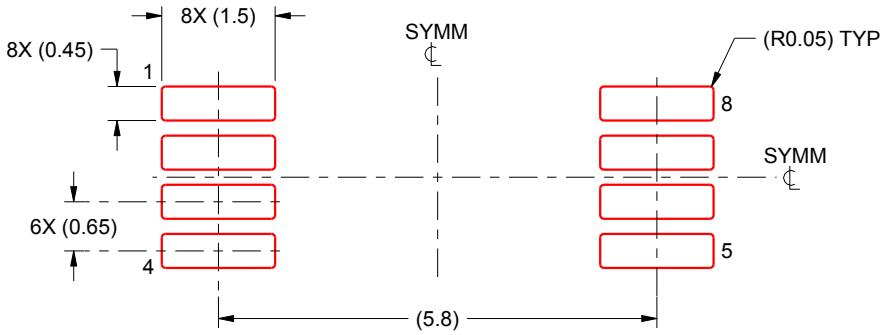


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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