TEXAS INSTRUMENTS
PCA9543A
JAJSLF7B – SEPTEMBER 2007 – REVISED MARCH 2021

PCA9543A 2 チャネル I²C バス・スイッチ、割り込みロジックおよびリセット付き

1 特長

- 1 対 2 の双方向変換スイッチ
- I²C バスおよび SMBus 互換
- 2 つのアクティブ LOW 割り込み入力
- アクティブ LOW 割り込み出力
- アクティブ LOW のリセット入力
- 2 本のアドレス・ピンにより、最大 4 個の PCA9543A を I²C バスに接続可能
- I²C バス経由で、任意の組み合わせのチャネルを選択可能
- 電源オン時は、すべてのスイッチ・チャネルが選択解除された状態
- 低い R_{ON} のスイッチ
- 1.8V、2.5V、3.3V、5V の各電圧のバス間での電圧レベル変換
- 電源オン時のグリッチなし
- 活線挿抜をサポート
- 低スタンバイ電流
- 2.3V～5.5V の動作電源電圧範囲
- 5.5V 許容の入力
- 0～400kHz のクロック周波数
- JESD 78 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、荷電デバイス・モデル (C101)

2 アプリケーション

- サーバー
- ルーター (テレコム・スイッチング機器)
- ファクトリ・オートメーション
- I²C スレーブ・アドレス競合がある製品 (複数の同一温度センサなど)

3 概要

PCA9543A は、I²C バスで制御されるデュアル双方向変換スイッチです。SCL/SDA 上流ペアが、2 つの下流ペア (チャネル) に展開されます。プログラム可能な制御レジスタの設定により、個々の SCn/SDn チャネルまたは両方のチャネルを選択できます。2 つの割り込み入力 ($\overline{INT1}$～$\overline{INT0}$、各下流ペアに 1 つ) を備えています。1 つの割り込み出力 ($\overline{INT}$) が 2 つの割り込み入力の論理積として機能します。

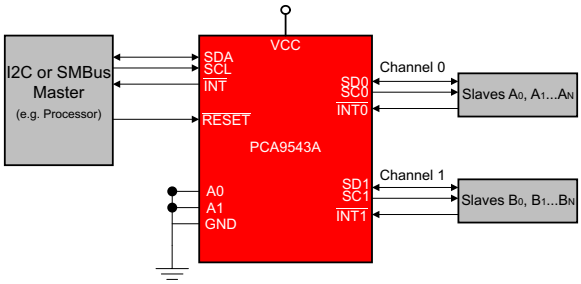
アクティブ LOW のリセット入力 ($\overline{RESET}$) により、PCA9543A は下流の I²C バスの 1 つが LOW 状態に固着した状況から回復できます。$\overline{RESET}$ を LOW にすると、I²C ステート・マシンがリセットされ、両方のチャネルが選択解除されます (内部のパワー・オン・リセット機能と同様)。

スイッチのパス・ゲートは、PCA9543A が出力する最大 HIGH 電圧を VCC ピンで制限できるように構成されています。これによって、ペアごとに異なるバス電圧を使用できるため、1.8V、2.5V、3.3V の部品が、追加保護の必要なしに 5V の部品と通信を行えます。外付けのプルアップ抵抗により、各チャネルに求められる電圧レベルにバスをプルアップします。すべての I/O ピンは 5.5V 許容です。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
PCA9543	TSSOP (14)	5.00mm × 4.40mm
	SOIC (14)	8.65mm × 3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略図

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- Deleted Package thermal impedance from the *Absolute Maximum Ratings* ... 4
- Moved the "Storage temperature range" to the *Absolute Maximum Ratings* ... 4
- Changed the PW package values in the *Thermal Information* ... 5
- Added D package values to the *Thermal Information* ... 5
- Changed the V_{PORR} row in the *Electrical Characteristics* ... 5
- Added V_{PORF} row to the *Electrical Characteristics* ... 5
- Changed the I_{CC} Low inputs and High inputs values in the *Electrical Characteristics* ... 5
- Changed the C_i SCL values in the *Electrical Characteristics* ... 5
- Changed the R_{on} (4.5 V to 5.5 V) TYP value From: 9 Ω To: 10 Ω in the *Electrical Characteristics* ... 5
- Changed the R_{on} (3 V to 3.6 V) TYP value From: 11 Ω To: 13 Ω in the *Electrical Characteristics* ... 5
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5 Pin Configuration and Functions

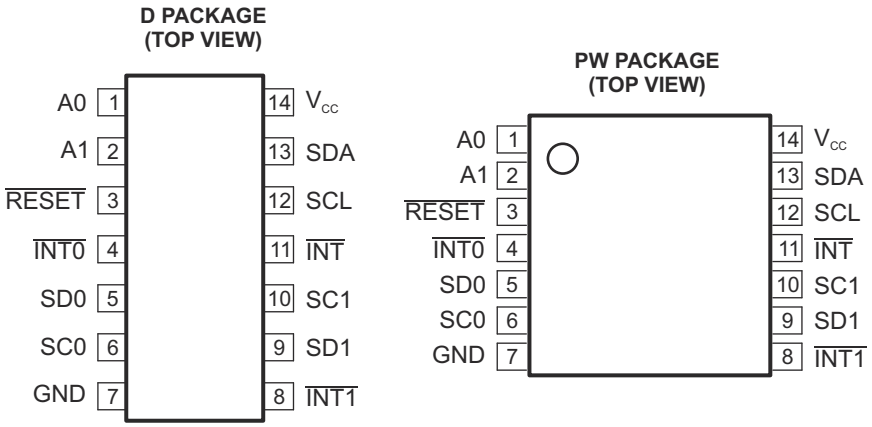


表 5-1. Pin Functions

PIN		DESCRIPTION
NAME	D, PW	
A0	1	Address input 0. Connect directly to V_{CC} or ground.
A1	2	Address input 1. Connect directly to V_{CC} or ground.
$\overline{\text{RESET}}$	3	Active-low reset input. Connect to V_{CC} or V_{DPUM} (1) through a pull-up resistor, if not used.
$\overline{\text{INT0}}$	4	Active-low interrupt input 0. Connect to V_{DPU0} (1) through a pull-up resistor.
SD0	5	Serial data 0. Connect to V_{DPU0} (1) through a pull-up resistor.
SC0	6	Serial clock 0. Connect to aV_{DPU0} (1) through a pull-up resistor.
GND	7	Ground
$\overline{\text{INT1}}$	8	Active-low interrupt input 1. Connect to V_{DPU1} (1) through a pull-up resistor.
SD1	9	Serial data 1. Connect to V_{DPU1} (1) through a pull-up resistor.
SC1	10	Serial clock 1. Connect to V_{DPU1} (1) through a pull-up resistor.
$\overline{\text{INT}}$	11	Active-low interrupt output. Connect to V_{DPUM} (1) through a pull-up resistor.
SCL	12	Serial clock line. Connect to V_{DPUM} (1) through a pull-up resistor.
SDA	13	Serial data line. Connect to V_{DPUM} (1) through a pull-up resistor.
VCC	14	Supply power

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C reference voltage while V_{DPU0} and V_{DPU1} are the slave channel reference voltages.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I	Input voltage range(2)	–0.5	7	V
I_I	Input current		±20	mA
I_O	Output current		±25	mA
	Continuous current through V_{CC}		±100	mA
	Continuous current through GND		±100	mA
P_{tot}	Total power dissipation		400	mW
T_A	Operating free-air temperature range	–40	85	°C
T_{stg}	Storage temperature range	–60	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA		0.7 × V_{CC}	6	V
		A1, A0, $\overline{INT1}$, $\overline{INT0}$, $\overline{RESET}$	V_{CC} = 2.3 V to 3.6 V	0.7 × V_{CC}	V_{CC} + 0.5	
			V_{CC} = 3.6 V to 4.5 V	0.7 × V_{CC}	V_{CC} + 0.5	
			V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	V_{CC} + 0.5	
V_{IL}	Low-level input voltage	SCL, SDA		–0.5	0.3 × V_{CC}	V
		A1, A0, $\overline{INT1}$, $\overline{INT0}$, $\overline{RESET}$		–0.5	0.3 × V_{CC}	
T_A	Operating free-air temperature			–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		PCA9543A PW (TSSOP) 14 PINS	PCA9543A D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130.1	102.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	59.2	63.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	73.1	57.1	
ψ_{JT}	Junction-to-top characterization parameter	11.7	26.7	
ψ_{JB}	Junction-to-board characterization parameter	72.5	56.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{PORR}	Power-on reset voltage, V_{CC} rising	No load: $V_I = V_{CC}$ or GND(2)			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	No load: $V_I = V_{CC}$ or GND(2)		0.8	1		V
V_{pass}	Switch output voltage	$V_{SWin} = V_{CC}$, $I_{SWout} = -100$ µA	5 V		3.6		V
			4.5 V to 5.5 V	2.6		4.5	
			3.3 V		1.9		
			3 V to 3.6 V	1.6		2.8	
			2.5 V		1.5		
			2.3 V to 2.7 V	1.1		2	
I_{OH}	$\overline{INT}$	$V_O = V_{CC}$	2.3 V to 5.5 V			100	µA
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	7		mA
		V_{OL} = 0.6 V		6	10		
	$\overline{INT}$	V_{OL} = 0.4 V		3			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V	–1		1	µA
	SC1–SC0, SD1–SD0	$V_I = V_{CC}$ or GND	2.3 V to 3.6 V	–1		1	
			4.5 V to 5.5 V	–1		100	
	A1, A0	$V_I = V_{CC}$ or GND	2.3 V to 3.6 V	–1		1	
			4.5 V to 5.5 V	–1		50	
	$\overline{INT1}$– $\overline{INT0}$	$V_I = V_{CC}$ or GND	2.3 V to 3.6 V	–1		1	
			4.5 V to 5.5 V	–1		50	
	$\overline{RESET}$	$V_I = V_{CC}$ or GND	2.3 V to 3.6 V	–1		1	
			4.5 V to 5.5 V	–1		50	

6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{CC}	Operating mode	f_{SCL} = 100 kHz	V_I = V_{CC} or GND, I_O = 0	5.5 V		17	50	μA
				3.6 V		6	20	
				2.7 V		3	16	
	Standby mode	Low inputs	V_I = GND, I_O = 0	5.5 V		1.6	2	
				3.6 V		1	1.3	
				2.7 V		0.7	1.1	
		High inputs	V_I = V_{CC}, I_O = 0	5.5 V		1.6	2	
				3.6 V		1	1.3	
				2.7 V		0.7	1.1	
ΔI_{CC}	Supply-current change	$\overline{INT1}$– $\overline{INT0}$	One $\overline{INT1}$– $\overline{INT0}$ input at 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V		8	20	μA
			One $\overline{INT1}$– $\overline{INT0}$ input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			8	20	
		SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND			8	20	
			SCL or SDA input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			8	20	
C_i	A1, A0		V_I = V_{CC} or GND	2.3 V to 3.6 V		4	5	pF
				4.5 V to 5.5 V		4	5	
	$\overline{INT1}$– $\overline{INT0}$		V_I = V_{CC} or GND	2.3 V to 3.6 V		4	6	
				4.5 V to 5.5 V		4	6	
	$\overline{RESET}$		V_I = V_{CC} or GND	2.3 V to 3.6 V		4	5	
				4.5 V to 5.5 V		4	5	
	SCL		V_I = V_{CC} or GND	2.3 V to 5.5 V		15	19	
$C_{i\ o(OFF)}$ (3)	SDA		V_I = V_{CC} or GND, Switch OFF	2.3 V to 5.5 V		15	19	pF
	SC1–SC0, SD1–SD0					6	8	
R_{on}	Switch on-state resistance		V_O = 0.4 V, I_O = 15 mA	4.5 V to 5.5 V	4	10	20	Ω
				3 V to 3.6 V	5	13	25	
			V_O = 0.4 V, I_O = 10 mA	2.3 V to 2.7 V	7	16	50	

(1) For operation between published voltage ranges, refer to the worst-case parameter in both ranges.
(2) To reset the part, either $\overline{RESET}$ must be low or V_{CC} must be lowered to 0.2 V.
(3) $C_{io(ON)}$ depends on the device capacitance and load that is downstream from the device.

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0(1)		0(1)		µs
t_{icr}	I²C input rise time			1000	20 + 0.1C_b (2)	300	ns
t_{icf}	I²C input fall time			300	20 + 0.1C_b (2)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	20 + 0.1C_b (2)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vdL(Data)}$	Valid-data time (high to low)(3)	SCL low to SDA output low valid		1		1	µs
$t_{vdH(Data)}$	Valid-data time (low to high)(3)	SCL low to SDA output high valid		0.6		0.6	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1		1	µs
C_b	I²C bus capacitive load			400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
(2) C_b = total bus capacitance of one bus line in pF
(3) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see 図 7-1)

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see 図 7-3)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd} (1)	Propagation delay time	R_{ON} = 20 Ω, C_L = 15 pF	SDA or SCL	SDn or SCn		0.3	ns
		R_{ON} = 20 Ω, C_L = 50 pF				1	
t_{iv}	Interrupt valid time(2)		$\overline{INTn}$	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time(2)		$\overline{INTn}$	$\overline{INT}$		2	µs

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) Data taken using a 4.7-kΩ pull-up resistor and 100-pF load (see 図 7-3)

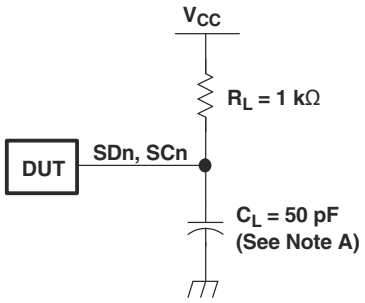
6.8 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-3)

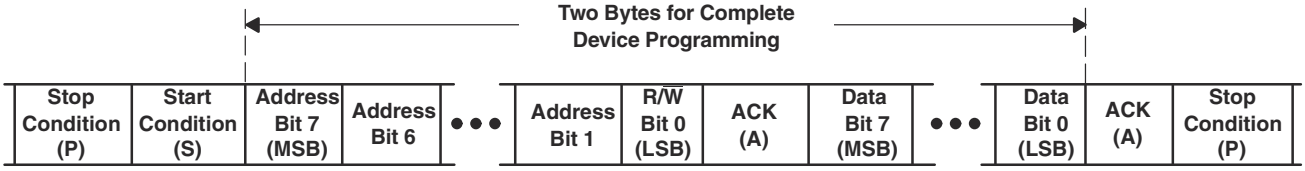
PARAMETER		MIN	MAX	UNIT
t_{PWRL}	Required low-level pulse duration of $\overline{INTn}$ inputs(2)	1		µs
t_{PWRH}	Required high-level pulse duration of $\overline{INTn}$ inputs(2)	0.5		µs
t_{WL}	Pulse duration, $\overline{RESET}$ low	4		ns
t_{rst} (1)	$\overline{RESET}$ time (SDA clear)		500	ns
t_{REC}	Recovery time from $\overline{RESET}$ to start	0		ns

(1) t_{rst} is the propagation delay measured from the time the $\overline{RESET}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.
(2) The device has interrupt input rejection circuitry for pulses less than the listed minimum.

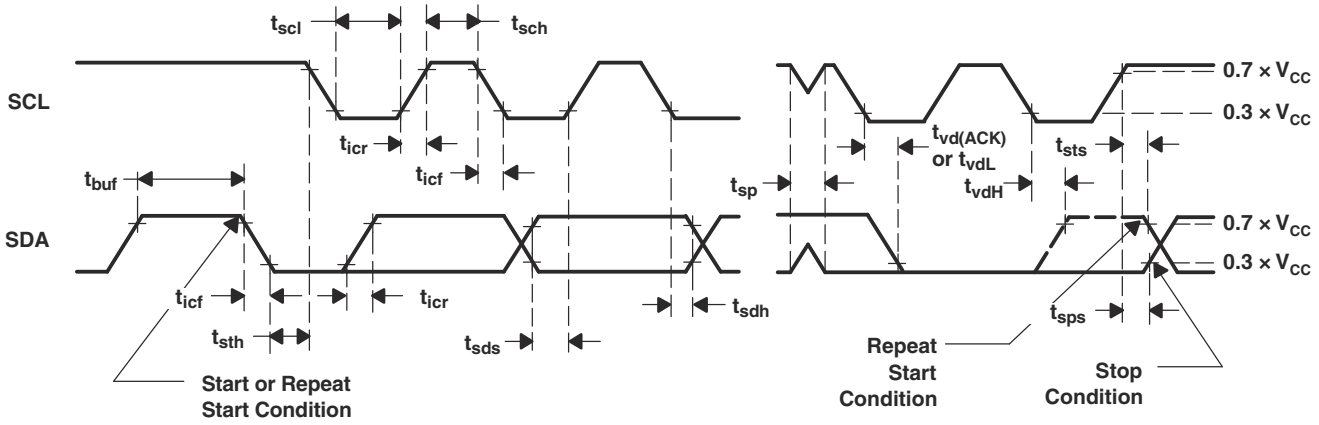
7 Parameter Measurement Information



I²C PORT LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I²C address + R/W
2	Control register data



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

図 7-1. I²C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

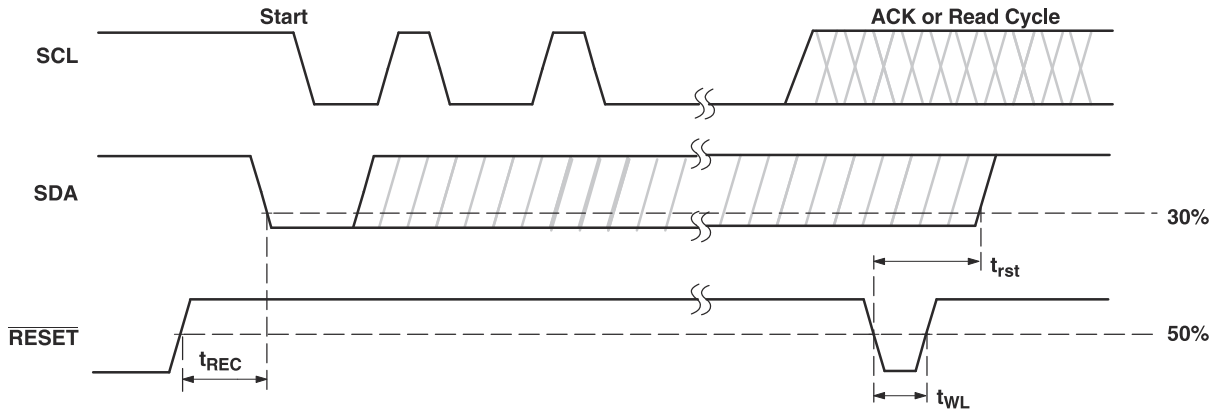
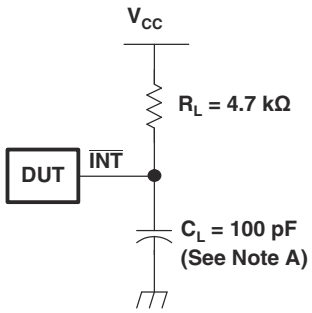
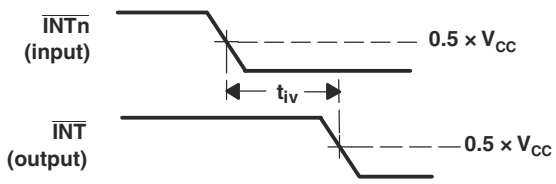


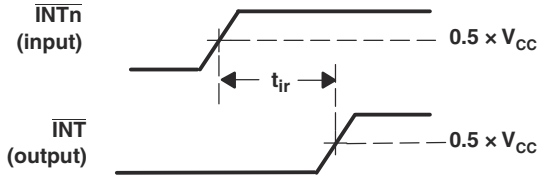
図 7-2. Reset Timing



INTERRUPT LOAD CONFIGURATION



VOLTAGE WAVEFORMS (t_{iv})



VOLTAGE WAVEFORMS (t_{ir})

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

図 7-3. Interrupt Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

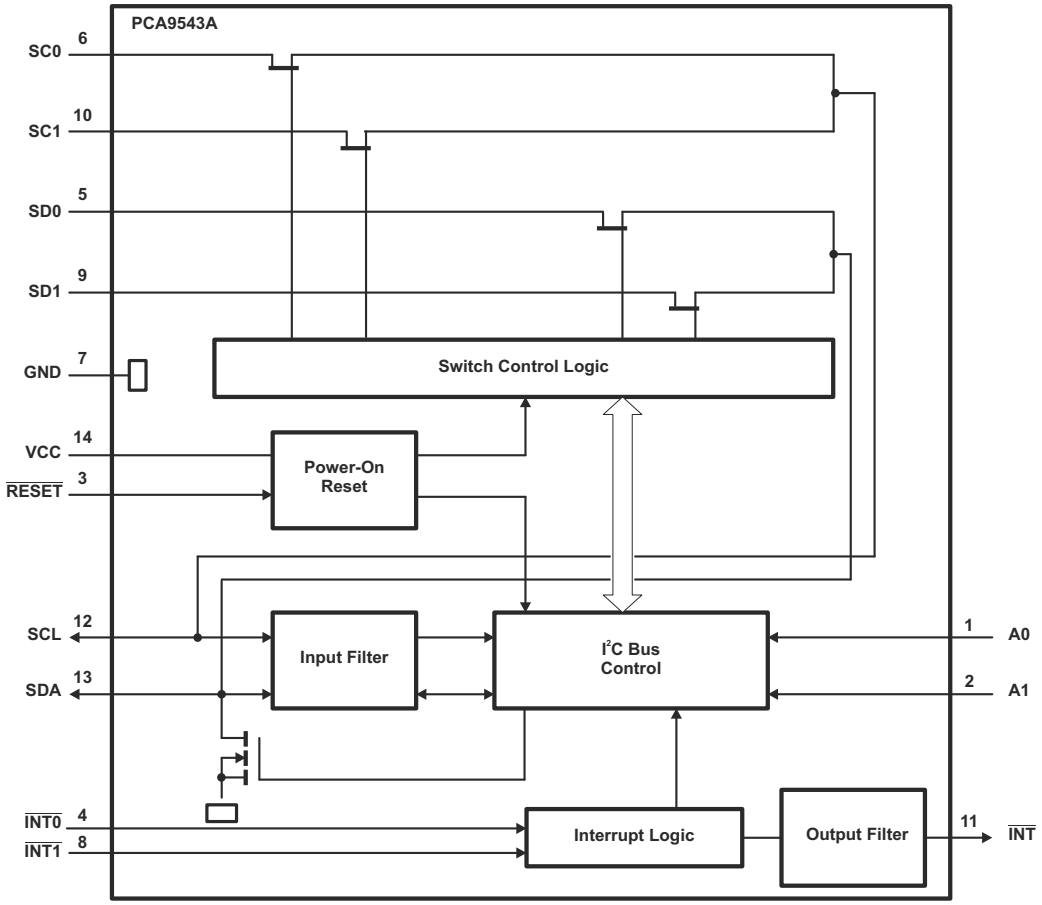
The PCA9543A is a 2-channel, bidirectional translating I^2C switch. The master SCL/SDA signal pair is directed to two channels of slave devices, SC0/SD0-SC1/SD1. Either individual downstream channel can be selected as well as both channels. The PCA9543A also supports interrupt signals in order for the master to detect an interrupt on the $\overline{INT}$ output pin that can result from any of the slave devices connected to the $\overline{INT1}$- $\overline{INT0}$ input pins.

The device offers an active-low $\overline{RESET}$ input which resets the state machine and allows the PCA9543A to recover should one of the downstream I^2C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR). Either using the $\overline{RESET}$ function or causing a POR will cause both channels to be deselected.

The connections of the I^2C data path are controlled by the same I^2C master device that is switched to communicate with multiple I^2C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 pins), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The PCA9543A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

8.2 Functional Block Diagram



8.3 Feature Description

The PCA9543A is a dual channel bidirectional translating switch for I^2C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The PCA9543A features I^2C control using a single 8-bit control register in which bits 1 and 0 control the enabling and disabling of the two switch channels of I^2C data flow. The PCA9543A also supports interrupt signals for each slave channel and this data is held in bits 5 and 4 of the control register. Depending on the application, voltage translation of the I^2C bus can also be achieved using the PCA9543A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I^2C bus enters a fault state, the PCA9543A can be reset to resume normal operation using the $\overline{\text{RESET}}$ pin feature or by a power-on reset which results from cycling power to the device.

8.4 Device Functional Modes

8.4.1 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input can be used to recover the PCA9543A from a bus-fault condition. The registers and the I^2C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL}. Both channels also are deselected in this case. $\overline{\text{RESET}}$ must be connected to V_{CC} through a pull-up resistor.

8.4.2 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9543A in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9543A registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

8.5 Programming

8.5.1 I^2C Interface

The I^2C bus is for two-way, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time is interpreted as control signals (see 図 8-1).

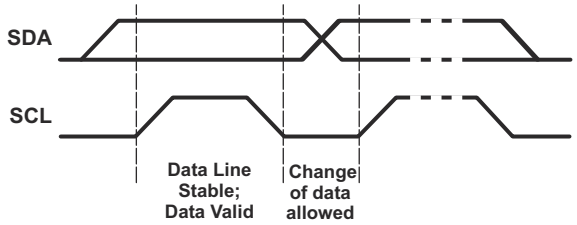


図 8-1. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see 図 8-2).

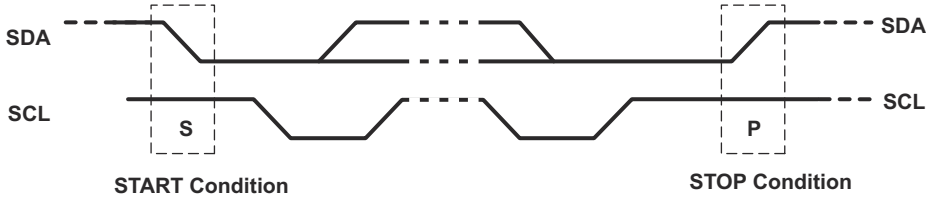


図 8-2. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices that are controlled by the master are the slaves (see 図 8-3).

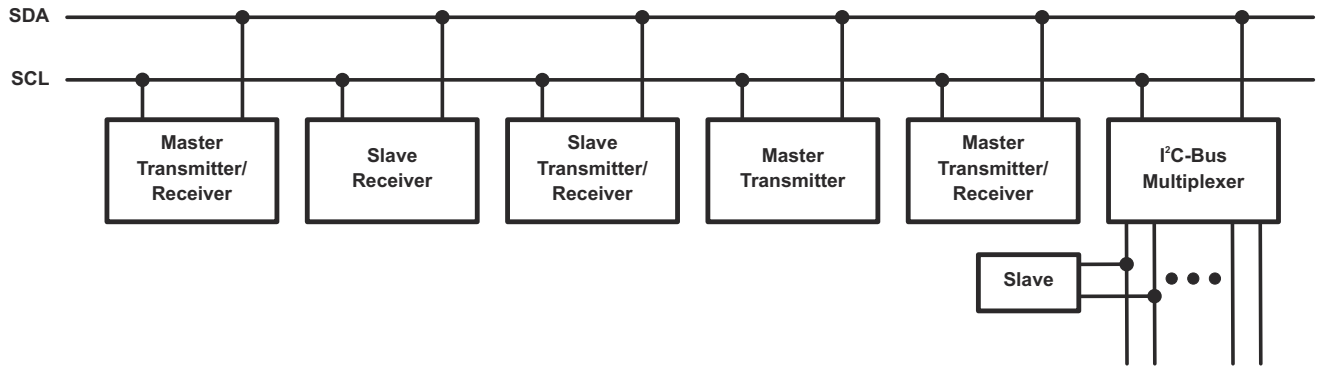


図 8-3. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 図 8-4). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

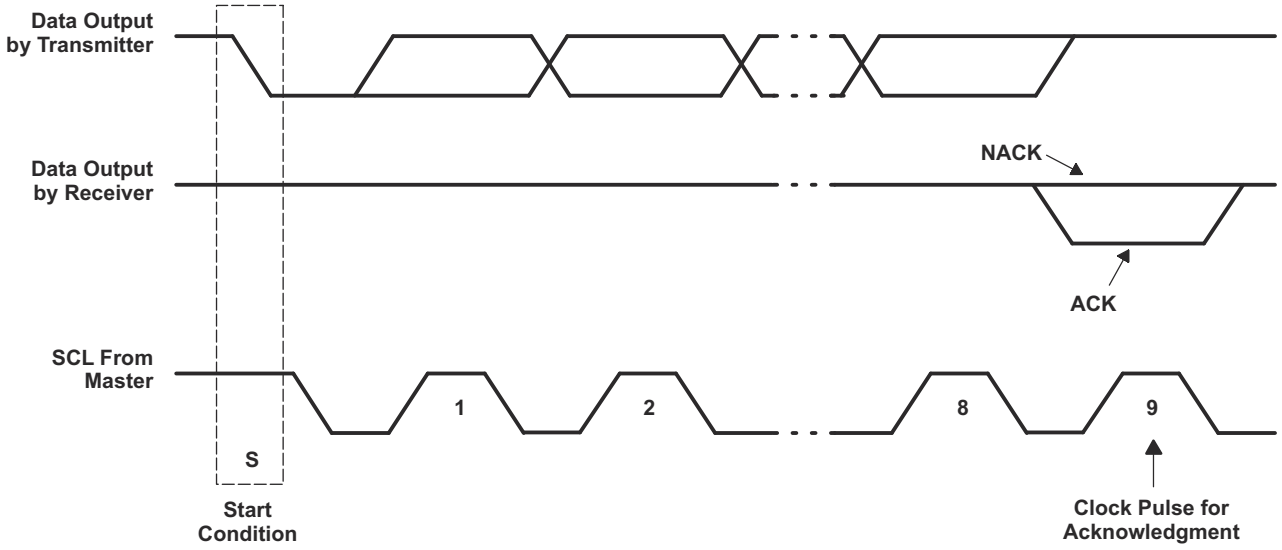


図 8-4. Acknowledgment on I²C Bus

Data is transmitted to the PCA9543A control register using the write mode shown in 図 8-5.

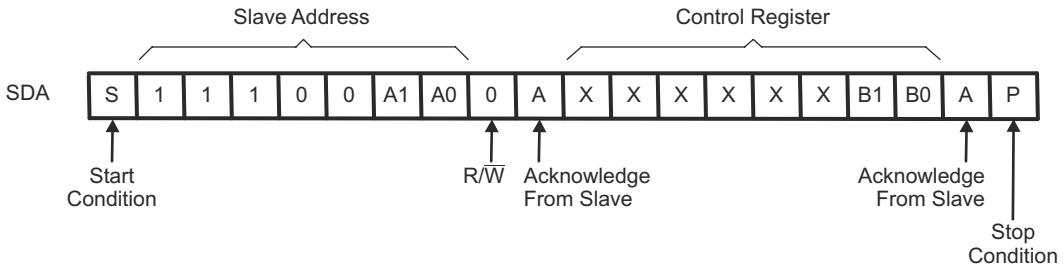


図 8-5. Write Control Register

Data is read from the PCA9543A control register using the read mode shown in 図 8-6.

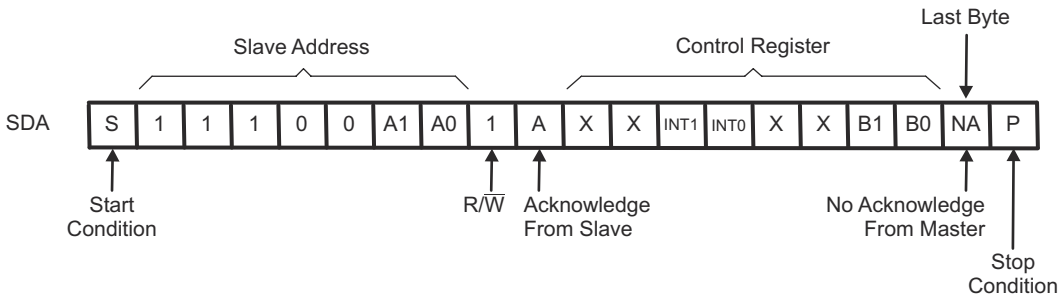


図 8-6. Read Control Register

8.6 Control Register

8.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9543A is shown in 図 8-7. To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address pins and they must be pulled high or low.

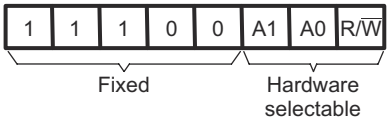


図 8-7. Slave Address PCA9543A

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

8.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9543A, which is stored in the control register (see 図 8-8). If multiple bytes are received by the PCA9543A, it saves the last byte received. This register can be written and read via the I^2C bus.

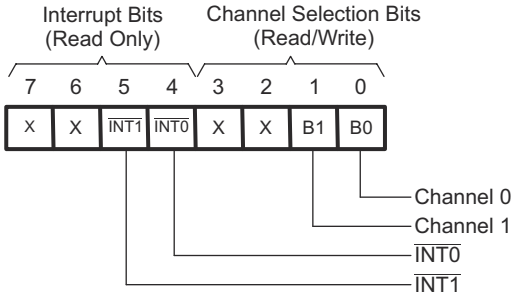


図 8-8. Control Register

8.6.3 Control Register Definition

One or both SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see 表 8-1). After the PCA9543A has been addressed, the control register is written. The two LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

表 8-1. Control Register Write (Channel Selection), Control Register Read (Channel Status)(1)

D7	D6	$\overline{INT1}$	$\overline{INT0}$	D3	D2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

(1) Channel 0 and channel 1 can be enabled at the same time. Care should be taken not to exceed the maximum bus capacitance.

8.6.4 Interrupt Handling

The PCA9543A provides two interrupt inputs (one for each channel) and one open-drain interrupt output (see 表 8-2). When an interrupt is generated by any device, it is detected by the PCA9543A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bit 4 and Bit 5 of the control register correspond to the $\overline{INT0}$ and $\overline{INT1}$ inputs of the PCA9543A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the PCA9543A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the PCA9543A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC} through a pull-up resistor.

表 8-2. Control Register Read (Interrupt)(1)

D7	D6	$\overline{INT1}$	$\overline{INT0}$	D3	D2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

(1) Two interrupts can be active at the same time.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

Applications of the PCA9543A will contain an I^2C (or SMBus) master device and up to two I^2C slave devices. The downstream channels are ideally used to resolve I^2C slave address conflicts. For example, if two identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0 and 1. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and the other channel switched off, the data can be retrieved, and the I^2C master can move on and read the next channel.

In an application where the I^2C bus will contain many additional slave devices that do not result in I^2C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across both channels. If both switches will be enabled simultaneously, additional design requirements must be considered (See *Design Requirements* and *Detailed Design Procedure*).

9.2 Typical Application

A typical application of the PCA9543A will contain anywhere from 1 to 3 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} and V_{DPU1}). In the event where the master device and both slave devices operate at the same voltage, then the pass voltage, V_{pass} = V_{DPUX}. Once the maximum V_{pass} is known, V_{cc} can be selected using 図 9-2. In an application where voltage translation is necessary, additional design requirements must be considered (See *Design Requirements*).

図 9-1 shows an application in which the PCA9543A can be used.

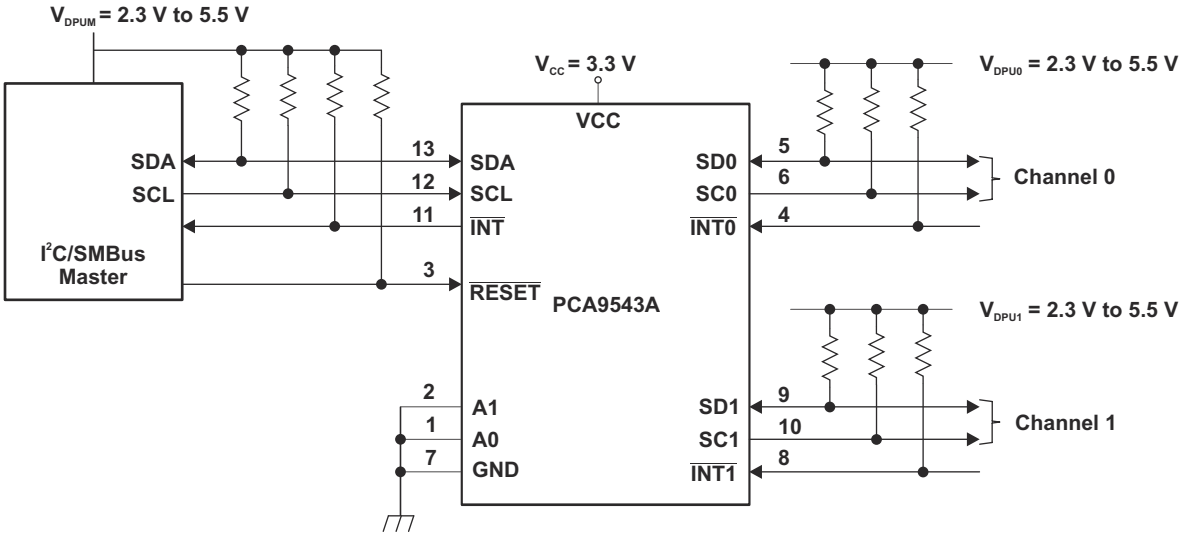


図 9-1. Typical Application

9.2.1 Design Requirements

The pull-up resistors on the $\overline{INT1}$- $\overline{INT0}$ pins in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

The A0 and A1 pins are hardware selectable to control the slave address of the PCA9543A. These pins may be tied directly to GND or V_{CC} in the application.

If both slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p.

The pass-gate transistors of the PCA9543A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

図 9-2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the *Electrical Characteristics* section of this data sheet). In order for the PCA9543A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in 図 9-2, $V_{pass(max)}$ is 2.7 V when the PCA9543A supply voltage is 4 V or lower, so the PCA9543A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see 図 9-1).

9.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9543A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If both channels will be activated simultaneously, each of the slaves on both channels will contribute to total bus capacitance.

9.2.3 Application Curves

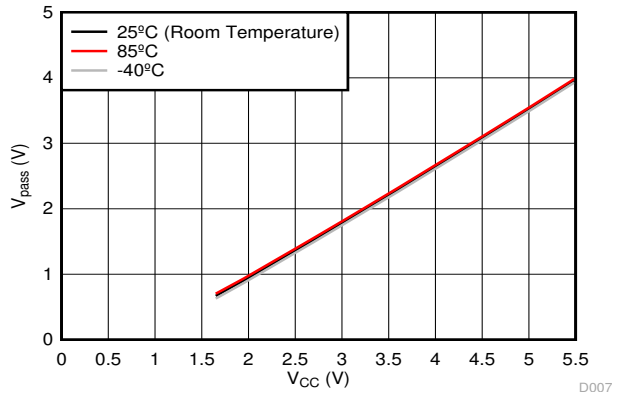
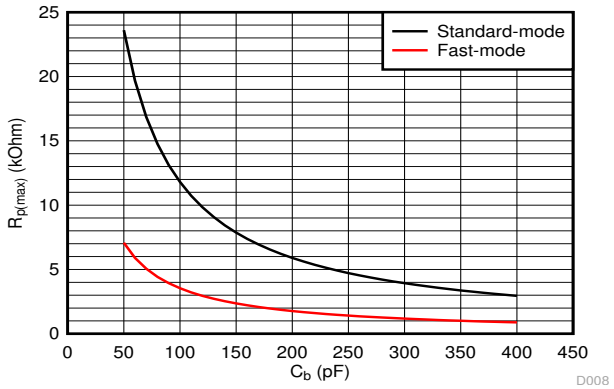
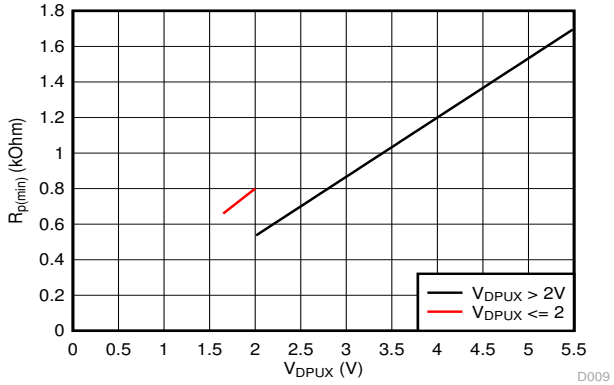


図 9-2. Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points



A. Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs) Fast-mode (f_{SCL}= 400 kHz, t_r= 300 ns)

図 9-3. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



A. V_{OL} = 0.2*V_{DPUX}, I_{OL} = 2 mA when V_{DPUX} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

図 9-4. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{DPUX})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9543A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 図 10-1 and 図 10-2.

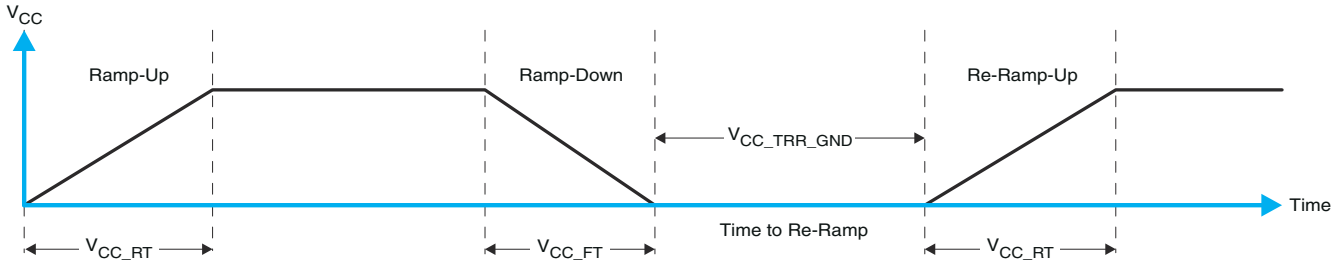


図 10-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

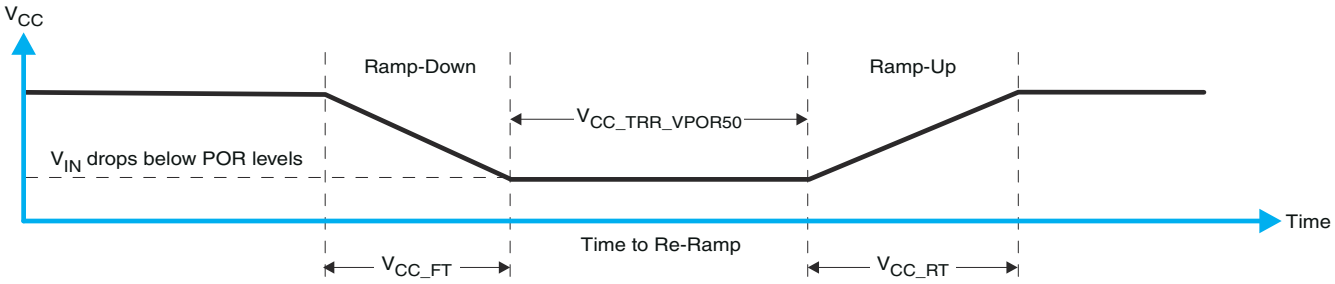


図 10-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

表 10-1 specifies the performance of the power-on reset feature for PCA9543A for both types of power-on reset.

表 10-1. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 図 10-1	1		100	ms
V_{CC_RT}	Rise rate	See 図 10-1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 図 10-1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 図 10-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See 図 10-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 図 10-3				µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 図 10-3 and 表 10-1 provide more information on how to measure these specifications.

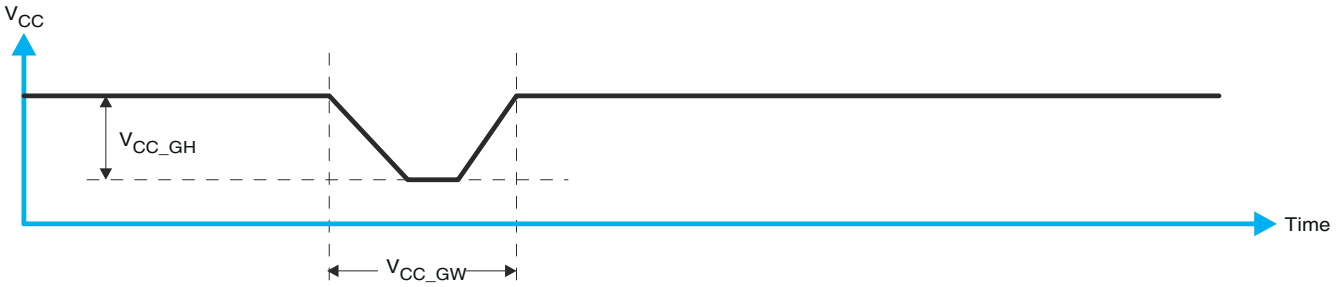


図 10-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 図 10-4 and 表 10-1 provide more details on this specification.

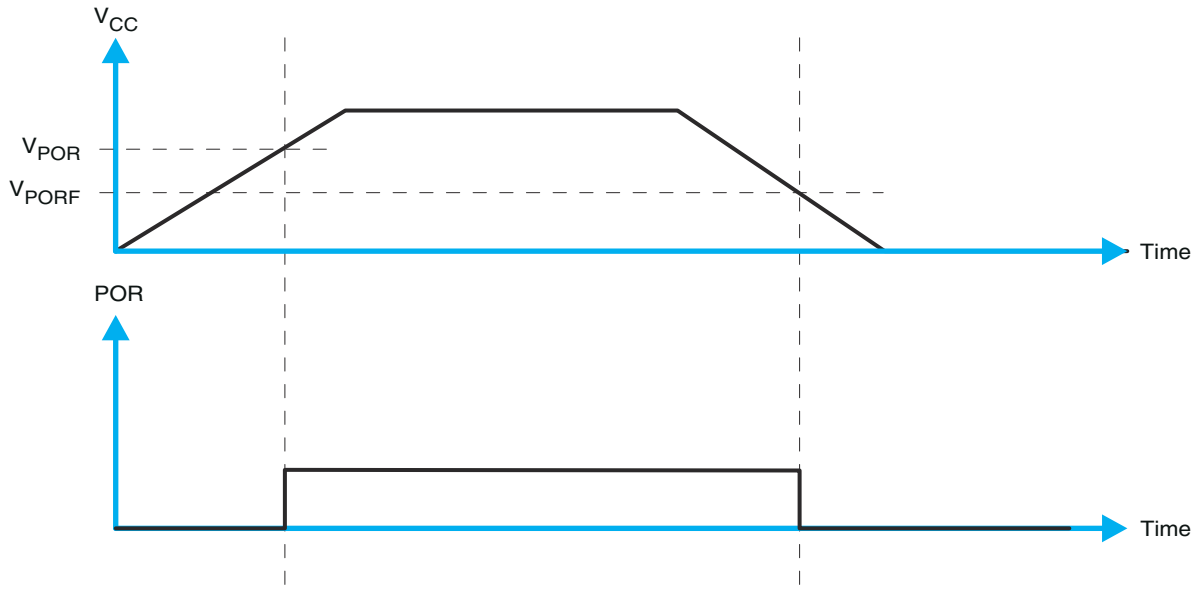


図 10-4. V_{POR}

11 Layout

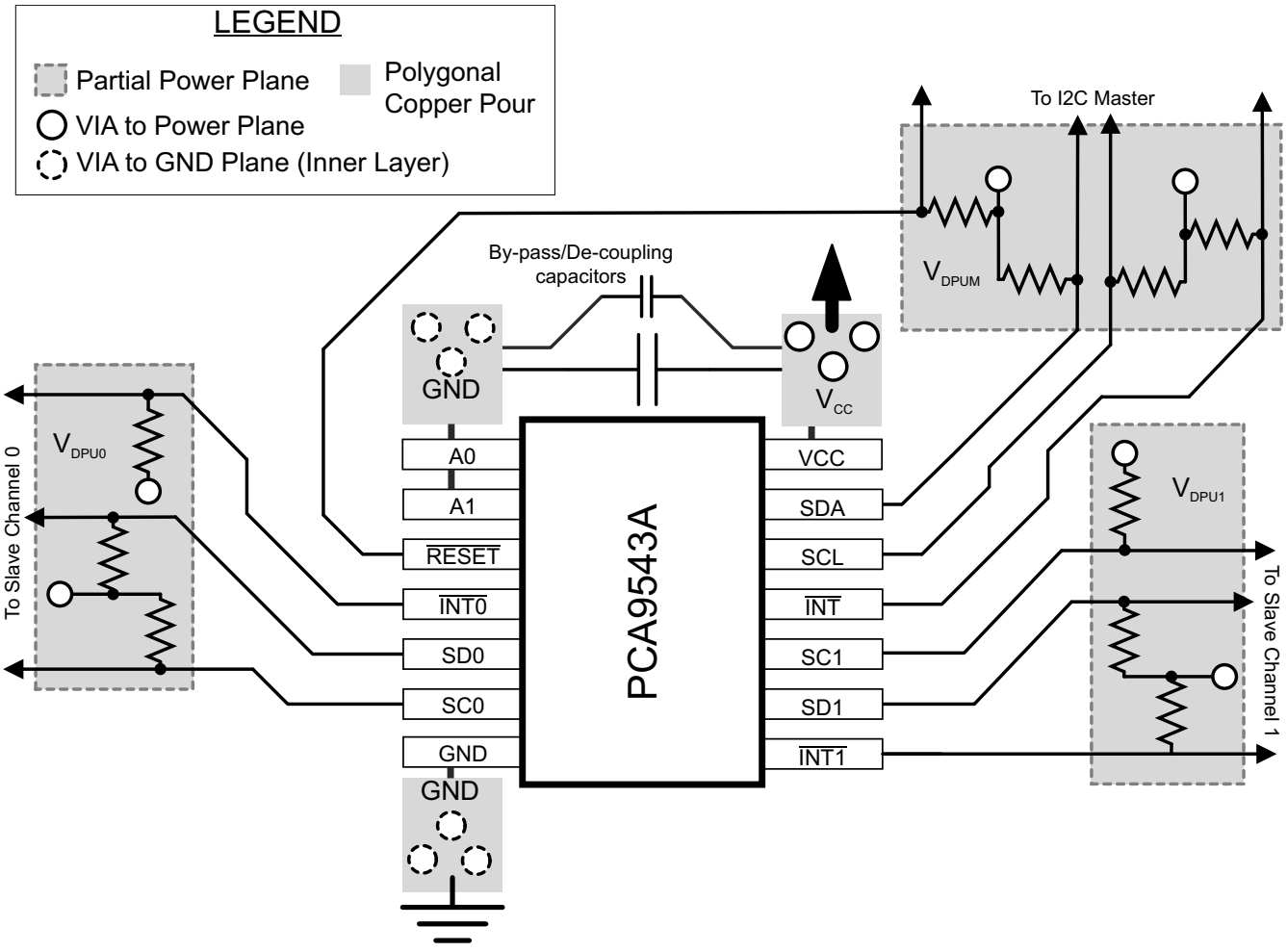
11.1 Layout Guidelines

For PCB layout of the PCA9543A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane can connect all of the pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}, and V_{DPU1}, may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I^2C bus capacitance added by PCB parasitics, data lines (SCn, SDn and $\overline{INTn}$) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

11.2 Layout Example



12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報の 1 週間分のダイジェストを受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、検証済みの迅速な回答と設計支援をエンジニアがエキスパートから直接得るための頼れる情報源です。既存の回答を検索し、または新たに質問することで、必要とする設計支援を迅速に得ることができます。

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9543AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	PCA9543A	
PCA9543ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9543A	Samples
PCA9543APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	PD543A	
PCA9543APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD543A	Samples
PCA9543APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD543A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

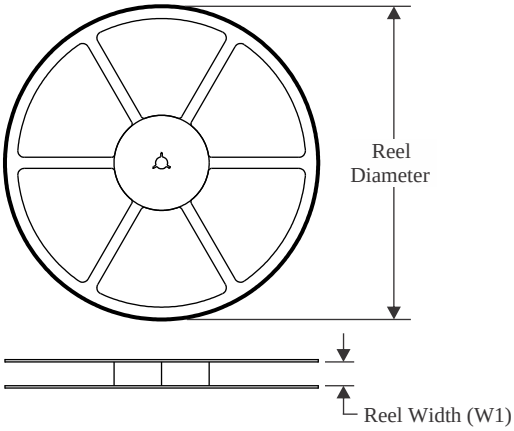
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

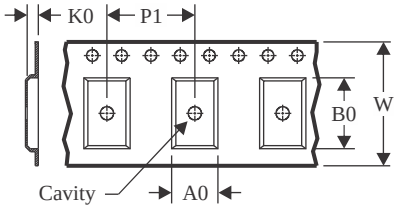
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

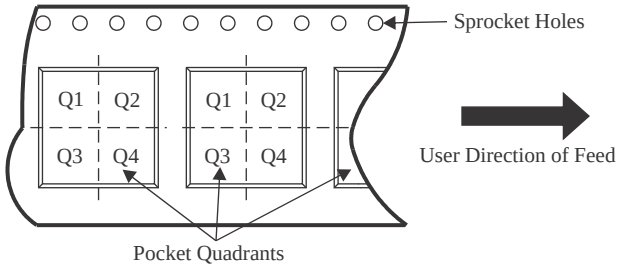


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

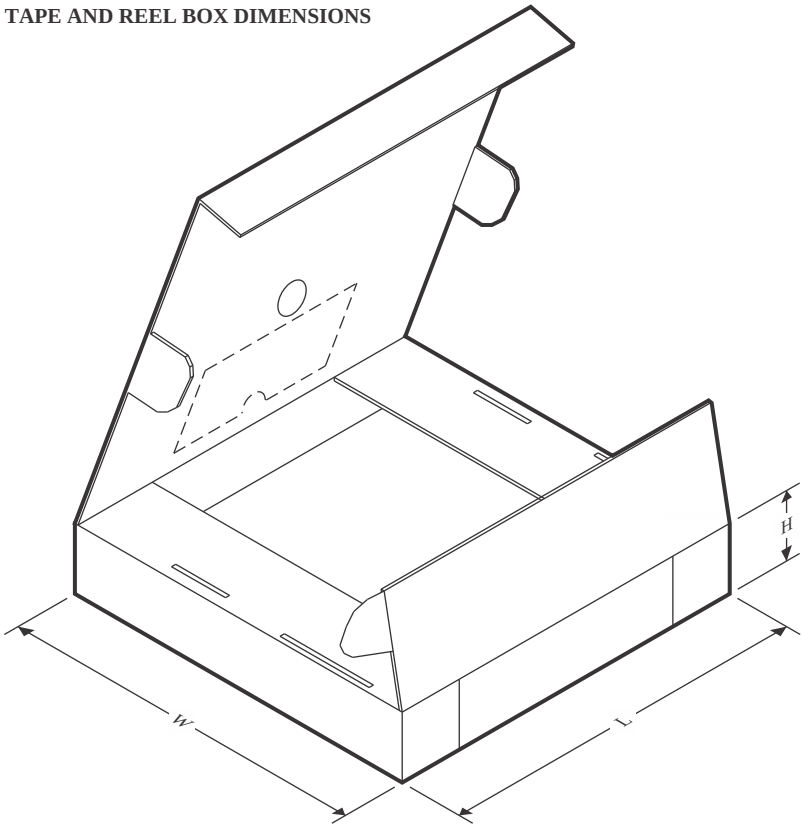
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

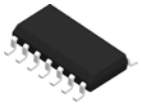
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9543ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCA9543APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9543APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9543ADR	SOIC	D	14	2500	356.0	356.0	35.0
PCA9543APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
PCA9543APWR	TSSOP	PW	14	2000	356.0	356.0	35.0

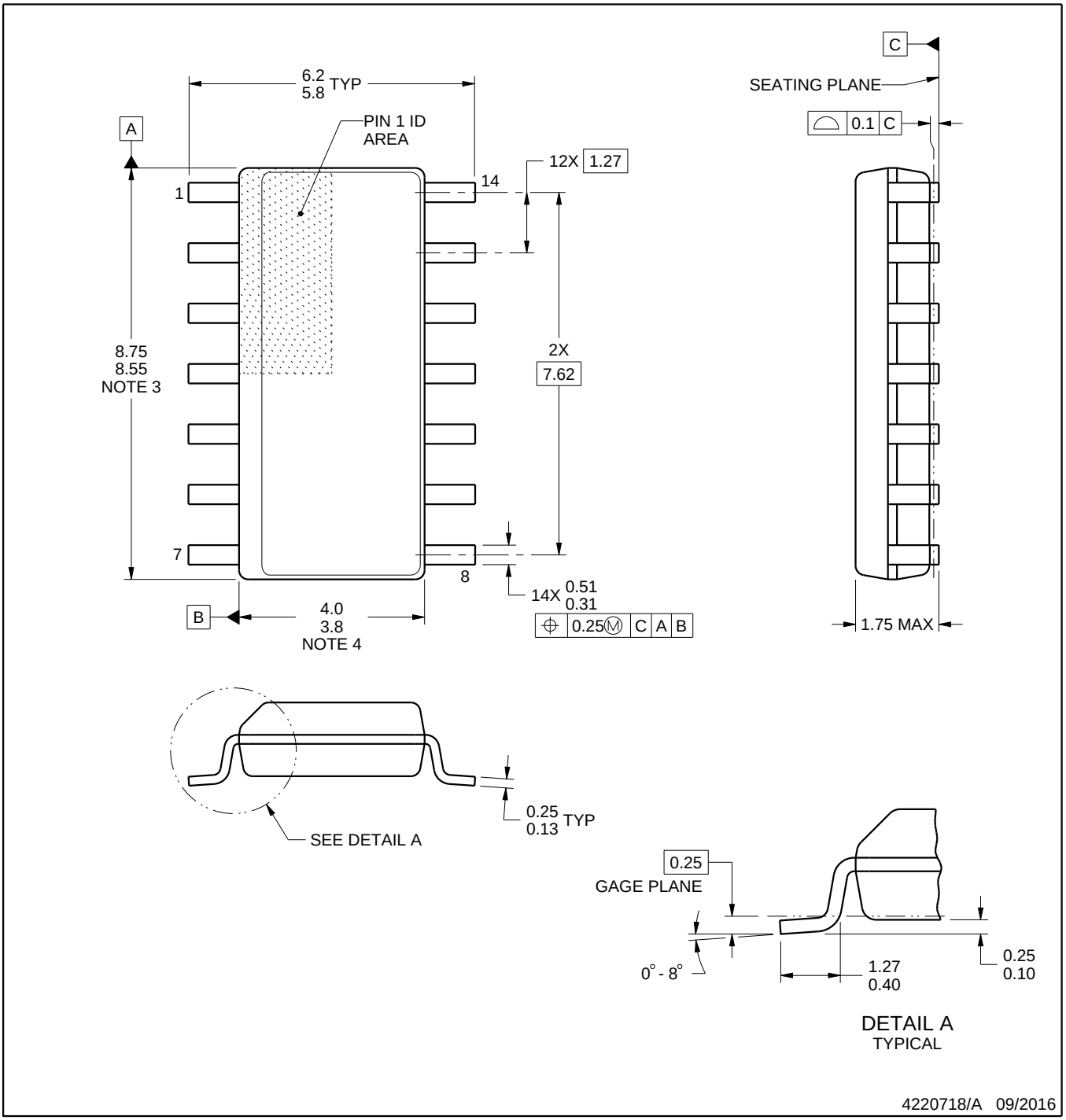


PACKAGE OUTLINE

D0014A

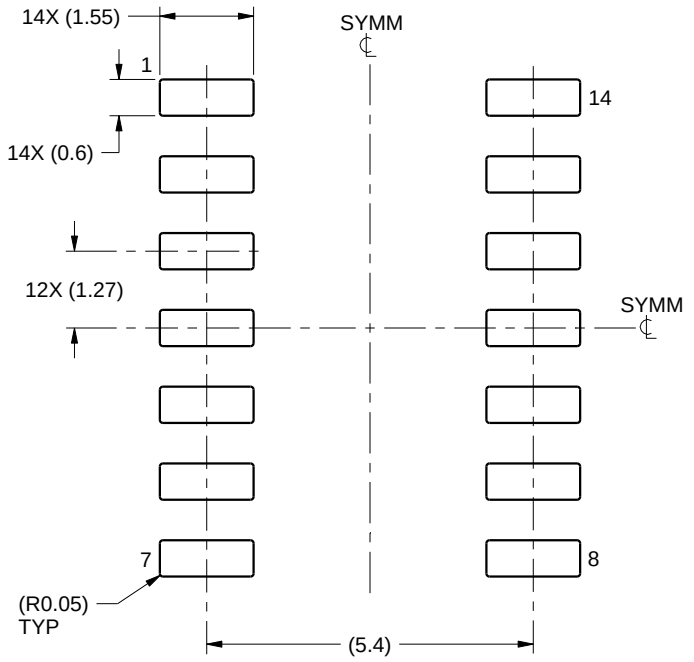
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

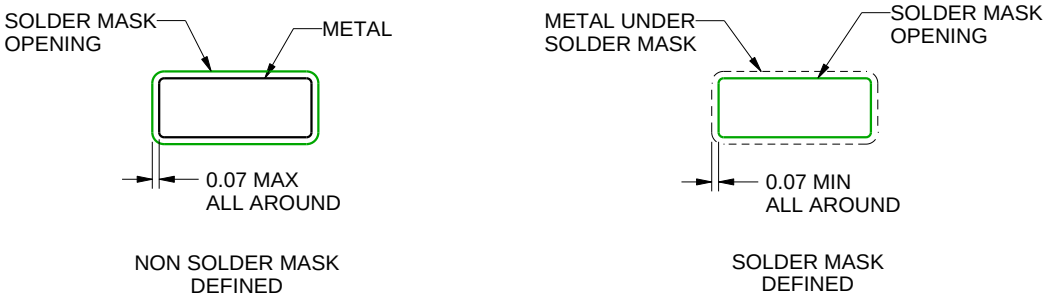


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

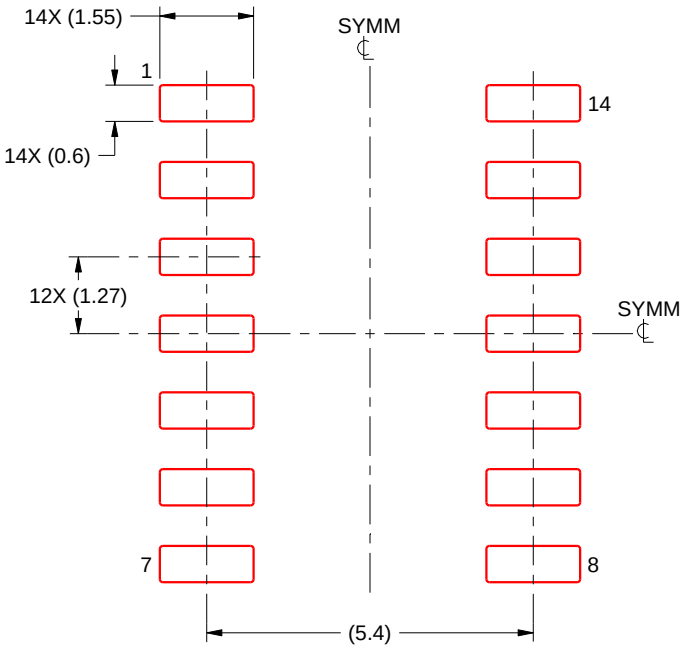
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

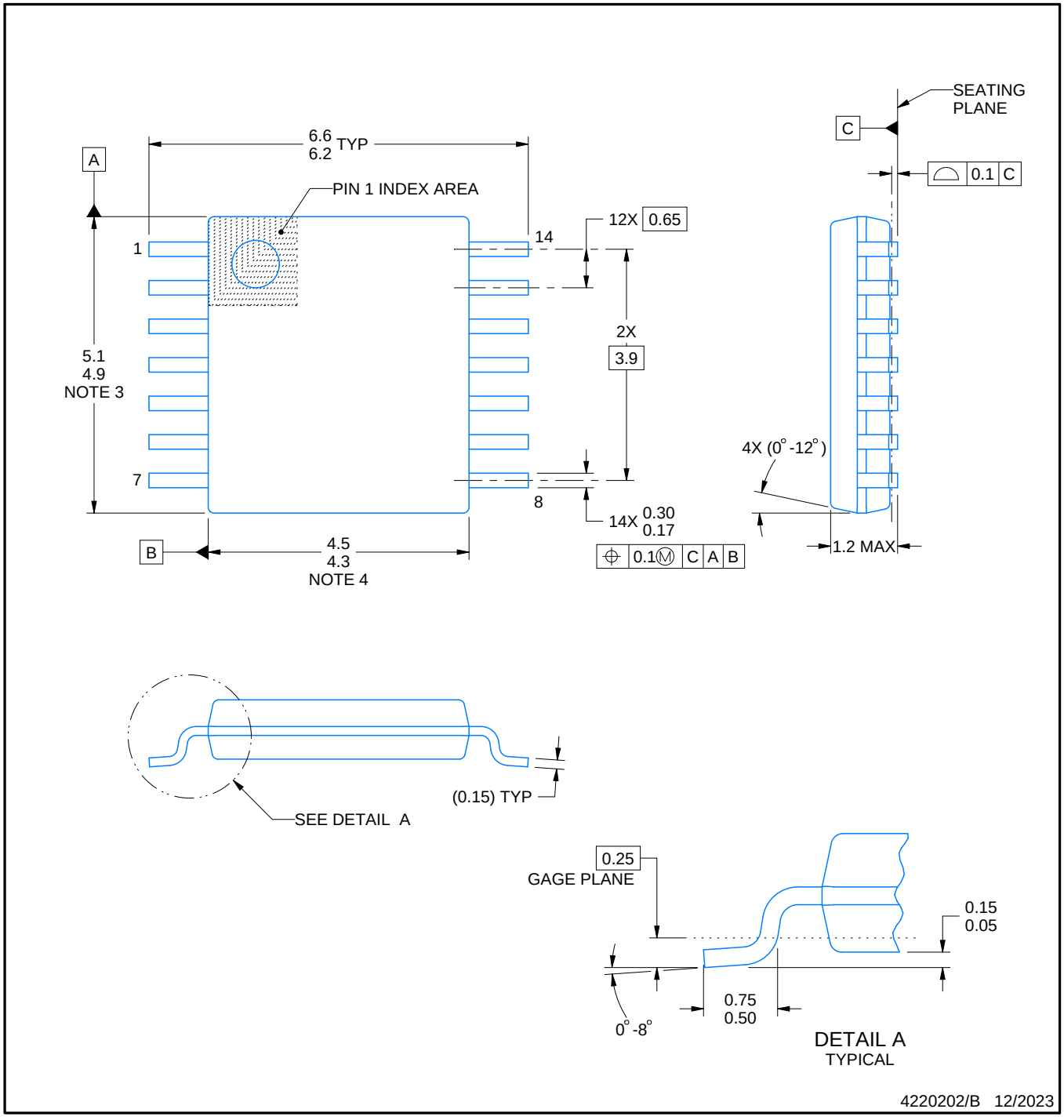
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

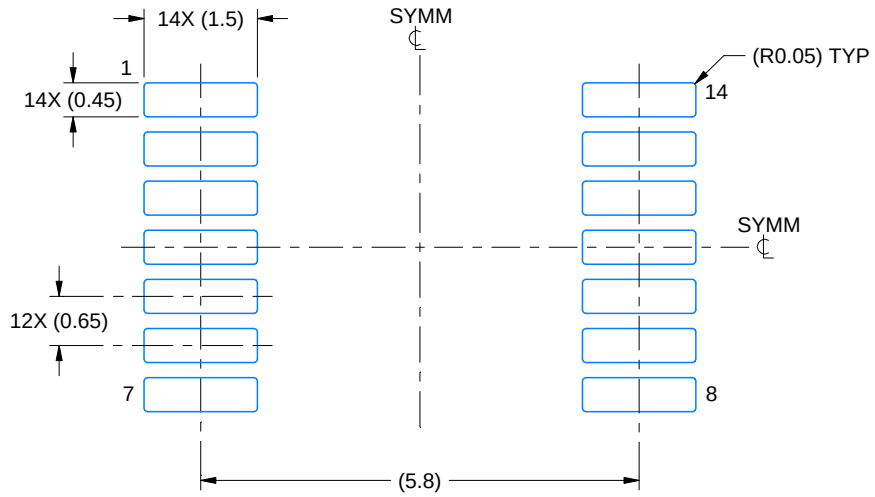
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

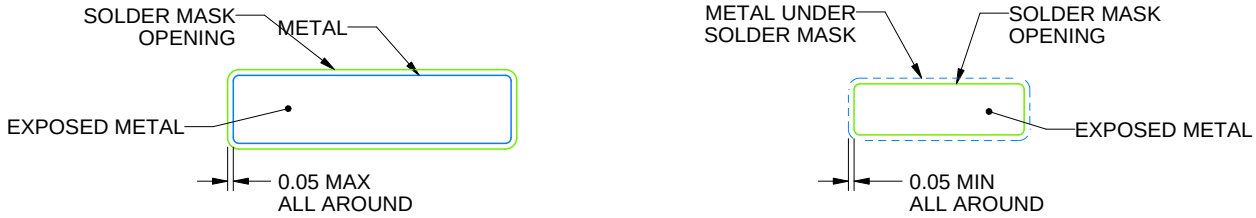


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

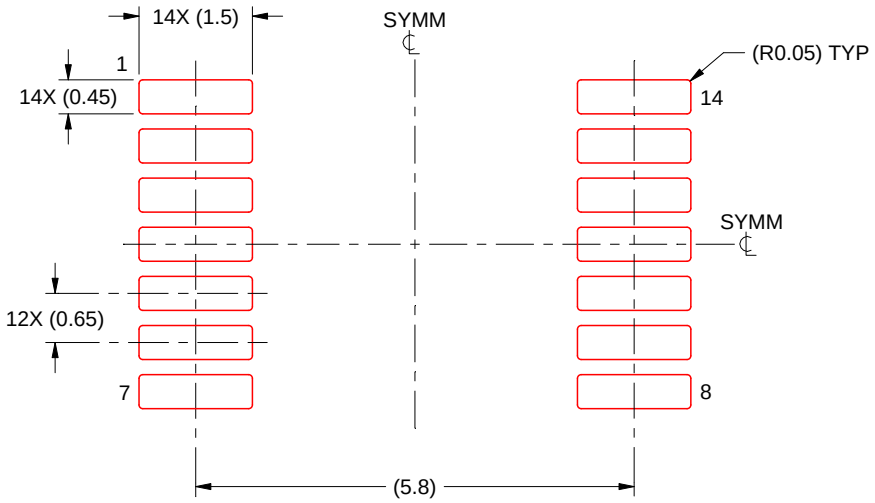


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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