TEXAS INSTRUMENTS
OPA859-Q1
JAJSKI5 – FEBRUARY 2021

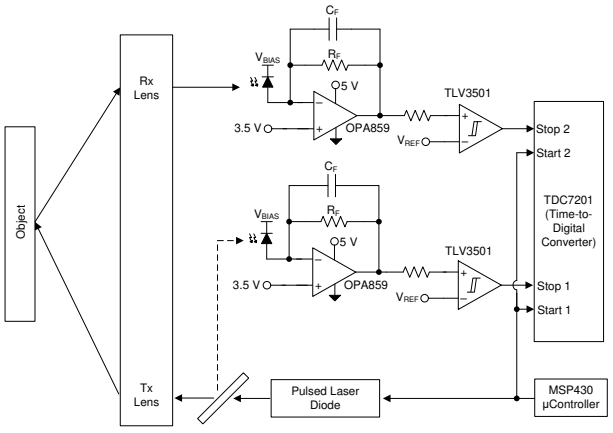
OPA859-Q1 1.8GHz ユニティ・ゲイン帯域幅、3.3-nV/√Hz、FET 入力アンプ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - 温度グレード 1:-40℃～+125℃、T_A
- 高いユニティ・ゲイン帯域幅:1.8GHz
- ゲイン帯域幅積:900MHz
- 極めて小さいバイアス電流 MOSFET 入力:10pA
- 小さい入力電圧ノイズ:3.3nV/√Hz
- スルーレート:1150V/µs
- 低い入力容量:
  - 同相:0.6pF
  - 差動:0.2pF
- 広い入力同相範囲:
  - 正電源から 1.4V
  - 負電源を含む
- TIA 構成で $2.5V_{PP}$ の出力スイング
- 電源電圧範囲:3.3V～5.25V
- 静止電流:20.5mA
- パッケージ:8 ピン WSON
- 温度範囲:–40℃～+125℃

2 アプリケーション

- 車載用 LIDAR
- タイム・オブ・フライト (ToF) カメラ
- 光学時間領域反射率測定 (OTDR)
- 3D スキャナ
- レーザーによる距離測定
- ソリッド・ステート・スキャン LIDAR
- 光学 ToF 位置センサ
- ドローン・ビジョン
- シリコン光電子増倍素子 (SiPM) バッファ・アンプ
- 光電子増倍管のポスト・アンプ



高速タイム・オブ・フライト・レシーバ

3 概要

OPA859-Q1 は、広帯域トランスインピーダンスおよび電圧アンプ・アプリケーション用、広帯域、低ノイズの CMOS 入力オペアンプです。デバイスがトランスインピーダンス・アンプ (TIA) として構成されているとき、0.9GHz のゲイン帯域幅積 (GBWP) により、低容量のフォトダイオード・アプリケーションで高い閉ループ帯域幅が得られます。

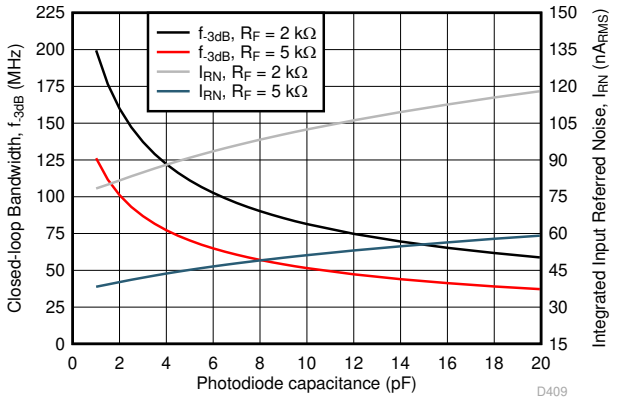
下のグラフは、アンプが TIA として構成されているときの OPA859-Q1 の帯域幅およびノイズ特性を、フォトダイオード容量の関数として示したものです。合計ノイズは、DC から左側のスケールで計算された周波数 (*f*) までの帯域幅の範囲にわたって計算されます。OPA859-Q1 のパッケージにはフィードバック・ピン (FB) があるため、入力と出力の間の帰還回路接続が簡単になります。

OPA859-Q1 は、OPA859-Q1 を TDC7201 などの時間 / デジタル・コンバータと組み合わせて使用する光学的タイム・オブ・フライト (ToF) システムで動作するよう最適化されています。OPA859-Q1 を使うと、THS4541-Q1 などの差動出力アンプを接続した高分解能 LIDAR システムで高速 A/D コンバータ (ADC) を駆動できます。

デバイス情報

部品番号(1)	パッケージ	本体サイズ (公称)
OPA859-Q1	WSON (8)	2.00 mm × 2.00 mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。



フォトダイオード容量と帯域幅およびノイズとの関係

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 4
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Typical Characteristics ... 8
7 Parameter Measurement Information ... 15
8 Detailed Description ... 16
8.1 Overview ... 16
8.2 Functional Block Diagram ... 16
8.3 Feature Description ... 17
8.4 Device Functional Modes ... 20
9 Application and Implementation ... 21
9.1 Application Information ... 21
9.2 Typical Application ... 21
10 Power Supply Recommendations ... 23
11 Layout ... 24
11.1 Layout Guidelines ... 24
11.2 Layout Example ... 24
12 Device and Documentation Support ... 25
12.1 Device Support ... 25
12.2 Documentation Support ... 25
12.3 Receiving Notification of Documentation Updates ... 25
12.4 サポート・リソース ... 25
12.5 Trademarks ... 25
12.6 静電気放電に関する注意事項 ... 25
12.7 用語集 ... 25
13 Mechanical, Packaging, and Orderable Information ... 25

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2021	*	Initial Release

Device Comparison Table

DEVICE	INPUT TYPE	MINIMUM STABLE GAIN	VOLTAGE NOISE (nV/√Hz)	INPUT CAPACITANCE (pF)	GAIN BANDWIDTH (GHz)
OPA855-Q1	Bipolar	7 V/V	0.98	0.8	8
OPA858-Q1	CMOS	7 V/V	2.5	0.8	5.5
OPA859-Q1	CMOS	1 V/V	3.3	0.8	0.9

5 Pin Configuration and Functions

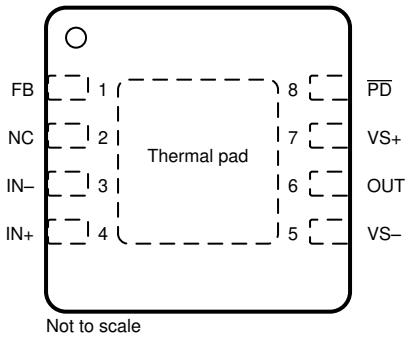


図 5-1. DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	1	I	Feedback connection to output of amplifier
IN–	3	I	Inverting input
IN+	4	I	Noninverting input
NC	2	—	Do not connect
OUT	6	O	Amplifier output
$\overline{PD}$	8	I	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VS–	5	—	Negative voltage supply
VS+	7	—	Positive voltage supply
Thermal pad		—	Connect the thermal pad to VS–

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)		5.5	V
V_{IN+}, $V_{IN–}$	Input voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
V_{ID}	Differential input voltage		1	V
VOUT	Output voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
I_{IN}	Continuous input current		±10	mA
I_{OUT}	Continuous output current(2)		±100	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	± 1500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)	3.3	5	5.25	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA859-Q1 DSG (WSON) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	100	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	45	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	6.8	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	45.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

V_{S+} = 5 V, V_{S-} = 0 V, input common-mode biased at midsupply, unity gain configuration, R_L = 200 Ω, output load is referenced to midsupply, and T_A ≈ +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		1.8		GHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		400		MHz
GBWP	Gain-bandwidth product			900		MHz
	Bandwidth for 0.1dB flatness			140		MHz
SR	Slew rate (10% - 90%)	V_{OUT} = 2-V step		1150		V/µs
t_r	Rise time	V_{OUT} = 100-mV step		0.3		ns
t_f	Fall time	V_{OUT} = 100-mV step		0.3		ns
	Settling time to 0.1%	V_{OUT} = 2-V step		8		ns
	Settling time to 0.001%	V_{OUT} = 2-V step		3000		ns
	Overshoot/undershoot	V_{OUT} = 2-V step		7%		
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		90		dBc
		f = 100 MHz, V_{OUT} = 2 V_{PP}		60		
HD3	Third-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		86		dBc
		f = 100 MHz, V_{OUT} = 2 V_{PP}		64		dBc
e_n	Input-referred voltage noise	f = 1 MHz		3.3		nV/√Hz
Z_{OUT}	Closed-loop output impedance	f = 1 MHz		0.15		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain		60	65		dB
V_{OS}	Input offset voltage	T_A = 25°C	–5	±0.9	5	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	T_A = –40°C to +125°C		–2		µV/°C
I_{BN}, I_{BI}	Input bias current	T_A = 25°C	–5	±0.5	5	pA
I_{BOS}	Input offset current	T_A = 25°C	–5	±0.1	5	pA
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V	70	84		dB
INPUT						
	Common-mode input resistance			1		GΩ
C_{CM}	Common-mode input capacitance			0.62		pF
	Differential input resistance			1		GΩ
C_{DIFF}	Differential input capacitance			0.2		pF
V_{IH}	Common-mode input range (high)	V_{S+} = 3.3 V, CMRR > 66 dB	1.7	1.9		V
V_{IL}	Common-mode input range (low)	V_{S+} = 3.3 V, CMRR > 66 dB		0	0.4	V
V_{IH}	Common-mode input range (high)	CMRR > 66 dB	3.4	3.6		V
		T_A = –40°C to +125°C, CMRR > 66 dB		3.3		
V_{IL}	Common-mode input range (low)	CMRR > 66 dB		0	0.4	V
		T_A = –40°C to +125°C, CMRR > 66 dB		0.35	0.45	
OUTPUT						
V_{OH}	Output voltage (high)	V_{S+} = 3.3 V, T_A = 25°C	2.3	2.4		V
V_{OH}	Output voltage (high)	TA = 25°C	3.95	4.1		V
		T_A = –40°C to +125°C		3.9		
V_{OL}	Output voltage (low)	V_{S+} = 3.3 V, T_A = 25°C		1.05	1.15	V
V_{OL}	Output voltage (low)	T_A = 25°C		1.1	1.15	V
		T_A = –40°C to +125°C		1.2		

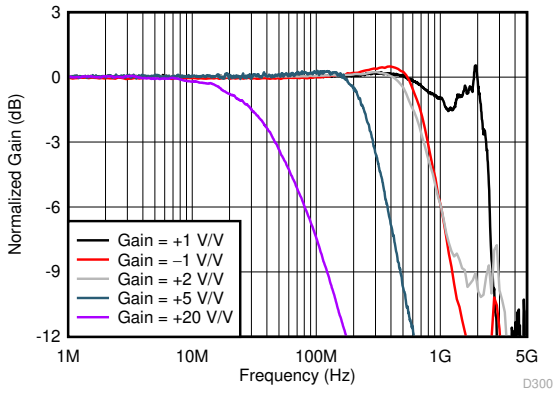
6.5 Electrical Characteristics (continued)

V_{S+} = 5 V, V_{S-} = 0 V, input common-mode biased at midsupply, unity gain configuration, R_L = 200 Ω, output load is referenced to midsupply, and T_A ≈ +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{O_LIN}	Linear output drive (sink and source)	R_L = 10 Ω, A_{OL} > 52 dB	65	76		mA
		T_A = –40°C to +125°C, R_L = 10 Ω, A_{OL} > 52 dB		64		
I_{SC}	Output short-circuit current		85	105		mA
POWER SUPPLY						
I_Q	Quiescent current	V_{S+} = 5 V	18	20.5	24	mA
		V_{S+} = 3.3 V	17.5	20	23.5	
		V_{S+} = 5.25 V	18	21	24	
		T_A = 125°C		24.5		
		T_A = –40°C		18.5		
PSRR+	Positive power-supply rejection ratio		66	74		dB
PSRR–	Negative power-supply rejection ratio		64	72		
POWER DOWN						
	Disable voltage threshold	Amplifier OFF below this voltage	0.65	1		V
	Enable voltage threshold	Amplifier ON above this voltage		1.5	1.8	V
	Power-down quiescent current			70	140	µA
	$\overline{PD}$ bias current			70	200	µA
	Turnon time delay	Time to V_{OUT} = 90% of final value		25		ns
	Turnoff time delay			120		ns

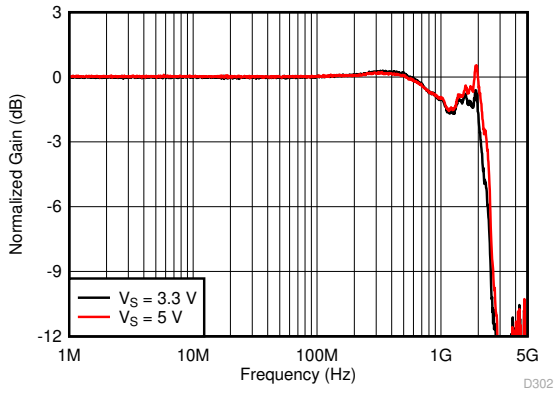
6.6 Typical Characteristics

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, Gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



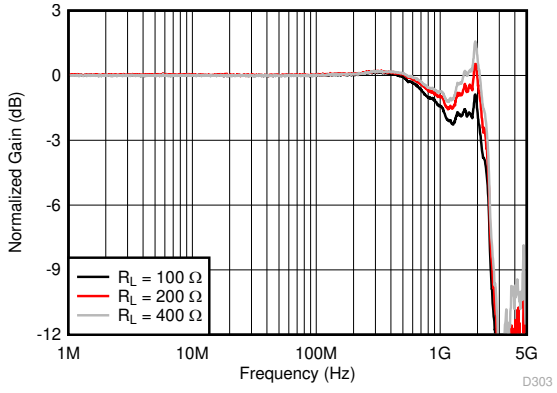
V_{OUT} = 100 mV_{PP}; see セクション 7 for circuit configuration

図 6-1. Small-Signal Frequency Response vs Gain



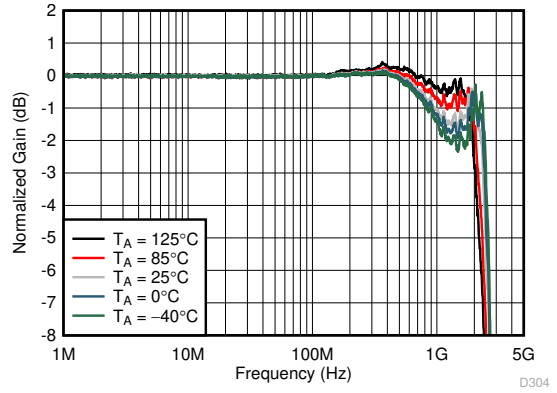
V_{OUT} = 100 mV_{PP}

図 6-2. Small-Signal Frequency Response vs Supply Voltage



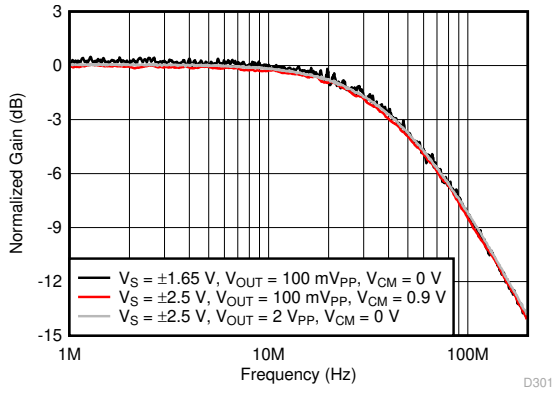
V_{OUT} = 100 mV_{PP}

図 6-3. Small-Signal Frequency Response vs Output Load



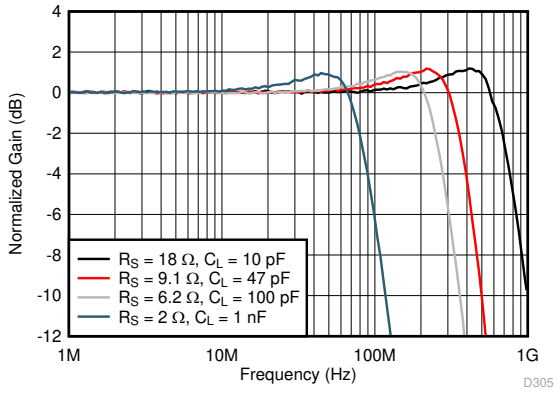
V_{OUT} = 100 mV_{PP}

図 6-4. Small-Signal Frequency Response vs Ambient Temperature



Gain = 20 V/V R_F = 453 Ω

図 6-5. Frequency Response at Gain = 20 V/V

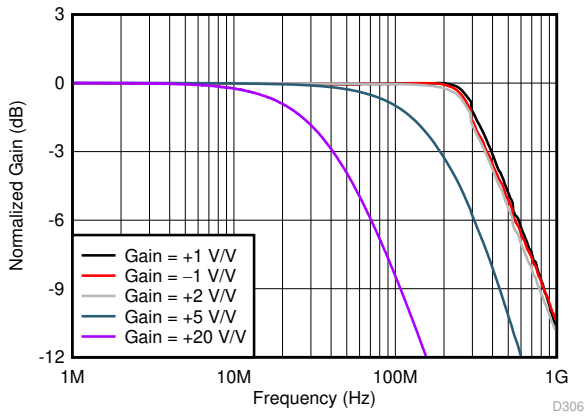


V_{OUT} = 100 mV_{PP}, See 図 7-4 for circuit configuration

図 6-6. Small-Signal Frequency Response vs Capacitive Load

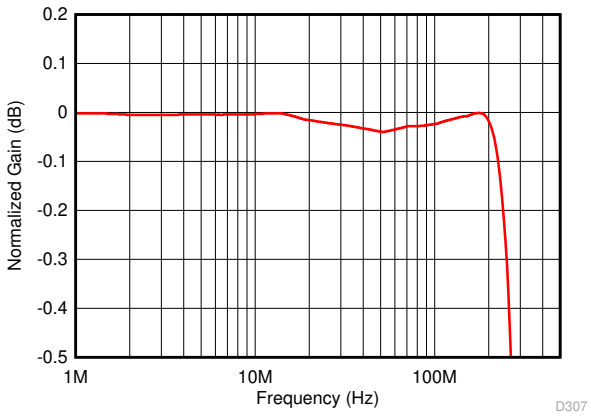
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, Gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



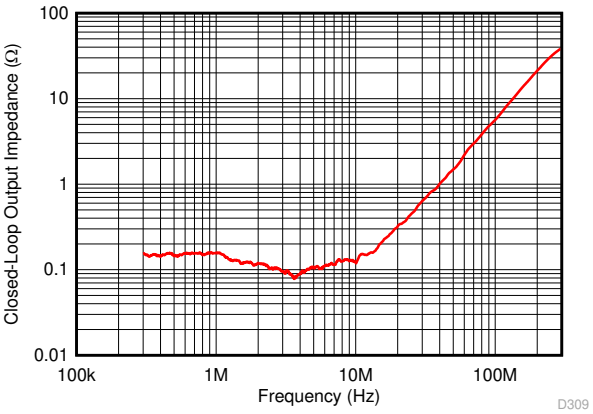
V_{OUT} = 2 V_{PP}

図 6-7. Large-Signal Frequency Response vs Gain



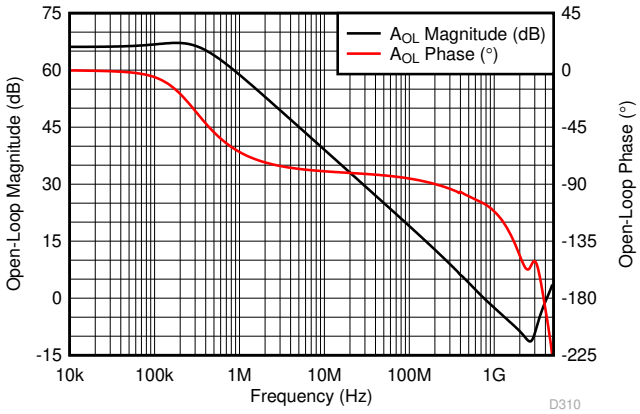
V_{OUT} = 2 V_{PP}

図 6-8. Large-Signal Response for 0.1-dB Gain Flatness



Small-Signal Response

図 6-9. Closed-Loop Output Impedance vs Frequency



Small-Signal Response

図 6-10. Open-Loop Magnitude and Phase vs Frequency

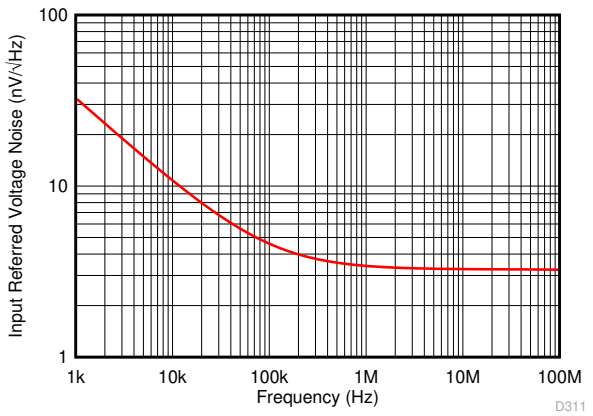
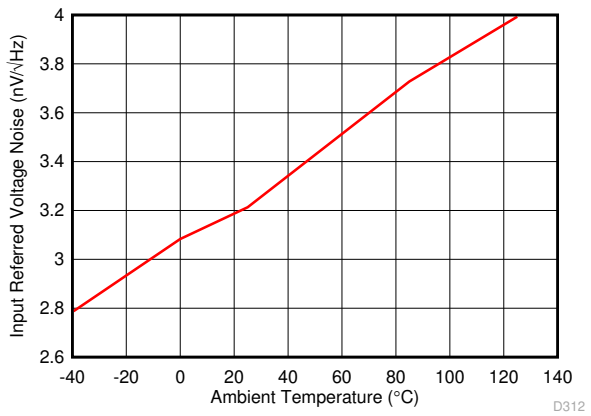


図 6-11. Voltage Noise Density vs Frequency



Frequency 10 MHz

図 6-12. Voltage Noise Density vs Ambient Temperature

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, Gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)

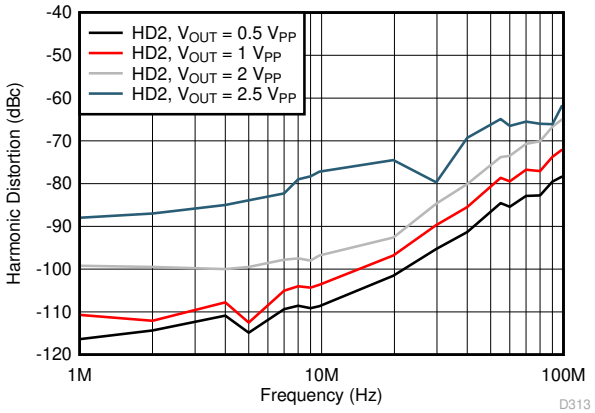


図 6-13. Harmonic Distortion (HD2) vs Output Swing

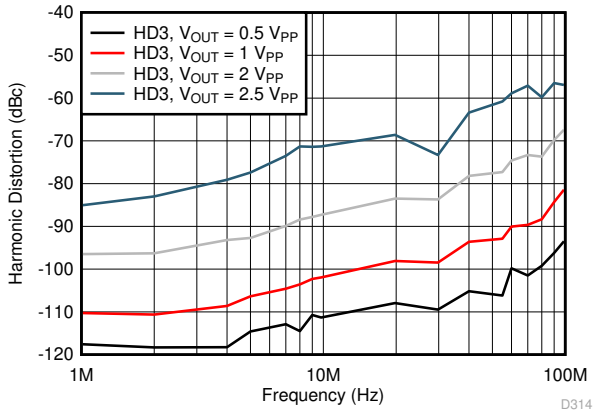
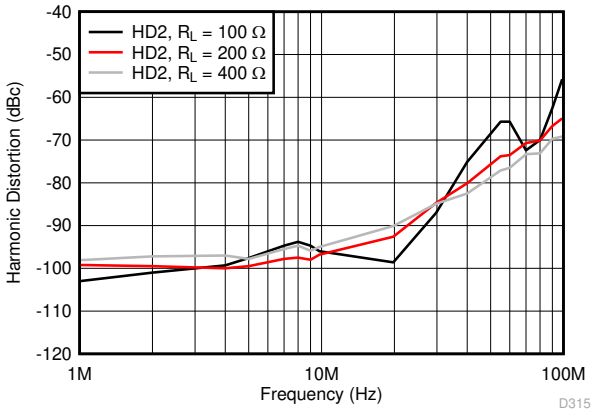
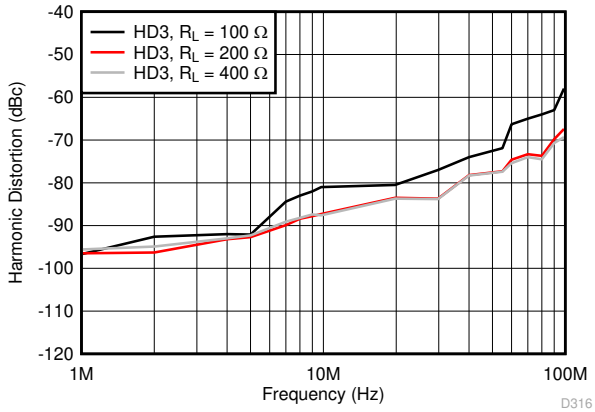


図 6-14. Harmonic Distortion (HD3) vs Output Swing



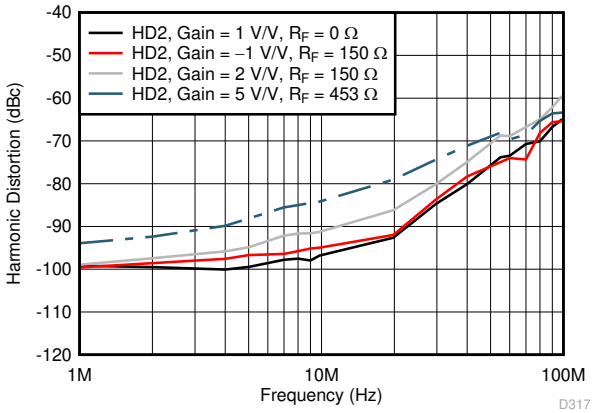
V_{OUT} = 2 V_{PP}

図 6-15. Harmonic Distortion (HD2) vs Output Load



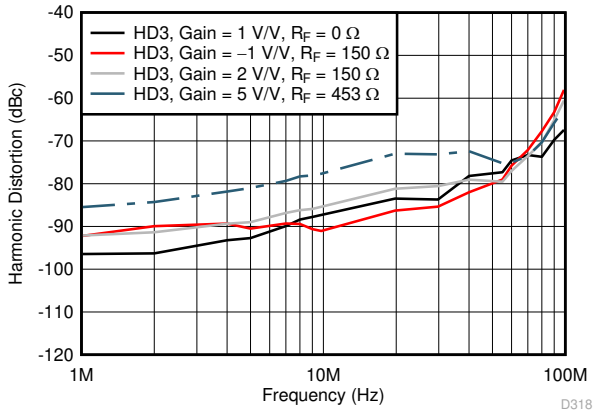
V_{OUT} = 2 V_{PP}

図 6-16. Harmonic Distortion (HD3) vs Output Load



V_{OUT} = 2 V_{PP}

図 6-17. Harmonic Distortion (HD2) vs Gain

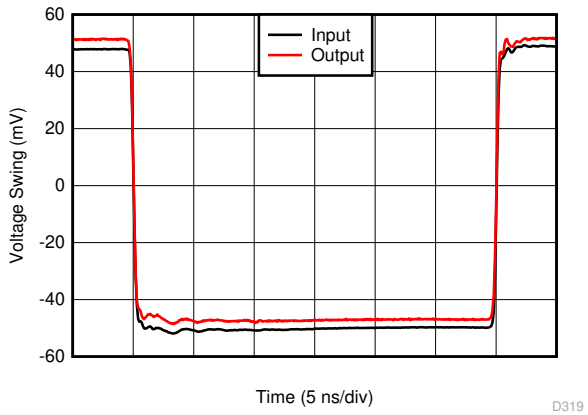


V_{OUT} = 2 V_{PP}

図 6-18. Harmonic Distortion (HD3) vs Gain

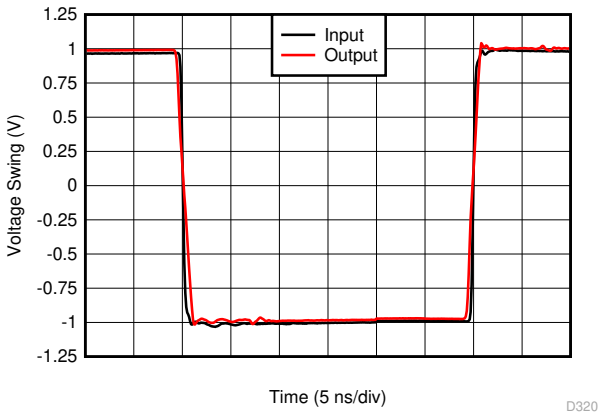
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, Gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



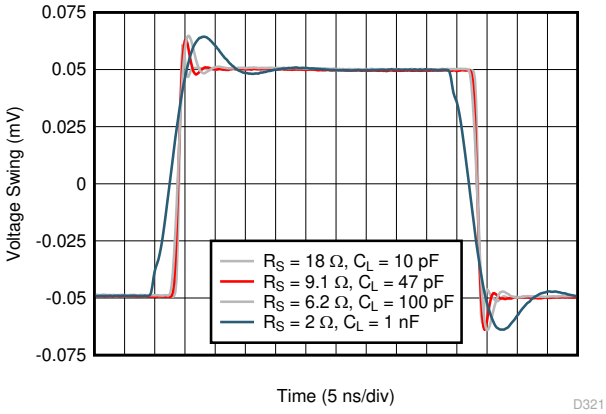
Average Rise and Fall Time (10% - 90%) = 450 ps

図 6-19. Small-Signal Transient Response



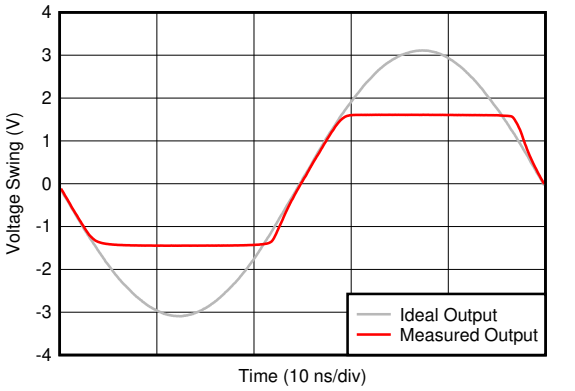
Slew Rate: Falling = 1160 V/µs, Rising = 1400 V/µs

図 6-20. Large-Signal Transient Response



See 図 7-4 for circuit configuration

図 6-21. Small-Signal Transient Response vs Capacitive Load



Gain = 5 V/V, R_F = 453 Ω, 2x Output Overdrive

図 6-22. Output Overload Response

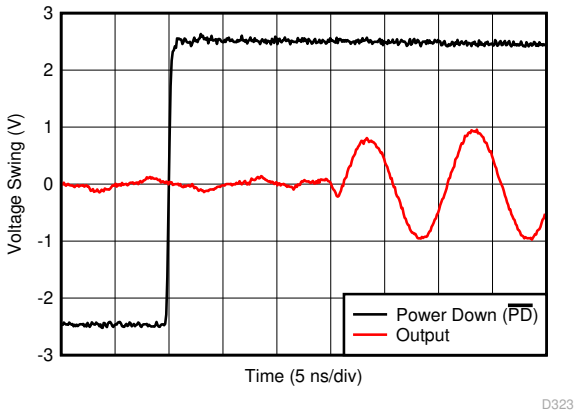


図 6-23. Turnon Transient Response

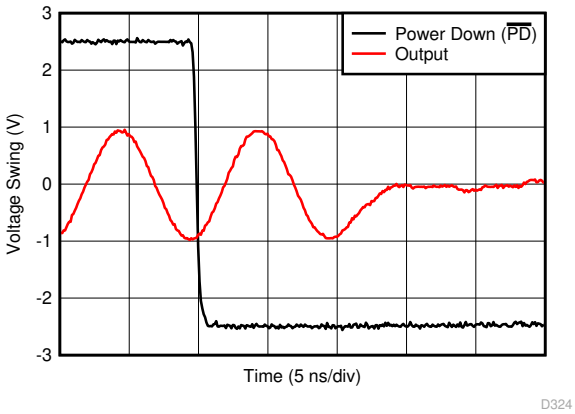
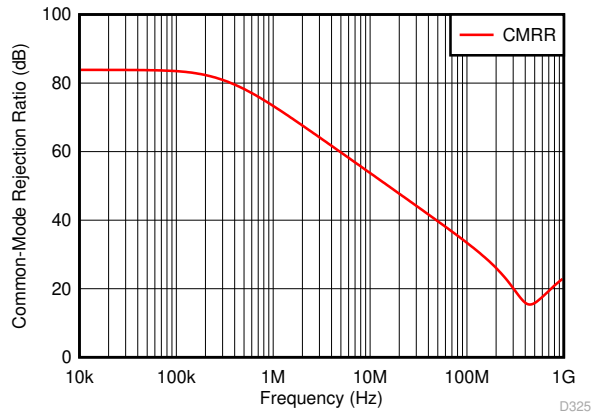


図 6-24. Turnoff Transient Response

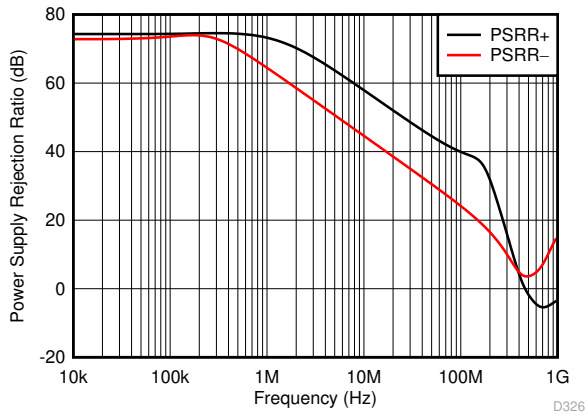
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, Gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



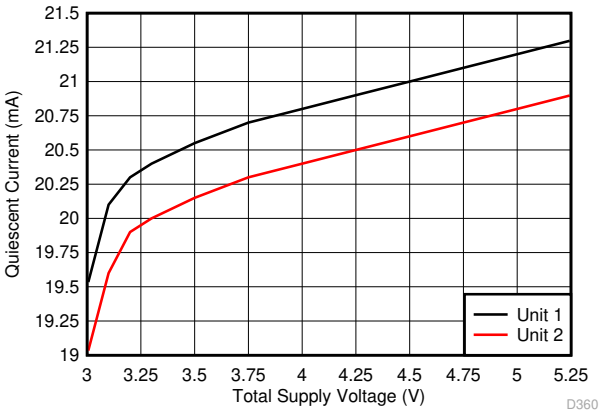
Small-Signal Response

図 6-25. Common-Mode Rejection Ratio vs Frequency



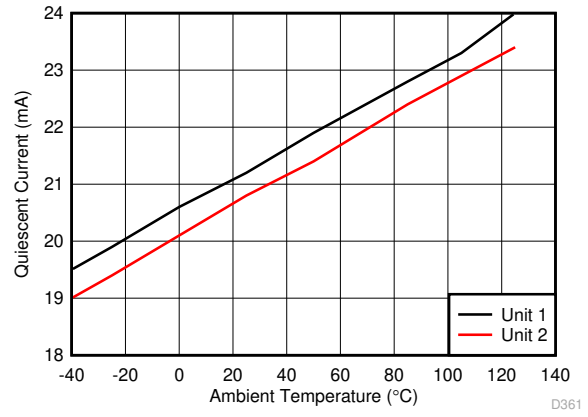
Small-Signal Response

図 6-26. Power Supply Rejection Ratio vs Frequency



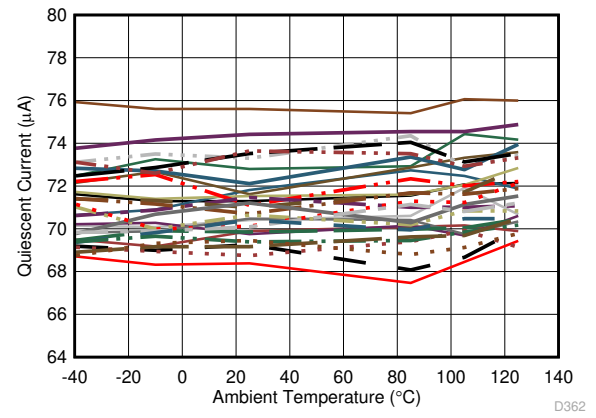
2 Typical Units

図 6-27. Quiescent Current vs Supply Voltage



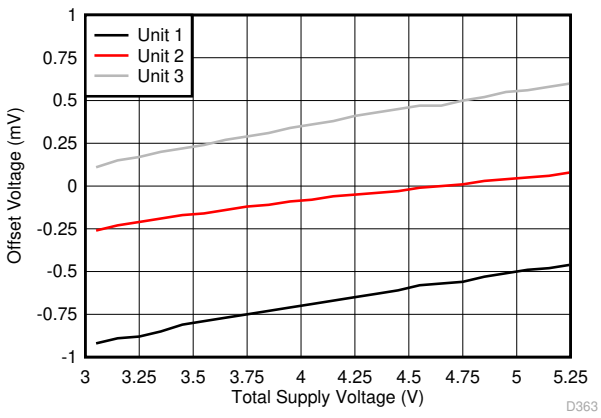
V_S = 5 V 2 Typical Units

図 6-28. Quiescent Current vs Ambient Temperature



32 Units Tested

図 6-29. Quiescent Current (Amplifier Disabled) vs Ambient Temperature

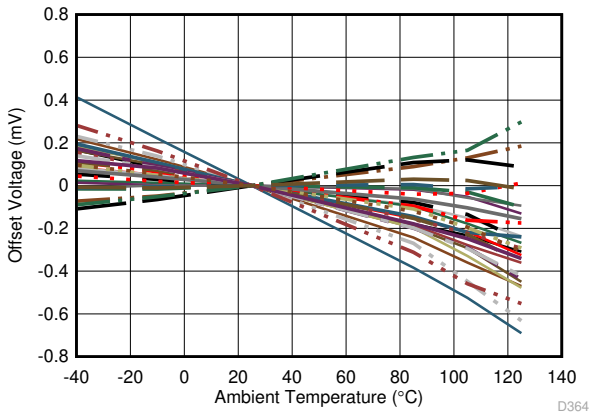


3 Typical Units

図 6-30. Offset Voltage vs Supply Voltage

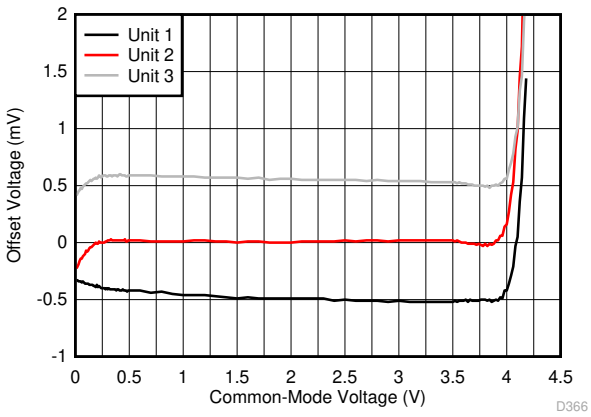
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, Gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



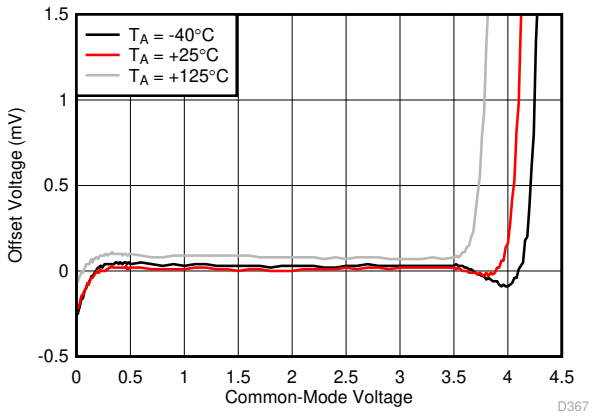
μ = –2.1 μV/°C σ = 2 μV/°C 32 Units Tested

図 6-31. Offset Voltage vs Ambient Temperature



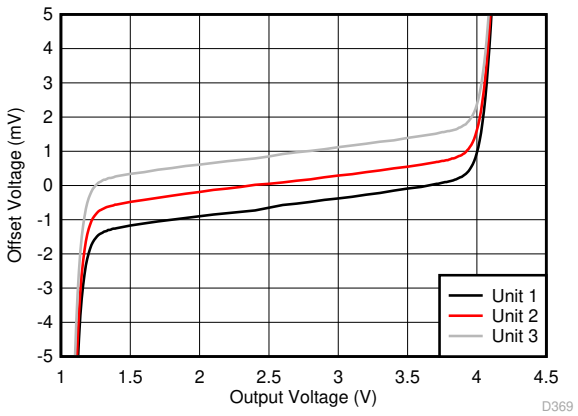
V_S = 5 V 3 Typical Units

図 6-32. Offset Voltage vs Input Common-Mode Voltage



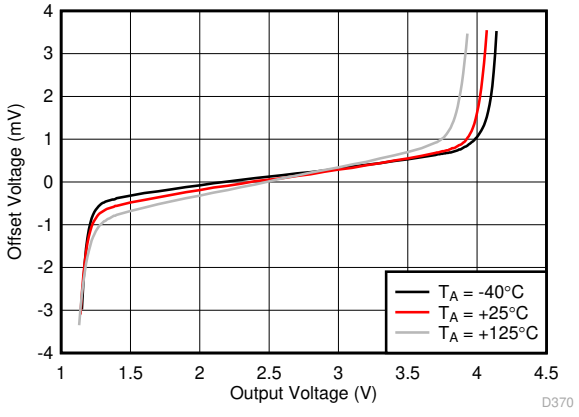
V_S = 5 V

図 6-33. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature



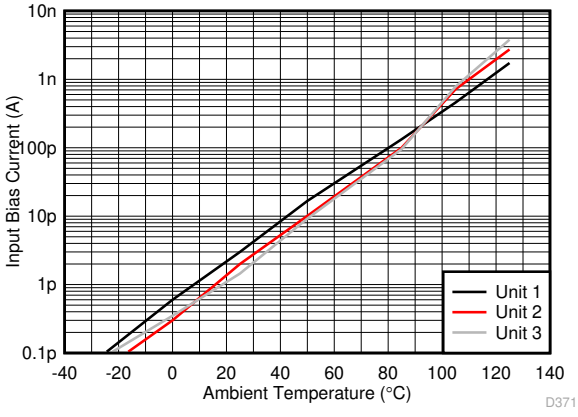
V_S = 5 V 3 Typical Units

図 6-34. Offset Voltage vs Output Swing



V_S = 5 V

図 6-35. Offset Voltage vs Output Swing vs Ambient Temperature

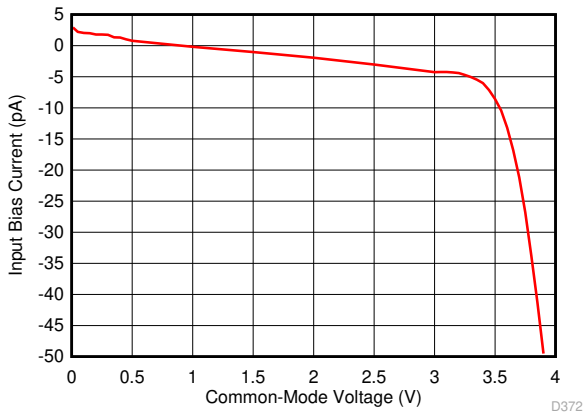


3 Typical Units

図 6-36. Input Bias Current vs Ambient Temperature

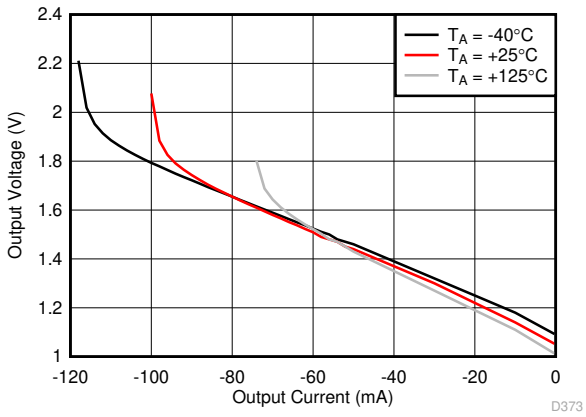
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, Gain = 1 V/V, R_F = 0 Ω, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



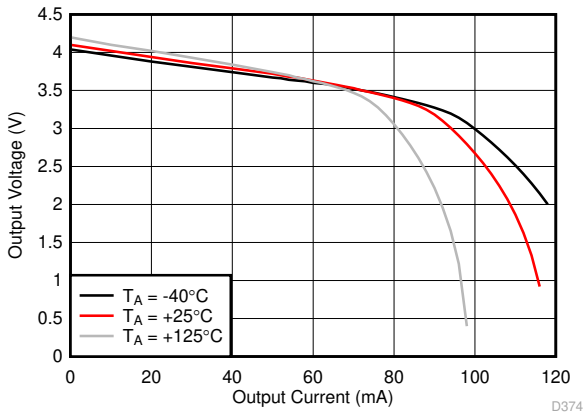
V_S = 5 V

図 6-37. Input Bias Current vs Input Common-Mode Voltage



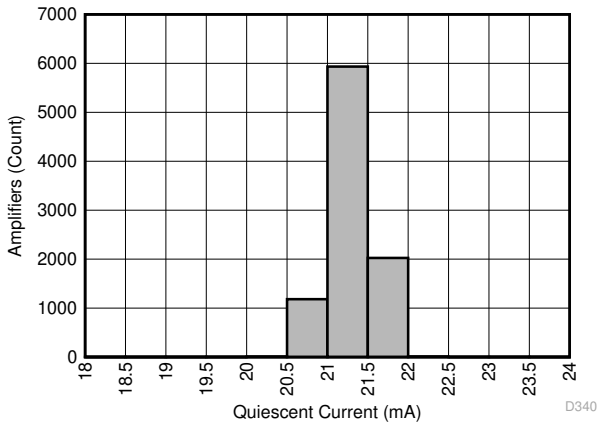
V_S = 5 V

図 6-38. Output Swing vs Sinking Current



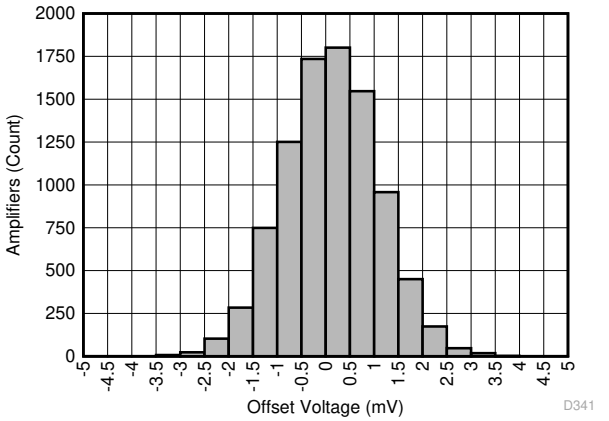
V_S = 5 V

図 6-39. Output Swing vs Sourcing Current



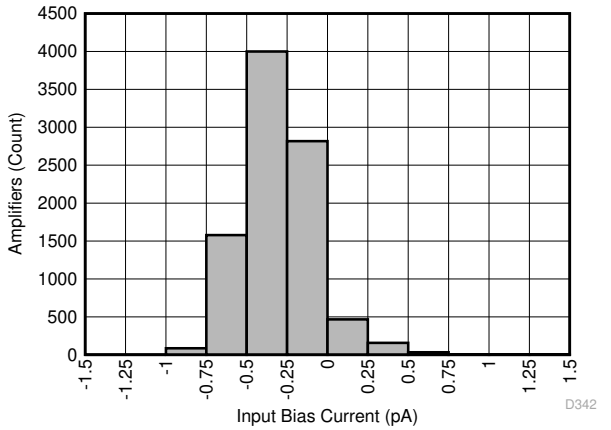
μ = 20.8 mA σ = 0.25 mA 9150 Units Tested

図 6-40. Quiescent Current Distribution



μ = –0.38 mV σ = 0.97 mV 9150 Units Tested

図 6-41. Offset Voltage Distribution



μ = –0.55 pA σ = 0.23 pA 9150 Units Tested

図 6-42. Input Bias Current Distribution

7 Parameter Measurement Information

The various test setup configurations for the OPA859-Q1 are shown in the figures below. When configuring the OPA859-Q1 as a noninverting amplifier in gains less 3 V/V, set R_F = 150 Ω. When configuring the OPA859-Q1 as a noninverting amplifier in gains of 4 V/V and greater, set R_F = 453 Ω.

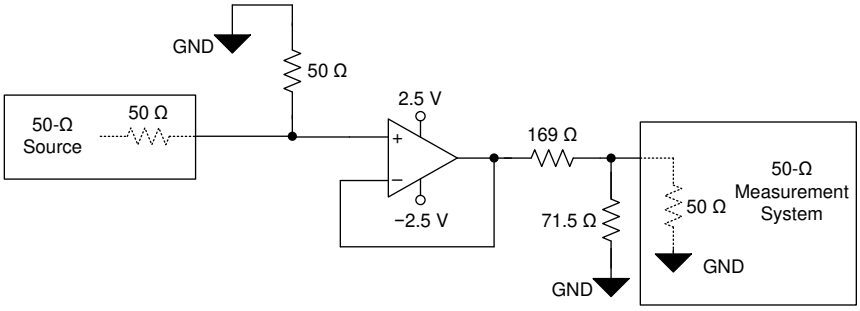
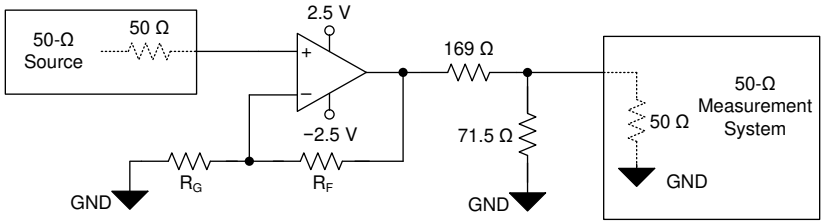


図 7-1. Unity-Gain Buffer Configuration



R_G values depend on gain configuration

図 7-2. Noninverting Configuration

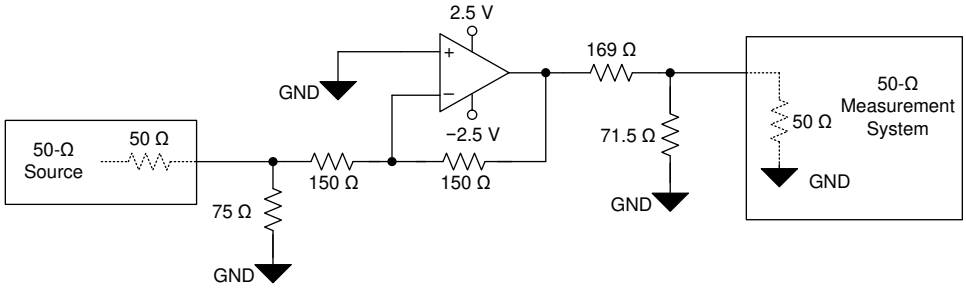


図 7-3. Inverting Configuration (Gain = –1 V/V)

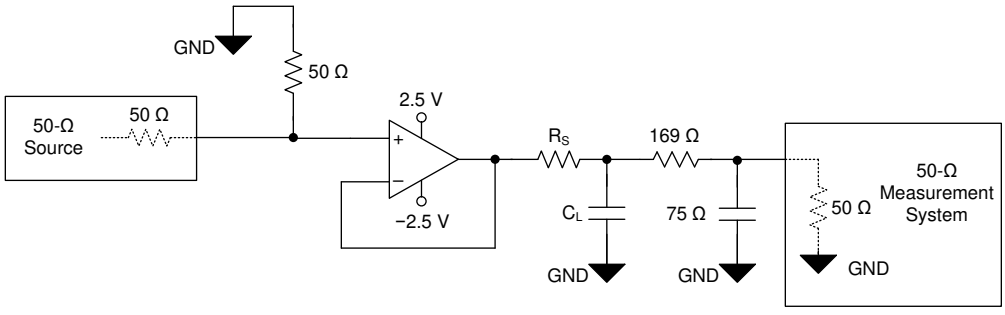


図 7-4. Capacitive Load Driver Configuration

8 Detailed Description

8.1 Overview

The ultra-wide, 900-MHz gain bandwidth product (GBWP) of the OPA859-Q1, combined with the broadband voltage noise of 3.3 nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA859-Q1 combines multiple features to optimize dynamic performance. In addition to the wide small-signal bandwidth, the OPA859-Q1 has 400 MHz of large-signal bandwidth (V_{OUT} = 2 V_{PP}), and a slew rate of 1150 V/µs.

The OPA859-Q1 is offered in a 2-mm × 2-mm, 8-pin WSON package that features a feedback (FB) pin for a simple feedback network connection between the amplifiers output and inverting input. Excess capacitance on an amplifiers input pin can reduce phase margin causing instability. This problem is exacerbated in the case of very wideband amplifiers like the OPA859-Q1. To reduce the effects of stray capacitance on the input node, the OPA859-Q1 pinout features an isolation pin (NC) between the feedback and inverting input pins that increases the physical spacing between them thereby reducing parasitic coupling at high frequencies. The OPA859-Q1 also features a very low capacitance input stage with only 0.8-pF of total input capacitance.

8.2 Functional Block Diagram

The OPA859-Q1 is a classic voltage feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, like the two basic options shown in 図 8-1 and 図 8-2. The DC operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically connected to ground in split-supply applications.

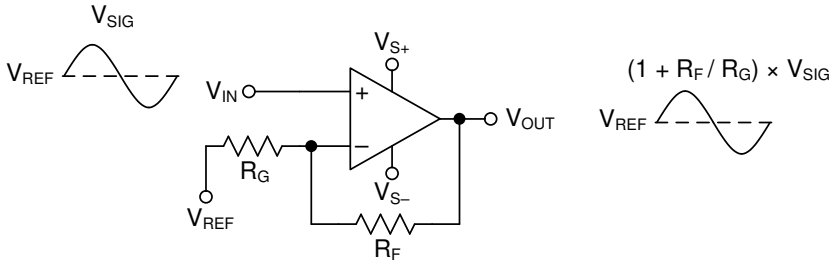


図 8-1. Noninverting Amplifier

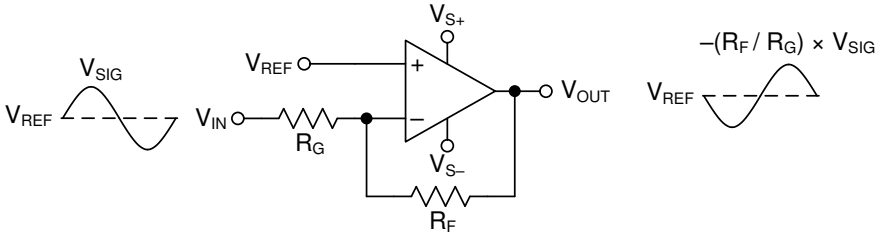


図 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input and ESD Protection

The OPA859-Q1 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as 図 8-3 shows. There are two antiparallel diodes between the inputs of the amplifier that clamp the inputs during an overrange or fault condition.

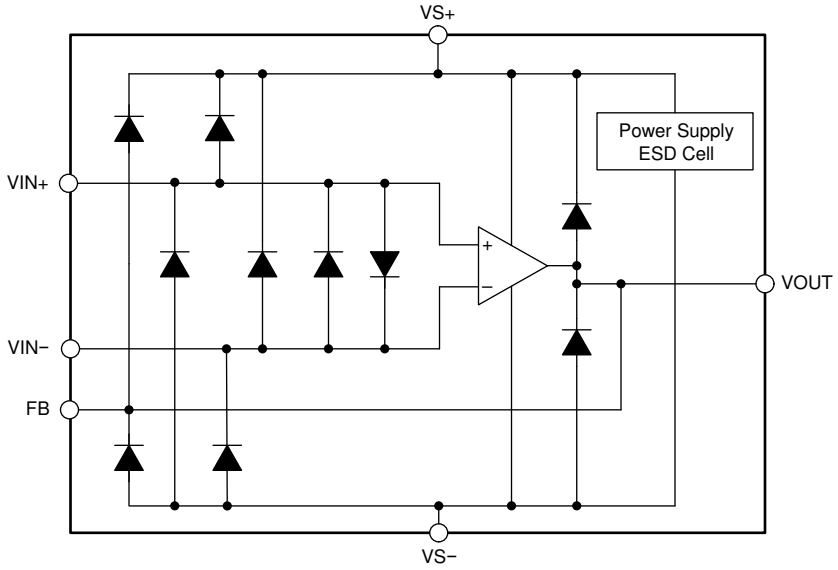


図 8-3. Internal ESD Structure

8.3.2 Feedback Pin

The OPA859-Q1 pin layout is optimized to minimize parasitic inductance and capacitance, which is a critical care about in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor (R_F) can connect between the FB and IN– pin on the same side of the package (see 図 8-4) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins by increasing the physical separation between the pins.

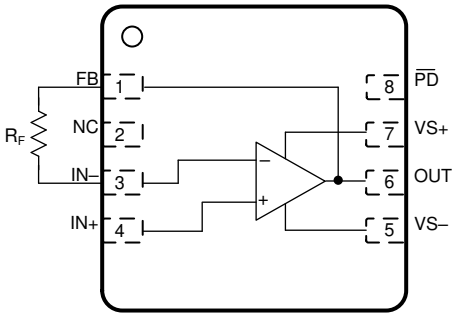


図 8-4. R_F Connection Between FB and IN– Pins

8.3.3 Wide Gain-Bandwidth Product

図 6-10 shows the open-loop magnitude and phase response of the OPA859-Q1. Calculate the gain bandwidth product of any op amp by determining the frequency at which the A_{OL} is 40 dB and multiplying that frequency by a factor of 100. The open-loop response shows the OPA859-Q1 to have approximately 63° of phase-margin when configured as a unity-gain buffer.

図 8-5 shows the open-loop magnitude (A_{OL}) of the OPA859-Q1 as a function of temperature. The results show approximately 5° of phase-margin variation over the entire temperature range. Semiconductor process variation is the naturally occurring variation in the attributes of a transistor (Early-voltage, β, channel-length, and width) and other passive elements (resistors and capacitors) when fabricated into an integrated circuit. The process variation can occur across devices on a single wafer or across devices over multiple wafer lots over time. Typically the variation across a single wafer is tightly controlled. 図 8-6 shows the A_{OL} magnitude of the OPA859-Q1 as a function of process variation over time. The results show the A_{OL} curve for the nominal process corner and the variation one standard deviation from the nominal. The simulated results show less than 2° of phase-margin difference within a standard deviation of process variation when the amplifier is configured as a unity-gain bufffer.

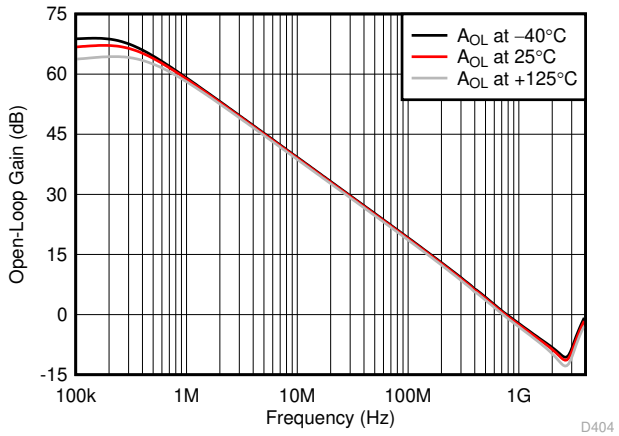


図 8-5. Open-Loop Gain vs Temperature

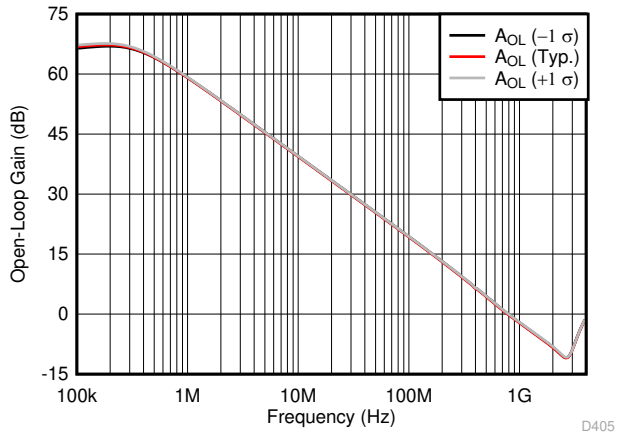


図 8-6. Open-Loop Gain vs Process Variation

8.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA859-Q1 features a high slew rate of 2750 V/µs. The slew rate is a critical parameter in high-speed pulse applications with narrow sub-10-ns pulses, such as optical time-domain reflectometry (OTDR) and LIDAR. The high slew rate of the OPA859-Q1 implies that the device accurately reproduces a 2-V, sub-ns pulse edge, as seen in 図 6-20. The wide bandwidth and slew rate of the OPA859-Q1 make it an excellent amplifier for high-speed signal-chain front ends.

図 8-7 shows the open-loop output impedance of the OPA859-Q1 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA859-Q1 is limited to approximately 3 V. The OPA859-Q1 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA859-Q1 output swing range coupled with the class-leading voltage noise specification for a CMOS amplifier maximizes the overall dynamic range of the signal chain.

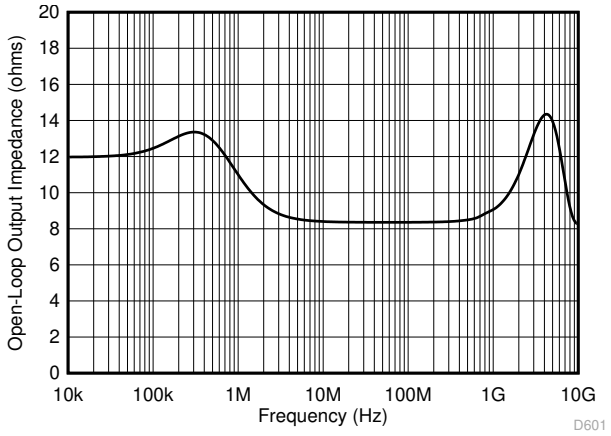


図 8-7. Open-Loop Output Impedance (Z_{OL}) vs Frequency

8.3.5 Current Noise

The input impedance of CMOS and JFET input amplifiers at low frequencies exceed several GΩs. However, at higher frequencies, the transistors parasitic capacitance to the drain, source, and substrate reduces the impedance. The high impedance at low frequencies eliminates any bias current and the associated shot noise. At higher frequencies, the input current noise increases (see 図 8-8) as a result of capacitive coupling between the CMOS gate oxide and the underlying transistor channel. This phenomenon is a natural artifact of the construction of the transistor and is unavoidable.

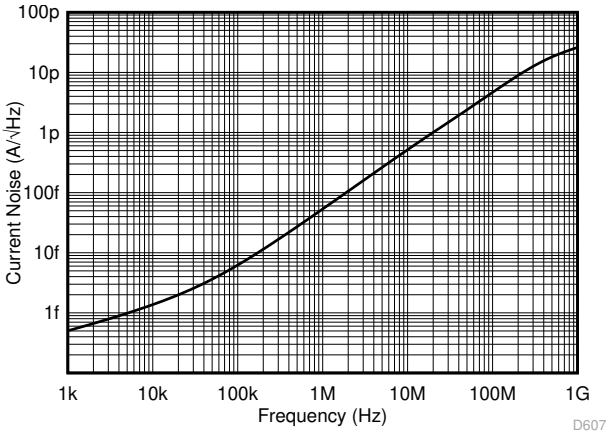


図 8-8. Input Current Noise (I_{BN} and I_{BI}) vs Frequency

8.4 Device Functional Modes

8.4.1 Split-Supply and Single-Supply Operation

The OPA859-Q1 can be configured with single-sided supplies or split-supplies as shown in 図 10-1. Split-supply operation using balanced supplies with the input common-mode set to ground eases lab testing because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground. In split-supply operation, the thermal pad must be connected to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA859-Q1 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. In single-supply operation, level shift the DC input and output reference voltages by half the difference between the power supply rails. This configuration maintains the input common-mode and output load reference at midsupply. To eliminate gain errors, the source driving the reference input common-mode voltage must have low output impedance across the frequency range of interest. In this case, the thermal pad must be connected to ground.

8.4.2 Power-Down Mode

The OPA859-Q1 features a power-down mode to reduce the quiescent current to conserve power. 図 6-23 and 図 6-24 show the transient response of the OPA859-Q1 as the $\overline{PD}$ pin toggles between the disabled and enabled states.

The $\overline{PD}$ disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable and enable threshold voltages are 0.65 V and 1.8 V, respectively. If the amplifier is configured with ±1.65 V supplies, then the threshold voltages are at –1 V and 0.15 V. If the amplifier is configured with ±2.5 V supplies, then the threshold voltages are at –1.85 V and –0.7 V.

図 8-9 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept down from the enabled state to the disabled state. Similarly, 図 8-10 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept up from the disabled state to the enabled state. The small difference in the switching thresholds between the down sweep and the up sweep is caused by the hysteresis designed into the amplifier to increase immunity to noise on the $\overline{PD}$ pin.

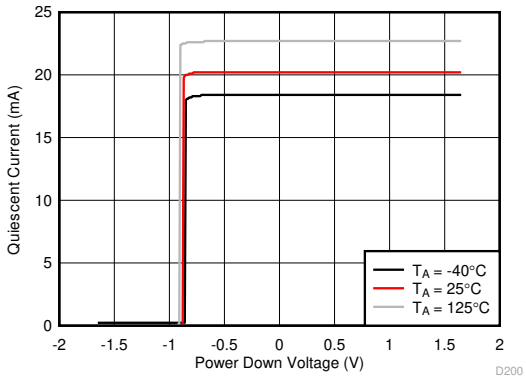


図 8-9. Switching Threshold ($\overline{PD}$ Pin Swept from High to Low)

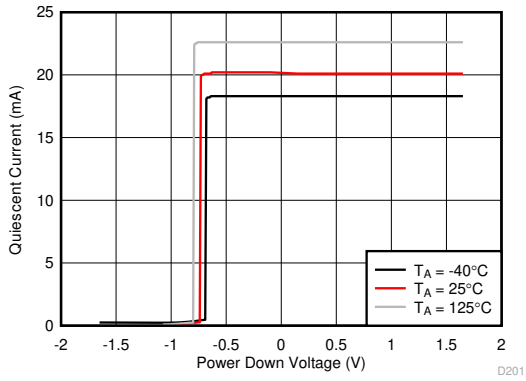


図 8-10. Switching Threshold ($\overline{PD}$ Pin Swept from Low to High)

Connecting the $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback (R_F) and gain (R_G) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA859-Q1 uses internal, back-to-back protection diodes between the inverting and noninverting input pins as 図 8-3 shows. In the power-down state, if the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the noninverting input pin and the output pin.

9 Application and Implementation

注

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9.1 Application Information

The OPA859-Q1 offers high input impedance, very high-bandwidth, high slew-rate, low noise, and better than –60 dBc of distortion performance at frequencies up to 100 MHz. These features make this device an excellent front-end buffer in high-speed data acquisition systems. The wide bandwidth also makes this amplifier an excellent choice for high-gain active filter systems.

9.2 Typical Application

図 9-1 shows the OPA859-Q1 configured as a transimpedance amplifier (U1) in a wide-bandwidth, optical front-end system. A second OPA859-Q1 configured as a unity-gain buffer (U2) sets a dc offset voltage to the THS4520. The THS4520 is used to convert the single-ended transimpedance output of the OPA859-Q1 into a differential output signal. The THS4520 drives the input of the ADS54J64, 14-bit, 1-GSPS analog-to-digital converter (ADC) that digitizes the analog signal.

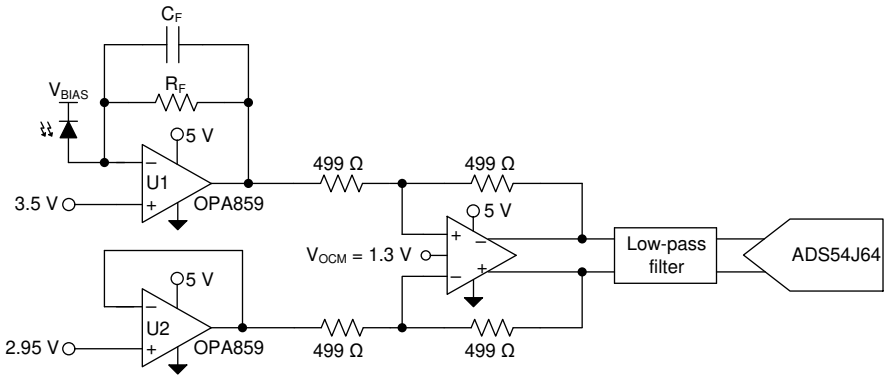


図 9-1. OPA859-Q1 as Both a TIA and a Buffer in an Optical Front-End System

9.2.1 Design Requirements

The objective is to design a low noise, wideband optical front-end system using the OPA859-Q1 as a transimpedance amplifier. The design requirements are:

- Amplifier supply voltage: 5 V
- TIA common-mode voltage: 3.5 V
- THS4520 gain: 1 V/V
- ADC input common-mode voltage: 1.3 V
- ADC analog differential input range: 1.1 V_{PP}

9.2.2 Detailed Design Procedure

The OPA859-Q1 meets the growing demand for wideband, low-noise photodiode amplifiers. The closed-loop bandwidth of a transimpedance amplifier is a function of the following:

1. The total input capacitance (C_{IN}). This total includes the photodiode capacitance, the input capacitance of the amplifier (common-mode and differential capacitance) and any stray capacitance from the PCB.

2. The op amp gain bandwidth product (GBWP).
3. The transimpedance gain (R_F).

図 9-1 shows the OPA859-Q1 configured as a TIA, with the avalanche photodiode (APD) reverse biased so that the APD cathode is tied to a large positive bias voltage. In this configuration, the APD sources current into the op amp feedback loop so that the output swings in a negative direction relative to the input common-mode voltage. To maximize the output swing in the negative direction, the OPA859-Q1 common-mode voltage is set close to the positive limit; only 1.5 V from the positive supply rail. The feedback resistance (R_F) and the input capacitance (C_{IN}) form a zero in the noise gain that results in instability if left unchecked. To counteract the effect of the zero, a pole is inserted into the noise gain transfer function by adding the feedback capacitor (C_F).

The *Transimpedance Considerations for High-Speed Amplifiers Application Report* discusses theories and equations that show how to compensate a transimpedance amplifier for a particular transimpedance gain and input capacitance. The bandwidth and compensation equations from the application report are available in an Excel® calculator. *What You Need To Know About Transimpedance Amplifiers – Part 1* provides a link to the calculator.

The equations and calculators in the referenced application report and blog posts are used to model the bandwidth (f_{-3dB}) and noise (I_{RN}) performance of the OPA859-Q1 configured as a TIA. The resultant performance is shown in 図 9-2 and 図 9-3. The left-side Y-axis shows the closed-loop bandwidth performance, whereas the right side of the graph shows the integrated input-referred noise. The noise bandwidth to calculate I_{RN} for a fixed R_F and C_{PD} is set equal to the f_{-3dB} frequency. 図 9-2 shows the amplifier performance as a function of photodiode capacitance (C_{PD}) for R_F = 10 kΩ and 20 kΩ. Increasing C_{PD} decreases the closed-loop bandwidth. To maximize bandwidth, make sure to reduce any stray parasitic capacitance from the PCB. The OPA859-Q1 is designed with 0.8 pF of total input capacitance to minimize the effect of stray capacitance on system performance. 図 9-3 shows the amplifier performance as a function of R_F for C_{PD} = 1 pF and 2 pF. Increasing R_F results in lower bandwidth. To maximize the signal-to-noise ratio (SNR) in an optical front-end system, maximize the gain in the TIA stage. Increasing R_F by a factor of X increases the signal level by X, but only increases the resistor noise contribution by √X, thereby improving SNR.

The OPA859-Q1 configured as a unity-gain buffer drives a dc offset voltage of 2.95 V into the lower half of the THS4520. To maximize the dynamic range of the ADC, the two OPA859 amplifiers drive a differential common-mode of 3.5 V and 2.95 V into the THS4520. The dc offset voltage of the buffer amplifier can be derived using 式 1.

$$V_{BUF\_DC} = V_{TIA\_CM} - \left(\frac{1}{2} \times \frac{V_{ADC\_DIFF\_IN}}{\left(\frac{R_F}{R_G} \right)} \right) \quad (1)$$

where

- V_{TIA_CM} is the common-mode voltage of the TIA (3.5 V)
- $V_{ADC\_DIFF\_IN}$ is the differential input voltage range of the ADC (1.1 V_{PP})
- R_F and R_G are the feedback resistance (499 Ω) and gain resistance (499 Ω) of the THS4520 differential amplifier

The low-pass filter between the THS4520 and the ADC54J64 minimizes high-frequency noise and maximizes SNR. The ADC54J64 has an internal buffer that isolates the output of the THS4520 from the ADC sampling-capacitor input, so a traditional charge bucket filter is not required.

9.2.3 Application Curves

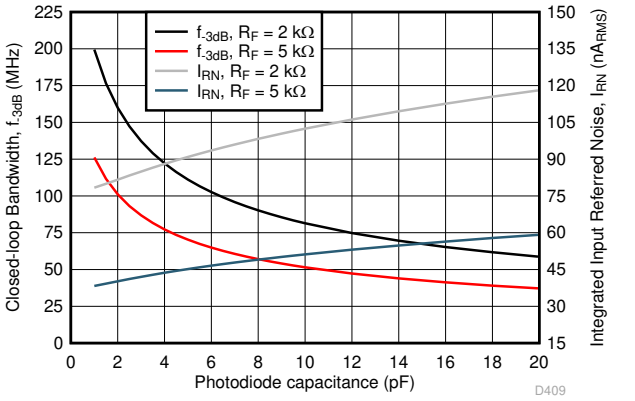


図 9-2. Bandwidth and Noise vs Photodiode Capacitance

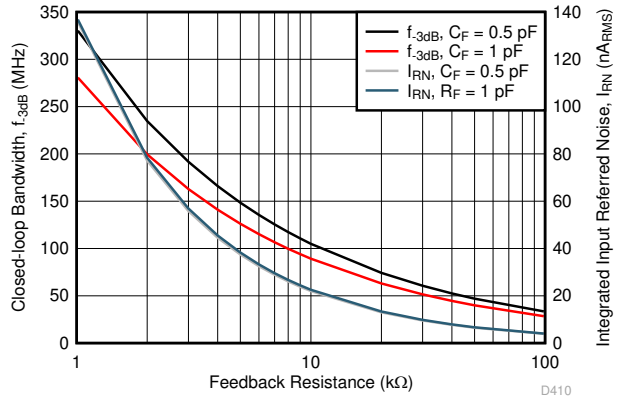
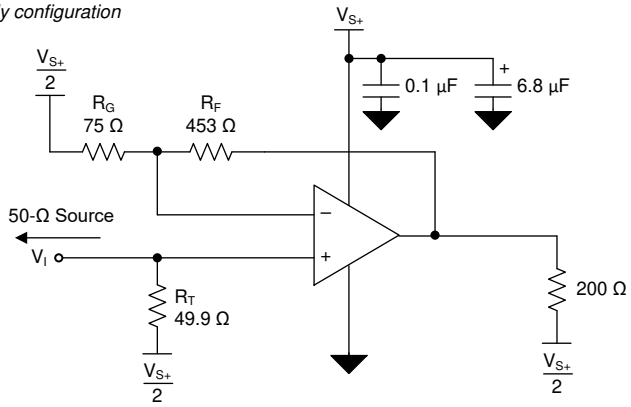


図 9-3. Bandwidth and Noise vs Feedback Resistance

10 Power Supply Recommendations

The OPA859-Q1 operates on supplies from 3.3 V to 5.25 V. The OPA859-Q1 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA859-Q1 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

a) Single supply configuration



b) Split supply configuration

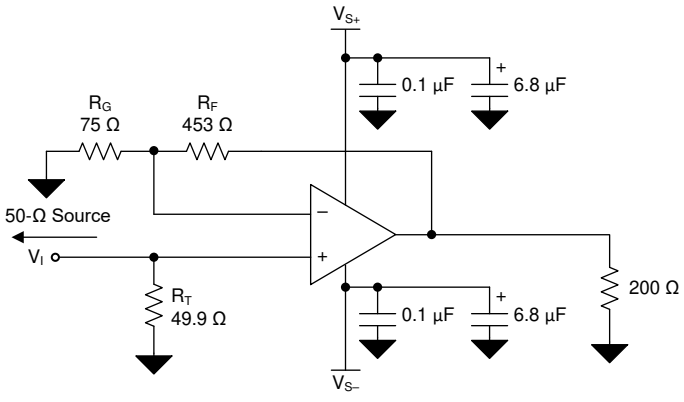


図 10-1. Split and Single Supply Circuit Configuration , Gain = 7 V/V

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA859-Q1 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is less than 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
- **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).
- **Careful selection and placement of external components preserves the high-frequency performance of the OPA859-Q1.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wirewound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. When configuring the OPA859-Q1 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

11.2 Layout Example

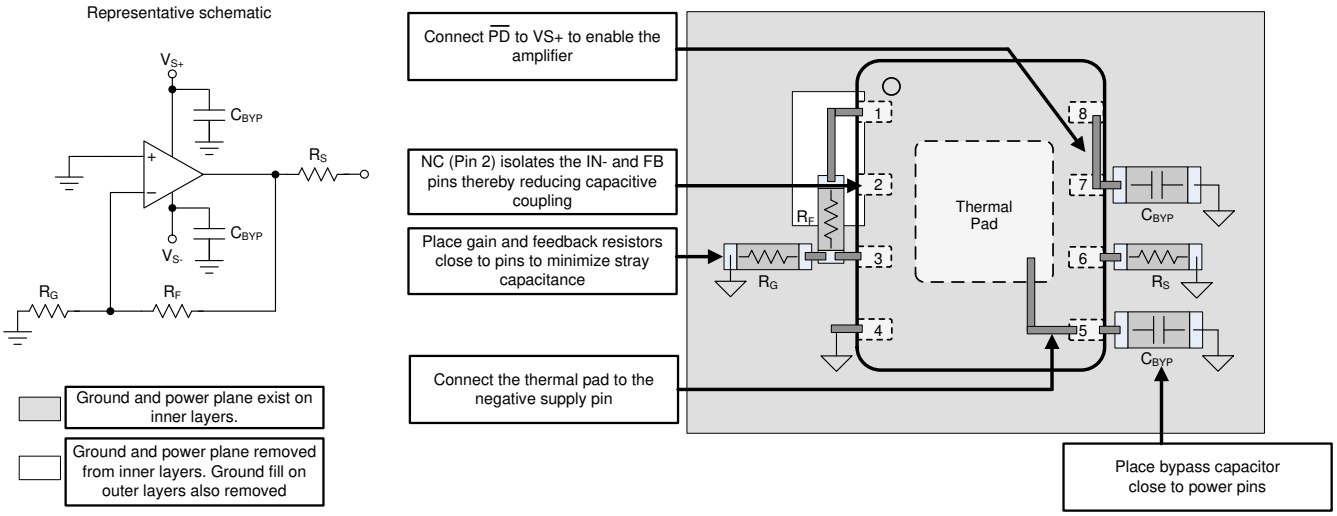


図 11-1. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- *LIDAR Pulsed Time of Flight Reference Design*
- *LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters*
- *Wide Bandwidth Optical Front-end Reference Design*

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA858EVM user's guide*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers application report*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments *What You Need To Know About Transimpedance Amplifiers – Part 2*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.7 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA859QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	859Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA859-Q1 :

- Catalog : OPA859

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

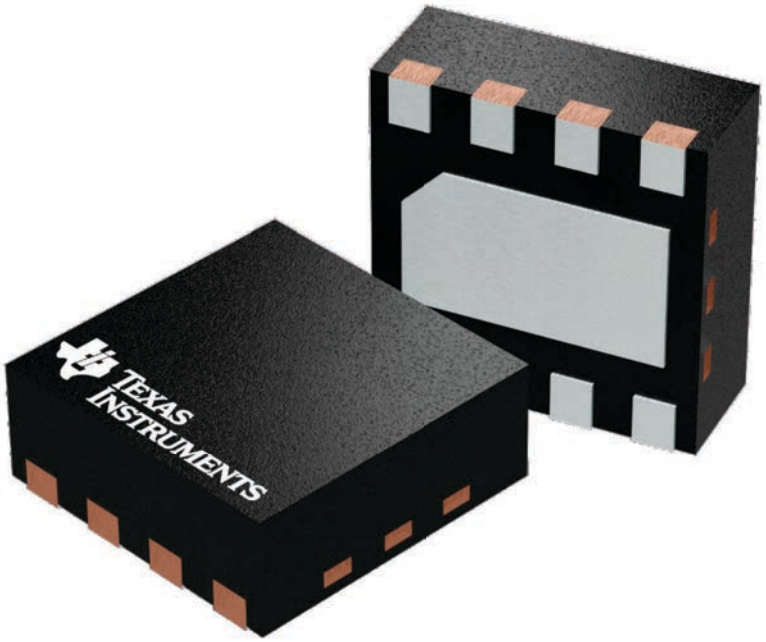
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



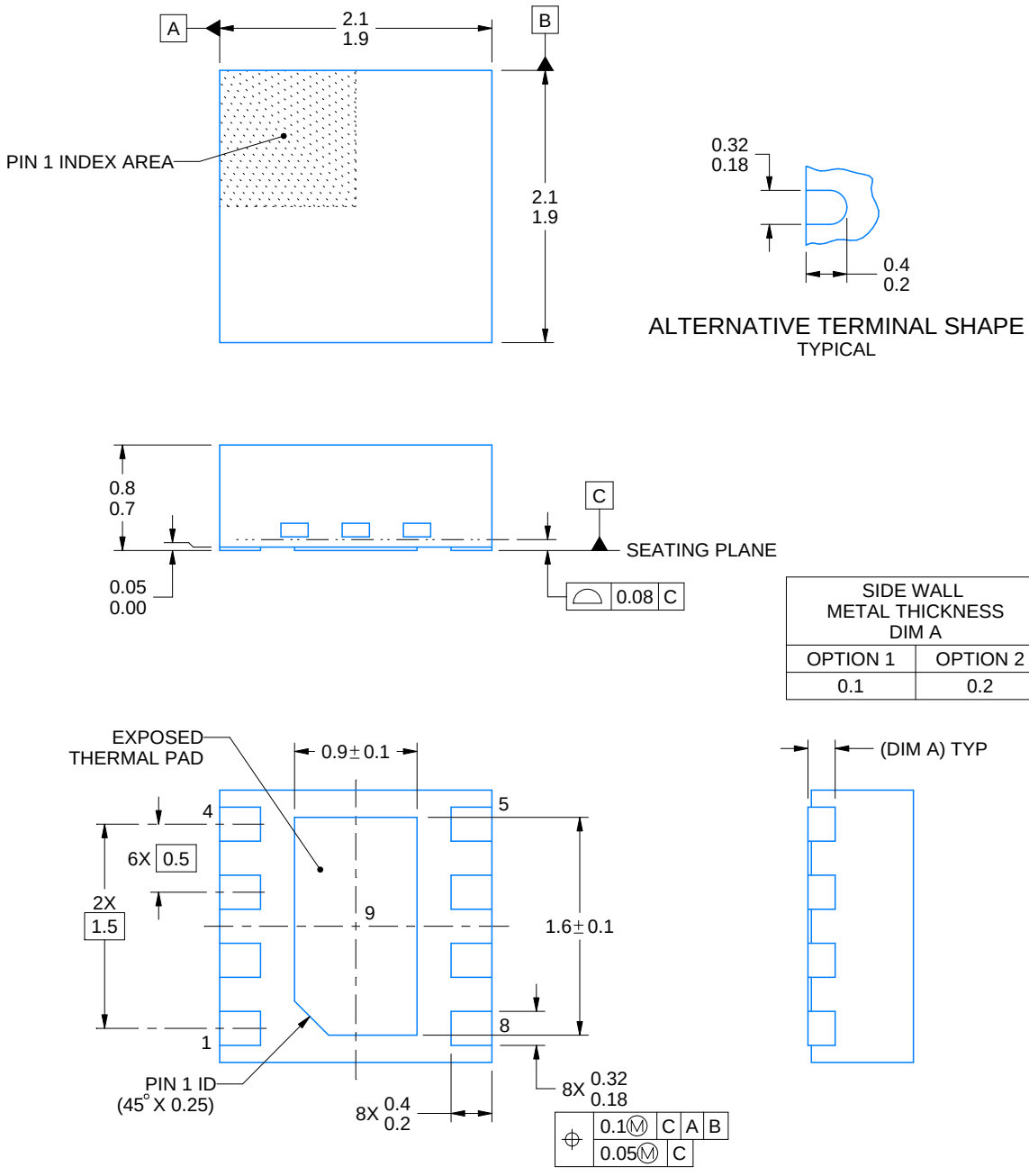
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

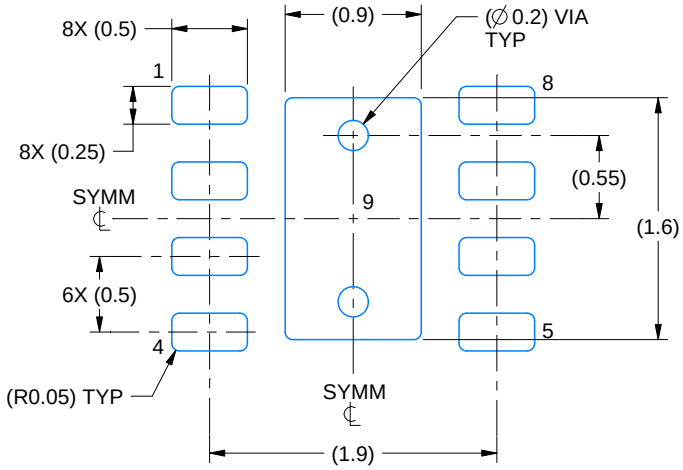
PLASTIC SMALL OUTLINE - NO LEAD



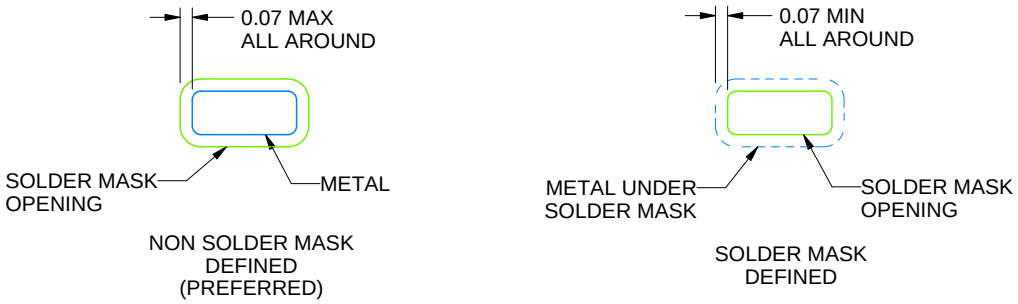
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

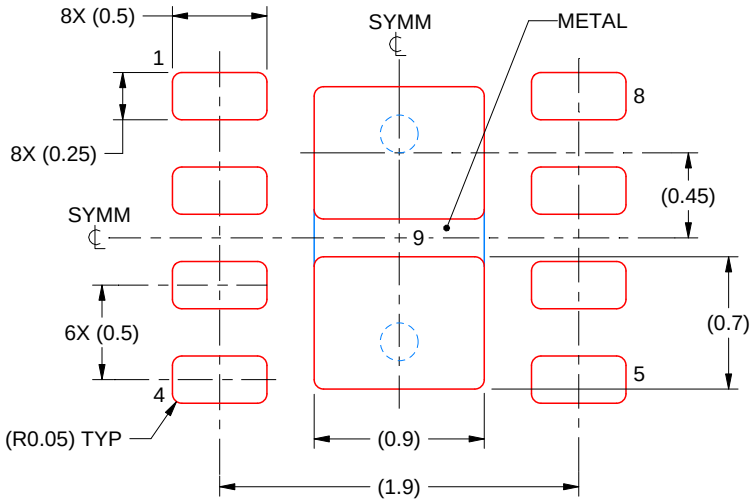


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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