

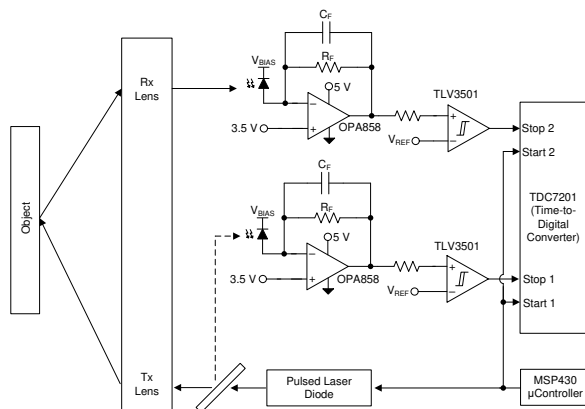
OPA858-Q1 5.5GHz ゲイン帯域幅積、7V/V ゲイン安定、FET 入力アンプ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
 - 温度グレード 1: -40°C ~ +125°C, T_A
- 高いゲイン帯域幅積: 5.5GHz
- 不完全補償型、ゲイン 7V/V 以上 (安定)
- 極めて小さいバイアス電流 MOSFET 入力: 10pA
- 小さい入力電圧ノイズ: 2.5nV/√Hz
- スルーレート: 2000V/μs
- 低い入力容量:
 - 同相: 0.6pF
 - 差動: 0.2pF
- 広い入力同相範囲:
 - 正電源から 1.4V
 - 負電源を含む
- TIA 構成で 2.5V_{pp} の出力シング
- 電源電圧範囲: 3.3V ~ 5.25V
- 静止電流: 20.5mA
- パッケージ: 8ピン WSON
- 温度範囲: -40°C ~ +125°C

2 アプリケーション

- 車載用 LIDAR
- タイム・オブ・フライト (ToF) カメラ
- 光学時間領域反射率測定 (OTDR)
- 3D スキャナ
- レーザーによる距離測定
- ソリッド・ステート・スキャン LIDAR
- 光学 ToF 位置センサ
- ドローン・ビジョン
- シリコン光電子増倍素子 (SiPM) バッファ・アンプ
- 光電子増倍管のポスト・アンプ



高速タイム・オブ・フライト・レーザ

3 概要

OPA858-Q1 は、広帯域トランスインピーダンスおよび電圧アンプ・アプリケーション用、広帯域、低ノイズの CMOS 入力オペアンプです。デバイスがトランスインピーダンス・アンプ (TIA) として構成されているとき、5.5GHz のゲイン帯域幅積 (GBWP) により、数十 kΩ から数百 kΩ までのトランスインピーダンス・ゲインで高い閉ループ帯域幅が得られます。

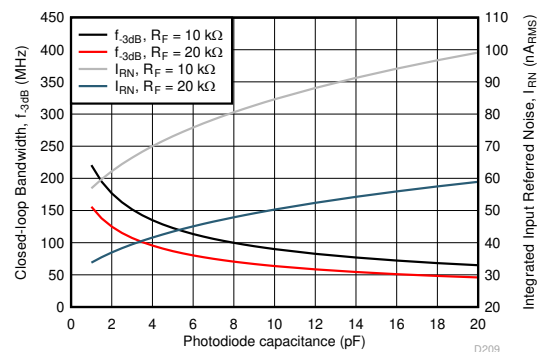
下のグラフは、アンプが TIA として構成されているときの OPA858-Q1 の帯域幅およびノイズ特性を、フォトダイオード容量の関数として示したものです。合計ノイズは、DC から左側のスケールで計算された周波数 (f) までの帯域幅の範囲にわたって計算されます。OPA858-Q1 のパッケージにはフィードバック・ピン (FB) があるため、入力と出力の間の帰還回路接続が簡単になります。

OPA858-Q1 は、OPA858-Q1 を TDC7201 などの時間 / デジタル・コンバータと組み合わせて使用する光学的タイム・オブ・フライト (ToF) システムで動作するよう最適化されています。OPA858-Q1 を使うと、THS4541-Q1 などの差動出力アンプを接続した高分解能 LIDAR システムで高速 A/D コンバータ (ADC) を駆動できます。

デバイス情報

部品番号 ⁽¹⁾	パッケージ	本体サイズ (公称)
OPA858-Q1	WSON (8)	2.00 mm × 2.00 mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。



フォトダイオード容量と帯域幅およびノイズとの関係



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4 Revision History

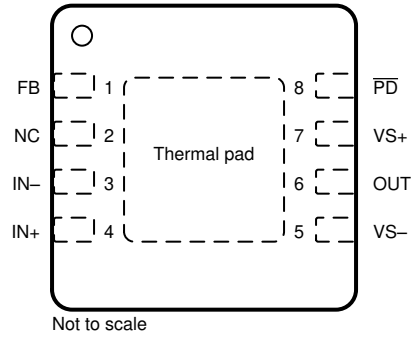
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2021	*	Initial Release

Device Comparison Table

DEVICE	INPUT TYPE	MINIMUM STABLE GAIN	VOLTAGE NOISE ($\text{nV}/\sqrt{\text{Hz}}$)	INPUT CAPACITANCE (pF)	GAIN BANDWIDTH (GHz)
OPA855-Q1	Bipolar	7 V/V	0.98	0.8	8
OPA858-Q1	CMOS	7 V/V	2.5	0.8	5.5
OPA859-Q1	CMOS	1 V/V	3.3	0.8	0.9

5 Pin Configuration and Functions



**图 5-1. DSG Package
 8-Pin WSON With Exposed Thermal Pad
 Top View**

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	1	I	Feedback connection to output of amplifier
IN-	3	I	Inverting input
IN+	4	I	Noninverting input
NC	2	—	Do not connect
OUT	6	O	Amplifier output
PD	8	I	Power down connection. \overline{PD} = logic low = power off mode; \overline{PD} = logic high = normal operation.
VS-	5	—	Negative voltage supply
VS+	7	—	Positive voltage supply
Thermal pad		—	Connect the thermal pad to VS-

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_S	Total supply voltage ($V_{S+} - V_{S-}$)		5.5	V
V_{IN+}, V_{IN-}	Input voltage	$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
V_{ID}	Differential input voltage		1	V
V_{OUT}	Output voltage	$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
I_{IN}	Continuous input current		±10	mA
I_{OUT}	Continuous output current ⁽²⁾		±100	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	± 1500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage ($V_{S+} - V_{S-}$)	3.3	5	5.25	V
T_A	Operating free-air temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA858-Q1	UNIT
		DSG (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	100	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	22.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

$V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $G = 7\text{ V/V}$, $R_F = 453\ \Omega$, input common-mode biased at midsupply, $R_L = 200\ \Omega$, output load is referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	$V_{OUT} = 100\text{ mV}_{PP}$		1.2		GHz
LSBW	Large-signal bandwidth	$V_{OUT} = 2\text{ V}_{PP}$		600		MHz
GBWP	Gain-bandwidth product			5.5		GHz
	Bandwidth for 0.1-dB flatness			130		MHz
SR	Slew rate (10% - 90%)	$V_{OUT} = 2\text{-V step}$		2000		V/ μs
t_r	Rise time	$V_{OUT} = 100\text{-mV step}$		0.3		ns
t_f	Fall time	$V_{OUT} = 100\text{-mV step}$		0.3		ns
	Settling time to 0.1%	$V_{OUT} = 2\text{-V step}$		8		ns
	Settling time to 0.001%	$V_{OUT} = 2\text{-V step}$		3000		ns
	Overshoot or undershoot	$V_{OUT} = 2\text{-V step}$		7%		
	Overdrive recovery	2x output overdrive (0.1% recovery)		200		ns
HD2	Second-order harmonic distortion	$f = 10\text{ MHz}$, $V_{OUT} = 2\text{ V}_{PP}$		88		dBc
		$f = 100\text{ MHz}$, $V_{OUT} = 2\text{ V}_{PP}$		64		
HD3	Third-order harmonic distortion	$f = 10\text{ MHz}$, $V_{OUT} = 2\text{ V}_{PP}$		86		dBc
		$f = 100\text{ MHz}$, $V_{OUT} = 2\text{ V}_{PP}$		68		
e_n	Input-referred voltage noise	$f = 1\text{ MHz}$		2.5		nV/ $\sqrt{\text{Hz}}$
Z_{OUT}	Closed-loop output impedance	$f = 1\text{ MHz}$		0.15		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain		72	75		dB
V_{OS}	Input offset voltage	$T_A = 25^\circ\text{C}$	-5	± 0.8	5	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		± 2		$\mu\text{V}/^\circ\text{C}$
I_{BN} , I_{BI}	Input bias current	$T_A = 25^\circ\text{C}$		± 0.4	5	μA
I_{BOS}	Input offset current	$T_A = 25^\circ\text{C}$		± 0.01	5	μA
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 0.5\text{ V}$, referenced to midsupply	70	90		dB
INPUT						
	Common-mode input resistance			1		G Ω
C_{CM}	Common-mode input capacitance			0.62		pF
	Differential input resistance			1		G Ω
C_{DIFF}	Differential input capacitance			0.2		pF
V_{IH}	Common-mode input range (high)	CMRR > 66 dB, $V_{S+} = 3.3\text{ V}$	1.7	1.9		V
V_{IL}	Common-mode input range (low)	CMRR > 66 dB, $V_{S+} = 3.3\text{ V}$		0	0.4	V
V_{IH}	Common-mode input range (high)	CMRR > 66 dB	3.4	3.6		V
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$, CMRR > 66 dB		3.3		
V_{IL}	Common-mode input range (low)	CMRR > 66 dB		0	0.4	V
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$, CMRR > 66 dB		0.35		
OUTPUT						
V_{OH}	Output voltage (high)	$T_A = 25^\circ\text{C}$, $V_{S+} = 3.3\text{ V}$	2.3	2.4		V
V_{OH}	Output voltage (high)	$T_A = 25^\circ\text{C}$	3.95	4.1		V
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		3.9		
V_{OL}	Output voltage (low)	$T_A = 25^\circ\text{C}$, $V_{S+} = 3.3\text{ V}$		1.05	1.15	V
V_{OL}	Output voltage (low)	$T_A = 25^\circ\text{C}$		1.05	1.15	V
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		1.2		

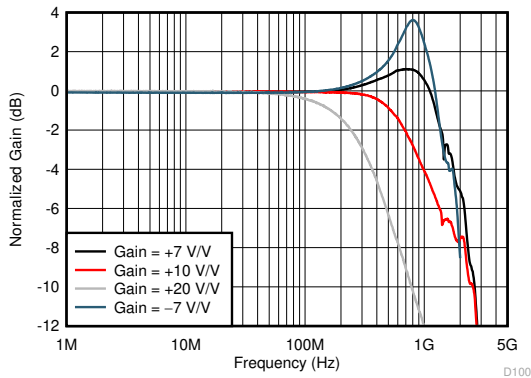
6.5 Electrical Characteristics (continued)

$V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $G = 7\text{ V/V}$, $R_F = 453\ \Omega$, input common-mode biased at midsupply, $R_L = 200\ \Omega$, output load is referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Linear output drive (sink and source)	$R_L = 10\ \Omega$, $A_{OL} > 60\text{ dB}$	65	80		mA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $R_L = 10\ \Omega$, $A_{OL} > 60\text{ dB}$		64		
I_{SC}	Output short-circuit current		85	105		mA
POWER SUPPLY						
V_S	Operating voltage		3.3		5.25	V
I_Q	Quiescent current	$V_{S+} = 5\text{ V}$	18	20.5	24	mA
I_Q	Quiescent current	$V_{S+} = 3.3\text{ V}$	17.5	20	23.5	mA
I_Q	Quiescent current	$V_{S+} = 5.25\text{ V}$	18	21	24	mA
I_Q	Quiescent current	$T_A = 125^\circ\text{C}$		24.5		mA
I_Q	Quiescent current	$T_A = -40^\circ\text{C}$		18.5		mA
PSRR+	Positive power-supply rejection ratio		74	84		dB
PSRR-	Negative power-supply rejection ratio		70	80		
POWER DOWN						
	Disable voltage threshold	Amplifier OFF below this voltage	0.65	1		V
	Enable voltage threshold	Amplifier ON above this voltage		1.5	1.8	V
	Power-down quiescent current			70	140	μA
	PD bias current			70	200	μA
	Turnon time delay	Time to $V_{OUT} = 90\%$ of final value		13		ns
	Turnoff time delay			120		ns

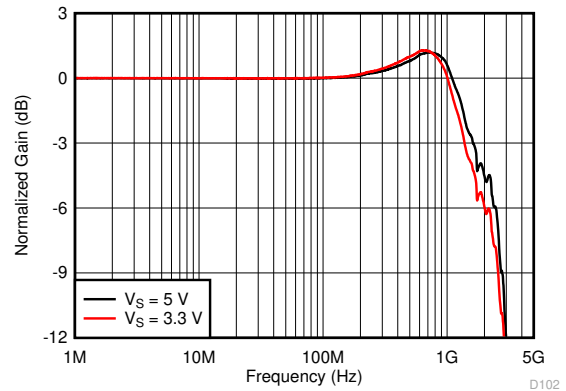
6.6 Typical Characteristics

at $V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{IN+} = 0\text{ V}$, $R_F = 453\ \Omega$, Gain = 7 V/V, $R_L = 200\ \Omega$, output load referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



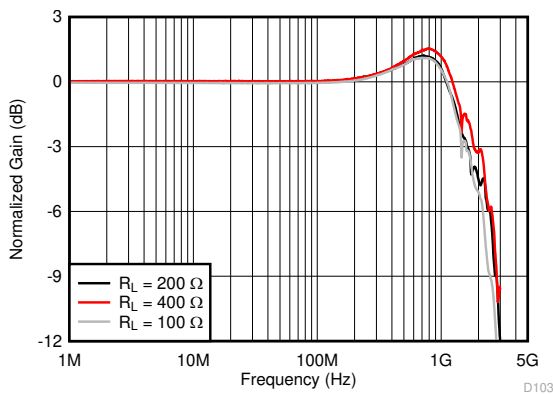
$V_{OUT} = 100\text{ mV}_{PP}$; see [7-1](#) and [7-2](#) for circuit configuration

6-1. Small-Signal Frequency Response vs Gain



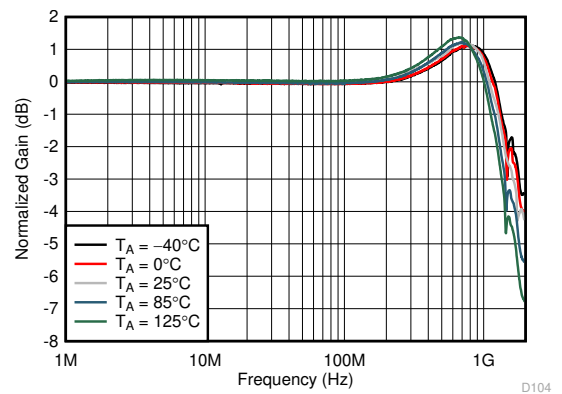
$V_{OUT} = 100\text{ mV}_{PP}$

6-2. Small-Signal Frequency Response vs Supply Voltage



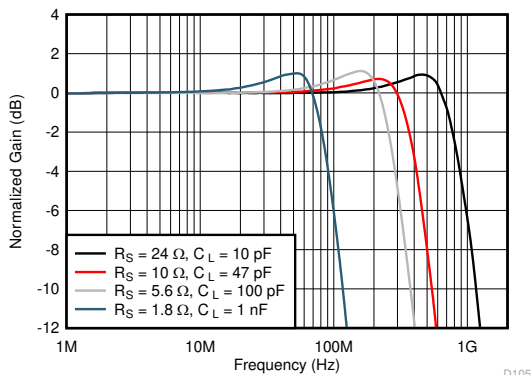
$V_{OUT} = 100\text{ mV}_{PP}$

6-3. Small-Signal Frequency Response vs Output Load



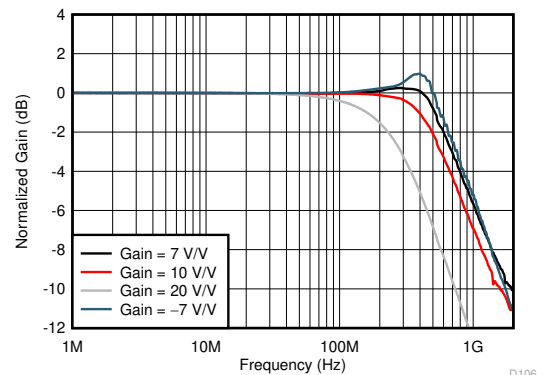
$V_{OUT} = 100\text{ mV}_{PP}$

6-4. Small-Signal Frequency Response vs Ambient Temperature



$V_{OUT} = 100\text{ mV}_{PP}$; see [7-3](#) for circuit configuration

6-5. Small-Signal Frequency Response vs Capacitive Load

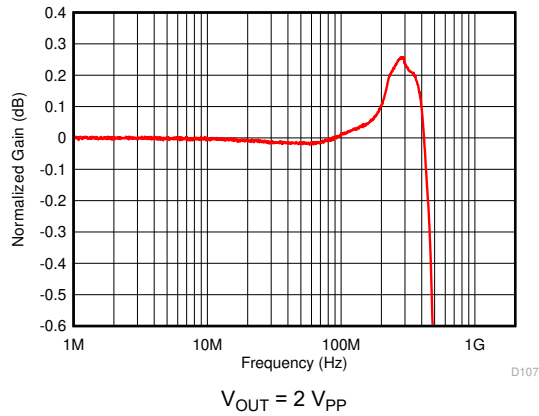


$V_{OUT} = 2\text{ V}_{PP}$

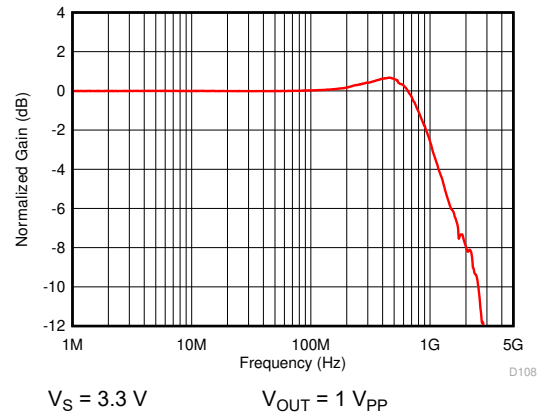
6-6. Large-Signal Frequency Response vs Gain

6.6 Typical Characteristics (continued)

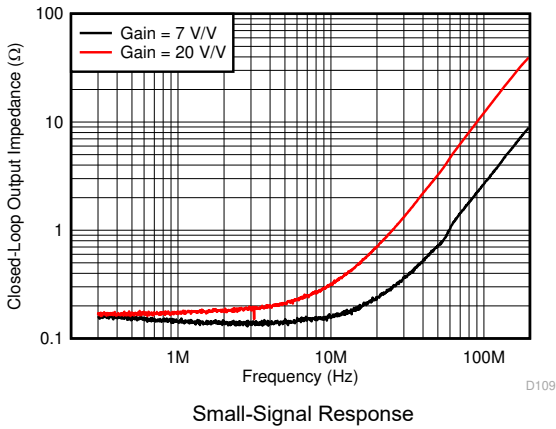
at $V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{IN+} = 0\text{ V}$, $R_F = 453\ \Omega$, Gain = 7 V/V, $R_L = 200\ \Omega$, output load referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



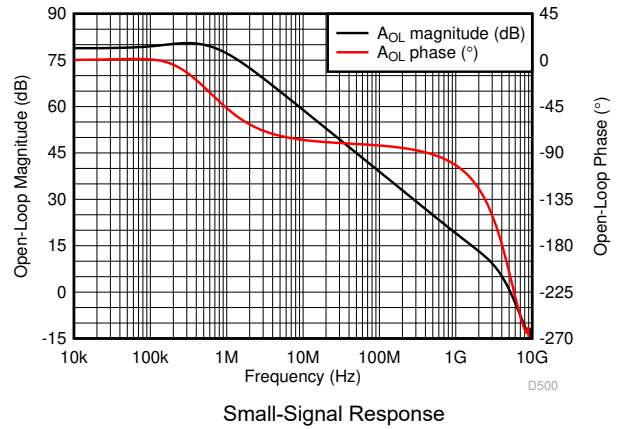
6-7. Large-Signal Response for 0.1-dB Gain Flatness



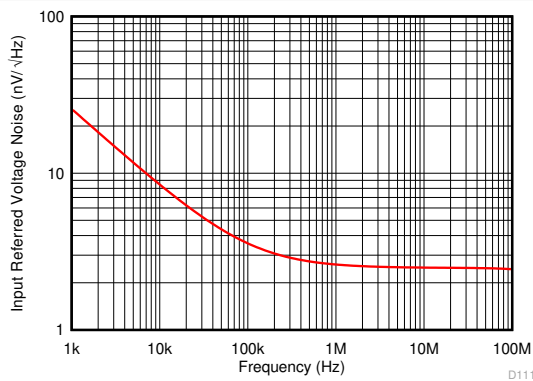
6-8. Large-Signal Frequency Response



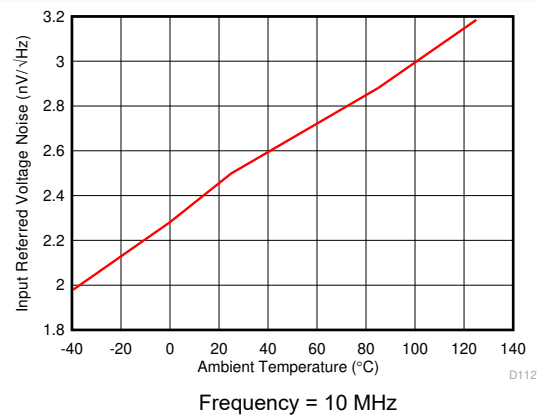
6-9. Closed-Loop Output Impedance vs Frequency



6-10. Open-Loop Magnitude and Phase vs Frequency



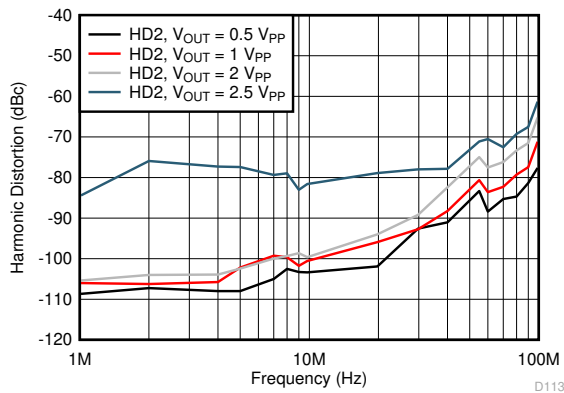
6-11. Voltage Noise Density vs Frequency



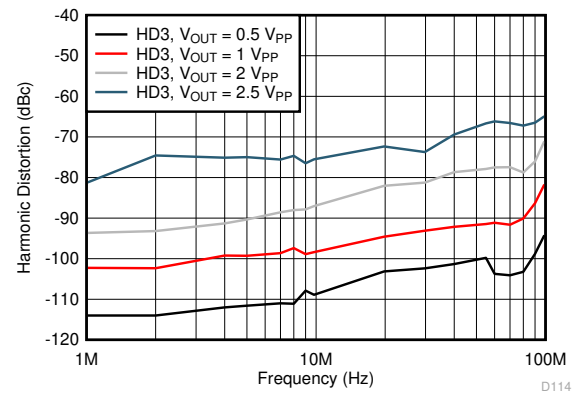
6-12. Voltage Noise Density vs Ambient Temperature

6.6 Typical Characteristics (continued)

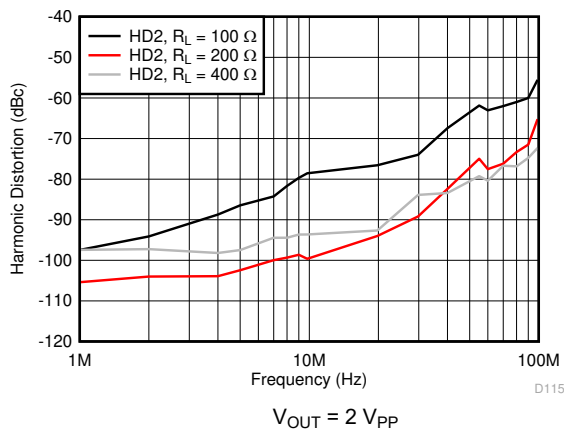
at $V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{IN+} = 0\text{ V}$, $R_F = 453\ \Omega$, Gain = 7 V/V , $R_L = 200\ \Omega$, output load referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



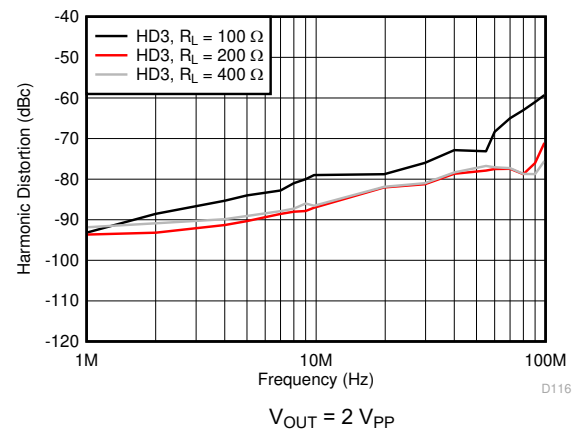
6-13. Harmonic Distortion (HD2) vs Output Swing



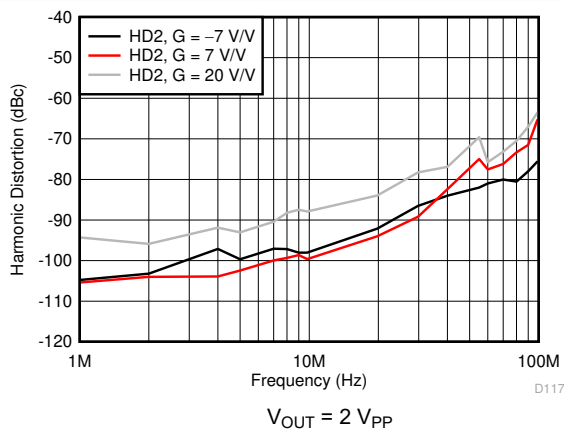
6-14. Harmonic Distortion (HD3) vs Output Swing



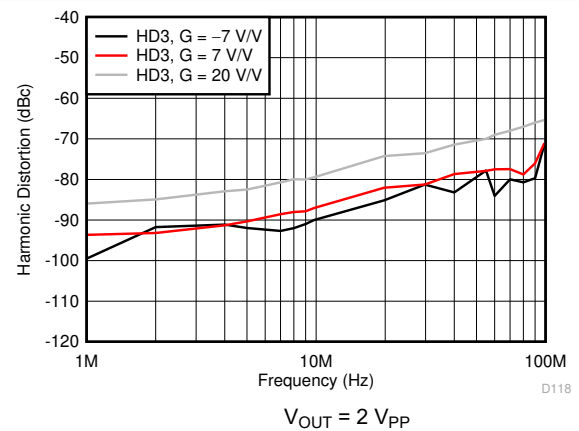
6-15. Harmonic Distortion (HD2) vs Output Load



6-16. Harmonic Distortion (HD3) vs Output Load



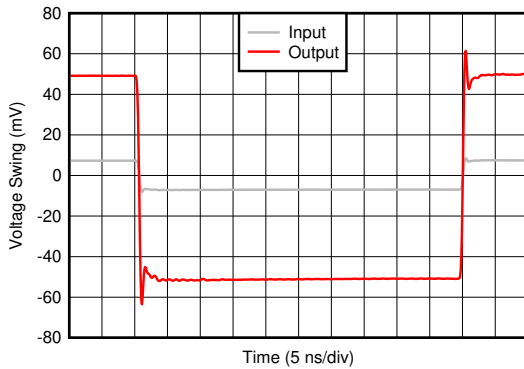
6-17. Harmonic Distortion (HD2) vs Gain



6-18. Harmonic Distortion (HD3) vs Gain

6.6 Typical Characteristics (continued)

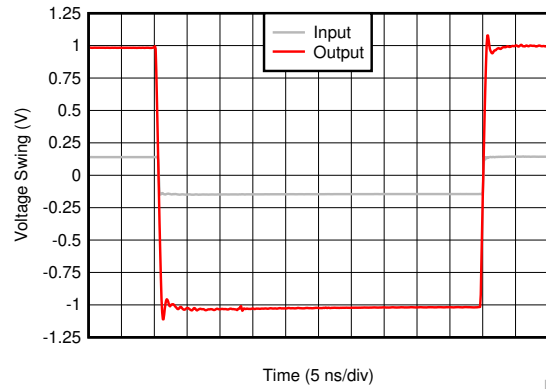
at $V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{IN+} = 0\text{ V}$, $R_F = 453\ \Omega$, Gain = 7 V/V, $R_L = 200\ \Omega$, output load referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



D119

Average Rise and Fall Time (10% - 90%) = 450 ps

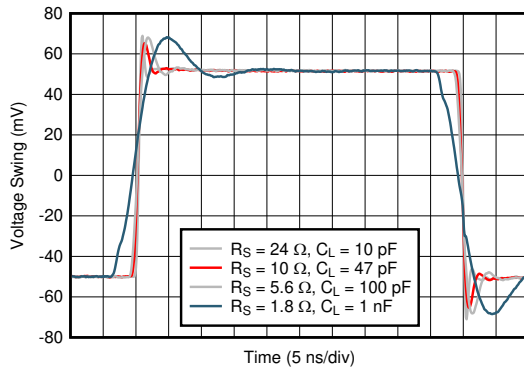
Figure 6-19. Small-Signal Transient Response



D120

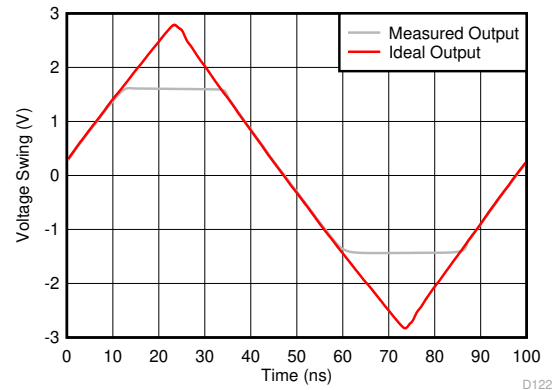
Average Rise and Fall Time (10% - 90%) = 750 ps

Figure 6-20. Large-Signal Transient Response



D121

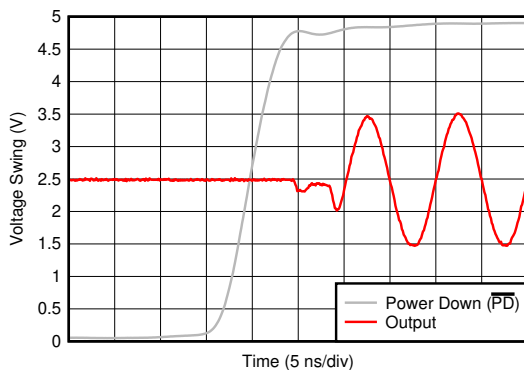
Figure 6-21. Small-Signal Transient Response vs Capacitive Load



D122

2x Output Overdrive

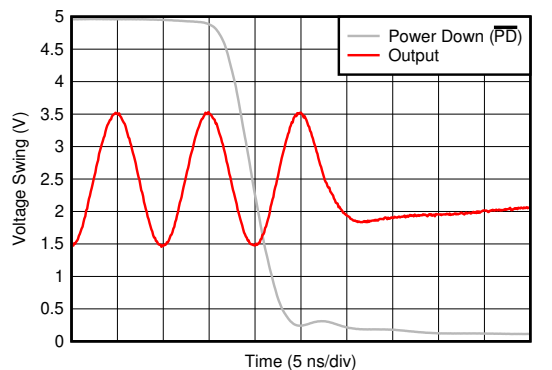
Figure 6-22. Output Overload Response



D123

$V_{S+} = 5\text{ V}$, $V_{S-} = \text{Ground}$

Figure 6-23. Turnon Transient Response



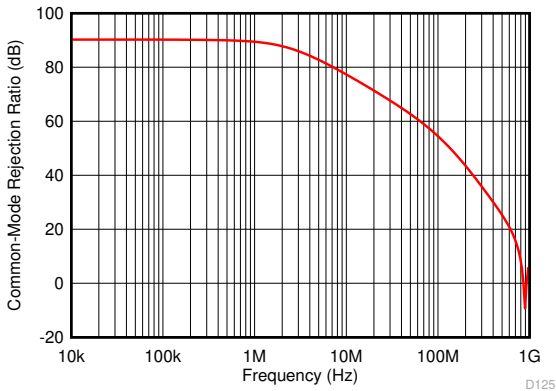
D124

$V_{S+} = 5\text{ V}$, $V_{S-} = \text{Ground}$

Figure 6-24. Turnoff Transient Response

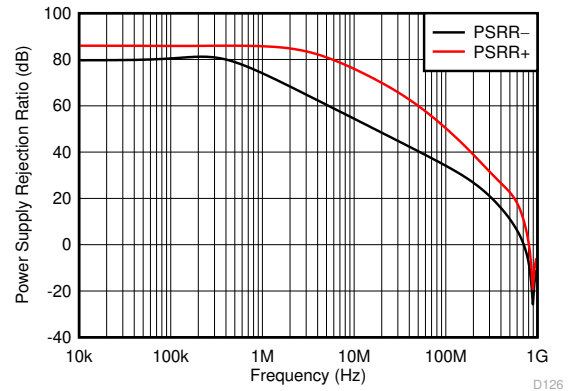
6.6 Typical Characteristics (continued)

at $V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{IN+} = 0\text{ V}$, $R_F = 453\ \Omega$, Gain = 7 V/V, $R_L = 200\ \Omega$, output load referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



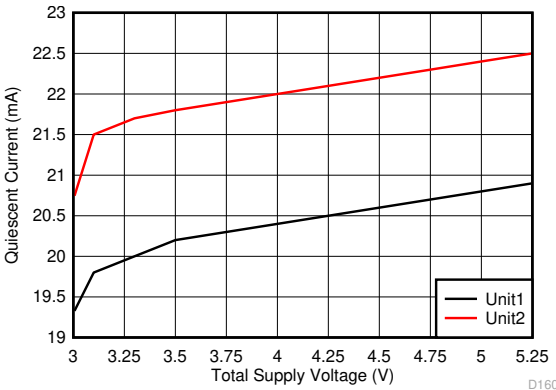
Small-Signal Response

6-25. Common-Mode Rejection Ratio vs Frequency



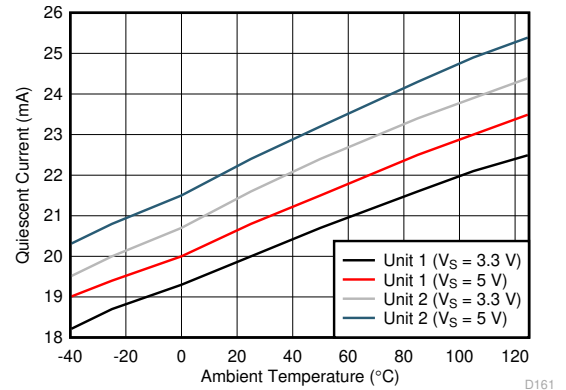
Small-Signal Response

6-26. Power Supply Rejection Ratio vs Frequency



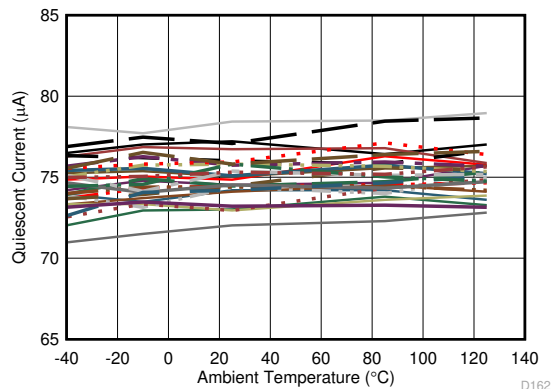
2 Typical Units

6-27. Quiescent Current vs Supply Voltage



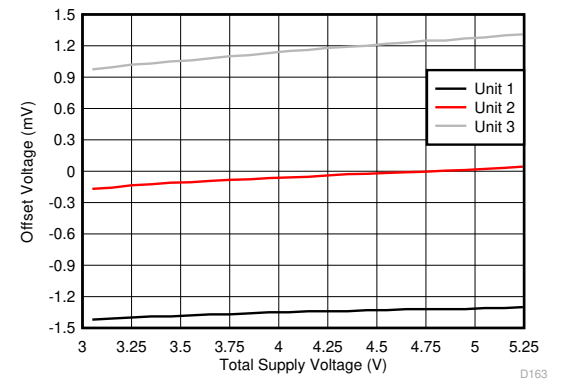
2 Typical Units

6-28. Quiescent Current vs Ambient Temperature



30 Units Tested

6-29. Quiescent Current (Amplifier Disabled) vs Ambient Temperature



3 Typical Units

6-30. Offset Voltage vs Supply Voltage

6.6 Typical Characteristics (continued)

at $V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{IN+} = 0\text{ V}$, $R_F = 453\ \Omega$, Gain = 7 V/V , $R_L = 200\ \Omega$, output load referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

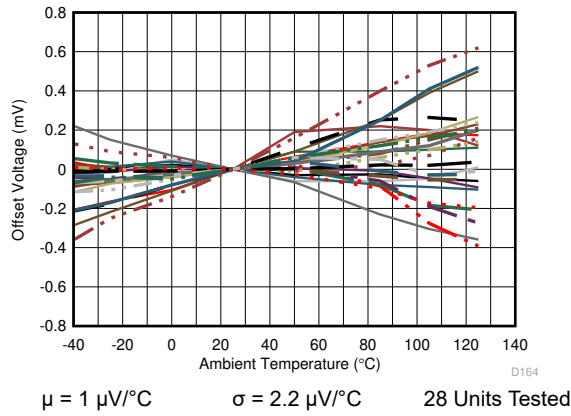


Fig 6-31. Offset Voltage vs Ambient Temperature

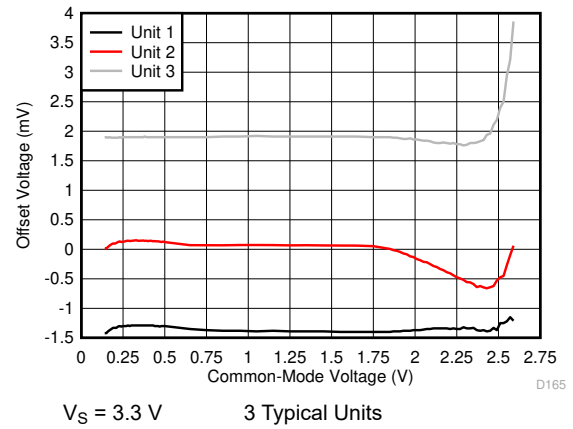


Fig 6-32. Offset Voltage vs Input Common-Mode Voltage

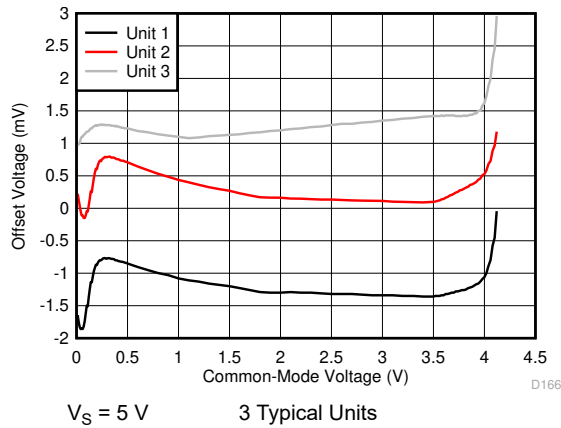


Fig 6-33. Offset Voltage vs Input Common-Mode Voltage

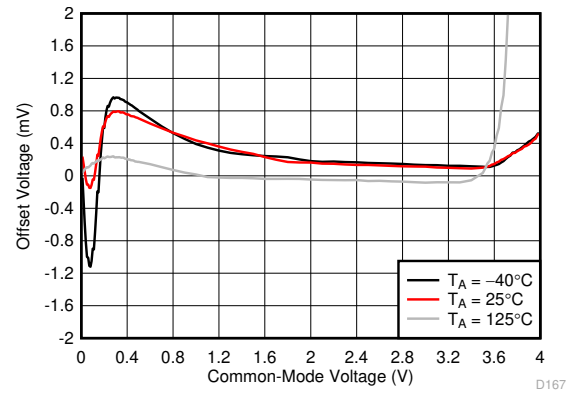


Fig 6-34. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature

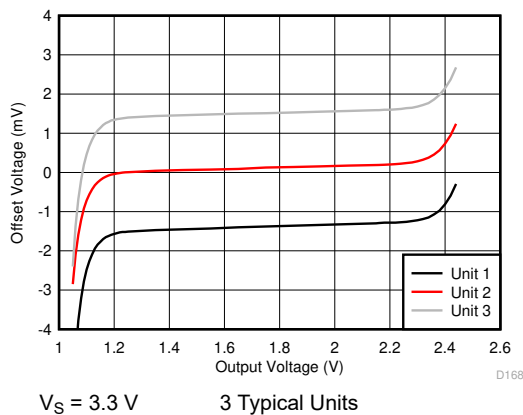


Fig 6-35. Offset Voltage vs Output Swing

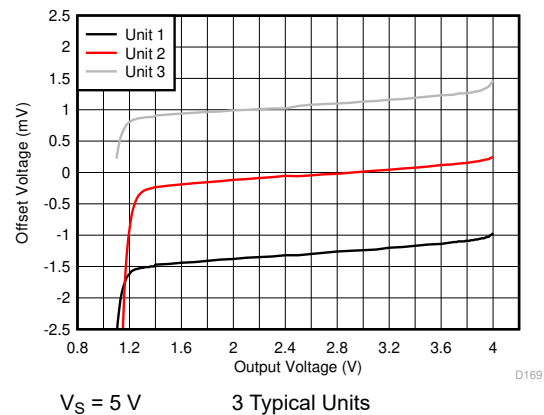
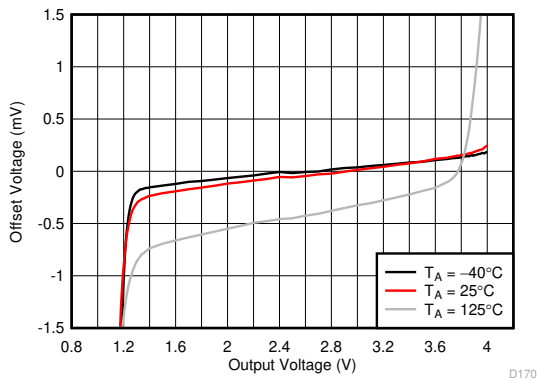


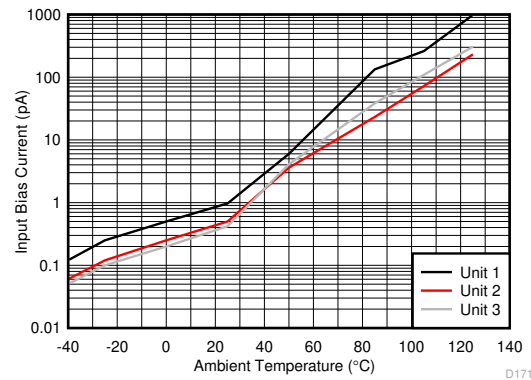
Fig 6-36. Offset Voltage vs Output Swing

6.6 Typical Characteristics (continued)

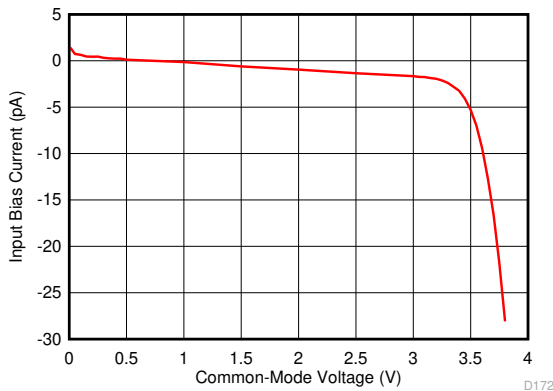
at $V_{S+} = 2.5\text{ V}$, $V_{S-} = -2.5\text{ V}$, $V_{IN+} = 0\text{ V}$, $R_F = 453\ \Omega$, Gain = 7 V/V, $R_L = 200\ \Omega$, output load referenced to midsupply, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



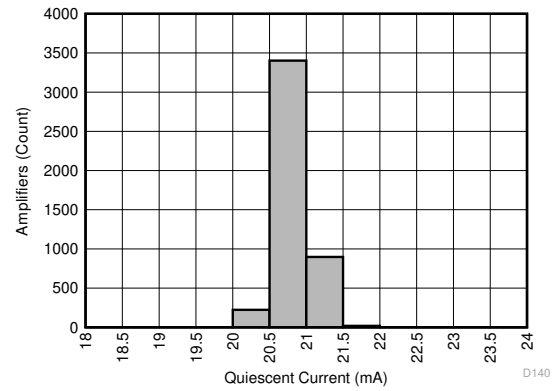
6-37. Offset Voltage vs Output Swing vs Ambient Temperature



6-38. Input Bias Current vs Ambient Temperature

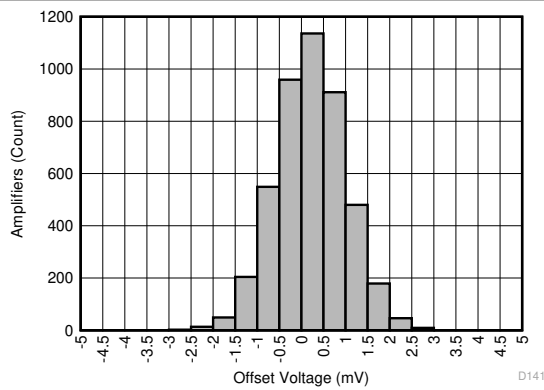


6-39. Input Bias Current vs Input Common-Mode Voltage



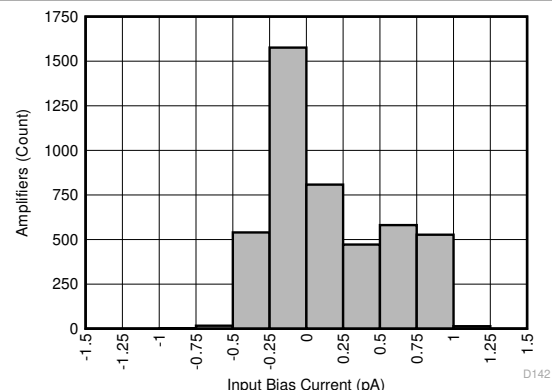
$\mu = 20.35\text{ mA}$ $\sigma = 0.2\text{ mA}$ 4555 units tested

6-40. Quiescent Current Distribution



$\mu = -0.28\text{ mV}$ $\sigma = 0.8\text{ mV}$ 4555 units tested

6-41. Offset Voltage Distribution



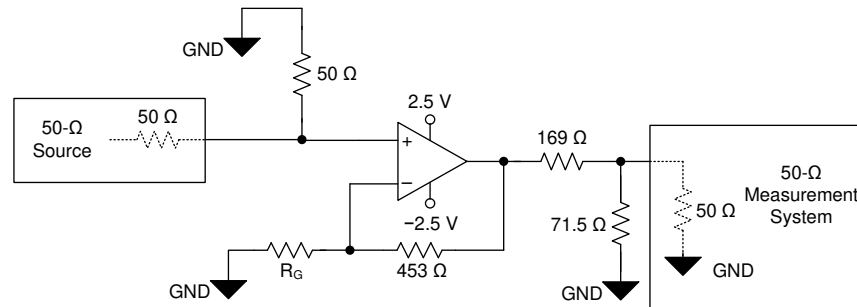
$\mu = -0.1\text{ pA}$ $\sigma = 0.39\text{ pA}$ 4555 units tested

6-42. Input Bias Current Distribution

7 Parameter Measurement Information

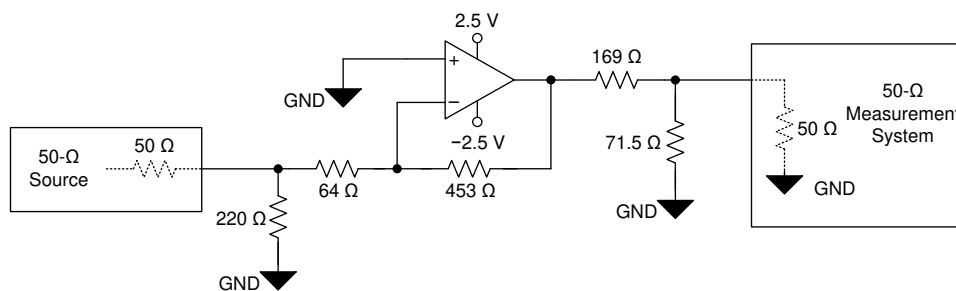
The various test setup configurations for the OPA858-Q1 are shown in [7-1](#), [7-2](#), and [7-3](#). When configuring the OPA858-Q1 in a gain of +39.2 V/V, feedback resistor R_F was set to 953 Ω .

[6-1](#) shows 5-dB of peaking with the amplifier in an inverting configuration of -7 V/V with the amplifier configured as shown in [7-2](#). The 50- Ω matched termination of this circuit configuration results in the amplifier being configured in a noise gain of 5.3 V/V, which is lower than the recommended +7 V/V.

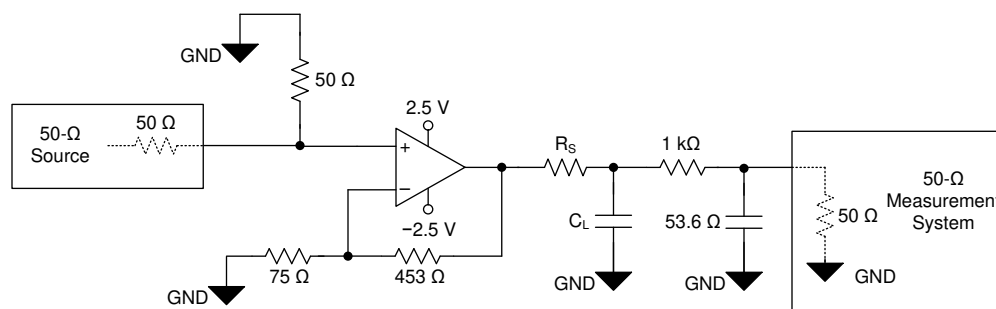


R_G values depend on gain configuration

7-1. Noninverting Configuration



7-2. Inverting Configuration (Gain = -7 V/V)



7-3. Capacitive Load Driver Configuration

8 Detailed Description

8.1 Overview

The ultra-wide, 5.5-GHz gain bandwidth product (GBWP) of the OPA858-Q1, combined with the broadband voltage noise of $2.5 \text{ nV}/\sqrt{\text{Hz}}$, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA858-Q1 combines multiple features to optimize dynamic performance. In addition to the wide, small-signal bandwidth, the OPA858-Q1 has 600 MHz of large-signal bandwidth ($V_{\text{OUT}} = 2 V_{\text{PP}}$), and a slew rate of $2000 \text{ V}/\mu\text{s}$.

The OPA858-Q1 is offered in a 2-mm × 2-mm, 8-pin WSON package that features a feedback (FB) pin for a simple feedback network connection between the amplifiers output and inverting input. Excess capacitance on an amplifiers input pin can reduce phase margin causing instability. This problem is exacerbated in the case of very wideband amplifiers like the OPA858-Q1. To reduce the effects of stray capacitance on the input node, the OPA858-Q1 pinout features an isolation pin (NC) between the feedback and inverting input pins that increases the physical spacing between them thereby reducing parasitic coupling at high frequencies. The OPA858-Q1 also features a very low capacitance input stage with only 0.8-pF of total input capacitance.

8.2 Functional Block Diagram

The OPA858-Q1 is a classic voltage feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, like the two basic options shown in [Figure 8-1](#) and [Figure 8-2](#). The DC operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically connected to ground in split-supply applications.

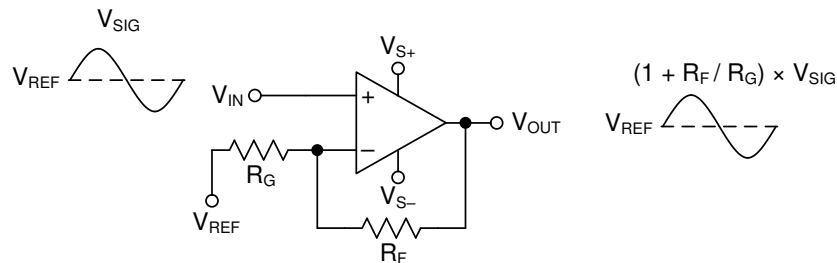


Figure 8-1. Noninverting Amplifier

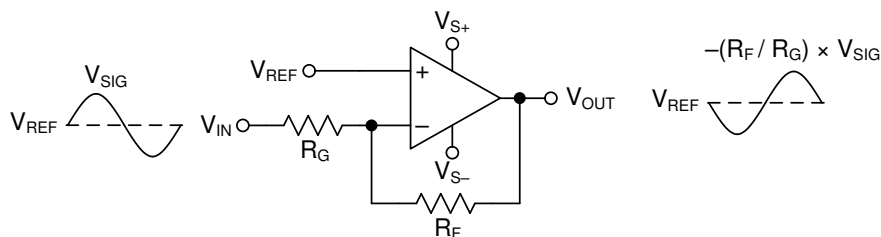


Figure 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input and ESD Protection

The OPA858-Q1 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as [Figure 8-3](#) shows. There are two antiparallel diodes between the inputs of the amplifier that clamp the inputs during an overrange or fault condition.

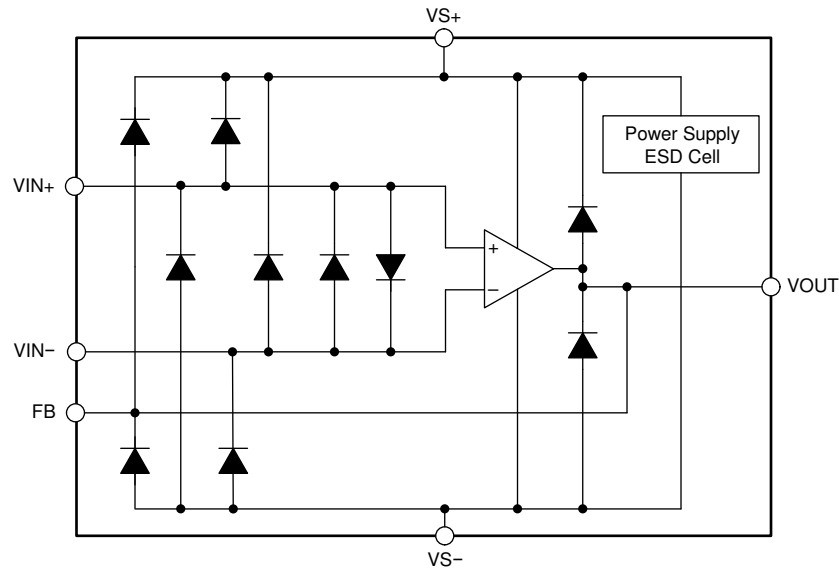


Figure 8-3. Internal ESD Structure

8.3.2 Feedback Pin

The OPA858-Q1 pin layout is optimized to minimize parasitic inductance and capacitance, which is a critical care about in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor (R_F) can connect between the FB and IN- pin on the same side of the package (see [Figure 8-4](#)) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN- pins by increasing the physical separation between the pins.

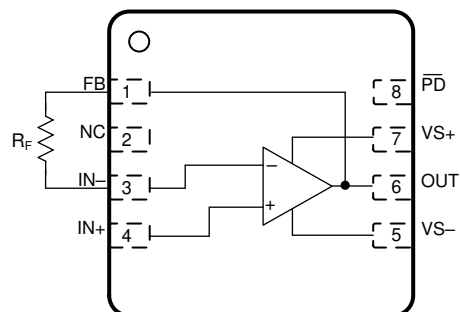


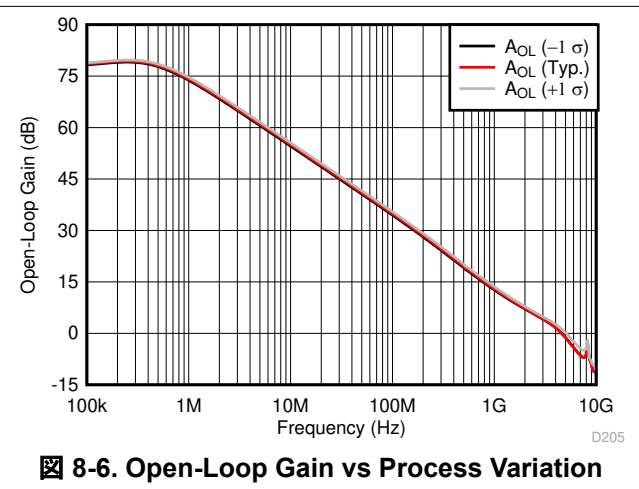
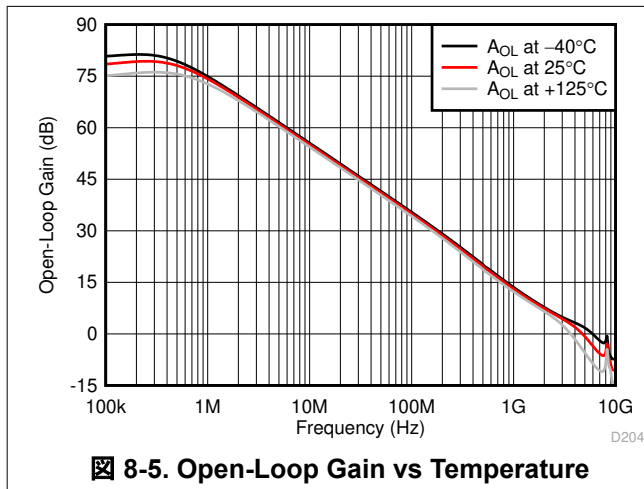
Figure 8-4. R_F Connection Between FB and IN- Pins

8.3.3 Wide Gain-Bandwidth Product

Figure 6-10 shows the open-loop magnitude and phase response of the OPA858-Q1. Calculate the gain bandwidth product of any op amp by determining the frequency at which the A_{OL} is 60 dB and multiplying that frequency by a factor of 1000. The second pole in the A_{OL} response occurs before the magnitude crosses 0 dB, and the resultant phase margin is less than 0° . This indicates instability at a gain of 0 dB (1 V/V). Amplifiers that are not unity-gain stable are known as decompensated amplifiers. Decompensated amplifiers typically have higher gain-bandwidth product, higher slew rate, and lower voltage noise, compared to a unity-gain stable amplifier with the same amount of quiescent power consumption.

Figure 8-5 shows the open-loop magnitude (A_{OL}) of the OPA858-Q1 as a function of temperature. The results show minimal variation over temperature. The phase margin of the OPA858-Q1 configured in a noise gain of 7 V/V (16.9 dB) is close to 55° across temperature. Similarly Figure 8-6 shows the A_{OL} magnitude of the OPA858-Q1 as a function of process variation. The results show the A_{OL} curve for the nominal process corner and the variation one standard deviation from the nominal. The simulated results suggest less than 1° of phase margin difference within a standard deviation of process variation when the amplifier is configured in a gain of 7 V/V.

One of the primary applications for the OPA858-Q1 is as a high-speed transimpedance amplifier (TIA), as Figure 9-4 shows. The low-frequency noise gain of a TIA is 0 dB (1 V/V). At high frequencies the ratio of the total input capacitance and the feedback capacitance set the noise gain. To maximize the TIA closed-loop bandwidth, the feedback capacitance is typically smaller than the input capacitance, which implies that the high-frequency noise gain is greater than 0 dB. As a result, op amps configured as TIAs are not required to be unity-gain stable, which makes a decompensated amplifier a viable option for a TIA. [What You Need To Know About Transimpedance Amplifiers – Part 1](#) and [What You Need To Know About Transimpedance Amplifiers – Part 2](#) describe transimpedance amplifier compensation in greater detail.



8.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA858-Q1 features a high slew rate of 2000 V/ μ s. The slew rate is a critical parameter in high-speed pulse applications with narrow sub-10-ns pulses, such as optical time-domain reflectometry (OTDR) and LIDAR. The high slew rate of the OPA858-Q1 implies that the device accurately reproduces a 2-V, sub-ns pulse edge, as seen in [Figure 6-20](#). The wide bandwidth and slew rate of the OPA858-Q1 make it an excellent amplifier for high-speed signal-chain front ends.

[Figure 8-7](#) shows the open-loop output impedance of the OPA858-Q1 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA858-Q1 is limited to approximately 3 V. The OPA858-Q1 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA858-Q1 output swing range coupled with the class-leading voltage noise specification for a CMOS amplifier maximizes the overall dynamic range of the signal chain.

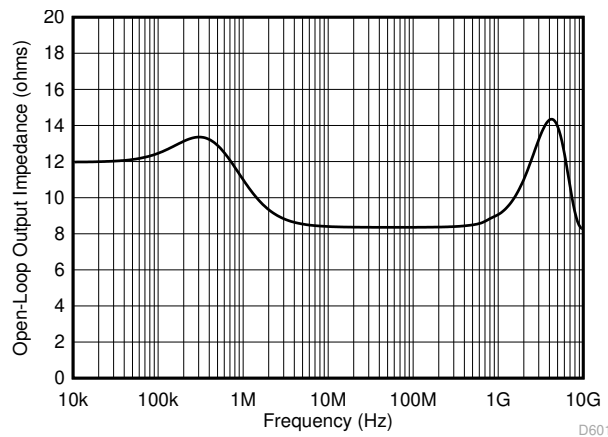


Figure 8-7. Open-Loop Output Impedance (Z_{OL}) vs Frequency

8.3.5 Current Noise

The input impedance of CMOS and JFET input amplifiers at low frequencies exceed several G Ω s. However, at higher frequencies, the transistors parasitic capacitance to the drain, source, and substrate reduces the impedance. The high impedance at low frequencies eliminates any bias current and the associated shot noise. At higher frequencies, the input current noise increases (see [Figure 8-8](#)) as a result of capacitive coupling between the CMOS gate oxide and the underlying transistor channel. This phenomenon is a natural artifact of the construction of the transistor and is unavoidable.

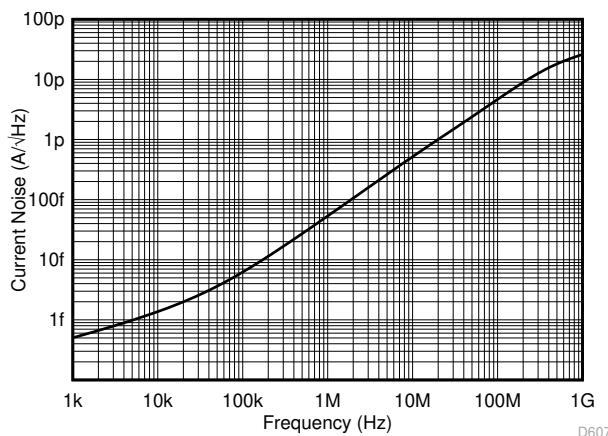


Figure 8-8. Input Current Noise (I_{BN} and I_{BI}) vs Frequency

8.4 Device Functional Modes

8.4.1 Split-Supply and Single-Supply Operation

The OPA858-Q1 can be configured with single-sided supplies or split-supplies as shown in [Figure 10-1](#). Split-supply operation using balanced supplies with the input common-mode set to ground eases lab testing because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground. In split-supply operation, the thermal pad must be connected to the negative supply.

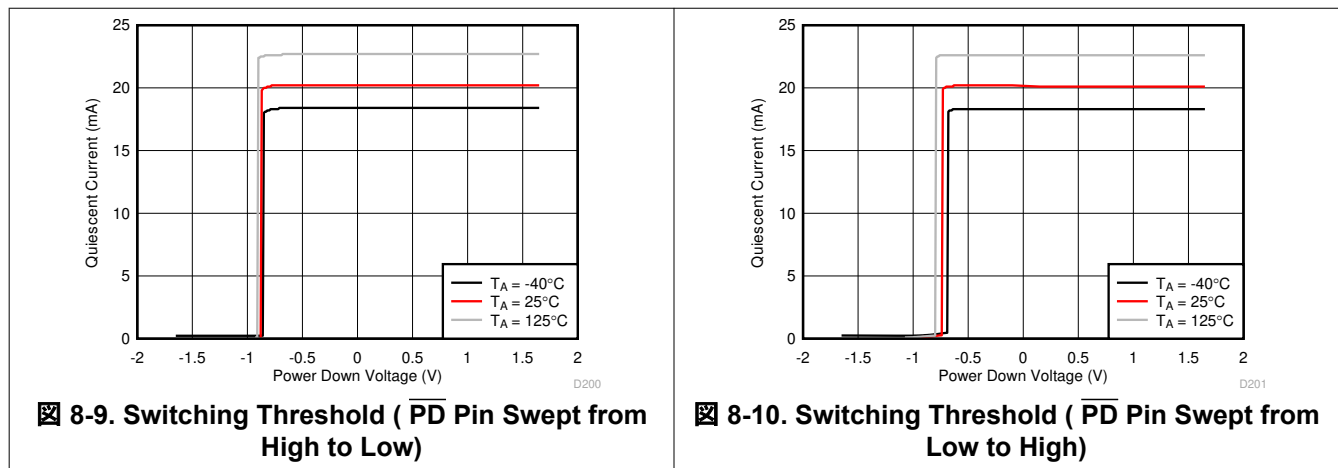
Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA858-Q1 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. In single-supply operation, level shift the DC input and output reference voltages by half the difference between the power supply rails. This configuration maintains the input common-mode and output load reference at midsupply. To eliminate gain errors, the source driving the reference input common-mode voltage must have low output impedance across the frequency range of interest. In this case, the thermal pad must be connected to ground.

8.4.2 Power-Down Mode

The OPA858-Q1 features a power-down mode to reduce the quiescent current to conserve power. [Figure 6-23](#) and [Figure 6-24](#) show the transient response of the OPA858-Q1 as the $\overline{\text{PD}}$ pin toggles between the disabled and enabled states.

The $\overline{\text{PD}}$ disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable and enable threshold voltages are 0.65 V and 1.8 V, respectively. If the amplifier is configured with ± 1.65 V supplies, then the threshold voltages are at -1 V and 0.15 V. If the amplifier is configured with ± 2.5 V supplies, then the threshold voltages are at -1.85 V and -0.7 V.

[Figure 8-9](#) shows the switching behavior of a typical amplifier as the $\overline{\text{PD}}$ pin is swept down from the enabled state to the disabled state. Similarly, [Figure 8-10](#) shows the switching behavior of a typical amplifier as the $\overline{\text{PD}}$ pin is swept up from the disabled state to the enabled state. The small difference in the switching thresholds between the down sweep and the up sweep is caused by the hysteresis designed into the amplifier to increase immunity to noise on the $\overline{\text{PD}}$ pin.



Connecting the $\overline{\text{PD}}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback (R_F) and gain (R_G) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA858-Q1 uses internal, back-to-back protection diodes between the inverting and noninverting input pins as [Figure 8-3](#) shows. In the power-down state, if the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the noninverting input pin and the output pin.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

9.1.1 Using the OPA858-Q1 as a Transimpedance Amplifier

The OPA858-Q1 design has been optimized to meet the industry's growing demand for wideband, low-noise photodiode amplifiers. The closed-loop bandwidth of a transimpedance amplifier is a function of the following:

1. The total input capacitance. This includes the photodiode capacitance, input capacitance of the amplifier (common-mode and differential capacitance) and any stray capacitance from the PCB.
2. The op amp gain bandwidth product (GBWP), and,
3. The transimpedance gain R_F .

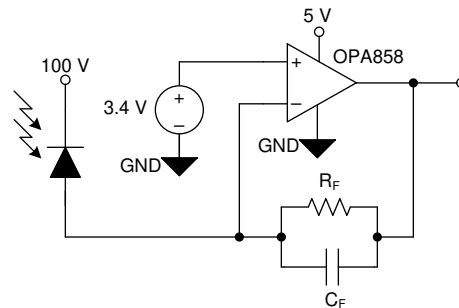
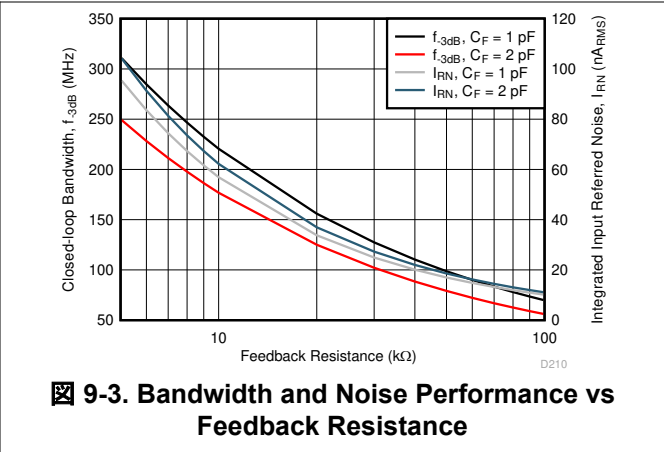
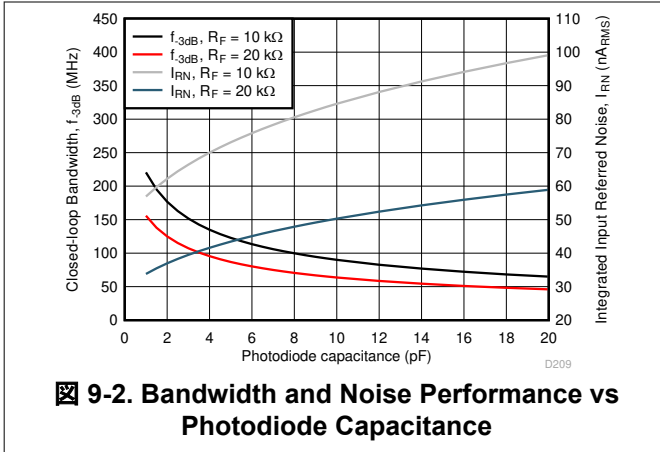


図 9-1. Transimpedance Amplifier Circuit

図 9-1 shows the OPA858-Q1 configured as a TIA with the avalanche photodiode (APD) reverse biased such that the APD cathode is tied to a large positive bias voltage. In this configuration the APD sources current into the op amp feedback loop so that the output swings in a negative direction relative to the input common-mode voltage. To maximize the output swing in the negative direction, the OPA858-Q1 common-mode is set close to the positive limit, 1.6 V from the positive supply rail.

The feedback resistance R_F and the input capacitance form a zero in the noise gain that results in instability if left unchecked. To counteract the effect of the zero, a pole is inserted by adding the feedback capacitor (C_F) into the noise gain transfer function. The [Transimpedance Considerations for High-Speed Amplifiers](#) application report discusses theories and equations that show how to compensate a transimpedance amplifier for a particular gain and input capacitance. The bandwidth and compensation equations from the application report are available in a Microsoft Excel[®] calculator. [What You Need To Know About Transimpedance Amplifiers – Part 1](#) provides a link to the calculator.



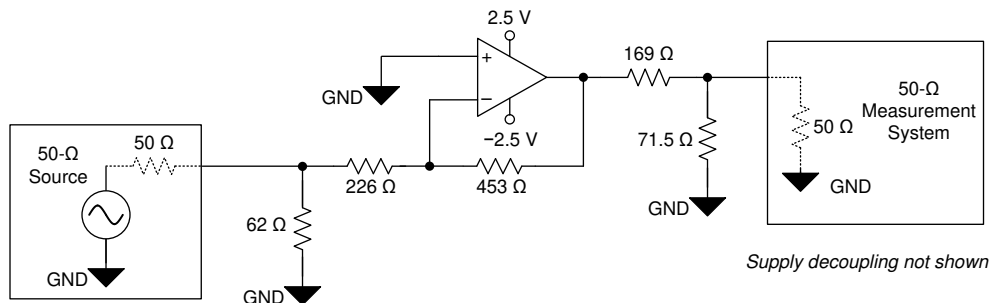
The equations and calculators in the application report and blog posts referenced above are used to model the bandwidth (f_{-3dB}) and noise (I_{RN}) performance of the OPA858-Q1 configured as a TIA. The resultant performance is shown in 9-2 and 9-3. The left side Y-axis shows the closed-loop bandwidth performance, while the right side of the graph shows the integrated input referred noise. The noise bandwidth to calculate I_{RN} , for a fixed R_F and C_{PD} is set equal to the f_{-3dB} frequency.

9-2 shows the amplifier performance as a function of photodiode capacitance (C_{PD}) for $R_F = 10\text{ k}\Omega$ and $20\text{ k}\Omega$. Increasing C_{PD} decreases the closed-loop bandwidth. It is vital to reduce any stray parasitic capacitance from the PCB to maximize bandwidth. The OPA858-Q1 is designed with 0.8 pF of total input capacitance to minimize the effect on system performance.

9-3 shows the amplifier performance as a function of R_F for $C_{PD} = 1\text{ pF}$ and 2 pF . Increasing R_F results in lower bandwidth. To maximize the signal-to-noise ratio (SNR) in an optical front-end system, maximize the gain in the TIA stage. Increasing R_F by a factor of X increases the signal level by X , but only increases the resistor noise contribution by \sqrt{X} , thereby improving SNR.

9.2 Typical Application

The high GBWP, low input voltage noise and high slew rate of the OPA858-Q1 makes the device a viable wideband, high input impedance voltage amplifier.



9-4. OPA858-Q1 in a Gain of $-2V/V$ (No Noise Gain Shaping)

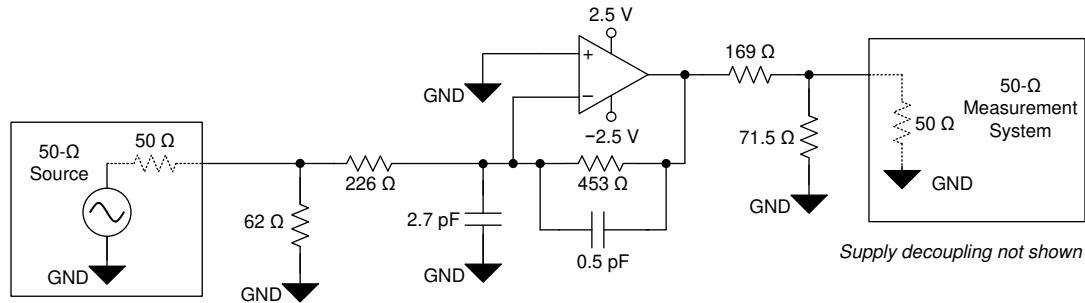


图 9-5. OPA858-Q1 in a Gain of $-2V/V$ (With Noise Gain Shaping)

9.2.1 Design Requirements

Design a high-bandwidth, high-gain, voltage amplifier with the design requirements listed in 表 9-1. An inverting amplifier configuration is chosen here; however, the theory is applicable to a noninverting configuration as well. In an inverting configuration the signal gain and noise gain transfer functions are not equal, unlike the noninverting configuration.

表 9-1. Design Requirements

TARGET BANDWIDTH (MHz)	SIGNAL GAIN (V/V)	FEEDBACK RESISTANCE (Ω)	FREQUENCY PEAKING (dB)
> 750	-2	453	< 2

9.2.2 Detailed Design Procedure

The OPA858-Q1 is compensated to have less than 1 dB of peaking in a gain of 7 V/V. Using the device in lower gains results in increased peaking and potential instability. 图 9-4 shows the OPA858-Q1 configured in a signal gain of $-2 V/V$. The DC noise gain ($1/\beta$) of the amplifier is affected by the 62- Ω termination resistor and the 50- Ω source resistor and is given by 式 1. At higher frequencies the noise gain is affected by reactive elements such as inductors and capacitors. These include both discrete board components as well as printed circuit board (PCB) parasitics.

$$\text{Noise Gain} = \frac{1}{\beta} = \left(1 + \frac{453 \Omega}{226 \Omega + (62 \Omega \parallel 50 \Omega)} \right) = 2.79 \text{ V/V} = 5.04 \text{ dB} \quad (1)$$

The stability and phase margin of the amplifier depend on the loop gain of the amplifier, which is the product of the A_{OL} and the feedback factor (β) of the amplifier. The β of a negative-feedback loop system is the portion of the output signal that is fed back to the input, and in the case of an amplifier is the inverse of the noise gain. The noise gain of the amplifier at high frequencies can be increased by adding an input capacitor and a feedback capacitor as 图 9-5 shows. If done carefully, increasing $1/\beta$ improves the phase margin just as any amplifier is more stable in a high gain configuration versus a unity-gain buffer configuration. The modified network with the added capacitors alters the high-frequency noise gain, but does not alter the signal gain. The [AN-1604 Decompensated Operational Amplifiers](#) application report provides a detailed analysis of noise gain-shaping techniques for decompensated amplifiers and shows how to choose external resistors and capacitor values.

图 9-6 shows the uncompensated frequency response of the OPA858-Q1 configured as shown in 图 9-4. Without any added noise gain shaping components, the OPA858-Q1 shows approximately 13 dB of peaking.

图 9-7 shows the noise gain compensated frequency response of the OPA858-Q1 configured as shown in 图 9-5. The noise gain shaping elements reduce the peaking to less than 1.5 dB. The 2.7-pF input capacitor, the input capacitance of the amplifier, the gain resistor, and the feedback resistor create a zero in the noise gain at a frequency f , as 式 2 shows.

$$f = \frac{1}{2\pi(R_F \parallel R_G)C_{IN}} \quad (2)$$

where

- R_F is the feedback resistor
- R_G is the input or gain resistor (includes the effect of the source and termination resistor)
- C_{IN} is the total input capacitance, which includes the external 2.7-pF capacitor, the amplifier input capacitance, and any parasitic PCB capacitance.

The zero in 式 2 increases the noise gain at higher frequencies, which is important when compensating a decompensated amplifier. However, the noise gain zero reduces the loop gain phase which results in a lower phase margin. To counteract the phase reduction due to the noise gain zero, add a pole to the noise gain curve by inserting the 0.5-pF feedback capacitor. The pole occurs at a frequency shown in 式 3. The noise gain pole and zero locations must be selected so that the rate-of-closure between the magnitude curves of A_{OL} and $1/\beta$ is approximately 20 dB. To ensure this, the noise gain pole must occur before the $1/\beta$ magnitude curve intersects the A_{OL} magnitude curve. In other words, the noise gain pole must occur before $|A_{OL}| = |1/\beta|$. The point at which the two curves intersect is known as the loop gain crossover frequency.

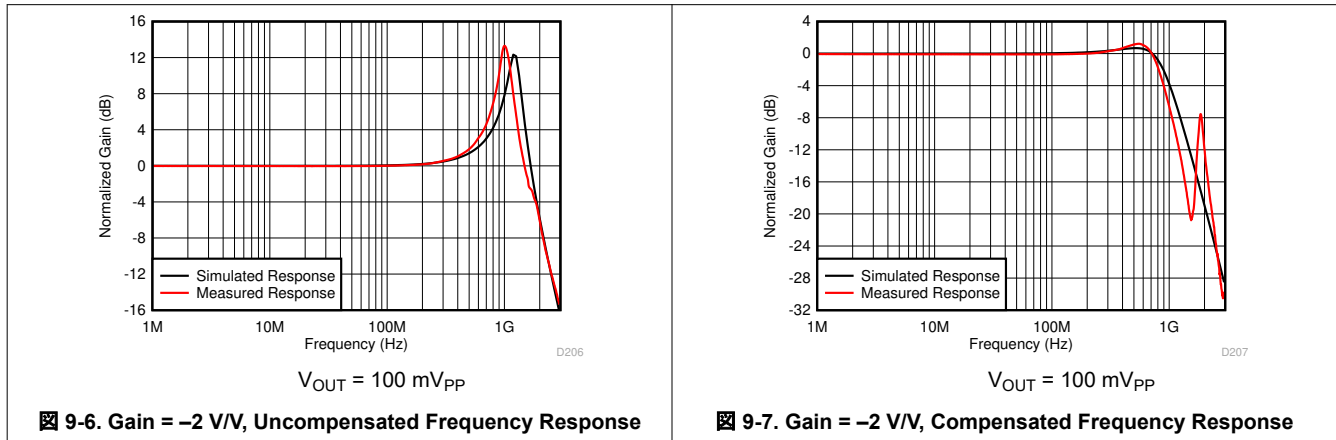
$$f = \frac{1}{2\pi R_F C_F} \quad (3)$$

where

- C_F is the feedback capacitor (includes any added PCB parasitic)

For more information on op amp stability, watch the [TI Precision Lab series on stability](#) video.

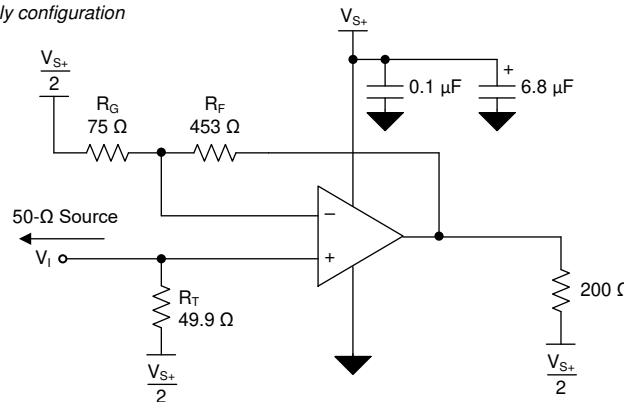
9.2.3 Application Curves



10 Power Supply Recommendations

The OPA858-Q1 operates on supplies from 3.3 V to 5.25 V. The OPA858-Q1 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA858-Q1 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

a) Single supply configuration



b) Split supply configuration

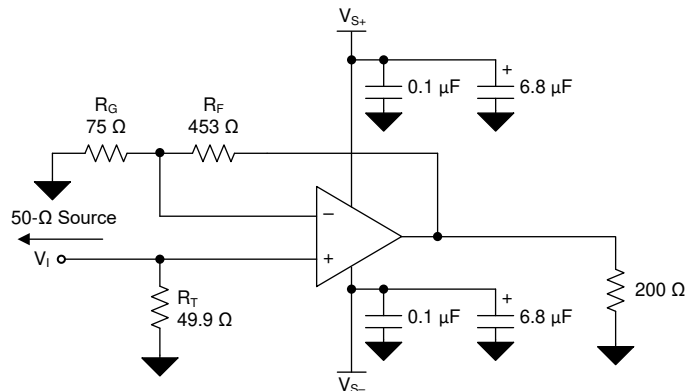


Figure 10-1. Split and Single Supply Circuit Configuration

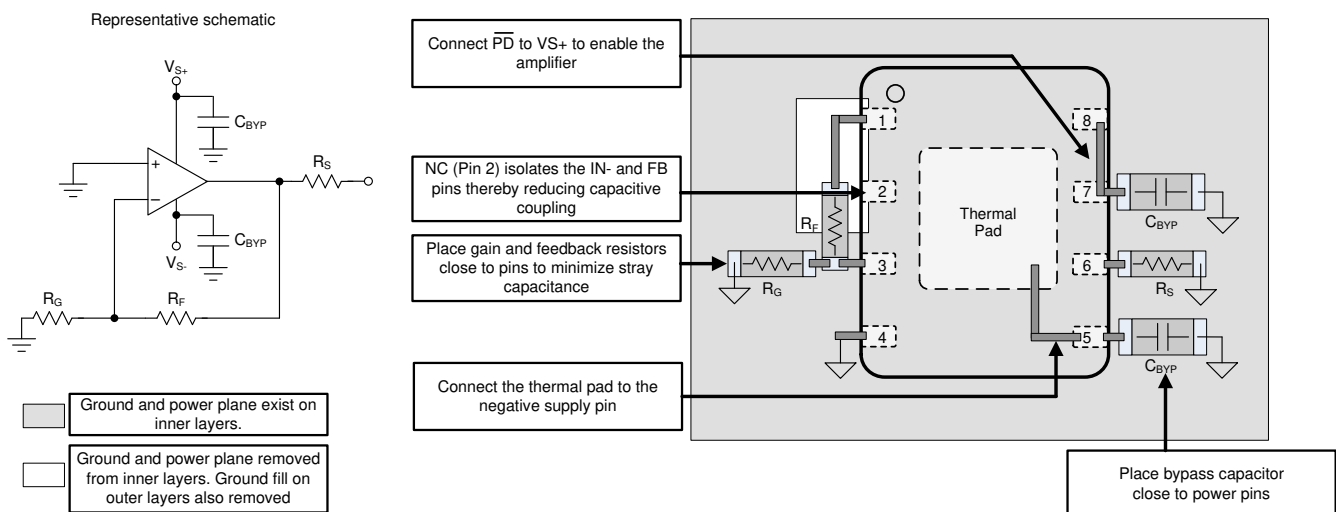
11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA858-Q1 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

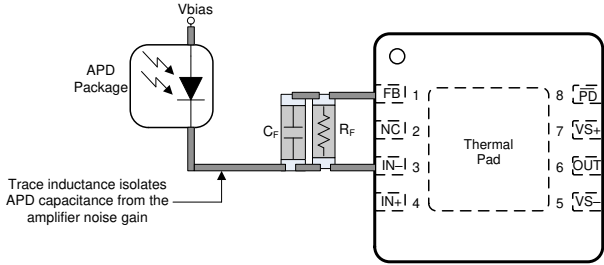
- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is less than 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
- **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1- μ F, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2- μ F to 6.8- μ F) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).
- **Careful selection and placement of external components preserves the high-frequency performance of the OPA858-Q1.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wirewound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. When configuring the OPA858-Q1 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

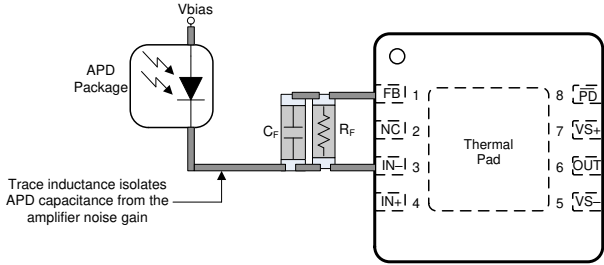
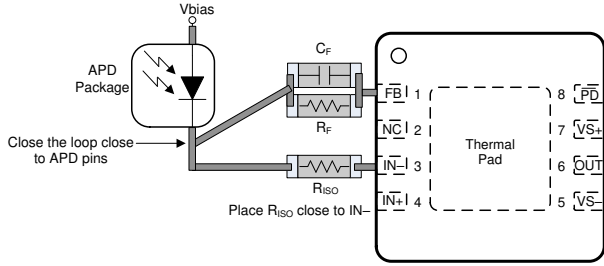
11.2 Layout Example



11-1. Layout Recommendation

When configuring the OPA858-Q1 as a transimpedance amplifier additional care must be taken to minimize the inductance between the avalanche photodiode (APD) and the amplifier. Always place the photodiode on the

same side of the PCB as the amplifier. Placing the amplifier and the APD on opposite sides of the PCB increases the parasitic effects due to via inductance. APD packaging can be quite large which often requires the APD to be placed further away from the amplifier than ideal. The added distance between the two device results in increased inductance between the APD and op amp feedback network as shown in  11-2. The added inductance is detrimental to a decompensated amplifiers stability since it isolates the APD capacitance from the noise gain transfer function. The noise gain is given by 式 4. The added PCB trace inductance between the feedback network increases the denominator in 式 4 thereby reducing the noise gain and the phase margin. In cases where a leaded APD in a TO can is used inductance should be further minimized by cutting the leads of the TO can as short as possible.

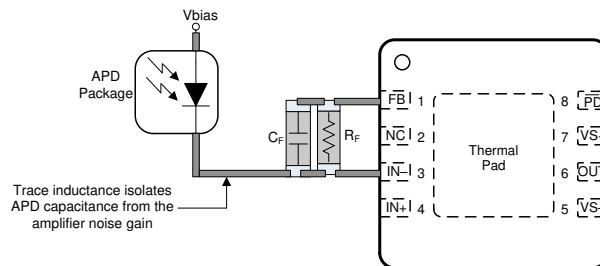
The layout shown in  11-2 can be improved by following some of the guidelines shown in  11-3. The two key rules to follow are:

- Add an isolation resistor R_{ISO} as close as possible to the inverting input of the amplifier. Select the value of R_{ISO} to be between $10\ \Omega$ and $20\ \Omega$. The resistor dampens the potential resonance caused by the trace inductance and the amplifiers internal capacitance.
- Close the loop between the feedback elements (R_F and C_F) and R_{ISO} as close to the APD pins as possible. This ensures a more balanced layout and reduces the inductive isolation between the APD and the feedback network.

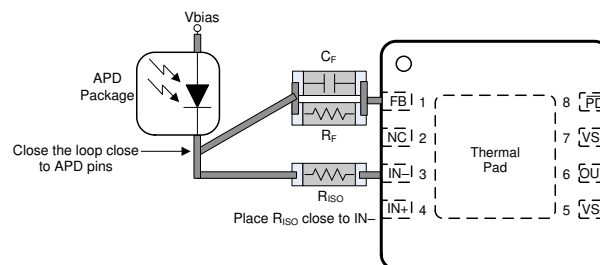
$$\text{Noise Gain} = \left(1 + \frac{Z_F}{Z_{IN}} \right) \quad (4)$$

where

- Z_F is the total impedance of the feedback network.
- Z_{IN} is the total impedance of the input network.



 11-2. Non-Ideal TIA Layout



 11-3. Improved TIA Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- [LIDAR Pulsed Time of Flight Reference Design](#)
- [LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters](#)
- [Wide Bandwidth Optical Front-end Reference Design](#)

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [OPA858EVM user's guide](#)
- Texas Instruments, [Training Video: High-Speed Transimpedance Amplifier Design Flow](#)
- Texas Instruments, [Training Video: How to Design Transimpedance Amplifier Circuits](#)
- Texas Instruments, [Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model](#)
- Texas Instruments, [Transimpedance Considerations for High-Speed Amplifiers application report](#)
- Texas Instruments, [What You Need To Know About Transimpedance Amplifiers – Part 1](#)
- Texas Instruments [What You Need To Know About Transimpedance Amplifiers – Part 2](#)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.7 用語集

TI 用語集 この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA858QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	858Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA858-Q1 :

- Catalog : [OPA858](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

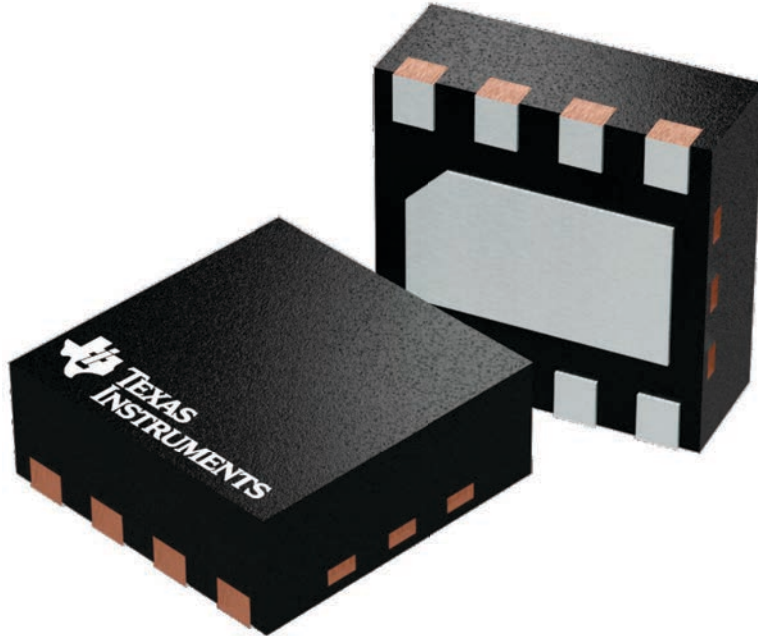
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

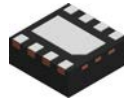
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

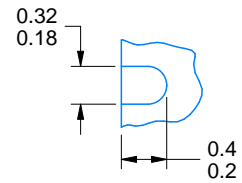
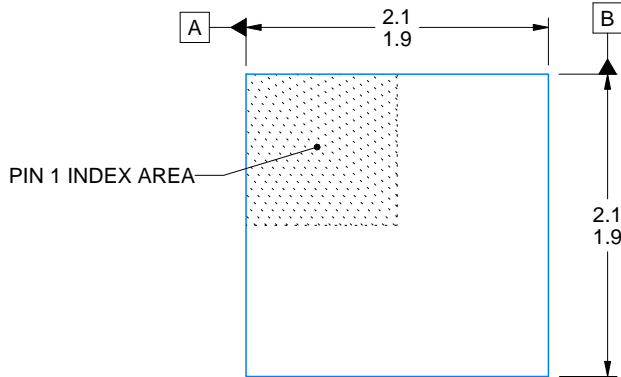
DSG0008A



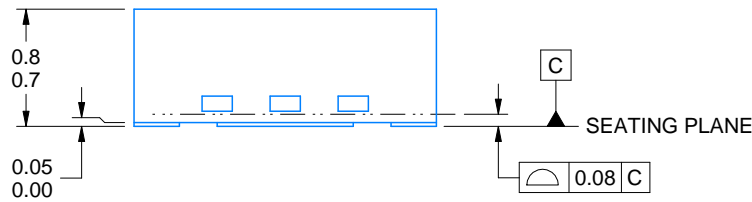
PACKAGE OUTLINE

WSON - 0.8 mm max height

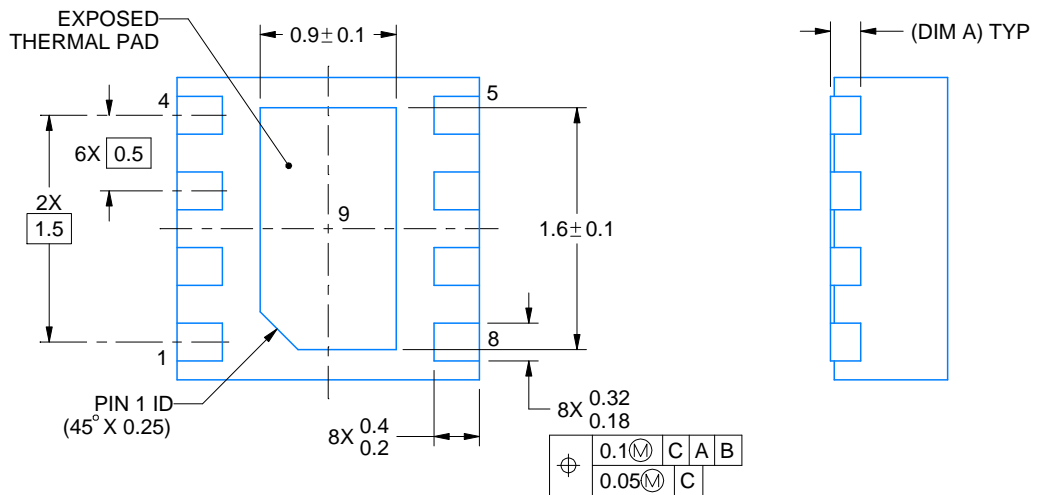
PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE
TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



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NOTES:

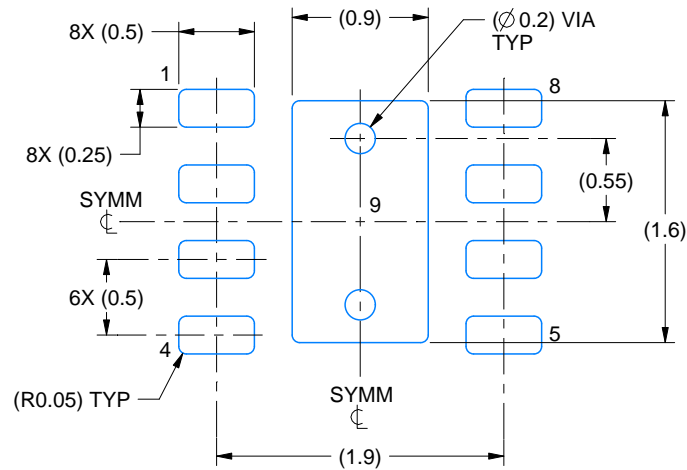
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

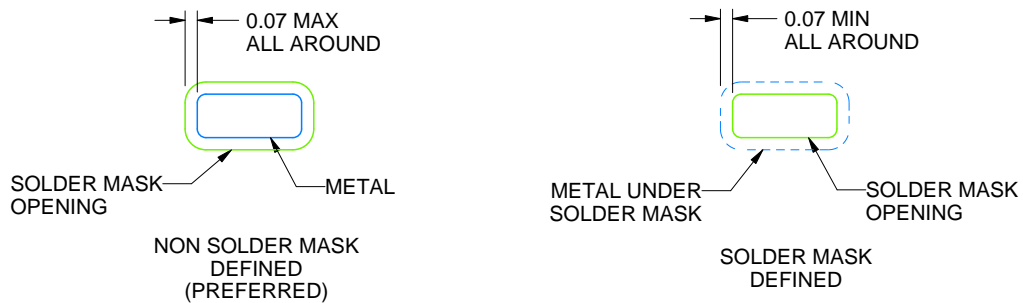
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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