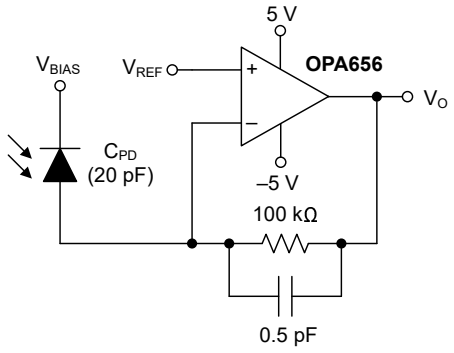
OPA656 550MHz、ユニティ ゲイン安定、FET 入力オペアンプ』

1 特長

- 広い帯域幅:
  - ゲイン帯域幅積:230MHz
  - ユニティ ゲイン帯域幅:550MHz
  - 大信号帯域幅 ($2V_{PP}$):150MHz
- 高精度:
  - 入力オフセット電圧:600µV (最大値)
  - 入力オフセット電圧ドリフト:6 µV/℃ (最大値)
- 入力電圧ノイズ:6nV/√Hz
- 入力バイアス電流:2pA
- 低歪み (R_L = 200Ω、V_O = $2V_{PP}$):
  - 5MHz での HD2、HD3:–80dBc、–100dBc
- 電源電圧範囲:8V～12V

2 アプリケーション

- 高速データ アクイジション (DAQ)
- 医療用および化学用分析器
- アクティブ プローブ
- オシロスコープ
- 光通信モジュール
- テストおよび測定機器のフロントエンド
- 光時間領域反射測定法 (OTDR)



広帯域フォトダイオード トランスインピーダンス アンプ

3 概要

OPA656 は、広帯域、ユニティ ゲイン安定の電圧帰還オペアンプと、低ノイズの接合ゲート電界効果トランジスタ (JFET) 入力段を組み合わせることで、トランスインピーダンス アプリケーションおよび高速データ収集フロントエンド用の超高ダイナミックレンジのアンプを実現します。DC 誤差が非常に小さいため、光学アプリケーションおよび試験/計測で優れた精度を達成しています.。

OPA656 は、きわめて低い入力電圧ノイズ (6nV/√Hz) を特長としており、トランスインピーダンス アプリケーションで非常に低い積分ノイズを実現します。OPA656 は入力インピーダンスが高く、入力電圧ノイズが低いため、光学テスト機器、通信機器、医療用および科学用計測機器に最適な優れた広帯域トランスインピーダンス アンプです。

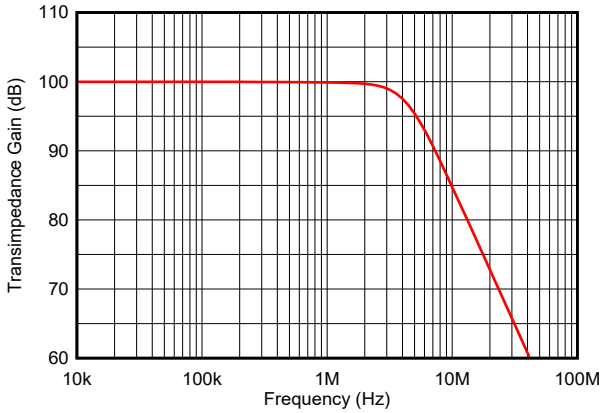
OPA656 は 230MHz の広いゲイン帯域幅を備えています。150MHz の大信号帯域幅で、歪みが小さいため、高速デジタイザ フロント エンド、アクティブ プローブ、その他の試験および測定フロント エンドに最適です。

このデバイスは、産業用温度範囲の -40℃～+85℃で動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
OPA656	D (SOIC、8)	4.9mm × 6mm
	DBV (SOT-23、5)	2.9mm × 2.8mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



トランスインピーダンス帯域幅：100kΩ

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4 Device Comparison Table

DEVICE	V_S (V)	GBW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	MINIMUM STABLE GAIN (V/V)
OPA656	±6	230	550	6	1
OPA814	±6.3	250	750	5.3	1
OPA817	±6.3	400	1000	4.5	1
OPA818	±6.5	2700	1400	2.2	7
OPA659	±6.5	350	2550	8.9	1
THS4631	±15	210	1000	7	1

5 Pin Configuration and Functions

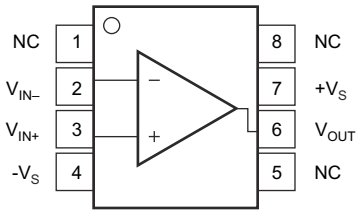
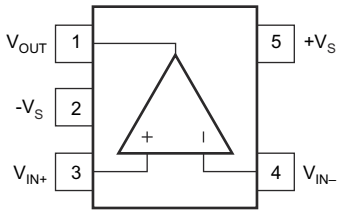
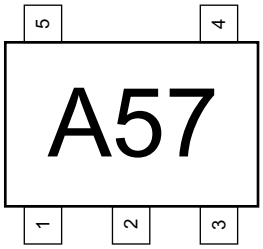


図 5-1. D Package, 8-Pin SOIC Surface-Mount (Top View)





Pin Orientation/Package Marking

図 5-2. DBV Package, 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC)	DBV (SOT-23)		
NC	1, 5, 8	—	—	No internal connection
$V_{IN–}$	2	4	Input	Inverting input
V_{IN+}	3	3	Input	Noninverting input
$–V_S$	4	2	Power	Negative power supply
$+V_S$	7	5	Power	Positive power supply
V_{OUT}	6	1	Output	Output of amplifier

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage (total bipolar supplies)		±6.5	V
	Maximum dV_S/dT for supply turn-on and turn-off(2)		1	V/µs
	Internal power dissipation	See *Thermal Information*		
V_I	Input voltage	$-V_S$	$+V_S$	V
V_{ID}	Differential input voltage	$-V_S$	$+V_S$	V
I_I	Continuous input current(3)		±10	mA
I_O	Continuous output current(4)		±30	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Staying less than this specification keeps the edge-triggered ESD absorption devices across the supply pins off.
(3) Continuous input current limit for the ESD diodes to supply pins.
(4) Long-term continuous current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	8	10	12	V
T_A	Ambient temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA656		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123	154	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.1	88.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.3	55.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.1	33.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	65.5	55.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A ≅ 25°C, V_S = ±5 V, G = +2 V/V, R_F = 250 Ω, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	G = +1 V/V, V_O = 200 mV_{PP}, R_F = 0 Ω		550		MHz
		G = +2 V/V, V_O = 200 mV_{PP}		230		
		G = +5 V/V, V_O = 200 mV_{PP}		59		
		G = +10 V/V, V_O = 200 mV_{PP}		23		
GBW	Gain-bandwidth product	G ≥ 10 V/V		230		MHz
	Bandwidth for 0.1-dB flatness	V_O = 200 mV_{PP}		50		MHz
	Peaking at G = +1 V/V	V_O = 200 mV_{PP}, R_F = 0 Ω		1		dB
LSBW	Large-signal bandwidth	V_O = 2 V_{PP}		130		MHz
SR	Slew rate	V_O = 1-V step		400		V/µs
	Rise-and-fall time	V_O = 0.2-V step		1.3		ns
	Settling time to 0.02%	V_O = 2-V step		19		ns
HD2	Second-order harmonic distortion	f = 5 MHz, V_O = 2 V_{PP} , R_L = 200 Ω		–75		dBc
		f = 5 MHz, V_O = 2 V_{PP} , R_L > 500 Ω		–78		
HD3	Third-order harmonic distortion	f = 5 MHz, V_O = 2 V_{PP} , R_L = 200 Ω		–90		dBc
		f = 5 MHz, V_O = 2 V_{PP} , R_L > 500 Ω		–100		
e_N	Input voltage noise	f > 100 kHz		6		nV/√Hz
	Input current noise	f = 100 kHz		5		fA/√Hz
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_O = 0 V	60	75		dB
		V_O = 0 V, T_A = –40°C to +85°C	58			
V_{OS}	Input-referred offset voltage	V_{CM} = 0 V		±0.2	±1.8	mV
		V_{CM} = 0 V, T_A = –40°C to +85°C			±2.6	
	Input offset voltage drift(1)	V_{CM} = 0 V		±2	±12	µV/°C
		V_{CM} = 0 V, T_A = –40°C to +85°C			±12	
I_B	Input bias current	V_{CM} = 0 V		±2	±20	pA
		V_{CM} = 0 V, T_A = –40°C to +85°C			±5000	
I_{OS}	Input offset current	V_{CM} = 0 V		±1	±20	pA
		V_{CM} = 0 V, T_A = –40°C to +85°C			±5000	
INPUT						
CMIR	Most positive input voltage(2)		2.1	2.75		V
		T_A = –40°C to +85°C	2			
CMIR	Most negative input voltage(2)			–4.3	–3.9	V
		T_A = –40°C to +85°C			–3.7	
CMIR	Most positive input voltage(3)		2.6	3.25		V
		T_A = –40°C to +85°C	2.4			
CMIR	Most negative input voltage(3)			–4.5	–4	V
		T_A = –40°C to +85°C			–3.8	
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V	80	90		dB
		V_{CM} = ±0.5 V, T_A = –40°C to +85°C	76			
	Input impedance common-mode			10^{12} || 0.4		Ω || pF
	Input impedance differential mode			10^{10} || 2.6		Ω || pF

6.5 Electrical Characteristics (続き)

at T_A ≅ 25°C, V_S = ±5 V, G = +2 V/V, R_F = 250 Ω, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing	No Load	±3.7	±3.9		V
		R_L = 100 Ω	±3.3	±3.5		
		R_L = 100 Ω, T_A = –40°C to +85°C	±3.1			
	Current output, sourcing		50	70		mA
		T_A = –40°C to +85°C	45			
	Current output, sinking			–70	–50	mA
		T_A = –40°C to +85°C			–45	
	Closed-loop output impedance	G = +1 V/V, f = 0.1 MHz		0.01		Ω
POWER SUPPLY						
	Specified operating voltage			±5		V
	Maximum operating voltage range				±6	V
		T_A = –40°C to +85°C			±6	
I_Q	Quiescent current		11.7	15	16.7	mA
		T_A = –40°C to +85°C	11.1		16.8	
+PSRR	Positive power-supply rejection ratio	$+V_S$ = 4.5 to 5.5 V	72	85		dB
		$+V_S$ = 4.5 to 5.5 V, T_A = –40°C to +85°C	68			
–PSRR	Negative power-supply rejection ratio	$–V_S$ = –4.5 to –5.5 V	56	80		dB
		$–V_S$ = –4.5 to –5.5 V, T_A = –40°C to +85°C	52			

(1) Based on electrical characterization of 32 devices. Minimum and maximum values are not specified by final automated test equipment (ATE) nor by QA sample testing. Typical specifications are ±1 sigma.
(2) Tested at 3 dB less than minimum specified CMRR at ±CMIR limits.
(3) Input range to give > 53-dB CMRR.

6.6 Electrical Characteristics: High Grade DC Specifications

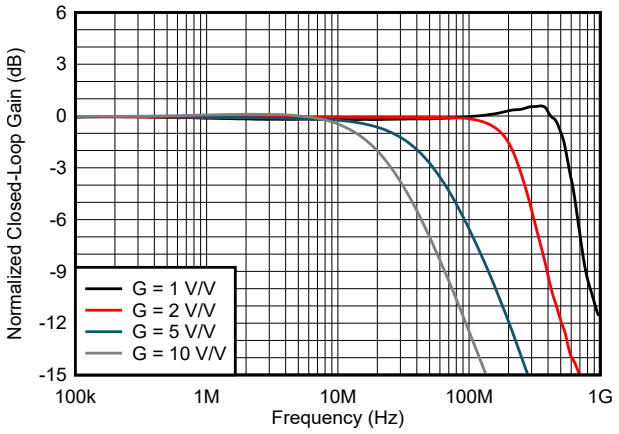
at T_A ≅ 25°C, V_S = ±5 V, G = +2 V/V, R_F = 250 Ω, R_L = 100 Ω, and input and output referenced to mid-supply (unless otherwise noted)(1)

PARAMETER			MIN	NOM	MAX	UNIT
V_{OS}	Input-referred offset voltage	V_{CM} = 0 V		±0.1	±0.6	mV
		V_{CM} = 0 V, T_A = –40°C to +85°C			±0.9	
	Input offset voltage drift	V_{CM} = 0 V		±2	±6	µV/°C
		V_{CM} = 0 V, T_A = –40°C to +85°C			±6	
I_B	Input bias current	V_{CM} = 0 V		±2	±20	pA
		V_{CM} = 0 V, T_A = –40°C to +85°C			±1250	
I_{OS}	Input offset current	V_{CM} = 0 V		±1	±20	pA
		V_{CM} = 0 V, T_A = –40°C to +85°C			±1250	
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V	84	95		dB
		V_{CM} = ±0.5 V, T_A = –40°C to +85°C	83			
+PSRR	Positive power-supply rejection ratio	$+V_S$ = 4.5 to 5.5 V	74	90		dB
		$+V_S$ = 4.5 to 5.5 V, T_A = –40°C to +85°C	70			
–PSRR	Negative power-supply rejection ratio	$–V_S$ = –4.5 to –5.5 V	62	85		dB
		$–V_S$ = –4.5 to –5.5 V, T_A = –40°C to +85°C	58			

(1) All other specifications are the same as the standard-grade.

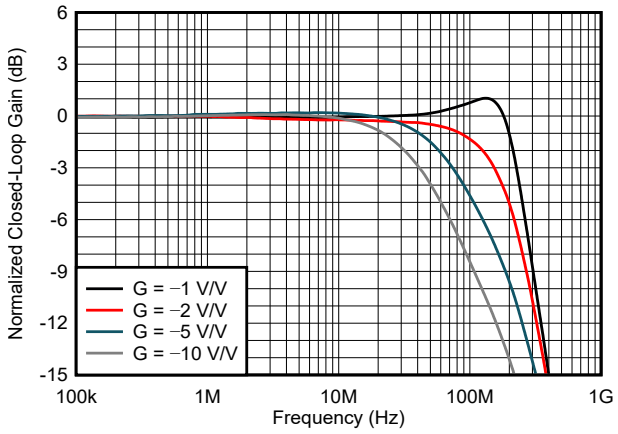
6.7 Typical Characteristics: V_S = ±5 V

at T_A = 25°C, G = +2 V/V, R_F = 250 Ω, and R_L = 100 Ω (unless otherwise noted)



V_{OUT} = 200 mV_{PP}

図 6-1. Noninverting Small-Signal Frequency Response



V_{OUT} = 200 mV_{PP}

図 6-2. Inverting Small-Signal Frequency Response

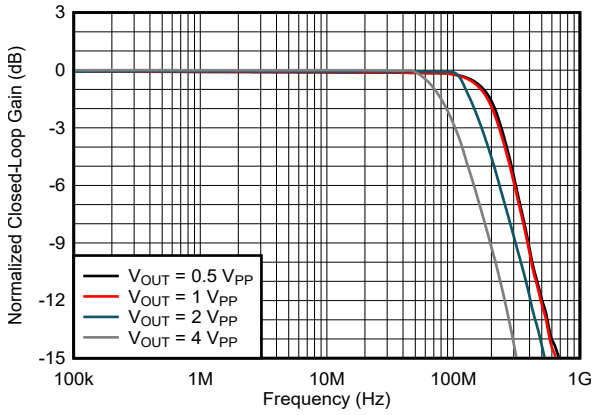
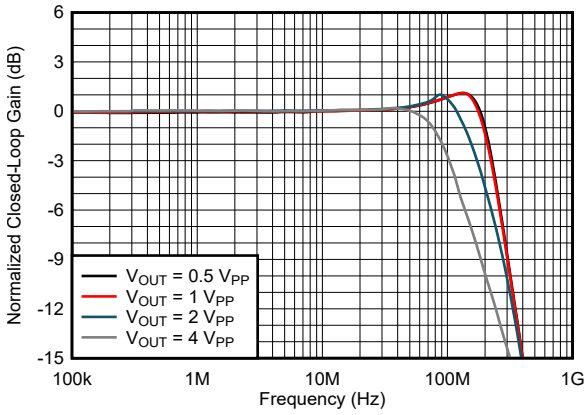


図 6-3. Noninverting Large-Signal Frequency Response



G = –1 V/V

図 6-4. Inverting Large-Signal Frequency Response

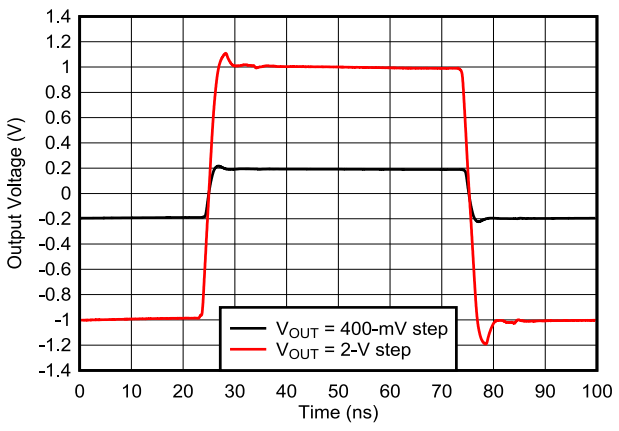
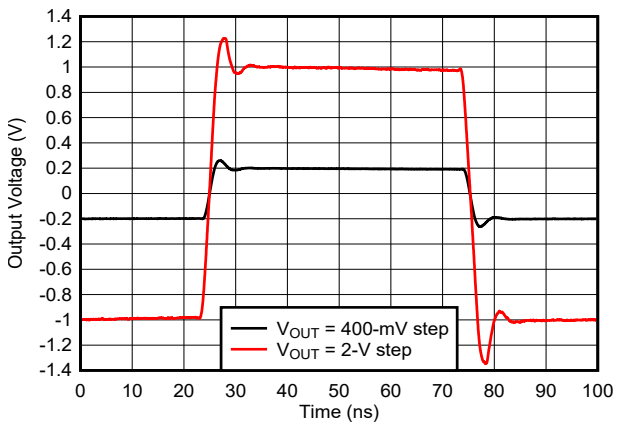


図 6-5. Noninverting Pulse Response



G = –1 V/V

図 6-6. Inverting Pulse Response

6.7 Typical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, G = +2 V/V, R_F = 250 Ω, and R_L = 100 Ω (unless otherwise noted)

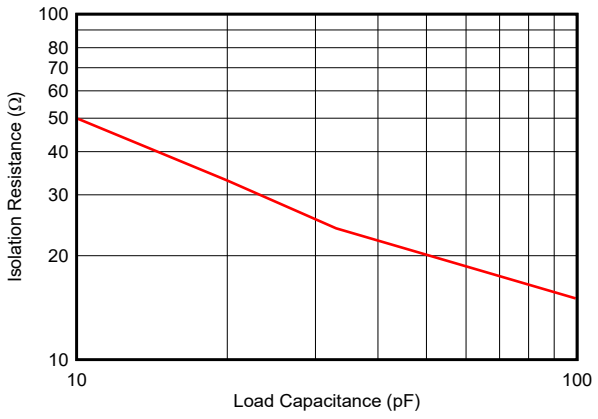


図 6-7. Recommended R_S vs Capacitive Load

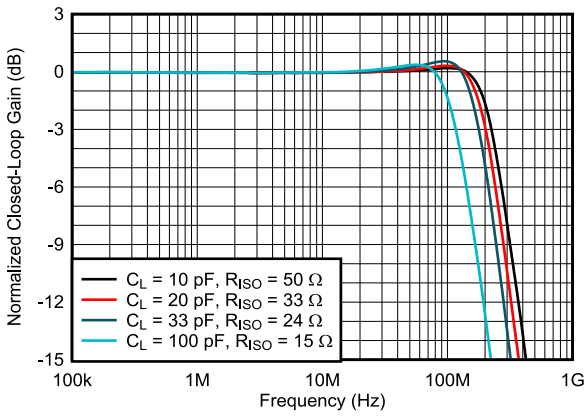


図 6-8. Frequency Response vs Capacitive Load

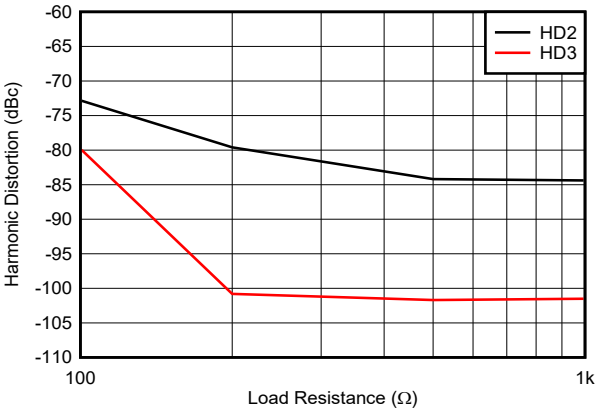


図 6-9. Harmonic Distortion vs Load Resistance

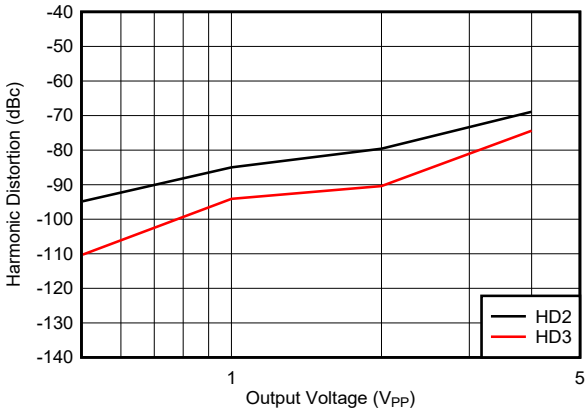


図 6-10. Harmonic Distortion vs Output Voltage

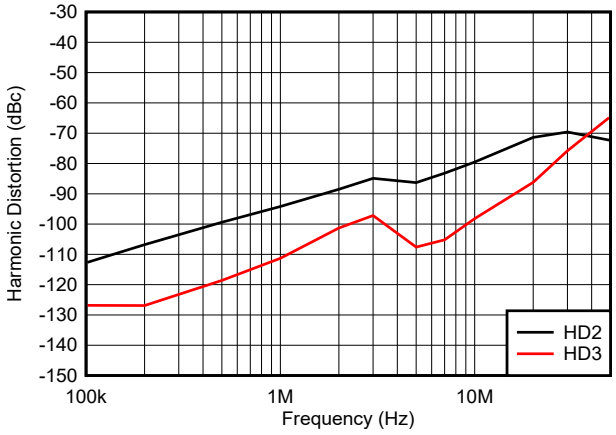


図 6-11. Harmonic Distortion vs Frequency

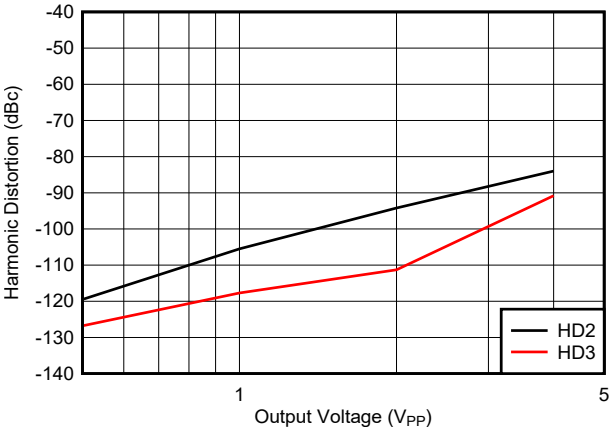


図 6-12. Harmonic Distortion vs Output Voltage

6.7 Typical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, G = +2 V/V, R_F = 250 Ω, and R_L = 100 Ω (unless otherwise noted)

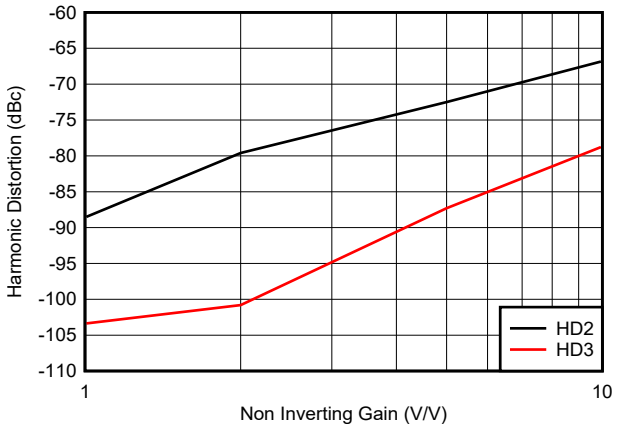


図 6-13. Harmonic Distortion vs Noninverting Gain

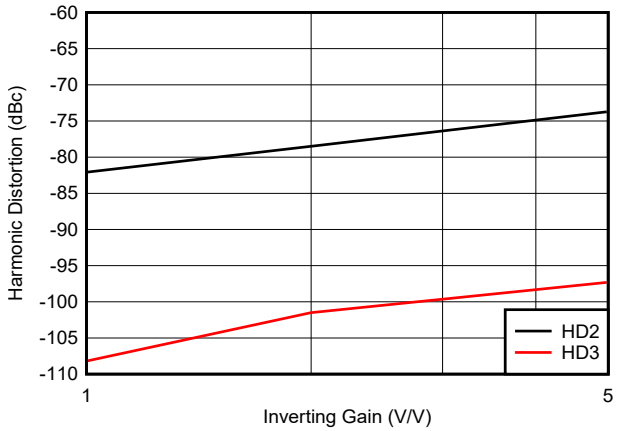


図 6-14. Harmonic Distortion vs Inverting Gain

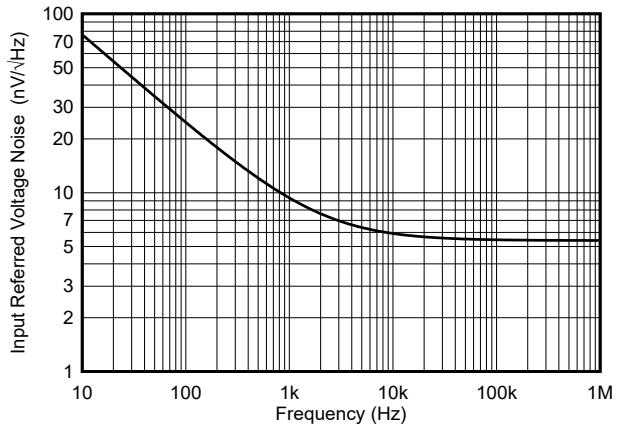


図 6-15. Input Voltage Noise Density

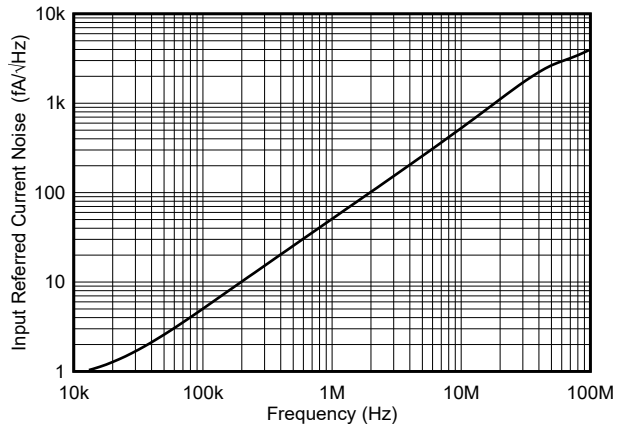


図 6-16. Input Current Noise Density

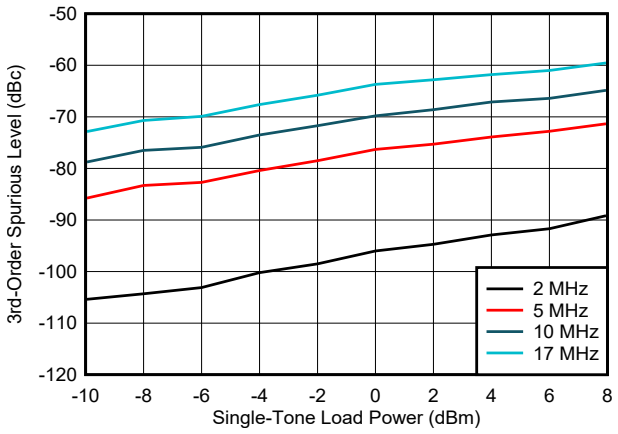


図 6-17. 2-Tone, 3rd-Order Intermodulation Spurious

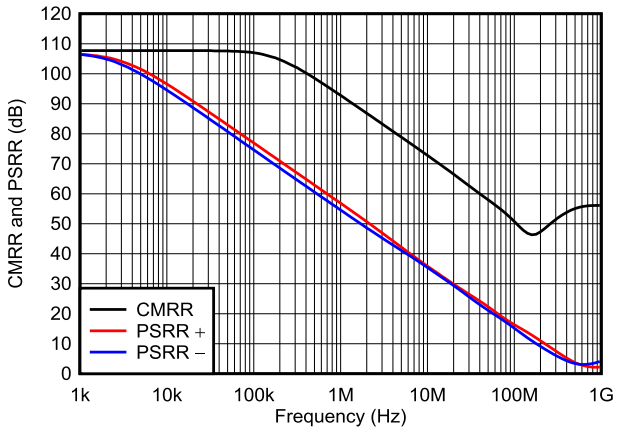


図 6-18. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

6.7 Typical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, G = +2 V/V, R_F = 250 Ω, and R_L = 100 Ω (unless otherwise noted)

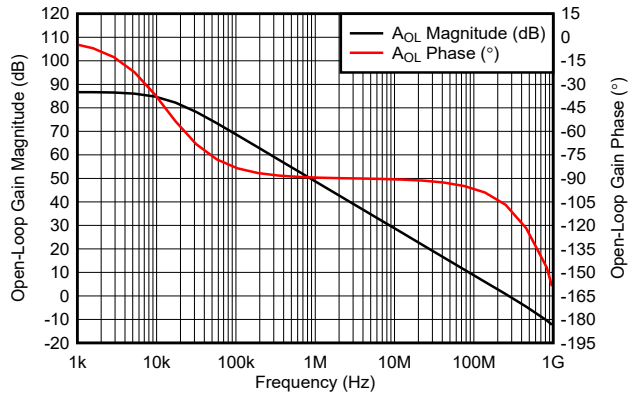


図 6-19. Open-Loop Gain and Phase

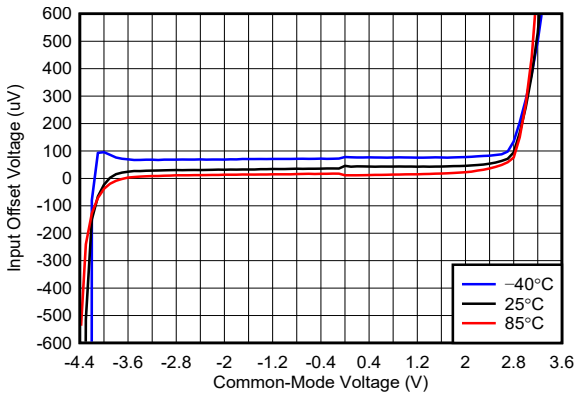


図 6-20. Input offset voltage vs Common-Mode Input Voltage

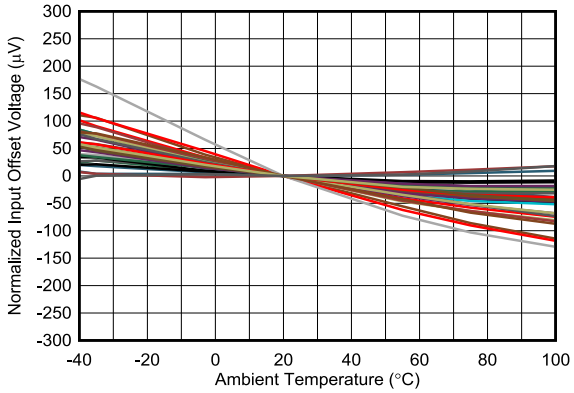


図 6-21. Typical Input Offset Voltage Over Temperature

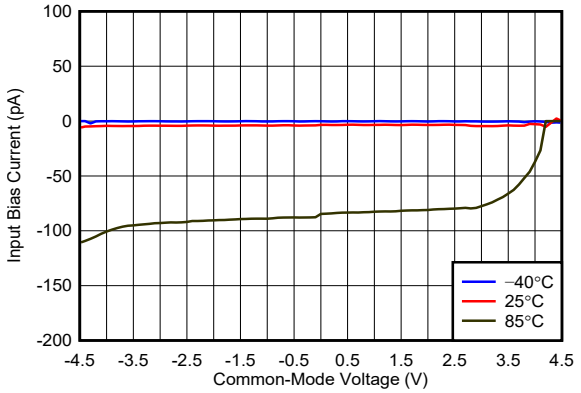


図 6-22. Typical Input Bias Current vs Common-Mode Input Voltage

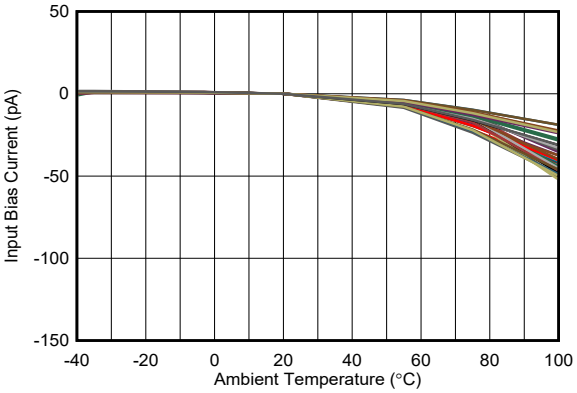


図 6-23. Typical Input Bias Current Over Temperature

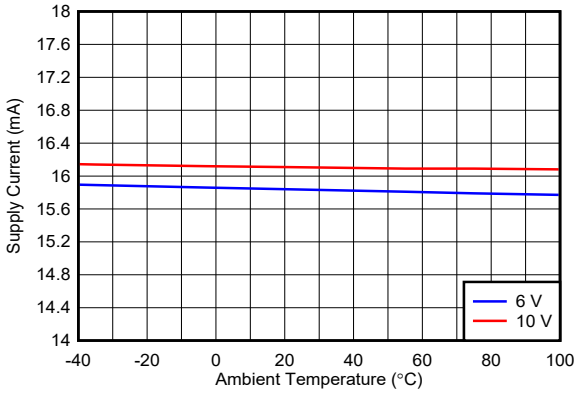


図 6-24. Supply Current vs Temperature

6.7 Typical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, G = +2 V/V, R_F = 250 Ω, and R_L = 100 Ω (unless otherwise noted)

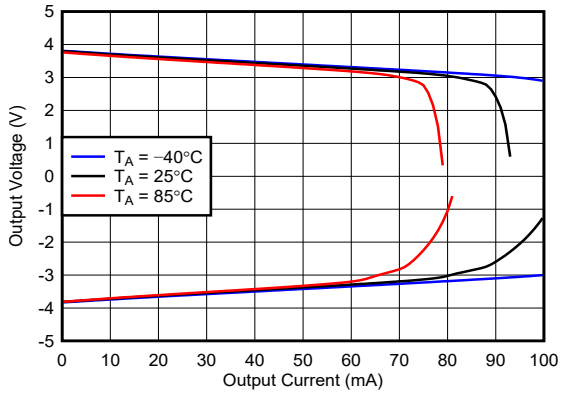


図 6-25. Output voltage vs Output Current Over Temperature

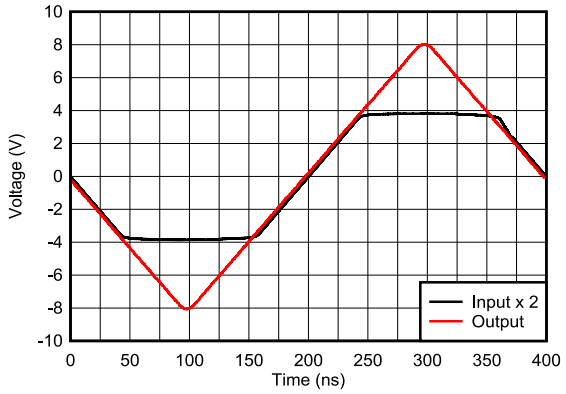
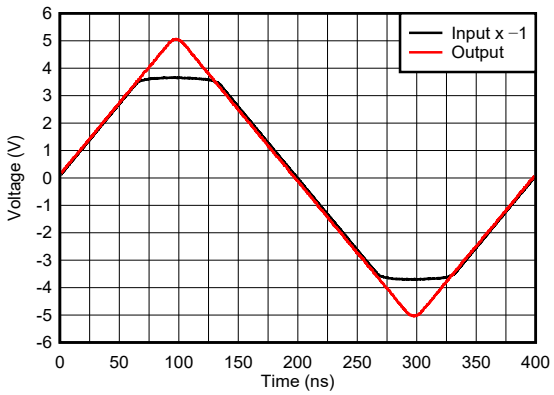
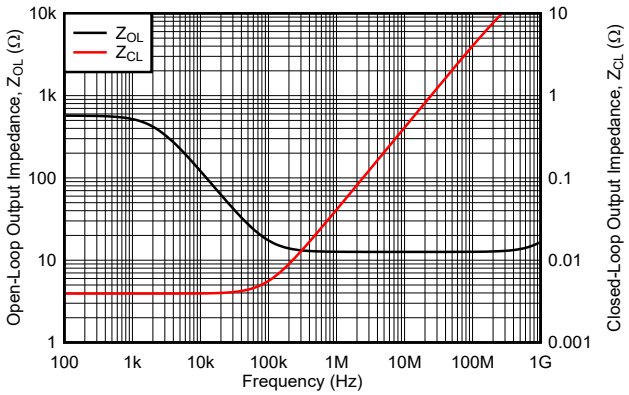


図 6-26. Noninverting Input Overdrive Recovery



G = –1 V/V

図 6-27. Inverting Overdrive Recovery



G = 1 V/V

図 6-28. Closed-Loop and open-loop Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

The OPA656 is a high gain-bandwidth, voltage-feedback operational amplifier featuring a low-noise JFET input stage. The OPA656 is compensated to be unity-gain stable and finds wide use in applications that require high input impedance, such as optical front-end applications and test and measurement systems. For the best dc precision, a high-grade version (OPA656UB or OPA656NB) is available that specifies the key dc parameters to even tighter limits.

7.2 Feature Description

7.2.1 Input and ESD Protection

The OPA656 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the table of *Absolute Maximum Ratings*. 図 7-1 shows how all device pins are protected with internal ESD protection diodes to the power supplies.

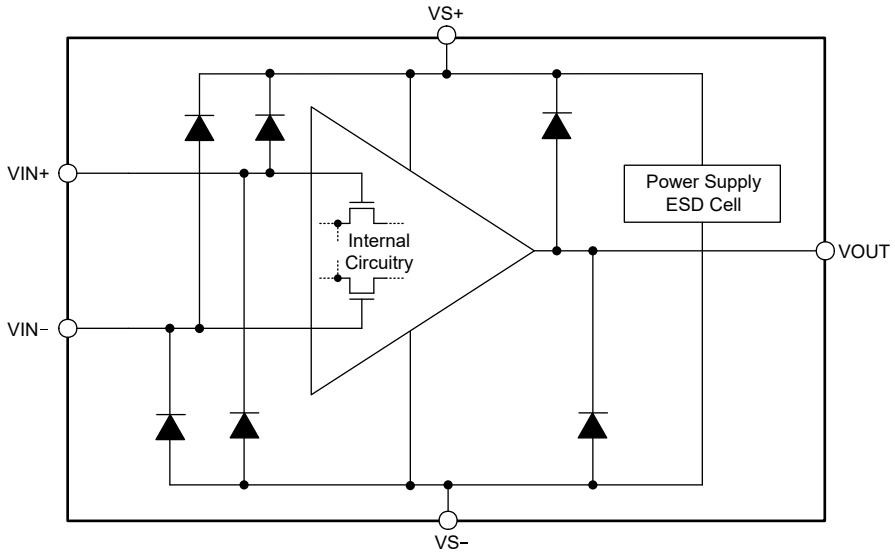


図 7-1. Internal ESD Protection

Along with ESD protection, these diodes provide moderate protection to input overdrive voltages greater than the supplies. The protection diodes typically support 10 mA of continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA656), add current limiting series resistors into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

7.3 Device Functional Modes

The OPA656 has a single functional mode and is operational when the power-supply voltage is greater than 8 V. The maximum power supply voltage for the OPA656 is 12 V (±6 V). The OPA656 can be operated on both single and dual supplies.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Wideband, Noninverting Operation

The OPA656 provides a unique combination of a broadband, unity gain stable, voltage-feedback amplifier with the dc precision of a trimmed JFET-input stage. The very high gain bandwidth product (GBP) of 230 MHz can be used to either deliver high signal bandwidths for low-gain buffers, or to deliver broadband, low-noise transimpedance bandwidth to photodiode-detector applications. To achieve the full performance of the OPA656, careful attention to printed-circuit-board (PCB) layout and component selection is required, as discussed in the remaining sections of this data sheet.

図 8-1 shows the noninverting gain of +2 V/V circuit used as the basis for most of the *Typical Characteristics*. Most of the curves were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. In 図 8-1, the 50-Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in 図 8-1) while output power specifications are at the matched 50-Ω load. The total 100-Ω load at the output combined with the 500-Ω total feedback network load, presents the OPA656 with an effective output load of 83 Ω for the circuit of 図 8-1.

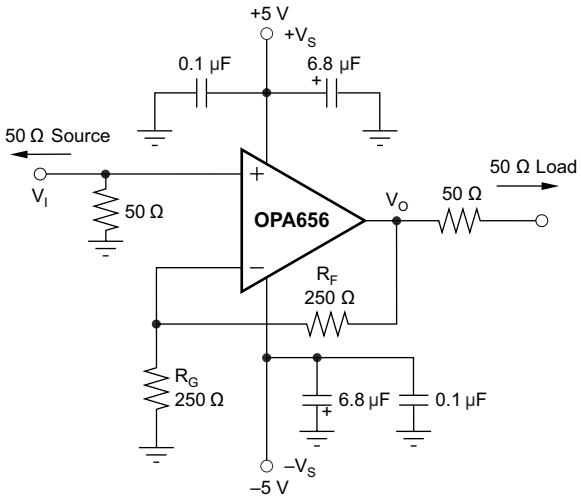


図 8-1. Noninverting G = +2 V/V Specifications and Test Circuit

Voltage-feedback operational amplifiers, unlike current feedback products, can use a wide range of resistor values to set the gain. To retain a controlled frequency response for the noninverting voltage amplifier of 図 8-1, ensure that the parallel combination of R_F || R_G is always < 200 Ω. In the noninverting configuration, the parallel combination of R_F || R_G forms a pole with the parasitic input capacitance at the inverting node of the OPA656 (including layout parasitics). For best performance, ensure this pole is at a frequency greater than the closed-loop bandwidth for the OPA656. For this reason, TI recommends a direct short from the output to the inverting input for the unity-gain follower application.

8.1.2 Wideband, Inverting Gain Operation

The circuit of 図 8-2 shows the inverting gain of –1 V/V test circuit used for most of the inverting typical characteristics. In this case, an additional resistor R_M is used to achieve the 50-Ω input impedance required by the test equipment using in characterization. This input impedance matching is optional in a circuit board environment where the OPA656 is used as an inverting amplifier at the output of a prior stage.

In this configuration, the feedback resistor acts as an additional load at output in parallel with the 100-Ω load used for test. Increase the R_F value to decrease the loading on the output (improving harmonic distortion) with the constraint that the parallel combination of R_F || R_G < 200 Ω. For higher gains with the dc precision provided by the FET input OPA656, consider the higher gain bandwidth product OPA814 or OPA818.

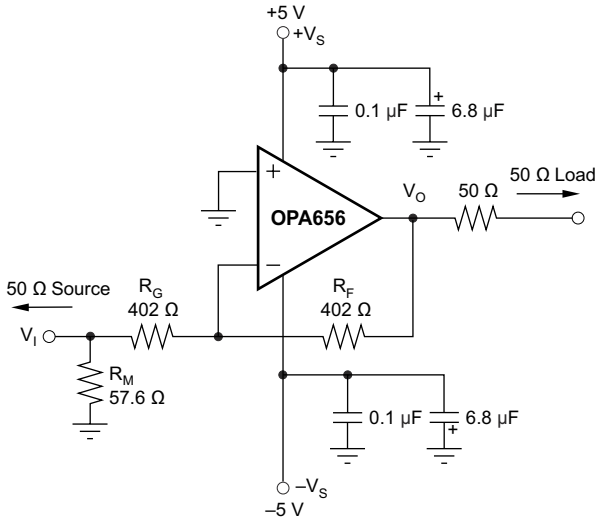


図 8-2. Inverting G = –1 V/V Specifications and Test Circuit

図 8-2 also shows the noninverting input tied directly to ground. Often, a bias current canceling resistor to ground is included here to null out the dc errors caused by input bias current effects. This resistor is only useful when the input bias currents are matched. For a JFET part such as the OPA656, the input bias currents do not match but are so low to begin with (< 20 pA) that dc errors due to input bias currents are negligible. Thus, no resistor is recommended at the noninverting inputs for the inverting signal path condition.

8.2 Typical Application

The high GBP and low input voltage and current noise for the OPA656 make the device an excellent wideband transimpedance amplifier for moderate to high transimpedance gains.

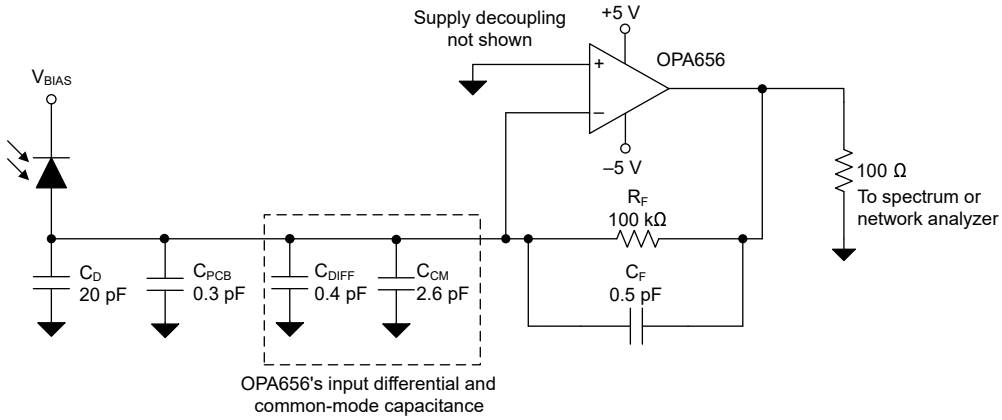


図 8-3. Wideband, High-Sensitivity, Transimpedance Amplifier

8.2.1 Design Requirements

Design a high-bandwidth, high-gain transimpedance amplifier with the design requirements shown in 表 8-1.

表 8-1. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE GAIN (KΩ)	PHOTODIODE CAPACITANCE (pF)
4	100	20

8.2.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA656. This input voltage noise is peaked up over frequency by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage (V_B) applied the desired transimpedance gain, R_F, and the GBP for the OPA656 (230 MHz). 図 8-3 shows a transimpedance circuit with the parameters as described in 表 8-1. With these three variables set (and including the parasitic input capacitance for the OPA656 and the PCB added to C_D), the feedback capacitor value (C_F) can be set to control the frequency response. To achieve a maximally-flat second-order Butterworth frequency response, set the feedback pole to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \tag{1}$$

The input capacitance of the amplifier is the sum of the common-mode and differential capacitance (0.4 + 2.6) pF. The parasitic capacitance from the photodiode package and the PCB is approximately 0.3 pF. These values result in a total effective input capacitance of C_D = 23.3 pF. From 式 1, set the feedback pole at 2.8 MHz. Setting the pole at 2.8 MHz requires a total feedback capacitance of 0.57 pF

The approximate −3-dB bandwidth of the transimpedance amplifier circuit is given by:

$$f_{-3dB} = \sqrt{GBP / \left(2\pi R_F C_D\right)}\ Hz \tag{2}$$

式 2 estimates a closed-loop bandwidth of 3.96 MHz. The total feedback capacitance for the circuit used in the design is estimated to be 0.6 pF. The total feedback capacitance includes the physical 0.5 pF feedback capacitor in parallel with 100-fF of parasitic capacitance due to the feedback resistor and PCB trace. The parasitic capacitance from the PCB trace can be minimized by removing the ground and power planes in the feedback path. A TINA SPICE simulation of the circuit in 図 8-3 results in a closed-loop bandwidth of 4.2 MHz.

図 8-4 shows the measured output noise of the system. The low-frequency output noise of 40 nV/√Hz gets input-referred to 0.40 pA/√Hz. The transimpedance gain resistor is the dominant noise source with the operational amplifier contributing a negligible amount, reflecting one of the main benefits in using a JFET input amplifier in a high-gain transimpedance application. If the total output noise of the TIA is band limited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent output noise voltage can be derived by 式 3.

$$V_{OUTN} = \sqrt{(I_N R_F)^2 + 4kTR_F + {E_N}^2 + \frac{(E_N 2\pi C_D R_F F)^2}{3}} \quad (3)$$

where

- V_{OUTN} = Equivalent output noise when band-limited to F < 1 / (2ΩRfCf)
- I_N = Input current noise for the operational amplifier inverting input
- E_N = Input voltage noise for the operational amplifier
- C_D = Diode capacitance including operational amplifier and PCB parasitic capacitance
- F = Band-limiting frequency in Hz (usually a postfilter before further signal processing)
- 4 kT = 1.6 e – 20 J at T = 290K

図 8-5 shows the frequency response of the design. The 4.2-MHz bandwidth of the circuit approximately matches the theoretical value calculated using 式 2.

8.2.3 Application Curves

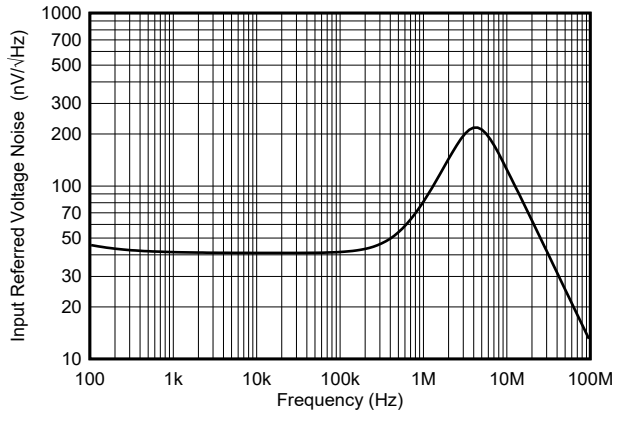


図 8-4. Total TIA noise over frequency

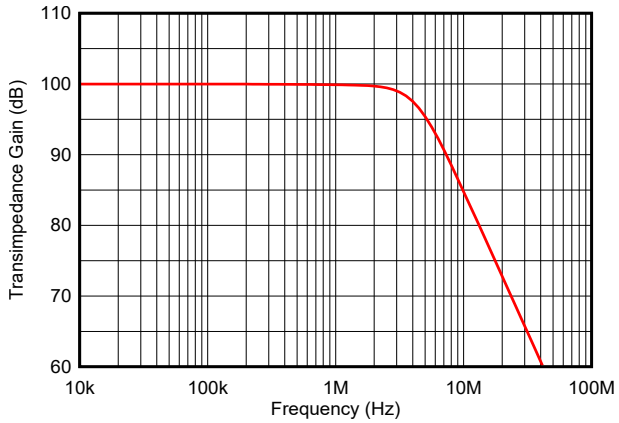


図 8-5. Closed-Loop bandwidth of TIA

8.3 Power Supply Recommendations

The OPA656 is intended to operate on supplies ranging from 8 V to 12 V. The OPA656 supports single-supply, split, balanced, and unbalanced bipolar supplies. The limit to lower supply-voltage operation is the useable input voltage range for the JFET-input stage. Operating from a single supply of 12 V can have numerous advantages. With the negative supply at ground, the dc errors due to the –PSRR term can be minimized. Typically, ac performance improves slightly at 12-V operation with a minimal increase in supply current.

8.4 Layout

8.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA656 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include the following.

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability. On the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band-limiting. Ground and power metal planes act as one of the plates of a capacitor, while the signal trace metal acts as the other separated by PCB dielectric. To reduce this unwanted capacitance, minimize the routing of the feedback network. A plane cutout around and underneath the inverting input pin on all ground and power planes is recommended. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.
2. **Minimize the distance (less than 0.25 inches) from the power-supply pins to high-frequency decoupling capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G- and NPO-type decoupling capacitors. These capacitors must have voltage ratings at least three times greater than the amplifiers maximum power supplies to provide a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequencies, must be used on the supply pins. These larger capacitors can be placed further from the device and shared among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserves the high-frequency performance of the OPA656.** Use low-reactance resistors. Small form-factor, surface-mount resistors work best and allow a tighter overall layout. The output pin and inverting input pin are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistor, if any, as close as possible to the inverting input and the output pin, respectively.

   Place other network components, such as noninverting input termination resistors, close to the package. Even with a low parasitic capacitance at the noninverting input, high external resistor values can create significant time constants that can degrade performance. When the OPA656 is configured as a conventional voltage amplifier, keep the resistor values as low as possible and consistent with the load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

8.4.1.1 Demonstration Fixtures

Two printed-circuit-boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA656 device in two package options. Both of these are offered as unpopulated PCBs, delivered with a user's guide. 表 8-2 shows the summary information for these fixtures.

表 8-2. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA656U	SO-8	DEM-OPA-SO-1A	SBOU009
OPA656N	SOT23-5	DEM-OPA-SOT-1A	SBOU010

Request the demonstration fixtures at the Texas Instruments website (www.ti.com) through the OPA656 product folder.

8.4.1.2 Thermal Considerations

The OPA656 does not require a heat sink or airflow in most applications. The following section describes how the maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

The operating junction temperature (T_J) is given by $T_A + P_D \times R_{\theta JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}), and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the device. The P_{DL} depends on the required output signal and load, but for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced, bipolar supplies). Under this condition, $P_{DL} = V_S{}^2 / (4 \times R_L)$, where R_L includes feedback network loading.

Be aware that the power in the output stage, and not into the load, determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA656N (SOT23-5 package) in the circuit of 図 8-1 operating at the maximum specified ambient temperature of 85°C and driving a grounded 100-Ω load.

$$P_D = 10\ V \times 16.8\ mA + 5^2 / (4 \times (100\ \Omega \parallel 800\ \Omega)) = 238\ mW \quad (4)$$

$$\text{Maximum } T_J = 85°C + (0.238\ W \times 154°C/W) = 121.6°C. \quad (5)$$

All actual applications operate at a lower internal power and junction temperature.

8.4.2 Layout Example

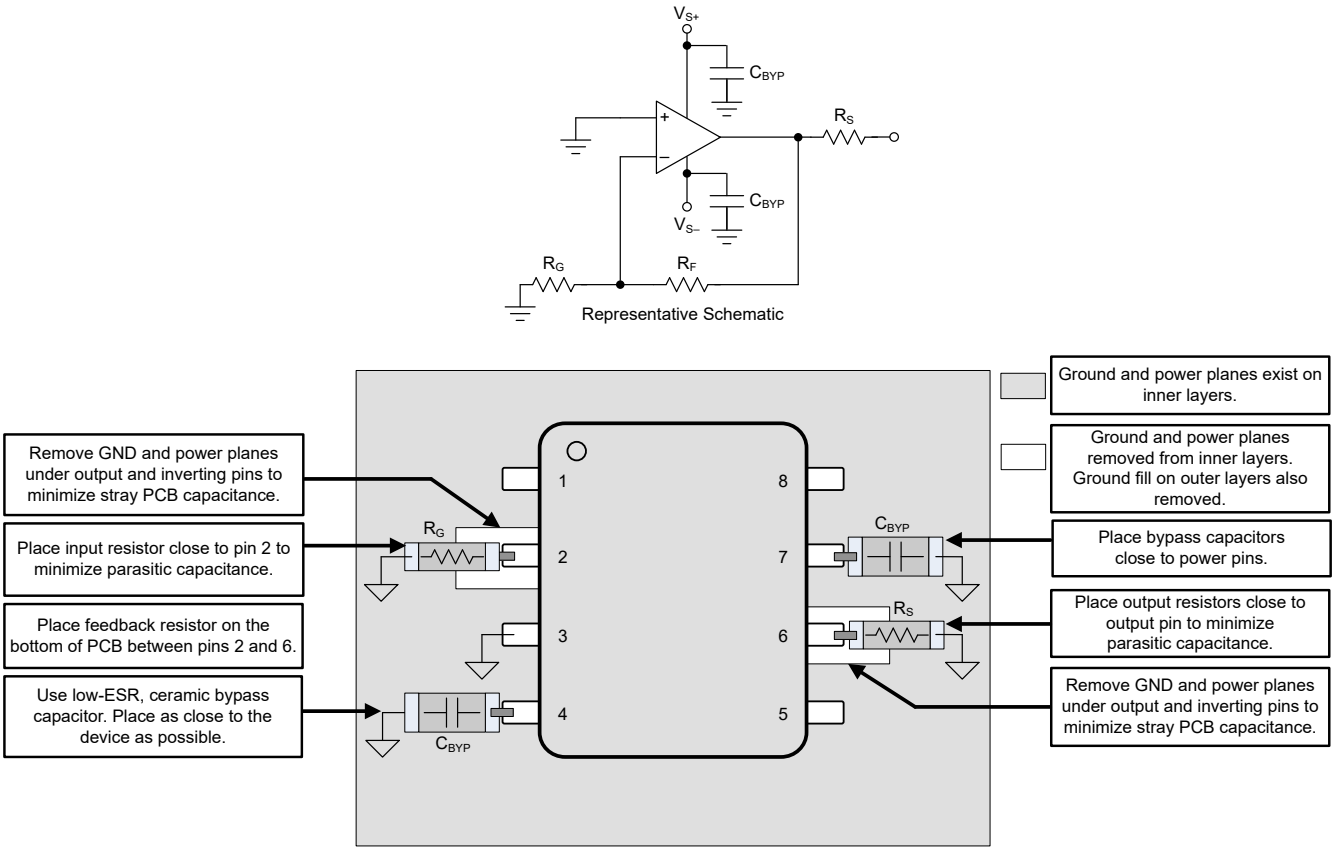


図 8-6. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *Optical Front-End System Reference Design*
- Texas Instruments, *Maximizing the Dynamic Range of Analog TIA Front-End* technical brief
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.5 静電気放電に関する注意事項

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (April 2015) to Revision I (February 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「特長」、「アプリケーション」、「概要」、「デバイス比較表」、「機能説明」、「デバイスの機能モード」、「アプリケーションと実装」、「電源に関する推奨事項」、「レイアウト」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」セクションを更新	1
• Added Supply turn-on and turn-off rate, continuous input and output current specifications to *Absolute Maximum Ratings* Table	4
• Updated footnote on *Absolute Maximum Ratings* table to add additional clarification	4

- Deleted Machine Model (MM) specification from *ESD Ratings Table* 4
- Updated thermal specifications for D and DBV package in *Thermal Information* table..... 4
- Updated the test conditions to add additional clarity, updated the table format and deleted the Test Level column on *Electrical Characteristics* table..... 5
- Changed the test condition from T_J = 25°C to T_A ≅ 25°C across *Electrical Characteristics* section..... 5
- Updated the *Electrical Characteristics AC performance* section with improved typical small-signal bandwidth, 0.1 dB flatness, large-signal bandwidth, slew rate, voltage noise, and distortion parameters..... 5
- Deleted differential gain and differential phase parameter from *Electrical Characteristics* section..... 5
- Changed the input current noise at f = 100 kHz from 1.3 fA/√Hz to 5 fA/√Hz..... 5
- Updated the *Electrical Characteristics DC Performance, Input, Output, and Power supply* sections with improved typical open loop gain, CMRR and PSRR parameters..... 5
- Deleted 0°C to +70°C conditions across *Electrical Characteristics* section..... 5
- Changed input offset current maximum from ±10 pA to ±20 pA..... 5
- Changed typical and maximum most negative input voltage for CMRR > 77 dB from –4.5 V and –4 V to –4.3 V and –3.9 V respectively..... 5
- Changed maximum most negative input voltage at –40°C to +85°C for CMRR > 77 dB from –3.8 V to –3.7 V 5
- Changed the typical common mode input impedance from 10^{12} || 0.7 to 10^{12} || 0.4..... 5
- Changed the typical differential mode input impedance from 10^{12} || 2.8 to 10^{10} || 2.6..... 5
- Changed minimum sourcing output current over –40°C to +85°C from 46 mA to 45 mA..... 5
- Changed maximum sinking output current over –40°C to +85°C from –46 mA to –45 mA..... 5
- Changed typical and maximum quiescent current from 14 mA to 15 mA and 16 mA to 16.7 mA respectively.. 5
- Changed maximum quiescent current over –40°C to +85°C from 16.3 mA to 16.8 mA..... 5
- Updated the *High Grade DC Specifications* section with improved typical CMRR and PSRR parameters..... 6
- Changed input bias current and input offset current maximum in *High Grade DC Specifications* section from ±5 pA to ±20 pA..... 6
- Changed CMRR minimum in *High Grade DC Specifications* section from 88 dB to 84 dB..... 6
- Changed CMRR minimum in *High Grade DC specifications* over –40°C to +85°C from 84 dB to 83 dB..... 6
- Updated *Typical Characteristics: V_S = ±5 V* section..... 7
- Changed the continuous current rating of the input protection diodes from 30 mA to 10 mA..... 12

Changes from Revision G (November 2008) to Revision H (April 2015) **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。..... 1

Changes from Revision F (March 2006) to Revision G (November 2008) **Page**

- Changed Storage temperature range from –40°C to 125°C to –65°C to 125°C..... 4
- Deleted in the DC Performance section: Drift from Input Offset Current specifications..... 5

Changes from Revision E (March 2006) to Revision F (November 2008) **Page**

- Added Design-In Tools paragraph and table 17

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA656N/250	OBSOLETE	SOT-23	DBV	5		RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B56	
OPA656NB/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	B56	Samples
OPA656U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	OPA 656U	
OPA656U/2K5	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	OPA 656U	
OPA656UB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	OPA 656U B	
OPA656UB/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA (656U, B 656U) B	Samples
OPA656UG4	NRND	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

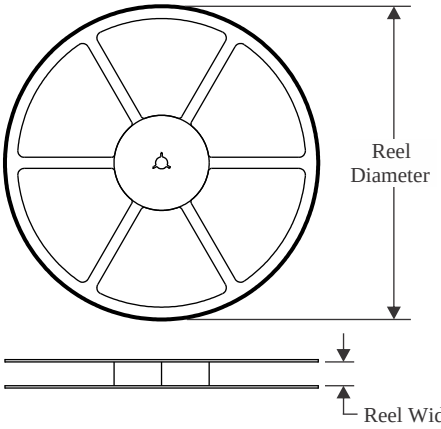
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

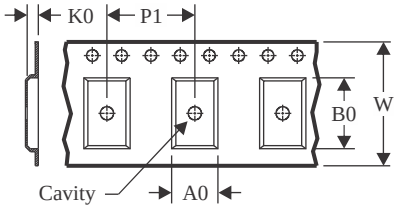
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

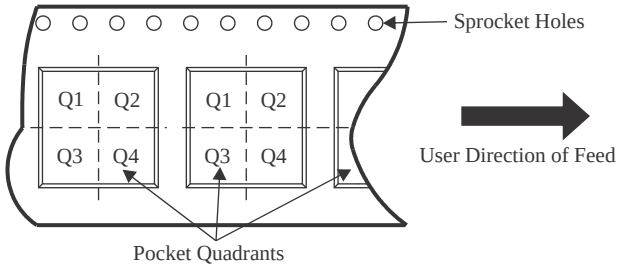


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

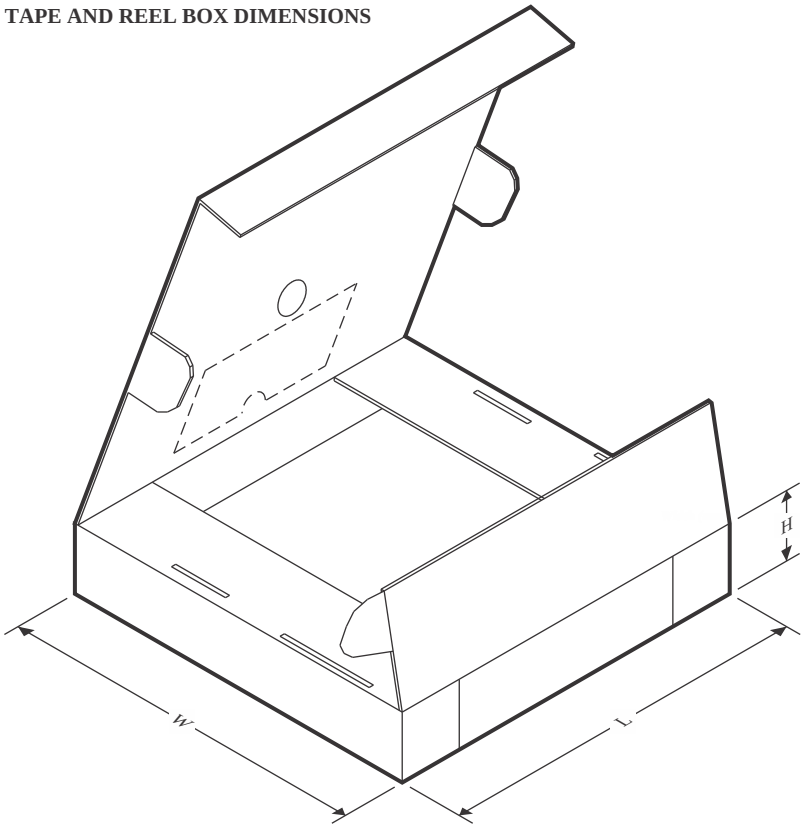
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA656NB/250	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA656UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA656UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

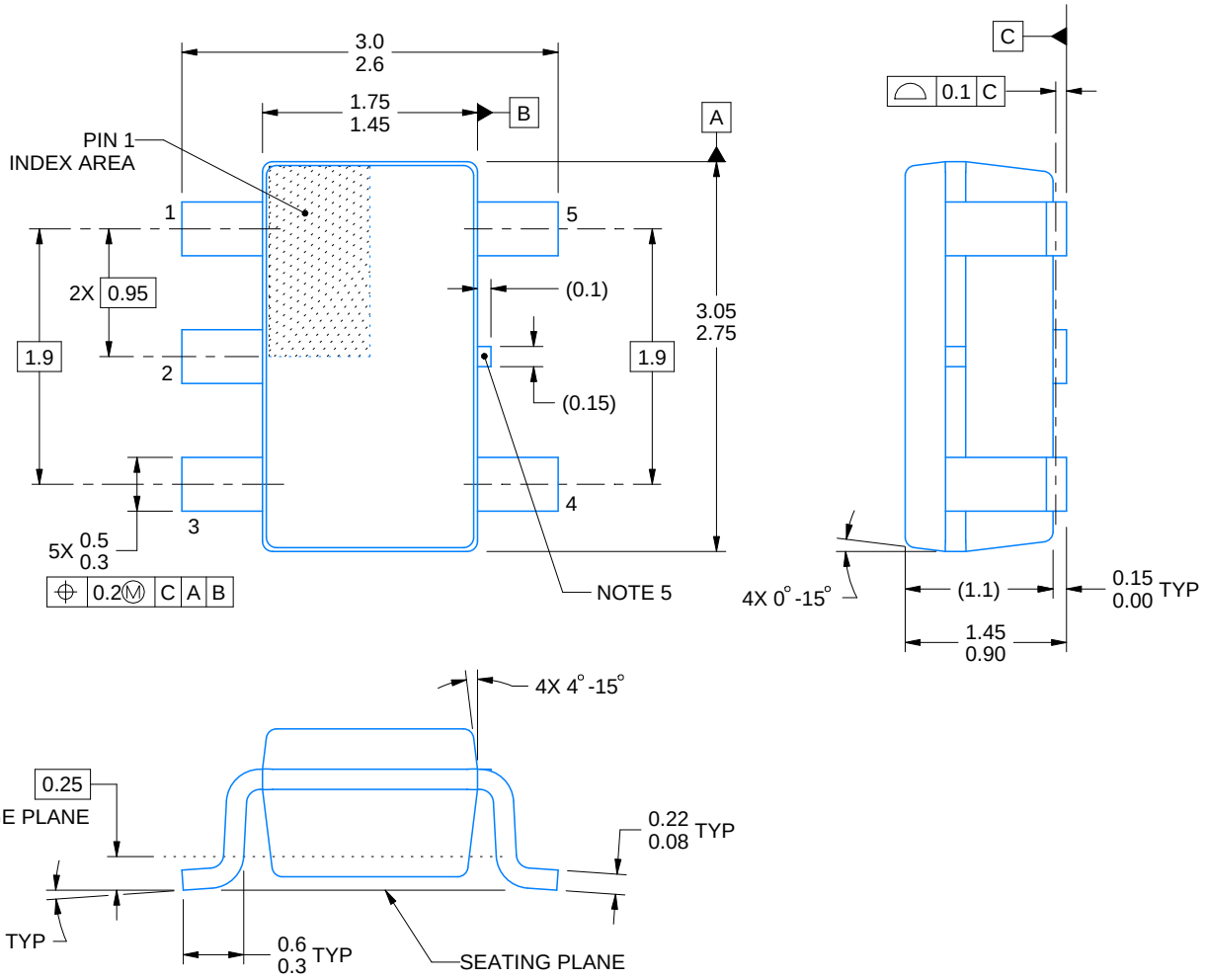
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA656NB/250	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA656UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA656UB/2K5	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

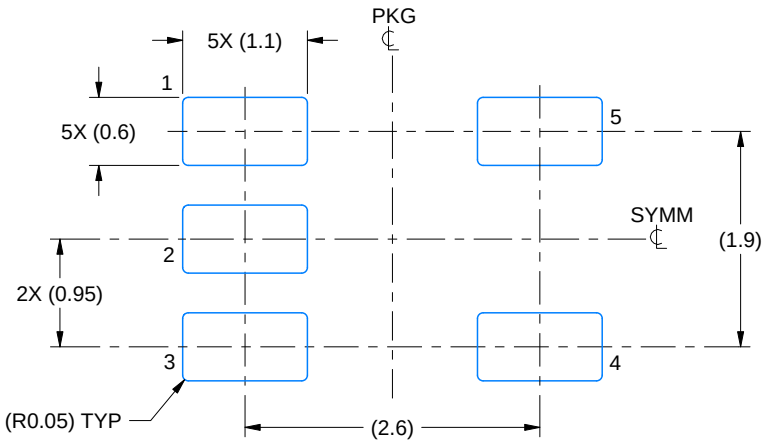
SMALL OUTLINE TRANSISTOR



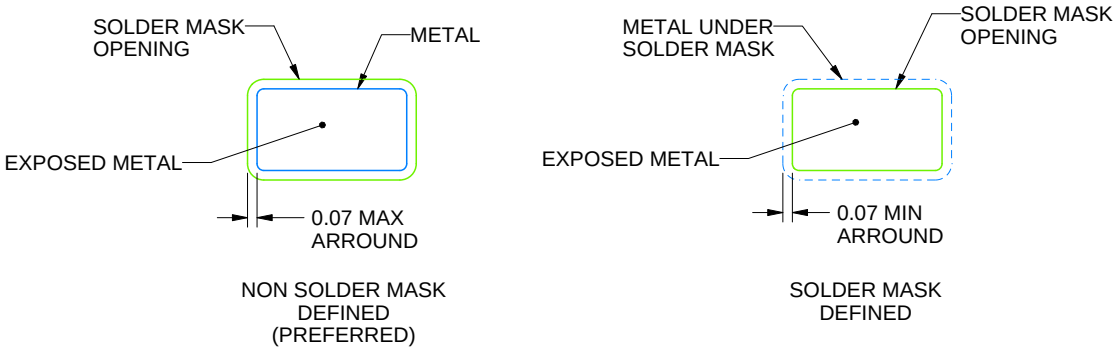
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

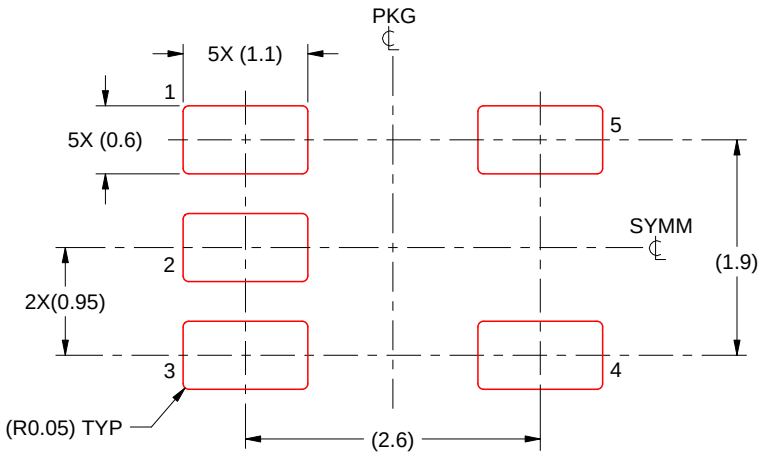


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

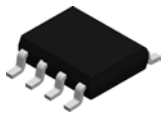


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

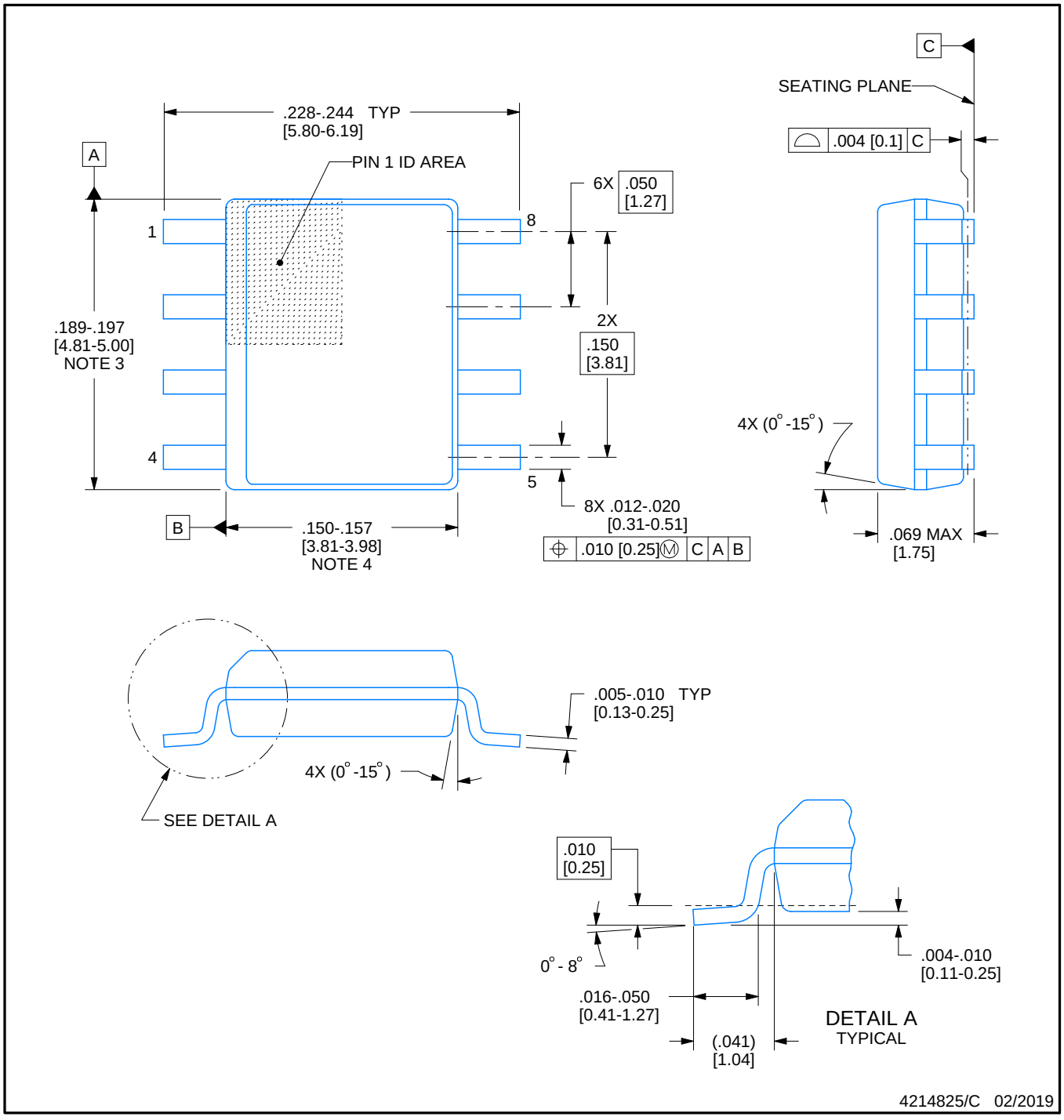


PACKAGE OUTLINE

D0008A

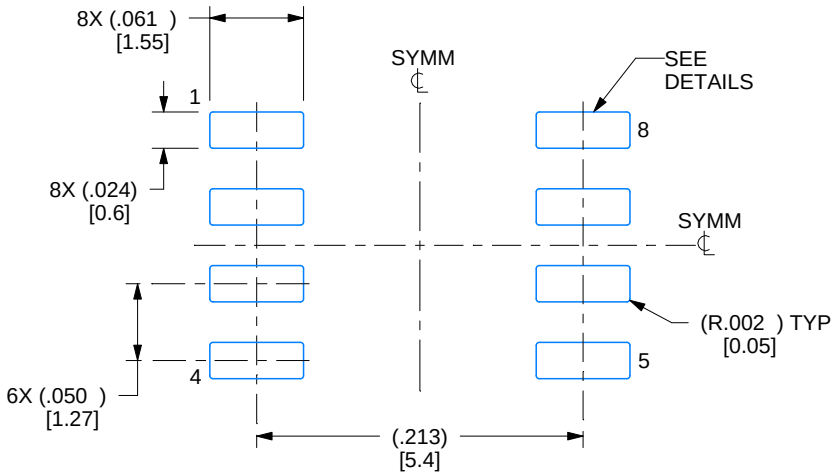
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

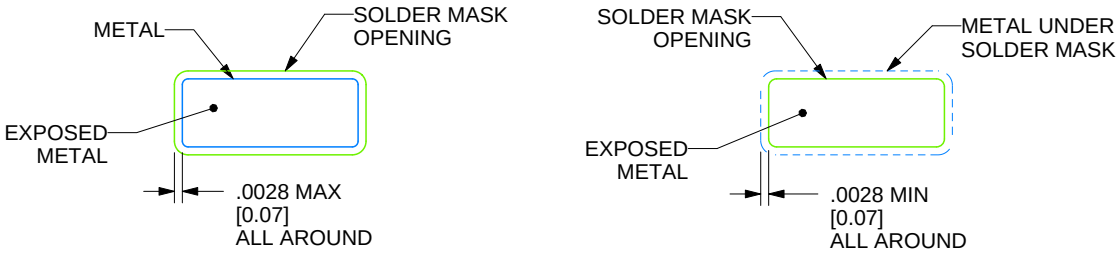


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

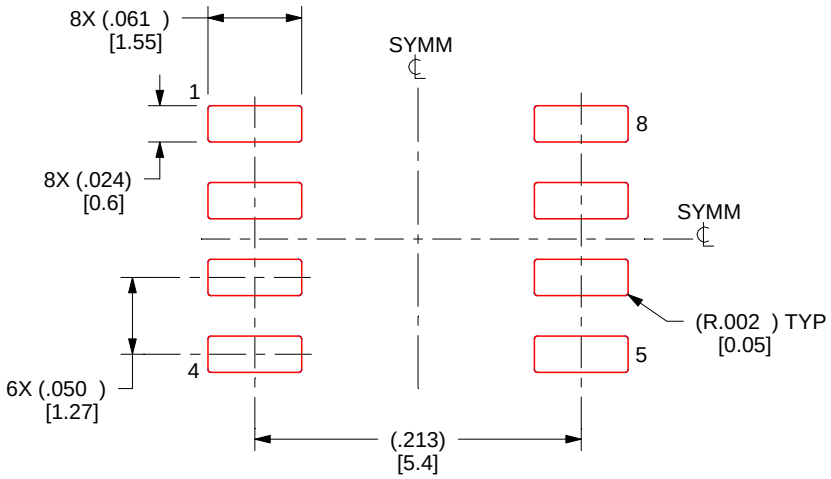
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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