OPA356-Q1 200MHz CMOSオペアンプ

1 特長

- **車載アプリケーション向けに認定済み**
- **下記内容でAEC-Q100認定済み**
  - デバイス温度グレード: 動作時周囲温度範囲 –40°C～125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC6
- **ユニティ・ゲイン帯域幅**: 450MHz
- **広い帯域幅**: 200MHz GBW
- **高いスルー・レート**: 360V/µs
- **低ノイズ**: 5.8nV/√Hz
- **非常に優れたビデオ性能**
  - 差動ゲイン: 0.02%
  - 差動位相: 0.05°
  - 0.1dBのゲイン・フラットネス: 75MHz
- **入力範囲にグランドを含む**
- **レール・ツー・レール出力(100mV以内)**
- **低い入力バイアス電流**: 3pA
- **サーマル・シャットダウン**
- **単一電源電圧範囲**: 2.5V～5.5V

2 アプリケーション

- **インフォテインメント・システム**
- ADASシステム
- **レーダー**
- **動的安定性制御(DSC)**

3 概要

OPA356-Q1は高速の電圧帰還型CMOSオペアンプで、広い帯域幅を必要とするビデオおよびその他のアプリケーション用に設計されています。OPA356-Q1はユニティ・ゲイン安定で、大きな出力電流を駆動できます。差動ゲインは0.02%、差動位相は0.05°です。静止電流はわずか8.3mAです。

OPA356-Q1は、最低2.5V (±1.25V)、最高5.5V (±2.75V)のシングルまたはデュアル電源で動作するよう最適化されています。同相入力範囲はグランドより100mV下、V+より1.5V上までです。出力スイングはレールから100mV以内で、広いダイナミック・レンジに対応しています。

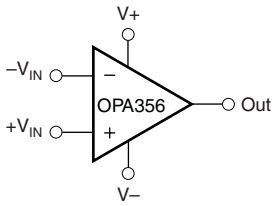
OPA356-Q1はSOT23-5パッケージで供給され、-40℃～125℃の範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA356-Q1	SOT-23 (5)	2.90mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



目次

4 改訂履歴

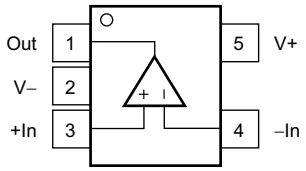
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2009年3月 発行のものから更新 **Page**

- 「*製品情報*」表、「*ESD定格*」表、「*熱に関する情報*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- 「特長」にAEC-Q100認定済みの箇条書き項目を 追加 ... 1
- Deleted *Ordering Information* table ... 3
- Deleted footnote 2 from *Absolute Maximum Ratings* table ... 4
- Deleted the SR, t_r, t_f, t_{settle}, and Overload recovery time rows from the *Electrical Characteristics* table and moved to the *Timing Requirements* table ... 5
- Changed *Layout Guidelines* title from *PCB Layout* ... 19

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Out	O	Output pin
2	V–	—	Negative power supply
3	+In	I	Noninverting input pin
4	–In	I	Inverting input pin
5	V+	—	Positive power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V+ to V–		7.5	V
V_{IN}	Signal input pins voltage range	–0.5	(V+) + 0.5	V
	V– current		10	mA
	Output short-circuit duration(2)	Continuous		
T_A	Operating free-air temperature range	–40	125	°C
T_J	Junction temperature		160	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.7	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA356-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_S = 2.7 V to 5.5 V, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage		V_S = 5 V, V_{CM} = V– + 0.8 V	25°C		±2	±9	mV
				Full range			±15	
$\Delta V_{OS}/\Delta T$	Offset voltage drift over temperature			Full range		±7		µV/°C
PSRR	Offset voltage drift vs power supply		V_S = 2.7 V to 5.5 V, V_{CM} = V_S / 2 – 0.15 V	25°C		±80	±350	µV/V
I_B	Input bias current			25°C		3	±50	pA
I_{OS}	Input offset current			25°C		±1	±50	pA
V_n	Input voltage noise density		f = 1 MHz	25°C		5.8		nV/√Hz
I_n	Input current noise density		f = 1 MHz	25°C		50		fA/√Hz
V_{CM}	Input common-mode voltage range			25°C	V– – 0.1		V+ – 1.5	V
CMRR	Input common-mode rejection ratio		V_S = 5.5 V, –0.1 V < V_{CM} < 4 V	25°C	66	80		dB
				Full range	66			
Z_{ID}	Differential input impedance			25°C		10^{13} || 1.5		Ω || pF
Z_{ICM}	Common-mode input impedance			25°C		10^{13} || 1.5		Ω || pF
A_{OL}	Open-loop gain		V_S = 5 V, 0.3 V < V_O < 4.7 V	25°C	84	92		dB
				Full range	80			
$f_{–3dB}$	Small-signal bandwidth		G = 1, V_O = 100 mVp-p, R_F = 0 Ω	25°C		450		MHz
			G = 2, V_O = 100 mVp-p, R_L = 50 Ω			100		
			G = 2, V_O = 100 mVp-p, R_L = 150 Ω			170		
			G = 2, V_O = 100 mVp-p, R_L = 1 kΩ			200		
GBW	Gain-bandwidth product		G = 10, R_L = 1 kΩ	25°C		200		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness		G = 2, V_O = 100 mVp-p, R_F = 560 Ω	25°C		75		MHz
SR	Slew rate		V_S = 5 V, G = 2, 4-V output step	25°C		+300		V/µs
						–360		
t_r, t_f	Rise and fall times		G = 2, V_O = 200 mVp-p, 10% to 90%	25°C		2.4		ns
			G = 2, V_O = 2 Vp-p, 10% to 90%			8		
t_{settle}	Settling time	0.1%	V_S = 5 V, G = 2, 2-V output step	25°C		30		ns
		0.01%				120		
	Overload recovery time		V_{IN} × Gain = V_S	25°C		8		ns
	Harmonic distortion	Second harmonic	G = 2, f = 1 MHz, V_O = 2 Vp-p, R_L = 200 Ω	25°C		–81		dBc
		Third harmonic		25°C		–93		
	Differential gain error		NTSC, R_L = 150 Ω	25°C		0.02%		
	Differential phase error		NTSC, R_L = 150 Ω	25°C		0.05		°
	Voltage output swing from rail		V_S = 5 V, R_L = 150 Ω, A_{OL} > 84 dB	25°C		0.2	0.3	V
			V_S = 5 V, R_L = 1 kΩ			0.1		
			V_S = 5 V, R_L = 50 Ω			0.4	0.6	
I_O	Output current (2)	Continuous		25°C	±60			mA
		Peak	V_S = 5 V		±100			
			V_S = 3 V			±80		
	Short-circuit current			25°C		+250		mA
						–200		
	Closed-loop output impedance			25°C		0.02		Ω
I_Q	Quiescent current		V_S = 5 V, I_O = 0	25°C		8.3	11	mA
				Full range			14	
	Thermal shutdown junction temperature		Shutdown	25°C		160		°C
			Reset from shutdown			140		

(1) Full range T_A = –40°C to 125°C.
(2) See Figure 20.

6.6 Typical Characteristics

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

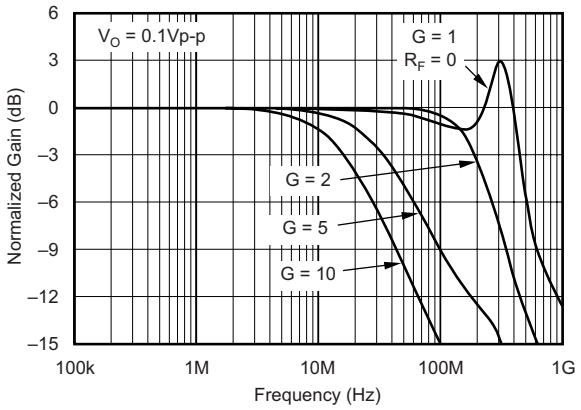


Figure 1. Noninverting Small-Signal Frequency Response

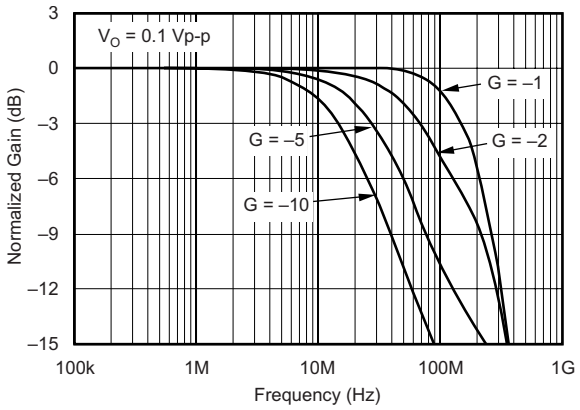


Figure 2. Inverting Small-Signal Frequency Response

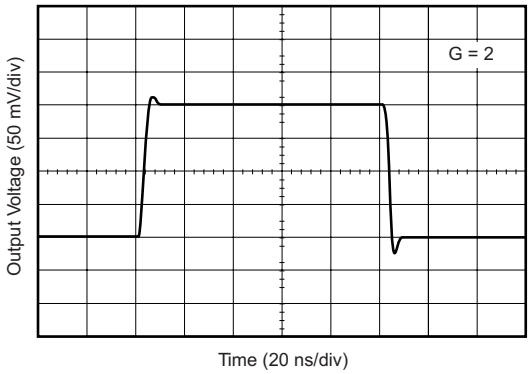


Figure 3. Noninverting Small-Signal Step Response

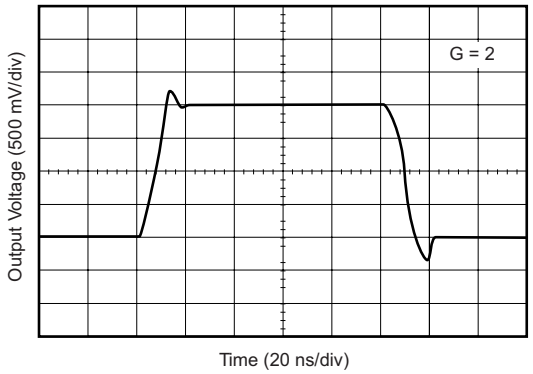


Figure 4. Noninverting Large-Signal Step Response

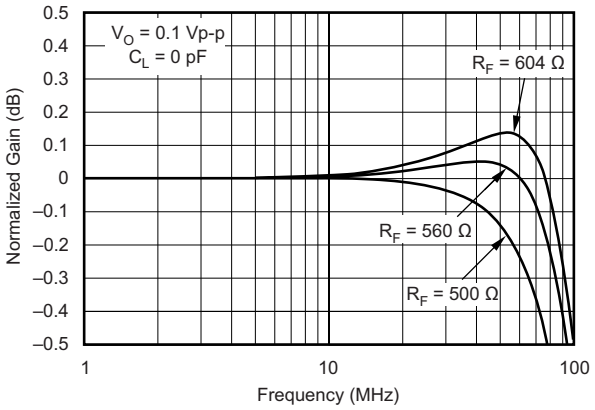


Figure 5. 0.1-dB Gain Flatness for Various R_F

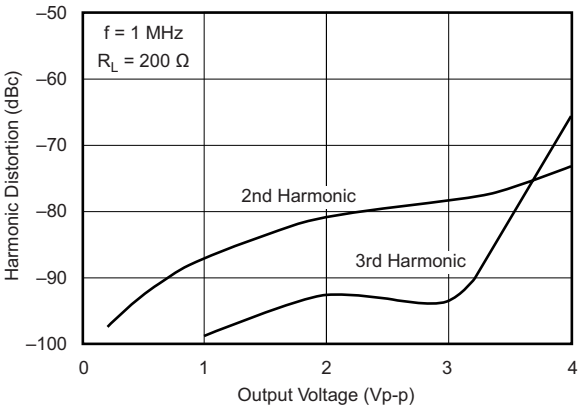


Figure 6. Harmonic Distortion vs Output Voltage

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

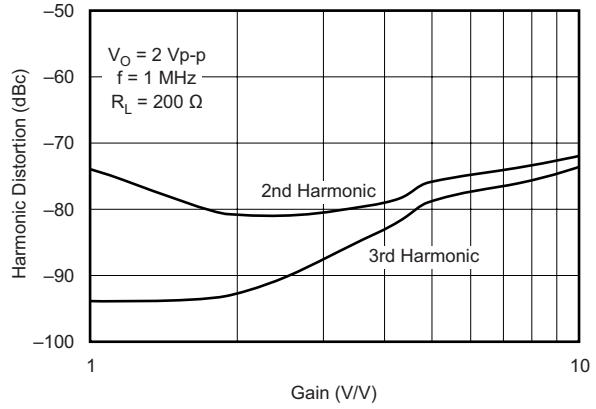


Figure 7. Harmonic Distortion vs Non-Inverting Gain

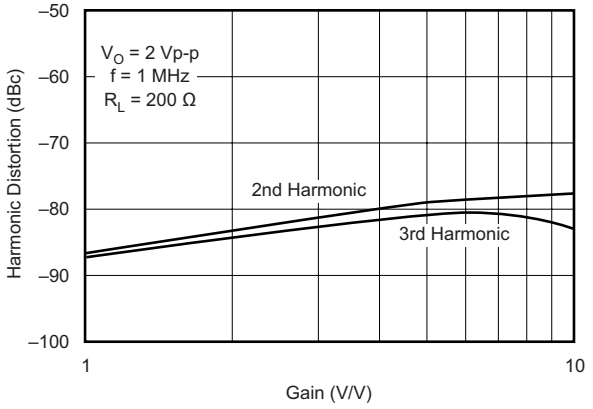


Figure 8. Harmonic Distortion vs Inverting Gain

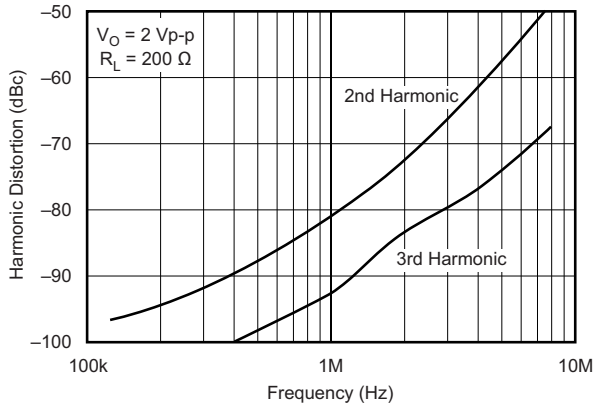


Figure 9. Harmonic Distortion vs Frequency

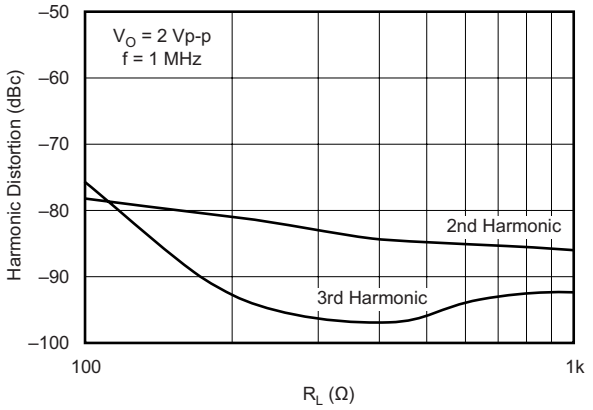


Figure 10. Harmonic Distortion vs Load Resistance

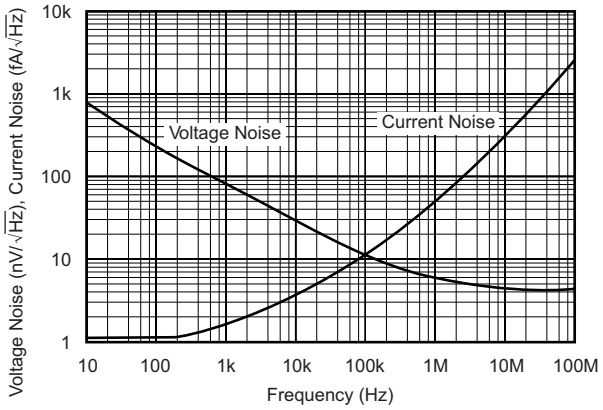


Figure 11. Input Voltage and Current Noise Spectral Density vs Frequency

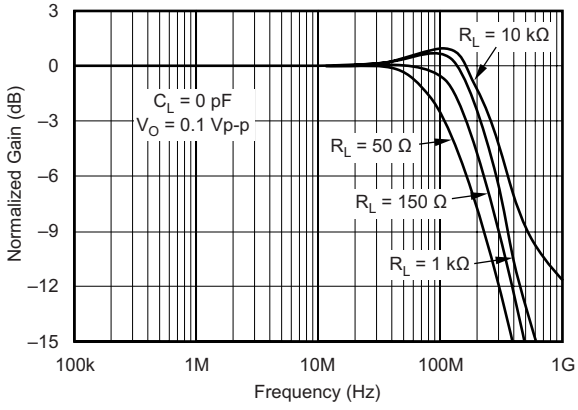


Figure 12. Frequency Response for Various R_L

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

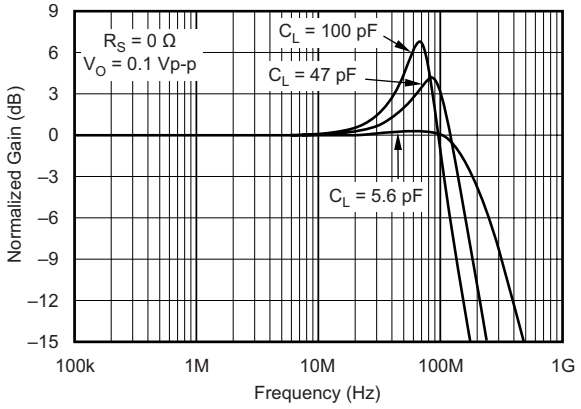


Figure 13. Frequency Response for Various C_L

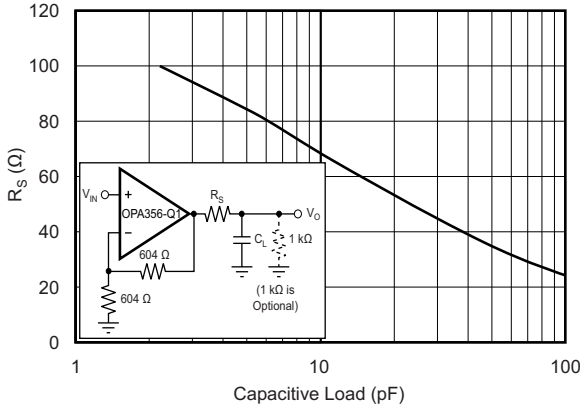


Figure 14. Recommended R_S vs Capacitive Load

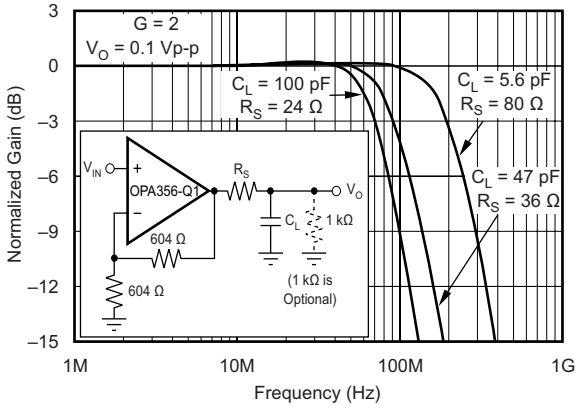


Figure 15. Frequency Response vs Capacitive Load

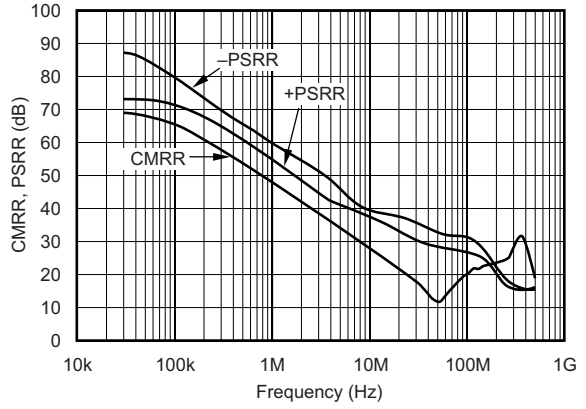


Figure 16. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

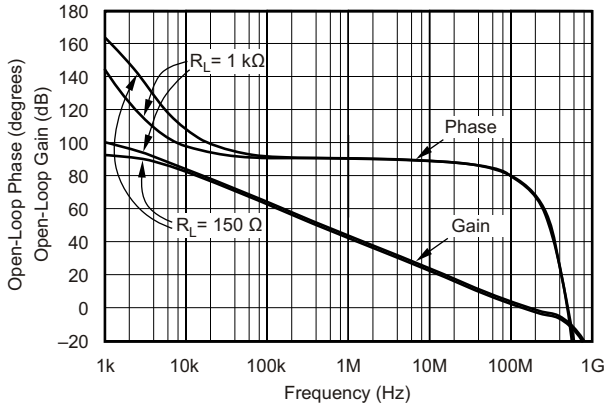


Figure 17. Open-Loop Gain and Phase

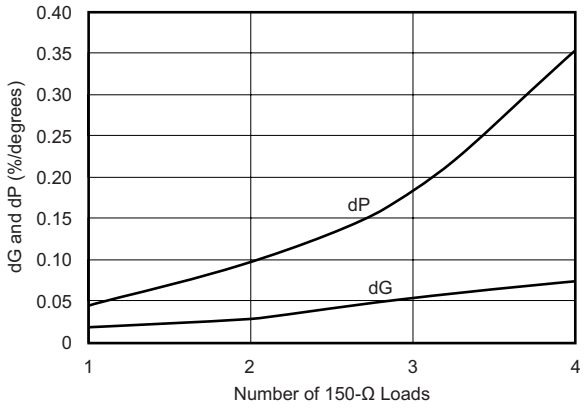


Figure 18. Composite Video Differential Gain and Phase

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

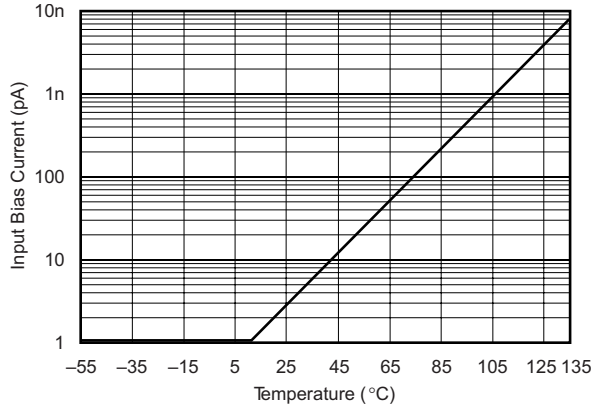


Figure 19. Input Bias Current vs Temperature

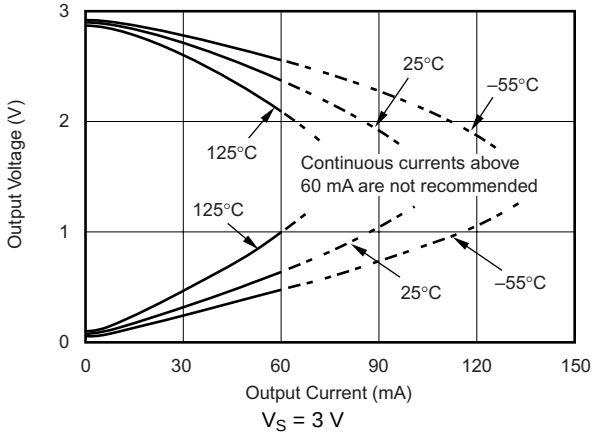


Figure 20. Output Voltage Swing vs Output Current

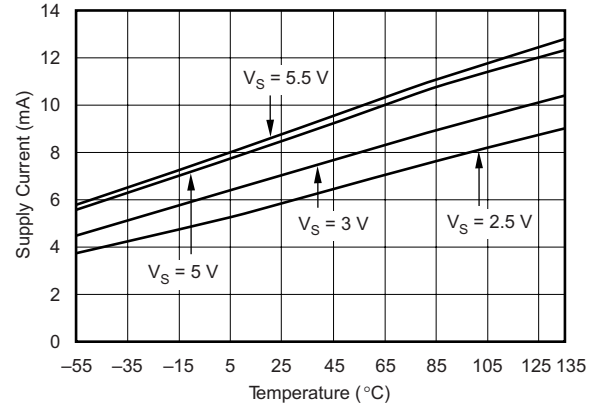


Figure 21. Supply Current vs Temperature

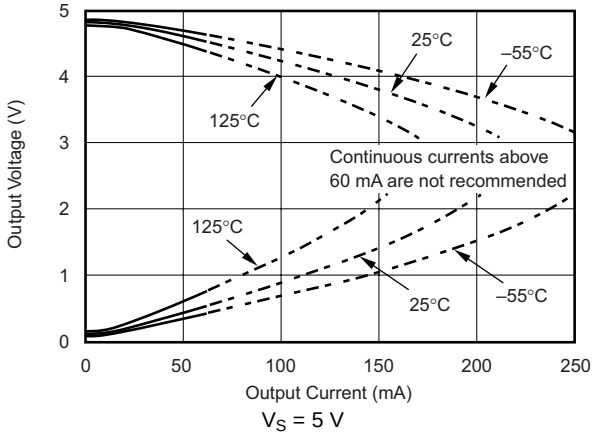


Figure 22. Output Voltage Swing vs Output Current

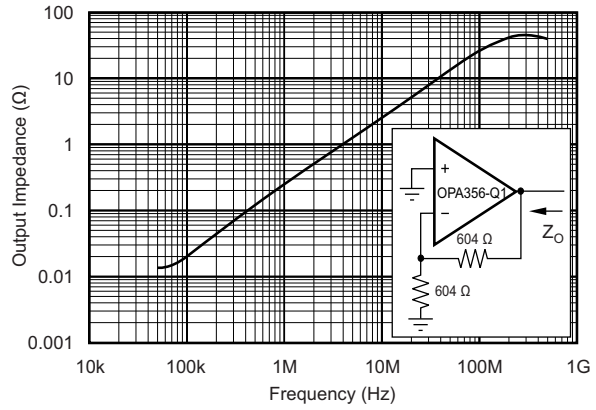


Figure 23. Closed-Loop Output Impedance vs Frequency

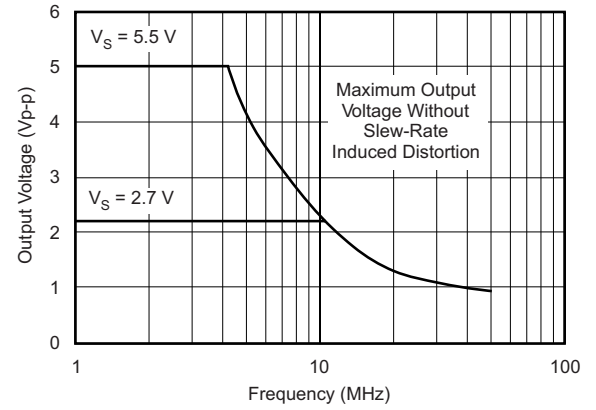


Figure 24. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

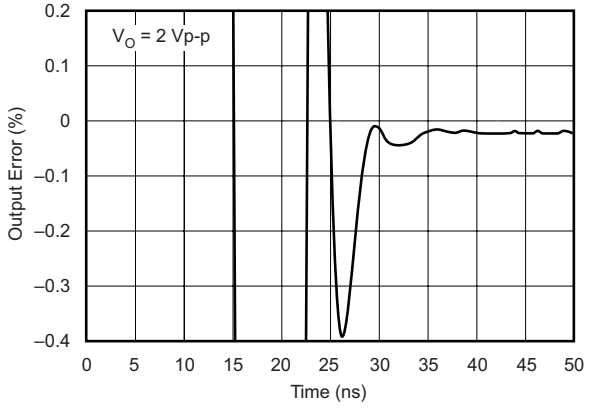


Figure 25. Output Settling Time to 0.1%

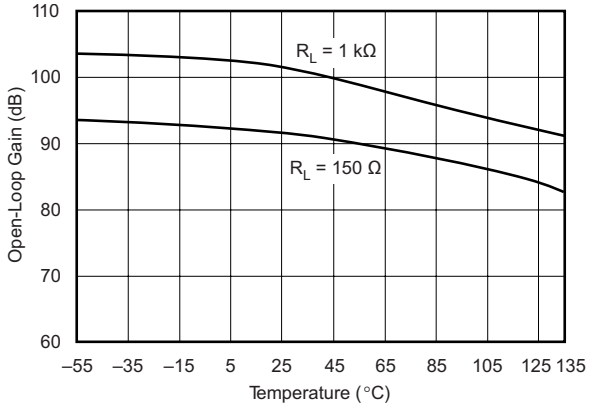


Figure 26. Open-Loop Gain vs Temperature

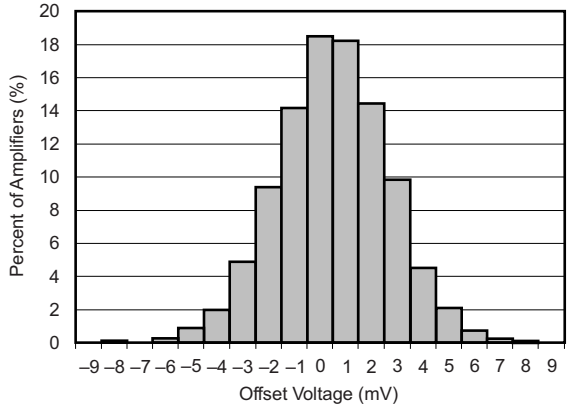


Figure 27. Offset Voltage Production Distribution

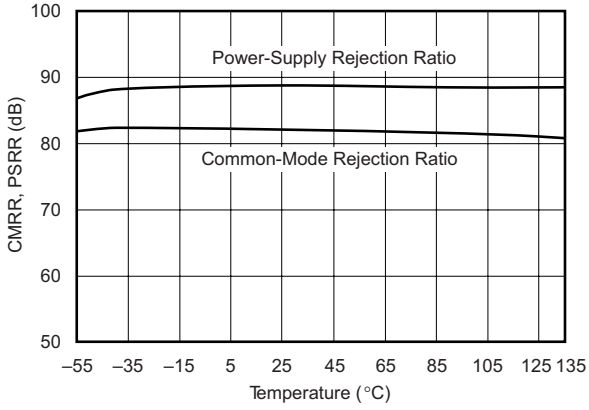


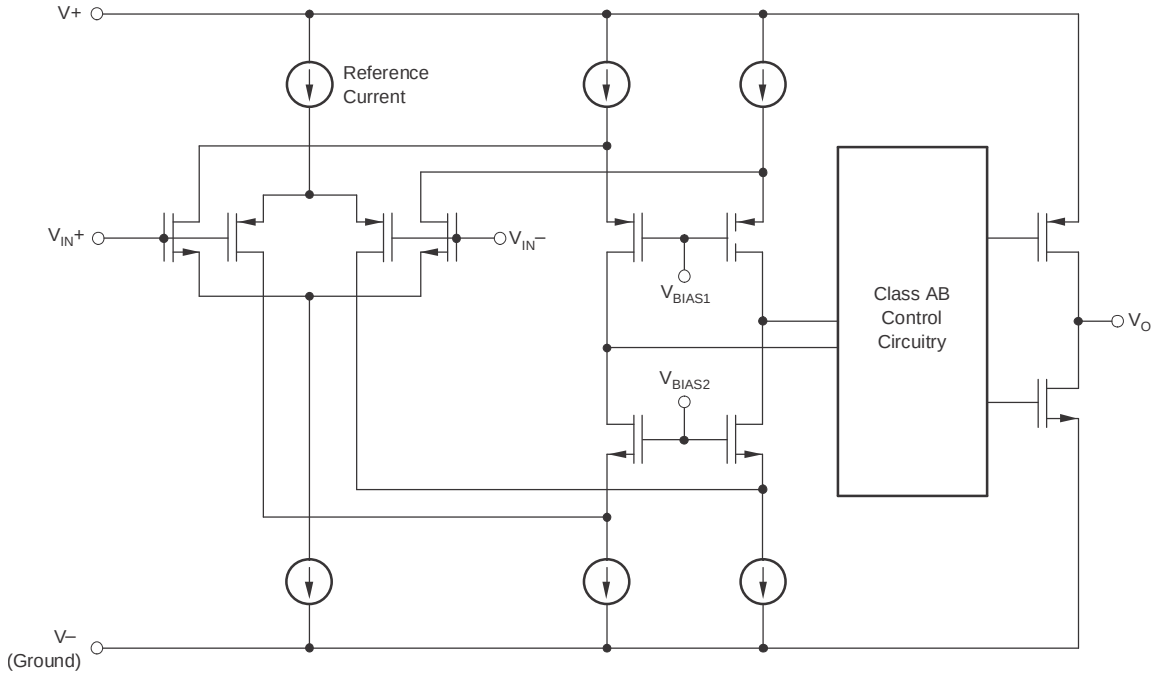
Figure 28. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

7 Detailed Description

7.1 Overview

The OPA356-Q1 operational amplifier is a high-speed, 360-V/μs, amplifier, making the device a great option for transimpedance applications. The device is unity-gain stable and can operate on a single-supply voltage (2.7 V to 5.5 V), or a split-supply voltage (±1.35 V to ±2.75 V), making the device highly versatile and simple to use. The OPA356-Q1 amplifier is specified from 2.7 V to 5.5 V and over the automotive temperature range of –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA356-Q1 is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

7.3.2 Output Drive

The output stage of the OPA356-Q1 is capable of driving a standard back-terminated 75-Ω video cable. A back-terminated transmission line does not exhibit a capacitive load to its driver. A properly back-terminated 75-Ω cable does not appear as capacitance; the cable presents only a 150-Ω resistive load to the OPA356-Q1 output.

The output stage can supply high short-circuit current (typically over 200 mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA356-Q1 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

NOTE

TI does not recommend running a continuous dc current in excess of ±60 mA. See Figure 20 in the *Typical Characteristics* section.

7.4 Device Functional Modes

The OPA356-Q1 is powered on when the supply is connected. The device can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application. The device can also be used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (for example, V– is set to –3.5 V and V+ is set to 1.5 V).

8 Application and Implementation

8.1 Application Information

The OPA355-Q1 is a CMOS, high-speed, voltage-feedback, operational amplifier (op-amp) designed for general-purpose applications.

The amplifier features a 200-MHz gain bandwidth and 300-V/μs slew rate, but the device is unity-gain stable and operates as a 1-V/V voltage follower.

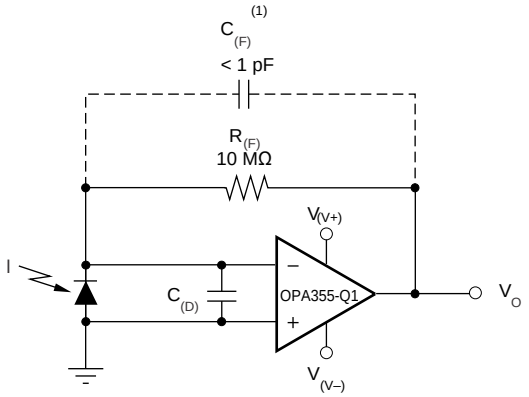
The input common-mode voltage range of the device includes ground, which allows the OPA356-Q1 to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

8.2 Typical Applications

8.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPA356-Q1 a preferred wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 29, are the expected diode capacitance ($C_{(D)}$), which must include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF), the desired transimpedance gain ($R_{(FB)}$), and the gain-bandwidth (GBW) for the OPA356-Q1 (20 MHz). With these three variables set, the feedback capacitor value ($C_{(FB)}$) is set to control the frequency response. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$, which is 0.2 pF for a typical surface-mount resistor.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

Figure 29. Dual-Supply Transimpedance Amplifier

8.2.1.1 Design Requirements

PARAMETER	VALUE
Supply voltage $V_{(V+)}$	2.5 V
Supply voltage $V_{(V–)}$	–2.5 V

8.2.1.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole must be set to:

$$\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (1)$$

Use Equation 2 to calculate the bandwidth.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (2)$$

For other transimpedance bandwidths, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), or OPA656 and OPA657 (400-MHz GBW).

For single-supply applications, the +INx input can be biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in Figure 30. This bias voltage appears across the photodiode, providing a reverse bias for faster operation.

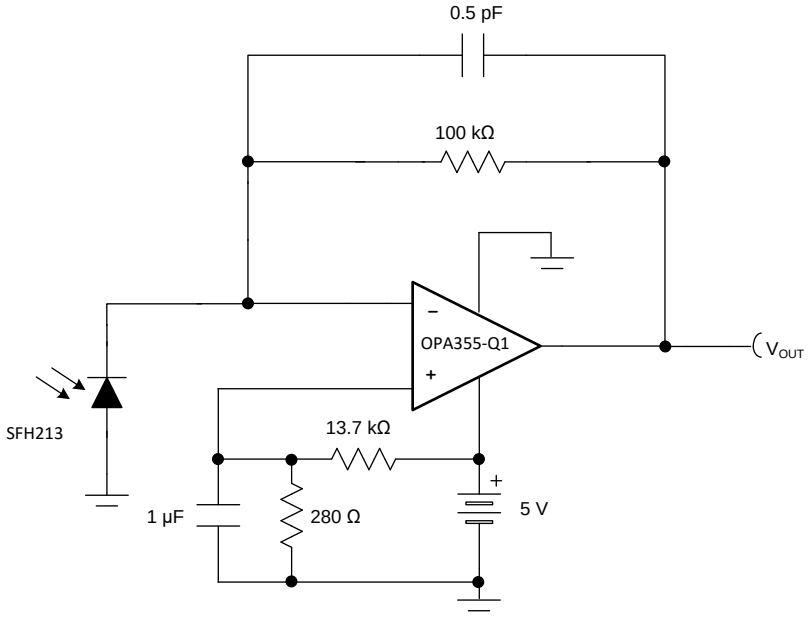


Figure 30. Single-Supply Transimpedance Amplifier

For additional information, see the *Compensate Transimpedance Amplifiers Intuitively* application bulletin.

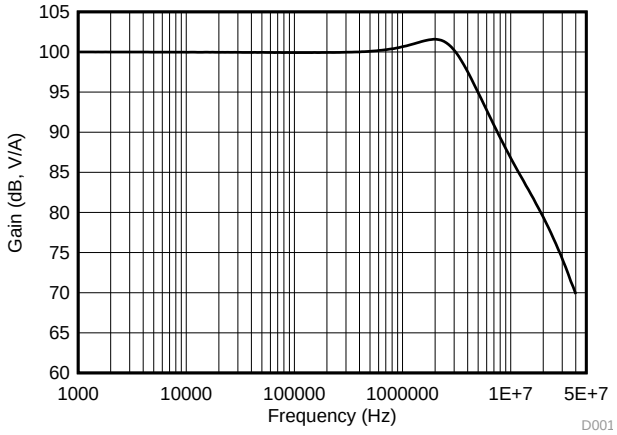
8.2.1.2.1 Optimizing The Transimpedance Circuit

To achieve the best performance, select components according to the following guidelines:

1. For lowest noise, select $R_{(FB)}$ to create the total required gain. Using a lower value for $R_{(FB)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(FB)}$ increases with the square-root of $R_{(FB)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the $R_{(FB)}$ to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, see the *Noise Analysis of FET Transimpedance Amplifiers* and *Noise Analysis for High-Speed Op Amps* application bulletins).

8.2.1.3 Application Curve



–3 dB bandwidth is 4.56 MHz

Figure 31. AC Transfer Function

8.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 32, where ($V_{(+INx)} = V_S – I_{(BIAS)} \times R_{(S)}$). The last term, $I_{(BIAS)} \times R_{(S)}$, shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, an op amp with very low input bias current must be used with high impedance sensors. This low current keeps the error contribution by $I_{(BIAS)} \times R_{(S)}$ less than the input voltage noise of the amplifier, so that the input voltage noise does not become the dominant noise factor. The OPA356-Q1 op amp features very low input bias current (typically 200 fA), and is therefore a preferred choice for such applications.

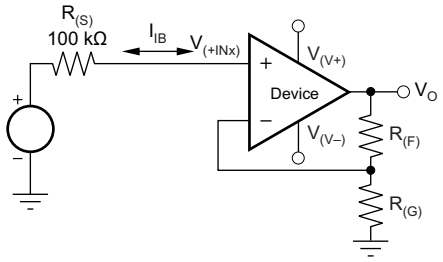
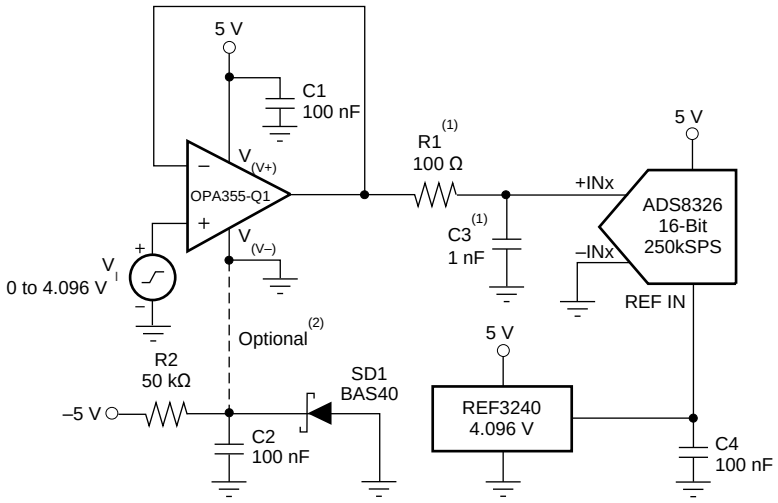


Figure 32. Noise as a Result of $I_{(BIAS)}$

8.2.3 Driving ADCs

The OPA356-Q1 op amps are designed for driving sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPA356-Q1 to drive ADCs without degradation of differential linearity and THD.

The OPA356-Q1 can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. Figure 33 shows the OPA356-Q1 configured to drive the ADS8326.



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3-V supply to allow output swing to true ground potential.

Figure 33. Driving the ADS8326

8.2.4 Active Filter

The OPA356-Q1 is designed for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 34 depicts a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is preferred for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (see Figure 35).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

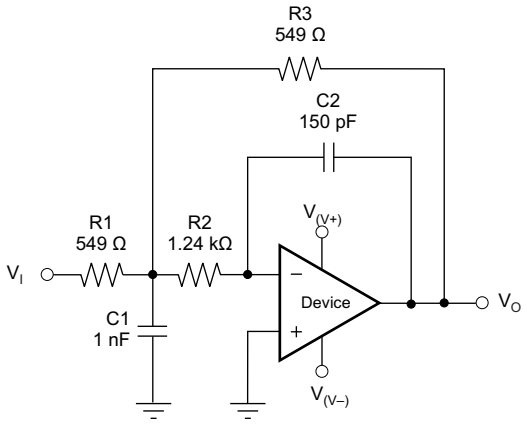


Figure 34. Second-Order Butterworth 500-kHz Low-Pass Filter

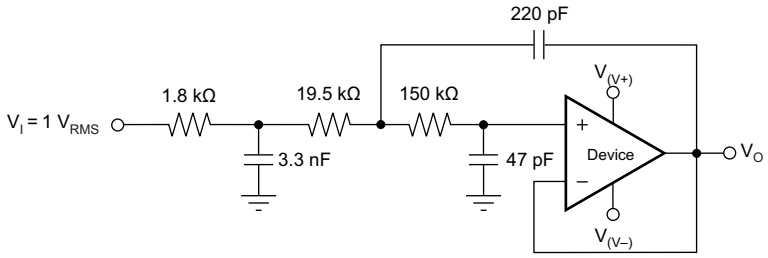


Figure 35. OPA356-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

9 Power Supply Recommendations

The OPA356-Q1 is specified for operation from 2.7 to 5.5 V (±1.35 to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, VS – VO. Minimize power dissipation by using the lowest possible power-supply voltage required to ensure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. Application bulletin AB-039, *Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads, and is available on www.ti.com.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature to trigger the thermal protection at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

10 Layout

10.1 Layout Guidelines

- Good high-frequency PC board layout techniques should be employed for the OPA356-Q1. Generous use of ground planes, short direct signal traces, and a suitable bypass capacitor located at the V+ pin assure clean, stable operation. Large areas of copper also provide a means of dissipating heat that is generated within the amplifier in normal operation.
- Sockets are definitely not recommended for use with any high-speed amplifier.
- A 10-µF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

10.2 Layout Example

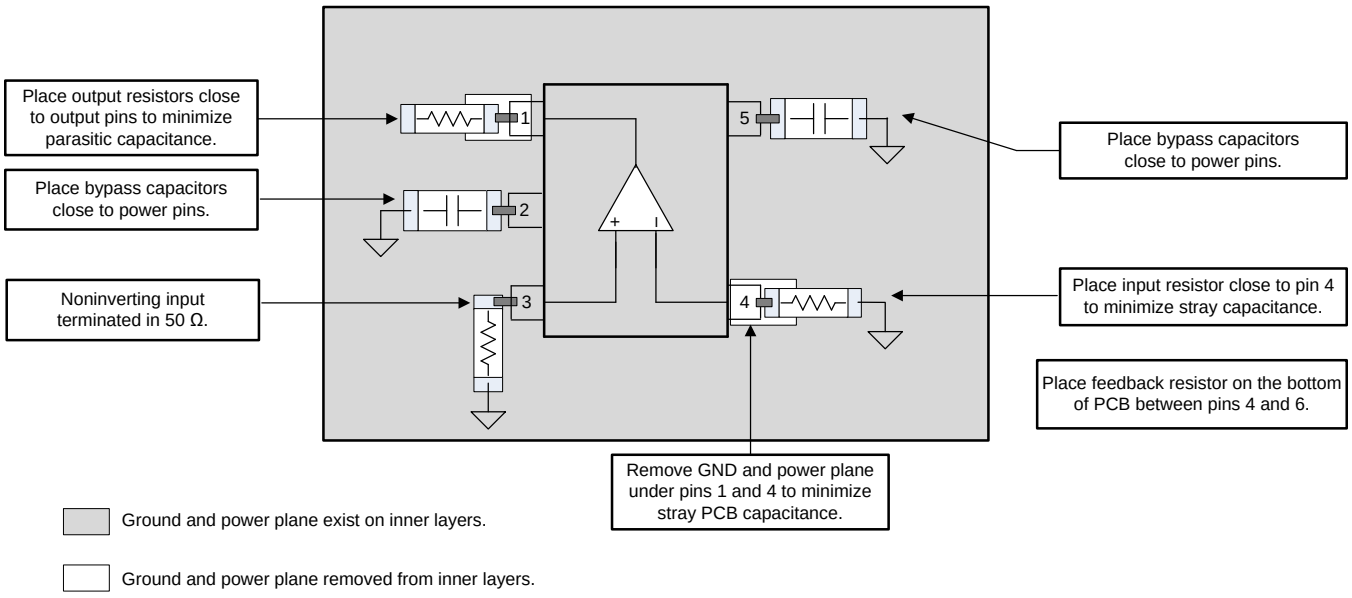


Figure 36. Example Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- *『OPAx380高精度、高速トランスインピーダンス・アンプ』*
- *『OPAx354 250MHz、レール・ツー・レールI/O、CMOSオペアンプ』*
- *『OPAx300低ノイズ、高速、16ビット高精度、CMOSオペアンプ』*
- *『OPAx355 200MHz、CMOSオペアンプ、シャットダウン付き』*
- *『OPA656広帯域、ユニティ・ゲイン安定、FET入力オペアンプ』*
- *『OPA657 1.6GHz、低ノイズ、FET入力オペアンプ』*
- *『トランスインピーダンス・アンプの直感的な補正』*
- *『FETトランスインピーダンス・アンプのノイズ解析』*
- *『高速オペアンプのノイズ解析』*
- *『ADS8326 16ビット、高速、2.7V～5.5V、マイクロパワー・サンプリングA/Dコンバータ』*
- FilterPro™

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。***

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

E2E is a trademark of Texas Instruments.
FilterPro is a trademark of Texas Instruments Incorporated.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA356AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOVQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

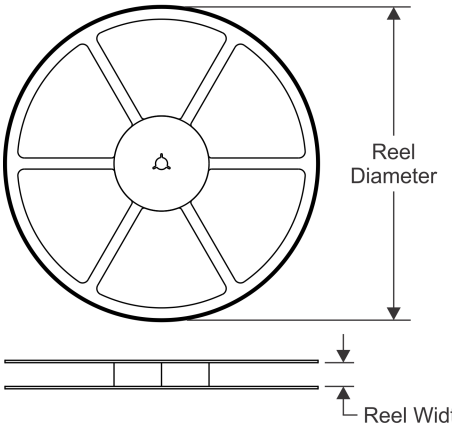
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

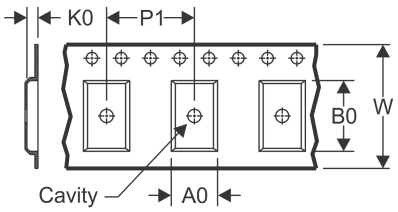
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

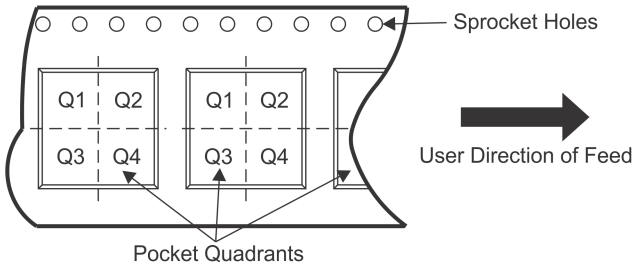


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

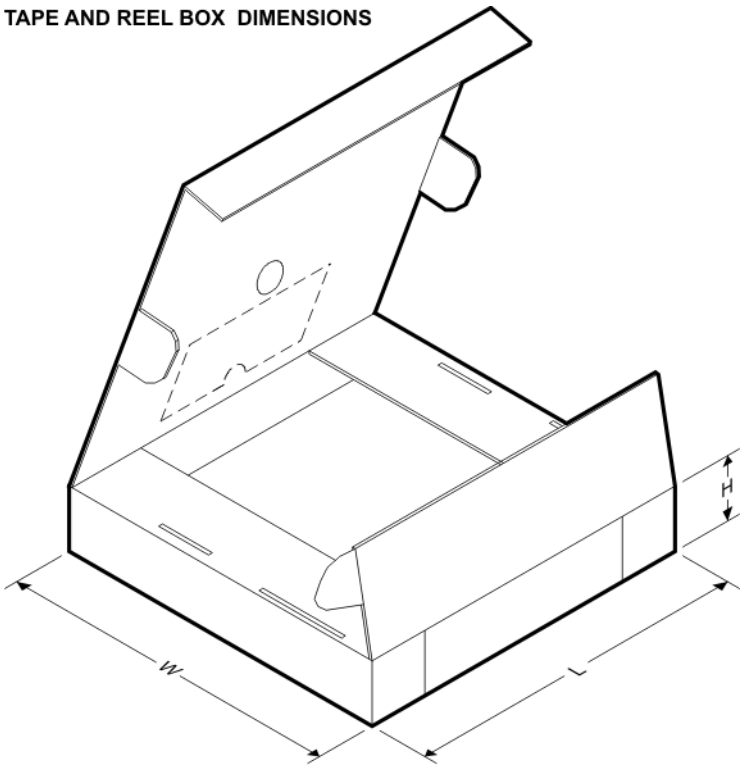
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA356AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

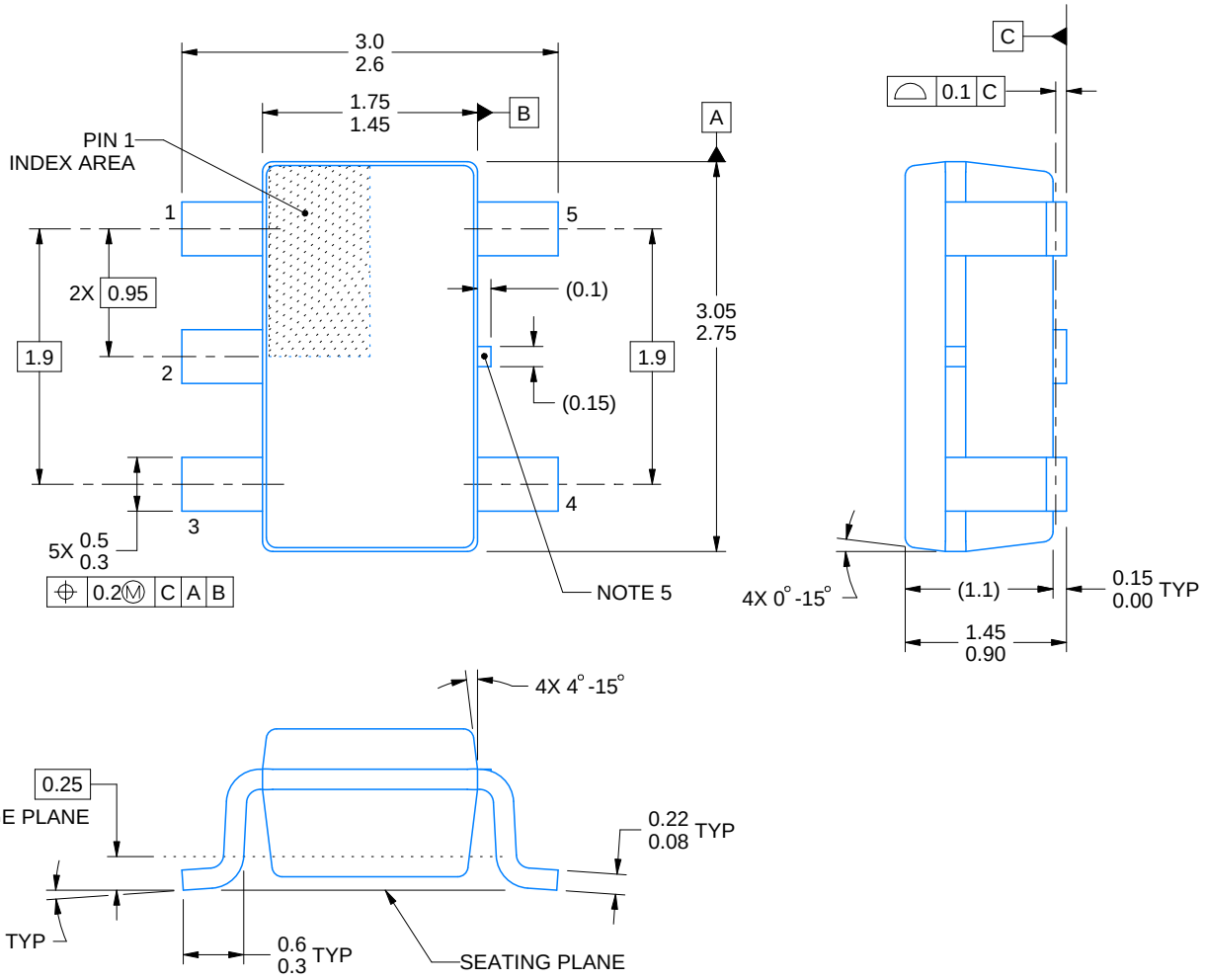
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA356AQDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

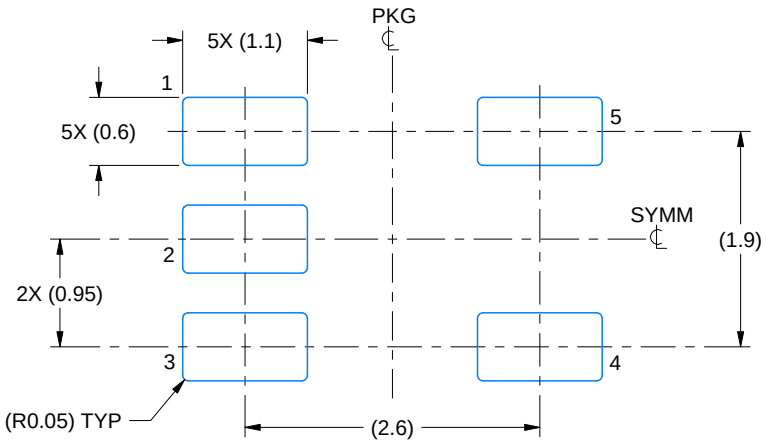
SMALL OUTLINE TRANSISTOR



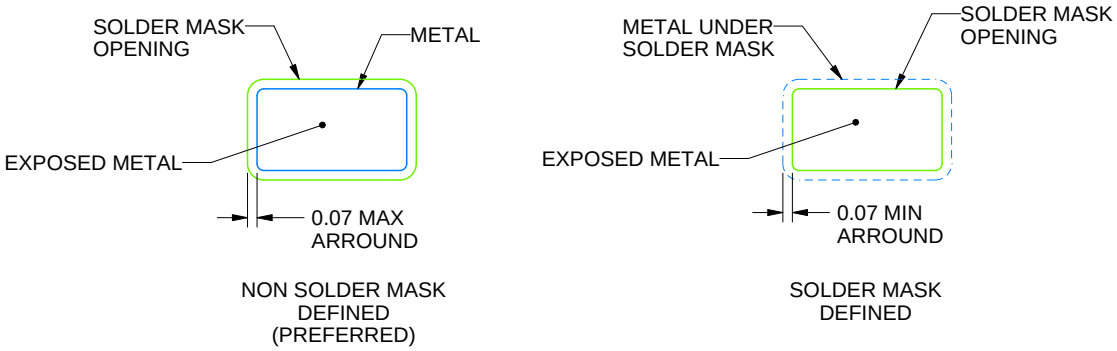
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

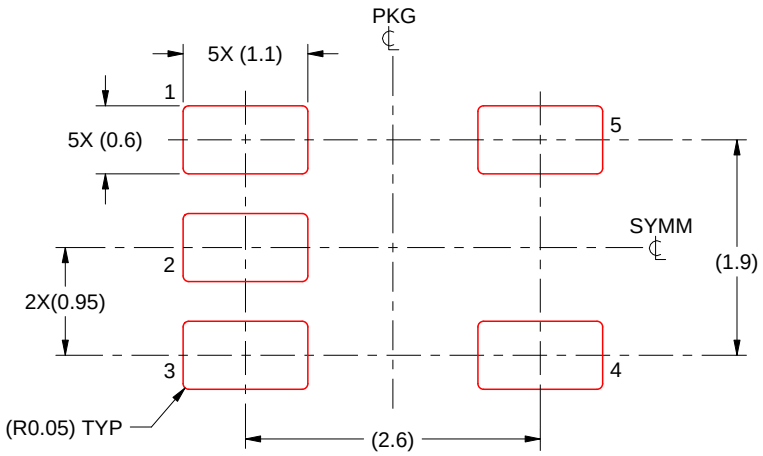


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265