MCF8315A センサレス・フィールド・オリエンテッド・コントロール (FOC)、FET BLDC ドライバ内蔵

1 特長

- センサレス・モーター制御アルゴリズムを統合した 3 相 BLDC モーター・ドライバ
  - コード・フリーのフィールド・オリエンテッド・コントロール (FOC)
  - アナログ、PWM、周波数ベースの速度入力モード：MCF8315A がスタンバイ・デバイスとして設定されている場合 (DEV_MODE = 0b) のみ使用可能
  - I²C ベースの速度入力モード：スリープ・デバイス (DEV_MODE = 1b) とスタンバイ・デバイス (DEV_MODE = 0b) の両方で使用可能。
  - モーター・パラメータ抽出ツール (MPET) を使用したオフライン・モーター・パラメータ測定
  - 設定可能な 5 点速度プロファイルをサポート
  - 順方向再同期と反転駆動による風車制御のサポート
  - アンチ電圧サージ (AVS) 保護機能により、
  - 自動デッド・タイム補償により音響性能を向上
- 動作電圧：4.5V～35V (絶対最大定格 40V)
- 高い出力電流能力：ピーク 4A
- 低い MOSFET ON 抵抗
  - T_A = 25℃での $R_{DS(ON)}$ (HS + LS)：240mΩ (標準値)
- 低消費電力スリープ・モード：『表 7-6』を参照してください
  - V_{VM} = 24V、T_A = 25℃で 5μA (最大値)
- 速度ループの精度：内部クロック使用時に 3%、外部クロックを基準とする場合は 1%
- 低インダクタンスのモーターをサポートするため、最大 75kHz の PWM 周波数に対応
- 電流センス機能を内蔵し外付け電流センス抵抗が不要
- 3.3V、20mA の LDO レギュレータを内蔵
- 3.3V / 5V、170mA の降圧レギュレータを内蔵
- 専用 DRVOFF ピンによる出力の無効化 (ハイ・インピーダンス)
- 拡散スペクトラムとスルーレート設定は EMI 低減に貢献
- 各種保護機能を内蔵
  - 電源低電圧誤動作防止 (UVLO)
  - 過電圧保護 (OVP)
  - モーター・ロック検出 (5 つの異なる種類)
  - 過電流保護 (OCP)
  - 熱警告およびシャットダウン (OTW/TSD)
  - フォルト状況表示ピン (nFAULT)
  - I²C インターフェイスによるフォルト診断 (任意)

2 アプリケーション

- ブラシレス DC (BLDC) モーター・モジュール
- 住宅用ファンとリビング・ファン
- 空気清浄機と加湿器ファン
- 洗浄機と食器洗い機ポンプ
- 車載用のファンとブロワー
- CPAP 機器

3 概要

MCF8315A は、速度制御を行う 12V～24V ブラシレス DC モーター (BLDC) または永久磁石同期モーター (PMSM) を、最大 4A のピーク電流で駆動できる、シングルチップでコード・フリーのセンサレス FOC ソリューションを提供します。MCF8315A には、絶対最大定格が 40V、$R_{DS(ON)}$ は (ハイサイドとローサイド FET の合計) で 240mΩ という低い値のハーフ・ブリッジを 3 つ内蔵しています。MCF8315A には、電圧調整可能な降圧レギュレータ (3.3V または 5V、170mA) および LDO (3.3V/20mA) を含む電源管理回路が内蔵されており、外部回路に電源を供給できます。

FOC アルゴリズムの構成は、不揮発性 EEPROM に保存されるため、構成後はデバイスをスタンドアロンで動作させることが可能です。デバイスは、PWM 入力、アナログ電圧、可変周波数の方形波、I²C コマンドによって速度コマンドを受信します。MCF8315A には、デバイス自体、モーター、およびシステムを故障イベントから保護するために、多数の保護機能が内蔵されています。

> **注**
> デバイスの電源投入後、またはスリープ状態からウェークアップしてから速度コマンドを入力する前に、200ms の遅延時間を追加することを推奨します。

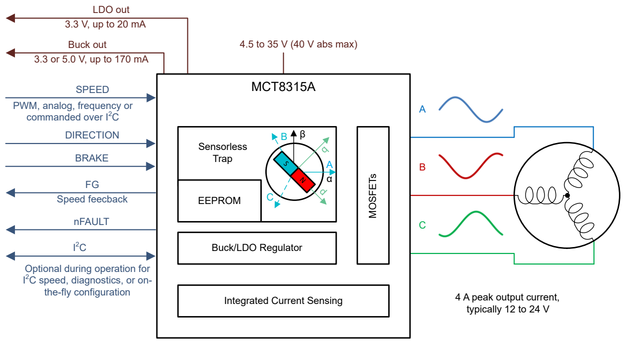
製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
MCF8315A1V	VQFN (40)	7.00mm × 5.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

参考用のドキュメント：

- 『MCF8315A チューニング・ガイド』を参照してください
- 『MCF8315A EVM GUI』を参照してください


LDO out
3.3 V, up to 20 mA
Buck out
3.3 or 5.0 V, up to 170 mA
4.5 to 35 V (40 V abs max)
MCT8315A
SPEED
PWM, analog, frequency or commanded over I2C
DIRECTION
BRAKE
FG
Speed feecback
nFAULT
I2C
Optional during operation for I2C speed, diagnostics, or on-the-fly configuration
Sensorless Trap
EEPROM
Buck/LDO Regulator
Integrated Current Sensing
MOSFETs
A
B
C
4 A peak output current, typically 12 to 24 V

概略回路図

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4 Revision History

DATE	REVISION	NOTES
December 2022	*	Initial Release

Changes from Revision * (December 2022) to Revision A (April 2023) **Page**

- Updated I^2C Data Word section to clarify default I^2C Target ID 77
- Updated CRC Byte Calculation section with CRC initial value 81

5 Pin Configuration and Functions

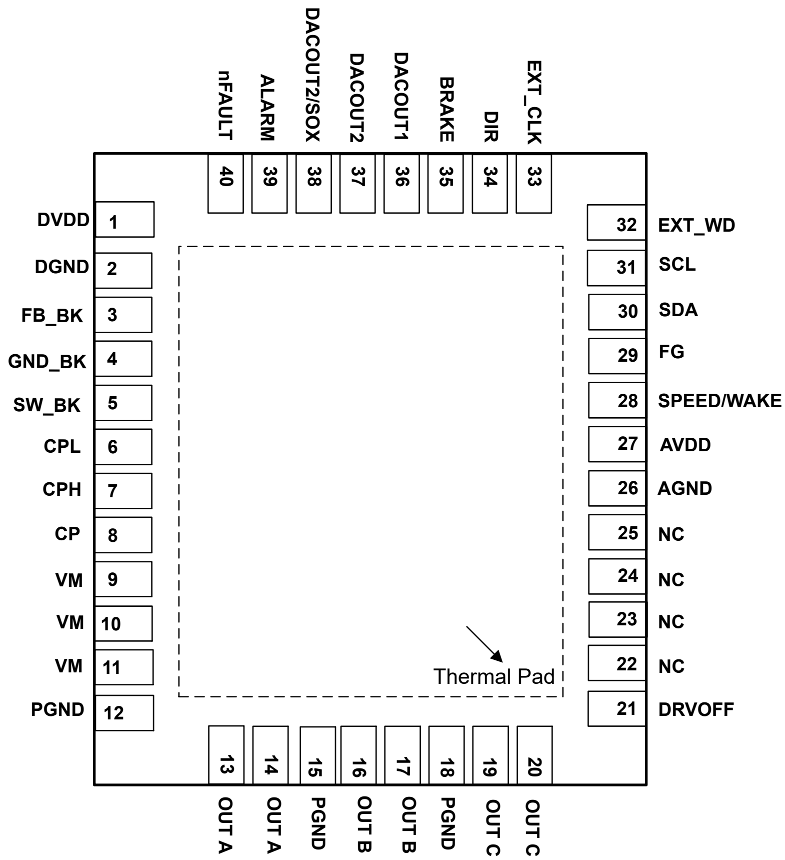

図 5-1. MCF8315A, 40-Pin VQFN With Exposed Thermal Pad, Top View

表 5-1. Pin Functions

PIN	40-pin Package	TYPE(1)	DESCRIPTION
NAME	MCF8315A		
AGND	26	GND	Device analog ground. Refer Layout Guidelines for connection recommendation.
ALARM	39	O	Alarm signal: push-pull output. Pulled logic high during fault condition, if enabled. If ALARM pin is not used, leave it floating.
AVDD	27	PWR O	3.3-V internal regulator output. Connect a X5R or X7R, 1-μF, 6.3-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 20 mA for external circuits.
BRAKE	35	I	High → Brake the motor Low → Normal motor operation If BRAKE pin is not used, connect to AGND directly. If BRAKE pin is used to brake the motor, use an external 100-kΩ pull-down resistor (to AGND).
CP	8	PWR	Charge pump output. Connect a X5R or X7R, 1-μF, 16-V ceramic capacitor between the CP and VM pins.
CPH	7	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
CPL	6	PWR	
DACOUT1	36	O	DAC output DACOUT1
DACOUT2	37	O	DAC output DACOUT2

表 5-1. Pin Functions (continued)

PIN NAME	40-pin Package MCF8315A	TYPE(1)	DESCRIPTION
DACOUT2/SOX	38	O	Multi-purpose pin: DAC output when configured as DACOUT2 CSA output when configured as SOX
DGND	2	GND	Device digital ground. Refer Layout Guidelines for connection recommendation.
DIR	34	I	Direction of motor spinning; When low, phase driving sequence is OUT A → OUT C → OUT B When high, phase driving sequence is OUT A → OUT B → OUT C If DIR pin is not used, connect to AGND or AVDD directly (depending on phase driving sequence needed). If DIR pin is used for changing motor spin direction, use an external 100-kΩ pull-down resistor (to AGND).
DRVOFF	21	I	Coast (Hi-Z) all six MOSFETs when DRVOFF is high.
DVDD	1	PWR	1.5-V internal regulator output. Connect a X5R or X7R, 2.2-μF, 6.3-V ceramic capacitor between the DVDD and DGND pins.
EXT_CLK	33	I	External clock reference input in external clock reference mode.
EXT_WD	32	I	External watchdog input.
FB_BK	3	PWR I/O	Feedback for buck regulator output control. Connect to buck regulator output after the inductor/resistor.
FG	29	O	Motor speed indicator : open-drain output; requires an external pull-up resistor to 1.8-V to 5.0-V.
GND_BK	4	GND	Buck regulator ground. Refer Layout Guidelines for connection recommendation.
NC	22, 23, 24, 25	-	No connection. Leave these pins floating.
nFAULT	40	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8 V to 5.0 V.
OUTA	13, 14	PWR O	Half-bridge output A
OUTB	16, 17	PWR O	Half-bridge output B
OUTC	19, 20	PWR O	Half-bridge output C
PGND	12, 15, 18	GND	Device power ground. Refer Layout Guidelines for connection recommendation.
SCL	31	I	I^2C clock input
SDA	30	I/O	I^2C data line
SPEED/WAKE	28	I	Device speed input; supports analog, PWM or frequency based speed input. The speed pin input can be configured through SPEED_MODE.
SW_BK	5	PWR	Buck switch node. Connect this pin to an inductor or resistor.
VM	9, 10, 11	PWR I	Device and motor power supply. Connect to motor supply voltage; bypass to PGND with one 0.1-μF capacitor plus one bulk capacitor. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
Thermal pad		GND	Must be connected to AGND.

(1) I = input, O = output, GND = ground, PWR = power, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	40	V
Voltage difference between ground pins (GND_BK, DGND, PGND, AGND)	–0.3	0.3	V
Charge pump voltage (CPH, CP)	–0.3	V_{VM} + 6	V
Charge pump negative switching pin voltage (CPL)	–0.3	V_{VM} +0.3	V
Switching node pin voltage (SW_BK)	–0.3	V_{VM} +0.3	V
Analog regulators pin voltage (AVDD)	–0.3	4	V
Analog regulators pin voltage (DVDD)	–0.3	1.7	V
Logic pin input voltage (BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SCL, SDA, SPEED)	–0.3	6	V
Open drain pin output voltage (nFAULT, FG)	–0.3	6	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_{VM} + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002[(2)]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	35	V
I_{OUT} [(1)]	Peak output winding current	OUTA, OUTB, OUTC			4	A
V_{IN_LOGIC}	Logic input voltage	BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SPEED, SDA, SCL	–0.1		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT, FG	–0.1		5.5	V
I_{OD}	Open drain output current capability	nFAULT, FG			5	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		MCF8315A RGF (VQFN) 40 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6 V, V_{SPEED} = 0, T_A = 25 °C		3	5	µA
		V_{SPEED} = 0, T_A = 125 °C		3.5	7	µA
I_{VMS}	VM standby mode current	V_{VM} ≥ 12 V, Standby Mode, DRVOFF = High, T_A = 25 °C, L_{BK} = 47 uH, C_{BK} = 22 µF		8	16	mA
		V_{VM} > 6 V, Standby Mode, DRVOFF = High, T_A = 25 °C, R_{BK} = 22 Ω, C_{BK} = 22 µF		25	29	mA
		V_{VM} ≥ 12 V, Standby Mode, DRVOFF = High, L_{BK} = 47 uH, C_{BK} = 22 µF		8	16.5	mA
		V_{VM} > 6 V, Standby Mode, DRVOFF = High, R_{BK} = 22 Ω, C_{BK} = 22 µF		25	29	mA
I_{VM}	VM operating mode current	V_{VM} > 6 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), T_A = 25 °C, L_{BK} = 47 uH, C_{BK} = 22 µF, No Motor Connected		11	18	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), T_A = 25 °C, R_{BK} = 22 Ω, C_{BK} = 22 µF, No Motor Connected		27	30.5	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), L_{BK} = 47 uH, C_{BK} = 22 µF, No Motor Connected		11	17	mA
		V_{VM} > 6 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), R_{BK} = 22 Ω, C_{BK} = 22 µF, No Motor Connected		28	30.5	mA
V_{AVDD}	Analog regulator voltage	0 mA ≤ I_{AVDD} ≤ 20 mA	3.125	3.3	3.465	V
I_{AVDD}	External analog regulator load				20	mA
V_{DVDD}	Digital regulator voltage		1.4	1.55	1.65	V
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM	4.0	4.7	5.5	V

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK REGULATOR						
V_{BK}	Buck regulator average voltage (L_{BK} = 47 μH, C_{BK} = 22 μF)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 170 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 170 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 170 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 170 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b, 11b), 0 mA ≤ I_{BK} ≤ 170 mA		V_{VM}– I_{BK}*(R_{LBK} +2) [1]		V
V_{BK}	Buck regulator average voltage (L_{BK} = 22 μH, C_{BK} = 22 μF)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 20 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 20 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 20 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 20 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b, 11b), 0 mA ≤ I_{BK} ≤ 20 mA		V_{VM}– I_{BK}*(R_{LBK} +2)[1]		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 μF)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 10 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 10 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 10 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 10 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b, 11b), 0 mA ≤ I_{BK} ≤ 10 mA		V_{VM}– I_{BK}*(R_{BK} +2)		V
V_{BK_RIP}	Buck regulator ripple voltage	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 170 mA, Buck regulator with inductor, L_{BK} = 47 uH, C_{BK} = 22 μF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 20 mA, Buck regulator with inductor, L_{BK} = 22 uH, C_{BK} = 22 μF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 10 mA, Buck regulator with resistor; R_{BK} = 22 Ω, C_{BK} = 22 μF	–100		100	mV

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BK}	External buck regulator load	L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			170	mA
		L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			170 – I_{AVDD}	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			20	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			20 – I_{AVDD}	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			10	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			10 – I_{AVDD}	mA
f_{SW_BK}	Buck regulator switching frequency	Regulation Mode	20		535	kHz
		Linear Mode	20		535	kHz
V_{BK_UV}	Buck regulator undervoltage lockout	V_{BK} rising, BUCK_SEL = 00b	2.7	2.8	2.95	V
		V_{BK} falling, BUCK_SEL = 00b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 01b	4.3	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 01b	4.1	4.2	4.36	V
		V_{BK} rising, BUCK_SEL = 10b	2.7	2.8	2.95	V
		V_{BK} falling, BUCK_SEL = 10b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 11b	4.3	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 11b	4.1	4.2	4.36	V
$V_{BK\_UV\_HYS}$	Buck regulator undervoltage lockout hysteresis	Rising to falling threshold, BUCK_SEL = 00b	90	200	400	mV
		Rising to falling threshold, BUCK_SEL = 01b	90	200	400	mV
		Rising to falling threshold, BUCK_SEL = 10b	90	200	400	mV
		Rising to falling threshold, BUCK_SEL =11b	90	200	400	mV
I_{BK_CL}	Buck regulator current limit threshold	BUCK_CL = 0b	360	600	910	mA
		BUCK_CL = 1b	80	150	250	mA
I_{BK_OCP}	Buck regulator over current protection trip point		2	3	4	A
t_{BK_RETRY}	Over current protection retry time		0.7	1	1.3	ms
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		240	260	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		250	270	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		360	400	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		370	415	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, SLEW_RATE = 00b	13	25	45	V/µs
		V_{VM} = 24 V, SLEW_RATE = 01b	30	50	80	V/µs
		V_{VM} = 24 V, SLEW_RATE = 10b	80	125	185	V/µs
		V_{VM} = 24 V, SLEW_RATE = 11b	130	200	280	V/µs
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	V_{VM} = 24 V, SLEW_RATE = 00b	14	25	45	V/µs
		V_{VM} = 24 V, SLEW_RATE = 01b	30	50	80	V/µs
		V_{VM} = 24 V, SLEW_RATE = 10b	80	125	185	V/µs
		V_{VM} = 24 V, SLEW_RATE = 11b	110	200	280	V/µs

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24 V, SR = 25 V/µs		1800	3000	ns
		V_{VM} = 24 V, SR = 50 V/µs		1100	1400	ns
		V_{VM} = 24 V, SR = 125 V/µs		650	850	ns
		V_{VM} = 24 V, SR = 200 V/µs		500	550	ns
SPEED INPUT - PWM MODE						
f_{PWM}	PWM input frequency		0.01		100	kHz
Res_{PWM}	PWM input resolution	f_{PWM} = 0.01 to 0.35 kHz	11	12	13	bits
		f_{PWM} = 0.35 to 2 kHz	11	13	14	bits
		f_{PWM} = 2 to 3.5 kHz	11	11.5	12	bits
		f_{PWM} = 3.5 to 7 kHz	12	13	13.5	bits
		f_{PWM} = 7 to 14 kHz	11	12	12.5	bits
		f_{PWM} = 14 to 29.2 kHz	10	11.5	12	bits
		f_{PWM} = 29.3 to 60 kHz	9	10.5	11	bits
		f_{PWM} = 60 to 100 kHz	8	9	10	bits
SPEED INPUT - ANALOG MODE						
V_{ANA_FS}	Analog full-speed voltage		2.95	3	3.05	V
V_{ANA_RES}	Analog voltage resolution			732		µV
SPEED INPUT - FREQUENCY MODE						
f_{PWM_FREQ}	PWM input frequency range	Duty cycle = 50%	3		32767	Hz
SLEEP MODE						
t_{DET_PWM}	Time needed to detect wake up signal on SPEED pin	SPEED_MODE = 11b (I^2C mode), V_{SPEED} > V_{IH}	0.5	1	1.5	µs
STANDBY MODE						
$t_{EX\_SB\_DR\_ANA}$	Time taken to drive motor after exiting standby mode, analog mode	SPEED_MODE = 00b (analog mode), V_{SPEED} > V_{EX_SB}, ISD detection disabled			6	ms
$t_{EX\_SB\_DR\_PWM}$	Time taken to drive motor after exiting standby mode, PWM mode	SPEED_MODE = 01b (PWM mode) V_{SPEED} > V_{IH}, ISD detection disabled			6	ms
$t_{DET\_SB\_ANA}$	Time needed to detect standby mode, analog mode	SPEED_MODE = 00b (analog mode), V_{SPEED} < V_{EN_SB}	0.5	1	2	ms
$t_{DET\_SB\_PWM}$	Time needed to detect standby command, PWM/Freq mode	SPEED_MODE = 01b (PWM mode) or SPEED_MODE = 11b (Freq mode), V_{SPEED} < V_{IL}, SLEEP_ENTRY_TIME = 00b	0.035	0.05	0.065	ms
		SPEED_MODE = 01b (PWM mode) or SPEED_MODE = 11b (Freq mode), V_{SPEED} < V_{IL}, SLEEP_ENTRY_TIME = 01b	0.14	0.2	0.26	ms
		SPEED_MODE = 01b (PWM mode) or SPEED_MODE = 11b (Freq mode), V_{SPEED} < V_{IL}, SLEEP_ENTRY_TIME = 10b	14	20	26	ms
		SPEED_MODE = 01b (PWM mode) or SPEED_MODE = 11b (Freq mode), V_{SPEED} < V_{IL}, SLEEP_ENTRY_TIME = 11b	140	200	260	ms
$t_{DET\_SB\_DIG}$	Time needed to detect standby mode, I^2C mode	SPEED_MODE = 10b (I^2C mode), DIGITAL_SPEED_CTRL = 0b		1	2	ms
t_{EN_SB}	Time needed to stop driving motor after detecting standby command	All speed input modes		1	2	ms
LOGIC-LEVEL INPUTS (BRAKE, DIR, EXT_CLK, EXT_WD, SPEED)						

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input logic low voltage	AVDD = 3 to 3.6 V			0.25*AVDD	V
V_{IH}	Input logic high voltage	AVDD = 3 to 3.6 V	0.65*AVDD			V
V_{HYS}	Input hysteresis		50	500	800	mV
I_{IL}	Input logic low current	AVDD = 3 to 3.6 V	-0.15		0.15	µA
I_{IH}	Input logic high current	AVDD = 3 to 3.6 V	-0.3		0	µA
R_{PD_SPEED}	Input pulldown resistance	SPEED pin To GND	0.6	1	1.4	MΩ
OPEN-DRAIN OUTPUTS (nFAULT, FG)						
V_{OL}	Output logic low voltage	I_{OD} = -5 mA			0.4	V
I_{OZ}	Output logic high current	V_{OD} = 3.3 V	0		0.5	µA
I^{2}C Serial Interface						
V_{I2C_L}	Input logic low voltage		-0.5		0.3*AVDD	V
V_{I2C_H}	Input logic high voltage		0.7*AVDD		5.5	V
V_{I2C_HYS}	Hysteresis		0.05*AVDD			V
V_{I2C_OL}	Output logic low voltage	Open-drain at 2mA sink current	0		0.4	V
I_{I2C_OL}	Output logic low current	V_{I2C_OL} = 0.6V			6	mA
I_{I2C_IL}	Input current on SDA and SCL		-10[2]		10[2]	µA
C_i	Capacitance for SDA and SCL				10	pF
t_{of}	Output fall time from V_{I2C_H}(min) to V_{I2C_L}(max)	Standard Mode			250[3]	ns
		Fast Mode			250[3]	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Fast Mode	0		50[4]	ns
OSCILLATOR						
f_{OSCREF}	External clock reference	EXT_CLK_CONFIG = 000b		8		kHz
		EXT_CLK_CONFIG = 001b		16		kHz
		EXT_CLK_CONFIG = 010b		32		kHz
		EXT_CLK_CONFIG = 011b		64		kHz
		EXT_CLK_CONFIG = 100b		128		kHz
		EXT_CLK_CONFIG = 101b		256		kHz
		EXT_CLK_CONFIG = 110b		512		kHz
		EXT_CLK_CONFIG = 111b		1024		kHz
EEPROM						
EE_{Prog}	Programming voltage		1.35	1.5	1.65	V
EE_{RET}	Retention	T_A = 25 ℃		100		Years
		T_J = -40 to 150 ℃	10			Years
EE_{END}	Endurance	T_J = -40 to 150 ℃	1000			Cycles
		T_J = -40 to 85 ℃	20000			Cycles
PROTECTION CIRCUITS						
V_{UVLO}	Supply under voltage lockout (UVLO)	VM rising	4.3	4.4	4.51	V
		VM falling	4.1	4.2	4.3	V
V_{UVLO_HYS}	Supply under voltage lockout hysteresis	Rising to falling threshold	110	200	350	mV
t_{UVLO}	Supply under voltage deglitch time		3	5	7	µs

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	Supply over voltage protection (OVP) threshold	Supply rising, OVP_EN = 1, OVP_SEL = 0	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	31.8	33	34.3	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	19	21	22	V
V_{OVP_HYS}	Supply over voltage protection hysteresis	Rising to falling threshold, OVP_SEL = 1	0.9	1	1.1	V
		Rising to falling threshold, OVP_SEL = 0	0.7	0.8	0.9	V
t_{OVP}	Supply over voltage deglitch time		2.5	5	7	µs
V_{CPUV}	Charge pump under voltage lockout (above VM)	Supply rising	2.25	2.5	2.75	V
		Supply falling	2.2	2.4	2.6	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	65	100	150	mV
V_{AVDD_UV}	Analog regulator (AVDD) under voltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.5	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator under voltage lockout hysteresis	Rising to falling threshold	180	200	240	mV
I_{OCP}	Over current protection trip point	OCP_LVL = 0b	5.5	9	12	A
		OCP_LVL = 1b	9	13	18	A
t_{OCP}	Over current protection deglitch time	OCP_DEG = 00b	0.02	0.2	0.4	µs
		OCP_DEG = 01b	0.2	0.6	1.2	µs
		OCP_DEG = 10b	0.5	1.2	1.8	µs
		OCP_DEG = 11b	0.9	1.6	2.5	µs
t_{RETRY}	Over current protection retry time	OCP_RETRY = 0	4	5	6	ms
		OCP_RETRY = 1	425	500	575	ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	135	145	155	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	20	25	30	°C
T_{TSD_BUCK}	Thermal shutdown temperature (Buck)	Die temperature (T_J)	170	180	190	°C
$T_{TSD\_BUCK\_HYS}$	Thermal shutdown hysteresis (Buck)	Die temperature (T_J)	20	25	30	°C
T_{TSD}	Thermal shutdown temperature (FET)	Die temperature (T_J)	165	175	185	°C
T_{TSD_HYS}	Thermal shutdown hysteresis (FET)	Die temperature (T_J)	20	25	30	°C

(1) R_{LBK} is resistance of inductor L_{BK}.
(2) If AVDD is switched off, I/O pins must not obstruct the SDA and SCL lines.
(3) The maximum tf for the SDA and SCL bus lines (300 ns) is longer than the specified maximum tof for the output stages (250 ns). This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
(4) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

6.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Standard-mode						
f_{SCL}	SCL clock frequency		0		100	kHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4			µs
t_{LOW}	LOW period of the SCL clock		4.7			µs
t_{HIGH}	HIGH period of the SCL clock		4			µs

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{SU_STA}	Set-up time for a repeated START condition		4.7			µs
t_{HD_DAT}	Data hold time (2)	I2C bus devices	0 (3)		(4)	µs
t_{SU_DAT}	Data set-up time		250			ns
t_r	Rise time for both SDA and SCL signals				1000	ns
t_f	Fall time of both SDA and SCL signals (3) (6) (7) (8)				300	ns
t_{SU_STO}	Set-up time for STOP condition		4			µs
t_{BUF}	Bus free time between STOP and START condition		4.7			µs
C_b	Capacitive load for each bus line (9)				400	pF
t_{VD_DAT}	Data valid time (10)				3.45 (4)	µs
t_{VD_ACK}	Data valid acknowledge time (11)				3.45 (4)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V
Fast-mode						
f_{SCL}	SCL clock frequency		0		400	KHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU_STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD_DAT}	Data hold time (2)		0 (3)		(4)	µs
t_{SU_DAT}	Data set-up time		100 (5)			ns
t_r	Rise time for both SDA and SCL signals		20		300	ns
t_f	Fall time of both SDA and SCL signals (3) (6) (7) (8)		20 x (AVDD/ 5.5V)		300	ns
t_{SU_STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between STOP and START condition		1.3			µs
C_b	Capacitive load for each bus line (9)				400	pF
t_{VD_DAT}	Data valid time (10)				0.9 (4)	µs
t_{VD_ACK}	Data valid acknowledge time (11)				0.9 (4)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V

(1) All values referred to $V_{IH(min)}$ ($0.3V_{DD}$) and $V_{IL(max)}$ levels
(2) t_{HD_DAT} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum t_{HD_DAT} could be 3.45 µs and .9 µs for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_DAT} or t_{VD_ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
(5) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement t_{SU_DAT} 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU\_DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

(6) If mixed with HS-mode devices, faster fall times according to Table 10 are allowed.
(7) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(8) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
(9) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
(10) t_{VD_DAT} = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
(11) t_{VD_ACK} = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, dependging on which one is worse).

6.7 Typical Characteristics

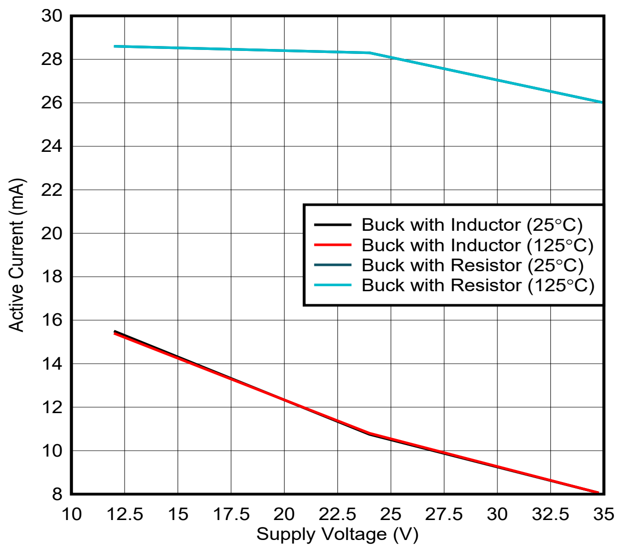

図 6-1. Supply current over supply voltage

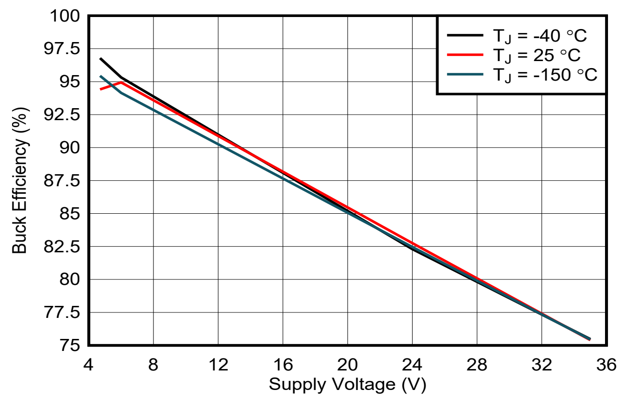

図 6-2. Buck regulator efficiency over supply voltage

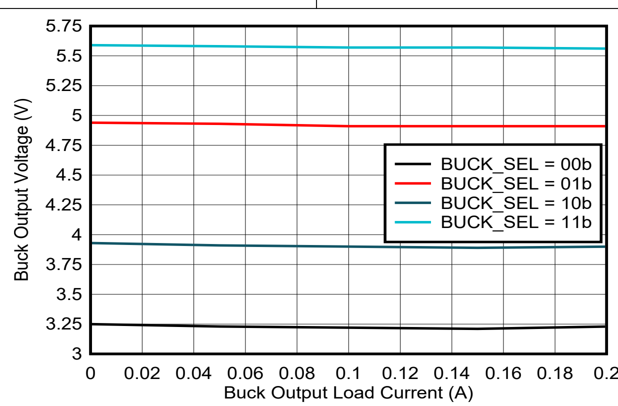

図 6-3. Buck regulator output voltage over load current

7 Detailed Description

7.1 Overview

The MCF8315A provides a single-chip, code-free sensorless FOC solution for customers driving speed-controlled 12- to 24-V brushless-DC motors requiring up to 4-A peak phase currents.

The MCF8315A integrates three ½-bridges with 40-V absolute maximum capability and a low $R_{DS(ON)}$ of 240-mΩ (high-side + low-side) to enable high power drive capability. Current is sensed using an integrated current sensing circuit which eliminates the need for external sense resistors. Power management features of an adjustable buck regulator and LDO generate the necessary voltage rails for the device and can also be used to power external circuits.

MCF8315A implements Sensorless FOC, and so an external microcontroller is not required to spin the brushless-DC motor. The algorithm is implemented in a fixed-function state machine, so no coding is needed. The algorithm is highly configurable through register settings ranging from motor start-up behavior to closed loop operation. Register settings can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. The device receives a speed command through a PWM input, analog voltage, frequency input or I^2C command.

In-built protection features include power-supply under voltage lockout (UVLO), charge-pump under voltage lockout (CPUV), over current protection (OCP), AVDD under voltage lockout (AVDD_UV), buck regulator UVLO, motor lock detection and over temperature warning and shutdown (OTW and TSD). Fault events are indicated by the nFAULT pin with detailed fault information available in the registers.

The MCF8315A device is available in a 0.5-mm pin pitch, VQFN surface-mount package. The VQFN package size is 7 mm × 5 mm with a height of 1 mm.

7.2 Functional Block Diagram

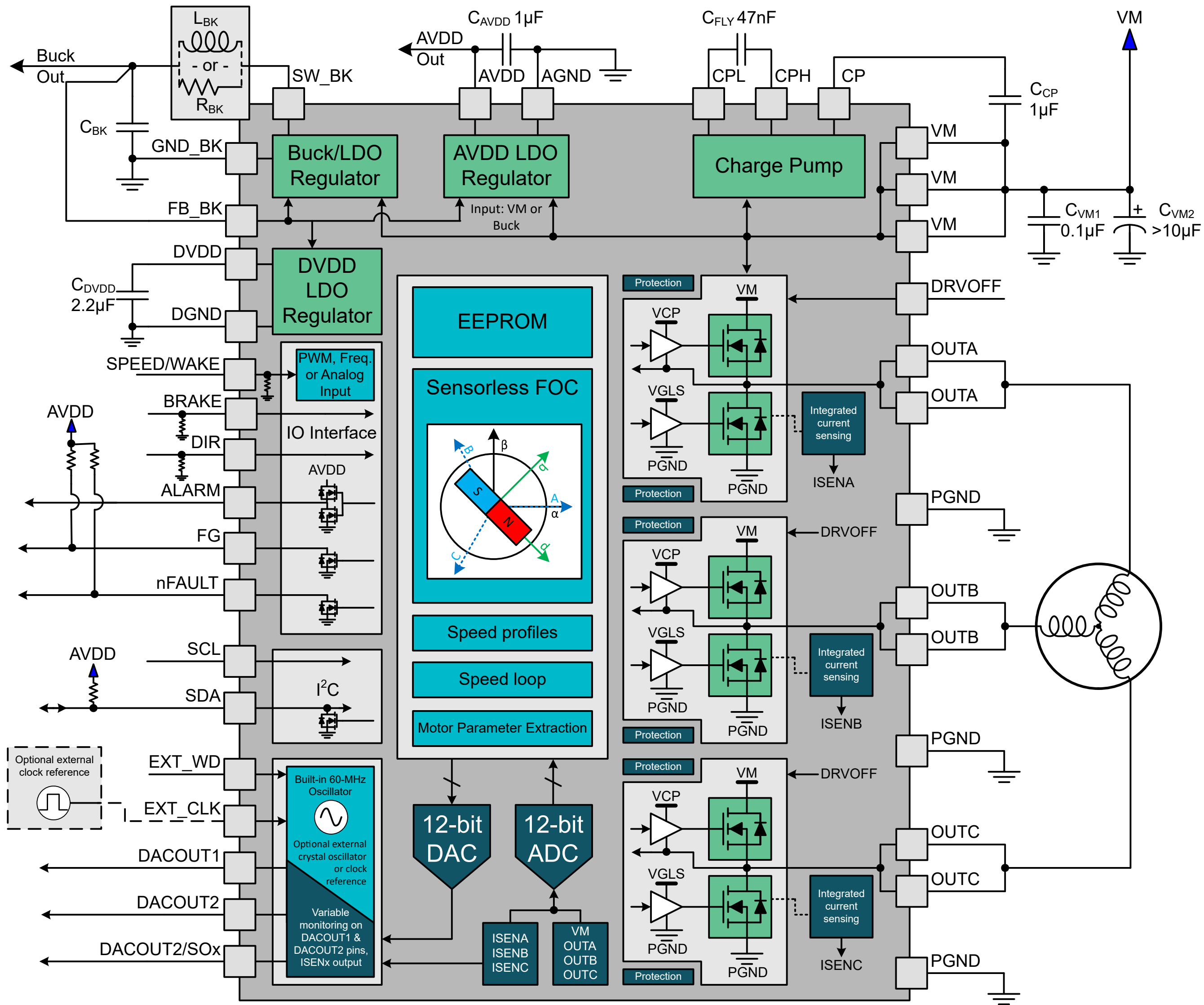

図 7-1. MCF8315A Functional Block Diagram

7.3 Feature Description

7.3.1 Output Stage

The MCF8315A consists of integrated 240-mΩ (combined high-side and low-side FETs' on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

7.3.2 Device Interface

The MCF8315A supports I^2C interface to provide end application design with adequate flexibility. MCF8315A allows controlling the motor operation and system through BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD and SPEED/WAKE pins. MCF8315A also provides different signals for monitoring system variables, speed, fault and phase current feedback through FG, nFAULT and SOX pins.

7.3.2.1 Interface - Control and Monitoring

Motor Control Signals

- When BRAKE pin is driven 'High', MCF8315A enters brake state. Brake state can be configured to either low side braking (see Low-Side Braking) or align brake (see Align Braking) through BRAKE_PIN_MODE. MCF8315A decreases output speed to value defined by BRAKE_SPEED_THRESHOLD before entering brake state. As long as BRAKE is driven 'High', MCF8315A stays in brake state. Brake pin input can be overwritten by configuring BRAKE_INPUT over the I^2C interface.
- The DIR pin decides the direction of motor spin; when driven 'High', the sequence is OUT A → OUT B → OUT C, and when driven 'Low', the sequence is OUT A → OUT C → OUT B. DIR pin input can be overwritten by configuring DIR_INPUT over the I^2C interface.
- When DRVOFF pin is driven 'High', MCF8315A stops driving the motor by turning OFF all MOSFETs (coast state). When DRVOFF is driven 'Low', MCF8315A returns to normal state of operation, as if it was restarting the motor (see DRVOFF Functionality). DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active. Entry and exit from sleep or standby condition is controlled by SPEED pin.
- SPEED/WAKE pin is used to control motor speed and to wake up MCF8315A from sleep mode. SPEED pin can be configured to accept PWM, frequency or analog input signals. It is used to enter and exit from sleep and standby mode (see 表 7-6).

External Oscillator and Watchdog Signals

- EXT_CLK pin can be used to provide an external clock reference (see External Clock Source).
- EXT_WD pin can be used to provide an external watchdog signal (see External Watchdog).

Output Signals

- DACOUT1 outputs internal variable defined by address in register DACOUT1_VAR_ADDR. DACOUT1 is refreshed every PWM cycle (see DAC outputs).
- DACOUT2 outputs internal variable defined by address in register DACOUT2_VAR_ADDR. DACOUT2 is refreshed every PWM cycle (see DAC outputs).
- FG pin provides pulses which are proportional to motor speed (see FG Configuration).
- nFAULT (active low) pin provides fault status in device or motor operation.
- ALARM pin, if enabled using ALARM_PIN_EN, provides fault status in device or motor operation. When ALARM pin is enabled, report only faults are reported only on ALARM pin (as logic high) and not reported on nFAULT pin (as logic low). When ALARM pin is enabled, actionable faults are reported on ALARM pin (as logic high) as well as on nFAULT pin (as logic low). When ALARM pin is disabled, it is in Hi-Z state and all faults (actionable and report only) are reported on nFAULT as logic low. ALARM pin should be left floating when unused/disabled.
- SOX pin provides the output of one of the current sense amplifiers.

7.3.2.2 I^2C Interface

The MCF8315A supports an I^2C serial communication interface that allows an external controller to send and receive data. This I^2C interface lets the external controller to configure the EEPROM and read detailed fault and motor state information. The I^2C bus is a two-wire interface using the SCL and SDA pins which are described as follows :

- The SCL pin is the clock signal input.
- The SDA pin is the data input and output.

7.3.3 Step-Down Mixed-Mode Buck Regulator

The MCF8315A has an integrated mixed-mode buck regulator to supply regulated 3.3-V or 5-V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4-V or 5.7-V for supporting the extra headroom for an external LDO for generating a 3.3-V or 5-V supplies. The output voltage of the buck is set by BUCK_SEL.

The buck regulator has a low quiescent current of ~1-2 mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

表 7-1. Recommended settings for Buck Regulator

Buck Mode	Buck output voltage	Max output current from AVDD (I_{AVDD_MAX})	Max output current from Buck (I_{BK_MAX})	Buck current limit	AVDD power sequencing
Inductor - 47 µH	3.3-V or 4-V	20 mA	170 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Not supported (BUCK_PS_DIS = 1b)
Inductor - 47 µH	5-V or 5.7-V	20 mA	170 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Supported (BUCK_PS_DIS = 0b)
Inductor - 22 µH	5-V or 5.7-V	20 mA	20 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1b)
Inductor - 22 µH	3.3-V or 4-V	20 mA	20 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0b)
Resistor - 22 Ω	5-V or 5.7-V	20 mA	10 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1b)
Resistor - 22 Ω	3.3-V or 4-V	20 mA	10 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0b)

7.3.3.1 Buck in Inductor Mode

The buck regulator in MCF8315A is primarily designed to support low inductance of 47-µH and 22-µH. A 47-µH inductor allows the buck regulator to operate up to 170-mA load current support, whereas applications requiring current up to 20-mA can use a 22-µH inductor which saves component size.

図 7-2 shows the connection of buck regulator in inductor mode.

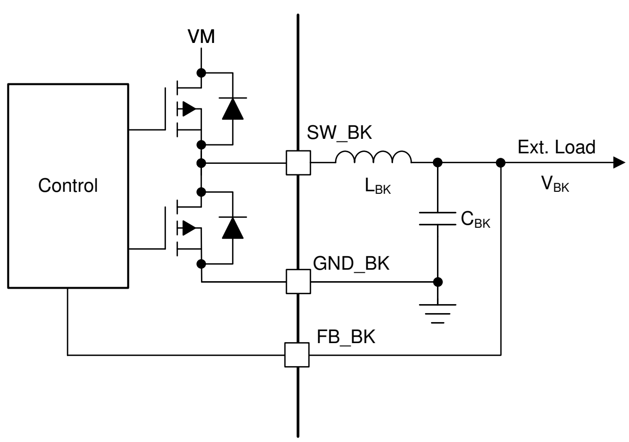

図 7-2. Buck (Inductor Mode)

7.3.3.2 Buck in Resistor mode

If the external load requirement is less than 10-mA, the inductor can be replaced with a resistor. In resistor mode the power is dissipated across the external resistor and the efficiency is lower than buck in inductor mode.

図 7-3 shows the connection of buck in resistor mode.

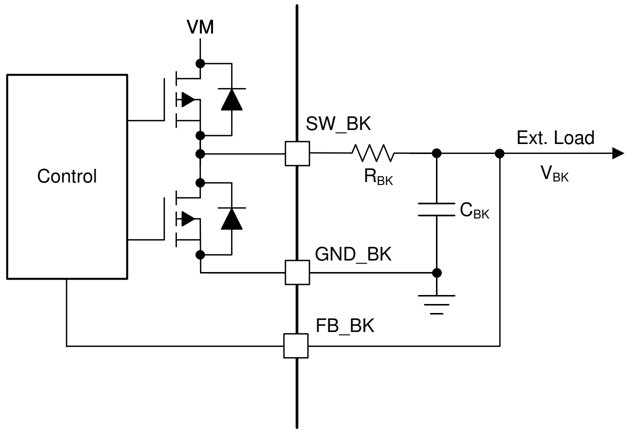

図 7-3. Buck (Resistor Mode)

7.3.3.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to supply an external LDO to generate standard 3.3-V or 5-V output rail with higher accuracies. The buck output voltage should be configured to 4-V or 5.7-V to provide extra headroom to support the external LDO for generating 3.3-V or 5-V rail as shown in 図 7-4. This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

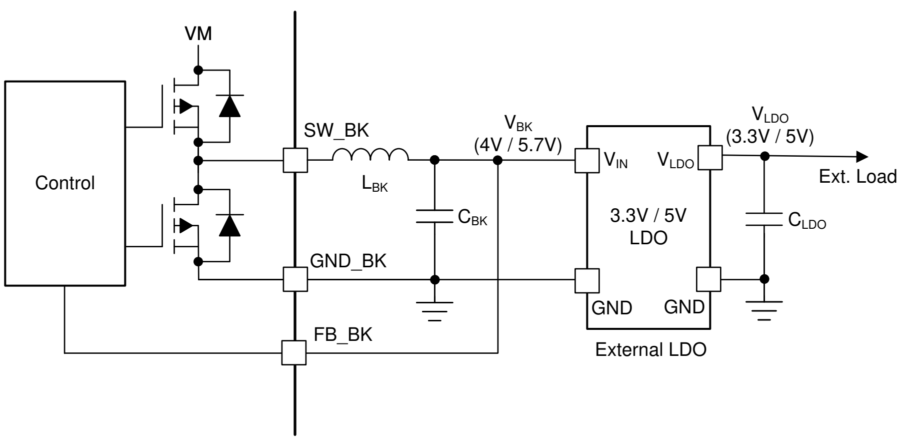

図 7-4. Buck Regulator with External LDO

7.3.3.4 AVDD Power Sequencing from Buck Regulator

The AVDD LDO has an option of using the power supply from mixed mode buck regulator to reduce the device power dissipation. The power sequencing mode allows on-the-fly changeover of AVDD LDO input from DC mains (VM) to buck output (V_{BK}) as shown in 図 7-5. This sequencing can be configured through the BUCK_PS_DIS bit . Power sequencing is supported only when buck output voltage is set to 5-V or 5.7-V.

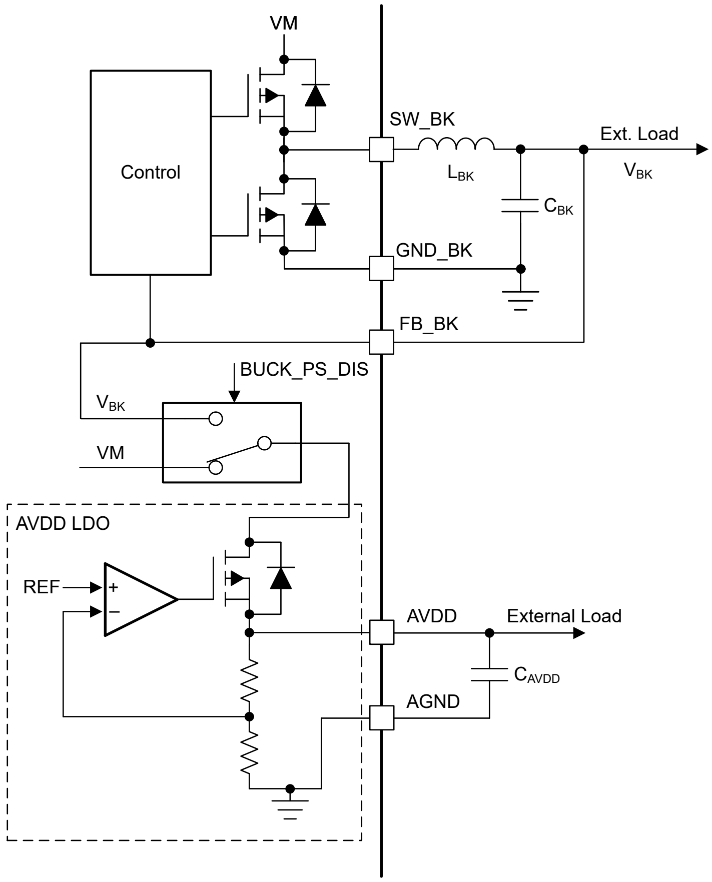

図 7-5. AVDD Power Sequencing from Mixed Mode Buck Regulator

7.3.3.5 Mixed Mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage (V_{BK_REF}) which is internally generated depending on the buck output voltage setting (BUCK_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ($V_{BK} < V_{BK\_REF}$) or low ($V_{BK} > V_{BK\_REF}$), the high-side power FET of the buck turns on and off respectively. An independent current control loop monitors the current in high-side power FET (I_{BK}) and turns off the high-side FET when the current becomes higher than the buck current limit (I_{BK_CL} set by BUCK_CL) - this implements a current limit control for the buck regulator. 図 7-6 shows the architecture of the buck and various control/protection loops.

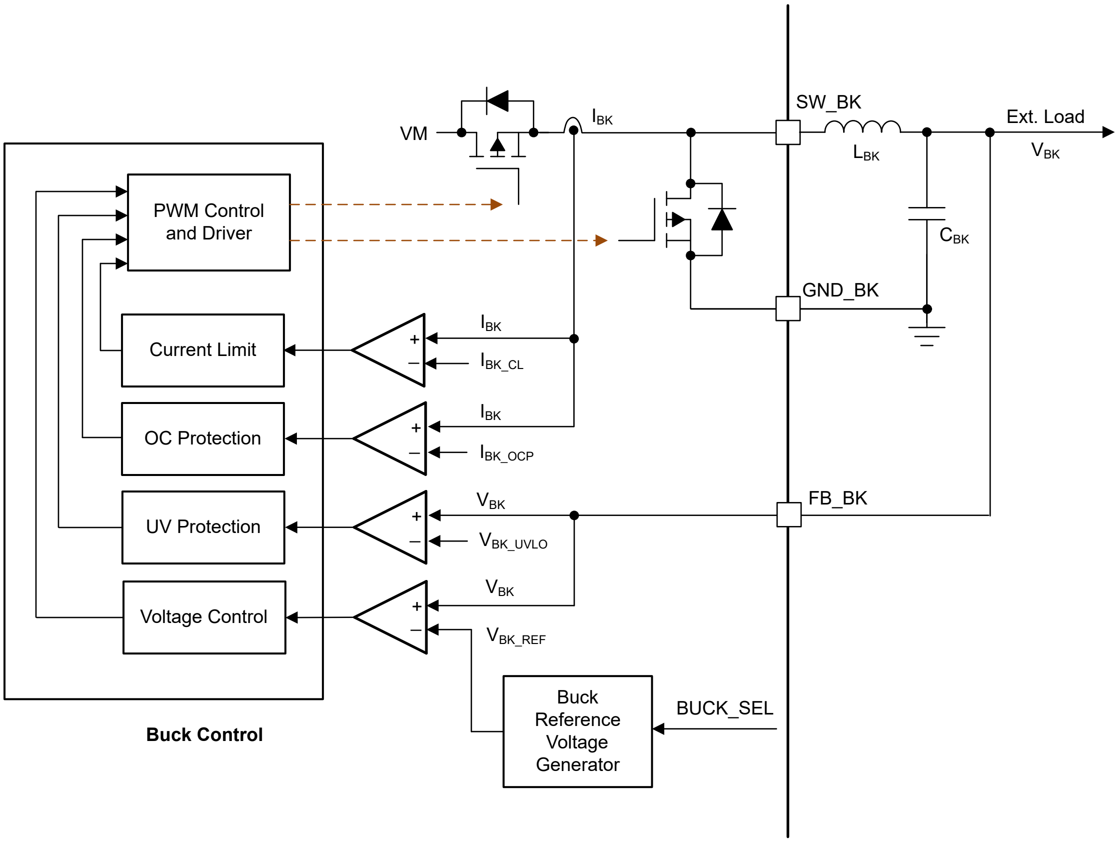

図 7-6. Buck Operation and Control Loops

7.3.3.6 Buck Under Voltage Protection

If at any time the voltage on the FB_BK pin (buck regulator output) falls lower than the V_{BK_UV} threshold, both the high-side and low-side MOSFETs of the buck regulator are disabled. MCF8315A goes into reset state whenever buck UV event occurs, since the internal circuitry in MCF8315A is powered from the buck regulator output.

7.3.3.7 Buck Over Current Protection

The buck over current event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current through the high-side MOSFET exceeds the I_{BK_OCP} threshold for a time longer than the deglitch time (t_{OCP_DEG}), a buck OCP event is recognized and both the high-side and low-side MOSFETs of the buck regulator are disabled. MCF8315A goes into reset state whenever buck OCP event occurs, since the internal circuitry in MCF8315A is powered from the buck regulator output.

7.3.4 AVDD Linear Voltage Regulator

A 3.3-V linear regulator is integrated into MCF8315A and is available for use by external circuitry. This AVDD LDO regulator is used for powering up the internal circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other external circuitry supporting up to 20-mA. The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1-μF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3-V.

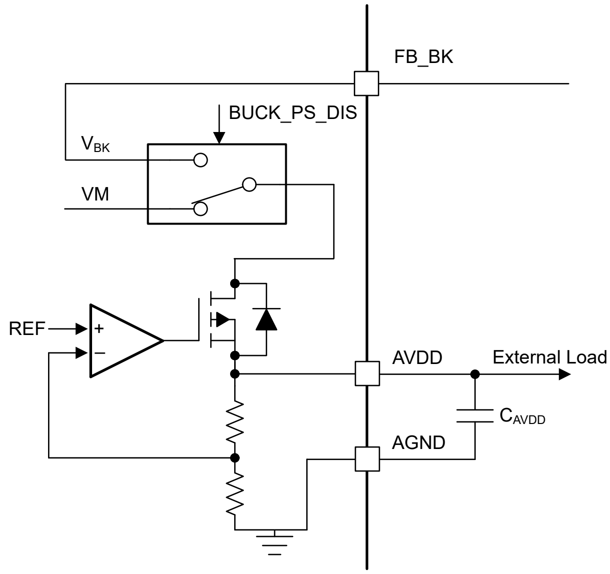

図 7-7. AVDD Linear Regulator Block Diagram

Use 式 1 to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply (BUCK_PS_DIS = 1b)

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{VM} of 24-V, drawing 20-mA out of AVDD results in a power dissipation as shown in 式 2.

$$\text{P} = (24\ \text{V} - 3.3\ \text{V}) \times 20\ \text{mA} = 414\ \text{mW} \quad (2)$$

Use 式 3 to calculate the power dissipated in the device by the AVDD linear regulator with buck output as supply (BUCK_PS_DIS = 0b)

$$P = (V_{FB\_BK} - V_{AVDD}) \times I_{AVDD} \quad (3)$$

7.3.5 Charge Pump

Since the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to turn-on the high-side FETs. The MCF8315A integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors (C_{CP}, C_{FLY}) for operation. See 図 7-1 and 表 5-1 for details on these capacitors (value, connection, and so forth).

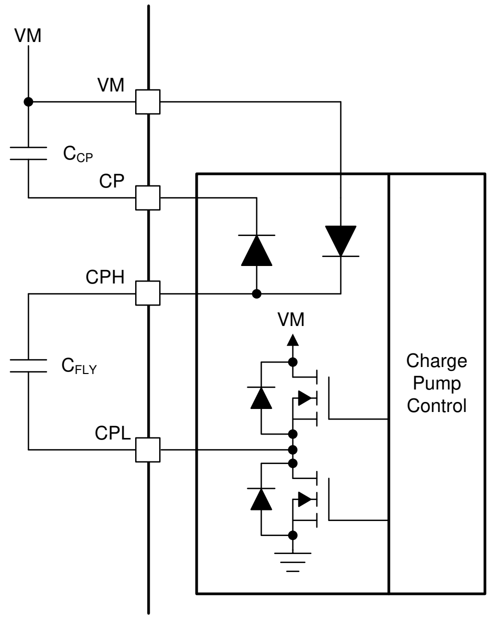

図 7-8. Charge Pump

7.3.6 Slew Rate Control

An adjustable gate-drive current control is provided for the output stage MOSFETs to achieve configurable slew rate for EMI mitigation. The MOSFET VDS slew rate is a critical factor for optimizing radiated emissions, total energy and duration of diode recovery spikes and switching voltage transients related to parasitic elements of the PCB. This slew rate is predominantly determined by the control of the internal MOSFET gate current as shown in 図 7-9.

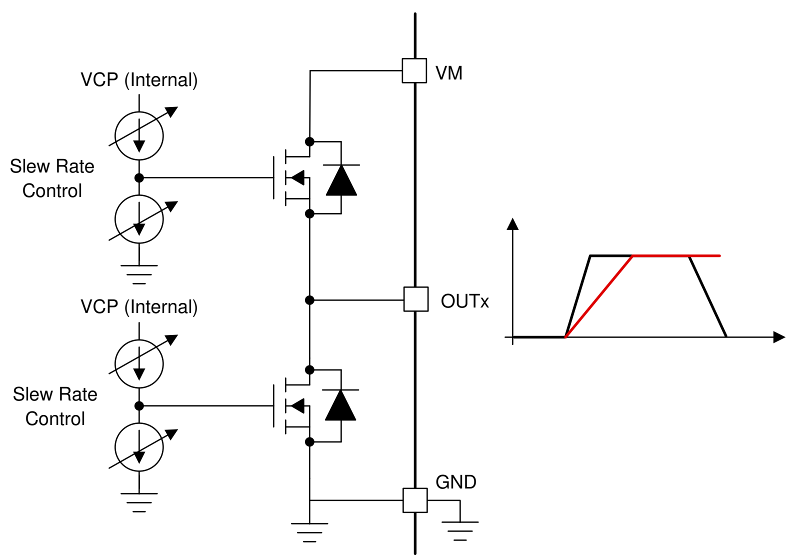

図 7-9. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted through SLEW_RATE settings. Slew rate can be configured as 25-V/µs, 50-V/µs, 125-V/µs or 200-V/µs. The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in 図 7-10.

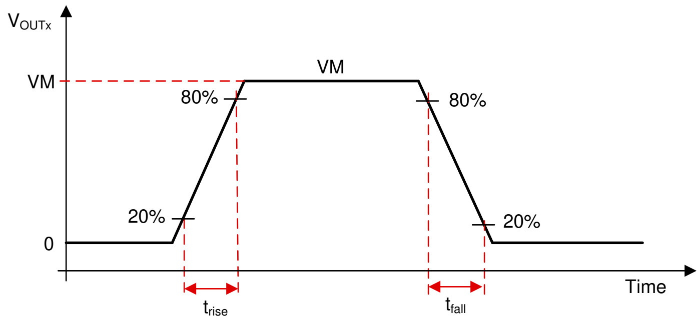

図 7-10. Slew Rate Timings

7.3.7 Cross Conduction (Dead Time)

The device is fully protected against any cross conduction of MOSFETs - during the switching of high-side and low-side MOSFETs, MCF8315A avoids shoot-through events by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that VGS of high-side MOSFET has dropped below turn-off level before switching on the low-side MOSFET of same half-bridge (or vice-versa) as shown in 図 7-11and 図 7-12. The VGS of the high-side and low-side MOSFETs (VGS_HS and VGS_LS) shown in 図 7-12 are internal signals.

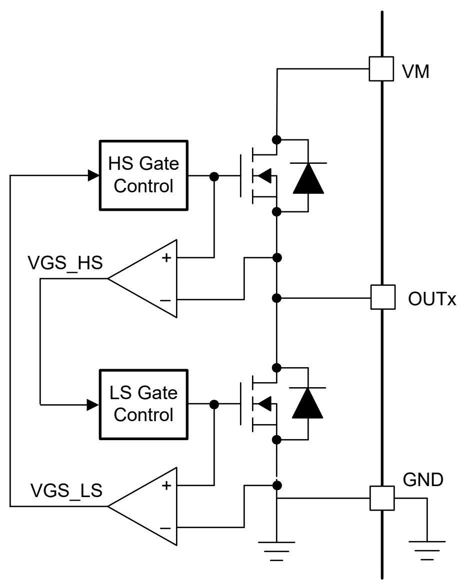

図 7-11. Cross Conduction Protection

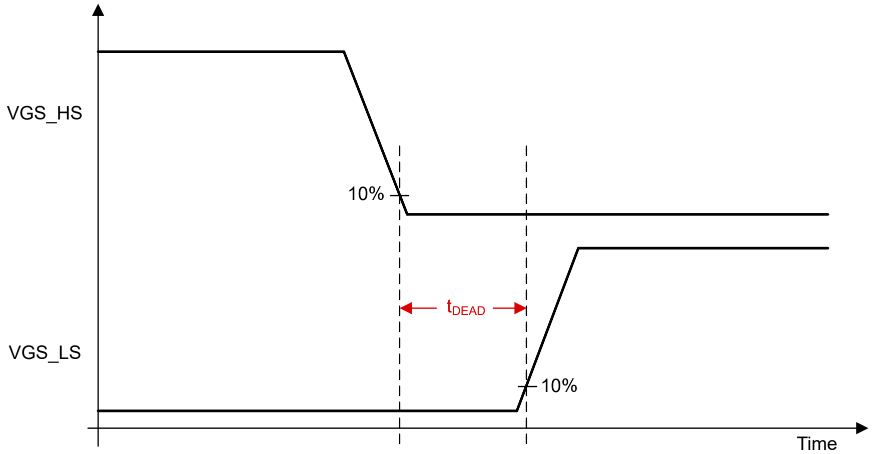

図 7-12. Dead Time

7.3.8 Speed Control

The MCF8315A offers four methods of directly controlling the speed of the motor. The speed control method is configured by SPEED_MODE. The speed command can be controlled in one of the following four ways.

- PWM input on SPEED pin by varying duty cycle of input signal
- Frequency input on SPEED pin by varying frequency of input signal
- Analog input on SPEED pin by varying amplitude of input signal
- Over I^2C by configuring DIGITAL_SPEED_CTRL register

The speed can also be indirectly controlled by varying the supply voltage (V_M).

The signal path from SPEED pin input (or I^2C based speed input) to output duty cycle (DUTY_OUT) applied to FETs is shown in 図 7-13.

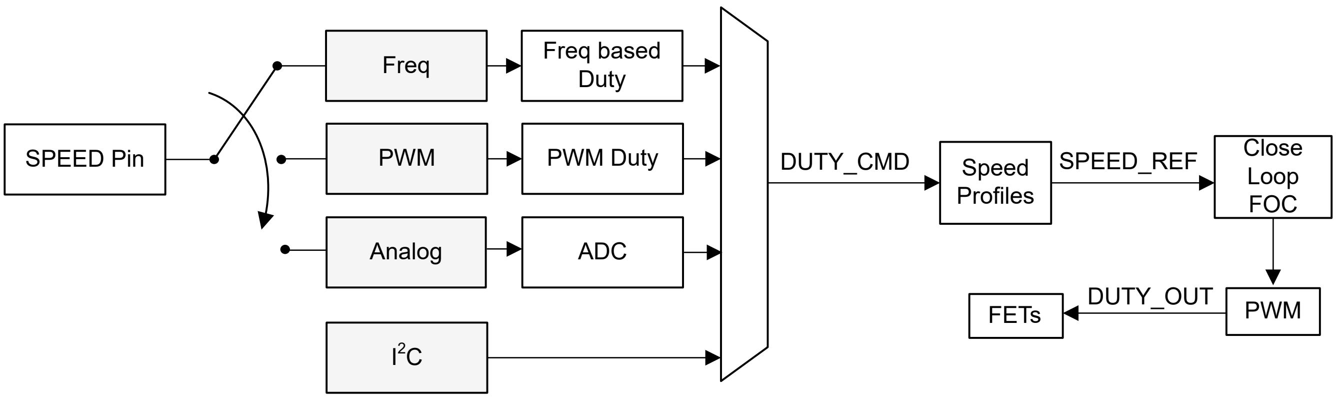

図 7-13. Multiplexing the Speed Command

注

1. Analog, PWM and Frequency based speed input modes are available only when MCF8315A is configured as a standby device (DEV_MODE = 0b).
2. I^2C based speed input mode is available in both sleep (DEV_MODE = 1b) and standby devices (DEV_MODE = 0b).
3. TI recommends adding a 200-ms delay after device power-up or wake-up from sleep mode before giving a speed command.
4. If MAX_SPEED is set to 0, SPEED_REF is clamped to zero (irrespective of DUTY_CMD) and motor is in stopped state.

7.3.8.1 Analog Mode Speed Control

Analog input based speed control can be configured by setting SPEED_MODE to 00b. In this mode, the duty command (DUTY_CMD) varies with the analog voltage input on the SPEED pin (V_{SPEED}). When $0 \leq V_{SPEED} \leq V_{EN\_SB}$, DUTY_CMD is set to zero and the motor is stopped. When $V_{EX\_SB} \leq V_{SPEED} \leq V_{ANA\_FS}$, DUTY_CMD varies linearly with V_{SPEED} as shown in 図 7-14. V_{EX_SB} and V_{EN_SB} are the standby entry and exit thresholds - refer セクション 7.4.1.2 for more information on V_{EX_SB} and V_{EN_SB}. When $V_{SPEED} > V_{ANA\_FS}$, DUTY_CMD is clamped to 100%.

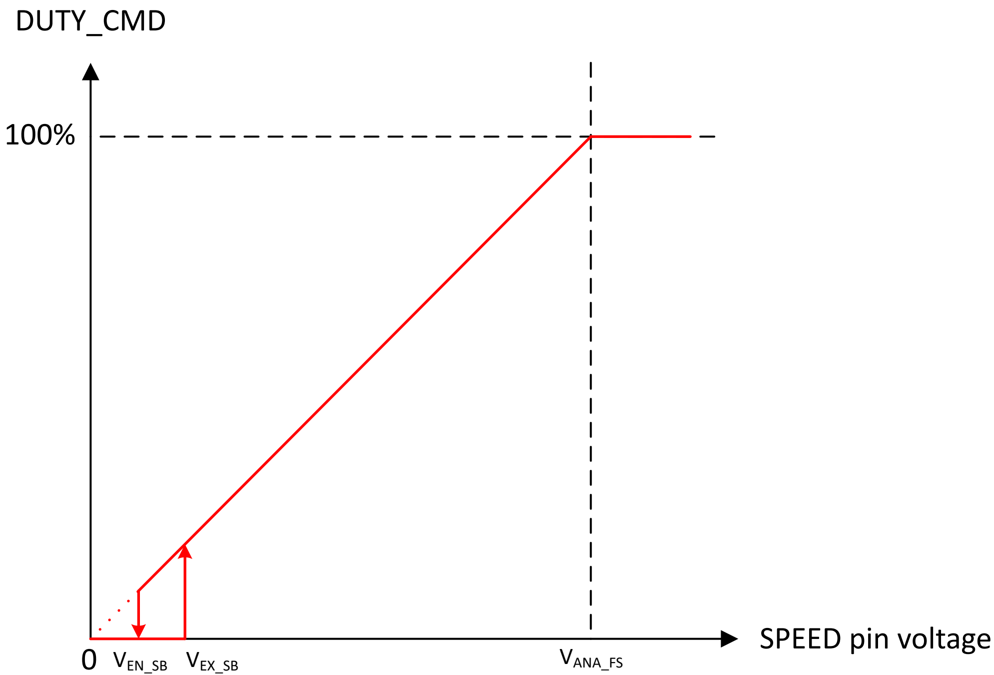

図 7-14. Analog Mode Speed Control

7.3.8.2 PWM Mode Speed Control

PWM based speed control can be configured by setting SPEED_MODE to 01b. In this mode, the PWM duty cycle applied to the SPEED pin can be varied from 0 to 100% and duty command (DUTY_CMD) varies linearly with the applied PWM duty cycle. When $0 \le Duty_{SPEED} \le Duty_{EN\_SB}$, DUTY_CMD is set to zero and the motor is stopped. When $Duty_{EX\_SB} \le Duty_{SPEED} \le 100\%$, DUTY_CMD varies linearly with $Duty_{SPEED}$ as shown in 図 7-15. $Duty_{EX\_SB}$ and $Duty_{EN\_SB}$ are the standby entry and exit thresholds - refer セクション 7.4.1.2 for more information on $Duty_{EX\_SB}$ and $Duty_{EN\_SB}$. The frequency of the PWM input signal applied to the SPEED pin is defined as f_{PWM} and the range for this frequency can be configured through SPEED_RANGE_SEL.

注

1. f_{PWM} is the frequency of the PWM signal the device can accept at SPEED pin to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phases. The PWM output frequency can be configured through PWM_FREQ_OUT (see セクション 7.3.15).
2. SLEEP_ENTRY_TIME should be set longer than the off time in PWM signal ($V_{SPEED} < V_{IL}$) at lowest duty input. For example, if f_{PWM} is 10 kHz and lowest duty input is 2%, SLEEP_ENTRY_TIME should be more than 98 μs to ensure there is no unintended sleep/standby entry.

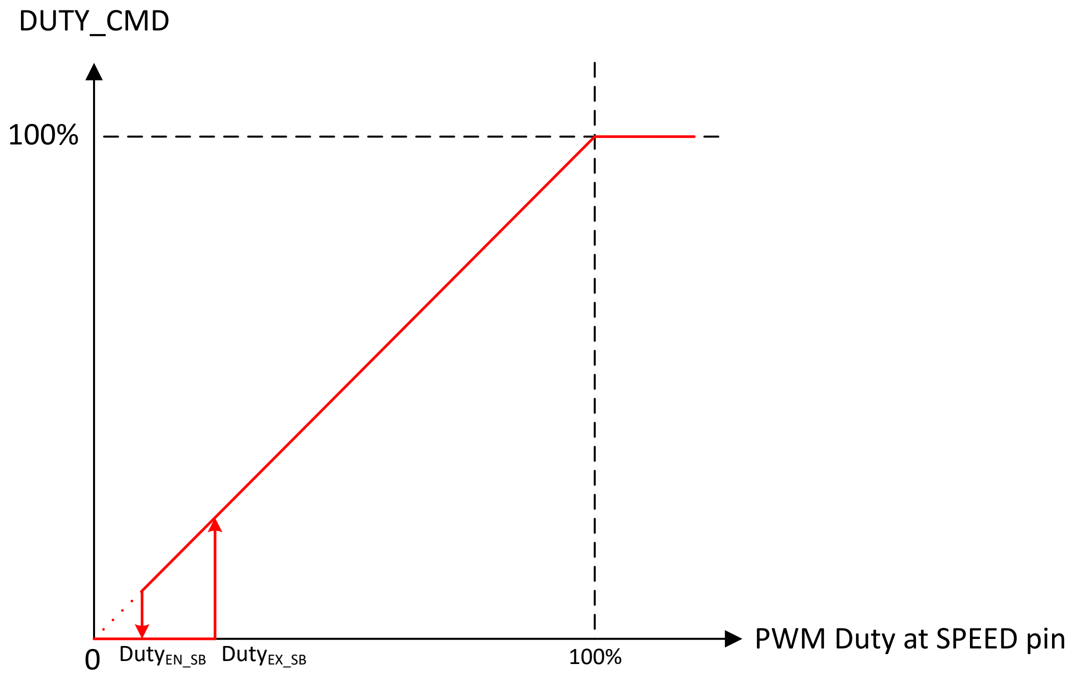

図 7-15. PWM Mode Speed Control

7.3.8.3 I2C based Speed Control

I2C based serial interface can be used for speed control by setting SPEED_MODE to 10b. In this mode, the speed command can be written directly into DIGITAL_SPEED_CTRL register. The SPEED pin can be used to control the sleep entry and exit - if SPEED pin input is set to a value lower than V_{EN_SL} after DIGITAL_SPEED_CTRL register has been set to 0b for a time longer than SLEEP_ENTRY_TIME, MCF8315A enters sleep state. When SPEED pin > V_{EX_SL}, MCF8315A exits sleep state and speed is controlled through DIGITAL_SPEED_CTRL register. If 0 ≤ DIGITAL_SPEED_CTRL register ≤ $DIGITAL\_SPEED\_CTRL_{EN\_SB}$ and SPEED pin > V_{EX_SL}, MCF8315A is in standby state. The relationship between DUTY_CMD and DIGITAL_SPEED_CTRL register is shown in 図 7-16. Refer セクション 7.4.1.2 for more information on $DIGITAL\_SPEED\_CTRL_{EN\_SB\ EX\_SB}$ and $DIGITAL\_SPEED\_CTRL_{EN\_SB\ EN\_SB}$.

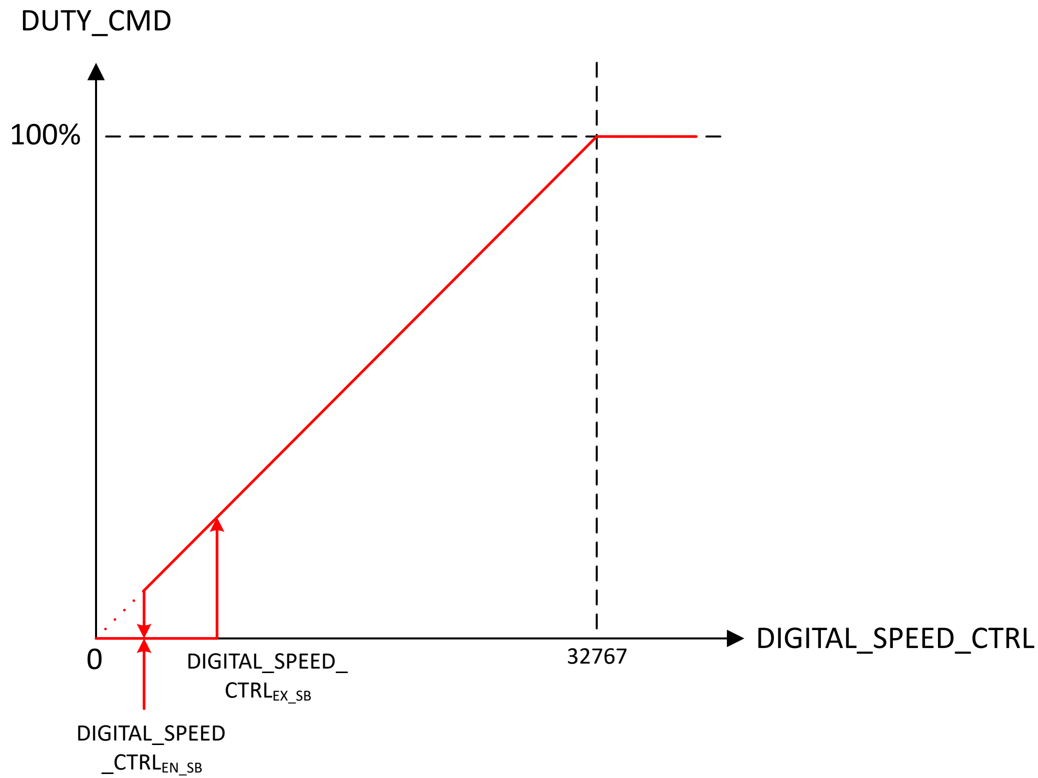

図 7-16. I2C Mode Speed Control

7.3.8.4 Frequency Mode Speed Control

Frequency based speed control is configured by setting SPEED_MODE to 11b. In this mode, duty command varies linearly as a function of the frequency of the square wave input at SPEED pin. When $0 \leq Freq_{SPEED} \leq Freq_{EN\_SB}$, DUTY_CMD is set to zero and the motor is stopped. When $Freq_{EX\_SB} \leq Freq_{SPEED} \leq$ INPUT_MAXIMUM_FREQ, DUTY_CMD varies linearly with $Freq_{SPEED}$ as shown in 図 7-17. $Freq_{EX\_SB}$ and $Freq_{EN\_SB}$ are the standby entry and exit thresholds - refer セクション 7.4.1.2 for more information on $Freq_{EX\_SB}$ and $Freq_{EN\_SB}$. Input frequency greater than INPUT_MAXIMUM_FREQ clamps the DUTY_CMD to 100%.

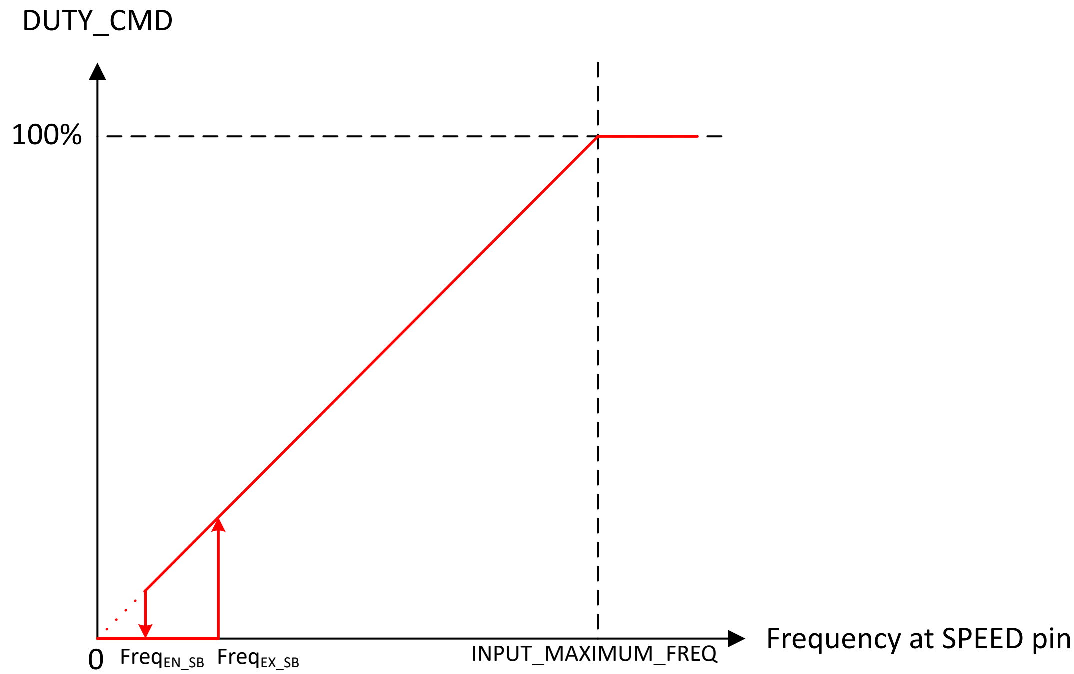

図 7-17. Frequency Mode Speed Control

7.3.8.5 Speed Profiles

MCF8315A supports three different kinds of speed profiles (linear, step, forward-reverse) to enable a variety of end-user applications. The different speed profiles can be configured through SPEED_PROFILE_CONFIG. When SPEED_PROFILE_CONFIG is set to 00b, the speed reference (SPEED_REF) is set by the duty command (DUTY_CMD) as shown in 図 7-18. When SPEED_PROFILE_CONFIG is set to 00b and DUTY_CMD > DUTY_HYST, any change in DUTY_CMD by a value less than DUTY_HYST does not produce a corresponding change in SPEED_REF; DUTY_HYST provides a hysteresis window around current DUTY_CMD for noise immunity.

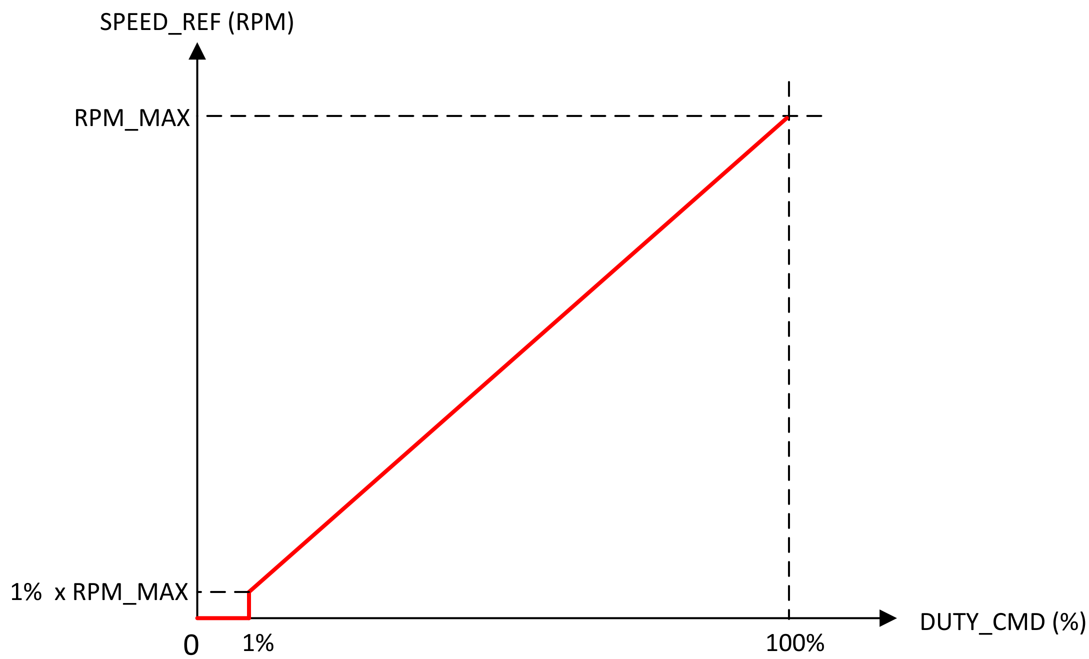

図 7-18. Speed reference (SPEED_PROFILE_CONFIG = 00b)

7.3.8.5.1 Linear Speed Profiles

注

For all types of speed profiles, a zero speed command (0-V in analog mode, 0% duty in PWM mode, DIGITAL_SPEED_CTRL = 0b I^{2}C mode or 0-Hz in frequency mode) stops the motor irrespective of the speed profile register settings.

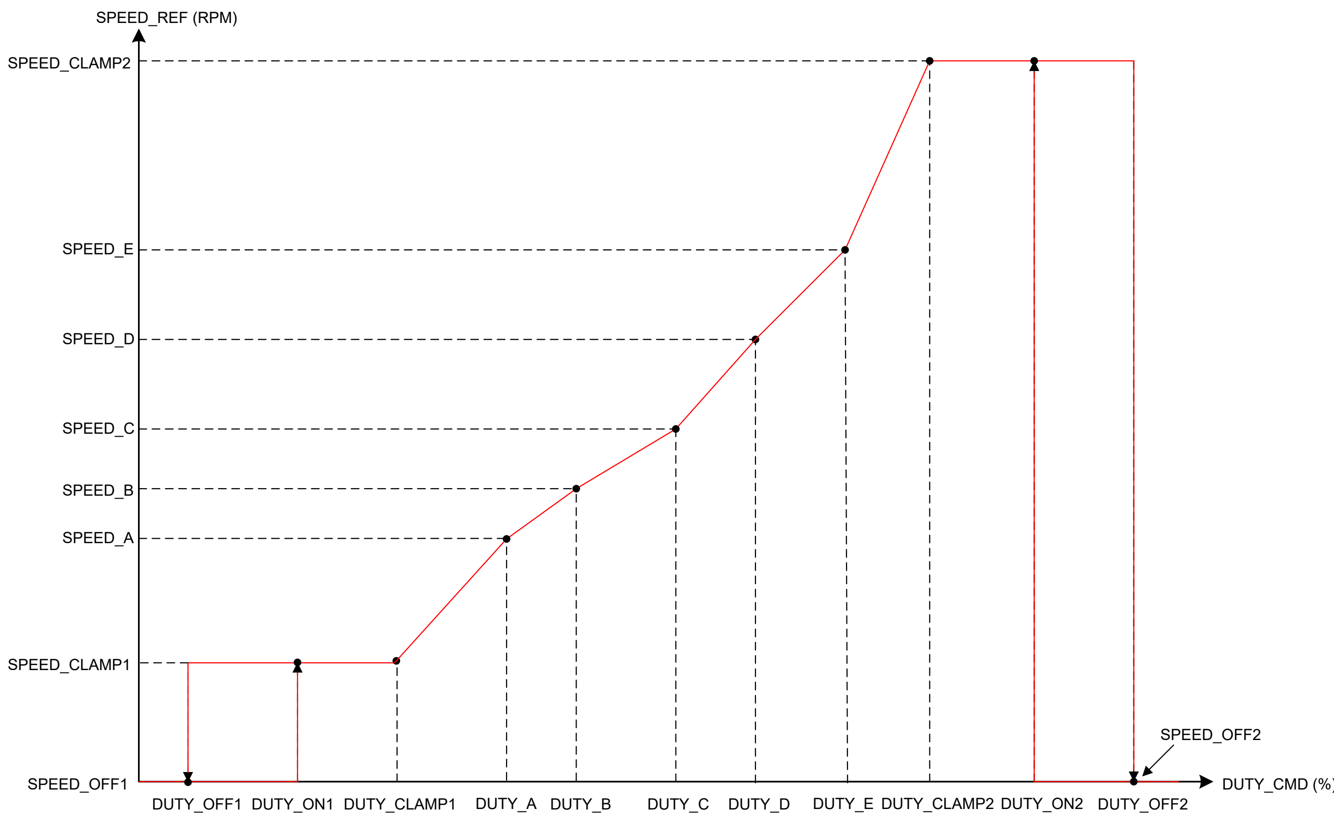

図 7-19. Linear Speed Profile

Linear speed profile can be configured by setting SPEED_PROFILE_CONFIG to 01b. Linear speed profile features speed references which change linearly between SPEED_CLAMP1 and SPEED_CLAMP2 with different slopes which can be set by configuring DUTY_x and SPEED_x combination.

- DUTY_ON1 configures the duty command above which MCF8315A starts driving the motor (to speed reference set by SPEED_CLAMP1) when the current speed reference is zero. When current speed reference is zero and duty command is below DUTY_ON1, MCF8315A continues to be in off state and motor is stationary.
- DUTY_OFF1 configures the duty command below which the speed reference changes to SPEED_OFF1.
- DUTY_CLAMP1 configures the duty command till which speed reference will be constant. SPEED_CLAMP1 configures this constant speed reference between between DUTY_OFF1 and DUTY_CLAMP1.
- DUTY_A configures the duty command for speed reference SPEED_A. The speed reference changes linearly between DUTY_CLAMP1 and DUTY_A.
- DUTY_B configures the duty command for speed reference SPEED_B. The speed reference changes linearly between DUTY_A and DUTY_B.
- DUTY_C configures the duty command for speed reference SPEED_C. The speed reference changes linearly between DUTY_B and DUTY_C.
- DUTY_D configures the duty command for speed reference SPEED_D. The speed reference changes linearly between DUTY_C and DUTY_D.

- DUTY_E configures the duty command for speed reference SPEED_E. The speed reference changes linearly between DUTY_D and DUTY_E.
- DUTY_CLAMP2 configures the duty command above which the speed reference will be constant at SPEED_CLAMP2. SPEED_CLAMP2 configures this constant speed reference between DUTY_CLAMP2 and DUTY_OFF2 . The speed reference changes linearly between DUTY_E and DUTY_CLAMP2.
- DUTY_ON2 configures the duty command below which MCF8315A starts driving the motor (to speed reference set by SPEED_CLAMP2) when the current speed reference is zero. When current speed reference is zero and duty command is above DUTY_ON2, MCF8315A continues to be in off state and motor is stationary.
- DUTY_OFF2 configures the duty command above which the speed reference will change from SPEED_CLAMP2 to SPEED_OFF2.

7.3.8.5.2 Staircase Speed Profile

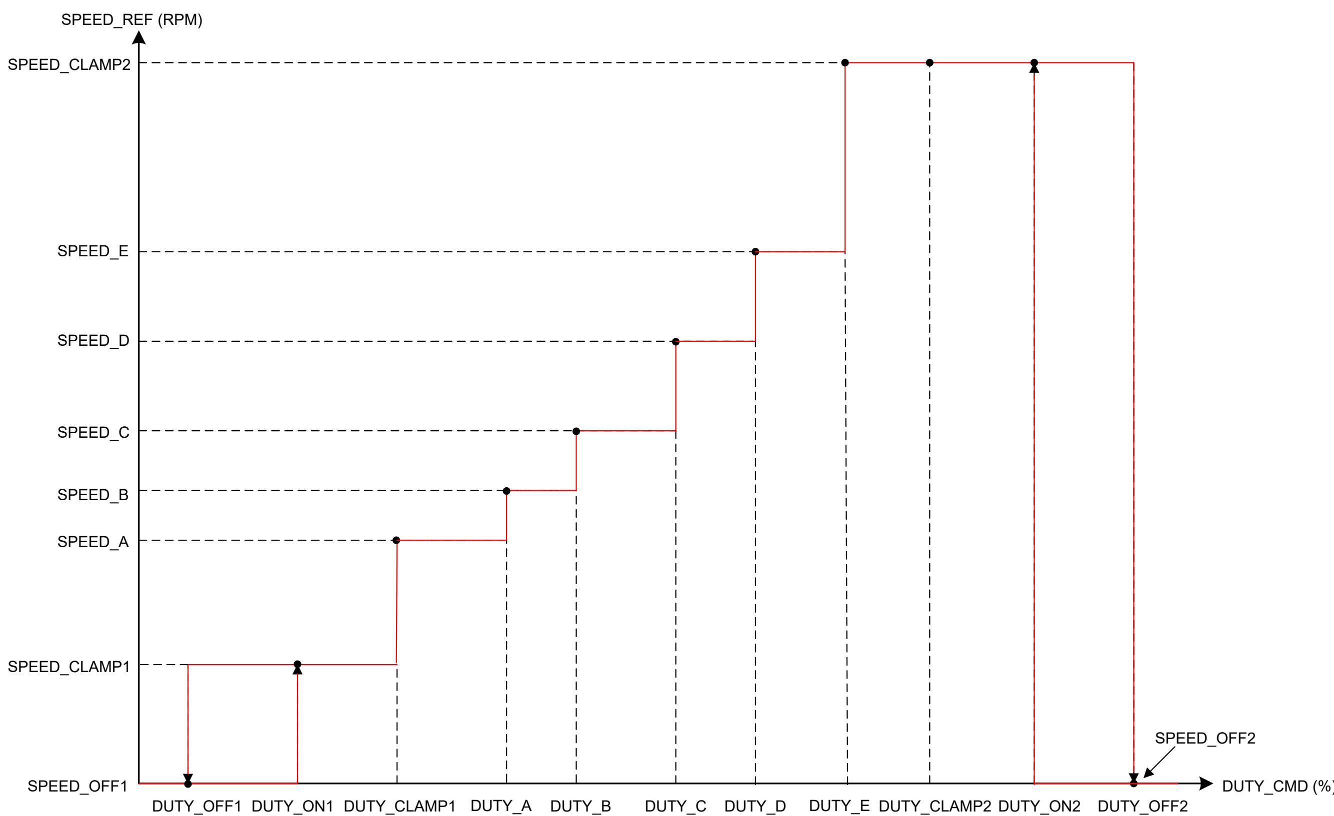

図 7-20. Staircase Speed Profile

Staircase speed profiles can be configured by setting SPEED_PROFILE_CONFIG to 10b. Staircase speed profiles feature speed changes in steps between SPEED_CLAMP1 and SPEED_CLAMP2. DUTY_x and SPEED_x configures the speed and duty command at which the step is increased

- DUTY_ON1 configures the duty command above which MCF8315A starts driving the motor (to speed reference set by SPEED_CLAMP1) when the current speed reference is zero. When current speed reference is zero and duty command is below DUTY_ON1, MCF8315A continues to be in off state and motor is stationary.
- DUTY_OFF1 configures the duty command below which the speed reference changes from SPEED_CLAMP1 to SPEED_OFF1.
- DUTY_CLAMP1 configures the duty command till which speed reference will be constant. SPEED_CLAMP1 configures this constant speed reference between DUTY_OFF1 and DUTY_CLAMP1.
- DUTY_A configures the duty command for speed reference SPEED_A. There is a step change in speed reference from SPEED_CLAMP1 to SPEED_A at DUTY_CLAMP1.

- DUTY_B configures the duty command for speed reference SPEED_B. There is a step change in speed reference from SPEED_A to SPEED_B at DUTY_A.
- DUTY_C configures the duty command for speed reference SPEED_C. There is a step change in speed reference from SPEED_B to SPEED_C at DUTY_B.
- DUTY_D configures the duty command for speed reference SPEED_D. There is a step change in speed reference from SPEED_C to SPEED_D at DUTY_C.
- DUTY_E configures the duty command for speed reference SPEED_E. There is a step change in speed reference from SPEED_D to SPEED_E at DUTY_D.
- DUTY_CLAMP2 configures the duty command above which the speed reference will be constant at SPEED_CLAMP2. SPEED_CLAMP2 configures this constant speed reference between DUTY_CLAMP2 and DUTY_OFF2. There is a step change in speed reference from SPEED_E to SPEED_CLAMP2 at DUTY_E.
- DUTY_ON2 configures the duty command below which MCF8315A starts driving the motor (to speed reference set by SPEED_CLAMP2) when the current speed reference is zero. When current speed reference is zero and duty command is above DUTY_ON2, MCF8315A continues to be in off state and motor is stationary.
- DUTY_OFF2 configures the duty command above which the speed reference will change from SPEED_CLAMP2 to SPEED_OFF2.

7.3.8.5.3 Forward-Reverse Speed Profile

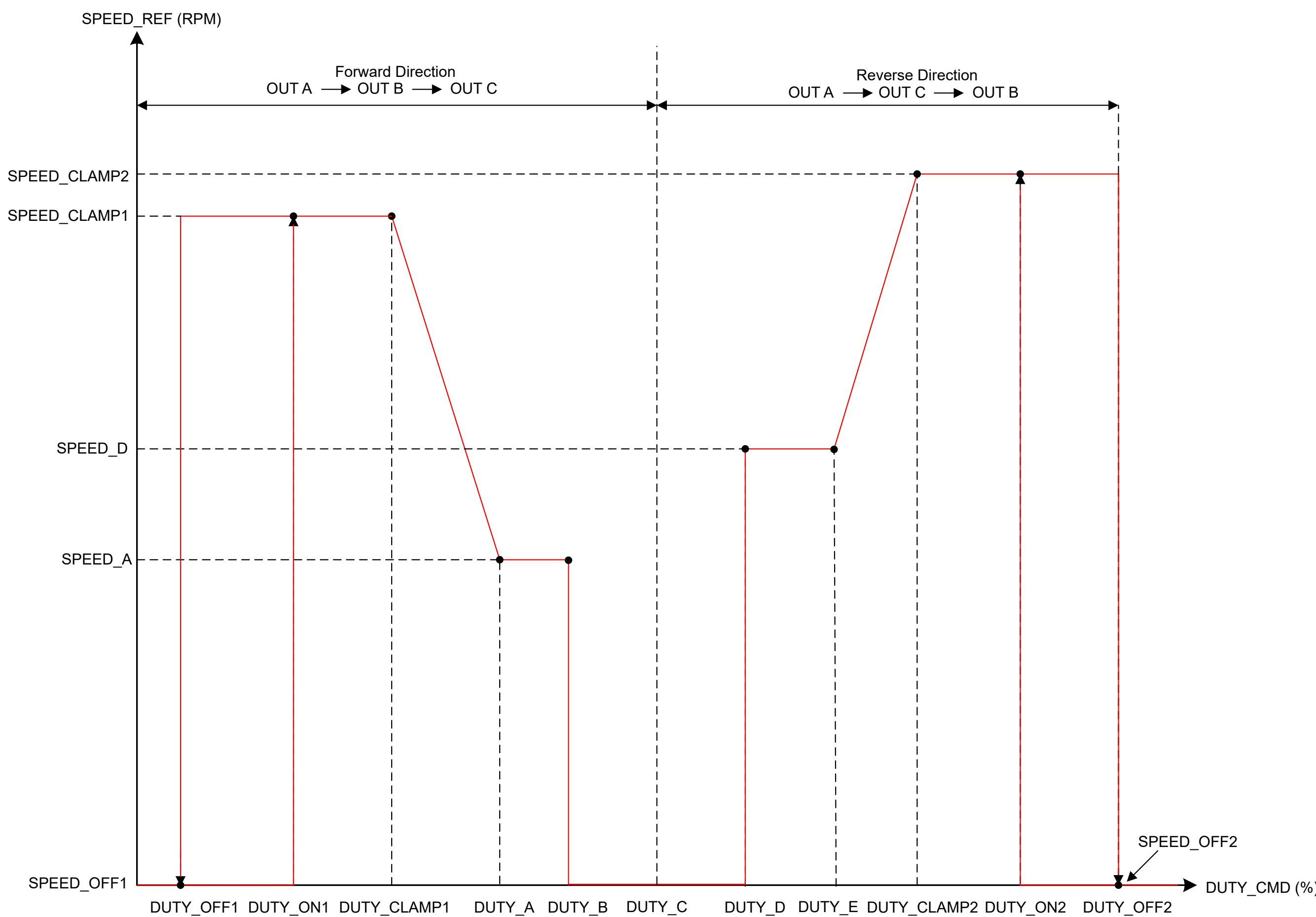

図 7-21. Forward-Reverse Speed Profile

Forward-Reverse speed profile can be configured by setting SPEED_PROFILE_CONFIG to 11b. Forward-Reverse speed profile features direction change through adjusting the duty command. DUTY_C configures duty command at which the direction will be changed. The Forward-Reverse speed profile can be used to eliminate the separate signal used to control the motor direction.

- DUTY_ON1 configures the duty command above which MCF8315A starts driving the motor in the forward direction (to speed reference set by SPEED_CLAMP1) when the current speed reference is zero. When current speed reference is zero and duty command is below DUTY_ON1, MCF8315A continues to be in off state and motor is stationary.
- DUTY_OFF1 configures the duty command below which the speed reference changes in the forward direction from SPEED_CLAMP1 to SPEED_OFF1.
- DUTY_CLAMP1 configures the duty command below which speed reference will be the constant in forward direction. SPEED_CLAMP1 configures constant speed reference between DUTY_CLAMP1 and DUTY_OFF1.
- DUTY_A configures the duty command for speed reference SPEED_A. The speed reference changes linearly between DUTY_CLAMP1 and DUTY_A.
- DUTY_B configures the duty command above which MCF8315A will be in off state. The speed reference remains constant at SPEED_A between DUTY_A and DUTY_B.
- DUTY_C configures the duty command at which the direction is changed
- DUTY_D configures the duty command above which the MCF8315A will be in running state in the reverse direction. SPEED_D configures constant speed reference between DUTY_D and DUTY_E.
- DUTY_CLAMP2 configures the duty command above which speed reference will be constant at SPEED_CLAMP2 in reverse direction. The speed reference changes linearly between DUTY_E and DUTY_CLAMP2.
- DUTY_ON2 configures the duty command below which MCF8315A starts driving the motor in the reverse direction (to speed reference set by SPEED_CLAMP2) when the current speed reference is zero. When current speed reference is zero and duty command is above DUTY_ON2, MCF8315A continues to be in off state and motor is stationary.
- DUTY_OFF2 configures the duty command above which the speed reference changes in the reverse direction from SPEED_CLAMP2 to SPEED_OFF2.

7.3.9 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when MCF8315A begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCF8315A includes a number of features to allow for reliable motor start-up under all of these conditions. 図 7-22 shows the motor start-up flow for each of the three initial motor states.

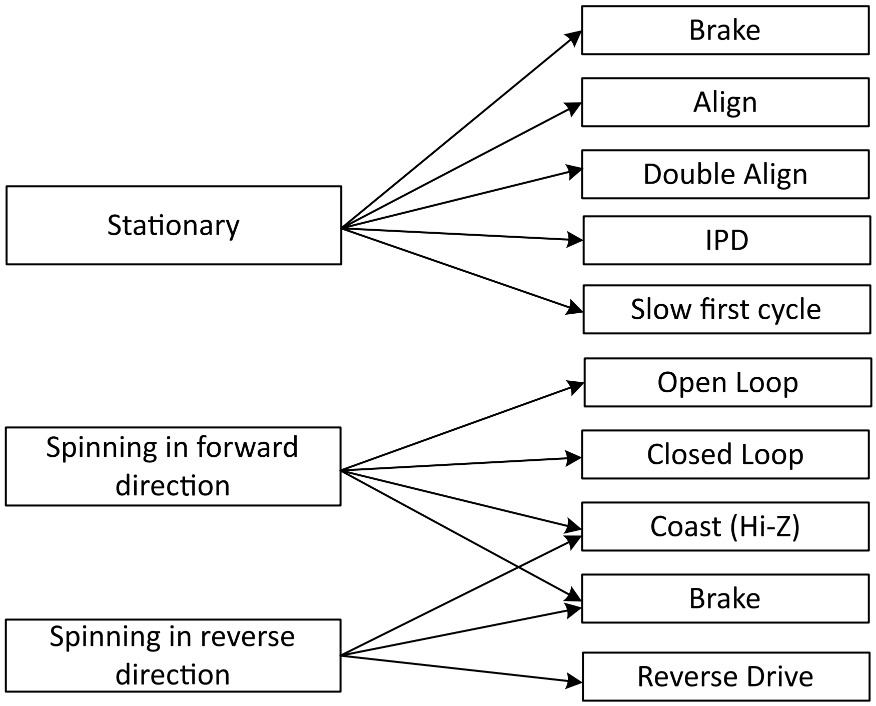

図 7-22. Starting the motor under different initial conditions

注

"Forward" means "spinning in the same direction as the commanded direction", and "Reverse" means "spinning in the opposite direction as the commanded direction".

7.3.9.1 Case 1 – Motor is Stationary

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCF8315A provides various options to initialize the commutation logic to the motor position and reliably start the motor.

- The align and double align techniques force the motor into alignment by applying a voltage across particular motor phases to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The slow first cycle method starts the motor by applying a low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

MCF8315A also provides a configurable brake option to ensure the motor is stationary before initiating one of the above start-up methods. Device enters open loop acceleration after going through the configured start-up method.

7.3.9.2 Case 2 – Motor is Spinning in the Forward Direction

If the motor is spinning forward (same direction as the commanded direction) with sufficient speed (BEMF), the MCF8315A resynchronizes with the spinning motor and continues commutation by going directly to closed loop operation. If the motor speed is too low for closed loop operation, MCF8315A enters open loop operation to accelerate the motor till it reaches sufficient speed to enter closed loop operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. This resynchronization feature can be enabled or disabled through RESYNC_EN. If resynchronization is disabled, the MCF8315A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

7.3.9.3 Case 3 – Motor is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction (the opposite direction as the commanded direction), the MCF8315A provides several methods to change the direction and drive the motor to the target speed reference in the commanded direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero speed. The motor achieves the shortest possible spin-up time when spinning in the reverse direction.

If reverse drive is not enabled, then the MCF8315A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

注

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

7.3.10 Motor Start Sequence (MSS)

図 7-23 shows the motor-start sequence implemented in the MCF8315A device.

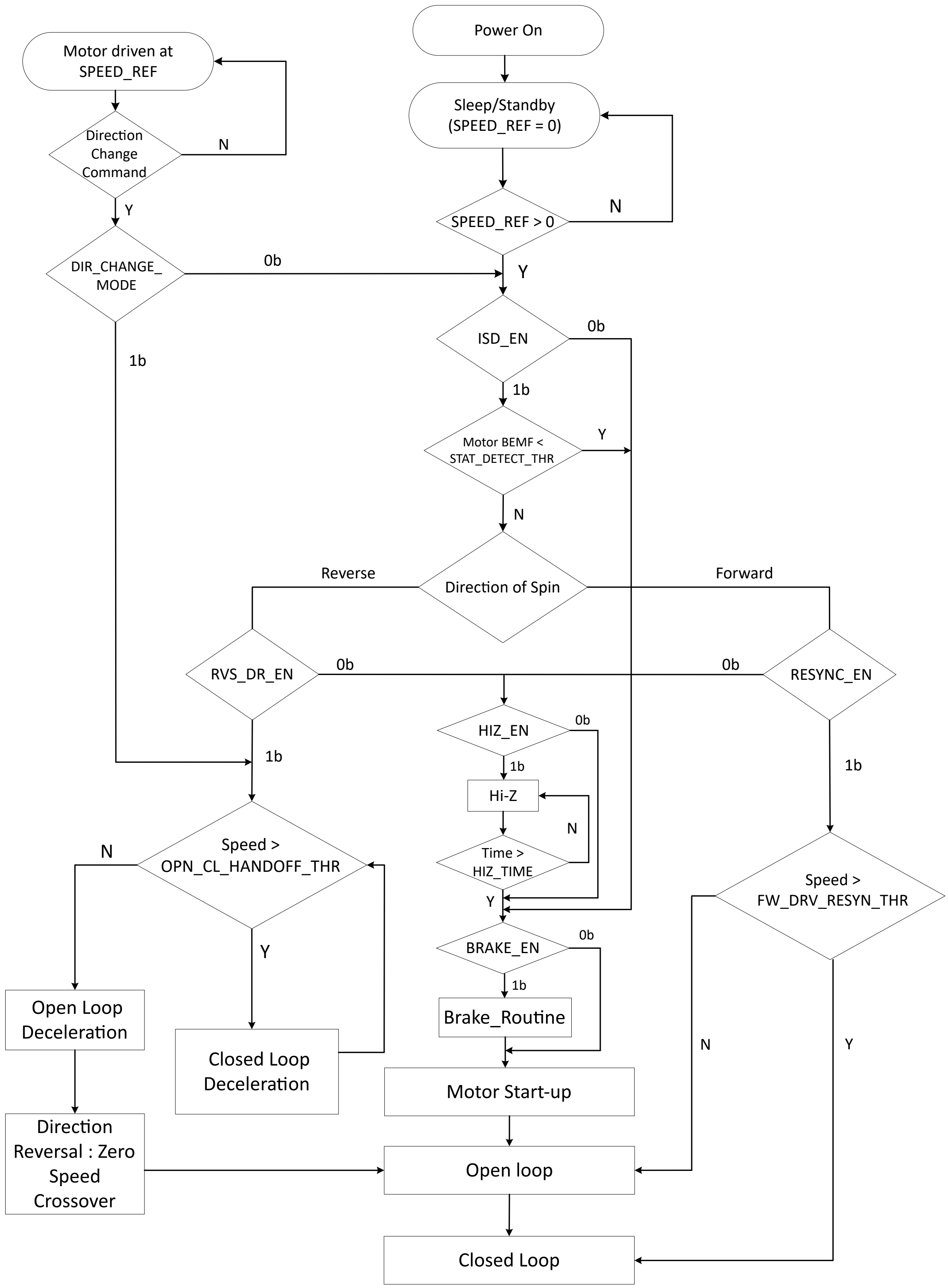

図 7-23. Motor Start Sequence

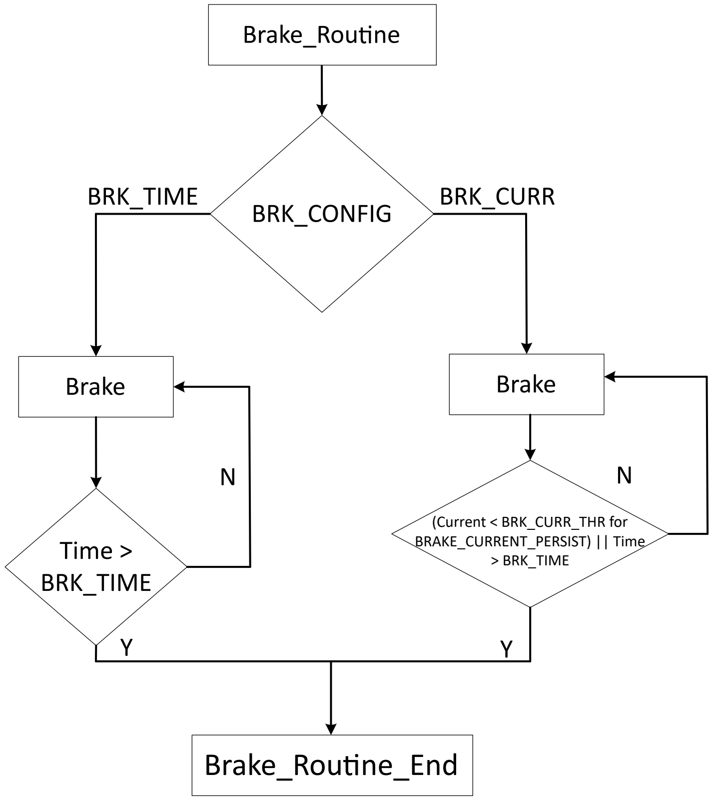

図 7-24. Brake Routine

Power-On State	This is the initial state of the Motor Start Sequence (MSS) when MCF8315A is powered on. In this state, MCF8315A configures the peripherals, initializes the algorithm parameters from EEPROM and prepares for driving the motor.
Sleep/Standby	In this state, SPEED_REF is set to zero and MCF8315A is either in sleep or standby mode depending on DEV_MODE and SPEED/WAKE pin voltage.
SPEED_REF > 0 Judgement	When SPEED_REF is set to greater than zero, MCF8315A exits the sleep/standby state and proceeds to ISD_EN judgement. As long as SPEED_REF is set to zero, MCF8315A stays in sleep/standby state.
Direction Change Command Judgement	When a direction change command is received, MCF8315A proceeds to DIR_CHANGE_MODE judgement.
DIR_CHANGE_MODE Judgement	If DIR_CHANGE_MODE is set to 0b, MCF8315A initiates direction change by proceeding to ISD_EN judgement. Instead, if DIR_CHANGE_MODE is set to 1b, MCF8315A initiates direction change by proceeding to Speed > OPN_CL_HANDOFF_THR judgement.
ISD_EN Judgement	MCF8315A checks to see if the initial speed detect (ISD) function is enabled (ISD_EN = 1b). If ISD is enabled, MSS proceeds to the BEMF < STAT_DETECT_THR judgement. Instead, if ISD is disabled, the MSS proceeds directly to the BRAKE_EN judgement.
BEMF < STAT_DETECT_THR or BEMF < FG_BEMF_THR Judgement	ISD determines the initial condition (speed, angle, direction of spin) of the motor (see セクション 7.3.10.1). If motor is deemed to be stationary (BEMF < STAT_DETECT_THR or BEMF < FG_BEMF_THR), the MSS proceeds to BRAKE_EN judgement. If the motor is not stationary, MSS proceeds to verify the direction of spin.

Direction of spin Judgement	The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the MCF8315A proceeds to the RESYNC_EN judgement. If the motor is spinning in the reverse direction, the MSS proceeds to the RVS_DR_EN judgement.
RESYNC_EN Judgement	If RESYNC_EN is set to 1b, MCF8315A proceeds to Speed > Open to Closed Loop Handoff (Resync) judgement. If RESYNC_EN is set to 0b, MSS proceeds to HIZ_EN judgement.
Speed > FW_DRV_RESYN_THR Judgement	If motor speed > FW_DRV_RESYN_THR, MCF8315A uses the speed and position information from the ISD to transition to the closed loop state (see セクション 7.3.10.2) directly. If motor speed < FW_DRV_RESYN_THR, MCF8315A transitions to open loop state.
RVS_DR_EN Judgement	The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1b). If it is enabled, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled (RVS_DR_EN = 0b), the MSS advances to the HIZ_EN judgement.
Speed > OPN_CL_HANDOFF_THR Judgement	The MSS checks to see if the reverse speed is high enough for MCF8315A to decelerate in closed loop. Till the speed (in reverse direction) is above OL_CL_HANDOFF_THR, MSS stays in closed loop deceleration. If speed is below OPN_CL_HANDOFF_THR, then the MSS transitions to open loop deceleration.
Reverse Closed Loop, Open Loop Deceleration and Zero Speed Crossover	The MCF8315A resynchronizes in the reverse direction, decelerates the motor in closed loop till motor speed falls below the handoff threshold. (see *Reverse Drive*). When motor speed in reverse direction is too low, the MCF8315A switches to open-loop, decelerates the motor in open-loop, crosses zero speed, and accelerates in the forward direction in open-loop before entering closed loop operation after motor speed is sufficiently high.
HIZ_EN Judgement	The MSS checks to determine whether the coast (Hi-Z) function is enabled (HIZ_EN = 1b). If the coast function is enabled (HIZ_EN = 1b), the MSS advances to the coast routine. If the coast function is disabled (HIZ_EN = 0b), the MSS advances to the BRAKE_EN judgement.
Coast (Hi-Z) Routine	The device coasts the motor by turning OFF all six MOSFETs for a certain time configured by HIZ_TIME.
BRAKE_EN Judgement	The MSS checks to determine whether the brake function is enabled (BRAKE_EN = 1b). If the brake function is enabled (BRAKE_EN = 1b), the MSS advances to the brake routine. If the brake function is disabled (BRAKE_EN = 0b), the MSS advances to the motor start-up state (see セクション 7.3.10.4).
Brake Routine	MCF8315A implements either a time based brake (duration configured by BRK_TIME) or a current based brake (brake applied till phase currents < BRK_CURR_THR for BRAKE_CURRENT_PERSIST) based on BRK_CONFIG. Current based brake has a timeout to ensure brake state ends in case phase currents do not drop below BRK_CURR_THR within BRK_TIME. Time based brake can be applied either using high-side or low-side MOSFETs based on BRK_MODE configuration. Current based brake is applied using low-side MOSFETs only.
Closed Loop State	In this state, the MCF8315A drives the motor with sensorless FOC based on rotor angle estimation.

7.3.10.1 Initial Speed Detect (ISD)

The ISD function is used to identify the initial condition of the motor and is enabled by setting ISD_EN to 1b. The initial speed, position and direction is determined by sensing the three phase voltages. ISD can be disabled by setting ISD_EN to 0b. If the function is disabled (ISD_EN set to 0b), the MCF8315A does not perform the initial speed detect function and proceeds to check if the brake routine (BRAKE_EN) is enabled.

7.3.10.2 Motor Resynchronization

The motor resynchronization function works when the ISD and resynchronization functions are both enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the commanded direction). The speed and position information measured during ISD are used to initialize the drive state of the MCF8315A, which can transition directly into closed loop (or open loop if motor speed is not sufficient for closed loop operation) state without needing to stop the motor. In the MCF8315A, motor resynchronization can be enabled/disabled through RESYNC_EN bit. If motor resynchronization is disabled, the device proceeds to check if the motor coast (Hi-Z) routine is enabled.

7.3.10.3 Reverse Drive

The MCF8315A uses the reverse drive function to change the direction of the motor rotation when ISD_EN and RVS_DR_EN are both set to 1b and the ISD determines the motor spin direction to be opposite to that of the commanded direction. Reverse drive includes synchronizing with the motor speed in the reverse direction, reverse decelerating the motor through zero speed, changing direction, and accelerating in open loop in forward (or commanded) direction until the device transitions into closed loop in forward direction (see 図 7-25). . MCF8315A provides the option of using the forward direction parameters or a separate set of reverse drive parameters by configuring REV_DRV_CONFIG.

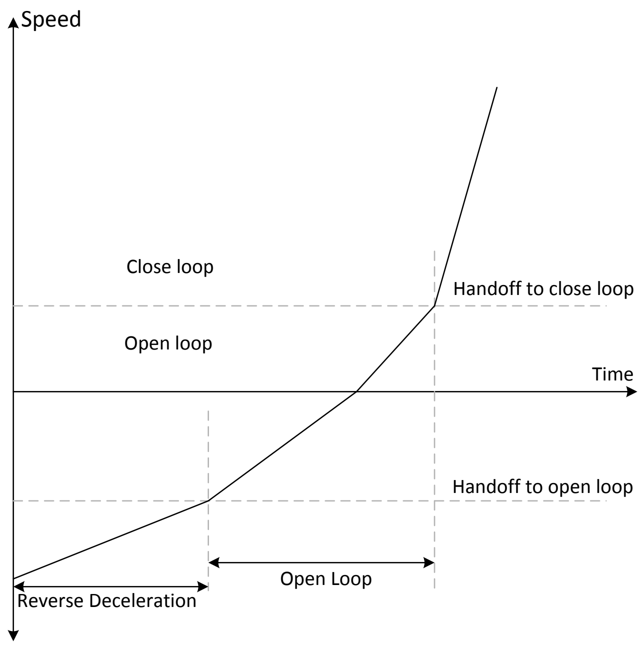

図 7-25. Reverse Drive Function

7.3.10.3.1 Reverse Drive Tuning

MCF8315A provides the option of tuning the open to closed loop handoff threshold, open loop acceleration (and deceleration) rates and open loop current limit in reverse drive to values different to those used in forward drive operation; the reverse drive specific parameters can be used by setting REV_DRV_CONFIG to 1b. If REV_DRV_CONFIG is set to 0b, MCF8315A uses the equivalent parameters configured for forward drive operation during the reverse drive operation too.

The speed at which motor would enter the open loop in reverse direction can be configured using REV_DRV_HANDOFF_THR. For a smooth transition without jerks or loss of synchronism, user can configure an appropriate current limit when the motor is spinning in open loop during speed reversal using REV_DRV_OPEN_LOOP_CURRENT. The open loop acceleration rates for the forward direction during speed reversal are defined using REV_DRV_OPEN_LOOP_ACCEL_A1 and REV_DRV_OPEN_LOOP_ACCEL_A2.

The reverse drive open loop deceleration rate, when the motor is decelerating in the opposite direction to zero speed, can be configured as a percentage of reverse drive open loop acceleration using REV_DRV_OPEN_LOOP_DEC.

7.3.10.4 Motor Start-up

There are different options available for motor start-up from a stationary position and these options can be configured by MTR_STARTUP. In align and double align mode, the motor is aligned to a known position by injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle.

7.3.10.4.1 Align

Align is enabled by configuring MTR_STARTUP to 00b. The MCF8315A aligns the motor by injecting a DC current through a particular phase pattern for a certain time configured by ALIGN_TIME. The phase pattern during align is generated based on ALIGN_ANGLE. In the MCF8315A, the current limit during align is configured through ALIGN_OR_SLOW_CURRENT LIMIT.

A fast change in the phase current may result in a sudden change in the driving torque and this could result in acoustic noise. To avoid this, the MCF8315A ramps up the current from 0 to the current limit at a configurable ramp rate set by ALIGN_SLOW_RAMP_RATE. At the end of align routine the motor, will be aligned at the known position.

7.3.10.4.2 Double Align

Double align is enabled by configuring MTR_STARTUP to 01b. Single align is not reliable when the initial position of the rotor is 180º out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In order to improve the reliabilty of align based start-up, the MCF8315A provides the option of double align start-up. In double align start-up, MCF8315A uses a phase pattern for the second align that is 90º ahead of the first align phase pattern. In double align, relevant parameters like align time, current limit, ramp rate are the same as in the case of single align - two different phase patterns are applied in succession with the same parameters to ensure that the motor will be aligned to a known position irrespective of initial rotor position.

7.3.10.4.3 Initial Position Detection (IPD)

Initial Position Detection (IPD) can be enabled by configuring MTR_STARTUP to 10b. In IPD, inductive sense method is used to determine the initial position of the motor using the spatial variation in the motor inductance.

Align or double align may result in the motor spinning in the reverse direction before starting open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. IPD does not wait for the motor to align with the commutation and therefore can allow for a faster motor start-up sequence. IPD works well when the inductance of the motor varies as a function of position. IPD works by pulsing current in to the motor and hence can generate acoustics which must be taken into account when determining the best start-up method for a particular application.

7.3.10.4.3.1 IPD Operation

IPD operates by sequentially applying six different phase patterns according to the following sequence: BC-> CB-> AB-> BA-> CA-> AC (see 図 7-26). When the current reaches the threshold configured by IPD_CURR_THR, the MCF8315A stops driving the particular phase pattern and measures the time taken to reach the current threshold from when the particular phase pattern was applied. Thus, the time taken to reach IPD_CURR_THR is measured for all six phase patterns - this time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

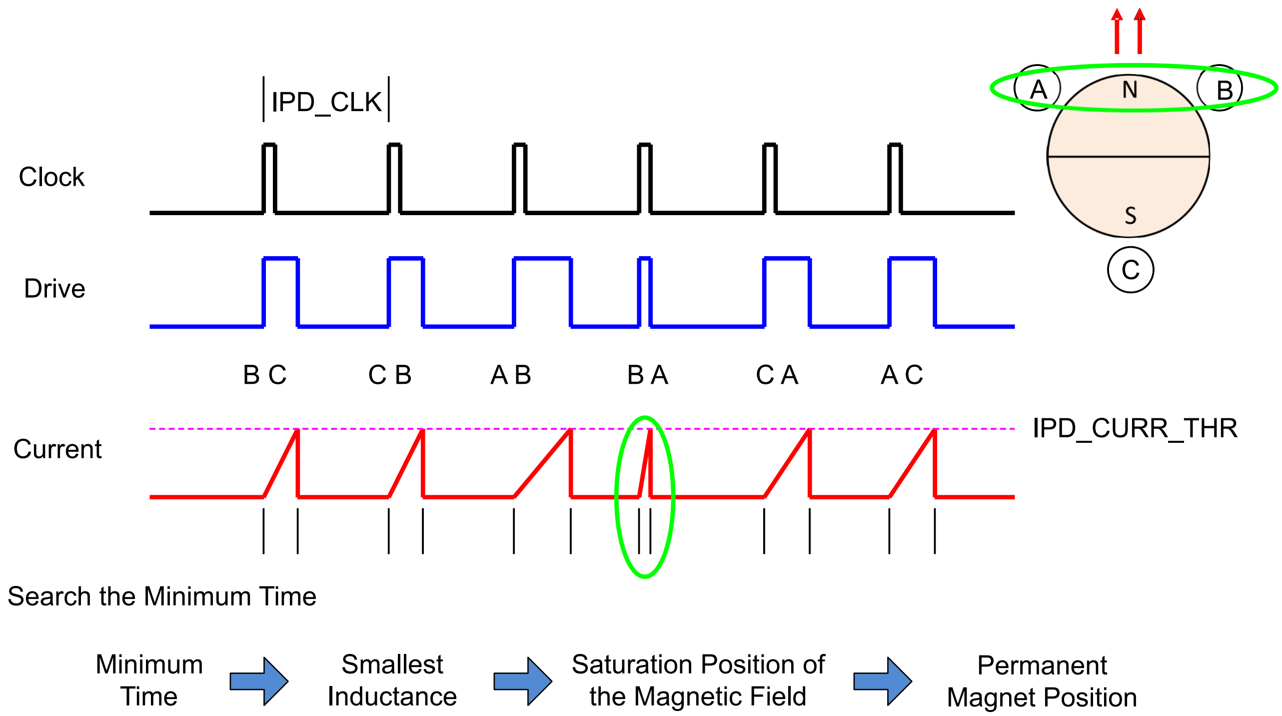

図 7-26. IPD Function

7.3.10.4.3.2 IPD Release Mode

Two modes are available for configuring the way the MCF8315A stops driving the motor when the current threshold is reached. The recirculate (or brake) mode is selected if IPD_RLS_MODE = 0b. In this configuration, the low-side (LSC) MOSFET remains ON to allow the current to recirculate between the MOSFET (LSC) and body diode (LSA) (see 図 7-27). Hi-Z mode is selected if IPD_RLS_MODE = 1b. In Hi-Z mode, both the high-side (HSA) and low-side (LSC) MOSFETs are turned OFF and the current recirculates through the body diodes back to the power supply (see 図 7-28).

In the Hi-Z mode, the phase current has a faster settle-down time, but that can result in a voltage increase on V_M. The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between V_M and PGND to absorb the energy. If the voltage surge cannot be contained or if it is unacceptable for the application, recirculate mode must be used. When using the recirculate mode, select the IPD_CLK_FREQ appropriately to give the current in the motor windings enough time to decay to 0-A before the next IPD phase pattern is applied.

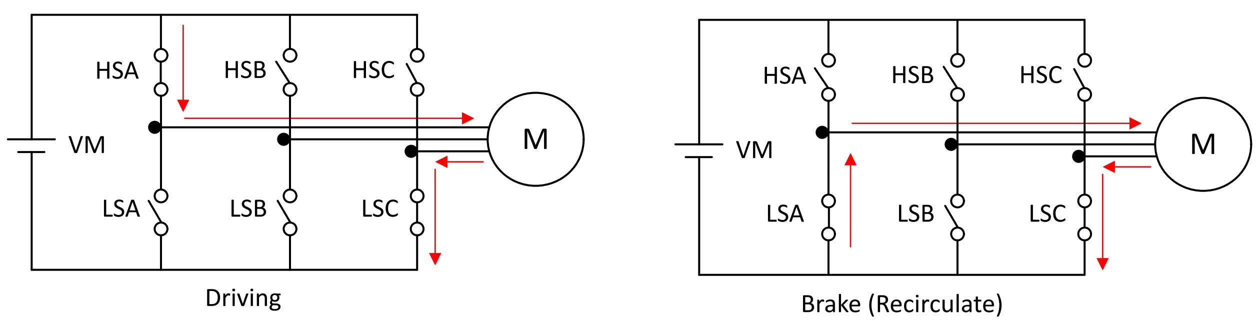

図 7-27. IPD Release Mode - Brake (0b)

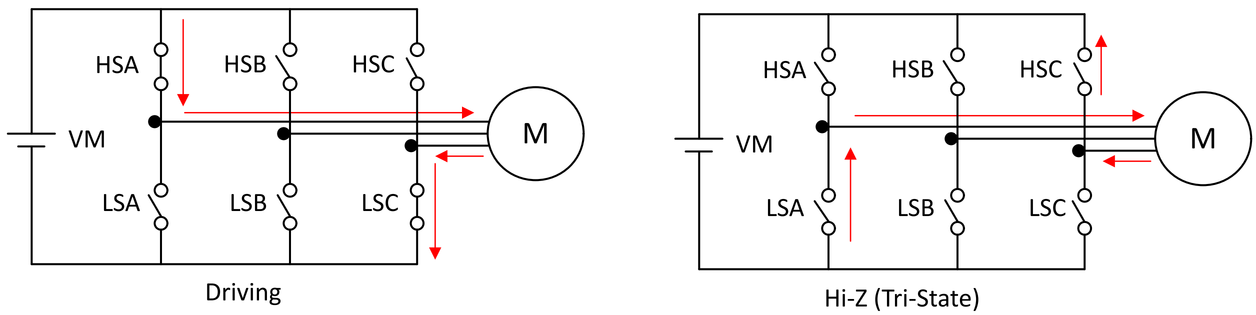

図 7-28. IPD Release Mode - Tristate (1b)

7.3.10.4.3.3 IPD Advance Angle

After the initial position is detected, the MCF8315A begins driving the motor in open loop at an angle specified by IPD_ADV_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD_ADV_ANGLE to allow for smooth acceleration in the application (see 図 7-29).

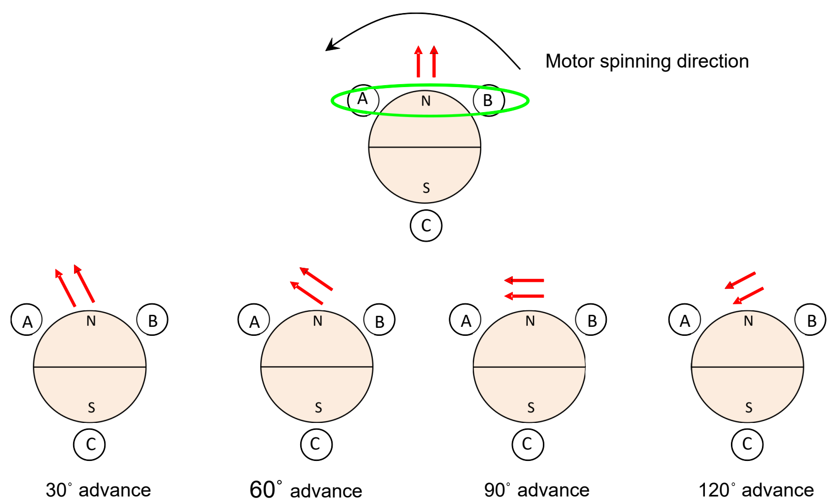

図 7-29. IPD Advance Angle

7.3.10.4.4 Slow First Cycle Startup

Slow First Cycle start-up is enabled by configuring MTR_STARTUP to 11b. In slow first cycle start-up, the MCF8315A starts motor commutation at a frequency defined by SLOW_FIRST_CYCLE_FREQ. The frequency configured is used only for first cycle, and then the motor commutation follows acceleration profile configured by open loop acceleration coefficients A1 and A2. The slow first cycle frequency has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

7.3.10.4.5 Open loop

Upon completing the motor position initialization with either align, double align, IPD or slow first cycle, the MCF8315A begins to accelerate the motor in open loop. During open loop, the speed is increased with a fixed current limit. In open loop, the control PI loops for I_q and I_d actively control the currents. The angle during open loop is provided from the ramp generator as shown in 図 7-30

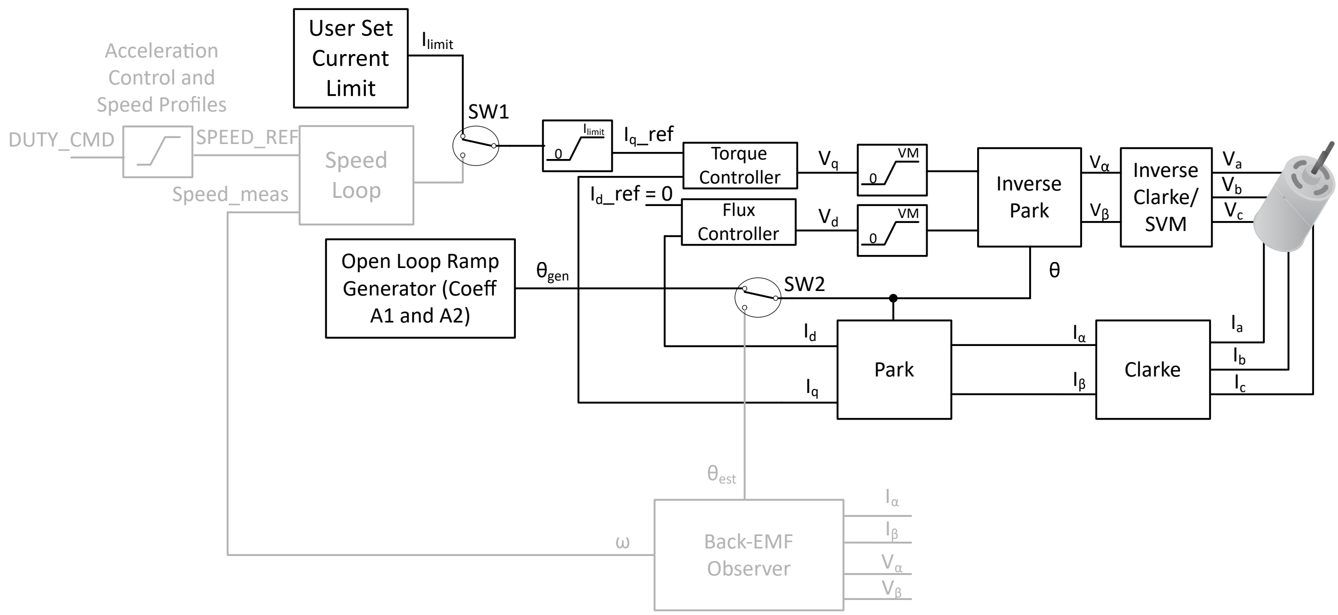

図 7-30. Open Loop

In MCF8315A, the current limit threshold is configured through OL_ILIMIT_CONFIG and is set by ILIMIT or OL_ILIMIT based on configuration of OL_ILIMIT_CONFIG. The function of the open-loop operation is to drive the motor to a speed at which the motor generates sufficient BEMF to allow the back-EMF observer to accurately detect the position of the rotor. The motor is accelerated in open loop and speed at any given time is determined by 式 4. In MCF8315A, open loop acceleration coefficients, A1 and A2 are configured through OL_ACC_A1 and OL_ACC_A2 respectively.

$$Speed(t) = A1 * t + 0.5 * A2 * t^2 \quad (4)$$

7.3.10.4.6 Transition from Open to Closed Loop

Once the motor has reached a sufficient speed for the back-EMF observer to estimate the angle and speed of the motor, the MCF8315A transitions into closed loop state. This handoff speed is automatically determined based on the measured back-EMF and motor speed. Users also have an option to manually set the handoff speed by configuring OPN_CL_HANDOFF_THR and setting AUTO_HANDOFF_EN to 0b. In order to have smooth transition and avoid speed transients, the theta_error (Θ_{gen} - Θ_{est}) is decreased linearly after transition. The ramp rate of theta_error reduction can be configured using THETA_ERROR_RAMP_RATE. If the current limit set during the open loop is high and if it is not reduced before transition to closed loop, the motor speed may momentarily rise to higher values than SPEED_REF after transition into closed loop. In order to avoid such speed variations, configure the IQ_RAMP_EN to 1b, so that i_{q_ref} decreases prior to transition into closed loop. However if the final speed reference (SPEED_REF) is more than two times the open loop to closed loop hand off speed (OPN_CL_HANDOFF_THR), then i_{q_ref} is not decreased independent of the IQ_RAMP_EN setting, to enable faster motor acceleration.

After hand off to closed loop at a sufficient speed, there could be still some theta error, as the estimators may not be fully aligned. A slow acceleration can be used after the open loop to closed loop transition, ensuring that the theta error reduces to zero. The slow acceleration can be configured using CL_SLOW_ACC.

図 7-31 shows the control sequence in open to closed loop transition. The current i_{q_ref} reduces to a lower value in current decay region, if IQ_RAMP_EN is set to 1b. If IQ_RAMP_EN is set to 0b, then the current decay region will not be present in the transition sequence.

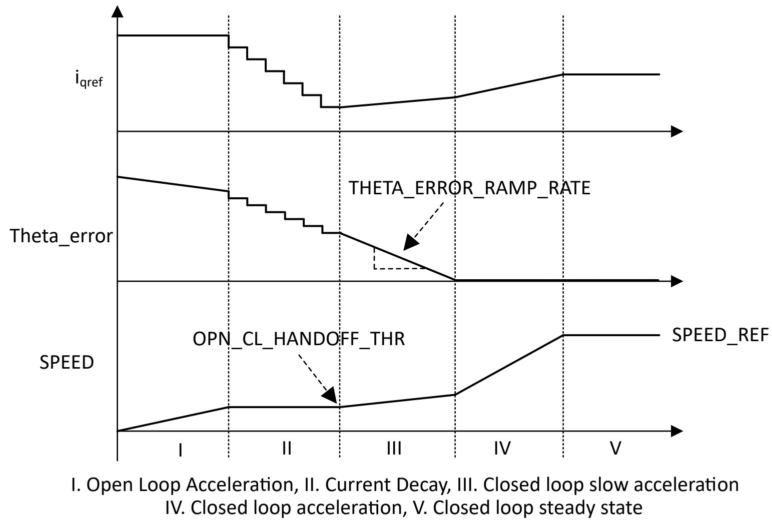

図 7-31. Control Sequence in Open to Closed Loop Transition

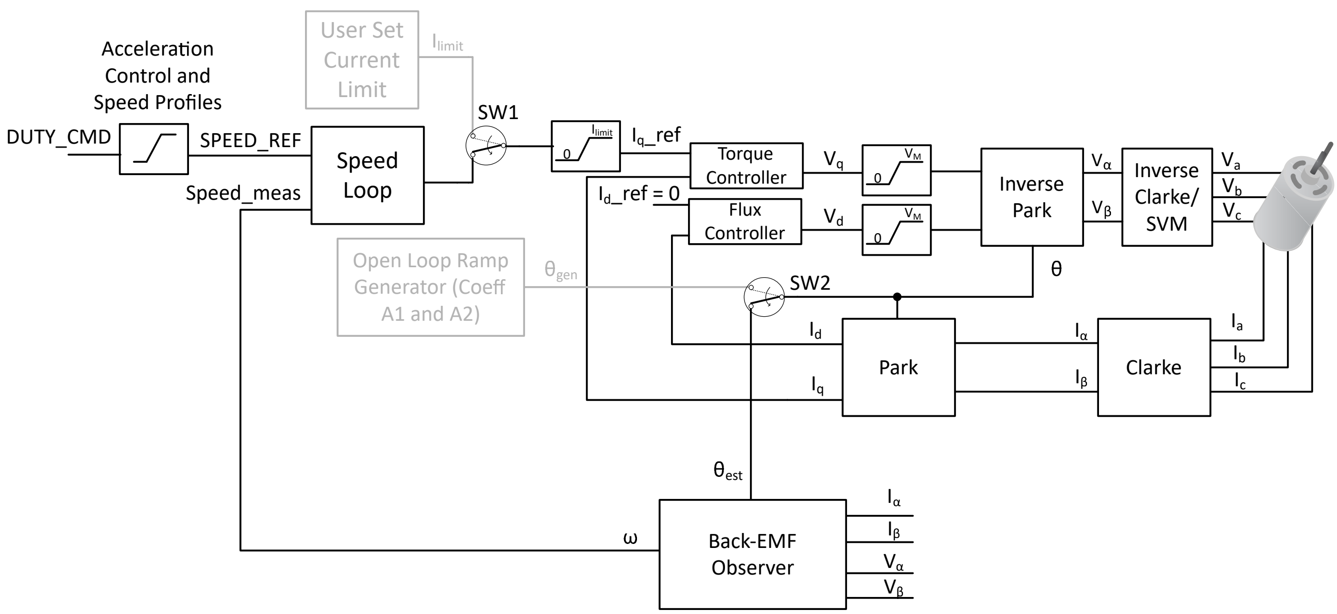

図 7-32. Open to Closed Loop Transition Control Block Diagram

7.3.11 Closed Loop Operation

The MCF8315A drives the motor using Field Oriented Control (FOC) as shown in 図 7-33. In closed loop operation, the motor angle (Θ_{est}) and speed (Speed_meas) are estimated using the back-EMF observer. The speed and current regulation are achieved using PI control loop. In order to achieve maximum efficiency, the direct axis current is set to zero (I_{d_ref} = 0), which will ensure that stator and rotor field are orthogonal (90° out of phase) to each other.

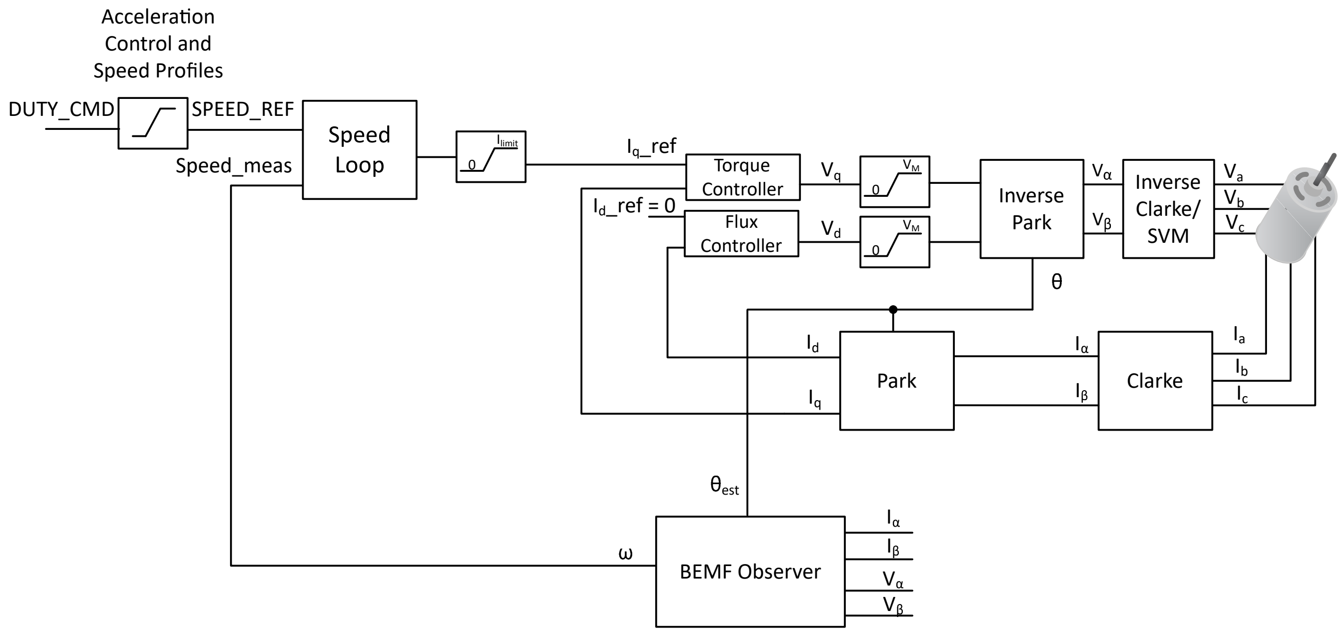

図 7-33. Closed Loop FOC Control

7.3.11.1 Closed loop accelerate

To prevent sudden changes in the torque applied to the motor which could result in acoustic noise, the MCF8315A device provides the option of limiting the maximum rate at which the speed command can change. The closed loop acceleration rate parameter sets the maximum rate at which the speed command changes (shown in 図 7-34). In the MCF8315A, closed loop acceleration rate is configured through CL_ACC.

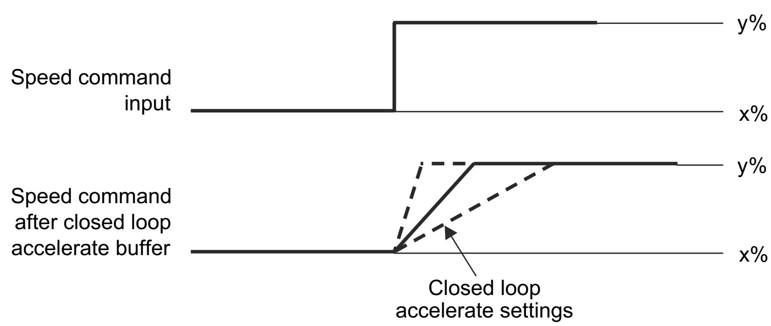

図 7-34. Closed loop accelerate

7.3.11.2 Speed PI Control

The integrated speed control loop helps maintain a constant speed over varying operating conditions. The K_p and K_i coefficients are configured through SPD_LOOP_KP and SPD_LOOP_KI. The output of the speed loop is used to generate the current reference for torque control (I_{q_ref}). The output of the speed loop is limited to implement a current limit. The current limit is set by configuring ILIMIT. When output of the speed loop saturates, the integrator is disabled to prevent integral wind-up.

SPEED_REF is derived from the duty command input and speed profiles configured by the user and SPEED_MEAS is the estimated speed from the back-EMF observer.

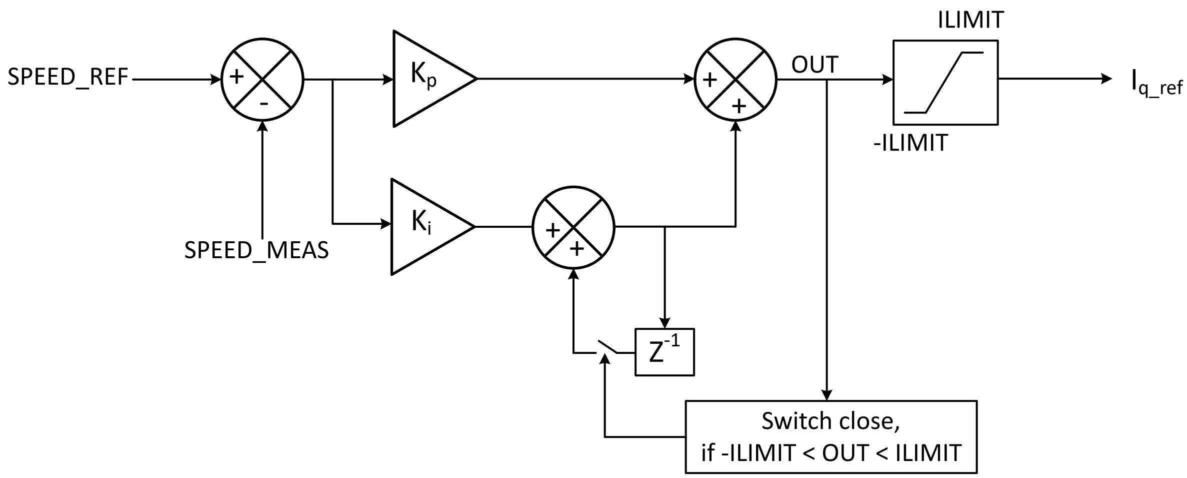

図 7-35. Speed PI Control

7.3.11.3 Current PI Control

The MCF8315A has two PI controllers, one each for I_d and I_q to control flux and torque separately. K_p and K_i coefficients are the same for both PI controllers and are configured through CURR_LOOP_KP and CURR_LOOP_KI. The outputs of the current control loops are used to generate voltage signals V_d and V_q to be applied to the motor. The outputs of the current loops are clamped to supply voltage V_M. I_d current PI loop is executed first and output of I_d current PI loop V_d is checked for saturation. When the output of the current loop saturates, the integration is disabled to prevent integral wind-up.

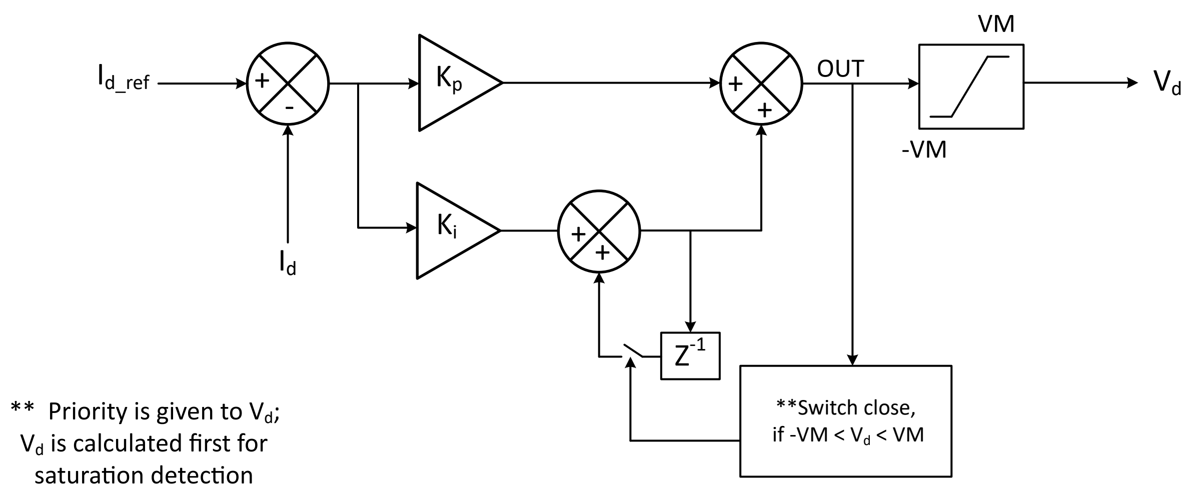

図 7-36. I_d Current PI Control

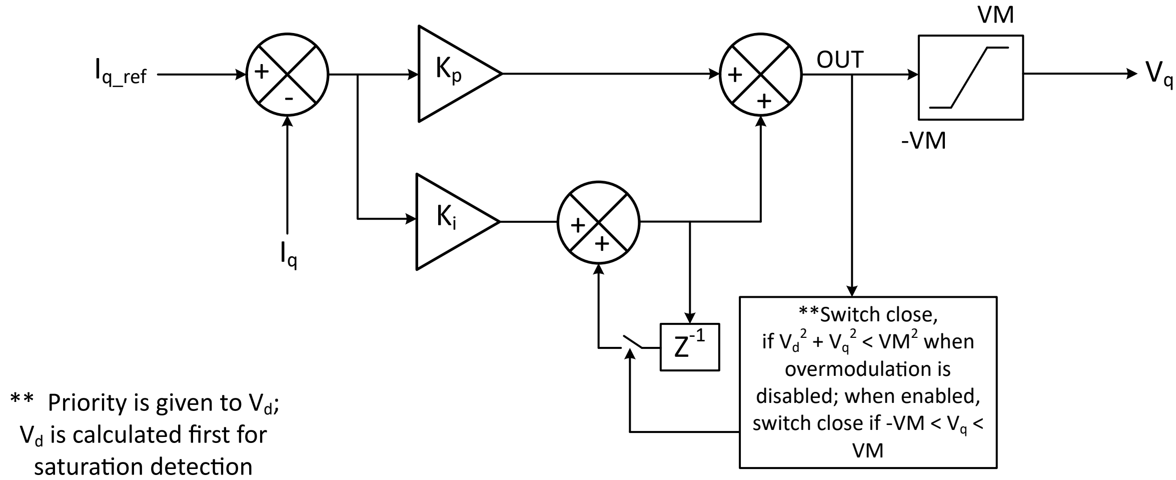

図 7-37. I_q Current PI Control

7.3.11.4 Overmodulation

MCF8315A provides an overmodulation option to operate the motor at a higher speed at the same VM voltage by increasing the applied fundamental phase voltage by suitably modifying the applied PWM pattern - the higher fundamental phase voltage is accompanied by an increase in higher order harmonics. This feature can be enabled by setting OVERMODULATION_ENABLE to 1b.

7.3.12 Motor Parameters

The MCF8315A uses the motor resistance, motor inductance and motor back-EMF constant to estimate motor position when operating in closed loop. The MCF8315A has the capability of measuring these motor parameters in the offline state (see Motor Parameter Extraction Tool (MPET)). Offline measurement of parameters, when enabled, takes place before normal motor operation. The user can also disable the offline measurement and configure motor parameters through EEPROM. This feature of offline motor parameter measurement is useful to account for motor to motor variation during manufacturing.

7.3.12.1 Motor Resistance

For a wye-connected motor, the motor phase resistance refers to the resistance from the phase output to the center tap, R_{PH} (denoted as R_{PH} in 図 7-38). For a delta-connected motor, the motor phase resistance refers to the equivalent phase to center tap in the wye configuration in 図 7-38.

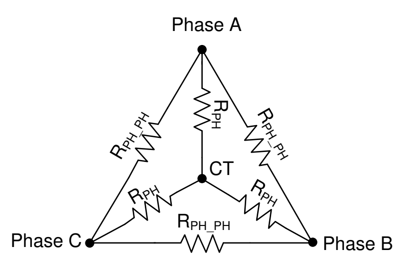

図 7-38. Motor Resistance

For both the delta-connected and the wye-connected motor, the easy way to get the equivalent R_{PH} is to measure the resistance between two phase terminals (R_{PH_PH}), and then divide this value by two, R_{PH} = ½ R_{PH_PH}. In wye-connected motor, if user has access to center tap (CT), R_{PH} can also be measured between center tap (CT) and phase terminal.

Configure the motor resistance (R_{PH}) to a nearest value from 表 7-2.

表 7-2. Motor Resistance Look-Up Table

MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	0.145	0x80	0.465	0xC0	2.1
0x01	0.006	0x41	0.150	0x81	0.470	0xC1	2.2
0x02	0.007	0x42	0.155	0x82	0.475	0xC2	2.3
0x03	0.008	0x43	0.160	0x83	0.480	0xC3	2.4
0x04	0.009	0x44	0.165	0x84	0.485	0xC4	2.5
0x05	0.010	0x45	0.170	0x85	0.490	0xC5	2.6
0x06	0.011	0x46	0.175	0x86	0.495	0xC6	2.7
0x07	0.012	0x47	0.180	0x87	0.50	0xC7	2.8
0x08	0.013	0x48	0.185	0x88	0.51	0xC8	2.9
0x09	0.014	0x49	0.190	0x89	0.52	0xC9	3.0
0x0A	0.015	0x4A	0.195	0x8A	0.53	0xCA	3.2
0x0B	0.016	0x4B	0.200	0x8B	0.54	0xCB	3.4
0x0C	0.017	0x4C	0.205	0x8C	0.55	0xCC	3.6
0x0D	0.018	0x4D	0.210	0x8D	0.56	0xCD	3.8
0x0E	0.019	0x4E	0.215	0x8E	0.57	0xCE	4.0
0x0F	0.020	0x4F	0.220	0x8F	0.58	0xCF	4.2
0x10	0.022	0x50	0.225	0x90	0.59	0xD0	4.4
0x11	0.024	0x51	0.230	0x91	0.60	0xD1	4.6
0x12	0.026	0x52	0.235	0x92	0.61	0xD2	4.8
0x13	0.028	0x53	0.240	0x93	0.62	0xD3	5.0
0x14	0.030	0x54	0.245	0x94	0.63	0xD4	5.2
0x15	0.032	0x55	0.250	0x95	0.64	0xD5	5.4
0x16	0.034	0x56	0.255	0x96	0.65	0xD6	5.6
0x17	0.036	0x57	0.260	0x97	0.66	0xD7	5.8
0x18	0.038	0x58	0.265	0x98	0.67	0xD8	6.0
0x19	0.040	0x59	0.270	0x99	0.68	0xD9	6.2
0x1A	0.042	0x5A	0.275	0x9A	0.69	0xDA	6.4
0x1B	0.044	0x5B	0.280	0x9B	0.70	0xDB	6.6
0x1C	0.046	0x5C	0.285	0x9C	0.72	0xDC	6.8
0x1D	0.048	0x5D	0.290	0x9D	0.74	0xDD	7.0
0x1E	0.050	0x5E	0.295	0x9E	0.76	0xDE	7.2
0x1F	0.052	0x5F	0.300	0x9F	0.78	0xDF	7.4
0x20	0.054	0x60	0.305	0xA0	0.80	0xE0	7.6
0x21	0.056	0x61	0.310	0xA1	0.82	0xE1	7.8
0x22	0.058	0x62	0.315	0xA2	0.84	0xE2	8.0
0x23	0.060	0x63	0.320	0xA3	0.86	0xE3	8.2
0x24	0.062	0x64	0.325	0xA4	0.88	0xE4	8.4
0x25	0.064	0x65	0.330	0xA5	0.90	0xE5	8.6
0x26	0.066	0x66	0.335	0xA6	0.92	0xE6	8.8
0x27	0.068	0x67	0.340	0xA7	0.94	0xE7	9
0x28	0.070	0x68	0.345	0xA8	0.96	0xE8	9.2

表 7-2. Motor Resistance Look-Up Table (continued)

MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)
0x29	0.072	0x69	0.350	0xA9	0.98	0xE9	9.4
0x2A	0.074	0x6A	0.355	0xAA	1.00	0xEA	9.6
0x2B	0.076	0x6B	0.360	0xAB	1.05	0xEB	9.8
0x2C	0.078	0x6C	0.365	0xAC	1.10	0xEC	10.0
0x2D	0.080	0x6D	0.370	0xAD	1.15	0xED	10.5
0x2E	0.082	0x6E	0.375	0xAE	1.20	0xEE	11.0
0x2F	0.084	0x6F	0.380	0xAF	1.25	0xEF	11.5
0x30	0.086	0x70	0.385	0xB0	1.30	0xF0	12.0
0x31	0.088	0x71	0.390	0xB1	1.35	0xF1	12.5
0x32	0.090	0x72	0.395	0xB2	1.40	0xF2	13.0
0x33	0.092	0x73	0.400	0xB3	1.45	0xF3	13.5
0x34	0.094	0x74	0.405	0xB4	1.50	0xF4	14.0
0x35	0.096	0x75	0.410	0xB5	1.55	0xF5	14.5
0x36	0.098	0x76	0.415	0xB6	1.60	0xF6	15.0
0x37	0.100	0x77	0.420	0xB7	1.65	0xF7	15.5
0x38	0.105	0x78	0.425	0xB8	1.70	0xF8	16.0
0x39	0.110	0x79	0.430	0xB9	1.75	0xF9	16.5
0x3A	0.115	0x7A	0.435	0xBA	1.80	0xFA	17.0
0x3B	0.120	0x7B	0.440	0xBB	1.85	0xFB	17.5
0x3C	0.125	0x7C	0.445	0xBC	1.90	0xFC	18.0
0x3D	0.130	0x7D	0.450	0xBD	1.95	0xFD	18.5
0x3E	0.135	0x7E	0.455	0xBE	2.00	0xFE	19.0
0x3F	0.140	0x7F	0.460	0xBF	2.05	0xFF	20.0

7.3.12.2 Motor Inductance

For a wye-connected motor, the motor phase inductance refers to the inductance from the phase output to the center tap, L_{PH} (denoted as L_{PH} in 図 7-39). For a delta-connected motor, the motor phase inductance refers to the equivalent phase to center tap in the wye configuration in 図 7-39.

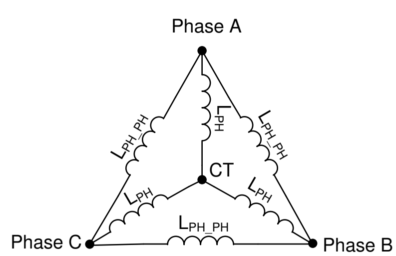

図 7-39. Motor Inductance

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent L_{PH} is to measure the inductance between two phase terminals (L_{PH_PH}), and then divide this value by two, $L_{PH} = ½ L_{PH\_PH}$. In wye-connected motor, if user has access to center tap (CT), L_{PH} can also be measured between center tap (CT) and phase terminal.

Configure the motor inductance (L_{PH}) to a nearest value from 表 7-3.

表 7-3. Motor Inductance Look-Up Table

MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	0.145	0x80	0.465	0xC0	2.1
0x01	0.006	0x41	0.150	0x81	0.470	0xC1	2.2
0x02	0.007	0x42	0.155	0x82	0.475	0xC2	2.3
0x03	0.008	0x43	0.160	0x83	0.480	0xC3	2.4
0x04	0.009	0x44	0.165	0x84	0.485	0xC4	2.5
0x05	0.010	0x45	0.170	0x85	0.490	0xC5	2.6
0x06	0.011	0x46	0.175	0x86	0.495	0xC6	2.7
0x07	0.012	0x47	0.180	0x87	0.50	0xC7	2.8
0x08	0.013	0x48	0.185	0x88	0.51	0xC8	2.9
0x09	0.014	0x49	0.190	0x89	0.52	0xC9	3.0
0x0A	0.015	0x4A	0.195	0x8A	0.53	0xCA	3.2
0x0B	0.016	0x4B	0.200	0x8B	0.54	0xCB	3.4
0x0C	0.017	0x4C	0.205	0x8C	0.55	0xCC	3.6
0x0D	0.018	0x4D	0.210	0x8D	0.56	0xCD	3.8
0x0E	0.019	0x4E	0.215	0x8E	0.57	0xCE	4.0
0x0F	0.020	0x4F	0.220	0x8F	0.58	0xCF	4.2
0x10	0.022	0x50	0.225	0x90	0.59	0xD0	4.4
0x11	0.024	0x51	0.230	0x91	0.60	0xD1	4.6
0x12	0.026	0x52	0.235	0x92	0.61	0xD2	4.8
0x13	0.028	0x53	0.240	0x93	0.62	0xD3	5.0
0x14	0.030	0x54	0.245	0x94	0.63	0xD4	5.2
0x15	0.032	0x55	0.250	0x95	0.64	0xD5	5.4
0x16	0.034	0x56	0.255	0x96	0.65	0xD6	5.6
0x17	0.036	0x57	0.260	0x97	0.66	0xD7	5.8
0x18	0.038	0x58	0.265	0x98	0.67	0xD8	6.0
0x19	0.040	0x59	0.270	0x99	0.68	0xD9	6.2
0x1A	0.042	0x5A	0.275	0x9A	0.69	0xDA	6.4
0x1B	0.044	0x5B	0.280	0x9B	0.70	0xDB	6.6
0x1C	0.046	0x5C	0.285	0x9C	0.72	0xDC	6.8
0x1D	0.048	0x5D	0.290	0x9D	0.74	0xDD	7.0
0x1E	0.050	0x5E	0.295	0x9E	0.76	0xDE	7.2
0x1F	0.052	0x5F	0.300	0x9F	0.78	0xDF	7.4
0x20	0.054	0x60	0.305	0xA0	0.80	0xE0	7.6
0x21	0.056	0x61	0.310	0xA1	0.82	0xE1	7.8
0x22	0.058	0x62	0.315	0xA2	0.84	0xE2	8.0
0x23	0.060	0x63	0.320	0xA3	0.86	0xE3	8.2
0x24	0.062	0x64	0.325	0xA4	0.88	0xE4	8.4
0x25	0.064	0x65	0.330	0xA5	0.90	0xE5	8.6
0x26	0.066	0x66	0.335	0xA6	0.92	0xE6	8.8
0x27	0.068	0x67	0.340	0xA7	0.94	0xE7	9
0x28	0.070	0x68	0.345	0xA8	0.96	0xE8	9.2

表 7-3. Motor Inductance Look-Up Table (continued)

MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)
0x29	0.072	0x69	0.350	0xA9	0.98	0xE9	9.4
0x2A	0.074	0x6A	0.355	0xAA	1.00	0xEA	9.6
0x2B	0.076	0x6B	0.360	0xAB	1.05	0xEB	9.8
0x2C	0.078	0x6C	0.365	0xAC	1.10	0xEC	10.0
0x2D	0.080	0x6D	0.370	0xAD	1.15	0xED	10.5
0x2E	0.082	0x6E	0.375	0xAE	1.20	0xEE	11.0
0x2F	0.084	0x6F	0.380	0xAF	1.25	0xEF	11.5
0x30	0.086	0x70	0.385	0xB0	1.30	0xF0	12.0
0x31	0.088	0x71	0.390	0xB1	1.35	0xF1	12.5
0x32	0.090	0x72	0.395	0xB2	1.40	0xF2	13.0
0x33	0.092	0x73	0.400	0xB3	1.45	0xF3	13.5
0x34	0.094	0x74	0.405	0xB4	1.50	0xF4	14.0
0x35	0.096	0x75	0.410	0xB5	1.55	0xF5	14.5
0x36	0.098	0x76	0.415	0xB6	1.60	0xF6	15.0
0x37	0.100	0x77	0.420	0xB7	1.65	0xF7	15.5
0x38	0.105	0x78	0.425	0xB8	1.70	0xF8	16.0
0x39	0.110	0x79	0.430	0xB9	1.75	0xF9	16.5
0x3A	0.115	0x7A	0.435	0xBA	1.80	0xFA	17.0
0x3B	0.120	0x7B	0.440	0xBB	1.85	0xFB	17.5
0x3C	0.125	0x7C	0.445	0xBC	1.90	0xFC	18.0
0x3D	0.130	0x7D	0.450	0xBD	1.95	0xFD	18.5
0x3E	0.135	0x7E	0.455	0xBE	2.00	0xFE	19.0
0x3F	0.140	0x7F	0.460	0xBF	2.05	0xFF	20.0

7.3.12.3 Motor Back-EMF constant

The back-EMF constant describes the motor phase-to-neutral back-EMF voltage as a function of the motor speed. For a wye-connected motor, the motor BEMF constant refers to the BEMF as a function of time from the phase output to the center tap, Kt_{PH_N} (denoted as Kt_{PH_N} in 図 7-40). For a delta-connected motor, the motor BEMF constant refers to the equivalent phase to center tap in the wye configuration in 図 7-40.

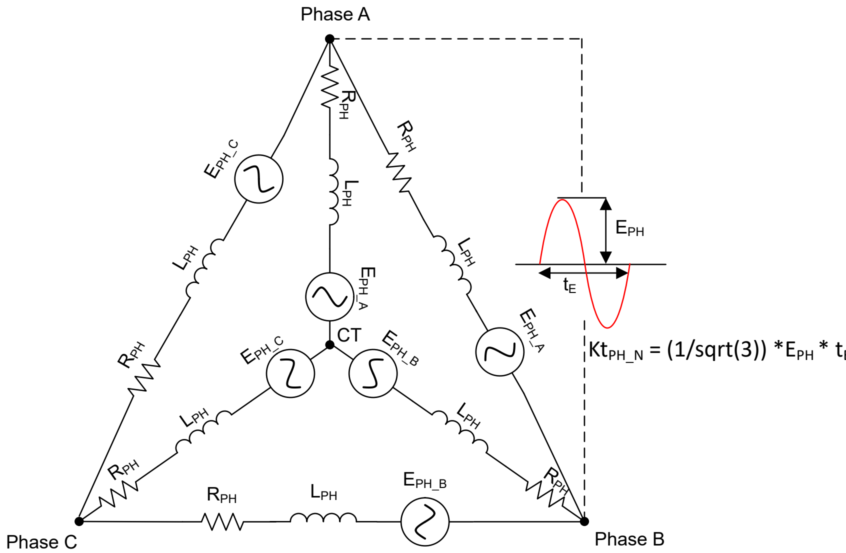

図 7-40. Motor back-EMF constant

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent Kt_{PH_N} is to measure the peak value of BEMF on scope for one electrical cycle between two phase terminals (E_{PH}), and then multiply by time duration of one electrical cycle and in order to convert from phase-to-phase to phase-to-neutral divide by sqrt(3) as shown in 式 5 .

$$Kt_{PH\_N} = {}^{1}\!/\!_{\sqrt{3}} \times E_{PH} \times t_E \quad (5)$$

Configure the motor BEMF constant (Kt_{PH_N}) to a nearest value from 表 7-4.

表 7-4. Motor BEMF constant Look-Up Table

MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	14.5	0x80	46.5	0xC0	210
0x01	0.6	0x41	15.0	0x81	47.0	0xC1	220
0x02	0.7	0x42	15.5	0x82	47.5	0xC2	230
0x03	0.8	0x43	16.0	0x83	48.0	0xC3	240
0x04	0.9	0x44	16.5	0x84	48.5	0xC4	250
0x05	1.0	0x45	17.0	0x85	49.0	0xC5	260
0x06	1.1	0x46	17.5	0x86	49.5	0xC6	270
0x07	1.2	0x47	18.0	0x87	50.0	0xC7	280
0x08	1.3	0x48	18.5	0x88	51	0xC8	290
0x09	1.4	0x49	19.0	0x89	52	0xC9	300
0x0A	1.5	0x4A	19.5	0x8A	53	0xCA	320
0x0B	1.6	0x4B	20.0	0x8B	54	0xCB	340
0x0C	1.7	0x4C	20.5	0x8C	55	0xCC	360
0x0D	1.8	0x4D	21.0	0x8D	56	0xCD	380
0x0E	1.9	0x4E	21.5	0x8E	57	0xCE	400
0x0F	2.0	0x4F	22.0	0x8F	58	0xCF	420

表 7-4. Motor BEMF constant Look-Up Table (continued)

MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)
0x10	2.2	0x50	22.5	0x90	59	0xD0	440
0x11	2.4	0x51	23.0	0x91	60	0xD1	460
0x12	2.6	0x52	23.5	0x92	61	0xD2	480
0x13	2.8	0x53	24.0	0x93	62	0xD3	500
0x14	3.0	0x54	24.5	0x94	63	0xD4	520
0x15	3.2	0x55	25.0	0x95	64	0xD5	540
0x16	3.4	0x56	25.5	0x96	65	0xD6	560
0x17	3.6	0x57	26.0	0x97	66	0xD7	580
0x18	3.8	0x58	26.5	0x98	67	0xD8	600
0x19	4.0	0x59	27.0	0x99	68	0xD9	620
0x1A	4.2	0x5A	27.5	0x9A	69	0xDA	640
0x1B	4.4	0x5B	28.0	0x9B	70	0xDB	660
0x1C	4.6	0x5C	28.5	0x9C	72	0xDC	680
0x1D	4.8	0x5D	29.0	0x9D	74	0xDD	700
0x1E	5.0	0x5E	29.5	0x9E	76	0xDE	720
0x1F	5.2	0x5F	30.0	0x9F	78	0xDF	740
0x20	5.4	0x60	30.5	0xA0	80	0xE0	760
0x21	5.6	0x61	31.0	0xA1	82	0xE1	780
0x22	5.8	0x62	31.5	0xA2	84	0xE2	800
0x23	6.0	0x63	32.0	0xA3	86	0xE3	820
0x24	6.2	0x64	32.5	0xA4	88	0xE4	840
0x25	6.4	0x65	33.0	0xA5	90	0xE5	860
0x26	6.6	0x66	33.5	0xA6	92	0xE6	880
0x27	6.8	0x67	34.0	0xA7	94	0xE7	900
0x28	7.0	0x68	34.5	0xA8	96	0xE8	920
0x29	7.2	0x69	35.0	0xA9	98	0xE9	940
0x2A	7.4	0x6A	35.5	0xAA	100	0xEA	960
0x2B	7.6	0x6B	36.0	0xAB	105	0xEB	980
0x2C	7.8	0x6C	36.5	0xAC	110	0xEC	1000
0x2D	8.0	0x6D	37.0	0xAD	115	0xED	1050
0x2E	8.2	0x6E	37.5	0xAE	120	0xEE	1100
0x2F	8.4	0x6F	38.0	0xAF	125	0xEF	1150
0x30	8.6	0x70	38.5	0xB0	130	0xF0	1200
0x31	8.8	0x71	39.0	0xB1	135	0xF1	1250
0x32	9.0	0x72	39.5	0xB2	140	0xF2	1300
0x33	9.2	0x73	40.0	0xB3	145	0xF3	1350
0x34	9.4	0x74	40.5	0xB4	150	0xF4	1400
0x35	9.6	0x75	41.0	0xB5	155	0xF5	1450
0x36	9.8	0x76	41.5	0xB6	160	0xF6	1500
0x37	10.0	0x77	42.0	0xB7	165	0xF7	1550
0x38	10.5	0x78	42.5	0xB8	170	0xF8	1600
0x39	11.0	0x79	43.0	0xB9	175	0xF9	1650
0x3A	11.5	0x7A	43.5	0xBA	180	0xFA	1700
0x3B	12.0	0x7B	44.0	0xBB	185	0xFB	1750

表 7-4. Motor BEMF constant Look-Up Table (continued)

MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)
0x3C	12.5	0x7C	44.5	0xBC	190	0xFC	1800
0x3D	13.0	0x7D	45.0	0xBD	195	0xFD	1850
0x3E	13.5	0x7E	45.5	0xBE	200	0xFE	1900
0x3F	14.0	0x7F	46.0	0xBF	205	0xFF	2000

7.3.13 Motor Parameter Extraction Tool (MPET)

The MCF8315A uses motor winding resistance, motor winding inductance and Back-EMF constant to estimate motor position in closed loop operation. The MCF8315A has capability of automatically measuring motor parameters in offline state, rather than having the user enter the values themselves. The MPET routine measures motor winding resistance, inductance, back EMF constant and mechanical load inertia and frictional coefficients. Offline measurement of parameters takes place before normal motor operation. TI recommends to estimate the motor parameters before motor startup to minimize the impact caused due to possible parameter variations.

図 7-41 shows the sequence of operation in the MPET routine. The MPET routine is entered when either the MPET_CMD bit is set to 1b or a non-zero target speed is set. The MPET routine consists of four steps namely, IPD, Open Loop Acceleration, Current Ramp Down and Coasting. Each one of these steps are executed if the condition shown below the step evaluates to TRUE; if the condition evaluates to FALSE, the algorithm bypasses that particular step and moves on to the next step in the sequence. Once all the 4 steps are completed (or bypassed), the algorithm exits the MPET routine. If target speed is set to a non-zero value, the algorithm begins the start-up and acceleration sequence (to target speed reference) once MPET routine is exited.

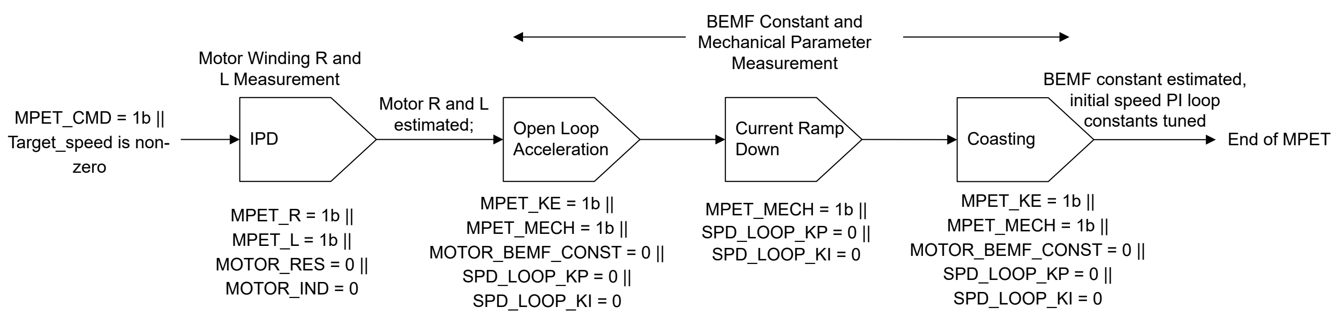

図 7-41. MPET Sequence

TI proprietary MPET routine includes following sequence of operation.

- **IPD**: The MPET routine starts with IPD, if the user enables motor winding resistance or inductance measurement by setting MPET_R = 1b and MPET_L = 1b or if the user defines MOTOR_RES = 0 or MOTOR_IND = 0. The IPD during MPET can be configured using MPET specific configuration parameters or using the normal motor operation IPD configuration parameters. The IPD configuration selection is done using MPET_IPD_SELECT. With MPET_IPD_SELECT = 1b, the IPD current limit is configured using MPET_IPD_CURRENT_LIMIT and the IPD repeat number is configured using MPET_IPD_FREQ. With MPET_IPD_SELECT = 0b, the IPD current limit and the repeat number is configured using IPD_CURR_THR and IPD_REPEAT. The IPD timer over flow or the IPD current decay time more than three times the current ramp up time can result in MPET_IPD_FAULT. TI recommends to run the MPET multiple times to observe for consistent resistance and inductance reading.
- **Open loop Acceleration**:

  After IPD, the MPET routine run align and then open loop acceleration if the back-EMF constant or mechanical parameter measurement are enabled by setting MPET_KE = 1b and MPET_MECH = 1b. The MPET routine incorporates the sequences for mechanical parameter measurement, if the speed loop PI constants are defined as zero, even if MPET_MECH = 0b. User can configure MPET specific open loop configuration parameters or use normal motor operation open loop configuration parameters. The open loop configuration selection is done using MPET_KE_MEAS_PARAMETER_SELECT. With MPET_KE_MEAS_PARAMETER_SELECT = 1b, the speed slew rate is defined using MPET_OPEN_LOOP_SLEW_RATE, the open loop current reference is defined using MPET_OPEN_LOOP_CURR_REF and the open loop speed reference is defined using MPET_OPEN_LOOP_SPEED_REF. With MPET_KE_MEAS_PARAMETER_SELECT = 0b, the speed slew rate is defined using OL_ACC_A1 and OL_ACC_A2, 80% of ILIMIT for current reference and 50% of MAX_SPEED for speed reference.

- **Current Ramp Down**: After open loop acceleration, if the mechanical parameter measurement is enabled, then the MPET routine optimizes the motor current to lower value sufficient to support the load. If mechanical parameter measurement is disabled (MPET_MECH = 0b, or non-zero speed loop PI parameters) then the MPET will not have the current ramp down sequence.
- **Coasting**: MPET routine completes the sequence by allowing the motor to coast by enabling Hi-Z. The motor back EMF and indicative values of mechanical parameters are measured during the motor coasting period. If the motor back EMF is lower than the threshold defined in STAT_DETECT_THR, the MPET_BEMF_FAULT is generated.

Selecting the parameters from EEPROM or MPET

The MPET estimated values are available in the MTR_PARAMS Register. Setting the MPET_WRITE_SHADOW bit to 1, writes the MPET estimated values to the shadow registers and the user-configured (from EEPROM) values in MOTOR_RES, MOTOR_IND, MOTOR_BEMF_CONST, CURR_LOOP_KP, CURR_LOOP_KI, SPD_LOOP_KP and SPD_LOOP_KI shadow registers will be overwritten by the estimated values from MPET. If any of the shadow registers are initialized to zero (from EEPROM registers), the MPET estimated values are used for those registers independent of the MPET_WRITE_SHADOW setting. The MPET calculates the current loop KP and KI by using the measured resistance and inductance. The MPET does an estimation of the mechanical parameters including the inertia and frictional coefficient at the shaft (includes both motor and shaft coupled load). These values are used to set an initial values speed loop KP and KI. The estimated speed loop KP and KI setting can be used as an initial setting only and TI recommends to tune these parameters on application by the user based on the performance requirement.

7.3.14 Anti-Voltage Surge (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive and mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the V_M voltage surges. The AVS feature works to prevent this voltage surge on V_M and can be enabled by setting AVS_EN to 1b. AVS can be disabled by setting AVS_EN to 0b. When AVS is disabled, the deceleration rate is configured through CL_DEC_CONFIG

7.3.15 Output PWM Switching Frequency

The MCF8315A provides the option to configure the output PWM switching frequency of the MOSFETs through PWM_FREQ_OUT. PWM_FREQ_OUT has range of 10-75 kHz. In order to select optimal output PWM switching frequency, user has to make tradeoff between the current ripple and the switching losses. Generally, motors having lower L/R ratio require higher PWM switching frequency to reduce current ripple.

7.3.16 Active Braking

Decelerating the motor quickly requires motor mechanical energy to be extracted and disposed - input DC voltage increases if this energy is returned to the DC input supply. When active braking is enabled, energy taken from DC power supply is used to brake the motor - this prevents DC voltage spike during fast deceleration. The mechanical energy of the motor and energy taken from DC source, both are dissipated within the motor itself. ACTIVE_BRAKE_EN should be set to 1b to enable active braking and avoid DC bus voltage spike during fast motor deceleration. Active braking can also be used during reverse drive (see Reverse Drive) or motor stop (see Active Spin-Down) to reduce the motor speed quickly without DC voltage spike.

The maximum limit on the current sourced from the DC bus (i_{dc_ref}) during active braking can be configured using ACTIVE_BRAKE_CURRENT_LIMIT. The power flow control during active braking is achieved by using both Q-axis (i_q) and D-axis (i_d) components of current. The D-axis current reference (i_{d_ref}) is generated from the error between DC bus current limit (i_{dc_ref}) and the estimated DC bus current (i_{dc}) using a PI controller. The i_{dc} value is estimated from the measured phase currents, phase voltage and DC bus voltage, using power balance equation (equating the instantaneous DC bus power to sum of all three instantaneous phase power assuming 100% efficiency). During active braking, the DC bus current limit (i_{dc_ref}) starts from zero and linearly increases to ACTIVE_BRAKE_CURRENT_LIMIT with current slew rate as defined by ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE. The gain constants of PI controller can be configured using ACTIVE_BRAKE_KP and ACTIVE_BRAKE_KI. 図 7-42 shows the active braking id current control loop.

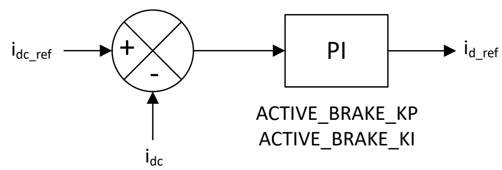

図 7-42. Active Braking Current Control Loop for i_{d_ref}

7.3.17 PWM Modulation Schemes

The MCF8315 supports two different modulation schemes, namely, continuous and discontinuous space vector PWM modulation schemes. In continuous PWM modulation, all the three phases switch all the time as per the defined switching frequency. In discontinuous PWM modulation, one of the phases is clamped to ground for 120° electrical period, and the other two phases are pulse width modulated. The modulation scheme is configured using PWM_MODE. 図 7-43 shows the modulated average phase voltages for different modulation schemes.

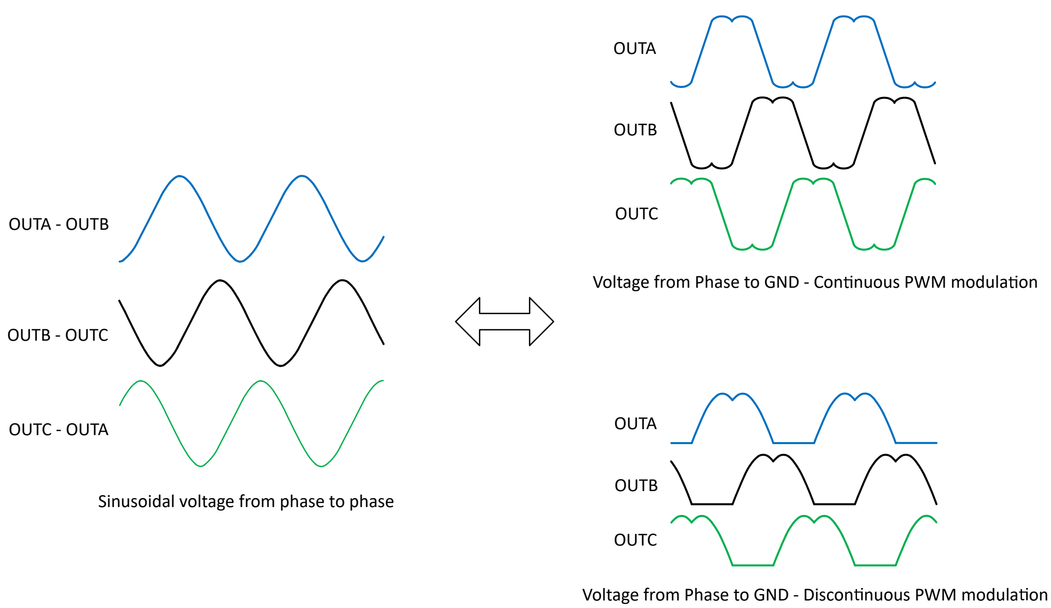

図 7-43. Continuous and Discontinuous PWM Modulation Phase Voltages

Continuous modulation helps in reducing current ripple for motors having low inductance but it results in higher switching losses because all three phases are switching. Discontinuous modulation has lower switching losses due to only two phases switching at a time, but higher current ripple.

7.3.18 Dead Time Compensation

Dead time is inserted between the switching instants of high-side and low-side MOSFET in a half bridge leg to avoid shoot-through condition. Due to dead time insertion, the expected voltage and applied voltage at the phase node differ based on the phase current direction. The phase node voltage distortion introduces undesired distortion in the phase current causing audible noise. The distortion in current waveform due to dead time appear as sixth harmonic of fundamental frequency in the dq reference frame. The MCF8315 integrates a proprietary dead time compensation using a resonant controller to control the sixth harmonic component in phase current to zero, ensuring that the current distortion due to dead time is alleviated. The resonant controller is employed in both i_q and i_d control paths. The dead time compensation can be enabled or disabled by configuring DEADTIME_COMP_EN.

7.3.19 Motor Stop Options

The MCF8315A provides different options for stopping the motor which can be configured by MTR_STOP.

7.3.19.1 Coast (Hi-Z) Mode

Coast (Hi-Z) mode is configured by setting MTR_STOP to 000b. When motor stop command is received, the MCF8315A will transition into a high impedance (Hi-Z) state by turning off all MOSFETs. When the MCF8315A transitions from driving the motor into a Hi-Z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the body diodes in the MOSFET output stage (see example 図 7-44).

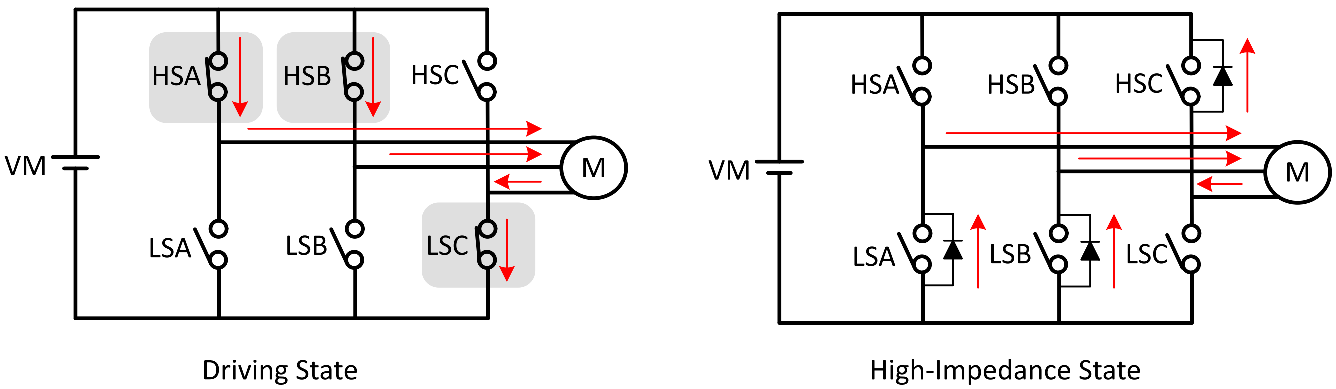

図 7-44. Coast (Hi-Z) Mode

In this example, current is applied to the motor through the high-side phase-A MOSFET (HSA), high-side phase-B MOSFET(HSB) and returned through the low-side phase-C MOSFET (LSC). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs LSA, LSB and HSC.

7.3.19.2 Recirculation Mode

Recirculation mode is configured by setting MTR_STOP to 001b. In order to prevent the inductive energy from returning to DC input supply during motor stop, the MCF8315A allows current to circulate within the MOSFETs by selectively turning OFF some of the active (ON) MOSFETs for a certain time (auto calculated recirculation time to allow the inductive current to decay to zero) before transitioning into Hi-Z by turning OFF the remaining MOSFETs.

Depending on the phase voltage pattern at the time of receiving the stop command, either low-side (see 図 7-45) or high-side recirculation (see 図 7-46) will be used to stop the motor without sending the inductive energy back to the DC input supply.

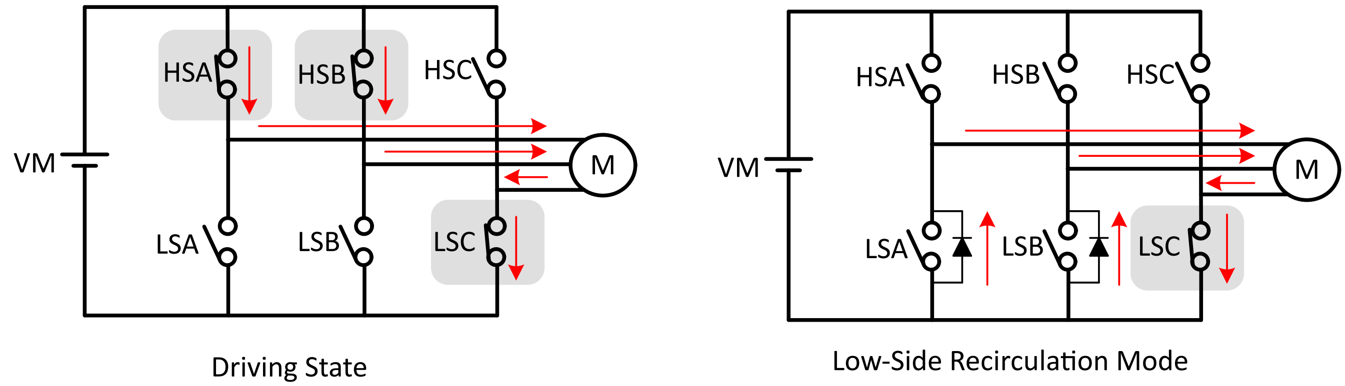

図 7-45. Low-Side Recirculation

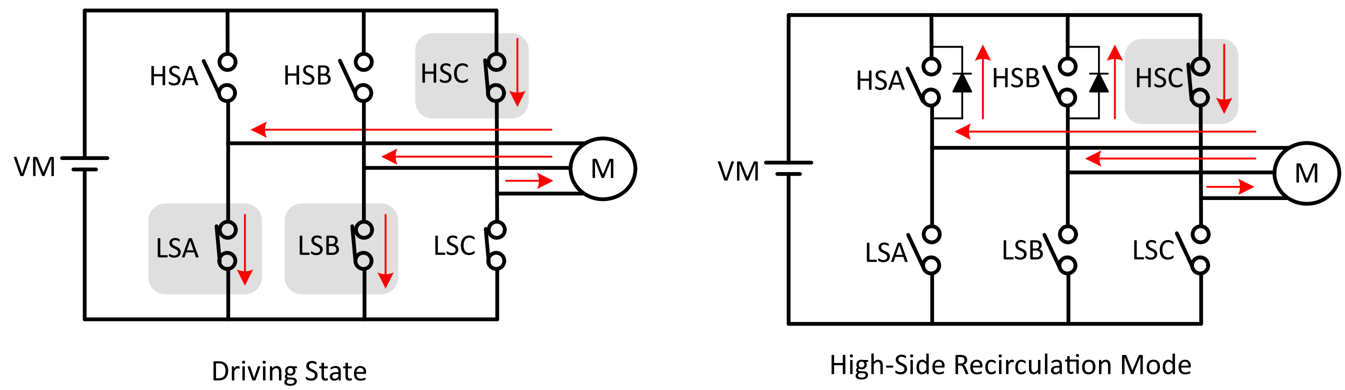

図 7-46. High-Side Recirculation

7.3.19.3 Low-Side Braking

Low-side braking mode is configured by setting MTR_STOP to 010b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all low-side MOSFETs ON (see example 図 7-47) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below BRAKE_SPEED_THRESHOLD prior to receiving stop command, then the MCF8315A transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCF8315A transitions into the Hi-Z state by turning OFF all MOSFETs.

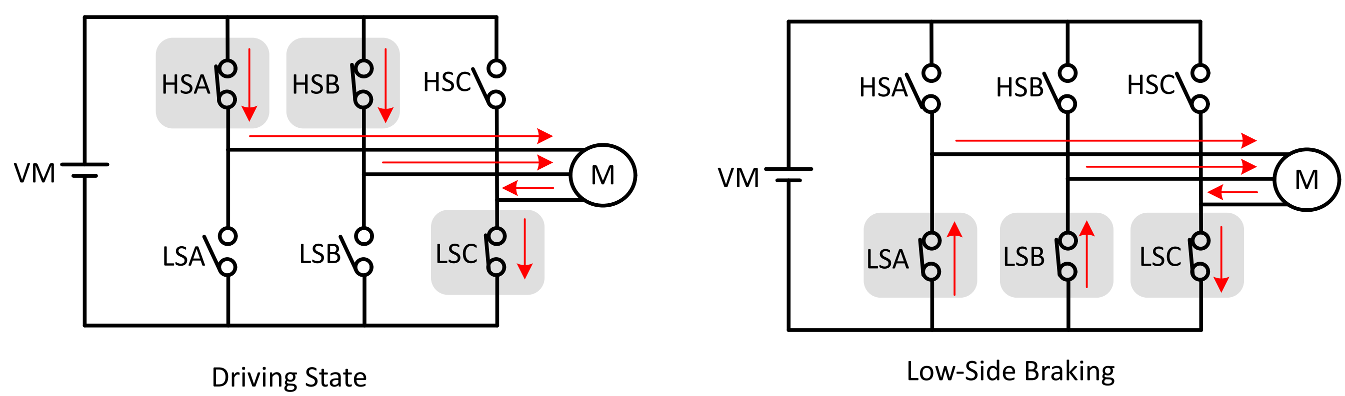

図 7-47. Low-Side Braking

The MCF8315A can also enter low-side braking through BRAKE pin input. When BRAKE pin is pulled to HIGH state, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all low-side MOSFETs ON. In this case, MCF8315A stays in low-side brake state till BRAKE pin changes to LOW state.

7.3.19.4 High-Side Braking

High-side braking mode is configured by setting MTR_STOP to 011b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all high-side MOSFETs ON (see example 図 7-48) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below BRAKE_SPEED_THRESHOLD prior to receiving stop command, then the MCF8315A transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCF8315A transitions into Hi-Z state by turning OFF all MOSFETs.

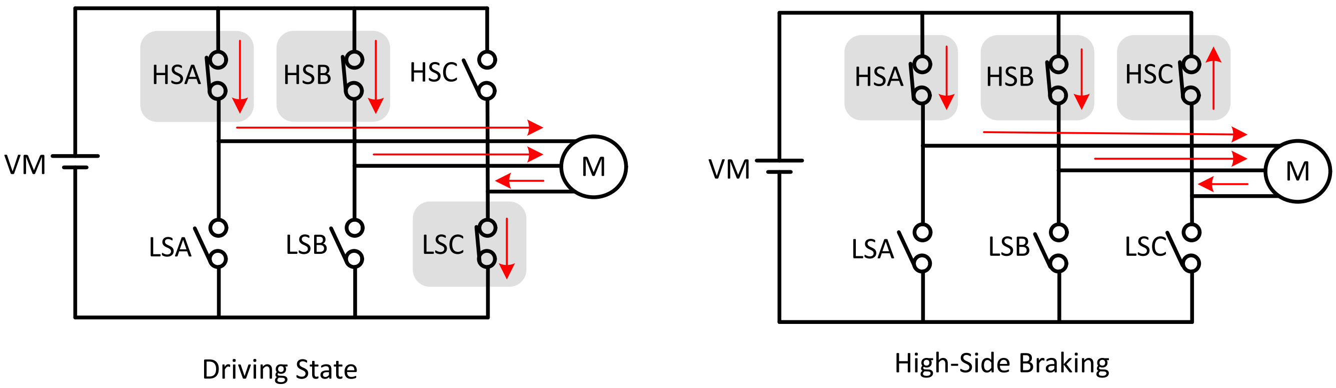

図 7-48. High-Side Braking

7.3.19.5 Active Spin-Down

Active spin down mode is configured by setting MTR_STOP to 100b. When a motor stop command is received, the MCF8315A reduces SPEED_REF to ACT_SPIN_THR and then transitions to Hi-Z state by turning all MOSFETs OFF. The advantage of this mode is that by reducing SPEED_REF, the motor is decelerated to lower speed thereby reducing the phase currents before entering Hi-Z. Now, when the motor transitions into Hi-Z state, the energy transfer to the power supply is reduced. The threshold ACT_SPIN_THR needs to configured high enough for MCF8315A to not lose synchronization with the motor.

7.3.19.6 Align Braking

Align braking based stop mode is configured by setting MTR_STOP to 101b. In this mode, on receiving the motor stop command, MCF8315A reduces the motor speed to a value defined by BRAKE_SPEED_THRSHOLD before bringing the motor to align stop by injecting a DC current through a particular phase pattern for a time configured by MTR_STOP_BRK_TIME. The phase pattern during align stop is generated based on the angle at which align needs to be performed and this angle can be configured through ALIGN_ANGLE or the last commutation angle. ALIGN_BRAKE_ANGLE_SEL can be configured to decide which align angle is to be used by MCF8315A. The current limit threshold during align braking is configured through ALIGN_OR_SLOW_CURRENT LIMIT.

7.3.20 FG Configuration

The MCF8315A provides information about the motor speed through the Frequency Generate (FG) pin. In MCF8315A, the FG pin output is configured through FG_CONFIG. When FG_CONFIG is configured to 0b, the FG output is active as long as the MCF8315A is driving the motor. When FG_CONFIG is configured to 1b, the MCF8315A provides an FG output until the motor back-EMF falls below FG_BEMF_THR.

7.3.20.1 FG Output Frequency

The FG output frequency can be configured by FG_DIV. Many applications require the FG output to provide a pulse for every mechanical rotation of the motor Different FG_DIV configurations can accomplish this for 2-pole up to 30-pole motors.

図 7-49 shows the FG output when MCF8315A has been configured to provide FG pulses once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.

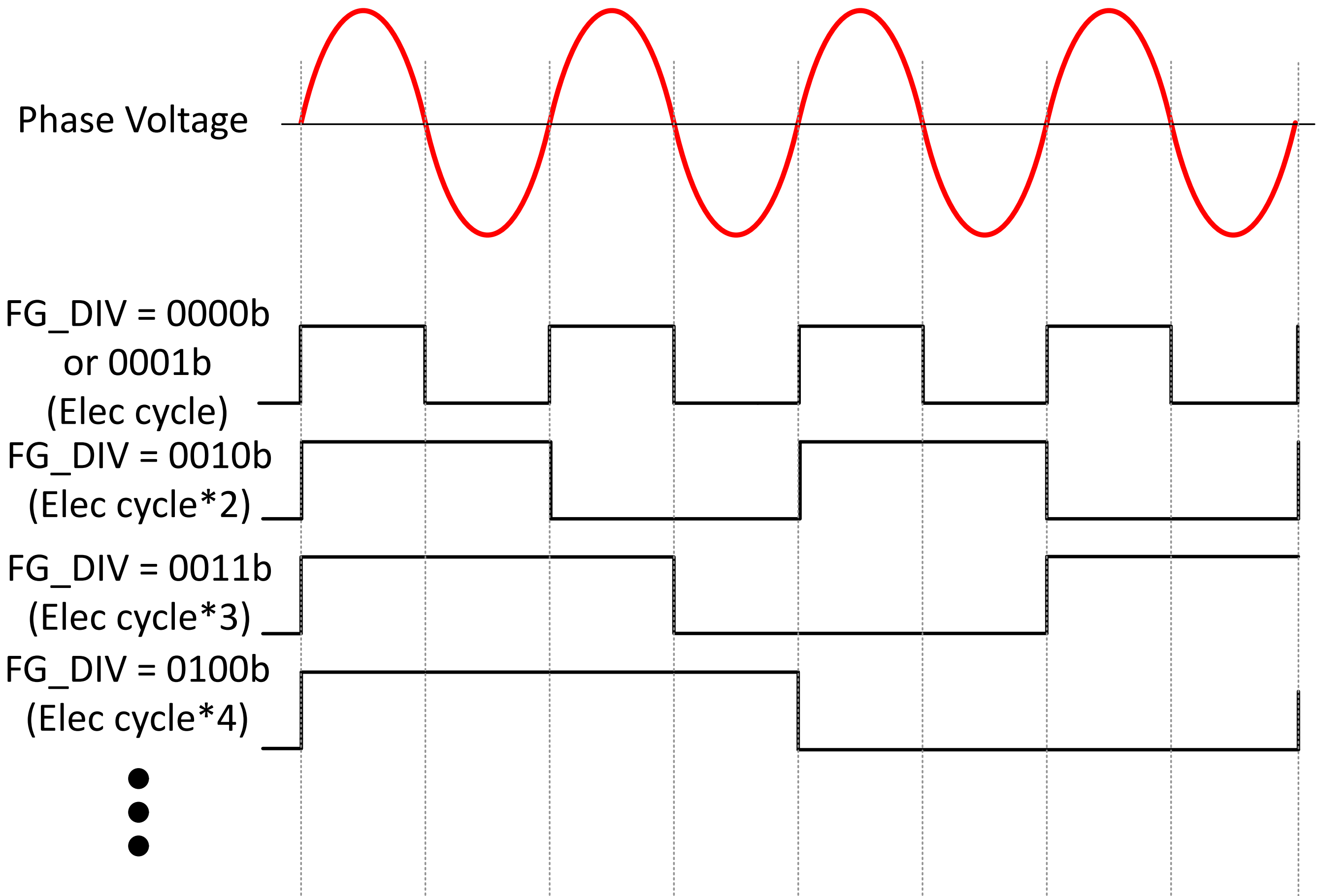

図 7-49. FG Frequency Divider

7.3.20.2 FG Open-Loop and Lock Behavior

During closed loop operation, the driving speed (FG output frequency) and the actual motor speed are synchronized. During open-loop operation, however, FG may not reflect the actual motor speed. During motor-lock condition, the FG output is driven high.

The MCF8315A provides three options for controlling the FG output during open loop, as shown in 図 7-50. The selection of these options is configured through FG_SEL.

If FG_SEL is set to,

- 00b: When in open loop, the FG output is based on the driving frequency.
- 01b: When in open loop, the FG output will be driven high.
- 10b: The FG output will reflect the driving frequency during open loop operation in the first motor start-up cycle after power-on, sleep/standby; FG will be held high during open loop operation in subsequent start-up cycles.

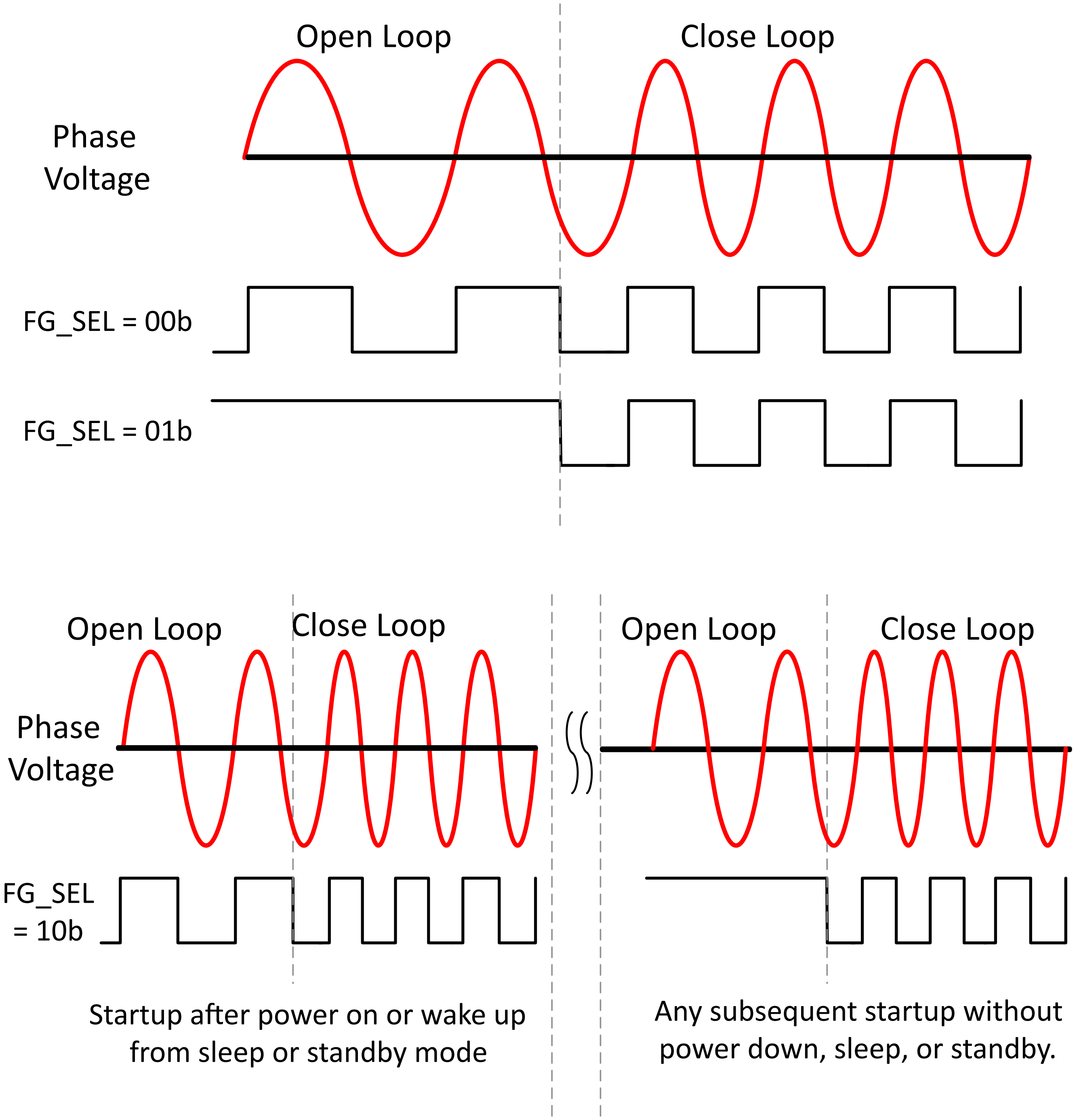

図 7-50. FG Behavior During Open Loop

7.3.21 DC Bus Current Limit

The DC bus current limit feature can be used in applications to limit the current supplied by source without entering the constant current mode. The DC bus current limit feature can be enabled by setting BUS_CURRENT_LIMIT_ENABLE to 1b. The DC bus current limit threshold can be configured using BUS_CURRENT_LIMIT. The DC bus current limit limits the speed reference and a functional diagram is shown in 図 7-51. Enabling this feature may restrict the speed of the motor so that current drawn from source is limited. The algorithm estimates the bus current using the measured phase currents, phase voltage and DC bus voltage. The current limit status is reported on BUS_CURRENT_LIMIT_STATUS.

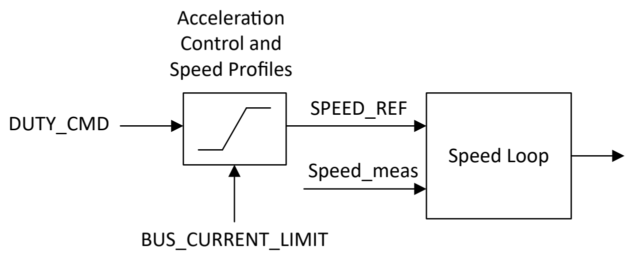

図 7-51. DC Bus Current Limit Functional Block Diagram

7.3.22 Protections

The MCF8315A is protected from a host of fault events including motor lock, VM undervoltage, AVDD undervoltage, buck undervoltage, charge pump undervoltage, overtemperature and overcurrent events. 表 7-5 summarizes the response, recovery modes, power stage status, reporting mechanism for different faults.

注

1. Actionable faults (latched or retry) are always reported on nFAULT pin (as logic low).
2. Actionable faults (latched or retry) are reported on ALARM pin (as logic high) when ALARM_PIN_EN is set to 1b.
3. Report only faults are reported on nFAULT (as logic low) only when ALARM_PIN_EN is set to 0b. When ALARM_PIN_EN is set to 1b, report only faults are reported only on ALARM pin (as logic high) while nFAULT stays high (external pull-up).
4. Priority order for multi-fault scenarios is latched > slower retry time fault > faster retry time fault > report only fault. For example, if a latched and retry fault happen simultaneously, the device stays latched in fault mode until user issues clear fault command by writing 1b to CLR_FLT. If two retry faults with different retry times happen simultaneously, the device retries only after the longer (slower) retry time lapses.
5. Recovery refers only to state of FETs (Hi-Z or active) after the fault condition is removed. Automatic indicates that the device automatically recovers (and FETs are active) when retry time lapses after the fault condition is removed. Latched indicates that the device waits for clearing of fault condition (by writing 1b to CLR_FLT bit) to make the FETs active again.
6. Actionable (latched or retry) faults can take up to 200-ms after fault response (FETs in Hi-Z) to be reported on nFAULT pin (as logic low), ALARM pin (as logic high) and fault status registers.
7. Latched faults can take up to 200-ms after CLR_FLT command is issued (over I^2C) to be cleared.

表 7-5. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	DIGITAL	RECOVERY
VM undervoltage	$V_{VM} < V_{UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO}$
AVDD undervoltage	$V_{AVDD} < V_{AVDD\_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_UV}$
Buck undervoltage (BUCK_UV)	$V_{FB\_BK} < V_{BK\_UV}$	—	—	Active/Hi-Z	Active/Disabled	Automatic: $V_{FB\_BK} > V_{BK\_UV}$
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPUV}$	—	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$
Over Voltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_EN = 0b	None	Active	Active	No action
		OVP_EN = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$

表 7-5. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	DIGITAL	RECOVERY
Over Current Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		OCP_MODE = 01b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Active	Active	No action
		OCP_MODE = 11b	None	Active	Active	No action
Buck Overcurrent Protection (BUCK_OCP)	$I_{BK} > I_{BK\_OCP}$	—	—	Hi-Z	Disabled	Automatic
Motor Lock (MTR_LCK)	Motor lock: Abnormal Speed; No Motor Lock; Abnormal BEMF	MTR_LCK_MODE = 0000b or 0001b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	High side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0011b	nFAULT and CONTROLLER_FAULT_STATUS register	Low side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0100b or 0101b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0110b	nFAULT and CONTROLLER_FAULT_STATUS register	High side brake	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0111b	nFAULT and CONTROLLER_FAULT_STATUS register	Low side brake	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 1000b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		MTR_LCK_MODE = 1xx1b	None	Active	Active	No action

表 7-5. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	DIGITAL	RECOVERY
Hardware Lock-Detection Current Limit (HW_LOCK_LIMIT)	V_{SOX} > HW_LOCK_ILIMIT	HW_LOCK_ILIMIT_MODE = 0000b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 0011b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 0100b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MODE = 0110b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MODE = 0111b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MODE= 1000b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		HW_LOCK_ILIMIT_MODE = 1xx1b	None	Active	Active	No action
Software Lock-Detection Current Limit (LOCK_LIMIT)	V_{SOX} > LOCK_ILIMIT	LOCK_ILIMIT_MODE = 0000b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0011b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0100b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0110b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0111b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE= 1000b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		LOCK_ILIMIT_MODE = 1xx1b	None	Active	Active	No action
IPD Timeout Fault (IPD_T1_FAULT and IPD_T2_FAULT)	IPD TIME > 500ms (approx.), during IPD current ramp up or ramp down	IPD_TIMEOUT_FAULT_EN = 0b	—	Active	Active	No action
		IPD_TIMEOUT_FAULT_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
IPD Frequency Fault (IPD_FREQ_FAULT)	IPD pulse before the current decay in previous IPD pulse	IPD_FREQ_FAULT_EN = 0b	—	Active	Active	No action
		IPD_FREQ_FAULT_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}

表 7-5. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	DIGITAL	RECOVERY
MPET IPD Fault (MPET_IPD_FAULT)	Same as IPD Timeout Fault.	MPET_CMD = 1b or MPET_R or MPET_L = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
MPET Back-EMF Fault (MPET_BEMF_FAULT)	Motor Back EMF < STAT_DETECT_THR	MPET_CMD = 1b or MPET_KE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
Maximum VM (overvoltage) fault	V_{VM} > MAX_VM_MOTOR, if MAX_VM_MOTOR ≠ 000b	MAX_VM_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		MAX_VM_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Automatic: (V_{VM} < MAX_VM_MOTOR - 1)-V
Minimum VM (undervoltage) fault	V_{VM} < MIN_VM_MOTOR, if MIN_VM_MOTOR ≠ 000b	MIN_VM_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		MIN_VM_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Automatic: (V_{VM} > MIN_VM_MOTOR + 0.5)-V
External Watchdog	Watchdog tickle does not arrive before configured time interval when EXT_WDT_EN =1b. Refer セクション 7.5.5	EXT_WDT_FAULT_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		EXT_WDT_FAULT_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
Bus Current Limit	I_{VM} > BUS_CURRENT_LIMIT. Refer セクション 7.3.21	BUS_CURRENT_LIMIT_ENABLE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed will be restricted to limit DC bus current	Active	Automatic: Speed restriction is removed when I_{VM} < BUS_CURRENT_LIMIT
Current Loop Saturation	Indication of current loop saturation due to lower V_{VM}	SATURATION_FLAGS_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed may not reach speed reference	Active	Automatic: motor will reach reference operating point upon exiting saturation
Speed Loop Saturation	Indication of speed loop saturation due to lower V_{VM}, lower ILIMIT setting etc.,	SATURATION_FLAGS_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed may not reach speed reference	Active	Automatic: motor will reach reference operating point upon exiting saturation
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	—	Active	Active	No action
		OTW_REP = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Active	Active	Automatic: $T_J < T_{OTW} - T_{OTW\_HYS}$
Thermal shutdown (TSD)	$T_J > T_{TSD}$	—	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Automatic: $T_J < T_{TSD} - T_{TSD\_HYS}$

7.3.22.1 VM Supply Undervoltage Lockout

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all the integrated FETs, driver charge-pump and digital logic are disabled as shown in 図 7-52. MCF8315A goes into reset state whenever VM UVLO event occurs.

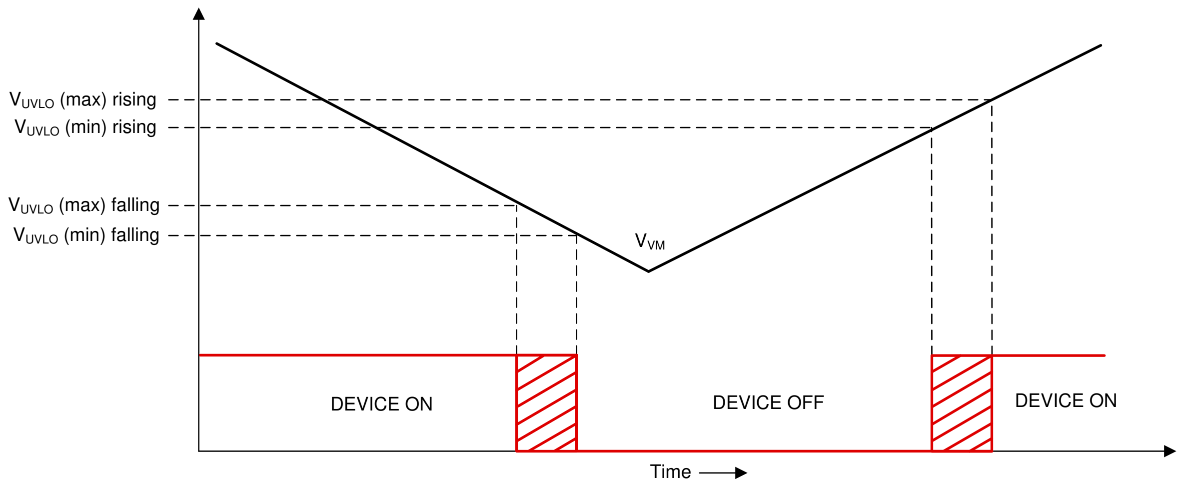

図 7-52. VM Supply Undervoltage Lockout

7.3.22.2 AVDD Undervoltage Lockout (AVDD_UV)

If at any time the voltage on the AVDD pin falls lower than the V_{AVDD_UV} threshold, all the integrated FETs, driver charge-pump and digital logic controller are disabled. Since internal circuitry in MCF8315A is powered through the AVDD regulator, MCF8315A goes into reset state whenever AVDD UV event occurs.

7.3.22.3 BUCK Undervoltage Lockout (BUCK_UV)

If at any time the input supply voltage on the FB_BK pin falls lower than the V_{BK_UVLO} threshold, both the high-side and low-side MOSFETs of the buck regulator are disabled . Since internal circuitry in MCF8315A is powered through the buck regulator, MCF8315A goes into reset state whenever buck UV event occurs.

7.3.22.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT and VCP_UV bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The VCP_UV bit stays set until cleared through the CLR_FLT bit.

7.3.22.5 Overvoltage Protection (OVP)

If at any time input supply voltage on the VM pins rises higher than V_{OVP}, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT and OVP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR_FLT bit. Setting the OVP_EN to 0b disables this protection feature.

The OVP threshold can be set to 22-V or 34-V based on the OVP_SEL bit.

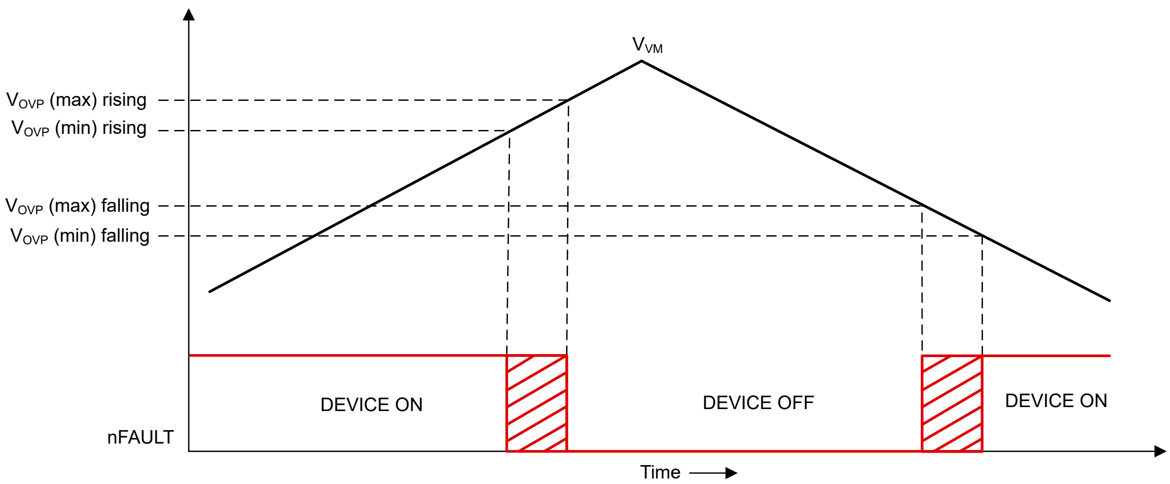

図 7-53. Over Voltage Protection

7.3.22.6 Overcurrent Protection (OCP)

MOSFET overcurrent event is sensed by monitoring the current flowing through the FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the deglitch time t_{OCP}, an OCP event is recognized and action is taken according to OCP_MODE. The I_{OCP} threshold is set through the OCP_LVL, t_{OCP} is set through OCP_DEG and the OCP_MODE can be configured in four different modes: latched shutdown, automatic retry, report only and disabled.

7.3.22.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

When an OCP event happens in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear fault command is issued through the CLR_FLT bit.

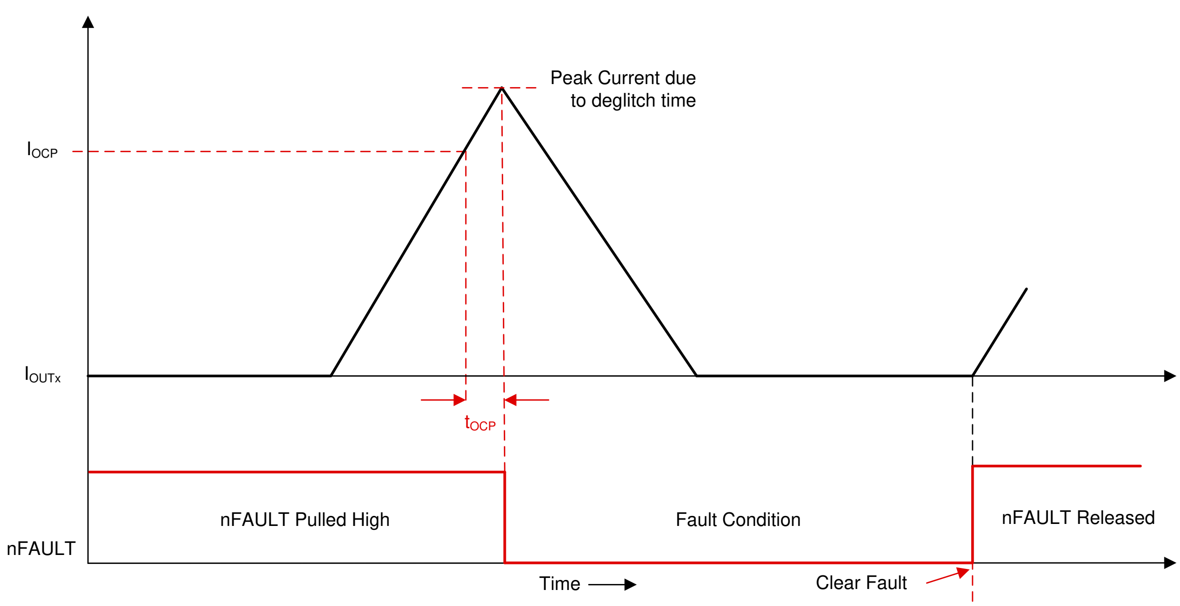

図 7-54. Overcurrent Protection - Latched Shutdown Mode

7.3.22.6.2 OCP Automatic Retry (OCP_MODE = 01b)

When an OCP event happens in this mode, all the FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} (TRETRY) time elapses. The DRIVER_FAULT bit is reset to 0b after the t_{RETRY} period expires. The OCP and corresponding FET's OCP bits are set to 1b until cleared through the CLR_FLT bit.

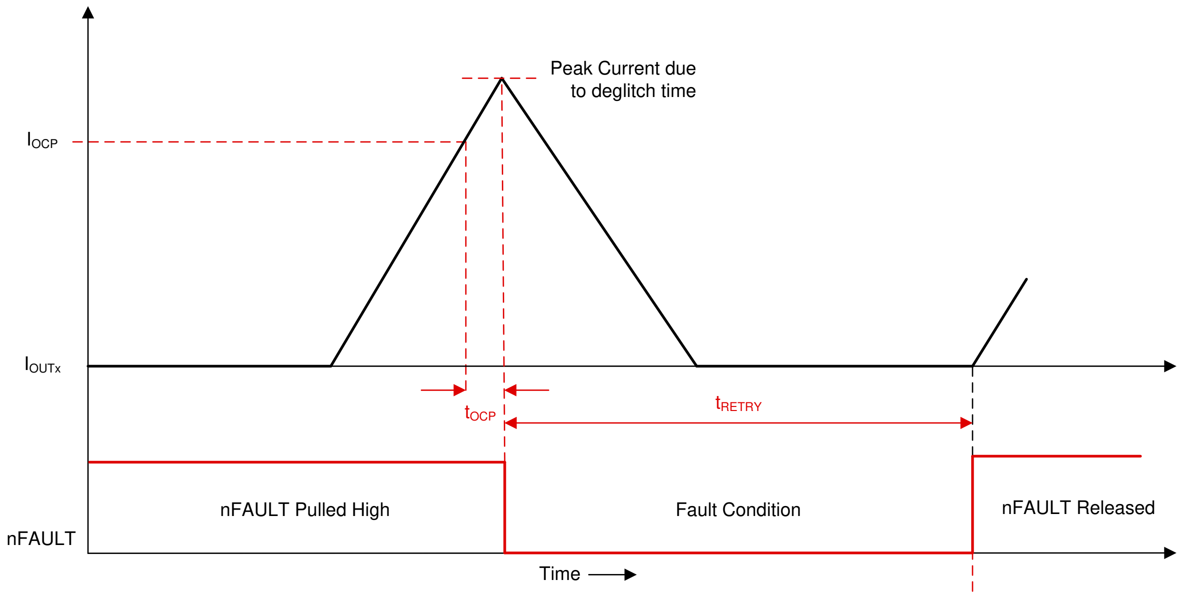

図 7-55. Overcurrent Protection - Automatic Retry Mode

7.3.22.6.3 OCP Report Only (OCP_MODE = 10b)

No protective action is taken when an OCP event happens in this mode. The overcurrent event is reported by setting the DRIVER_FAULT, OCP, and corresponding FET's OCP bits to 1b in the fault status registers. The device continues to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears when the OCP condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.22.6.4 OCP Disabled (OCP_MODE = 11b)

No action is taken when an OCP event happens in this mode.

7.3.22.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current through the high-side MOSFET exceeds the I_{BK_OCP} threshold for a time longer than the deglitch time (t_{OCP}), a buck OCP event is recognized and the buck regulator MOSFETs are disabled (Hi-Z). MCF8315A goes into reset state whenever buck OCP event occurs, since the internal circuitry in MCF8315A is powered from the buck regulator output.

7.3.22.8 Hardware Lock Detection Current Limit (HW_LOCK_ILIMIT)

The hardware lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The output of current sense amplifier is connected to hardware comparator. If at any time, the voltage on the output of CSA exceeds HW_LOCK_ILIMIT threshold for a time longer than $t_{HW\_LOCK\_ILIMIT}$, a HW_LOCK_ILIMIT event is recognized and action is taken according to the HW_LOCK_ILIMIT_MODE. The threshold is set through HW_LOCK_ILIMIT, the $t_{HW\_LCK\_ILIMIT}$ is set through the HW_LOCK_ILIMIT_DEG. HW_LOCK_ILIMIT_MODE bit can operate in four different modes: HW_LOCK_ILIMIT latched shutdown, HW_LOCK_ILIMIT automatic retry, HW_LOCK_ILIMIT report only, and HW_LOCK_ILIMIT disabled.

7.3.22.8.1 HW_LOCK_ILIMIT Latched Shutdown (HW_LOCK_ILIMIT_MODE = 00xxb)

When a HW_LOCK_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW_LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFETs during HW_LOCK_ILIMIT:

- HW_ LOCK_ILIMIT_MODE = 0000b: All MOSFETs are turned OFF.
- HW_ LOCK_ILIMIT_MODE = 0001b: Some of the MOSFETs which are switching are turned OFF while the rest stay ON till inductive energy is completely recirculated.
- HW_LOCK_ILIMIT_MODE = 0010b: All-high side MOSFETs are turned ON.
- HW_LOCK_ILIMIT_MODE = 0011b: All-low side MOSFETs are turned ON.

The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the HW_LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.22.8.2 HW_LOCK_ILIMIT Automatic recovery (HW_LOCK_ILIMIT_MODE = 01xxb)

When a HW_LOCK_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW_LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFET during HW_LOCK_ILIMIT:

- HW_LOCK_ILIMIT_MODE = 0100b: All MOSFETs are turned OFF.
- HW_LOCK_ILIMIT_MODE = 0101b: Some of the MOSFETs which are switching are turned OFF while the rest stay ON till inductive energy is completely recirculated.
- HW_LOCK_ILIMIT_MODE = 0110b: All high-side MOSFETs are turned ON
- HW_LOCK_ILIMIT_MODE = 0111b: All low-side MOSFETs are turned ON

The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are reset to 0b after the t_{LCK_RETRY} period expires.

7.3.22.8.3 HW_LOCK_ILIMIT Report Only (HW_LOCK_ILIMIT_MODE = 1000b)

No protective action is taken when a HW_ LOCK_ILIMIT event happens in this mode. The hardware lock detection current limit event is reported by setting the CONTROLLER_FAULT and HW_LOCK_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the HW_LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.22.8.4 HW_LOCK_ILIMIT Disabled (HW_LOCK_ILIMIT_MODE= 1xx1b)

No action is taken when a HW_LOCK_ILIMIT event happens in this mode.

7.3.22.9 Thermal Warning (OTW)

If the die temperature exceeds the thermal warning limit (T_{OTW}), nFAULT is pulled low and the OT and OTW bits in the gate driver status register are set to 1b. The reporting of OTW (on nFAULT and status bits) can be enabled by setting OTW_REP to 1b. The device performs no additional action and continues to function. In this case, the nFAULT pin is released when the die temperature decreases below the hysteresis point of the thermal warning limit (T_{OTW} - T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit and the die temperature is lower than thermal warning limit. (T_{OTW} - T_{OTW_HYS}).

7.3.22.10 Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown limit (T_{TSD}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the DRIVER_FAULT, OT and OTS bit in the status register are set to 1b. Normal operation resumes (driver operation and the nFAULT pin is released) when the die temperature decreases below the hysteresis point of the thermal shutdown limit (T_{TSD} - T_{TSD_HYS}). The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

7.3.22.11 Motor Lock (MTR_LCK)

The MCF8315A continuously checks for different motor lock conditions (see Motor Lock Detection) during motor operation. When one of the enabled lock condition happens, a MTR_LCK event is recognized and action is taken according to the MTR_LCK_MODE.

All locks can be enabled or disabled individually and retry times can be configured through LCK_RETRY. MTR_LCK_MODE bit can operate in four different modes: MTR_LCK latched shutdown, MTR_LCK automatic retry, MTR_LCK report only and MTR_LCK disabled.

7.3.22.11.1 MTR_LCK Latched Shutdown (MTR_LCK_MODE = 00xxb)

When a MTR_LCK event happens in this mode, the status of MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 0000b: All MOSFETs are turned OFF.
- MTR_LCK_MODE = 0001b: Some of the MOSFETs which are switching are turned OFF while the rest stay ON till inductive energy is completely recirculated.
- MTR_LCK_MODE = 0010b: All high-side MOSFETs are turned ON.
- MTR_LCK_MODE = 0011b: All low-side MOSFETs are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.22.11.2 MTR_LCK Automatic Recovery (MTR_LCK_MODE= 01xxb)

When a MTR_LCK event happens in this mode, the status of MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 0100b: All MOSFETs are turned OFF.
- MTR_LCK_MODE = 0101b: Some of the MOSFETs which are switching are turned OFF while the rest stay ON till inductive energy is completely recirculated.
- MTR_LCK_MODE = 0110b: All high-side MOSFETs are turned ON.
- MTR_LCK_MODE = 0111b: All low-side MOSFETs are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are reset to 0b after the t_{LCK_RETRY} period expires.

7.3.22.11.3 MTR_LCK Report Only (MTR_LCK_MODE = 1000b)

No protective action is taken when a MTR_LCK event happens in this mode. The motor lock event is reported by setting the CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.22.11.4 MTR_LCK Disabled (MTR_LCK_MODE = 1xx1b)

No action is taken when a MTR_LCK event happens in this mode.

7.3.22.12 Motor Lock Detection

The MCF8315A provides different lock detect mechanisms to determine if the motor is in a locked state. Multiple detection mechanisms work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCF8315A can also identify and take action if there is no motor connected to the system. Each of the lock detect mechanisms and the no-motor detection can be disabled by their respective register bits (LOCK1/2/3_EN).

7.3.22.12.1 Lock 1: Abnormal Speed (ABN_SPEED)

MCF8315A monitors the speed continuously and at any time the speed exceeds LOCK_ABN_SPEED, an ABN_SPEED lock event is recognized and action is taken according to the MTR_LCK_MODE. The threshold is set through the LOCK_ABN_SPEED register. ABN_SPEED lock can be enabled/disabled by LOCK1_EN.

7.3.22.12.2 Lock 2: Abnormal BEMF (ABN_BEMF)

MCF8315A estimates back-EMF in order to run motor optimally in closed loop. This estimated back-EMF is compared against the expected back-EMF calculated using the estimated speed and the BEMF constant. Whenever motor is stalled the estimated back-EMF is inaccurate due to lower back-EMF at low speed. When the difference between estimated and expected back-EMF exceeds ABNORMAL_BEMF_THR, an abnormal BEMF fault is triggered and action is taken according to the MTR_LCK_MODE.

ABN_BEMF lock can be enabled/disabled by LOCK2_EN.

7.3.22.12.3 Lock3: No-Motor Fault (NO_MTR)

The MCF8315A continuously monitors phase currents on all three phases; if any phase current stays below NO_MTR_THR for 500ms, a NO_MTR event is recognized. The response to the NO_MTR event is configured through MTR_LCK_MODE. NO_MTR lock can be enabled/disabled by LOCK3_EN.

7.3.22.13 MPET Faults

An error during resistance and inductance measurement is reported using MPET_IPD_FAULT. The MPET_IPD_FAULT gets triggered when the IPD timer overflows due to unsuccessful attempt to ramp up the current to the threshold value, same as explained in セクション 7.3.22.14. The fault typically gets triggered when there is no motor connected to MCF8315 or when the MPET IPD current threshold is set high for motors with high resistance.

An error during BEMF constant measurement is reported using MPET_BEMF_FAULT. This fault gets triggered when the measured back EMF is less than the threshold set in STAT_DETECT_THR. One example of such fault scenario can be the motor stall while running in open loop due to incorrect open loop configuration used.

7.3.22.14 IPD Faults

The MCF8315A uses 12-bit timers to estimate the time during the current ramp up and ramp down during IPD, when the motor start-up is configured as IPD (MTR_STARTUP is set to 10b). During IPD, the algorithm checks for a successful current ramp-up to IPD_CURR_THR, starting with an IPD clock of 10MHz; if unsuccessful (timer overflow before current reaches IPD_CURR_THR), IPD is repeated with lower frequency clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD_CURR_THR) with all the four clock frequencies, then the IPD_T1_FAULT gets triggered. Similarly the algorithm checks for a successful current decay to zero during IPD current ramp down using all the mentioned IPD clock frequencies. If the IPD timer overflows (current does not ramp down to zero) in all the four attempts, then the IPD_T2_FAULT gets triggered. The user can enable IPD timeout (IPD timer overflow) by setting IPD_TIMEOUT_FAULT_EN to 1b.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCF8315A can generate a fault called IPD_FREQ_FAULT during such a scenario by setting IPD_FREQ_FAULT_EN to 1b. The IPD_FREQ_FAULT maybe triggered if the IPD frequency is too high for the IPD current limit and the IPD release mode or if the motor inductance is too high for the IPD frequency, IPD current limit and IPD release mode.

7.4 Device Functional Modes

7.4.1 Functional Modes

7.4.1.1 Sleep Mode

In sleep mode, the MOSFETs, sense amplifiers, buck regulator, charge pump, AVDD LDO regulator and the I^2C bus are disabled. The device can be configured to enter sleep (instead of standby) mode by configuring DEV_MODE to 1b. SPEED pin and I^2C speed command determine entry and exit from sleep state as described in 表 7-6.

7.4.1.2 Standby Mode

The device can be configured to operate as a standby device by setting DEV_MODE to 0b. In standby mode, the charge pump, AVDD LDO, buck regulator and I^2C bus are active while the motor is in stopped state waiting for a suitable non-zero speed command. SPEED pin (analog, PWM or frequency based speed input) or I^2C speed command (I^2C based speed input) determines entry and exit from standby state as described in 表 7-6.

The thresholds for entering and exiting standby mode in different speed input modes are as follows,

1. Analog : V_{EN_SB/EX_SB} = (1% x V_{ANA_FS}) if DUTY_HYST ≤ 10b, V_{EN_SB/EX_SB} = (2% x V_{ANA_FS}) if DUTY_HYST =11b
2. PWM : $Duty_{EN\_SB/EX\_SB}$ = 1% if DUTY_HYST ≤ 10b, $Duty_{EN\_SB/EX\_SB}$ = 2% if DUTY_HYST =11b
3. I^2C : $SPEED\_CTRL_{EN\_SBEX\_SB}$ = 328 if DUTY_HYST ≤ 10b, $SPEED\_CTRL_{EN\_SB/EX\_SB}$ = 656 if DUTY_HYST =11b
4. Frequency : $Freq_{EN\_SB/EX\_SB}$ = 1% x INPUT_MAXIMUM_FREQ if DUTY_HYST ≤ 10b, $Freq_{EN\_SB/EX\_SB}$ = 2% x INPUT_MAXIMUM_FREQ if DUTY_HYST = 11b

表 7-6. Conditions to Enter or Exit Sleep or Standby Modes

SPEED COMMAND MODE	ENTER STANDBY CONDITION	EXIT FROM STANDBY CONDITION	ENTER SLEEP CONDITION	EXIT FROM SLEEP CONDITION
Analog	$V_{SPEED} < V_{EN\_SB}$	$V_{SPEED} > V_{EX\_SB}$	Not Available	Not Available
PWM	$Duty_{SPEED} < Duty_{EN\_SB}$	$Duty_{SPEED} > Duty_{EX\_SB}$	Not Available	Not Available
I^2C	DIGITAL_SPEED_CTRL < $DIGITAL\_SPEED\_CTRL_{EN\_SB}$	DIGITAL_SPEED_CTRL > $DIGITAL\_SPEED\_CTRL_{EX\_SB}$	DIGITAL_SPEED_CTRL is set to 0b for SLEEP_ENTRY_TIME and $V_{SPEED} < V_{IL}$	$V_{SPEED} > V_{IH}$ for t_{DET_PWM}
Frequency	$Freq_{SPEED} < Freq_{EN\_SB}$	$Freq_{SPEED} > Freq_{EX\_SB}$	Not Available	Not Available

注

V_{SPEED} : SPEED pin input voltage, $Duty_{SPEED}$: SPEED pin input PWM duty, $Freq_{SPEED}$: SPEED pin input frequency

7.4.1.3 Fault Reset (CLR_FLT)

In the case of latched faults, the device goes into a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR_FLT to 1b.

7.5 External Interface

7.5.1 DRVOFF Functionality

When DRVOFF pin is driven high, all six MOSFETs are put in Hi-Z state, irrespective of speed command. If motor speed command is non-zero when DRVOFF is driven high, device may encounter a fault like no motor or abnormal BEMF.

7.5.2 DAC outputs

MCF8315A has two 12-bit DACs which output analog voltage equivalent of digital variables on the DACOUT1 and DACOUT2 pins. The maximum DAC output voltage is 3-V. Signals available on DACOUT pins are useful in tracking internal variables in real-time and can be used for tuning speed controller or motor acceleration time. The address for variables to be tracked on DACOUT1 and DACOUT2 are configured using DACOUT1_VAR_ADDR and DACOUT2_VAR_ADDR respectively. DACOUT1 is available on pin 36 and DACOUT2 can be configured on pin 38 by setting PIN_38_CONFIG to 00b. DACOUT2 is also available on pin 37. PIN_36_37_CONFIG should be configured to 1b for pins 36, 37 to function as DAC outputs.

7.5.3 Current Sense Output

MCF8315A can provide the built-in current sense amplifiers' output on the SOX pin. SOX output is available on pin 38 and can be configured by PIN_38_CONFIG.

7.5.4 Oscillator Source

MCF8315A has a built-in oscillator that is used as the clock source for all digital peripherals and timing measurements. Default configuration for MCF8315A is to use the internal oscillator and it is sufficient to drive the motor without need for any external crystal or clock sources.

In case MCF8315A does not meet accuracy requirements of timing measurement or speed loop, then MCF8315A has an option to support an external clock reference.

In order to improve EMI performance, MCF8315A provides the option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SPREAD_SPECTRUM_MODULATION_DIS.

7.5.4.1 External Clock Source

Speed loop accuracy of MCF8315A over the operating temperature range can be improved by providing a more accurate clock reference on EXT_CLK pin as shown in 図 7-56. EXT_CLK will be used to calibrate the internal clock oscillator - this will help match the accuracy of the internal clock oscillator to that of the external clock. External clock source can be selected by configuring CLK_SEL to 11b and setting EXT_CLK_EN to 1b. The external clock source frequency can be configured through EXT_CLK_CONFIG.

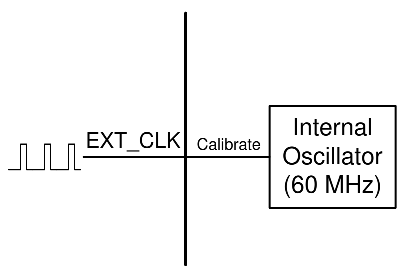

図 7-56. External Clock Reference

注

External clock is optional and can be used when higher clock accuracy is needed. MCF8315A will always power up using the internal oscillator in all modes.

7.5.5 External Watchdog

MCF8315A provides an external watchdog feature - EXT_WDT_EN bit should be set to 1b to enable the external watchdog. When this feature is enabled, the device waits for a tickle (low to high transition in EXT_WD pin, WATCHDOG_TICKLE set to 1b in I^2C mode) from the external watchdog input for a configured time interval; if the time interval between two consecutive tickles is higher than the configured time, a watchdog fault is triggered. This fault can be configured using EXT_WDT_FAULT_MODE either as a report only fault or as a latched fault with outputs in Hi-Z state. The latched fault can be cleared by writing 1b to CLR_FLT. When a watchdog timeout occurs, WATCHDOG_FAULT bit is set to 1b. In case, the next tickle arrives before the configured time interval elapses, the watchdog timer is reset and it begins to wait for the next tickle. This can be used to continuously monitor the health of an external MCU (which is the external watchdog input) and put the MCF8315A outputs in Hi-Z in case the external MCU is in an erroneous state.

The external watchdog input is selected using EXT_WDT_INPUT_MODE and can either be the EXT_WD pin or the I^2C interface. The time interval between two tickles to trigger a watchdog fault is configured by EXT_WDT_CONFIG; there are 4 time settings - 100, 200, 500 and 1000ms for the EXT_WD pin based watchdog and 4 time settings - 1, 2, 5 and 10s for the I^2C based watchdog.

注

Watchdog should be disabled by setting EXT_WDT_EN to 0b before changing EXT_WDT_CONFIG configuration.

7.6 EEPROM access and I2C interface

7.6.1 EEPROM Access

MCF8315A has 1024 bits (16 rows of 64 bits each) of EEPROM, which are used to store the motor configuration parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit write and read operations are supported. EEPROM can be written and read using the I2C serial interface but erase cannot be performed using I2C serial interface. The shadow registers corresponding to the EEPROM are located at addresses 0x000080-0x0000AE.

注

MCF8315A allows EEPROM write and read operations only when the motor is not spinning.

7.6.1.1 EEPROM Write

In MCF8315A, EEPROM write procedure is as follows,

1. Write register 0x000080 (ISD_CONFIG) with ISD and reverse drive configuration like resync enable, reverse drive enable, stationary detect threshold, reverse drive handoff threshold etc.
2. Write register 0x000082 (REV_DRIVE_CONFIG) with reverse drive and active brake configuration like reverse drive open loop acceleration, active brake current limit, Kp, Ki values etc.
3. Write register 0x000084 (MOTOR_STARTUP1) with motor start-up configuration like start-up method, IPD parameters, align parameters etc.
4. Write register 0x000086 (MOTOR_STARTUP2) with motor start-up configuration like open loop acceleration, open loop current limit, first cycle frequency etc.
5. Write register 0x000088 (CLOSED_LOOP1) with motor control configuration like closed loop acceleration, overmodulation enable, PWM frequency, FG signal parameters etc.
6. Write register 0x00008A (CLOSED_LOOP2) with motor control configuration like motor winding resistance and inductance, motor stop options, brake speed threshold etc.
7. Write register 0x00008C (CLOSED_LOOP3) with motor control configuration like motor BEMF constant, current loop Kp, Ki etc.
8. Write register 0x00008E (CLOSED_LOOP4) with motor control configuration like speed loop Kp, Ki and maximum speed.
9. Write register 0x000090 (FAULT_CONFIG1) with fault control configuration software and hardware current limits, lock current limit and actions, retry times etc.
10. Write register 0x000092 (FAULT_CONFIG2) with fault control configuration like hardware current limit actions, OV, UV limits and actions, abnormal speed level, no motor threshold etc.
11. Write registers 0x000094 – 0x00009E (SPEED_PROFILES1-6) with speed profile configuration like profile type, duty cycle, speed clamp level, duty cycle clamp level etc.
12. Write register 0x0000A0 (INT_ALGO_1) with miscellaneous configuration like ISD run time and timeout, MPET parameters etc.
13. Write register 0x0000A2 (INT_ALGO_2) with miscellaneous configuration like additional MPET parameters, IPD high resolution enable, active brake current slew rate, closed loop slow acceleration etc.
14. Write registers 0x0000A4 (PIN_CONFIG1) with pin configuration for speed input mode (analog or PWM), BRAKE pin mode etc.
15. Write registers 0x0000A6 and 0x0000A8 (DEVICE_CONFIG1 and DEVICE_CONFIG2) with device configuration like pins 36, 37 configuration, pin 38 configuration, dynamic CSA gain enable, dynamic voltage gain enable, clock source select, speed range select etc.
16. Write register 0x0000AA (PERI_CONFIG1) with peripheral configuration like dead time, bus current limit, DIR input, SSM enable etc.
17. Write registers 0x0000AC and 0x0000AE (GD_CONFIG1 and GD_CONFIG2) with gate driver configuration like slew rate, CSA gain, OCP level, mode, OVP enable, level, buck voltage level, buck current limit etc.
18. Write 0x8A500000 into register 0x0000EA to write the shadow register(0x000080-0x0000AE) values into the EEPROM.
19. Wait for 300ms for the EEPROM write operation to complete

Steps 1-17 can be selectively executed based on registers/parameters that need to be modified. After all shadow registers have been updated with the required values, step 18 should be executed to copy the contents of the shadow registers into the EEPROM.

7.6.1.2 EEPROM Read

In MCF8315A, EEPROM read procedure is as follows,

1. Write 0x40000000 into register 0x0000EA to read the EEPROM data into the shadow registers (0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow register values,1 or 2 registers at a time, using the I²C read command as explained in セクション 7.6.2. Shadow register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation (since each address is a 16-bit location).

7.6.2 I²C Serial Interface

MCF8315A interfaces with an external MCU over an I²C serial interface. MCF8315A is an I²C target to be interfaced with a controller. External MCU can use this interface to read/write from/to any non-reserved register in MCF8315A

注
For reliable communication, a 100-μs delay should be used between every byte transferred over the I²C bus.

7.6.2.1 I²C Data Word

The I²C data word format is shown in 表 7-7.

表 7-7. I²C Data Word Format

TARGET_ID	R/W	CONTROL WORD	DATA	CRC-8
A6 - A0	W0	CW23 - CW0	D15 / D31/ D63 - D0	C7 - C0

Target ID and R/W Bit: The first byte includes the 7-bit I²C target ID (default 0x01, but can be modified by setting I2C_SLAVE_ADDR), followed by the read/write command bit. Every packet in MCF8315A the communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

24-bit Control Word: The Target Address is followed by a 24-bit control bit. The control word format is shown in 表 7-8.

表 7-8. 24-bit Control Word Format

OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR
CW23	CW22	CW21- CW20	CW19 - CW16	CW15 - CW12	CW11 - CW0

Each field in the control word is explained in detail below.

OP_R/W – Read/Write: R/W bit gives information on whether this is a read (1b) operation or write (0b) operation. For write operation, MCF8315A will expect data bytes to be sent after the 24-bit control word. For read operation, MCF8315A will expect an I²C read request with repeated start or normal start after the 24-bit control word.

CRC_EN – Cyclic Redundancy Check(CRC) Enable: MCF8315A supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

DLEN – Data Length: DLEN field determines the length of the data that will be sent by external MCU to MCF8315A. MCF8315A protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

表 7-9. Data Length Configuration

DLEN Value	Data Length
00b	16-bit
01b	32-bit
10b	64-bit
11b	Reserved

MEM_SEC – Memory Section: Each memory location in MCF8315A is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

MEM_PAGE – Memory Page: Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

MEM_ADDR – Memory Address: Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCF8315A using all three fields – Memory Section, Memory Page, Memory Address. For memory locations 0x000000-0x000800, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x800 for 0x000800). All relevant memory locations (EEPROM and RAM variables) have MEM_SEC and MEM_PAGE values both corresponding to 0x0. All other MEM_SEC, MEM_PAGE values are reserved and not for external use.

Data Bytes: For a write operation to MCF8315A, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section. In case of mismatch between number of data bytes and DLEN, the write operation is discarded.

CRC Byte: If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Refer to セクション 7.6.2.6 for detailed information on CRC byte calculation.

7.6.2.2 I^{2}C Write Transaction

MCF8315A write transaction over I^{2}C involves the following sequence (see 図 7-57).

1. I^{2}C start condition.
2. Start is followed by the I^{2}C target ID byte, made up of 7-bit target ID along with the R/W bit set to 0b. ACK in yellow box indicates that MCF8315A has processed the received target ID which has matched with it's I^{2}C target ID and therefore will proceed with this transaction. If target ID received does not match with the I^{2}C ID of MCF8315A, then the transaction is ignored. and no ACK is sent by MCF8315A.
3. The target ID byte is followed by the 24-bit control word sent one byte at a time. Bit 23 in the control word is 0b as it is a write transaction. ACK in blue boxes correspond to acknowledgements sent by MCF8315A to the controller that the previous byte (of control word) has been received and next byte can be sent.
4. The 24-bit control word is then followed by the data bytes. The number of data bytes sent by the controller depends on the DLEN field in the control word.
   a. While sending data bytes, the LSB byte is sent first. Refer to セクション 7.6.2.4 for more details.
   b. 16-bit/32-bit write – The data sent is written to the address mentioned in control word.
   c. 64-bit Write – 64-bit is treated as two successive 32-bit writes. The address mentioned in control word is taken as Addr_1. Addr_2 is internally calculated by MCF8315A by incrementing Addr_1 by 0x2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first) are written to Addr_1 and the next 4 bytes are written to Addr_2.
   d. ACK in blue boxes (after every data byte) correspond to the acknowledgement sent by MCF8315A to the controller that the previous data byte has been received and next data byte can be sent.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes). MCF8315A will send an ACK on receiving the CRC byte.
6. I^{2}C Stop condition from the controller to terminate the transaction.

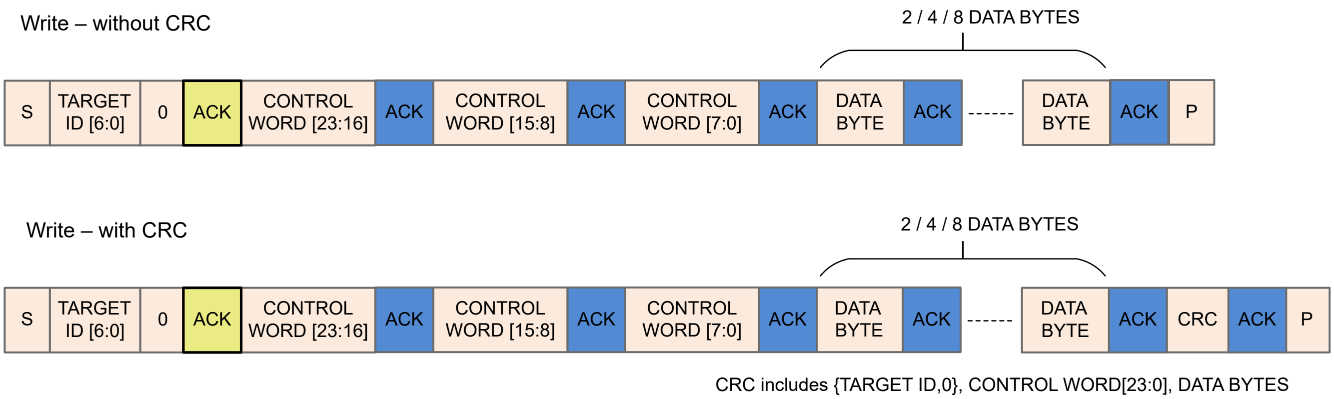

図 7-57. I²C Write Transaction Sequence

7.6.2.3 I²C Read Transaction

MCF8315A read transaction over I²C involves the following sequence (see 図 7-58).

1. I²C Start condition from the controller to initiate the transaction.
2. Start is followed by the I²C target ID byte, made up of 7-bit target ID along with the R/W bit set to 0b. ACK (in yellow box) indicates that MCF8315A has processed the received target ID which has matched with it's I²C target ID and therefore will proceed with this transaction. If target ID received does not match with the I²C ID of MCF8315A, then the transaction is ignored and no ACK is sent by MCF8315A.
3. The target ID byte is followed by the 24-bit control word sent one byte at a time. Bit 23 in the control word is set to 1b as it is a read transaction. ACK (in blue boxes) correspond to acknowledgements sent by MCF8315A to the controller that the previous byte (of control word) has been received and next byte can be sent.
4. The control word is followed by a Repeated Start (RS, start without a preceding stop) or normal Start (P followed by S) to initiate the data (to be read back) transfer from MCF8315A to I²C controller. RS or S is followed by the 7-bit target ID along with R/W bit set to 1b to initiate the read transaction. MCF8315A sends an ACK (in grey box after RS) to the controller to acknowledge the receipt of read transaction request.
5. Post acknowledgement of read transaction request, MCF8315A sends the data bytes on SDA one byte at a time. The number of data bytes sent by MCF8315A depends on the DLEN field in the control word.
   a. While sending data bytes, the LSB byte is sent first. Refer the examples in セクション 7.6.2.4 for more details.
   b. 16-bit/32-bit Read – The data from the address mentioned in control word is sent back to the controller.
   c. 64-bit Read – 64-bit is treated as two successive 32-bit reads. The address mentioned in control word is taken as Addr_1. Addr_2 is internally calculated by MCF8315A by incrementing Addr_1 by 0x2. A total of 8 data bytes are sent by MCF8315A. The first 4 bytes (sent in LSB first) are read from Addr_1 and the next 4 bytes are read from Addr_2.
   d. ACK in orange boxes correspond to acknowledgements sent by the controller to MCF8315A that the previous byte has been received and next byte can be sent.
6. If CRC is enabled in the control word, then MCF8315A sends an additional CRC byte at the end. Controller has to read the CRC byte and then send the last ACK (in orange). CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).
7. I²C Stop condition from the controller to terminate the transaction.

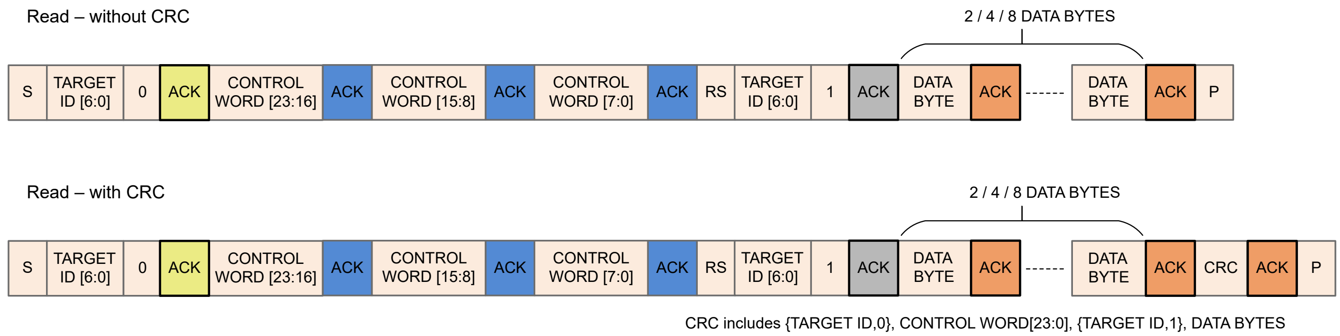

図 7-58. I²C Read Transaction Sequence

7.6.2.4 I²C Communication Protocol Packet Examples

All values used in this example section are in hex format. I²C target ID used in the examples is 0x60.

Example for 32-bit Write Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

表 7-10. Example for 32-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes				CRC
Target ID	I²C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x60	0x0	0x0	0x1	0x1	0x0	0x0	0x0	0x80	0xCD	0xAB	0x34	0x12	0x45
0xC0		0x50				0x00		0x80	0xCD	0xAB	0x34	0x12	0x45

Example for 64-bit Write Operation: Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

表 7-11. Example for 64-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes	CRC
Target ID	I²C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0 - DB7	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	[D7-D0] x 8	C7-C0
0x60	0x0	0x0	0x1	0x2	0x0	0x0	0x0	0x80	0x67452301EFCDAB89	0x45
0xC0		0x60				0x00		0x80	0x67452301EFCDAB89	0x45

Example for 32-bit Read Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

表 7-12. Example for 32-bit Read Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Start Byte		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Target ID	I²C Write	R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	Target ID	I²C Read	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	A6-A0	W0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x60	0x0	0x1	0x1	0x1	0x0	0x0	0x0	0x80	0x60	0x1	0xCD	0xAB	0x34	0x12	0x56

表 7-12. Example for 32-bit Read Operation Packet (continued)

0xC0	0xD0	0x00	0x80	0xC1	0xCD	0xAB	0x34	0x12	0x56

7.6.2.5 I²C Clock Stretching

The I^2C peripheral in MCF8315A implements clock stretching under certain conditions when there are pending I^2C interrupts waiting to be processed. During clock stretching, MCF8315A pulls SCL low and the I^2C bus is unavailable for use by other devices. The following is a list of conditions under which clock stretching can occur:

1. **Start interrupt pending**: There are two scenarios when a start interrupt can result in clock stretching,
    a. When target ID is a match, I^2C peripheral in MCF8315A raises a start interrupt request. Until this start interrupt request is processed, clock is stretched. Upon processing this request, clock is released and an ACK (marked in yellow or grey in 図 7-57 and 図 7-58) is sent to the controller for continuing with the transaction.
    b. If Start (followed by target ID match) for a new transaction is received when a receive interrupt from previous transaction is yet to be processed, clock is stretched until both the receive interrupt and start interrupt are processed in chronological order. This process ensures that previous transaction is executed correctly before initiating the next transaction.
2. **Receive interrupt pending**: When a receive interrupt is waiting to be processed and the receive register is full which occurs when two successive bytes (data or control) have been received by MCF8315A (separated by one ACK shown as blue boxes in 図 7-57 and 図 7-58) without the receive interrupt generated by the first byte being processed. Upon receive of second byte, clock is stretched until receive interrupt generated by the first byte is processed.
3. **Transmit buffer is empty**: In case of a transmit interrupt pending (to send data back to controller), if the transmit buffer is waiting to be populated with data to be read back to the controller, clock stretching is done until the transmit buffer is populated with requested data. After the buffer is populated, clock is released and data is sent to controller.

注

I^2C clock stretching is timed out after 5 ms by MCF8315A to allow I^2C bus access for other devices on the same bus.

7.6.2.6 CRC Byte Calculation

An 8-bit CCIT polynomial ($x^8 + x^2 + x + 1$) and CRC initial value 0xFF is used for CRC computation.

CRC Calculation in Write Operation: When the external MCU writes to MCF8315A, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCF8315A will compute CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

CRC Calculation in Read Operation: When the external MCU reads from MCF8315A, if the CRC is enabled, MCF8315A sends the CRC byte at the end of the data. The CRC computation in read operation involves the start byte, control words sent by external MCU along with data bytes sent by MCF8315A. Input data for CRC calculation by external MCU to verify the data sent by MCF8315A are listed below :

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

7.7 EEPROM (Non-Volatile) Register Map

7.7.1 Algorithm_Configuration Registers

表 7-13 lists the memory-mapped registers for the Algorithm_Configuration registers. All register offset addresses not listed in 表 7-13 should be considered as reserved locations and the register contents should not be modified.

表 7-13. ALGORITHM_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
80h	ISD_CONFIG	ISD Configuration	ISD_CONFIG Register (Offset = 80h) [Reset = 00000000h]
82h	REV_DRIVE_CONFIG	Reverse Drive Configuration	REV_DRIVE_CONFIG Register (Offset = 82h) [Reset = 00000000h]
84h	MOTOR_STARTUP1	Motor Startup Configuration1	MOTOR_STARTUP1 Register (Offset = 84h) [Reset = 00000000h]
86h	MOTOR_STARTUP2	Motor Startup Configuration2	MOTOR_STARTUP2 Register (Offset = 86h) [Reset = 00000000h]
88h	CLOSED_LOOP1	Close Loop Configuration1	CLOSED_LOOP1 Register (Offset = 88h) [Reset = 00000000h]
8Ah	CLOSED_LOOP2	Close Loop Configuration2	CLOSED_LOOP2 Register (Offset = 8Ah) [Reset = X]
8Ch	CLOSED_LOOP3	Close Loop Configuration3	CLOSED_LOOP3 Register (Offset = 8Ch) [Reset = X]
8Eh	CLOSED_LOOP4	Close Loop Configuration4	CLOSED_LOOP4 Register (Offset = 8Eh) [Reset = X]
94h	SPEED_PROFILES1	Speed Profile Configuration1	SPEED_PROFILES1 Register (Offset = 94h) [Reset = X]
96h	SPEED_PROFILES2	Speed Profile Configuration2	SPEED_PROFILES2 Register (Offset = 96h) [Reset = X]
98h	SPEED_PROFILES3	Speed Profile Configuration3	SPEED_PROFILES3 Register (Offset = 98h) [Reset = X]
9Ah	SPEED_PROFILES4	Speed Profile Configuration4	SPEED_PROFILES4 Register (Offset = 9Ah) [Reset = X]
9Ch	SPEED_PROFILES5	Speed Profile Configuration5	SPEED_PROFILES5 Register (Offset = 9Ch) [Reset = X]
9Eh	SPEED_PROFILES6	Speed Profile Configuration6	SPEED_PROFILES6 Register (Offset = 9Eh) [Reset = X]

Complex bit access types are encoded to fit into small table cells. 表 7-14 shows the codes that are used for access types in this section.

表 7-14. Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.1.1 ISD_CONFIG Register (Offset = 80h) [Reset = 00000000h]

ISD_CONFIG is shown in 図 7-59 and described in 表 7-15.

Return to the Summary Table.

Register to configure initial speed detect settings

図 7-59. ISD_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED	ISD_EN	BRAKE_EN	HIZ_EN	RVS_DR_EN	RESYNC_EN	FW_DRV_RESYN_THR	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FW_DRV_RESYN_THR		BRK_MODE	BRK_CONFIG	BRK_CURR_THR			BRK_TIME
R/W-0h		R/W-0h	R/W-0h	R/W-0h			R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BRK_TIME			HIZ_TIME				STAT_DETECT_THR
R/W-0h			R/W-0h				R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STAT_DETECT_THR		REV_DRV_HANDOFF_THR				REV_DRV_OPEN_LOOP_CURRENT	
R/W-0h		R/W-0h				R/W-0h	

表 7-15. ISD_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	ISD_EN	R/W	0h	ISD Enable 0h = Disable 1h = Enable
29	BRAKE_EN	R/W	0h	Brake enable 0h = Disable 1h = Enable
28	HIZ_EN	R/W	0h	Hi-Z enable 0h = Disable 1h = Enable
27	RVS_DR_EN	R/W	0h	Reverse Drive Enable 0h = Disable 1h = Enable
26	RESYNC_EN	R/W	0h	Resynchronization Enable 0h = Disable 1h = Enable

表 7-15. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-22	FW_DRV_RESYN_THR	R/W	0h	Minimum Speed threshold to resynchronize to close loop (% of MAX_SPEED) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 35% 7h = 40% 8h = 45% 9h = 50% Ah = 55% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%
21	BRK_MODE	R/W	0h	Brake mode 0h = All three high side FETs turned ON 1h = All three low side FETs turned ON
20	BRK_CONFIG	R/W	0h	Brake configuration 0h = Brake time is used to come out of Brake state 1h = Brake current threshold and Brake time is used to come out of Brake state
19-17	BRK_CURR_THR	R/W	0h	Brake current threshold (A) 0h = 0.0625 A 1h = 0.125 A 2h = 0.1875 A 3h = 0.3125 A 4h = 0.625 A 5h = 1.25 A 6h = 2.5 A 7h = 5.0 A
16-13	BRK_TIME	R/W	0h	Brake time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 S 9h = 2 S Ah = 3 S Bh = 4 S Ch = 5 S Dh = 7.5 S Eh = 10 S Fh = 15 S

表 7-15. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-9	HIZ_TIME	R/W	0h	Hi-Z time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
8-6	STAT_DETECT_THR	R/W	0h	BEMF threshold to detect if motor is stationary 0h = 50 mV 1h = 75 mV 2h = 100 mV 3h = 250 mV 4h = 500 mV 5h = 750 mV 6h = 1000 mV 7h = 1500 mV
5-2	REV_DRV_HANDOFF_THR	R/W	0h	Speed threshold used to transition to open loop during reverse deceleration (% of MAX_SPEED) 0h = 2.5% 1h = 5% 2h = 7.5% 3h = 10% 4h = 12.5% 5h = 15% 6h = 20% 7h = 25% 8h = 30% 9h = 40% Ah = 50% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%
1-0	REV_DRV_OPEN_LOOP_CURRENT	R/W	0h	Open loop current limit during speed reversal (A) 0h = 0.9375 A 1h = 1.5625 A 2h = 2.1875 A 3h = 3.125 A

7.7.1.2 REV_DRIVE_CONFIG Register (Offset = 82h) [Reset = 00000000h]

REV_DRIVE_CONFIG is shown in 図 7-60 and described in 表 7-16.

Return to the Summary Table.

Register to configure reverse drive settings

図 7-60. REV_DRIVE_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED	REV_DRV_OPEN_LOOP_ACCEL_A1				REV_DRV_OPEN_LOOP_ACCEL_A2		
R/W-0h	R/W-0h				R/W-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REV_DRV_OPEN_LOOP_ACCEL_A2	ACTIVE_BRAKE_CURRENT_LIMIT			ACTIVE_BRAKE_KP			
R/W-0h	R/W-0h			R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE_BRAKE_KP						ACTIVE_BRAKE_KI	
R/W-0h						R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE_BRAKE_KI							
R/W-0h							

表 7-16. REV_DRIVE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-27	REV_DRV_OPEN_LOOP_ACCEL_A1	R/W	0h	Open loop acceleration coefficient A1 during reverse drive 0h = 0.01 Hz/s 1h = 0.05 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s

表 7-16. REV_DRIVE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	REV_DRV_OPEN_LOOP_ACCEL_A2	R/W	0h	Open loop acceleration coefficient A2 during reverse drive 0h = 0.0 Hz/s2 1h = 0.05 Hz/s2 2h = 1 Hz/s2 3h = 2.5 Hz/s2 4h = 5 Hz/s2 5h = 10 Hz/s2 6h = 25 Hz/s2 7h = 50 Hz/s2 8h = 75 Hz/s2 9h = 100 Hz/s2 Ah = 250 Hz/s2 Bh = 500 Hz/s2 Ch = 750 Hz/s2 Dh = 1000 Hz/s2 Eh = 5000 Hz/s2 Fh = 10000 Hz/s2
22-20	ACTIVE_BRAKE_CURRENT_LIMIT	R/W	0h	Bus current limit during active braking (A) 0h = 0.3125 A 1h = 0.625 A 2h = 1.25 A 3h = 1.875 A 4h = 2.5 A 5h = 3.125 A 6h = 3.75 A 7h = Reserved
19-10	ACTIVE_BRAKE_KP	R/W	0h	10-bit value for active braking loop Kp. Kp = ACTIVE_BRAKE_KP / 2^7
9-0	ACTIVE_BRAKE_KI	R/W	0h	10-bit value for active braking loop Ki. Ki = ACTIVE_BRAKE_KI / 2^9

7.7.1.3 MOTOR_STARTUP1 Register (Offset = 84h) [Reset = 00000000h]

MOTOR_STARTUP1 is shown in 図 7-61 and described in 表 7-17.

Return to the Summary Table.

Register to configure motor startup settings1

図 7-61. MOTOR_STARTUP1 Register

31	30	29	28	27	26	25	24
RESERVED	MTR_STARTUP		ALIGN_SLOW_RAMP_RATE				ALIGN_TIME
R/W-0h	R/W-0h		R/W-0h				R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ALIGN_TIME			ALIGN_OR_SLOW_CURRENT_ILIMIT				IPD_CLK_FREQ
R/W-0h			R/W-0h				R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPD_CLK_FREQ		IPD_CURR_THR					IPD_RLS_MODE
R/W-0h		R/W-0h					R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPD_ADV_ANGLE		IPD_REPEAT		OL_ILIMIT_CONFIG	IQ_RAMP_EN	ACTIVE_BRAKE_EN	REV_DRV_CONFIG
R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-17. MOTOR_STARTUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-29	MTR_STARTUP	R/W	0h	Motor start-up options 0h = Align 1h = Double Align 2h = IPD 3h = Slow first cycle
28-25	ALIGN_SLOW_RAMP_RATE	R/W	0h	Align, slow first cycle and open loop current ramp rate 0h = 0.1 A/s 1h = 1 A/s 2h = 5 A/s 3h = 10 A/s 4h = 15 A/s 5h = 25 A/s 6h = 50 A/s 7h = 100 A/s 8h = 150 A/s 9h = 200 A/s Ah = 250 A/s Bh = 500 A/s Ch = 1000 A/s Dh = 2000 A/s Eh = 5000 A/s Fh = No Limit A/s

表 7-17. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-21	ALIGN_TIME	R/W	0h	Align time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 S 9h = 1.5 S Ah = 2 S Bh = 3 S Ch = 4 S Dh = 5 S Eh = 7.5 S Fh = 10 S
20-17	ALIGN_OR_SLOW_CURRENT_ILIMIT	R/W	0h	Align or slow first cycle current limit (A) 0h = 0.078125 A 1h = 0.15625 A 2h = 0.3125 A 3h = 0.625 A 4h = 0.9375 A 5h = 1.25 A 6h = 1.5625 A 7h = 1.875 A 8h = 2.1875 A 9h = 2.5 A Ah = 2.8125 A Bh = 3.125 A Ch = 3.4375 A Dh = 3.75 A Eh = Reserved Fh = Reserved
16-14	IPD_CLK_FREQ	R/W	0h	IPD Clock Frequency 0h = 50 Hz 1h = 100 Hz 2h = 250 Hz 3h = 500 Hz 4h = 1000 Hz 5h = 2000 Hz 6h = 5000 Hz 7h = 10000 Hz

表 7-17. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-9	IPD_CURR_THR	R/W	0h	IPD Current Threshold (A) 0h = 0.15625 A 1h = 0.3125 A 2h = 0.468 A 3h = 00.625 A 4h = 0.78125 A 5h = 0.9375 A 6h = 1.25 A 7h = 1.5625 A 8h = 1.875 A 9h = 2.291 A Ah = 2.5 A Bh = 2.916 A Ch = 3.125 A Dh = 3.333 A Eh = 3.75 A Fh = 4.166 A 10h = 4.583 A 11h = 5 A 12h = Reserved 13h = Reserved 14h = Reserved 15h = Reserved 16h = Reserved 17h = Reserved 18h = Reserved 19h = Reserved 1Ah = Reserved 1Bh = Reserved 1Ch = Reserved 1Dh = Reserved 1Eh = Reserved 1Fh = Reserved
8	IPD_RLS_MODE	R/W	0h	IPD release mode 0h = Brake 1h = Tristate
7-6	IPD_ADV_ANGLE	R/W	0h	IPD advance angle 0h = 0 deg 1h = 30 deg 2h = 60 deg 3h = 90 deg
5-4	IPD_REPEAT	R/W	0h	Number of times IPD is executed 0h = 1 time 1h = average of 2 times 2h = average of 3 times 3h = average of 4 times
3	OL_ILIMIT_CONFIG	R/W	0h	Open loop current limit configuration 0h = Open loop current limit defined by OL_ILIMIT 1h = Open loop current limit defined by ILIMIT
2	IQ_RAMP_EN	R/W	0h	Iq ramp down after transition to close loop enable 0h = Disable Iq ramp down 1h = Enable Iq ramp down
1	ACTIVE_BRAKE_EN	R/W	0h	Enables active braking during deceleration 0h = Disable Active Brake Reverse Drive 1h = Enable Active Brake Reverse Drive
0	REV_DRV_CONFIG	R/W	0h	Chooses between forward and reverse drive setting for reverse drive 0h = Open loop current, A1, A2 based on forward drive 1h = Open loop current, A1, A2 based on reverse drive

7.7.1.4 MOTOR_STARTUP2 Register (Offset = 86h) [Reset = 00000000h]

MOTOR_STARTUP2 is shown in 図 7-62 and described in 表 7-18.

Return to the Summary Table.

Register to configure motor startup settings2

図 7-62. MOTOR_STARTUP2 Register

31	30	29	28	27	26	25	24
RESERVED	OL_ILIMIT				OL_ACC_A1		
R/W-0h	R/W-0h				R/W-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OL_ACC_A1	OL_ACC_A2				AUTO_HANDOFF_EN	OPN_CL_HANDOFF_THR	
R/W-0h	R/W-0h				R/W-0h	R/W-0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OPN_CL_HANDOFF_THR			ALIGN_ANGLE				
R/W-0h			R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SLOW_FIRST_CYC_FREQ				FIRST_CYCLE_FREQ_SEL	THETA_ERROR_RAMP_RATE		
R/W-0h				R/W-0h	R/W-0h		

表 7-18. MOTOR_STARTUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-27	OL_ILIMIT	R/W	0h	Open Loop current limit (A) 0h = 0.078125 A 1h = 0.15625 A 2h = 0.3125 A 3h = 0.625 A 4h = 0.9375 A 5h = 1.25 A 6h = 1.5625 A 7h = 1.875 A 8h = 2.1875 A 9h = 2.5 A Ah = 2.8125 A Bh = 3.125 A Ch = 3.4375 A Dh = 3.75 A Eh = Reserved Fh = Reserved

表 7-18. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	OL_ACC_A1	R/W	0h	Open loop acceleration coefficient A1 0h = 0.01 Hz/s 1h = 0.05 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s
22-19	OL_ACC_A2	R/W	0h	Open loop acceleration coefficient A2 0h = 0.0 Hz/s2 1h = 0.05 Hz/s2 2h = 1 Hz/s2 3h = 2.5 Hz/s2 4h = 5 Hz/s2 5h = 10 Hz/s2 6h = 25 Hz/s2 7h = 50 Hz/s2 8h = 75 Hz/s2 9h = 100 Hz/s2 Ah = 250 Hz/s2 Bh = 500 Hz/s2 Ch = 750 Hz/s2 Dh = 1000 Hz/s2 Eh = 5000 Hz/s2 Fh = 10000 Hz/s2
18	AUTO_HANDOFF_EN	R/W	0h	Auto Handoff Enable 0h = Disable Auto Handoff (and use OPN_CL_HANDOFF_THR) 1h = Enable Auto Handoff

表 7-18. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-13	OPN_CL_HANDOFF_TH R	R/W	0h	Open to Close loop Handoff Threshold (% of MAX_SPEED) 0h = 1% 1h = 2% 2h = 3% 3h = 4% 4h = 5% 5h = 6% 6h = 7% 7h = 8% 8h = 9% 9h = 10% Ah = 11% Bh = 12% Ch = 13% Dh = 14% Eh = 15% Fh = 16% 10h = 17% 11h = 18% 12h = 19% 13h = 20% 14h = 22.5% 15h = 25% 16h = 27.5% 17h = 30% 18h = 32.5% 19h = 35% 1Ah = 37.5% 1Bh = 40% 1Ch = 42.5% 1Dh = 45% 1Eh = 47.5% 1Fh = 50%

表 7-18. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	ALIGN_ANGLE	R/W	0h	Align Angle 0h = 0 deg 1h = 10 deg 2h = 20 deg 3h = 30 deg 4h = 45 deg 5h = 60 deg 6h = 70 deg 7h = 80 deg 8h = 90 deg 9h = 110 deg Ah = 120 deg Bh = 135 deg Ch = 150 deg Dh = 160 deg Eh = 170 deg Fh = 180 deg 10h = 190 deg 11h = 210 deg 12h = 225 deg 13h = 240 deg 14h = 250 deg 15h = 260 deg 16h = 270 deg 17h = 280 deg 18h = 290 deg 19h = 315 deg 1Ah = 330 deg 1Bh = 340 deg 1Ch = 350 deg 1Dh = Reserved 1Eh = Reserved 1Fh = Reserved
7-4	SLOW_FIRST_CYC_FREQ	R/W	0h	Frequency of first cycle in close loop start-up (% of MAX_SPEED) 0h = 1% 1h = 2% 2h = 3% 3h = 5% 4h = 7.5% 5h = 10% 6h = 12.5% 7h = 15% 8h = 17.5% 9h = 20% Ah = 25% Bh = 30% Ch = 35% Dh = 40% Eh = 45% Fh = 50%
3	FIRST_CYCLE_FREQ_SEL	R/W	0h	First cycle frequency in open loop for align, double align and IPD start-up options 0h = 0 Hz 1h = Defined by SLOW_FIRST_CYC_FREQ

表 7-18. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	THETA_ERROR_RAMP_RATE	R/W	0h	Ramp rate for reducing difference between estimated theta and open loop theta (deg/ms) 0h = 0.01 deg/ms 1h = 0.05 deg/ms 2h = 0.1 deg/ms 3h = 0.15 deg/ms 4h = 0.2 deg/ms 5h = 0.5 deg/ms 6h = 1 deg/ms 7h = 2 deg/ms

7.7.1.5 CLOSED_LOOP1 Register (Offset = 88h) [Reset = 00000000h]

CLOSED_LOOP1 is shown in 図 7-63 and described in 表 7-19.

Return to the Summary Table.

Register to configure close loop settings1

図 7-63. CLOSED_LOOP1 Register

31	30	29	28	27	26	25	24
RESERVED	OVERMODULATION_ENABLE	CL_ACC					CL_DEC_CONFIG
R/W-0h	R/W-0h	R/W-0h					R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CL_DEC					PWM_FREQ_OUT		
R/W-0h					R/W-0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWM_FREQ_OUT	PWM_MODE	FG_SEL		FG_DIV			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FG_CONFIG	FG_BEMF_THR			AVS_EN	DEADTIME_COMP_EN	SPEED_LOOP_DIS	LOW_SPEED_RECIRC_BRAKE_EN
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-19. CLOSED_LOOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	OVERMODULATION_ENABLE	R/W	0h	Enables Over modulation 0h = Disable Over Modulation 1h = Enable Over Modulation

表 7-19. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29-25	CL_ACC	R/W	0h	Closed loop acceleration (Hz / sec) 0h = 0.5 Hz/s 1h = 1 Hz/s 2h = 2.5 Hz/s 3h = 5 Hz/s 4h = 7.5 Hz/s 5h = 10 Hz/s 6h = 20 Hz/s 7h = 40 Hz/s 8h = 60 Hz/s 9h = 80 Hz/s Ah = 100 Hz/s Bh = 200 Hz/s Ch = 300 Hz/s Dh = 400 Hz/s Eh = 500 Hz/s Fh = 600 Hz/s 10h = 700 Hz/s 11h = 800 Hz/s 12h = 900 Hz/s 13h = 1000 Hz/s 14h = 2000 Hz/s 15h = 4000 Hz/s 16h = 6000 Hz/s 17h = 8000 Hz/s 18h = 10000 Hz/s 19h = 20000 Hz/s 1Ah = 30000 Hz/s 1Bh = 40000 Hz/s 1Ch = 50000 Hz/s 1Dh = 60000 Hz/s 1Eh = 70000 Hz/s 1Fh = No limit
24	CL_DEC_CONFIG	R/W	0h	Closed loop deceleration configuration 0h = Closed loop deceleration defined by CL_DEC 1h = Closed loop deceleration defined by CL_ACC

表 7-19. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-19	CL_DEC	R/W	0h	Closed loop deceleration. This register is used only if AVS is disabled and CL_DEC_CONFIG is set to '0' 0h = 0.5 Hz/s 1h = 1 Hz/s 2h = 2.5 Hz/s 3h = 5 Hz/s 4h = 7.5 Hz/s 5h = 10 Hz/s 6h = 20 Hz/s 7h = 40 Hz/s 8h = 60 Hz/s 9h = 80 Hz/s Ah = 100 Hz/s Bh = 200 Hz/s Ch = 300 Hz/s Dh = 400 Hz/s Eh = 500 Hz/s Fh = 600 Hz/s 10h = 700 Hz/s 11h = 800 Hz/s 12h = 900 Hz/s 13h = 1000 Hz/s 14h = 2000 Hz/s 15h = 4000 Hz/s 16h = 6000 Hz/s 17h = 8000 Hz/s 18h = 10000 Hz/s 19h = 20000 Hz/s 1Ah = 30000 Hz/s 1Bh = 40000 Hz/s 1Ch = 50000 Hz/s 1Dh = 60000 Hz/s 1Eh = 70000 Hz/s 1Fh = No limit
18-15	PWM_FREQ_OUT	R/W	0h	PWM output frequency 0h = 10 kHz 1h = 15 kHz 2h = 20 kHz 3h = 25 kHz 4h = 30 kHz 5h = 35 kHz 6h = 40 kHz 7h = 45 kHz 8h = 50 kHz 9h = 55 kHz Ah = 60 kHz Bh = 65 kHz Ch = 70 kHz Dh = 75 kHz Eh = Reserved Fh = Reserved
14	PWM_MODE	R/W	0h	PWM modulation 0h = Continuous Space Vector Modulation 1h = Discontinuous Space Vector Modulation
13-12	FG_SEL	R/W	0h	FG select 0h = Output FG in open loop and closed loop 1h = Output FG in only closed loop 2h = Output FG in open loop for the first try. 3h = Not Defined

表 7-19. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	FG_DIV	R/W	0h	FG Division factor 0h = Divide by 1 (2-pole motor mechanical speed) 1h = Divide by 1 (2-pole motor mechanical speed) 2h = Divide by 2 (4-pole motor mechanical speed) 3h = Divide by 3 (6-pole motor mechanical speed) 4h = Divide by 4 (8-pole motor mechanical speed) ... Fh = Divide by 15 (30-pole motor mechanical speed)
7	FG_CONFIG	R/W	0h	FG output configuration 0h = FG active as long as motor is driven 1h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR
6-4	FG_BEMF_THR	R/W	0h	FG output BEMF threshold 0h = +/- 1mV 1h = +/- 2mV 2h = +/- 5mV 3h = +/- 10mV 4h = +/- 20mV 5h = +/- 30mV 6h = Reserved 7h = Reserved
3	AVS_EN	R/W	0h	AVS enable 0h = Disable 1h = Enable
2	DEADTIME_COMP_EN	R/W	0h	Deadtime compensation enable 0h = Disable 1h = Enable
1	SPEED_LOOP_DIS	R/W	0h	Speed Loop Disable 0h = Enable 1h = Disable
0	LOW_SPEED_RECIRC_BRAKE_EN	R/W	0h	Stop mode applied when stop mode is recirculation brake and motor running in align or open loop 0h = Hi-Z 1h = Low Side Brake

7.7.1.6 CLOSED_LOOP2 Register (Offset = 8Ah) [Reset = X]

CLOSED_LOOP2 is shown in 図 7-64 and described in 表 7-20.

Return to the Summary Table.

Register to configure close loop settings2

図 7-64. CLOSED_LOOP2 Register

31	30	29	28	27	26	25	24
RESERVED	MTR_STOP			MTR_STOP_BRK_TIME			
R/W-0h	R/W-0h			R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACT_SPIN_THR				BRAKE_SPEED_THRESHOLD			
R/W-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MOTOR_RES							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MOTOR_IND							
R/W-X							

表 7-20. CLOSED_LOOP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-28	MTR_STOP	R/W	0h	Motor stop options 0h = Hi-z 1h = Reserved 2h = Low side braking 3h = High side braking 4h = Active spin down 5h = Align braking 6h = Not Defined 7h = Not Defined
27-24	MTR_STOP_BRK_TIME	R/W	0h	Brake time during motor stop 0h = 1 ms 1h = 1 ms 2h = 1 ms 3h = 1 ms 4h = 1 ms 5h = 5 ms 6h = 10 ms 7h = 50 ms 8h = 100 ms 9h = 250 ms Ah = 500 ms Bh = 1000 ms Ch = 2500 ms Dh = 5000 ms Eh = 10000 ms Fh = 15000 ms

表 7-20. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-20	ACT_SPIN_THR	R/W	0h	Speed threshold for active spin down (% of MAX_SPEED) 0h = 100 % 1h = 90 % 2h = 80 % 3h = 70 % 4h = 60% 5h = 50 % 6h = 45 % 7h = 40 % 8h = 35 % 9h = 30 % Ah = 25 % Bh = 20 % Ch = 15 % Dh = 10 % Eh = 5 % Fh = 2.5 %
19-16	BRAKE_SPEED_THRESHOLD	R/W	0h	Speed threshold for BRAKE pin and Motor stop options (Low side Braking or High Side Braking or Align Braking) (% of MAX_SPEED) 0h = 100 % 1h = 90 % 2h = 80 % 3h = 70 % 4h = 60% 5h = 50 % 6h = 45 % 7h = 40 % 8h = 35 % 9h = 30 % Ah = 25 % Bh = 20 % Ch = 15 % Dh = 10 % Eh = 5 % Fh = 2.5 %
15-8	MOTOR_RES	R/W	X	8-bit values for motor phase resistance. See 表 7-2 for values of phase resistance
7-0	MOTOR_IND	R/W	X	8-bit values for motor phase inductance. See Table 7-3 for values of phase inductance

7.7.1.7 CLOSED_LOOP3 Register (Offset = 8Ch) [Reset = X]

CLOSED_LOOP3 is shown in 図 7-65 and described in 表 7-21.

Return to the Summary Table.

Register to configure close loop settings3

図 7-65. CLOSED_LOOP3 Register

31	30	29	28	27	26	25	24
RESERVED	MOTOR_BEMF_CONST						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MOTOR_BEMF_CONST	CURR_LOOP_KP						
R/W-X	R/W-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CURR_LOOP_KP			CURR_LOOP_KI				
R/W-0h			R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURR_LOOP_KI					SPD_LOOP_KP		
R/W-0h					R/W-0h		

表 7-21. CLOSED_LOOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-23	MOTOR_BEMF_CONST	R/W	X	8-bit values for motor BEMF Constant. See Table 7-4 for values of BEMF constant
22-13	CURR_LOOP_KP	R/W	0h	10-bit value for current Iq and Id loop Kp. Kp = 8LSB of CURR_LOOP_KP / 10^2MSB of CURR_LOOP_KP. Please make 0 for auto calculation of current Kp and Ki
12-3	CURR_LOOP_KI	R/W	0h	10-bit value for current Iq and Id loop Ki. Ki = 1000 * 8LSB of CURR_LOOP_KI / 10^2MSB of CURR_LOOP_KI. Please make 0 for auto calculation of current Kp and Ki
2-0	SPD_LOOP_KP	R/W	0h	3 MSB bits for speed loop Kp. Kp = 0.01 * 8LSB of SPD_LOOP_KP / 10^2MSB of SPD_LOOP_KP

7.7.1.8 CLOSED_LOOP4 Register (Offset = 8Eh) [Reset = X]

CLOSED_LOOP4 is shown in 図 7-66 and described in 表 7-22.

Return to the Summary Table.

Register to configure close loop settings4

図 7-66. CLOSED_LOOP4 Register

31	30	29	28	27	26	25	24
RESERVED	SPD_LOOP_KP						
R/W-0h	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPD_LOOP_KI							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPD_LOOP_KI		MAX_SPEED					
R/W-0h		R/W-X					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX_SPEED							
R/W-X							

表 7-22. CLOSED_LOOP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-24	SPD_LOOP_KP	R/W	0h	7 LSB bits for speed loop Kp. Kp = 0.01 * 8LSB of SPD_LOOP_KP / 10^2MSB of SPD_LOOP_KP
23-14	SPD_LOOP_KI	R/W	0h	10 bit value for speed loop Ki. Ki = 0.1 * 8LSB of SPD_LOOP_KI / 10^2MSB of SPD_LOOP_KI
13-0	MAX_SPEED	R/W	X	14-bit value for setting maximum value of Speed in electrical Hz Maximum motor electrical speed (Hz): {MOTOR_SPEED/6} For example: if MOTOR_SPEED is 0x2710, then maximum motor speed (Hz) = 10000(0x2710)/6 = 1666 Hz

7.7.1.9 SPEED_PROFILES1 Register (Offset = 94h) [Reset = X]

SPEED_PROFILES1 is shown in 図 7-67 and described in 表 7-23.

Return to the Summary Table.

Register to configure speed profile1

図 7-67. SPEED_PROFILES1 Register

31	30	29	28	27	26	25	24
RESERVED	SPEED_PROFILE_CONFIG		DUTY_ON1				
R/W-0h	R/W-0h		R/W-X				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DUTY_ON1			DUTY_OFF1				
R/W-X			R/W-X				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DUTY_OFF1			DUTY_CLAMP1				
R/W-X			R/W-X				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DUTY_CLAMP1			DUTY_A				
R/W-X			R/W-X				

表 7-23. SPEED_PROFILES1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-29	SPEED_PROFILE_CONFIG	R/W	0h	Configuration for speed profiles 0h = Speed Reference Mode 1h = Linear Mode 2h = Staircase Mode 3h = Forward Reverse Mode
28-21	DUTY_ON1	R/W	X	Duty_ON1 Configuration Turn On Duty Cycle (%) = {(DUTY_ON1/255)*100}
20-13	DUTY_OFF1	R/W	X	Duty_OFF1 Configuration Turn Off Duty Cycle (%) = {(DUTY_OFF1/255)*100}
12-5	DUTY_CLAMP1	R/W	X	Duty_CLAMP1 Configuration Duty Cycle for clamping speed (%) = {(DUTY_CLAMP1/255)*100}
4-0	DUTY_A	R/W	X	5 MSB bits for Duty Cycle A

7.7.1.10 SPEED_PROFILES2 Register (Offset = 96h) [Reset = X]

SPEED_PROFILES2 is shown in 図 7-68 and described in 表 7-24.

Return to the Summary Table.

Register to configure speed profile2

図 7-68. SPEED_PROFILES2 Register

31	30	29	28	27	26	25	24
RESERVED	DUTY_A			DUTY_B			
R/W-0h	R/W-X			R/W-X			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DUTY_B				DUTY_C			
R/W-X				R/W-X			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DUTY_C				DUTY_D			
R/W-X				R/W-X			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DUTY_D				DUTY_E			
R/W-X				R/W-0h			

表 7-24. SPEED_PROFILES2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-28	DUTY_A	R/W	X	3 LSB bits for Duty Cycle A Duty_A Configuration Duty Cycle A (%) = {(DUTY_A/255)*100}
27-20	DUTY_B	R/W	X	Duty_B Configuration Duty Cycle B (%) = {(DUTY_B/255)*100}
19-12	DUTY_C	R/W	X	Duty_C Configuration Duty Cycle C (%) = {(DUTY_C/255)*100}
11-4	DUTY_D	R/W	X	Duty_D Configuration Duty Cycle D (%) = {(DUTY_D/255)*100}
3-0	DUTY_E	R/W	0h	4 MSB bits for Duty Cycle E

7.7.1.11 SPEED_PROFILES3 Register (Offset = 98h) [Reset = X]

SPEED_PROFILES3 is shown in 図 7-69 and described in 表 7-25.

Return to the Summary Table.

Register to configure speed profile3

図 7-69. SPEED_PROFILES3 Register

31	30	29	28	27	26	25	24
RESERVED	DUTY_E				DUTY_ON2		
R/W-0h	R/W-X				R/W-X		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DUTY_ON2					DUTY_OFF2		
R/W-X					R/W-X		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DUTY_OFF2					DUTY_CLAMP2		
R/W-X					R/W-X		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DUTY_CLAMP2					DUTY_HYST		RESERVED
R/W-X					R/W-0h		R/W-0h

表 7-25. SPEED_PROFILES3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-27	DUTY_E	R/W	X	4 LSB bits for Duty Cycle E Duty_E Configuration Duty Cycle E (%) = {(DUTY_E/255)*100}
26-19	DUTY_ON2	R/W	X	Duty_ON2 Configuration Turn On Duty Cycle (%) = {(DUTY_ON2/255)*100}
18-11	DUTY_OFF2	R/W	X	Duty_OFF2 Configuration Turn Off Duty Cycle (%) = {(DUTY_OFF2/255)*100}
10-3	DUTY_CLAMP2	R/W	X	Duty_CLAMP2 Configuration Duty Cycle for clamping speed (%) = {(DUTY_CLAMP1/255)*100}
2-1	DUTY_HYST	R/W	0h	Duty hysteresis for speed reference mode 0h = 0% 1h = 0.5% 2h = 1% 3h = 2%
0	RESERVED	R/W	0h	Reserved

7.7.1.12 SPEED_PROFILES4 Register (Offset = 9Ah) [Reset = X]

SPEED_PROFILES4 is shown in 図 7-70 and described in 表 7-26.

Return to the Summary Table.

Register to configure speed profile4

図 7-70. SPEED_PROFILES4 Register

31	30	29	28	27	26	25	24
RESERVED	SPEED_OFF1						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPEED_OFF1	SPEED_CLAMP1						
R/W-X	R/W-X						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPEED_CLAMP1	SPEED_A						
R/W-X	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEED_A	SPEED_B						
R/W-X	R/W-X						

表 7-26. SPEED_PROFILES4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-23	SPEED_OFF1	R/W	X	Turn off speed Configuration Turn off speed (% of MAX_SPEED) = {(SPEED_OFF1/255)*100}
22-15	SPEED_CLAMP1	R/W	X	Clamp Speed Configuration Clamp Speed (% of MAX_SPEED) = {(SPEED_CLAMP1/255)*100}
14-7	SPEED_A	R/W	X	Speed A configuration SPEED A (% of MAX_SPEED) = {(SPEED_A/255)*100}
6-0	SPEED_B	R/W	X	7 MSB of SPEED_B configuration

7.7.1.13 SPEED_PROFILES5 Register (Offset = 9Ch) [Reset = X]

SPEED_PROFILES5 is shown in 図 7-71 and described in 表 7-27.

Return to the Summary Table.

Register to configure speed profile5

図 7-71. SPEED_PROFILES5 Register

31	30	29	28	27	26	25	24
RESERVED	SPEED_B	SPEED_C					
R/W-0h	R/W-X	R/W-X					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPEED_C		SPEED_D					
R/W-X		R/W-X					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPEED_D		SPEED_E					
R/W-X		R/W-X					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPEED_E		RESERVED					
R/W-X		R/W-0h					

表 7-27. SPEED_PROFILES5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	SPEED_B	R/W	X	1 LSB of SPEED_B configuration Speed B Configuration SPEED B(% of MAX_SPEED) = {(SPEED_B/255)*100}
29-22	SPEED_C	R/W	X	Speed C configuration SPEED C (% of MAX_SPEED) = {(SPEED_A/255)*100}
21-14	SPEED_D	R/W	X	Speed D configuration SPEED D (% of MAX_SPEED) = {(SPEED_D/255)*100}
13-6	SPEED_E	R/W	X	Speed E Configuration SPEED E(% of MAX_SPEED) = {(SPEED_E/255)*100}
5-0	RESERVED	R/W	0h	Reserved

7.7.1.14 SPEED_PROFILES6 Register (Offset = 9Eh) [Reset = X]

SPEED_PROFILES6 is shown in 図 7-72 and described in 表 7-28.

Return to the Summary Table.

Register to configure speed profile6

図 7-72. SPEED_PROFILES6 Register

31	30	29	28	27	26	25	24
RESERVED	SPEED_OFF2						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SPEED_OFF2	SPEED_CLAMP2						
R/W-X	R/W-X						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPEED_CLAMP2	RESERVED						
R/W-X	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-X							

表 7-28. SPEED_PROFILES6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-23	SPEED_OFF2	R/W	X	Turn off speed Configuration Turn off speed (% of MAX_SPEED) = {(SPEED_OFF2/255)*100}
22-15	SPEED_CLAMP2	R/W	X	Clamp Speed Configuration Clamp Speed (% of MAX_SPEED) = {(SPEED_CLAMP2/255)*100}
14-0	RESERVED	R/W	X	Reserved

7.7.2 Fault_Configuration Registers

表 7-29 lists the memory-mapped registers for the Fault_Configuration registers. All register offset addresses not listed in 表 7-29 should be considered as reserved locations and the register contents should not be modified.

表 7-29. FAULT_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
90h	FAULT_CONFIG1	Fault Configuration1	FAULT_CONFIG1 Register (Offset = 90h) [Reset = 00000000h]
92h	FAULT_CONFIG2	Fault Configuration2	FAULT_CONFIG2 Register (Offset = 92h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. 表 7-30 shows the codes that are used for access types in this section.

表 7-30. Fault_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

表 7-30. Fault_Configuration Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

7.7.2.1 FAULT_CONFIG1 Register (Offset = 90h) [Reset = 00000000h]

FAULT_CONFIG1 is shown in 図 7-73 and described in 表 7-31.

Return to the Summary Table.

Register to configure fault settings1

図 7-73. FAULT_CONFIG1 Register

31	30	29	28	27	26	25	24
RESERVED	ILIMIT				HW_LOCK_ILIMIT		
R/W-0h	R/W-0h				R/W-0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HW_LOCK_ILIMIT	LOCK_ILIMIT				LOCK_ILIMIT_MODE		
R/W-0h	R/W-0h				R/W-0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOCK_ILIMIT_MODE	LOCK_ILIMIT_DEG				LCK_RETRY		
R/W-0h	R/W-0h				R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LCK_RETRY	MTR_LCK_MODE				IPD_TIMEOUT_FAULT_EN	IPD_FREQ_FAULT_EN	SATURATION_FLAGS_EN
R/W-0h	R/W-0h				R/W-0h	R/W-0h	R/W-0h

表 7-31. FAULT_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-27	ILIMIT	R/W	0h	Reference for Torque PI Loop (A) 0h = 0.078125 A 1h = 0.15625 A 2h = 0.3125 A 3h = 0.625 A 4h = 0.9375 A 5h = 1.25 A 6h = 1.5625 A 7h = 1.875 A 8h = 2.1875 A 9h = 2.5 A Ah = 2.8125 A Bh = 3.125 A Ch = 3.4375 A Dh = 3.75 A Eh = Reserved Fh = Reserved

表 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	HW_LOCK_ILIMIT	R/W	0h	Comparator based lock detection current limit (A) 0h = 0.078125 A 1h = 0.15625 A 2h = 0.3125 A 3h = 0.625 A 4h = 0.9375 A 5h = 1.25 A 6h = 1.5625 A 7h = 1.875 A 8h = 2.1875 A 9h = 2.5 A Ah = 2.8125 A Bh = 3.125 A Ch = 3.4375 A Dh = 3.75 A Eh = Reserved Fh = Reserved
22-19	LOCK_ILIMIT	R/W	0h	ADC based lock detection current threshold (A) 0h = 0.078125 A 1h = 0.15625 A 2h = 0.3125 A 3h = 0.625 A 4h = 0.9375 A 5h = 1.25 A 6h = 1.5625 A 7h = 1.875 A 8h = 2.1875 A 9h = 2.5 A Ah = 2.8125 A Bh = 3.125 A Ch = 3.4375 A Dh = 3.75 A Eh = Reserved Fh = Reserved

表 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	LOCK_ILIMIT_MODE	R/W	0h	Lock current Limit Mode 0h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode 2h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON) 3h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFault active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode; nFault active 6h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in high side brake mode (All high side FETs are turned ON); nFault active 7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFault active 8h = Ilimit lock detection current limit is in report only but no action is taken; nFault active 9h = ILIMIT LOCK is disabled Ah = ILIMIT LOCK is disabled Bh = ILIMIT LOCK is disabled Ch = ILIMIT LOCK is disabled Dh = ILIMIT LOCK is disabled Eh = ILIMIT LOCK is disabled Fh = ILIMIT LOCK is disabled
14-11	LOCK_ILIMIT_DEG	R/W	0h	Lock Detection current limit deglitch time 0h = 0.05 ms 1h = 0.1 ms 2h = 0.2 ms 3h = 0.5 ms 4h = 1 ms 5h = 2.5 ms 6h = 5 ms 7h = 7.5 ms 8h = 10 ms 9h = 25 ms Ah = 50 ms Bh = 75 ms Ch = 100 ms Dh = 200 ms Eh = 500 ms Fh = 1000 ms

表 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-7	LCK_RETRY	R/W	0h	Lock detection retry time 0h = Reserved 1h = 500 ms 2h = 1 s 3h = 2 s 4h = 3 s 5h = 4 s 6h = 5 s 7h = 6 s 8h = 7 s 9h = 8 s Ah = 9 s Bh = 10 s Ch = 11 s Dh = 12 s Eh = 13 s Fh = 14 s
6-3	MTR_LCK_MODE	R/W	0h	Motor Lock Mode 0h = Motor lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode 2h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON) 3h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFault active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode; nFault active 6h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in high side brake mode (All high side FETs are turned ON); nFault active 7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFault active 8h = Motor lock detection current limit is in report only but no action is taken; nFault active 9h = Motor lock detection is disabled Ah = Motor lock detection is disabled Bh = Motor lock detection is disabled Ch = Motor lock detection is disabled Dh = Motor lock detection is disabled Eh = Motor lock detection is disabled Fh = Motor lock detection is disabled
2	IPD_TIMEOUT_FAULT_EN	R/W	0h	IPD timeout fault Enable 0h = Disable 1h = Enable
1	IPD_FREQ_FAULT_EN	R/W	0h	IPD frequency fault Enable 0h = Disable 1h = Enable
0	SATURATION_FLAGS_EN	R/W	0h	Enables indication of current loop and speed loop saturation 0h = Disable 1h = Enable

7.7.2.2 FAULT_CONFIG2 Register (Offset = 92h) [Reset = 00000000h]

FAULT_CONFIG2 is shown in 図 7-74 and described in 表 7-32.

Return to the Summary Table.

Register to configure fault settings2

図 7-74. FAULT_CONFIG2 Register

31	30	29	28	27	26	25	24
RESERVED	LOCK1_EN	LOCK2_EN	LOCK3_EN	LOCK_ABN_SPEED			ABNORMAL_BEMF_THR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
23	22	21	20	19	18	17	16
ABNORMAL_BEMF_THR		NO_MTR_THR			HW_LOCK_ILIMIT_MODE		
R/W-0h		R/W-0h			R/W-0h		
15	14	13	12	11	10	9	8
HW_LOCK_ILIMIT_MODE	HW_LOCK_ILIMIT_DEG			RESERVED	MIN_VM_MOTOR		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
MIN_VM_MODE	MAX_VM_MOTOR			MAX_VM_MODE	AUTO_RETRY_TIMES		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

表 7-32. FAULT_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	LOCK1_EN	R/W	0h	Lock 1 (Abnormal Speed) Enable 0h = Disable 1h = Enable
29	LOCK2_EN	R/W	0h	Lock 2 (Abnormal BEMF) Enable 0h = Disable 1h = Enable
28	LOCK3_EN	R/W	0h	Lock 3 (No Motor) Enable 0h = Disable 1h = Enable
27-25	LOCK_ABN_SPEED	R/W	0h	Abnormal speed lock threshold (% of MAX_SPEED) 0h = 130% 1h = 140% 2h = 150% 3h = 160% 4h = 170% 5h = 180% 6h = 190% 7h = 200%
24-22	ABNORMAL_BEMF_THR	R/W	0h	Abnormal BEMF lock threshold (% of expected BEMF) 0h = 40% 1h = 45% 2h = 50% 3h = 55% 4h = 60% 5h = 65% 6h = 67.5% 7h = 70%

表 7-32. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-19	NO_MTR_THR	R/W	0h	No motor lock threshold (A) 0h = 0.03125 A 1h = 0.0468 A 2h = 0.0625A 3h = 0.078 A 4h = 0.156 A 5h = 0.312 A 6h = 0.468 A 7h = 0.625 A
18-15	HW_LOCK_ILIMIT_MODE	R/W	0h	Hardware Lock Detection current mode 0h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode 2h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON) 3h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode 6h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high side brake mode (All high side FETs are turned ON) 7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON) 8h = Hardware ILIMIT lock detection is in report only but no action is taken 9h = Hardware ILIMIT lock detection is disabled Ah = Hardware ILIMIT lock detection is disabled Bh = Hardware ILIMIT lock detection is disabled Ch = Hardware ILIMIT lock detection is disabled Dh = Hardware ILIMIT lock detection is disabled Eh = Hardware ILIMIT lock detection is disabled Fh = Hardware ILIMIT lock detection is disabled
14-12	HW_LOCK_ILIMIT_DEG	R/W	0h	Hardware Lock Detection current limit deglitch time (Bit Number 11 is reserved 0h = No Deglitch 1h = 1 us 2h = 2 us 3h = 3 us 4h = 4 us 5h = 5 us 6h = 6 us 7h = 7 us
11	RESERVED	R/W	0h	Reserved

表 7-32. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	MIN_VM_MOTOR	R/W	0h	Minimum voltage for running motor (V) 0h = No Limit 1h = 4.5 V 2h = 5 V 3h = 5.5 V 4h = 6 V 5h = 7.5 V 6h = 10 V 7h = 12.5 V
7	MIN_VM_MODE	R/W	0h	Undervoltage Fault Recovery Mode 0h = Latch on Undervoltage 1h = Automatic clear if voltage in bounds
6-4	MAX_VM_MOTOR	R/W	0h	Maximum voltage for running motor 0h = No Limit 1h = 20 V 2h = 22.5 V 3h = 25 V 4h = 27.5 V 5h = 30 V 6h = 32.5 V 7h = 35 V
3	MAX_VM_MODE	R/W	0h	Overvoltage Fault Recovery Mode 0h = Latch on Overvoltage 1h = Automatic clear if voltage in bounds
2-0	AUTO_RETRY_TIMES	R/W	0h	Automatic retry attempts 0h = No Limit 1h = 2 2h = 3 3h = 5 4h = 7 5h = 10 6h = 15 7h = 20

7.7.3 Hardware_Configuration Registers

表 7-33 lists the memory-mapped registers for the Hardware_Configuration registers. All register offset addresses not listed in 表 7-33 should be considered as reserved locations and the register contents should not be modified.

表 7-33. HARDWARE_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
A4h	PIN_CONFIG	Hardware Pin Configuration	PIN_CONFIG Register (Offset = A4h) [Reset = X]
A6h	DEVICE_CONFIG1	Device configuration1	DEVICE_CONFIG1 Register (Offset = A6h) [Reset = X]
A8h	DEVICE_CONFIG2	Device configuration2	DEVICE_CONFIG2 Register (Offset = A8h) [Reset = 00000000h]
AAh	PERI_CONFIG1	Peripheral Configuration1	PERI_CONFIG1 Register (Offset = AAh) [Reset = 40000000h]
ACh	GD_CONFIG1	Gate Driver Configuration1	GD_CONFIG1 Register (Offset = ACh) [Reset = 10228100h]
AEh	GD_CONFIG2	Gate Driver Configuration2	GD_CONFIG2 Register (Offset = AEh) [Reset = 01200000h]

Complex bit access types are encoded to fit into small table cells. 表 7-34 shows the codes that are used for access types in this section.

表 7-34. Hardware_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

7.7.3.1 PIN_CONFIG Register (Offset = A4h) [Reset = X]

PIN_CONFIG is shown in 図 7-75 and described in 表 7-35.

Return to the Summary Table.

Register to configure hardware pins

図 7-75. PIN_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED			VDC_FILT_DIS	RESERVED		
R/W-0h	R/W-0h			R/W-0h	R/W-X		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			RESERVED		FG_IDLE_CONFIG		FG_FAULT_CONFIG
R/W-X			R/W-0h		R/W-0h		R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FG_FAULT_CONFIG	ALARM_PIN_EN	BRAKE_PIN_MODE	ALIGN_BRAKE_ANGLE_SEL	BRAKE_INPUT		SPEED_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

表 7-35. PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-28	RESERVED	R/W	0h	Reserved
27	VDC_FILT_DIS	R/W	0h	Vdc filter disable 0h = Enable 1h = Disable
26-13	RESERVED	R/W	X	Reserved
12-11	RESERVED	R/W	0h	Reserved
10-9	FG_IDLE_CONFIG	R/W	0h	FG Configuration During Stop 0h = FG continues and end state not defined, provided FG_CONFIG (defining FG during coasting) 1h = FG is pulled High 2h = FG is pulled Low 3h = FG is pulled High
8-7	FG_FAULT_CONFIG	R/W	0h	FG Configuration During Fault 0h = Use last FG state when motor was driven 1h = FG is pulled High 2h = FG is pulled Low 3h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR if FG_CONFIG set to 1b
6	ALARM_PIN_EN	R/W	0h	Alarm Pin Enable 0h = Disable 1h = Enable
5	BRAKE_PIN_MODE	R/W	0h	Brake Pin Mode 0h = Low side Brake 1h = Align Brake
4	ALIGN_BRAKE_ANGLE_SEL	R/W	0h	Align Brake Angle Select 0h = Use last commutation angle before entering align braking 1h = Use ALIGN_ANGLE configuration for align braking

表 7-35. PIN_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	BRAKE_INPUT	R/W	0h	Brake pin override 0h = Hardware Pin BRAKE 1h = Override pin and brake / align according to BRAKE_PIN_MODE 2h = Override pin and do not brake / align 3h = Hardware Pin BRAKE
1-0	SPEED_MODE	R/W	0h	Configure Speed Ctrl mode from Speed pin 0h = Analog mode 1h = PWM mode 2h = 0x2 3h = Frequency mode

7.7.3.2 DEVICE_CONFIG1 Register (Offset = A6h) [Reset = X]

DEVICE_CONFIG1 is shown in 図 7-76 and described in 表 7-36.

Return to the Summary Table.

Register to configure device

図 7-76. DEVICE_CONFIG1 Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	PIN_38_CONFIG		PIN_36_37_CONFIG	I2C_SLAVE_ADDR		
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-X		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
I2C_SLAVE_ADDR				RESERVED			
R/W-X				R/W-X			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-X							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RESERVED			BUS_VOLT	
R/W-X			R/W-0h			R/W-0h	

表 7-36. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	RESERVED	R/W	0h	Reserved
29-28	PIN_38_CONFIG	R/W	0h	Pin 38 configuration 0h = DACOUT2 1h = SOA 2h = SOB 3h = SOC
27	PIN_36_37_CONFIG	R/W	0h	Pin 36 and Pin 37 configuration 0h = Reserved 1h = Pin 36 as DACOUT1 and Pin 37 as DACOUT2
26-20	I2C_SLAVE_ADDR	R/W	X	I2C slave address
19-5	RESERVED	R/W	X	Reserved
4-2	RESERVED	R/W	0h	Reserved
1-0	BUS_VOLT	R/W	0h	Maximum Bus Voltage Configuration 0h = 15 V 1h = 30 V 2h = 60 V 3h = Not defined

7.7.3.3 DEVICE_CONFIG2 Register (Offset = A8h) [Reset = 00000000h]

DEVICE_CONFIG2 is shown in 図 7-77 and described in 表 7-37.

Return to the Summary Table.

Register to configure device

図 7-77. DEVICE_CONFIG2 Register

31	30	29	28	27	26	25	24
RESERVED	INPUT_MAXIMUM_FREQ						
R/W-0h	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INPUT_MAXIMUM_FREQ							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SLEEP_ENTRY_TIME		DYNAMIC_CSA_GAIN_EN	DYNAMIC_VOLTAGE_GAIN_EN	DEV_MODE	CLK_SEL		EXT_CLK_EN
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXT_CLK_CONFIG			EXT_WDT_EN	EXT_WDT_CONFIG		EXT_WDT_INPUT_MODE	EXT_WDT_FAULT_MODE
R/W-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h

表 7-37. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-16	INPUT_MAXIMUM_FREQ	R/W	0h	Input frequency on speed pin for speed control mode as "controlled by frequency speed pin input" that corresponds to 100% duty cycle. Input duty cycle = Input frequency / INPUT_MAXIMUM_FREQ
15-14	SLEEP_ENTRY_TIME	R/W	0h	Device enters sleep mode when speed input is held continuously below the speed threshold for SLEEP_ENTRY_TIME 0h = Sleep Entry when SPEED pin remains low for 50μs 1h = Sleep Entry when SPEED pin remains low for 200μs 2h = Sleep Entry when SPEED pin remains low for 20ms 3h = Sleep Entry when SPEED pin remains low for 200ms
13	DYNAMIC_CSA_GAIN_EN	R/W	0h	Adjust CSA gain at 1ms rate for optimal current resolution at all current levels 0h = Disable 1h = Enable
12	DYNAMIC_VOLTAGE_GAIN_EN	R/W	0h	Adjust voltage gain at 1ms rate for optimal voltage resolution at all voltage levels 0h = Dynamic Voltage Gain is Disabled 1h = Dynamic Voltage Gain is Enabled
11	DEV_MODE	R/W	0h	Device mode select 0h = Standby Mode 1h = Sleep Mode
10-9	CLK_SEL	R/W	0h	Clock Source 0h = Internal Oscillator 1h = Crude Oscillator -- WDT 2h = Reserved 3h = External Clock input
8	EXT_CLK_EN	R/W	0h	Enable External Clock mode 0h = Disable 1h = Enable

表 7-37. DEVICE_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	EXT_CLK_CONFIG	R/W	0h	External Clock Configuration 0h = 8 kHz 1h = 16 kHz 2h = 32 kHz 3h = 64 kHz 4h = 128 kHz 5h = 256 kHz 6h = 512 kHz 7h = 1024 kHz
4	EXT_WDT_EN	R/W	0h	Enable external Watch Dog 0h = Disable 1h = Enable
3-2	EXT_WDT_CONFIG	R/W	0h	Time between watchdog tickles 0h = 100ms (GPIO), 1s (I2C) 1h = 200ms (GPIO), 2s (I2C) 2h = 500ms (GPIO), 5s (I2C) 3h = 1000ms (GPIO), 10s (I2C)
1	EXT_WDT_INPUT_MODE	R/W	0h	External Watchdog input mode 0h = Watchdog tickle over I2C 1h = Watchdog tickle over GPIO
0	EXT_WDT_FAULT_MODE	R/W	0h	External Watchdog fault mode 0h = Report Only 1h = Latch with Hi-z

7.7.3.4 PERI_CONFIG1 Register (Offset = AAh) [Reset = 40000000h]

PERI_CONFIG1 is shown in 図 7-78 and described in 表 7-38.

Return to the Summary Table.

Register to peripheral1

図 7-78. PERI_CONFIG1 Register

31	30	29	28	27	26	25	24
RESERVED	SPREAD_SPECTRUM_MODULATION_DIS	RESERVED				BUS_CURRENT_LIMIT	
R/W-0h	R/W-1h	R/W-0h				R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BUS_CURRENT_LIMIT		BUS_CURRENT_LIMIT_ENABLE	DIR_INPUT		DIR_CHANGE_MODE	SELF_TEST_ENABLE	ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY
R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY			ACTIVE_BRAKE_MOD_INDEX_LIMIT			SPEED_RANGE_SEL	RESERVED
R/W-0h			R/W-0h			R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

表 7-38. PERI_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	SPREAD_SPECTRUM_MODULATION_DIS	R/W	1h	Spread Spectrum Modulation Disable 0h = SSM is Enabled 1h = SSM is Disabled
29-26	RESERVED	R/W	0h	Reserved
25-22	BUS_CURRENT_LIMIT	R/W	0h	Bus Current Limit (A) 0h = 0.078125 A 1h = 0.15625 A 2h = 0.3125 A 3h = 0.625 A 4h = 0.9375 A 5h = 1.25 A 6h = 1.5625 A 7h = 1.875 A 8h = 2.1875 A 9h = 2.5 A Ah = 2.8125 A Bh = 3.125 A Ch = 3.4375 A Dh = 3.75 A Eh = Reserved Fh = Reserved
21	BUS_CURRENT_LIMIT_ENABLE	R/W	0h	Bus Current Limit Enable 0h = Disable 1h = Enable

表 7-38. PERI_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-19	DIR_INPUT	R/W	0h	DIR pin override 0h = Hardware Pin DIR 1h = Override DIR pin with clockwise rotation OUTA-OUTB-OUTC 2h = Override DIR pin with counter clockwise rotation OUTA-OUTC-OUTB 3h = Hardware Pin DIR
18	DIR_CHANGE_MODE	R/W	0h	Response to change of DIR pin status 0h = Follow motor stop options and ISD routine on detecting DIR change 1h = Change the direction through Reverse Drive while continuously driving the motor
17	SELF_TEST_ENABLE	R/W	0h	Enables self test on power up 0h = STL is disabled 1h = STL is enabled
16-13	ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY	R/W	0h	Difference between final speed and present speed below which active braking will be applied 0h = reserved 1h = 5% 2h = 10% 3h = 15% 4h = 20% 5h = 25% 6h = 30% 7h = 35% 8h = 40% 9h = 45% Ah = 50% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%
12-10	ACTIVE_BRAKE_MOD_INDEX_LIMIT	R/W	0h	Modulation Index limit beyond which active braking will be applied 0h = 0% 1h = 40% 2h = 50% 3h = 60% 4h = 70% 5h = 80% 6h = 90% 7h = 100%
9	SPEED_RANGE_SEL	R/W	0h	Speed range selection for digital speed (PWM Duty or Frequency to speed mode) 0h = 325Hz to 100kHz 1h = 10Hz to 325Hz
8	RESERVED	R/W	0h	Reserved
7-0	RESERVED	R/W	0h	Reserved

7.7.3.5 GD_CONFIG1 Register (Offset = ACh) [Reset = 10228100h]

GD_CONFIG1 is shown in 図 7-79 and described in 表 7-39.

Return to the Summary Table.

Register to configure gated driver settings1

図 7-79. GD_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED		RESERVED	SLEW_RATE		RESERVED	
R/W-0h	R/W-0h		R/W-1h	R/W-0h		R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLR_FLT	RESERVED	RESERVED	RESERVED	OVP_SEL	OVP_EN	RESERVED	OTW_REP
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	RESERVED	OCP_DEG		TRETRY	OCP_LVL	OCP_MODE	
R/W-1h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CSA_GAIN	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

表 7-39. GD_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	RESERVED	R/W	0h	Reserved
28	RESERVED	R/W	1h	Reserved
27-26	SLEW_RATE	R/W	0h	Slew Rate Settings 0h = Slew rate is 25 V/µs 1h = Slew rate is 50 V/µs 2h = Slew rate is 125 V/µs 3h = Slew rate is 200 V/µs
25-24	RESERVED	R/W	0h	Reserved
23	CLR_FLT	R/W	0h	Clear Fault 0h = No clear faualt command is issued 1h = To clear the latched fault bits. This bit automatically resets after being written.
22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	1h	Reserved
20	RESERVED	R/W	0h	Reserved
19	OVP_SEL	R/W	0h	Overvoltage Level Setting 0h = VM overvoltage level is 32-V 1h = VM overvoltage level is 20-V
18	OVP_EN	R/W	0h	Overvoltage Enable Bit 0h = Overvoltage protection is disabled 1h = Overvoltage protection is enabled
17	RESERVED	R/W	1h	Reserved
16	OTW_REP	R/W	0h	Overtemperature Warning Reporting Bit 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled
15	RESERVED	R/W	1h	Reserved
14	RESERVED	R/W	0h	Reserved

表 7-39. GD_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	OCP_DEG	R/W	0h	OCP Deglitch Time Settings 0h = OCP deglitch time is 0.2 µs 1h = OCP deglitch time is 0.6 µs 2h = OCP deglitch time is 1.2 µs 3h = OCP deglitch time is 1.6 µs
11	TRETRY	R/W	0h	OCP Retry Time Settings 0h = OCP retry time is 5 ms 1h = OCP retry time is 500 ms
10	OCP_LVL	R/W	0h	Overcurrent Level Setting 0h = OCP level is 9 A (Typical) 1h = OCP level is 13 A (Typical)
9-8	OCP_MODE	R/W	1h	OCP Fault Options 0h = Overcurrent causes a latched fault 1h = Overcurrent causes an automatic retrying fault 2h = Overcurrent is report only but no action is taken 3h = Overcurrent is not reported and no action is taken
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1-0	CSA_GAIN	R/W	0h	Current Sense Amplifier's Gain Settings (Used only if DYNAMIC_CSA_GAIN_EN = 0) 0h = CSA gain is 0.24 V/A 1h = CSA gain is 0.48 V/A 2h = CSA gain is 0.96 V/A 3h = CSA gain is 1.92 V/A

7.7.3.6 GD_CONFIG2 Register (Offset = AEh) [Reset = 01200000h]

GD_CONFIG2 is shown in 図 7-80 and described in 表 7-40.

Return to the Summary Table.

Register to configure gated driver settings2

図 7-80. GD_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	DELAY_COMP_EN	TARGET_DELAY				RESERVED	BUCK_PS_DIS
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W1C-1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BUCK_CL	BUCK_SEL		RESERVED	RESERVED			
R/W-0h	R/W-1h		R/W-0h	R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

表 7-40. GD_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	DELAY_COMP_EN	R/W	0h	Driver Delay Compensation enable 0h = Disable 1h = Enable
29-26	TARGET_DELAY	R/W	0h	0h = Automatic based on slew rate 1h = 0.4 us 2h = 0.6 us 3h = 0.8 us 4h = 1 us 5h = 1.2 us 6h = 1.4 us 7h = 1.6 us 8h = 1.8 us 9h = 2 us Ah = 2.2 us Bh = 2.4 us Ch = 2.6 us Dh = 2.8 us Eh = 3 us Fh = 3.2 us
25	RESERVED	R/W	0h	Reserved
24	BUCK_PS_DIS	R/W1C	1h	Buck Power Sequencing Disable Bit 0h = Buck power sequencing is enabled 1h = Buck power sequencing is disabled
23	BUCK_CL	R/W	0h	Buck Current Limit Setting 0h = Buck regulator current limit is set to 600 mA 1h = Buck regulator current limit is set to 150 mA
22-21	BUCK_SEL	R/W	1h	Buck Voltage Selection 0h = Buck voltage is 3.3 V 1h = Buck voltage is 5.0 V 2h = Buck voltage is 4.0 V 3h = Buck voltage is 5.7 V

表 7-40. GD_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	RESERVED	R/W	0h	Reserved
19-0	RESERVED	R/W	0h	Reserved

7.7.4 Internal_Algorithm_Configuration Registers

表 7-41 lists the memory-mapped registers for the Internal_Algorithm_Configuration registers. All register offset addresses not listed in 表 7-41 should be considered as reserved locations and the register contents should not be modified.

表 7-41. INTERNAL_ALGORITHM_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
A0h	INT_ALGO_1	Internal Algorithm Configuration1	INT_ALGO_1 Register (Offset = A0h) [Reset = 00000000h]
A2h	INT_ALGO_2	Internal Algorithm Configuration2	INT_ALGO_2 Register (Offset = A2h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. 表 7-42 shows the codes that are used for access types in this section.

表 7-42. Internal_Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.4.1 INT_ALGO_1 Register (Offset = A0h) [Reset = 00000000h]

INT_ALGO_1 is shown in 図 7-81 and described in 表 7-43.

Return to the Summary Table.

Register to configure internal algorithm parameters1

図 7-81. INT_ALGO_1 Register

31	30	29	28	27	26	25	24
RESERVED	ACTIVE_BRAKE_SPEED__DELTA_LIMIT_EXIT		SPEED_PIN_GLITCH_FILTER		FAST_ISD_EN	ISD_STOP_TIME	
R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISD_RUN_TIME		ISD_TIMEOUT		AUTO_HANDOFF_MIN_BEMF			BRAKE_CURRENT_PERSIST
R/W-0h		R/W-0h		R/W-0h			R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BRAKE_CURRENT_PERSIST	MPET_IPD_CURRENT_LIMIT		MPET_IPD_FREQ		MPET_OPEN_LOOP_CURRENT_REF		
R/W-0h	R/W-0h		R/W-0h		R/W-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPET_OPEN_LOOP_SPEED_REF		MPET_OPEN_LOOP_SLEW_RATE			REV_DRV_OPEN_LOOP_DEC		
R/W-0h		R/W-0h			R/W-0h		

表 7-43. INT_ALGO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-29	ACTIVE_BRAKE_SPEED__DELTA_LIMIT_EXIT	R/W	0h	Difference between final speed and present speed below which active braking will be stopped 0h = 2.5% 1h = 5% 2h = 7.5% 3h = 10%
28-27	SPEED_PIN_GLITCH_FILTER	R/W	0h	Glitch filter applied on speed pin input 0h = No Glitch Filter 1h = 0.2 μs 2h = 0.5 μs 3h = 1.0 μs
26	FAST_ISD_EN	R/W	0h	Enable fast speed detection 0h = Disable Fast ISD 1h = Enable Fast ISD
25-24	ISD_STOP_TIME	R/W	0h	Persistence time for declaring motor has stopped 0h = 1 ms 1h = 5 ms 2h = 50 ms 3h = 100 ms
23-22	ISD_RUN_TIME	R/W	0h	Persistence time for declaring motor is running 0h = 1 ms 1h = 5 ms 2h = 50 ms 3h = 100 ms

表 7-43. INT_ALGO_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	ISD_TIMEOUT	R/W	0h	Timeout in case ISD is unable to reliably detect speed or direction 0h = 500ms 1h = 750 ms 2h = 1000 ms 3h = 2000 ms
19-17	AUTO_HANDOFF_MIN_BEMF	R/W	0h	Minimum BEMF for handoff (V) 0h = 0 mV 1h = 50 mV 2h = 100 mV 3h = 250 mV 4h = 500 mV 5h = 1000 mV 6h = 1250 mV 7h = 1500 mV
16-15	BRAKE_CURRENT_PERSIST	R/W	0h	Persistence time for current below threshold during low side brake 0h = 50 ms 1h = 100 ms 2h = 250 ms 3h = 500 ms
14-13	MPET_IPD_CURRENT_LIMIT	R/W	0h	IPD current limit for MPET (A) 0h = 0.0625 A 1h = 0.3125 A 2h = 0.625 A 3h = 1.25 A
12-11	MPET_IPD_FREQ	R/W	0h	Number of times IPD is executed for MPET 0h = 1 1h = 2 2h = 4 3h = 8
10-8	MPET_OPEN_LOOP_CURRENT_REF	R/W	0h	Open Loop Current Reference (A) 0h = 0.625 A 1h = 1.25 A 2h = 1.875 A 3h = 2.5 A 4h = 3.125 A 5h = 3.75 A 6h = Reserved 7h = Reserved
7-6	MPET_OPEN_LOOP_SPEED_REF	R/W	0h	Open Loop Speed Reference for MPET (% of MAXIMUM_SPEED) 0h = 15% 1h = 25% 2h = 35% 3h = 50%
5-3	MPET_OPEN_LOOP_SLEW_RATE	R/W	0h	Open Loop Slew Rate for MPET (Hz/s) 0h = 0.1 Hz/s 1h = 0.5 Hz/s 2h = 1 Hz/s 3h = 2 Hz/s 4h = 3 Hz/s 5h = 5 Hz/s 6h = 10 Hz/s 7h = 20 Hz/s

表 7-43. INT_ALGO_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	REV_DRV_OPEN_LOOP_DEC	R/W	0h	% of open loop acceleration to be applied during open loop deceleration in reverse drive 0h = 50% 1h = 60% 2h = 70% 3h = 80% 4h = 90% 5h = 100% 6h = 125% 7h = 150%

7.7.4.2 INT_ALGO_2 Register (Offset = A2h) [Reset = 00000000h]

INT_ALGO_2 is shown in 図 7-82 and described in 表 7-44.

Return to the Summary Table.

Register to configure internal algorithm parameters2

図 7-82. INT_ALGO_2 Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R/W-0h	R/W-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CL_SLOW_ACC	
R/W-0h						R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CL_SLOW_ACC		ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE			MPET_IPD_SELECT	MPET_KE_MEAS_PARAMETER_SELECT	IPD_HIGH_RESOLUTION_EN
R/W-0h		R/W-0h			R/W-0h	R/W-0h	R/W-0h

表 7-44. INT_ALGO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-10	RESERVED	R/W	0h	Reserved
9-6	CL_SLOW_ACC	R/W	0h	Close loop acceleration when estimator is not yet fully aligned (Hz / sec) 0h = 0.1 Hz/s 1h = 1 Hz/s 2h = 2 Hz/s 3h = 3 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 20 Hz/s 7h = 30 Hz/s 8h = 40 Hz/s 9h = 50 Hz/s Ah = 100 Hz/s Bh = 200 Hz/s Ch = 500 Hz/s Dh = 750 Hz/s Eh = 1000 Hz/s Fh = 2000 Hz/s
5-3	ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE	R/W	0h	Bus Current slew rate during active braking (A/s) 0h = 10 A/s 1h = 50 A/s 2h = 100 A/s 3h = 250 A/s 4h = 500 A/s 5h = 1000 A/s 6h = 5000 A/s 7h = No Limit

表 7-44. INT_ALGO_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MPET_IPD_SELECT	R/W	0h	Selection between MPET_IPD_CURRENT_LIMIT for IPD current limit, MPET_IPD_FREQ for IPD Repeat OR IPD_CURR_THR for IPD current limit, IPD_REPEAT for IPD Repeat 0h = Configured parameters for normal motor operation 1h = MPET specific parameters
1	MPET_KE_MEAS_PARAMETER_SELECT	R/W	0h	Selection between MPET_OPEN_LOOP_SLEW_RATE for slew rate, MPET_OPEN_LOOP_CURR_REF for current reference, MPET_OPEN_LOOP_SPEED_REF for speed reference OR OL_ACC_A1, OL_ACC_A2 for slew rate, open loop current reference for current reference and open to closed loop speed threshold for speed reference 0h = Configured parameters for normal motor operation 1h = MPET specific parameters
0	IPD_HIGH_RESOLUTION_EN	R/W	0h	IPD high resolution enable 0h = Disable 1h = Enable

7.8 RAM (Volatile) Register Map

7.8.1 Fault_Status Registers

表 7-45 lists the memory-mapped registers for the Fault_Status registers. All register offset addresses not listed in 表 7-45 should be considered as reserved locations and the register contents should not be modified.

表 7-45. FAULT_STATUS Registers

Offset	Acronym	Register Name	Section
E0h	GATE_DRIVER_FAULT_STATUS	Fault Status Register	GATE_DRIVER_FAULT_STATUS Register (Offset = E0h) [Reset = 00000000h]
E2h	CONTROLLER_FAULT_STATUS	Fault Status Register	CONTROLLER_FAULT_STATUS Register (Offset = E2h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. 表 7-46 shows the codes that are used for access types in this section.

表 7-46. Fault_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-*n*		Value after reset or the default value

7.8.1.1 GATE_DRIVER_FAULT_STATUS Register (Offset = E0h) [Reset = 00000000h]

GATE_DRIVER_FAULT_STATUS is shown in 図 7-83 and described in 表 7-47.

Return to the Summary Table.

Status of various gate driver faults

図 7-83. GATE_DRIVER_FAULT_STATUS Register

31	30	29	28	27	26	25	24
DRIVER_FAULT	BK_FLT	RESERVED	OCP	NPOR	OVP	OT	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OTW	OTS	OCP_HC	OCP_LC	OCP_HB	OCP_LB	OCP_HA	OCP_LA
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	OTP_ERR	BUCK_OCP	BUCK_UV	VCP_UV	RESERVED		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

表 7-47. GATE_DRIVER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRIVER_FAULT	R	0h	Logic OR of FAULT status registers. Mirrors nFAULT pin.
30	BK_FLT	R	0h	Buck Fault Bit 0h = No buck regulator fault condition is detected 1h = Buck regulator fault condition is detected
29	RESERVED	R	0h	Reserved
28	OCP	R	0h	Over Current Protection Status Bit 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
27	NPOR	R	0h	Supply Power On Reset Bit 0h = Power on reset condition is detected on VM 1h = No power-on-reset condition is detected on VM
26	OVP	R	0h	Supply Overvoltage Protection Status Bit 0h = No overvoltage condition is detected on VM 1h = Overvoltage condition is detected on VM
25	OT	R	0h	Overtemperature Fault Status Bit 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
24	RESERVED	R	0h	Reserved
23	OTW	R	0h	Overtemperature Warning Status Bit 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
22	OTS	R	0h	Overtemperature Shutdown Status Bit 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected
21	OCP_HC	R	0h	Overcurrent Status on High-side switch of OUTC 0h = No overcurrent detected on high-side switch of OUTC 1h = Overcurrent detected on high-side switch of OUTC
20	OCP_LC	R	0h	Overcurrent Status on Low-side switch of OUTC 0h = No overcurrent detected on low-side switch of OUTC 1h = Overcurrent detected on low-side switch of OUTC

表 7-47. GATE_DRIVER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	OCP_HB	R	0h	Overcurrent Status on High-side switch of OUTB 0h = No overcurrent detected on high-side switch of OUTB 1h = Overcurrent detected on high-side switch of OUTB
18	OCP_LB	R	0h	Overcurrent Status on Low-side switch of OUTB 0h = No overcurrent detected on low-side switch of OUTB 1h = Overcurrent detected on low-side switch of OUTB
17	OCP_HA	R	0h	Overcurrent Status on High-side switch of OUTA 0h = No overcurrent detected on high-side switch of OUTA 1h = Overcurrent detected on high-side switch of OUTA
16	OCP_LA	R	0h	Overcurrent Status on Low-side switch of OUTA 0h = No overcurrent detected on low-side switch of OUTA 1h = Overcurrent detected on low-side switch of OUTA
15	RESERVED	R	0h	Reserved
14	OTP_ERR	R	0h	OTP Error 0h = No OTP error is detected 1h = OTP Error is detected
13	BUCK_OCP	R	0h	Buck Regulator Overcurrent Status Bit 0h = No buck regulator overcurrent is detected 1h = Buck regulator overcurrent is detected
12	BUCK_UV	R	0h	Buck Regulator Undervoltage Status Bit 0h = No buck regulator undervoltage is detected 1h = Buck regulator undervoltage is detected
11	VCP_UV	R	0h	Charge Pump Undervoltage Status Bit 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
10-0	RESERVED	R	0h	Reserved

7.8.1.2 CONTROLLER_FAULT_STATUS Register (Offset = E2h) [Reset = 00000000h]

CONTROLLER_FAULT_STATUS is shown in 図 7-84 and described in 表 7-48.

Return to the Summary Table.

Status of various controller faults

図 7-84. CONTROLLER_FAULT_STATUS Register

31	30	29	28	27	26	25	24
CONTROLLER_FAULT	OTW_MCE	IPD_FREQ_FAULT	IPD_T1_FAULT	IPD_T2_FAULT	BUS_CURRENT_LIMIT_STATUS	MPET_IPD_FAULT	MPET_BEMF_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ABN_SPEED	ABN_BEMF	NO_MTR	MTR_LCK	LOCK_LIMIT	HW_LOCK_LIMIT	MTR_UNDER_VOLTAGE	MTR_OVER_VOLTAGE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SPEED_LOOP_SATURATION	CURRENT_LOOP_SATURATION	RESERVED					
R-0h	R-0h	R-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				WATCHDOG_FAULT	STL_ENABLE_STATUS	STL_STATUS	APP_RESET
R-0h				R-0h	R-0h	R-0h	R-0h

表 7-48. CONTROLLER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CONTROLLER_FAULT	R	0h	Logic OR of Controller FAULT status registers
30	OTW_MCE	R	0h	Indicates overtemperature MCE
29	IPD_FREQ_FAULT	R	0h	Indicates IPD frequency fault
28	IPD_T1_FAULT	R	0h	Indicates IPD T1 fault
27	IPD_T2_FAULT	R	0h	Indicates IPD T2 fault
26	BUS_CURRENT_LIMIT_STATUS	R	0h	Indicates status of Bus Current limit
25	MPET_IPD_FAULT	R	0h	Indicates error during resistance and inductance measurement
24	MPET_BEMF_FAULT	R	0h	Indicates error during BEMF constant measurement
23	ABN_SPEED	R	0h	Indicates Abnormal speed motor lock condition
22	ABN_BEMF	R	0h	Indicates Abnormal BEMF motor lock condition
21	NO_MTR	R	0h	Indicates No Motor fault
20	MTR_LCK	R	0h	Indicates when one of the motor lock is triggered
19	LOCK_LIMIT	R	0h	Indicates Lock Ilimit fault
18	HW_LOCK_LIMIT	R	0h	Indicates Hardware Lock Ilimit fault
17	MTR_UNDER_VOLTAGE	R	0h	Indicates Motor Undervoltage fault
16	MTR_OVER_VOLTAGE	R	0h	Indicates Motor Over voltage fault
15	SPEED_LOOP_SATURATION	R	0h	Indicates speed loop saturation
14	CURRENT_LOOP_SATURATION	R	0h	Indicates current loop saturation
13-4	RESERVED	R	0h	Reserved

表 7-48. CONTROLLER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	WATCHDOG_FAULT	R	0h	indicates Watchdog fault
2	STL_ENABLE_STATUS	R	0h	STL Enable Status
1	STL_STATUS	R	0h	STL Status
0	APP_RESET	R	0h	App Reset

7.8.2 System_Status Registers

表 7-49 lists the memory-mapped registers for the System_Status registers. All register offset addresses not listed in 表 7-49 should be considered as reserved locations and the register contents should not be modified.

表 7-49. SYSTEM_STATUS Registers

Offset	Acronym	Register Name	Section
E4h	ALGO_STATUS	System Status Register	ALGO_STATUS Register (Offset = E4h) [Reset = 00000000h]
E6h	MTR_PARAMS	System Status Register	MTR_PARAMS Register (Offset = E6h) [Reset = 00000000h]
E8h	ALGO_STATUS_MPET	System Status Register	ALGO_STATUS_MPET Register (Offset = E8h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. 表 7-50 shows the codes that are used for access types in this section.

表 7-50. System_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.2.1 ALGO_STATUS Register (Offset = E4h) [Reset = 00000000h]

ALGO_STATUS is shown in 図 7-85 and described in 表 7-51.

Return to the Summary Table.

Status of various system and algorithm parameters

図 7-85. ALGO_STATUS Register

31	30	29	28	27	26	25	24
VOLT_MAG							
R-0h							
23	22	21	20	19	18	17	16
VOLT_MAG							
R-0h							
15	14	13	12	11	10	9	8
DUTY_CMD							
R-0h							
7	6	5	4	3	2	1	0
DUTY_CMD				SYS_INIT_DONE	SYS_ENABLE_FLAG	RESERVED	
R-0h				R-0h	R-0h	R-0h	

表 7-51. ALGO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VOLT_MAG	R	0h	16-bit value indicating applied voltage magnitude. Voltage magnitude applied = VOLT_MAG * 100 / 32768 %
15-4	DUTY_CMD	R	0h	12-bit value indicating decoded speed command in PWM/Analog mode DUTY_CMD (%) = DUTY_CMD/4096 * 100%.
3	SYS_INIT_DONE	R	0h	1 indicates device is ready for GUI control 0 indicates firmware is still copying EEPROM to shadow memory
2	SYS_ENABLE_FLAG	R	0h	1 indicates GUI can control the register 0 indicates GUI is still copying default parameters from shadow memory
1-0	RESERVED	R	0h	Reserved

7.8.2.2 MTR_PARAMS Register (Offset = E6h) [Reset = 00000000h]

MTR_PARAMS is shown in 図 7-86 and described in 表 7-52.

Return to the Summary Table.

Status of various motor parameters

図 7-86. MTR_PARAMS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOTOR_R								MOTOR_BEMF_CONST							
R-0h								R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MOTOR_L								RESERVED							
R-0h								R-0h							

表 7-52. MTR_PARAMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MOTOR_R	R	0h	8-bit value indicating measured Motor Resistance
23-16	MOTOR_BEMF_CONST	R	0h	8-bit value indicating measured BEMF constant
15-8	MOTOR_L	R	0h	8-bit value indicating measured Motor Inductance
7-0	RESERVED	R	0h	Reserved

7.8.2.3 ALGO_STATUS_MPET Register (Offset = E8h) [Reset = 00000000h]

ALGO_STATUS_MPET is shown in 図 7-87 and described in 表 7-53.

Return to the Summary Table.

Status of various MPET parameters

図 7-87. ALGO_STATUS_MPET Register

31	30	29	28	27	26	25	24
MPET_R_STATUS	MPET_L_STATUS	MPET_KE_STATUS	MPET_MECH_STATUS	MPET_PWM_FREQ			
R-0h	R-0h	R-0h	R-0h	R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

表 7-53. ALGO_STATUS_MPET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MPET_R_STATUS	R	0h	Indicates status of Resistance measurement
30	MPET_L_STATUS	R	0h	Indicates status of Inductance measurement
29	MPET_KE_STATUS	R	0h	Indicates status of BEMF constant measurement
28	MPET_MECH_STATUS	R	0h	Indicates status of mechanical parameter measurement
27-24	MPET_PWM_FREQ	R	0h	4-bit value indicating PWM frequency used during BEMF constant measurement
23-0	RESERVED	R	0h	Reserved

7.8.3 Device_Control Registers

表 7-54 lists the memory-mapped registers for the Device_Control registers. All register offset addresses not listed in 表 7-54 should be considered as reserved locations and the register contents should not be modified.

表 7-54. DEVICE_CONTROL Registers

Offset	Acronym	Register Name	Section
EAh	ALGO_CTRL1	Device Control Register	ALGO_CTRL1 Register (Offset = EAh) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. 表 7-55 shows the codes that are used for access types in this section.

表 7-55. Device_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

表 7-55. Device_Control Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

7.8.3.1 ALGO_CTRL1 Register (Offset = EAh) [Reset = 00000000h]

ALGO_CTRL1 is shown in 図 7-88 and described in 表 7-56.

Return to the Summary Table.

Control settings

図 7-88. ALGO_CTRL1 Register

31	30	29	28	27	26	25	24
EEPROM_WRT	EEPROM_READ	CLR_FLT	CLR_FLT_RETRY_COUNT	RESERVED			
R/W-0h	R/W-0h	W-0h	W-0h	W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				FORCED_ALIGN_ANGLE			
W-0h				W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCED_ALIGN_ANGLE					WATCHDOG_TICKLE	RESERVED	
W-0h					R/W-0h	W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
W-0h							

表 7-56. ALGO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EEPROM_WRT	R/W	0h	Write the configuration to EEPROM
30	EEPROM_READ	R/W	0h	Read the default configuration from EEPROM
29	CLR_FLT	W	0h	Clears all faults
28	CLR_FLT_RETRY_COUNT	W	0h	Clears fault retry count
27-20	RESERVED	W	0h	Reserved
19-11	FORCED_ALIGN_ANGLE	W	0h	9-bit value (in degrees) used during forced Align state (FORCE_ALIGN_EN = 1) Angle applied = FORCED_ALIGN_ANGLE % 360deg
10	WATCHDOG_TICKLE	R/W	0h	RAM bit to tickle watchdog in I2C mode. This bit should be written 1 by external controller every EXT_WDT_CFG. The MCF will reset this bit
9-0	RESERVED	W	0h	Reserved

7.8.4 Algorithm_Control Registers

表 7-57 lists the memory-mapped registers for the Algorithm_Control registers. All register offset addresses not listed in 表 7-57 should be considered as reserved locations and the register contents should not be modified.

表 7-57. ALGORITHM_CONTROL Registers

Offset	Acronym	Register Name	Section
ECh	ALGO_DEBUG1	Algorithm Control Register	ALGO_DEBUG1 Register (Offset = ECh) [Reset = 00000000h]
EEh	ALGO_DEBUG2	Algorithm Control Register	ALGO_DEBUG2 Register (Offset = EEh) [Reset = 00000000h]
F0h	CURRENT_PI	Current PI Controller used	CURRENT_PI Register (Offset = F0h) [Reset = 00000000h]

表 7-57. ALGORITHM_CONTROL Registers (continued)

Offset	Acronym	Register Name	Section
F2h	SPEED_PI	Speed PI controller used	SPEED_PI Register (Offset = F2h) [Reset = 00000000h]
F4h	DAC_1	DAC1 Control Register	DAC_1 Register (Offset = F4h) [Reset = 00110000h]
F6h	DAC_2	DAC2 Control Register	DAC_2 Register (Offset = F6h) [Reset = X]

Complex bit access types are encoded to fit into small table cells. 表 7-58 shows the codes that are used for access types in this section.

表 7-58. Algorithm_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.8.4.1 ALGO_DEBUG1 Register (Offset = ECh) [Reset = 00000000h]

ALGO_DEBUG1 is shown in 図 7-89 and described in 表 7-59.

Return to the Summary Table.

Algorithm control register for debug

図 7-89. ALGO_DEBUG1 Register

31	30	29	28	27	26	25	24
OVERRIDE	DIGITAL_SPEED_CTRL						
W-0h	W-0h						
23	22	21	20	19	18	17	16
DIGITAL_SPEED_CTRL							
W-0h							
15	14	13	12	11	10	9	8
CLOSED_LOOP_DIS	FORCE_ALIGN_EN	FORCE_SLOW_FIRST_CYCLE_EN	FORCE_IPD_EN	FORCE_ISD_EN	FORCE_ALIGN_ANGLE_SRC_SEL	FORCE_IQ_REF_SPEED_LOOP_DIS	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	
7	6	5	4	3	2	1	0
FORCE_IQ_REF_SPEED_LOOP_DIS							
W-0h							

表 7-59. ALGO_DEBUG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVERRIDE	W	0h	Use to control the SPD_CTRL bits. If OVERRIDE = '1', speed command can be written by the user through serial interface. 0h = SPEED_CMD using Analog/PWM mode 1h = SPEED_CMD using SPD_CTRL[11:0]
30-16	DIGITAL_SPEED_CTRL	W	0h	Digital Speed Control If OVERRIDE = 0b1, then SPEED_CMD is control using DIGITAL_SPEED_CTRL
15	CLOSED_LOOP_DIS	W	0h	Use to disable Closed loop 0h = Enable Closed Loop 1h = Disable Closed loop, motor commutation in open loop
14	FORCE_ALIGN_EN	W	0h	Force Align State Enable 0h = Disable Force Align state, device comes out of align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN 1h = Enable Force Align state, device stays in align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN
13	FORCE_SLOW_FIRST_CYCLE_EN	W	0h	Force Slow First Cycle Enable 0h = Disable Force Slow First Cycle state, device comes out of slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE 1h = Enable Force Slow First Cycle state, device stays in slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE
12	FORCE_IPD_EN	W	0h	Force IPD Enable 0h = Disable Force IPD state, device comes out of IPD state if MTR_STARTUP is selected as IPD 1h = Enable Force IPD state, device stays in IPD state if MTR_STARTUP is selected as IPD
11	FORCE_ISD_EN	W	0h	Force ISD enable 0h = Disable Force ISD state, device comes out of ISD state if ISD_EN is set 1h = Enable Force ISD state, device stays in ISD state if ISD_EN is set

表 7-59. ALGO_DEBUG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	FORCE_ALIGN_ANGLE_SRC_SEL	W	0h	Force Align Angle State Source Select 0h = Force Align Angle defined by ALIGN_ANGLE 1h = Force Align Angle defined by FORCED_ALIGN_ANGLE
9-0	FORCE_IQ_REF_SPEED_LOOP_DIS	W	0h	Sets IQ Ref (% of BASE_CURRENT) when speed loop is disabled If SPEED_LOOP_DIS = 0b1, then Iq_ref is control using IQ_REF_SPEED_LOOP_DIS iqRef = (FORCE_IQ_REF_SPEED_LOOP_DIS /500) * BASE_CURRENT if FORCE_IQ_REF_SPEED_LOOP_DIS < 500 (FORCE_IQ_REF_SPEED_LOOP_DIS - 1024)/500 * BASE_CURRENT if FORCE_IQ_REF_SPEED_LOOP_DIS > 512 Valid values are 0 to 500 and 512 to 1000

7.8.4.2 ALGO_DEBUG2 Register (Offset = EEh) [Reset = 00000000h]

ALGO_DEBUG2 is shown in 図 7-90 and described in 表 7-60.

Return to the Summary Table.

Algorithm control register for debug

図 7-90. ALGO_DEBUG2 Register

31	30	29	28	27	26	25	24
RESERVED	FORCE_RECIRCULATE_STOP_SECTOR			FORCE_RECIRCULATE_STOP_EN	CURRENT_LOOP_DIS	FORCE_VD_CURRENT_LOOP_DIS	
W-0h	W-0h			W-0h	W-0h	W-0h	
23	22	21	20	19	18	17	16
FORCE_VD_CURRENT_LOOP_DIS							
W-0h							
15	14	13	12	11	10	9	8
FORCE_VQ_CURRENT_LOOP_DIS							
W-0h							
7	6	5	4	3	2	1	0
FORCE_VQ_CURRENT_LOOP_DIS		MPET_CMD	MPET_R	MPET_L	MPET_KE	MPET_MECH	MPET_WRITE_SHADOW
W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

表 7-60. ALGO_DEBUG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	W	0h	Reserved
30-28	FORCE_RECIRCULATE_STOP_SECTOR	W	0h	use to do the recirculation at specific sector during force motor stop condition 0h = The last sector before stop condition 1h = Sector1 2h = Sector2 3h = Sector3 4h = Sector4 5h = Sector5 6h = Sector6 7h = The last sector before stop condition
27	FORCE_RECIRCULATE_STOP_EN	W	0h	Force recirculate stop Enable 0h = Enable Force recirculate stop 1h = Disable Force recirculate stop
26	CURRENT_LOOP_DIS	W	0h	Use to control the FORCE_VD_CURRENT_LOOP_DIS and FORCE_VQ_CURRENT_LOOP_DIS. If CURRENT_LOOP_DIS = '1', Current loop and speed loop is disabled 0h = Enable Current Loop 1h = Disable Current Loop
25-16	FORCE_VD_CURRENT_LOOP_DIS	W	0h	Sets Vd when current loop speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vd is control using FORCE_VD_CURRENT_LOOP_DIS mdRef = (FORCE_VD_CURRENT_LOOP_DIS /500) if FORCE_VD_CURRENT_LOOP_DIS < 500 - (FORCE_VD_CURRENT_LOOP_DIS - 512)/500 if FORCE_VD_CURRENT_LOOP_DIS > 512 Valid values: 0 to 500 and 512 to 1000

表 7-60. ALGO_DEBUG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-6	FORCE_VQ_CURRENT_LOOP_DIS	W	0h	Sets Vq when current loop speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vq is control using FORCE_VQ_CURRENT_LOOP_DIS mqRef = (FORCE_VQ_CURRENT_LOOP_DIS /500) if FORCE_VQ_CURRENT_LOOP_DIS < 500 - (FORCE_VQ_CURRENT_LOOP_DIS - 512)/500 if FORCE_VQ_CURRENT_LOOP_DIS > 512 Valid values: 0 to 500 and 512 to 1000
5	MPET_CMD	W	0h	Initiates motor parameter measurement routine when set to 1
4	MPET_R	W	0h	Enables motor resistance measurement during motor parameter measurement routine 0h = Disables Motor Resistance measurement during motor parameter measurement routine 1h = Enable Motor Resistance measurement during motor parameter measurement routine
3	MPET_L	W	0h	Enables motor inductance measurement during motor parameter measurement routine 0h = Disables Motor Inductance measurement during motor parameter measurement routine 1h = Enable Motor Inductance measurement during motor parameter measurement routine
2	MPET_KE	W	0h	Enables motor BEMF constant measurement during motor parameter measurement routine 0h = Disables Motor BEMF constant measurement during motor parameter measurement routine 1h = Enable Motor BEMF constant measurement during motor parameter measurement routine
1	MPET_MECH	W	0h	Enables motor mechanical parameter measurement during motor parameter measurement routine 0h = Disables Motor mechanical parameter measurement during motor parameter measurement routine 1h = Enable Motor mechanical parameter measurement during motor parameter measurement routine
0	MPET_WRITE_SHADOW	W	0h	Write measured parameters to shadow register when set to 1

7.8.4.3 CURRENT_PI Register (Offset = F0h) [Reset = 00000000h]

CURRENT_PI is shown in 図 7-91 and described in 表 7-61.

Return to the Summary Table.

Current PI controller used

図 7-91. CURRENT_PI Register

31-16	15-0
CURRENT_LOOP_KI	CURRENT_LOOP_KP
R-0h	R-0h

表 7-61. CURRENT_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CURRENT_LOOP_KI	R	0h	10 bit for current loop ki Same Scaling as CURR_LOOP_KI
15-0	CURRENT_LOOP_KP	R	0h	10 bit for current loop kp Same Scaling as CURR_LOOP_KP

7.8.4.4 SPEED_PI Register (Offset = F2h) [Reset = 00000000h]

SPEED_PI is shown in 図 7-92 and described in 表 7-62.

Return to the Summary Table.

Speed PI controller used

図 7-92. SPEED_PI Register

31-16	15-0
SPEED_LOOP_KI	SPEED_LOOP_KP
R-0h	R-0h

表 7-62. SPEED_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SPEED_LOOP_KI	R	0h	10 bit for current loop ki Same Scaling as SPD_LOOP_KI
15-0	SPEED_LOOP_KP	R	0h	10 bit for current loop kp Same Scaling as SPD_LOOP_KP

7.8.4.5 DAC_1 Register (Offset = F4h) [Reset = 00110000h]

DAC_1 is shown in 図 7-93 and described in 表 7-63.

Return to the Summary Table.

DAC1 Control Register

図 7-93. DAC_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED			DACOUT1_ENUM_SCALING				DACOUT1_SCALING
R-0h			W-8h				W-8h
15	14	13	12	11	10	9	8
DACOUT1_SCALING			DACOUT1_UNIPOLAR	DACOUT1_VAR_ADDR			
W-8h			W-0h	R/W-0h			
7	6	5	4	3	2	1	0
DACOUT1_VAR_ADDR							
R/W-0h							

表 7-63. DAC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-17	DACOUT1_ENUM_SCALING	W	8h	Multiplication Factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR multiplied with $2^{DACOUT1\_ENUM\_SCALING}$. DACOUT1_ENUM_SCALING comes into effect only if DACOUT1_SCALING is zero
16-13	DACOUT1_SCALING	W	8h	Scaling factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR scaled with DACOUT1_SCALING / 8. Actual voltage depends on DACOUT1_UNIPOLAR. If DACOUT1_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT1_SCALING / 8, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 8 If DACOUT1_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT1_SCALING / 8, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 8 0h = Treated s Enum with max value being 31 1h = 1 / 8 2h = 2 / 8 3h = 3 / 8 4h = 4 / 8 5h = 5 / 8 6h = 6 / 8 7h = 7 / 8 8h = 8 / 8 9h = 9 / 8 Ah = 10 / 8 Bh = 11 / 8 Ch = 12 / 8 Dh = 13 / 8 Eh = 14 / 8 Fh = 15 / 8

表 7-63. DAC_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	DACOUT1_UNIPOLAR	W	0h	Configures output of DACOUT1 If DACOUT1_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT1_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 16 If DACOUT1_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT1_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 16 0h = Bipolar (Offset of 1.5 V) 1h = Unipolar (No Offset)
11-0	DACOUT1_VAR_ADDR	R/W	0h	12-bit address of variable to be monitored

7.8.4.6 DAC_2 Register (Offset = F6h) [Reset = X]

DAC_2 is shown in 図 7-94 and described in 表 7-64.

Return to the Summary Table.

DAC2 Control Register

図 7-94. DAC_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	DACOUT2_ENUM_SCALING				DACOUT2_SCALING		
R-0h	W-X				W-8h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DACOUT2_SCALING	DACOUT2_UNIPOLAR	DACOUT2_VAR_ADDR					
W-8h	W-0h	R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACOUT2_VAR_ADDR							
R/W-0h							

表 7-64. DAC_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-19	DACOUT2_ENUM_SCALING	W	X	Multiplication Factor for DACOUT2 Algorithm Variable extracted from the address contained in DACOUT2_VAR_ADDR multiplied with $2^{DACOUT2\_ENUM\_SCALING}$. DACOUT2_ENUM_SCALING comes into effect only if DACOUT2_SCALING is zero
18-15	DACOUT2_SCALING	W	8h	Scaling factor for DACOUT2 Algorithm Variable extracted from the address contained in DACOUT2_VAR_ADDR scaled with DACOUT2_SCALING / 8. Actual voltage depends on DACOUT2_UNIPOLAR. If DACOUT2_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT2_SCALING / 8, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 8 If DACOUT2_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT2_SCALING / 8, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 8 0h = Treated s Enum with max value being 31 1h = 1 / 8 2h = 2 / 8 3h = 3 / 8 4h = 4 / 8 5h = 5 / 8 6h = 6 / 8 7h = 7 / 8 8h = 8 / 8 9h = 9 / 8 Ah = 10 / 8 Bh = 11 / 8 Ch = 12 / 8 Dh = 13 / 8 Eh = 14 / 8 Fh = 15 / 8

表 7-64. DAC_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DACOUT2_UNIPOLAR	W	0h	Configures output of DACOUT2 If DACOUT2_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT2_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 16 If DACOUT2_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT2_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 16 0h = Bipolar (Offset of 1.5 V) 1h = Unipolar (No Offset)
13-0	DACOUT2_VAR_ADDR	R/W	0h	14-bit address of variable to be monitored

7.8.5 Algorithm_Variables Registers

表 7-65 lists the memory-mapped registers for the Algorithm_Variables registers. All register offset addresses not listed in 表 7-65 should be considered as reserved locations and the register contents should not be modified.

表 7-65. ALGORITHM_VARIABLES Registers

Offset	Acronym	Register Name	Section
190h	ALGORITHM_STATE	Current Algorithm State Register	ALGORITHM_STATE Register (Offset = 190h) [Reset = 0000h]
196h	FG_SPEED_FDBK	FG Speed Feedback Register	FG_SPEED_FDBK Register (Offset = 196h) [Reset = 00000000h]
410h	BUS_CURRENT	Calculated DC Bus Current Register	BUS_CURRENT Register (Offset = 410h) [Reset = 00000000h]
440h	PHASE_CURRENT_A	Measured Current on Phase A Register	PHASE_CURRENT_A Register (Offset = 440h) [Reset = 00000000h]
442h	PHASE_CURRENT_B	Measured Current on Phase B Register	PHASE_CURRENT_B Register (Offset = 442h) [Reset = 00000000h]
444h	PHASE_CURRENT_C	Measured Current on Phase C Register	PHASE_CURRENT_C Register (Offset = 444h) [Reset = 00000000h]
468h	CSA_GAIN_FEEDBACK	CSA Gain Register	CSA_GAIN_FEEDBACK Register (Offset = 468h) [Reset = 0000h]
472h	VOLTAGE_GAIN_FEEDBACK	Voltage Gain Register	VOLTAGE_GAIN_FEEDBACK Register (Offset = 472h) [Reset = 0000h]
474h	VM_VOLTAGE	VM Voltage Register	VM_VOLTAGE Register (Offset = 474h) [Reset = 00000000h]
47Ah	PHASE_VOLTAGE_VA	Phase A Voltage Register	PHASE_VOLTAGE_VA Register (Offset = 47Ah) [Reset = 00000000h]
47Ch	PHASE_VOLTAGE_VB	Phase B Voltage Register	PHASE_VOLTAGE_VB Register (Offset = 47Ch) [Reset = 00000000h]
47Eh	PHASE_VOLTAGE_VC	Phase C Voltage Register	PHASE_VOLTAGE_VC Register (Offset = 47Eh) [Reset = 00000000h]
4B6h	SIN_COMMUTATION_ANGLE	Sine of Commutation Angle	SIN_COMMUTATION_ANGLE Register (Offset = 4B6h) [Reset = 00000000h]
4B8h	COS_COMMUTATION_ANGLE	Cosine of Commutation Angle	COS_COMMUTATION_ANGLE Register (Offset = 4B8h) [Reset = 00000000h]
4D2h	IALPHA	IALPHA Current Register	IALPHA Register (Offset = 4D2h) [Reset = 00000000h]
4D4h	IBETA	IBETA Current Register	IBETA Register (Offset = 4D4h) [Reset = 00000000h]
4D6h	VALPHA	VALPHA Voltage Register	VALPHA Register (Offset = 4D6h) [Reset = 00000000h]
4D8h	VBETA	VBETA Voltage Register	VBETA Register (Offset = 4D8h) [Reset = 00000000h]
4E2h	ID	Measured d-axis Current Register	ID Register (Offset = 4E2h) [Reset = 00000000h]

表 7-65. ALGORITHM_VARIABLES Registers (continued)

Offset	Acronym	Register Name	Section
4E4h	IQ	Measured q-axis Current Register	IQ Register (Offset = 4E4h) [Reset = 00000000h]
4E6h	VD	VD Voltage Register	VD Register (Offset = 4E6h) [Reset = 00000000h]
4E8h	VQ	VQ Voltage Register	VQ Register (Offset = 4E8h) [Reset = 00000000h]
524h	IQ_REF_ROTOR_ALIGN	Align Current Reference	IQ_REF_ROTOR_ALIGN Register (Offset = 524h) [Reset = 00000000h]
53Ch	SPEED_REF_OPEN_LOOP	Open Loop Speed Register	SPEED_REF_OPEN_LOOP Register (Offset = 53Ch) [Reset = 00000000h]
54Ch	IQ_REF_OPEN_LOOP	Open Loop Current Reference	IQ_REF_OPEN_LOOP Register (Offset = 54Ch) [Reset = 00000000h]
5D2h	SPEED_REF_CLOSED_LOOP	Speed Reference Register	SPEED_REF_CLOSED_LOOP Register (Offset = 5D2h) [Reset = 00000000h]
604h	ID_REF_CLOSED_LOOP	Reference for Current Loop Register	ID_REF_CLOSED_LOOP Register (Offset = 604h) [Reset = 00000000h]
606h	IQ_REF_CLOSED_LOOP	Reference for Current Loop Register	IQ_REF_CLOSED_LOOP Register (Offset = 606h) [Reset = 00000000h]
680h	ISD_STATE	ISD State Register	ISD_STATE Register (Offset = 680h) [Reset = 0000h]
68Ah	ISD_SPEED	ISD Speed Register	ISD_SPEED Register (Offset = 68Ah) [Reset = 00000000h]
6BEh	IPD_STATE	IPD State Register	IPD_STATE Register (Offset = 6BEh) [Reset = 0000h]
702h	IPD_ANGLE	Calculated IPD Angle Register	IPD_ANGLE Register (Offset = 702h) [Reset = 00000000h]
748h	ED	Estimated BEMF EQ Register	ED Register (Offset = 748h) [Reset = 00000000h]
74Ah	EQ	Estimated BEMF ED Register	EQ Register (Offset = 74Ah) [Reset = 00000000h]
758h	SPEED_FDBK	Speed Feedback Register	SPEED_FDBK Register (Offset = 758h) [Reset = 00000000h]
75Ch	THETA_EST	Estimated rotor Position Register	THETA_EST Register (Offset = 75Ch) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. 表 7-66 shows the codes that are used for access types in this section.

表 7-66. Algorithm_Variables Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.5.1 ALGORITHM_STATE Register (Offset = 190h) [Reset = 0000h]

ALGORITHM_STATE is shown in 図 7-95 and described in 表 7-67.

Return to the Summary Table.

Current Algorithm State Register

図 7-95. ALGORITHM_STATE Register

15	14	13	12	11	10	9	8
ALGORITHM_STATE							
R-0h							
7	6	5	4	3	2	1	0
ALGORITHM_STATE							
R-0h							

表 7-67. ALGORITHM_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ALGORITHM_STATE	R	0h	16-bit value indicating current state of device 0h = MOTOR_IDLE 1h = MOTOR_ISD 2h = MOTOR_TRISTATE 3h = MOTOR_BRAKE_ON_START 4h = MOTOR_IPD 5h = MOTOR_SLOW_FIRST_CYCLE 6h = MOTOR_ALIGN 7h = MOTOR_OPEN_LOOP 8h = MOTOR_CLOSED_LOOP_UNALIGNED 9h = MOTOR_CLOSED_LOOP_ALIGNED Ah = MOTOR_CLOSED_LOOP_ACTIVE_BRAKING Bh = MOTOR_SOFT_STOP Ch = MOTOR_RECIRCULATE_STOP Dh = MOTOR_BRAKE_ON_STOP Eh = MOTOR_FAULT Fh = MOTOR_MPET_MOTOR_STOP_CHECK 10h = MOTOR_MPET_MOTOR_STOP_WAIT 11h = MOTOR_MPET_MOTOR_BRAKE 12h = MOTOR_MPET_ALGORITHM_PARAMETERS_INIT 13h = MOTOR_MPET_RL_MEASURE 14h = MOTOR_MPET_KE_MEASURE 15h = MOTOR_MPET_STALL_CURRENT_MEASURE 16h = MOTOR_MPET_TORQUE_MODE 17h = MOTOR_MPET_DONE 18h = MOTOR_MPET_FAULT

7.8.5.2 FG_SPEED_FDBK Register (Offset = 196h) [Reset = 00000000h]

FG_SPEED_FDBK is shown in 図 7-96 and described in 表 7-68.

Return to the Summary Table.

Speed Feedback from FG

図 7-96. FG_SPEED_FDBK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FG_SPEED_FDBK																															
R-0h																															

表 7-68. FG_SPEED_FDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FG_SPEED_FDBK	R	0h	32-bit value indicating estimated rotor speed estimatedSpeed = (FG_SPEED_FDBK / 2^{27})*MAXIMUM_SPEED_HZ

7.8.5.3 BUS_CURRENT Register (Offset = 410h) [Reset = 00000000h]

BUS_CURRENT is shown in 図 7-97 and described in 表 7-69.

Return to the Summary Table.

Calculated Supply Current Register

図 7-97. BUS_CURRENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUS_CURRENT																															
R-0h																															

表 7-69. BUS_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUS_CURRENT	R	0h	32-bit value indicating bus current iBus = (BUS_CURRENT / 2^{27}) * Base_Current/8

7.8.5.4 PHASE_CURRENT_A Register (Offset = 440h) [Reset = 00000000h]

PHASE_CURRENT_A is shown in 図 7-98 and described in 表 7-70.

Return to the Summary Table.

Measured current on Phase A Register

図 7-98. PHASE_CURRENT_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_A																															
R-0h																															

表 7-70. PHASE_CURRENT_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_A	R	0h	32-bit value indicating measured current on Phase A iA = (PHASE_CURRENT_A / 2^{27}) * Base_Current/8

7.8.5.5 PHASE_CURRENT_B Register (Offset = 442h) [Reset = 00000000h]

PHASE_CURRENT_B is shown in 図 7-99 and described in 表 7-71.

Return to the Summary Table.

Measured current on Phase B Register

図 7-99. PHASE_CURRENT_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_B																															
R-0h																															

表 7-71. PHASE_CURRENT_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_B	R	0h	32-bit value indicating measured current on Phase B iB = (PHASE_CURRENT_B / 2^{27}) * Base_Current/8

7.8.5.6 PHASE_CURRENT_C Register (Offset = 444h) [Reset = 00000000h]

PHASE_CURRENT_C is shown in 図 7-100 and described in 表 7-72.

Return to the Summary Table.

Measured current on Phase C Register

図 7-100. PHASE_CURRENT_C Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_C																															
R-0h																															

表 7-72. PHASE_CURRENT_C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_C	R	0h	32-bit value indicating measured current on Phase C iC = (PHASE_CURRENT_C / 2^{27}) * Base_Current/8

7.8.5.7 CSA_GAIN_FEEDBACK Register (Offset = 468h) [Reset = 0000h]

CSA_GAIN_FEEDBACK is shown in 図 7-101 and described in 表 7-73.

Return to the Summary Table.

VM Voltage Register

図 7-101. CSA_GAIN_FEEDBACK Register

15	14	13	12	11	10	9	8
CSA_GAIN_FEEDBACK							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CSA_GAIN_FEEDBACK							
R-0h							

表 7-73. CSA_GAIN_FEEDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CSA_GAIN_FEEDBACK	R	0h	16-bit value indicating current sense gain 0h = MAX_CSA_GAIN * 8 1h = MAX_CSA_GAIN * 4 2h = MAX_CSA_GAIN * 2 3h = MAX_CSA_GAIN * 1

7.8.5.8 VOLTAGE_GAIN_FEEDBACK Register (Offset = 472h) [Reset = 0000h]

VOLTAGE_GAIN_FEEDBACK is shown in 図 7-102 and described in 表 7-74.

Return to the Summary Table.

Voltage Gain Register

図 7-102. VOLTAGE_GAIN_FEEDBACK Register

15	14	13	12	11	10	9	8
VOLTAGE_GAIN_FEEDBACK							
R-0h							
7	6	5	4	3	2	1	0
VOLTAGE_GAIN_FEEDBACK							
R-0h							

表 7-74. VOLTAGE_GAIN_FEEDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VOLTAGE_GAIN_FEEDBACK	R	0h	16-bit value indicating voltage gain 0h = 60V 1h = 30V 2h = 15V

7.8.5.9 VM_VOLTAGE Register (Offset = 474h) [Reset = 00000000h]

VM_VOLTAGE is shown in 図 7-103 and described in 表 7-75.

Return to the Summary Table.

Supply voltage register

図 7-103. VM_VOLTAGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VM_VOLTAGE																															
R-0h																															

表 7-75. VM_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VM_VOLTAGE	R	0h	32-bit value indicating dc bus voltage DC Bus Voltage = VM_VOLTAGE * 60 / 2^{27}

7.8.5.10 PHASE_VOLTAGE_VA Register (Offset = 47Ah) [Reset = 00000000h]

PHASE_VOLTAGE_VA is shown in 図 7-104 and described in 表 7-76.

Return to the Summary Table.

Phase A Voltage Register

図 7-104. PHASE_VOLTAGE_VA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VA																															
R-0h																															

表 7-76. PHASE_VOLTAGE_VA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VA	R	0h	32-bit value indicating Phase Voltage Va during ISD Phase A voltage = PHASE_VOLTAGE_VA * 60 / (sqrt(3) * 2^{27})

7.8.5.11 PHASE_VOLTAGE_VB Register (Offset = 47Ch) [Reset = 00000000h]

PHASE_VOLTAGE_VB is shown in 図 7-105 and described in 表 7-77.

Return to the Summary Table.

Phase B Voltage Register

図 7-105. PHASE_VOLTAGE_VB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VB																															
R-0h																															

表 7-77. PHASE_VOLTAGE_VB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VB	R	0h	32-bit value indicating Phase Voltage Vb during ISD Phase B voltage = PHASE_VOLTAGE_VB * 60 / (sqrt(3) * 2^{27})

7.8.5.12 PHASE_VOLTAGE_VC Register (Offset = 47Eh) [Reset = 00000000h]

PHASE_VOLTAGE_VC is shown in 図 7-106 and described in 表 7-78.

Return to the Summary Table.

Phase C Voltage Register

図 7-106. PHASE_VOLTAGE_VC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VC																															
R-0h																															

表 7-78. PHASE_VOLTAGE_VC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VC	R	0h	32-bit value indicating Phase Voltage Vc during ISD Phase C voltage = PHASE_VOLTAGE_VC * 60 / (sqrt(3) * 2^{27})

7.8.5.13 SIN_COMMUTATION_ANGLE Register (Offset = 4B6h) [Reset = 00000000h]

SIN_COMMUTATION_ANGLE is shown in 図 7-107 and described in 表 7-79.

Return to the Summary Table.

Sine of Commutation Angle

図 7-107. SIN_COMMUTATION_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIN_COMMUTATION_ANGLE																															
R-0h																															

表 7-79. SIN_COMMUTATION_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SIN_COMMUTATION_ANGLE	R	0h	32-bit value indicating sine of commutation Angle sinCommutationAngle = (SIN_COMMUTATION_ANGLE / 2^{27})

7.8.5.14 COS_COMMUTATION_ANGLE Register (Offset = 4B8h) [Reset = 00000000h]

COS_COMMUTATION_ANGLE is shown in 図 7-108 and described in 表 7-80.

Return to the Summary Table.

Cosine of Commutation Angle

図 7-108. COS_COMMUTATION_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COS_COMMUTATION_ANGLE																															
R-0h																															

表 7-80. COS_COMMUTATION_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COS_COMMUTATION_ANGLE	R	0h	32-bit value indicating cosine of commutation Angle cosCommutationAngle = (COS_COMMUTATION_ANGLE / 2^{27})

7.8.5.15 IALPHA Register (Offset = 4D2h) [Reset = 00000000h]

IALPHA is shown in 図 7-109 and described in 表 7-81.

Return to the Summary Table.

IALPHA Current Register

図 7-109. IALPHA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IALPHA																															
R-0h																															

表 7-81. IALPHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IALPHA	R	0h	32-bit value indicating calculated IALPHA iAlpha = (IALPHA / 2^{27}) * Base_Current/8

7.8.5.16 IBETA Register (Offset = 4D4h) [Reset = 00000000h]

IBETA is shown in 図 7-110 and described in 表 7-82.

Return to the Summary Table.

IBETA Current Register

図 7-110. IBETA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IBETA																															
R-0h																															

表 7-82. IBETA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IBETA	R	0h	32-bit value indicating calculated IBETA iBeta = (IBETA / 2^{27}) * Base_Current/8

7.8.5.17 VALPHA Register (Offset = 4D6h) [Reset = 00000000h]

VALPHA is shown in 図 7-111 and described in 表 7-83.

Return to the Summary Table.

VALPHA Voltage Register

図 7-111. VALPHA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALPHA																															
R-0h																															

表 7-83. VALPHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALPHA	R	0h	32-bit value indicating calculated VALPHA vAlpha = (VALPHA / 2^{27}) * 60 / sqrt(3)

7.8.5.18 VBETA Register (Offset = 4D8h) [Reset = 00000000h]

VBETA is shown in 図 7-112 and described in 表 7-84.

Return to the Summary Table.

VBETA Voltage Register

図 7-112. VBETA Register

31–0
VBETA
R-0h

表 7-84. VBETA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VBETA	R	0h	32-bit value indicating calculated VBETA vBeta = (VBETA / 2^{27}) * 60 / sqrt(3)

7.8.5.19 ID Register (Offset = 4E2h) [Reset = 00000000h]

ID is shown in 図 7-113 and described in 表 7-85.

Return to the Summary Table.

Measured d-axis Current Register

図 7-113. ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															
R-0h																															

表 7-85. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID	R	0h	32-bit value indicating estimated Id id = (ID / 2^{27}) * Base_Current/8

7.8.5.20 IQ Register (Offset = 4E4h) [Reset = 00000000h]

IQ is shown in 図 7-114 and described in 表 7-86.

Return to the Summary Table.

Measured q-axis Current Register

図 7-114. IQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ																															
R-0h																															

表 7-86. IQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ	R	0h	32-bit value indicating estimated Iq iq = (IQ / 2^{27}) * Base_Current/8

7.8.5.21 VD Register (Offset = 4E6h) [Reset = 00000000h]

VD is shown in 図 7-115 and described in 表 7-87.

Return to the Summary Table.

VD Voltage Register

図 7-115. VD Register

31-0
VD
R-0h

表 7-87. VD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VD	R	0h	32-bit value indicating applied Vd vd = (VD / 2^{27}) * 60 / sqrt(3)

7.8.5.22 VQ Register (Offset = 4E8h) [Reset = 00000000h]

VQ is shown in 図 7-116 and described in 表 7-88.

Return to the Summary Table.

VQ Voltage Register

図 7-116. VQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VQ																															
R-0h																															

表 7-88. VQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VQ	R	0h	32-bit value indicating applied Vq vq = (VQ / 2^{27}) * 60 / sqrt(3)

7.8.5.23 IQ_REF_ROTOR_ALIGN Register (Offset = 524h) [Reset = 00000000h]

IQ_REF_ROTOR_ALIGN is shown in 図 7-117 and described in 表 7-89.

Return to the Summary Table.

Align Current Reference

図 7-117. IQ_REF_ROTOR_ALIGN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_ROTOR_ALIGN																															
R-0h																															

表 7-89. IQ_REF_ROTOR_ALIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_ROTOR_ALIGN	R	0h	32-bit value indicating Align Current Reference iqRefRotorAlign = (IQ_REF_ROTOR_ALIGN / 2^{27}) * Base_Current/8

7.8.5.24 SPEED_REF_OPEN_LOOP Register (Offset = 53Ch) [Reset = 00000000h]

SPEED_REF_OPEN_LOOP is shown in 図 7-118 and described in 表 7-90.

Return to the Summary Table.

Speed at which motor transitions to close loop

図 7-118. SPEED_REF_OPEN_LOOP Register

31-0
SPEED_REF_OPEN_LOOP
R-0h

表 7-90. SPEED_REF_OPEN_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_OPEN_LOOP	R	0h	32-bit value indicating Open Loop Speed openLoopSpeedRef = (SPEED_REF_OPEN_LOOP / 2^{27}) * max_Speed- In Hz

7.8.5.25 IQ_REF_OPEN_LOOP Register (Offset = 54Ch) [Reset = 00000000h]

IQ_REF_OPEN_LOOP is shown in 図 7-119 and described in 表 7-91.

Return to the Summary Table.

Open Loop Current Reference

図 7-119. IQ_REF_OPEN_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_OPEN_LOOP																															
R-0h																															

表 7-91. IQ_REF_OPEN_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_OPEN_LOOP	R	0h	32-bit value indicating Open Loop Current Reference iqRefOpenLoop = (IQ_REF_OPEN_LOOP / 2^{27}) * Base_Current/8

7.8.5.26 SPEED_REF_CLOSED_LOOP Register (Offset = 5D2h) [Reset = 00000000h]

SPEED_REF_CLOSED_LOOP is shown in 図 7-120 and described in 表 7-92.

Return to the Summary Table.

Speed Reference Register

図 7-120. SPEED_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_REF_CLOSED_LOOP																															
R-0h																															

表 7-92. SPEED_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_CLOSED_LOOP	R	0h	32-bit value indicating reference for speed loop Speed Reference in closed loop (Hz) = (SPEED_REF_CLOSED_LOOP/ 2^{27}) * max_Speed- In Hz

7.8.5.27 ID_REF_CLOSED_LOOP Register (Offset = 604h) [Reset = 00000000h]

ID_REF_CLOSED_LOOP is shown in 図 7-121 and described in 表 7-93.

Return to the Summary Table.

Reference for Current Loop Register

図 7-121. ID_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_REF_CLOSED_LOOP																															
R-0h																															

表 7-93. ID_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID_REF_CLOSED_LOOP	R	0h	32-bit value indicating Id_ref for flux loop idRefClosedLoop = (ID_REF_CLOSED_LOOP / 2^{27}) * Base_Current/8

7.8.5.28 IQ_REF_CLOSED_LOOP Register (Offset = 606h) [Reset = 00000000h]

IQ_REF_CLOSED_LOOP is shown in 図 7-122 and described in 表 7-94.

Return to the Summary Table.

Reference for Current Loop Register

図 7-122. IQ_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_CLOSED_LOOP																															
R-0h																															

表 7-94. IQ_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_CLOSED_LOOP	R	0h	32-bit value indicating Iq_ref for torque loop iqRefClosedLoop = (IQ_REF_CLOSED_LOOP / 2^{27}) * Base_Current/8

7.8.5.29 ISD_STATE Register (Offset = 680h) [Reset = 0000h]

ISD_STATE is shown in 図 7-123 and described in 表 7-95.

Return to the Summary Table.

ISD state Register

図 7-123. ISD_STATE Register

15	14	13	12	11	10	9	8
ISD_STATE							
R-0h							
7	6	5	4	3	2	1	0
ISD_STATE							
R-0h							

表 7-95. ISD_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ISD_STATE	R	0h	16-bit value indicating current ISD state 0h = ISD_INIT 1h = ISD_MOTOR_STOP_CHECK 2h = ISD_MOTOR_DIRECTION_CHECK 3h = ISD_COMPLETE 4h = ISD_FAULT

7.8.5.30 ISD_SPEED Register (Offset = 68Ah) [Reset = 00000000h]

ISD_SPEED is shown in 図 7-124 and described in 表 7-96.

Return to the Summary Table.

ISD Speed Register

図 7-124. ISD_SPEED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISD_SPEED																															
R-0h																															

表 7-96. ISD_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ISD_SPEED	R	0h	32-bit value indicating calculated speed during ISD state isdSpeed = (ISD_SPEED / 2^{27}) * max_Speed- In Hz

7.8.5.31 IPD_STATE Register (Offset = 6BEh) [Reset = 0000h]

IPD_STATE is shown in 図 7-125 and described in 表 7-97.

Return to the Summary Table.

IPD state Register

図 7-125. IPD_STATE Register

15	14	13	12	11	10	9	8
IPD_STATE							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPD_STATE							
R-0h							

表 7-97. IPD_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IPD_STATE	R	0h	16-bit value indicating current IPD state 0h = IPD_INIT 1h = IPD_VECTOR_CONFIG 2h = IPD_RUN 3h = IPD_SLOW_RISE_CLOCK 4h = IPD_SLOW_FALL_CLOCK 5h = IPD_WAIT_CURRENT_DECAY 6h = IPD_GET_TIMES 7h = IPD_SET_NEXT_VECTOR 8h = IPD_CALC_SECTOR_RISE 9h = IPD_CALC_ROTOR_POSITION Ah = IPD_CALC_ANGLE Bh = IPD_COMPLETE Ch = IPD_FAULT

7.8.5.32 IPD_ANGLE Register (Offset = 702h) [Reset = 00000000h]

IPD_ANGLE is shown in 図 7-126 and described in 表 7-98.

Return to the Summary Table.

Calculated IPD Angle Register

図 7-126. IPD_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPD_ANGLE																															
R-0h																															

表 7-98. IPD_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPD_ANGLE	R	0h	32-bit value indicating measured IPD angle ipdAngle = (IPD_ANGLE / 2^{27}) * 360 (Degree)

7.8.5.33 ED Register (Offset = 748h) [Reset = 00000000h]

ED is shown in 図 7-127 and described in 表 7-99.

Return to the Summary Table.

Estimated BEMF EQ Register

図 7-127. ED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ED																															
R-0h																															

表 7-99. ED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ED	R	0h	32-bit value indicating estimated ED Ed = (ED / 2^{27}) * 60 / sqrt(3)

7.8.5.34 EQ Register (Offset = 74Ah) [Reset = 00000000h]

EQ is shown in 図 7-128 and described in 表 7-100.

Return to the Summary Table.

Estimated BEMF ED Register

図 7-128. EQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EQ																															
R-0h																															

表 7-100. EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EQ	R	0h	32-bit value indicating estimated EQ Eq = (EQ / 2^{27}) * 60 / sqrt(3)

7.8.5.35 SPEED_FDBK Register (Offset = 758h) [Reset = 00000000h]

SPEED_FDBK is shown in 図 7-129 and described in 表 7-101.

Return to the Summary Table.

Speed Feedback Register

図 7-129. SPEED_FDBK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_FDBK																															
R-0h																															

表 7-101. SPEED_FDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_FDBK	R	0h	32-bit value indicating estimated rotor speed estimatedSpeed = (SPEED_FDBK / 2^{27})*MAXIMUM_SPEED_HZ

7.8.5.36 THETA_EST Register (Offset = 75Ch) [Reset = 00000000h]

THETA_EST is shown in 図 7-130 and described in 表 7-102.

Return to the Summary Table.

Estimated rotor Position Register

図 7-130. THETA_EST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THETA_EST																															
R-0h																															

表 7-102. THETA_EST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	THETA_EST	R	0h	32-bit value indicating estimated rotor angle estimatedAngle = (THETA_EST / 2^{27})*360 (Degree)

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The MCF8315A device is used in sensorless 3-phase BLDC motor control. The driver provides a high performance, high-reliability, flexible solution for appliances, fans, pumps, residential and living fans, seat cooling fans, automotive fans and blowers. The following section shows a common application of the MCF8315A device.

8.2 Typical Applications

図 8-1 shows the typical schematic of MCF8315A

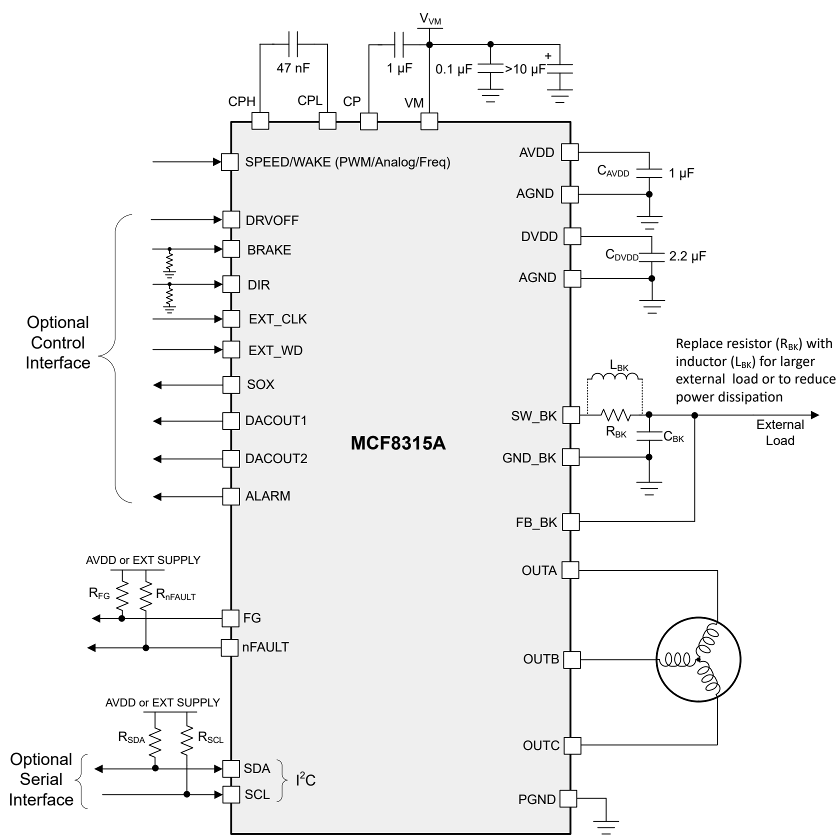

図 8-1. Example Application Schematic

表 8-1 lists the recommended values of the external components for MCF8315A.

表 8-1. MCF8315A External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{VM2}	VM	PGND	≥ 10-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device

表 8-1. MCF8315A External Components (continued)

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{CP}	CP	VM	X5R or X7R, 16-V, 1-µF capacitor
C_{FLY}	CPH	CPL	X5R or X7R, 47-nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin
C_{AVDD}	AVDD	AGND	X5R or X7R, 1-µF, ≥ 6.3-V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-µF to 1.3-µF at 3.3-V across operating temperature.
C_{DVDD}	DVDD	DGND	X5R or X7R, 2.2-µF, ≥ 6.3-V. In order for DVDD to accurately regulate output voltage, capacitor should have effective capacitance between 1.1-µF to 2.5-µF at 1.5-V across operating temperature.
C_{BK}	FB_BK	GND_BK	X5R or X7R, buck-output rated capacitor
L_{BK}	SW_BK	FB_BK	Buck-output inductor
R_{FG}	1.8 to 5-V Supply	FG	5.1-kΩ, Pull-up resistor
R_{nFAULT}	1.8 to 5-V Supply	nFAULT	5.1-kΩ, Pull-up resistor
R_{SDA}	1.8 to 3.3-V Supply	SDA	5.1-kΩ, Pull-up resistor
R_{SCL}	1.8 to 3.3-V Supply	SCL	5.1-kΩ, Pull-up resistor

Recommended application range for MCF8315A is shown in 表 8-2.

表 8-2. Recommended Application Range

Parameter	Min	Max	Unit
Motor voltage	4.5	35	V
Back-EMF constant (see セクション 7.3.12.3)	0.6	2000	mV/Hz
Motor resistance (see セクション 7.3.12.1)	0.006	20	Ω
Motor inductance (see セクション 7.3.12.2)	0.006	20	mH
Motor electrical speed	-	1500	Hz
Peak motor phase current	-	4	A

Default EEPROM configuration for MCF8315A is listed in 表 8-3. Default values are chosen for reliable motor start-up and closed loop operation. Refer to MCF8315A tuning guide which provides step by step procedure to tune a 3-phase BLDC motor in closed loop, conform to use-case and explore features in the device.

表 8-3. Recommended Default Values

Address Name	Address	Recommended Value
ISD_CONFIG	0x00000080	0x64738C20
REV_DRIVE_CONFIG	0x00000082	0x28200000
MOTOR_STARTUP1	0x00000084	0x0B6807D0
MOTOR_STARTUP2	0x00000086	0x2306600C
CLOSED_LOOP1	0x00000088	0x0D3201B4
CLOSED_LOOP2	0x0000008A	0x0BAD0000
CLOSED_LOOP3	0x0000008C	0x00000000
CLOSED_LOOP4	0x0000008E	0x00000000
SPEED_PROFILES1	0x00000094	0x00000000
SPEED_PROFILES2	0x00000096	0x00000000
SPEED_PROFILES3	0x00000098	0x00000000
SPEED_PROFILES4	0x0000009A	0x000D0000
SPEED_PROFILES5	0x0000009C	0x00000000

表 8-3. Recommended Default Values (continued)

Address Name	Address	Recommended Value
SPEED_PROFILES6	0x0000009E	0x00000000
FAULT_CONFIG1	0x00000090	0x3EC80106
FAULT_CONFIG2	0x00000092	0x70D00888
PIN_CONFIG	0x000000A4	0x00000000
DEVICE_CONFIG1	0x000000A6	0x00101462
DEVICE_CONFIG2	0x000000A8	0x4000F00F
PERI_CONFIG1	0x000000AA	0x41C05F00
GD_CONFIG1	0x000000AC	0x1C450100
GD_CONFIG2	0x000000AE	0x00200000
INT_ALGO_1	0x000000A0	0x2433407D
INT_ALGO_2	0x000000A2	0x000001A7

Once the device EEPROM is programmed with the desired configuration, device can be operated stand-alone and I^2C serial interface is not required anymore. Speed can be commanded using SPEED pin.

Below are the two essential parameters that are required to spin the motor in closed loop.

1. Maximum motor speed.
2. Current limit for torque PI loop.

8.2.1 Speed Input before VM Power-up

TI recommends adding a 200-ms delay after VM power-up or device wake-up (from sleep mode) before giving a speed command over SPEED pin or I^2C interface. In applications wherein a non-zero speed command is applied before VM is powered up, adding a circuit (red box in 図 8-2) to introduce a 200-ms delay will ensure optimal motor start-up performance.

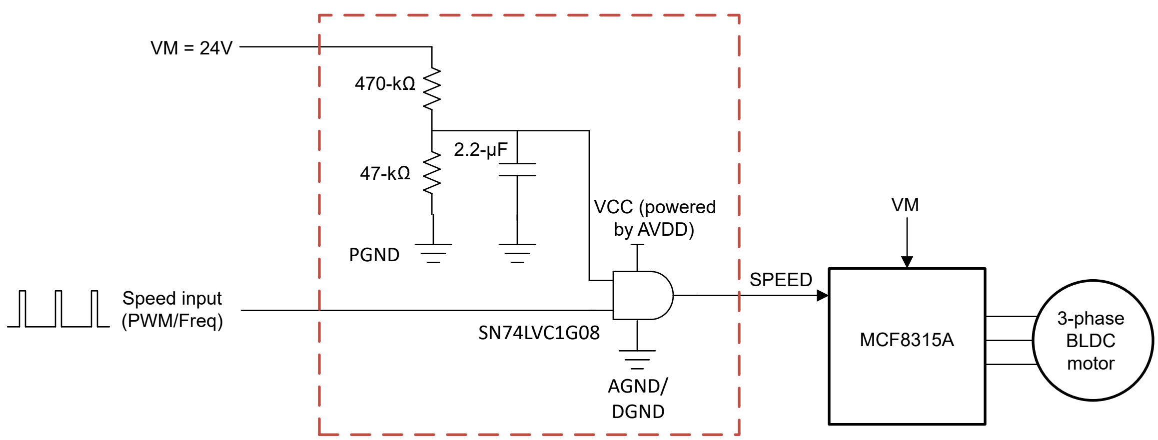

図 8-2. Delay circuit when speed command applied before VM power-up

R, C values in the delay circuit (470-kΩ, 47-kΩ, 2.2-µF) are designed to ensure the divided down voltage at the AND gate input is > V_{IH} at lowest operating value of VM while also ensuring the divided down voltage does not exceed the maximum allowable voltage at the AND gate input at highest operating VM. R, C values should also be designed to provide at least 200-ms delay to reach V_{IH} at lowest operating value of VM.

8.2.2 Application Curves

8.2.2.1 Motor startup

図 8-3 shows the FG waveform and the phase current waveform at different motor operations.

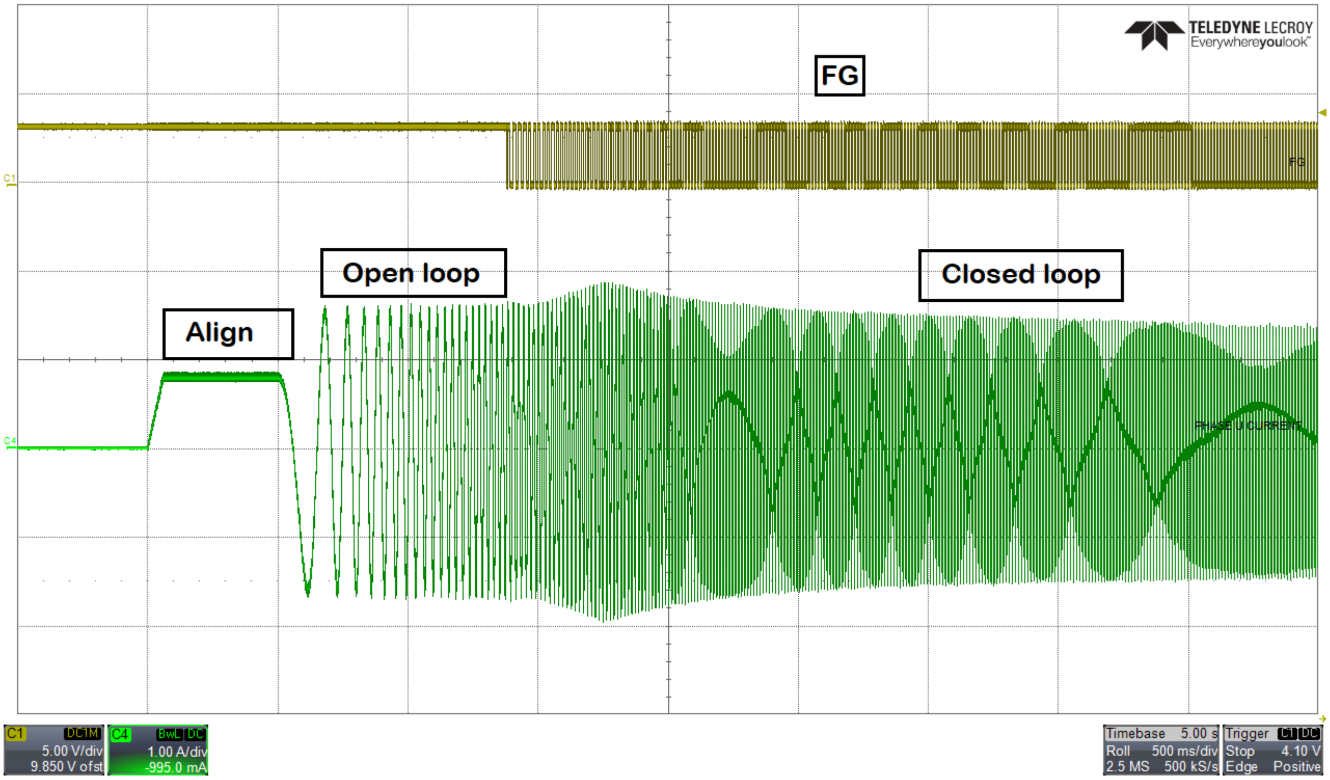

図 8-3. Motor Startup - FG and Phase current

8.2.2.2 MPET

図 8-4 shows the phase current waveform during motor parameter measurement. 図 8-5 shows the IPD current waveform during R, L and Ke measurement. Bottom half of 図 8-5 shows the IPD current waveform during R and L measurement. R is measured during the rising of phase current and L is measured during the falling of phase current. After R and L measurement, motor spins in open loop. Once the speed reaches MPET open loop speed reference [MPET_OPEN_LOOP_SPEED_REF], motor is coasted. BEMF voltage of all three phases are measured and Ke is calculated.

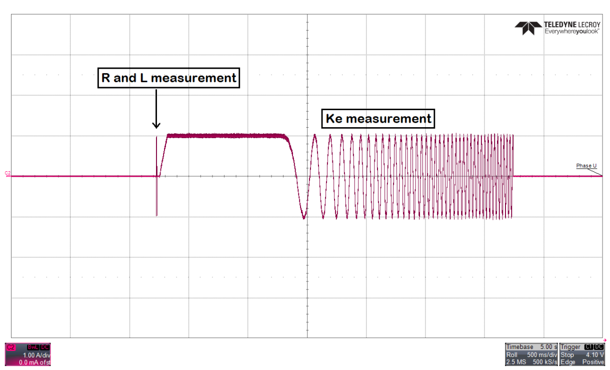

図 8-4. MPET - Phase current

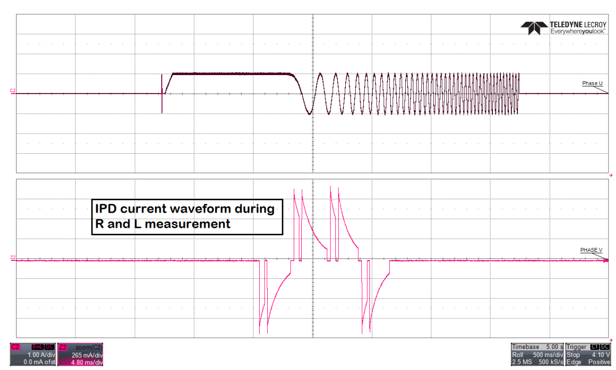

図 8-5. IPD current waveform during Rand L measurement

8.2.2.3 Dead time compensation

図 8-6 shows the phase current waveform when dead time compensation is disabled. Fundamental frequency of phase current is 40 Hz. Fast Fourier transform (FFT) of phase current plot shows harmonics at 160 Hz and 220

Hz. 図 8-7 shows the phase current waveform when dead time compensation is enabled. Phase current looks more sinusoidal and the FFT of phase current plot does not have any harmonics.

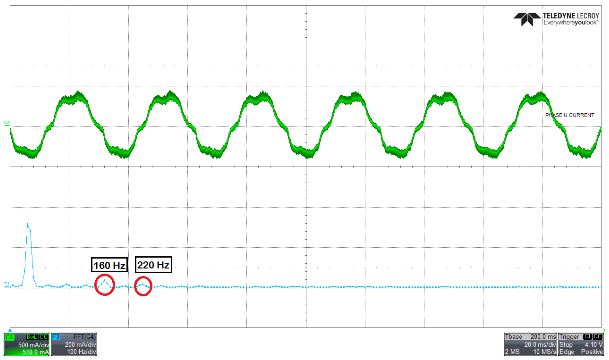

図 8-6. Phase current and FFT - Dead time compensation disabled

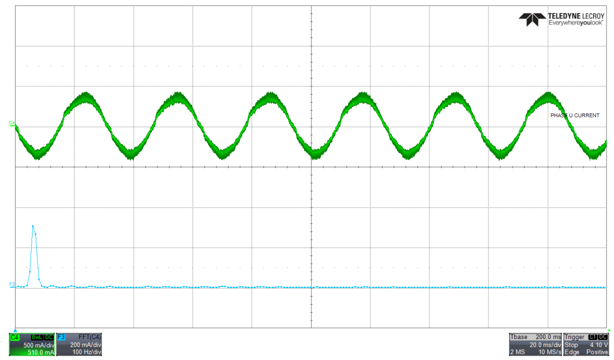

図 8-7. Phase current and FFT - Dead time compensation enabled

8.2.2.4 Auto handoff

図 8-8 shows the auto handoff feature in MCF8315A where the motor transitions seamlessly from open loop to closed loop.

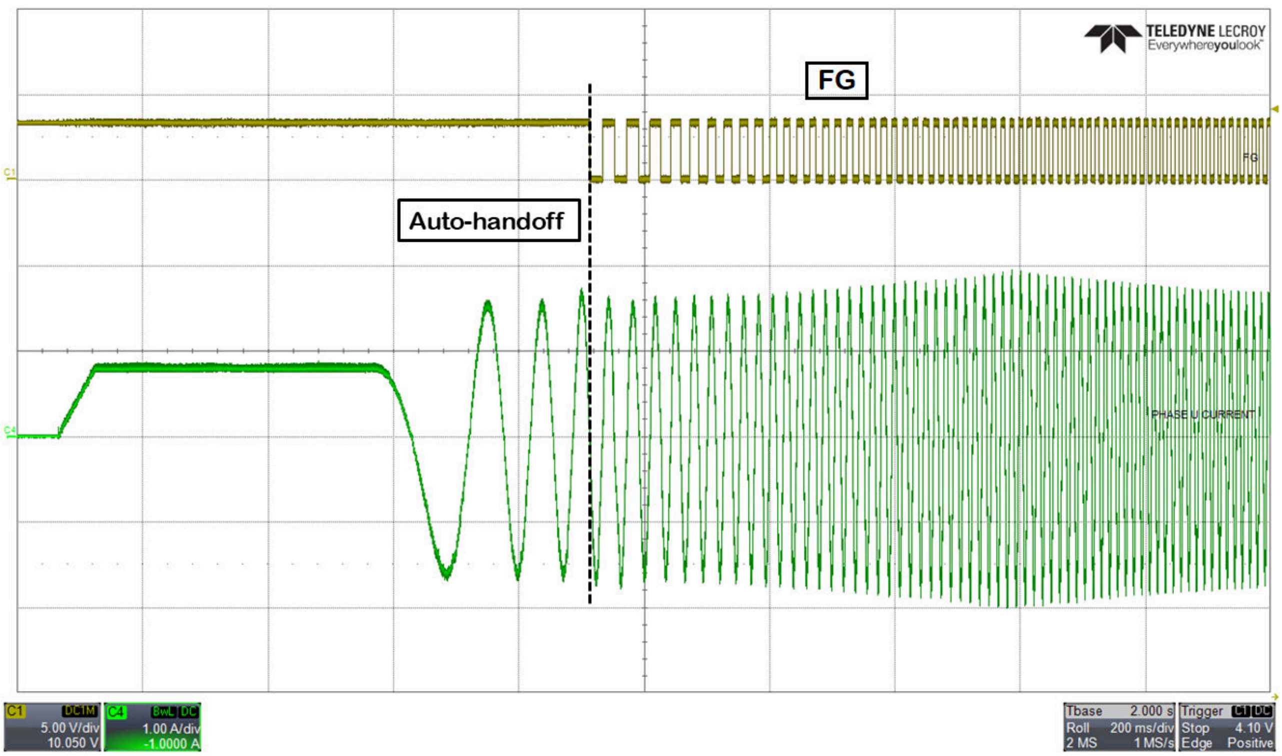

図 8-8. Auto-handoff

8.2.2.5 Motor stop – recirculation mode

図 8-9 shows the supply voltage and phase current waveform after stopping the motor. Recirculation mode in MCF8315A prevents the supply voltage from overshoots.

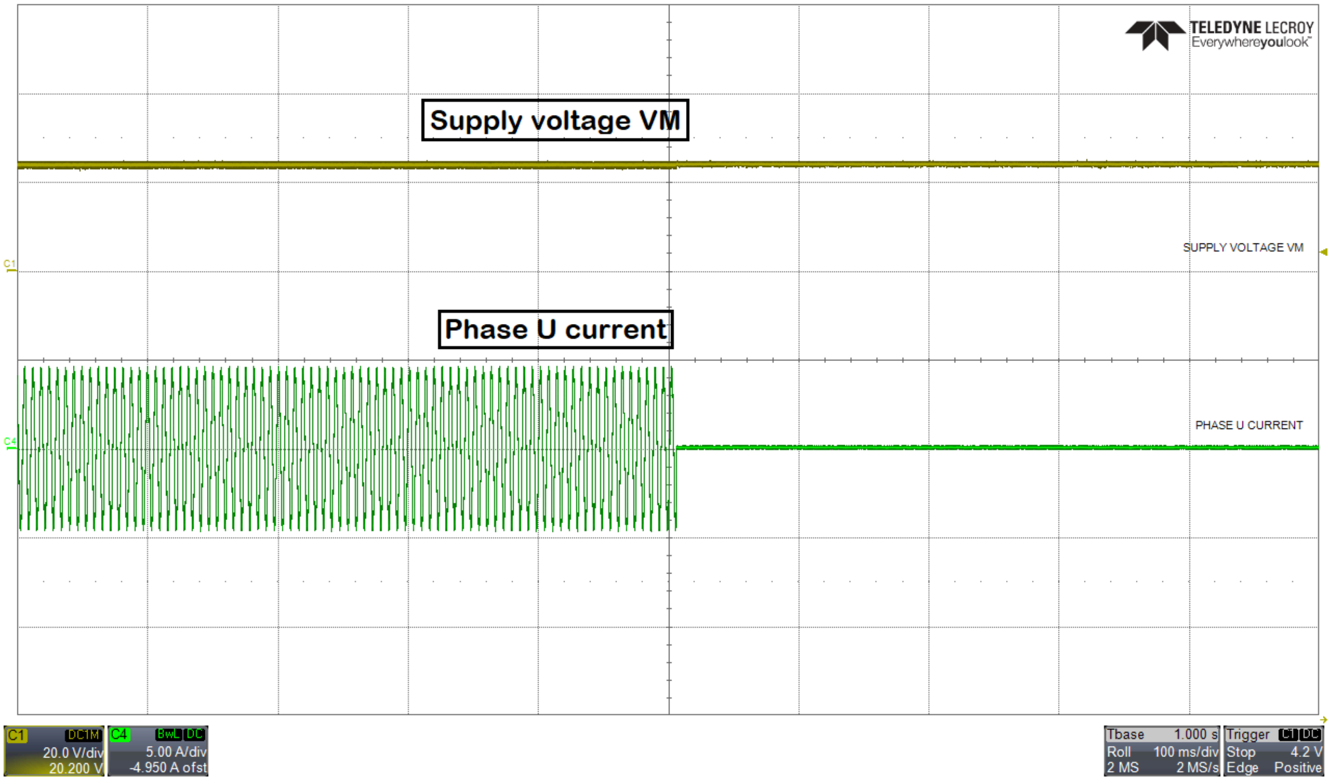

図 8-9. Motor stop - recirculation mode

8.2.2.6 Anti voltage surge (AVS)

When motor speed decelerates at a very high deceleration rate, mechanical energy from the motor returns to the power supply which could result in pumping up the supply voltage, VM. 図 8-10 shows overshoot in power supply voltage when AVS is disabled. Motor decelerates from 100% duty cycle to 10% duty cycle at a deceleration rate of 70,000 Hz/sec. 図 8-11 shows no overshoot in power supply voltage when AVS is enabled.

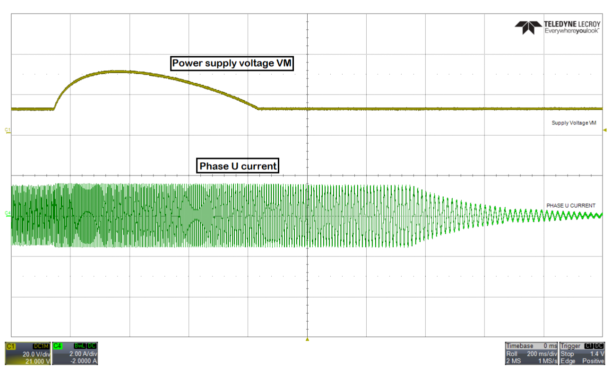

図 8-10. Power supply voltage and phase current waveform when AVS is disabled

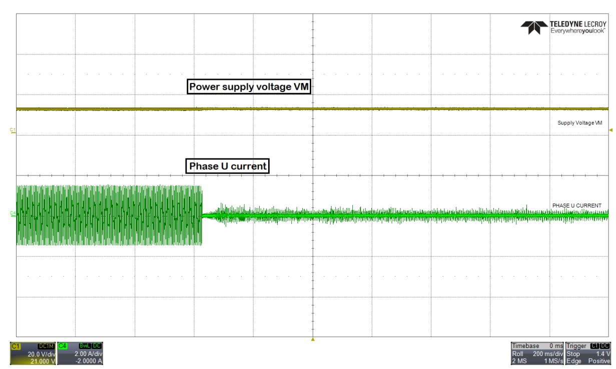

図 8-11. Power supply voltage and phase current waveform when AVS is enabled

8.2.2.7 Real time variable tracking using DACOUT

MCF8315A has two 12-bit DAC which outputs analog voltage equivalent of digital variables on DACOUT1 and DACOUT2 pins with resolution of 12 bits and max voltage of 3V. Signals available on DACOUT pins can be used for tuning speed controller or other driver configuration or bus current monitoring. Check algorithm variable registers in datasheet for list of all algorithm variables.

The addresses for variables for DACOUT1 and DACOUT2 are configured using register bits DACOUT1_VAR_ADDR and DACOUT2_VAR_ADDR. This is useful in applications which require tracking algorithm variables in real time without having any delay from the communication bus. Pin 37 and 38 should be configured as DACOUT1 and DACOUT2.

For example, if the user wants to read phase A current from pin 37, configure pin 37 as DACOUT1 and program the phase A current register address (0x00000440) in Hex in [DACOUT1_VAR_ADDR]. If the user wants to read estimated rotor angle from pin 38, configure pin 38 as DACOUT2 and program the estimated rotor angle register address (0x00000736) in Hex in [DACOUT2_VAR_ADDR].

図 8-12 shows the outputs of DACOUT1 and DACOUT2. DACOUT1 is configured to read phase A current and DACOUT2 is configured to read estimated rotor angle.

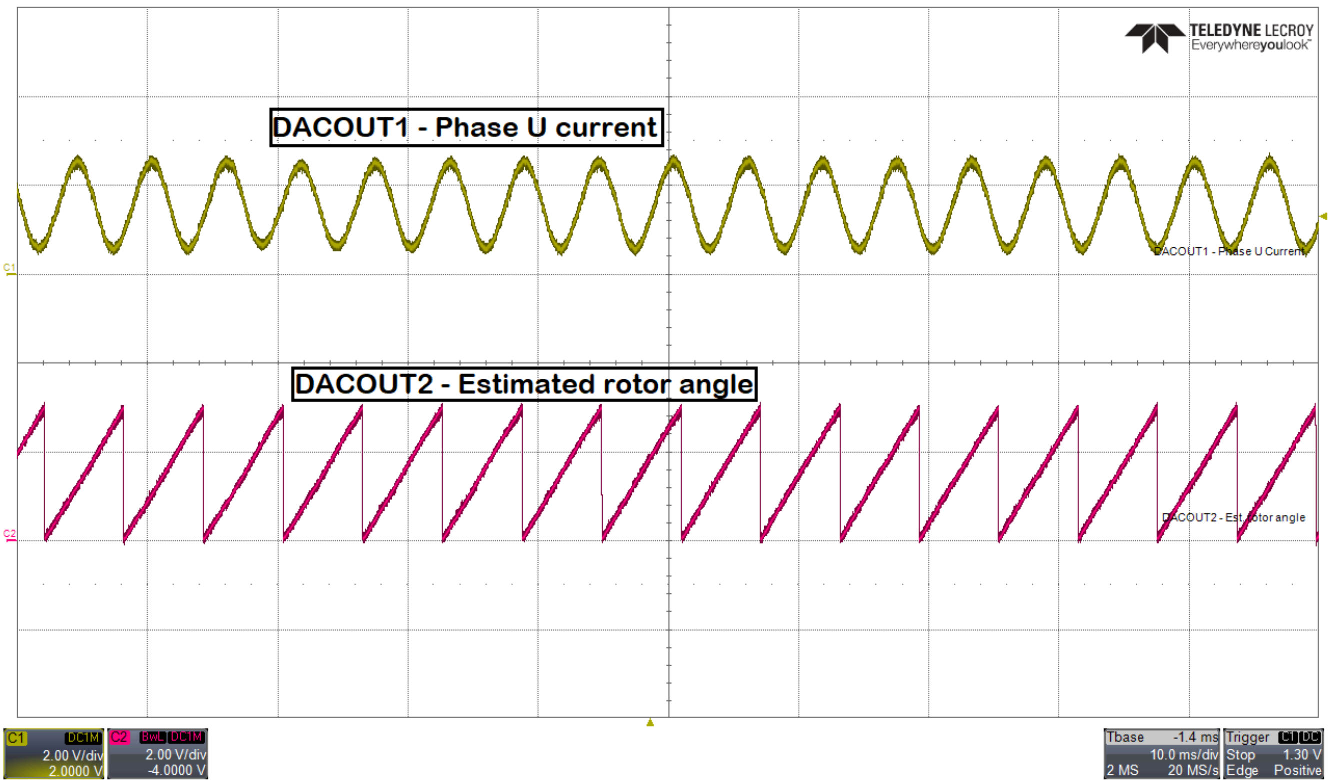

図 8-12. DACOUT1 and DACOUT2

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in VM voltage. When adequate bulk capacitance is used, the VM voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate bulk capacitor.

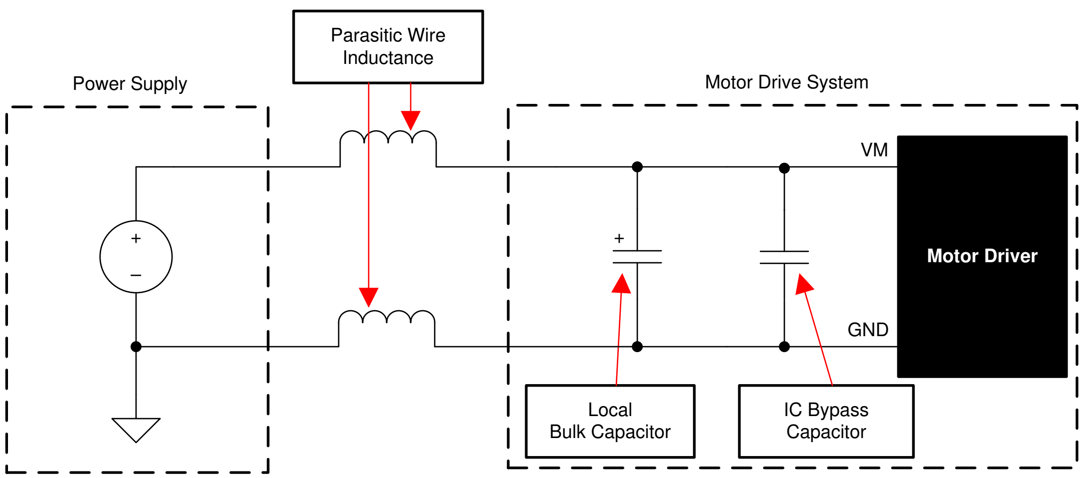

図 9-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize parasitic inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND_BK can be split. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW_BK and FB_BK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB_BK trace as much as possible to allow for faster load switching.

図 10-1 shows a layout example for the MCF8315A. Also, for layout example, refer to MCF8315A EVM.

10.2 Layout Example

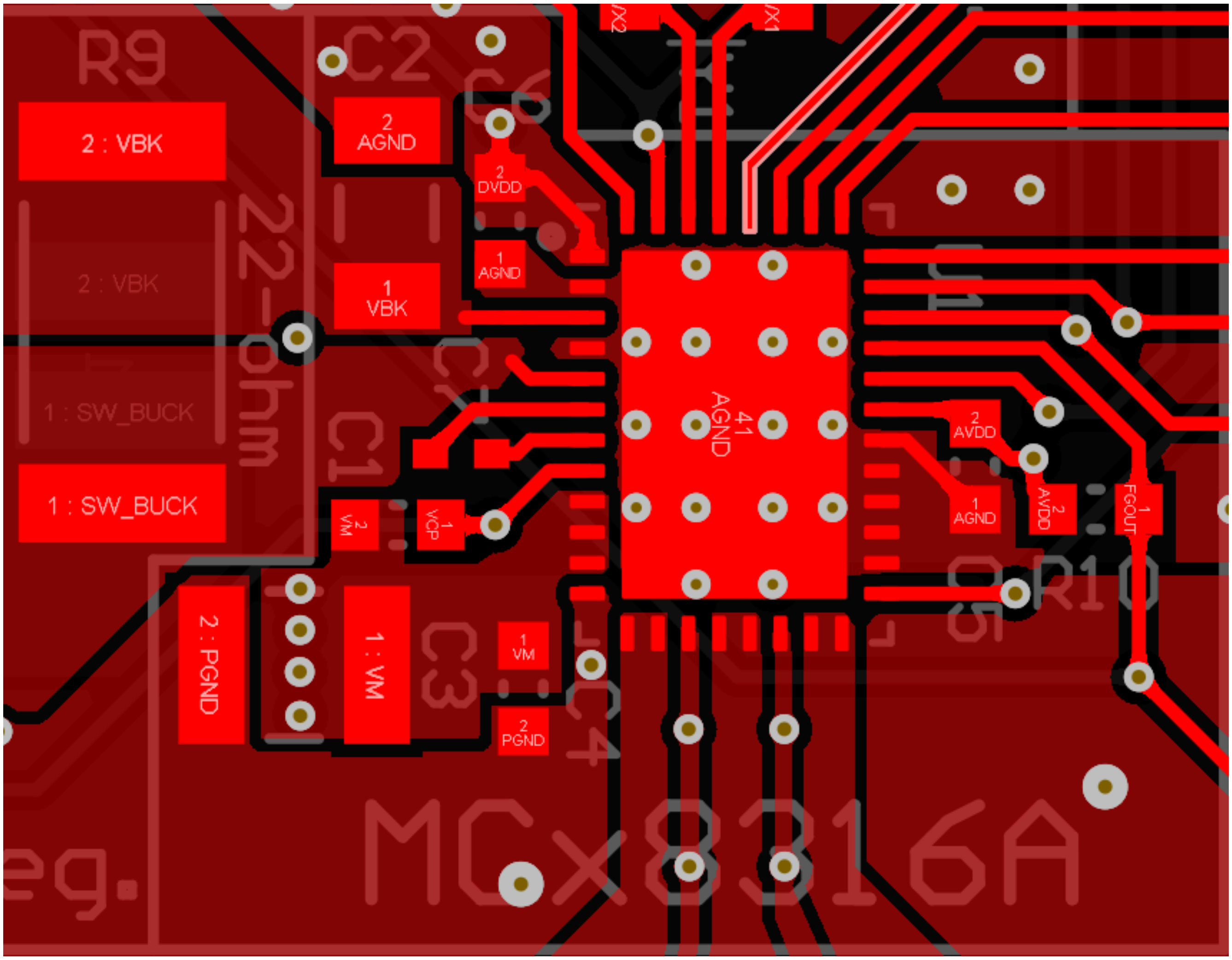

図 10-1. Recommended Layout Example

10.3 Thermal Considerations

The MCF8315A has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

The power dissipated in the output FET resistance ($R_{DS(on)}$) dominates power dissipation in MCF8315A.

At start-up and fault conditions, the FET current is much higher than normal operating FET current; remember to take these peak currents and their duration into consideration.

The total device power dissipation is the power dissipated in each of the three half-bridges added together along with standby power, LDO and buck regulator losses.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

A summary of equations for calculating each loss is shown below in 表 10-1.

表 10-1. Power Losses for MCF8315A

Loss type	MCF8315A
Standby power	$P_{standby}$ = VM x I_{VM_TA}
LDO	P_{LDO} = (VM-V_{AVDD}) x I_{AVDD}, if BUCK_PS_DIS = 1b P_{LDO} = (V_{BK}-V_{AVDD}) x I_{AVDD}, if BUCK_PS_DIS = 0b
FET conduction	P_{CON} = 3 x $(I_{RMS(FOC)})^2$ x $R_{ds,on(TA)}$
FET switching	P_{SW} = 3 x $I_{PK(FOC)}$ x $V_{PK(FOC)}$ x $t_{rise/fall}$ x f_{PWM}
Diode	P_{diode} = 3 x $I_{PK(FOC)}$ x V_{diode} x t_{dead} x f_{PWM}
Buck	P_{BK} = 0.11 x V_{BK} x I_{BK} (η_{BK} = 90%)

11 Device and Documentation Support

11.1 サポート・リソース

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11.3 静電気放電に関する注意事項

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11.4 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MCF8315A1VRGFR	ACTIVE	VQFN	RGF	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MCF83 15A1V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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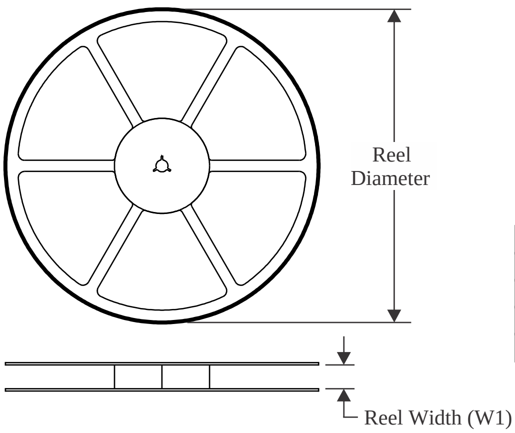
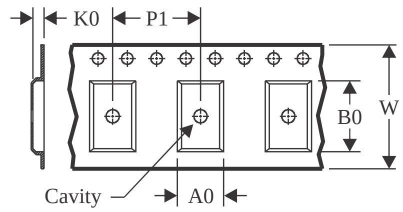
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

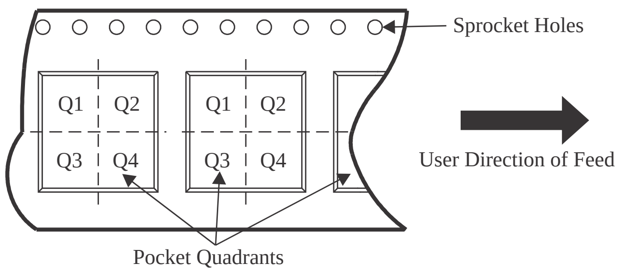


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

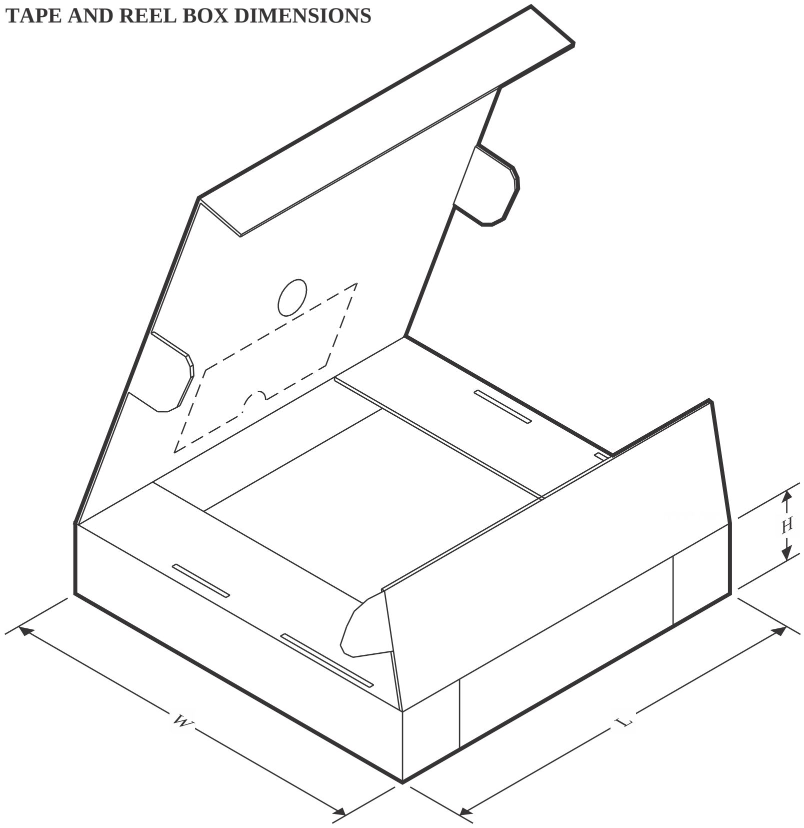
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCF8315A1VRGFR	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



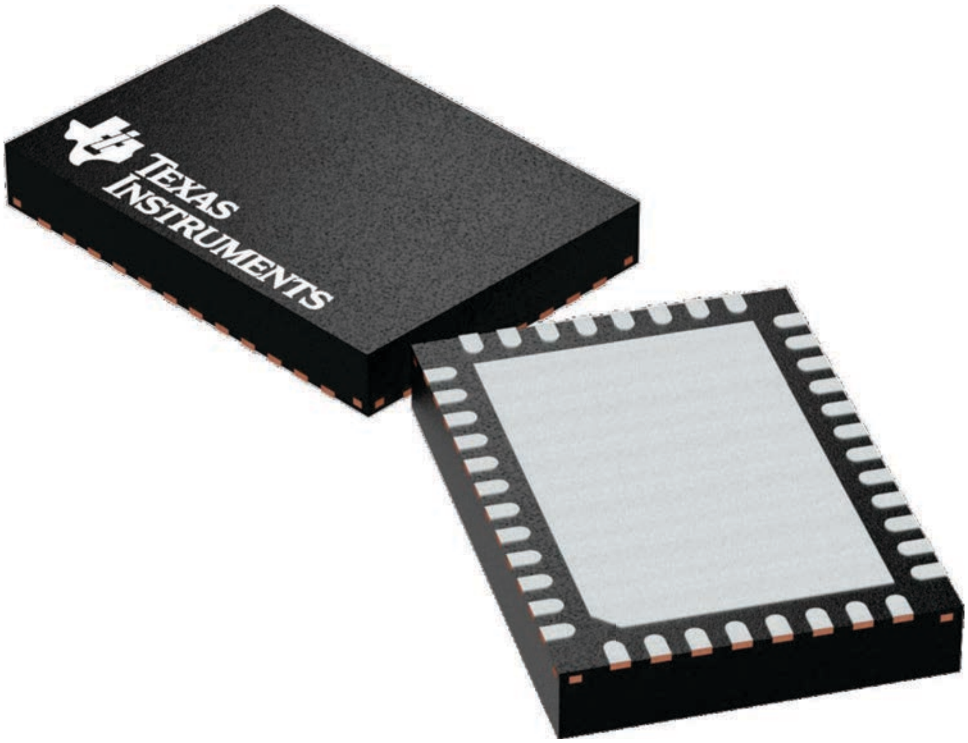
*All dimensions are nominal

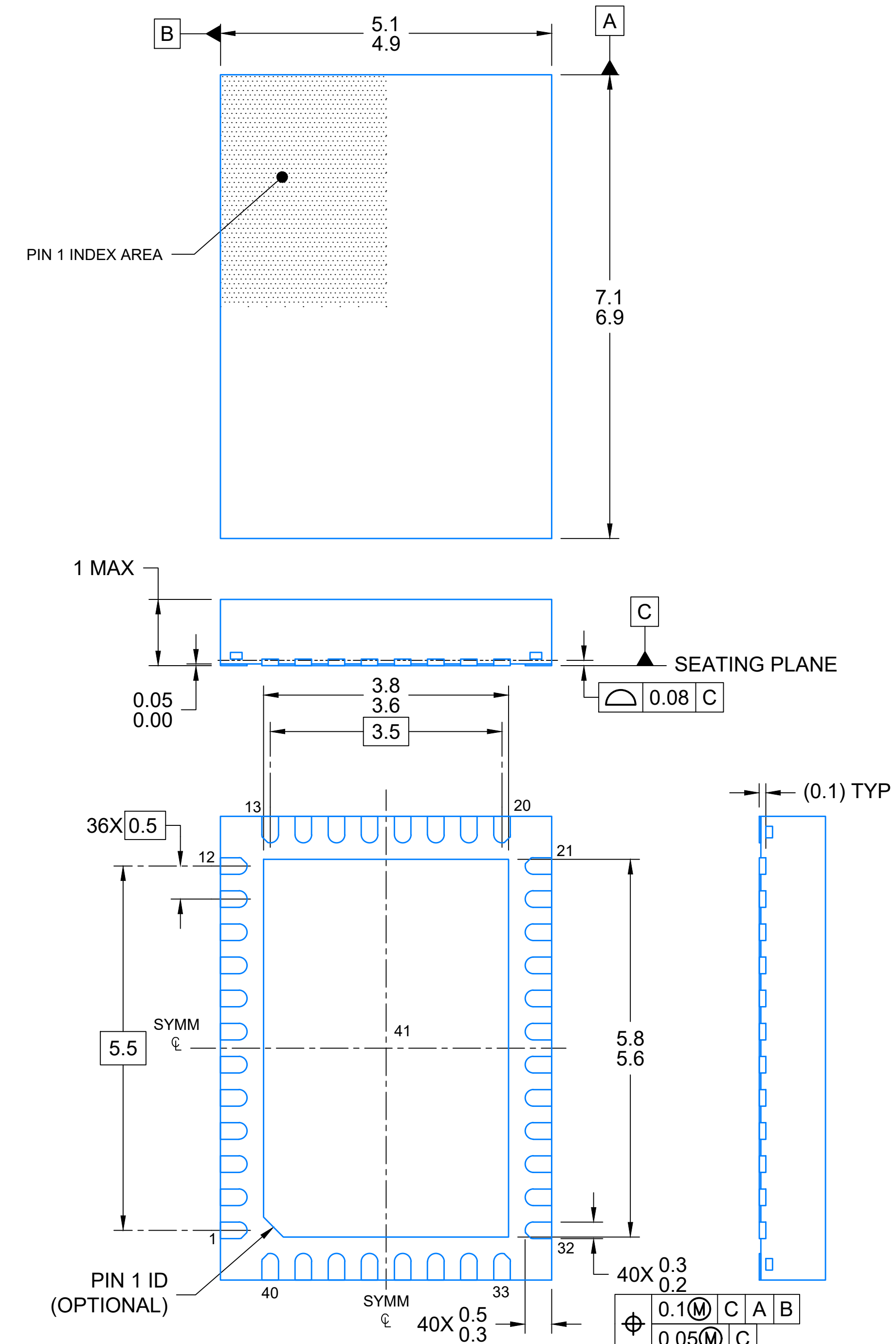
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCF8315A1VRGFR	VQFN	RGF	40	3000	367.0	367.0	35.0

5 x 7, 0.5 mm pitch

PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





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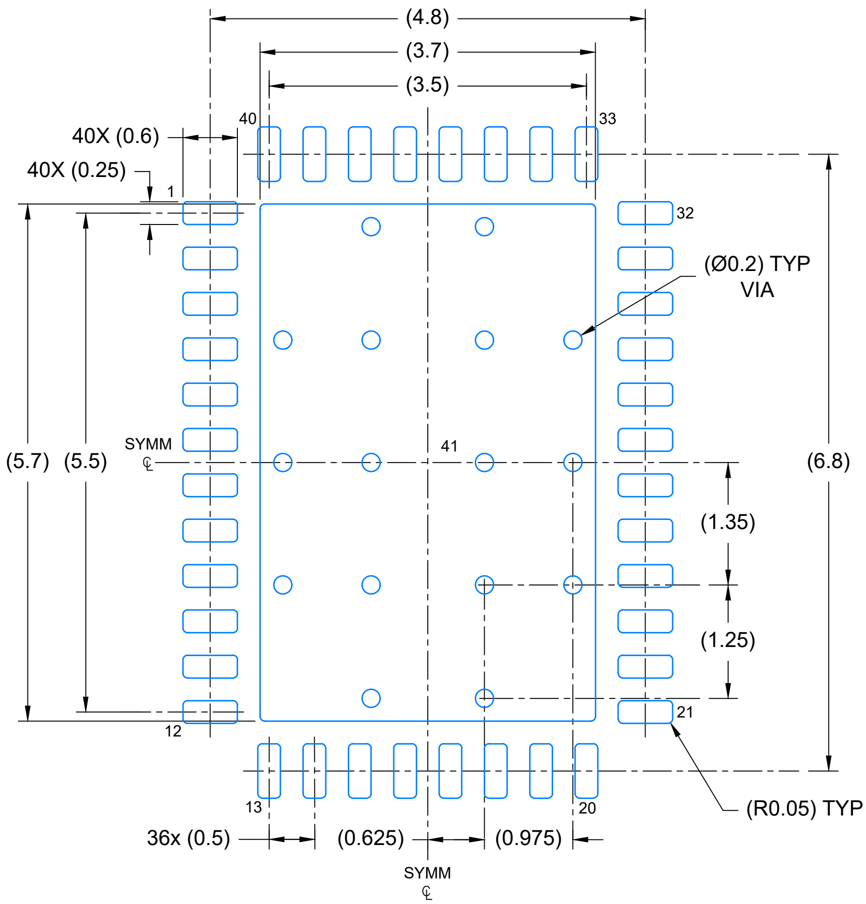
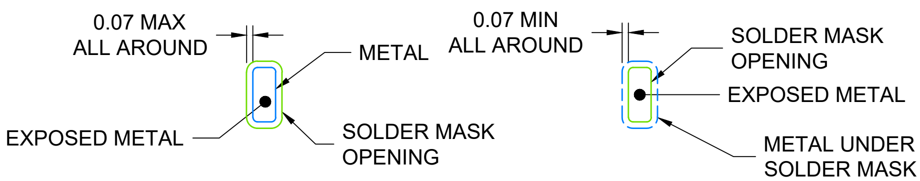
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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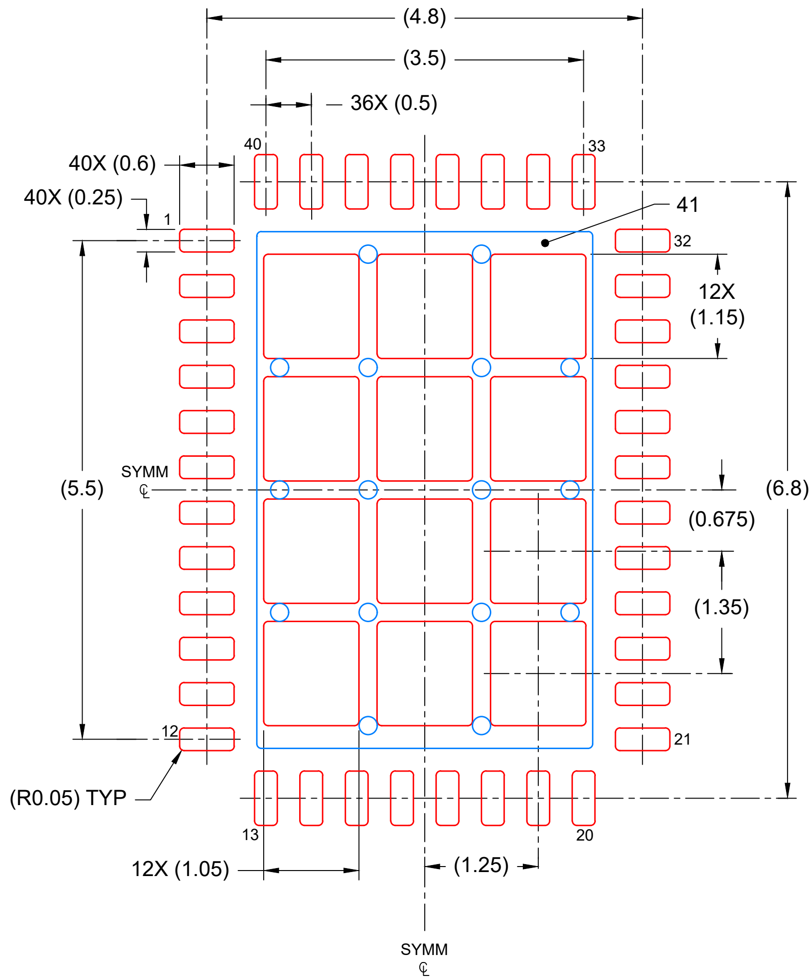
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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