LP87702-Q1 診断機能付きデュアル降圧コンバータ / 5V 昇圧回路

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - デバイス温度グレード 1:–40℃～+125℃、T_A
- 機能安全品質管理
  - 機能安全システムの設計に役立つ資料を利用可能
  - 外部電圧監視用の 2 つの入力
  - 2 つのプログラム可能なパワー・グッド信号
  - 診断専用の基準電圧
  - リセット出力付きのウィンドウ・ウォッチドッグ
  - 出力短絡および過負荷保護
  - 過熱警告および保護
  - 過電圧保護 (OVP) および低電圧誤動作防止 (UVLO)
- 2 つの高効率降圧 DC/DC コンバータ
  - 最大出力電流:3.5A
  - 2MHz、3MHz、4MHz のスイッチング周波数
  - PWM/PFM 自動切り替えおよび強制 PWM での動作
  - 出力電圧:0.7V～3.36V
- 5V 昇圧コンバータ
  - 最大出力電流:600mA
- スイッチングを同期するための外部クロック入力
- 拡散スペクトラム変調
- プログラム可能なスタートアップ / シャットダウン・シーケンス (イネーブル信号に同期)
- 汎用出力 (GPO) を設定可能
- I^2C 互換インターフェイスの Standard (100kHz)、Fast (400kHz)、Fast+ (1MHz)、High-Speed (3.4MHz) モードをサポート
- マスクをプログラム可能な割り込み機能

2 アプリケーション

- 車載用レーダー
- 車載用カメラ
- 車載センサ・フュージョン
- 産業用レーダー
- ビル・オートメーション

3 概要

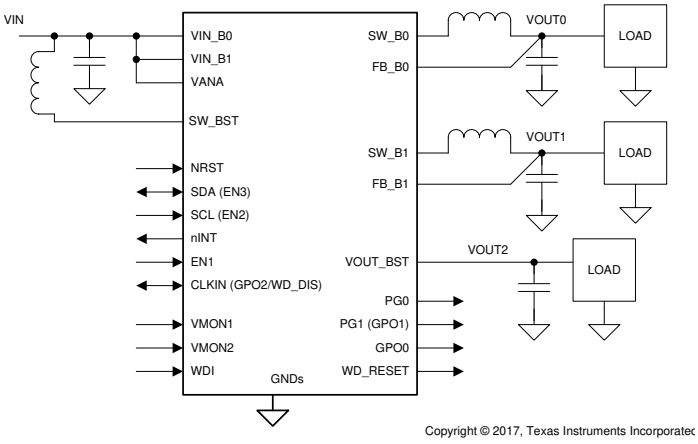
LP87702-Q1 を使用すると、最新のプラットフォーム、特に車載用レーダー / カメラおよび産業用レーダー・アプリケーションの電力管理要件を簡単に満たすことができます。このデバイスは、セーフティ・クリティカル・アプリケーションをサポートするための 2 つの降圧 DC/DC コンバータ、5V 昇圧コンバータを内蔵しています。外部電源用の 2 つの電圧監視入力と、ウィンドウ・ウォッチドッグを内蔵しています。

PWM/PFM の自動切り替え (AUTO モード) 動作により、降圧コンバータは広い出力電流範囲にわたって高い効率が得られます。LP87702-Q1 は、リモート電圧センシングを使用してコンバータ出力とポイント・オブ・ロード (POL) の間の IR 降下を補償することで、出力電圧の精度を向上させています。

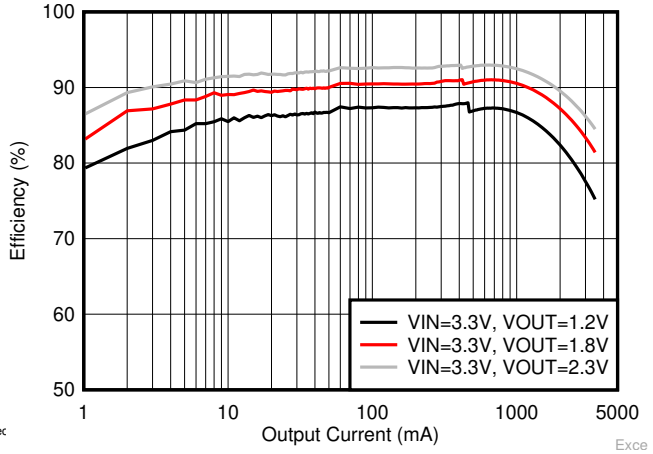
製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
LP87702-Q1	VQFN (32)	5.00mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



降圧効率と出力電流との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (September 2019) to Revision C (June 2021)	Page
• 機能安全関連機能を機能安全品質管理の下に移動	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Changed multiple register bit descriptions	45

Changes from Revision A (July 2018) to Revision B (September 2019)	Page
• 特長の FMEDA と機能安全マニュアルの提供を追加	1
• 「概要」の表現を変更	1
• Added test condition	7
• Changed from typical value to max value	7
• Added comment on $VANA_{OVP}$ setting and it's impact on device input voltage range	16
• Added comment on minimum WDI pulse length	26
• Changed BOOST_SC_INT bit set delay from immediate to 1 ms	36
• Changed multiple register bit descriptions	45

Changes from Revision * (December 2017) to Revision A (July 2018)	Page
• 量産データのデータシートの初版	1

5 概要 (続き)

イネーブル信号と同期したプログラム可能なスタートアップおよびシャットダウン・シーケンスがサポートされ、汎用デジタル出力も含まれています。

スタートアップ時および電圧の変化時に、デバイスは出力スルー・レートを制御し、出力電圧のオーバーシュートおよび突入電流を最小限に抑えます。ワンタイム・プログラマブル (OTP) メモリも搭載しており、各注文用型番の OTP は所定のアプリケーション向けに設定されています。各注文型番のデフォルトの OTP 設定については、テクニカル・リファレンス・マニュアルを参照してください。

6 Pin Configuration and Functions

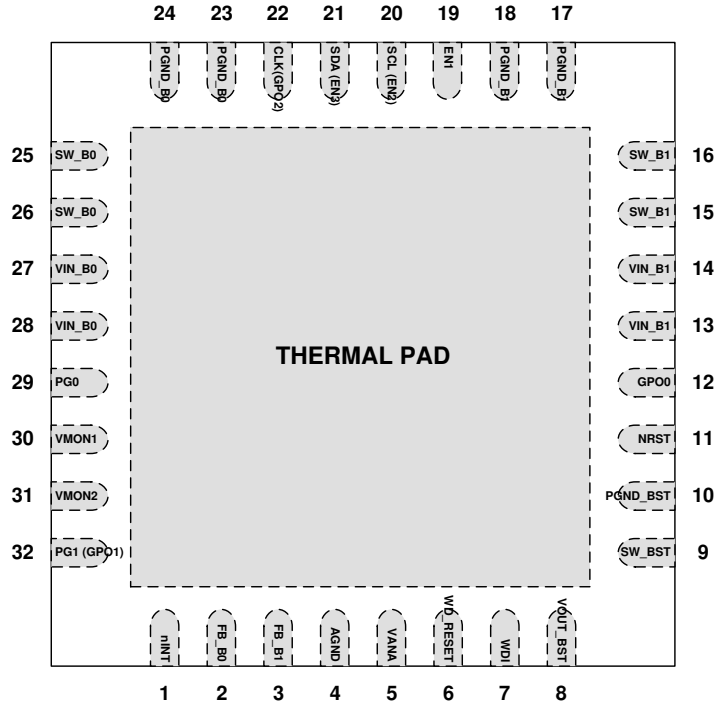

図 6-1. RHB Package 32-Pin VQFN With Thermal Pad Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
AGND	4	G	Ground
CLKIN	22	D/I/O	External clock input. Alternative function is general purpose digital output 2 (GPO2). Second alternative function is watchdog disable (WD_DIS)
EN1	19	D/I	Programmable Enable 1 signal.
FB_B0	2	A	Output voltage feedback for Buck0.
FB_B1	3	A	Output voltage feedback for Buck1.
GPO0	12	D/O	General purpose digital output 0.
nINT	1	D/O	Open-drain interrupt output. Active LOW.
NRST	11	D/I	Reset signal for the device.
PG0	29	D/O	Programmable power-good indication signal.
PG1	32	D/O	Programmable power-good indication signal. Alternative function is general purpose digital output 1 (GPO1).
PGND_B0	23, 24	P/G	Power ground for Buck0.
PGND_B1	17, 18	P/G	Power Ground for Buck1.
PGND_BST	10	P/G	Power ground for boost.
SCL	20	D/I	Serial interface clock input for I2C access. Connect a pullup resistor. Alternative function is programmable to the enable 2 signal.
SDA	21	D/I/O	Serial interface data input and output for I2C access. Connect a pullup resistor. Alternative function is programmable to the enable 3 signal.
SW_B0	25, 26	P/O	Buck0 switch node.
SW_B1	15, 16	P/O	Buck1 switch node.
SW_BST	9	P/I	Boost input. Bypass switch input when this mode is selected.
VANA	5	P	Supply voltage for analog and digital blocks. Must be connected to same node with VIN_Bx.

表 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VMON1	30	A/I	Voltage monitoring input 1.
VMON2	31	A/I	Voltage monitoring input 2.
VIN_B0	27, 28	P/I	Input for Buck0. The separate power pins VIN_Bx are not connected together internally – VIN_Bx pins must be connected together in the application and be locally bypassed.
VIN_B1	13, 14	P/I	Input for Buck1. The separate power pins VIN_Bx are not connected together internally – VIN_Bx pins must be connected together in the application and be locally bypassed.
VOUT_BST	8	P/O	Boost output. Bypass switch output when this mode is selected.
WD_RESET	6	D/O	Reset output from window watchdog
WDI	7	D/I	Digital input signal for window watchdog
Thermal pad	N/A	G	
A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin			

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VIN_B0, VIN_B1, SW_BST, VANA	Voltage on input power connections	–0.3	6	V
SW_B0, SW_B1	Voltage on buck switch nodes	–0.3	(VIN_Bx + 0.3 V) with 6-V maximum	V
FB_B0, FB_B1	Voltage on buck voltage sense nodes	–0.3	(VANA + 0.3 V) with 6-V maximum	V
VOUT_BST	Voltage on boost output	–0.3	6	V
SCL (EN2), SDA (EN3), VMON1, VMON2	Voltage on voltage monitoring pins	–0.3	(VANA + 0.3 V) with 6-V maximum	V
NRST, EN1, nINT	Voltage on logic pins (input or output pins)	–0.3	6	V
PG0, PG1 (GPO1), GPO0, CLKIN (GPO2), WDI, WD_RESET	Voltage on logic pins (input or output pins)	–0.3	(VANA + 0.3 V) with 6-V maximum	V
T_{J-MAX}	Junction temperature	−40	150	°C
T_{stg}	Storage temperature	–65	150	°C
Maximum lead temperature (soldering, 10 sec.)			260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 8, 9, 16, 17, 24, 25, 32)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
INPUT VOLTAGE				
VIN_B0, VIN_B1, SW_BST, VANA	Voltage on input power connections	2.8	5.5	V
VMON1, VMON2	Voltage on voltage monitoring pins	0	5.5	V
NRST, EN1, EN2, EN3, nINT	Voltage on logic pins (input or output pins)	0	5.5	
PG0, PG1 (GPO1), GPO0, CLKIN (GPO2), WDI, WD_RESET	Voltage on logic pins (input or output pins)	0	VANA	V
SCL, SDA	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes	0	1.95	V
	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), and Fast+ (1 MHz) Modes	0	VANA with 3.6-V maximum	V
TEMPERATURE				
Junction temperature, T_J		−40	140	°C

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Ambient temperature, T_A	−40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	17.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL COMPONENTS						
C_{IN_BUCK}	Input filtering capacitance for buck converters	Effective capacitance, connected from VIN_Bx to PGND_Bx	1.9	10		µF
C_{OUT_BUCK}	Output filtering capacitance for buck converters	Effective total capacitance. Maximum includes POL capacitance	15	22	100	µF
$C_{OUT\_BUCK\_POL}$	Point-of-load (POL) capacitance for buck converters	Optional POL capacitance		22		µF
C_{OUT_BST}	Output filtering capacitance for boost converter	Effective capacitance	10	22	40	µF
ESR_C	Input and output capacitor ESR	[1-10] MHz		2	10	mΩ
L_{BUCK}	Inductor for buck converters	Inductance of the inductor		0.47		µH
			–30%		30%	
L_{BST}	Inductor for boost converters	Inductance of the inductor, 2-MHz switching		1		µH
		Inductance of the inductor, 4-MHz switching		1		
		Inductance of the inductor	–30%		30%	
DCR_L	Inductor DCR			25		mΩ
BUCK CONVERTERS						
$V_{(VIN\_Bx)}$, $V_{(VANA)}$	Input voltage range		2.8	3.3	5.5	V
V_{OUT_Bx}	Output voltage	Programmable voltage range	0.7	1	3.36	V
		Step size, 0.7 V ≤ V_{OUT} < 0.73 V		10		mV
		Step size, 0.73 V ≤ V_{OUT} < 1.4 V		5		
		Step size, 1.4 V ≤ V_{OUT} ≤ 3.36 V		20		
I_{OUT_Bx}	Output current	Output current			3.5 (3)	A

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Minimum voltage difference between $V_{(VIN\_Bx)}$ and V_{OUT_Bx} for electrical characteristics	$V_{(VIN\_Bx)} – V_{OUT}$, I_{OUT_Bx} ≤ 2 A	0.8			V
		$V_{(VIN\_Bx)} – V_{OUT}$, I_{OUT_Bx} > 2 A	1			
	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	Force PWM mode, V_{OUT} < 1.0 V	–20		20	mV
		Force PWM mode, V_{OUT} ≥ 1.0 V	–2%		2%	
		PFM mode, V_{OUT} < 1.0 V, the average output voltage level is increased by max. 20 mV	–20		40	mV
		PFM mode, V_{OUT} ≥ 1.0 V, the average output voltage level is increased by max. 20 mV	–2%		2% + 20mV	
	Ripple voltage	PWM mode, V_{OUT} = 1.2 V, f_{SW} = 4 MHz, C_{OUT} = 22 + 22 µF (GCM31CR71A226KE02)		5		mV_{p-p}
		PFM mode, L = 0.47 µH, C_{OUT} = 22 + 22 µF (GCM31CR71A226KE02)		25		
DC_{LNR}	DC line regulation	I_{OUT} = $I_{OUT(max)}$		±0.05		%/V
DC_{LDR}	DC load regulation in PWM mode	V_{OUT_Bx} = 1.0 V, I_{OUT} from 0 to $I_{OUT(max)}$		0.3%		
T_{LDSR}	Transient load step response	I_{OUT} = 0 A to 3 A, T_R = T_F = 1 µs, PWM mode, V_{VIN_Bx} = 3.3V, V_{OUT_Bx} = 1.2 V, C_{OUT} = 22 + 22 µF, L = 0.47 µH, f_{SW} = 4 MHz		±65		mV
T_{LNSR}	Transient line response	$V_{(VIN\_Bx)}$ stepping 3 V ↔ 3.5 V, T_R = T_F = 10 µs, I_{OUT} = $I_{OUT(max)}$		±20		mV
$I_{LIM\ FWD}$	Forward current limit for both bucks (peak for every switching cycle)	Programmable range	1.5		4.5	A
		Step size		0.5		
		Accuracy, $V_{(VIN\_Bx)}$ ≥ 3 V, I_{LIM} = 4 A	–5%	7.5%	20%	
		Accuracy, 2.8 V ≤ $V_{(VIN\_Bx)}$ < 3 V, I_{LIM} = 4 A	–20%	7.5%	20%	
$I_{LIM\ NEG}$	Negative current limit		1.6	2	3	A
$R_{DS(ON)\ BUCK\ HS\ FET}$	On-resistance, high-side FET	Each phase, between VIN_Bx and SW_Bx pins (I = 1.0 A)		60	110	mΩ
$R_{DS(ON)\ BUCK\ LS\ FET}$	On-resistance, low-side FET	Each phase, between SW_Bx and PGND_Bx pins (I = 1.0 A)		55	80	mΩ
f_{SW}	Switching frequency, PWM mode OTP programmable	2-MHz setting or V_{OUT_Bx} < 0.8 V	1.8	2	2.2	MHz
		3-MHz setting and V_{OUT_Bx} ≥ 0.8 V	2.7	3	3.3	
		4-MHz setting and V_{OUT_Bx} ≥ 1.1 V	3.6	4	4.4	
	Start-up time (soft start)	From ENx to V_{OUT_Bx} = 0.35 V (slew-rate control begins)		120		µs
	Overshoot during start-up				50	mV
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 010, V_{VOUT_Bx} ≥ 0.7 V	–15%	10	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 011, V_{VOUT_Bx} ≥ 0.7 V	–15%	7.5	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 100, V_{VOUT_Bx} ≥ 0.7 V	–15%	3.8	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 101, V_{VOUT_Bx} ≥ 0.7 V	–15%	1.9	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 110, V_{VOUT_Bx} ≥ 0.7 V	–15%	0.94	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 111, V_{VOUT_Bx} ≥ 0.7 V	–15%	0.47	15%	mV/µs

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PFM-PWM}$	PFM-to-PWM switch - current threshold(5)			520		mA
$I_{PWM-PFM}$	PWM-to-PFM switch - current threshold(5)			240		mA
	Output pull-down resistance	Converter disabled	75	125	175	Ω
BOOST CONVERTER						
V_{IN_BST}	Input voltage range for boost power inputs		2.8	3.3	4	V
	Input voltage range when bypass switch mode selected		4.5		5.5	V
V_{OUT_BST}	Output voltage, boost mode	BOOST_VSET = 00		4.9		V
		BOOST_VSET = 01		5.0		
		BOOST_VSET = 10		5.1		
		BOOST_VSET = 11		5.2		
I_{OUT_BST}	Output current	Both boost and bypass mode			0.6	A
I_{LIM_BST}	Output current limit	BOOST_ILIM = 00, V_{IN_BST} < 3.6 V	0.8	1	1.3	A
		BOOST_ILIM = 01, V_{IN_BST} < 3.6 V	1.1	1.4	1.9	
		BOOST_ILIM = 10, V_{IN_BST} < 3.6 V	1.5	1.9	2.3	
		BOOST_ILIM = 11, V_{IN_BST} < 3.6 V	2.2	2.8	3.4	
$V_{OUT\_BST\_DC}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature. Boost mode	Default output voltage	–3%		3%	
V_{DROP}	Voltage drop, bypass mode,	Iout = 250 mA			83	mV
	Ripple voltage, boost mode	22 µF effective output capacitance		20		mV_{p-p}
DC_{LDR}	DC load regulation, boost mode	I_{OUT} = 1 mA to $I_{OUT(max)}$		0.3%		
T_{LDSR}	Transient load step response, boost mode	I_{OUT} = 1 mA to 250 mA, T_R = T_F = 1 µs, 22 µF effective output capacitance, VIN > 3 V	–220		220	mV
I_{SHORT}	Short circuit current limitation	During start-up, both boost and bypass mode. Short circuit current limit applies until V_{OUT_BST} = V_{IN_BST}		625		mA
$R_{DS(ON)}$ BST HS FET	On-resistance, high-side FET	Pin-to-pin, between SW_BST and VOUT_BST pins (I = 250 mA)		145	220	mΩ
$R_{DS(ON)}$ BST LS FET	On-resistance, low-side FET	Pin-to-pin, between SW_BST and PGND_BST pins (I = 250 mA)		90	175	mΩ
f_{SW}	Switching frequency, boost mode	2-MHz setting	1.8	2	2.2	MHz
		4-MHz setting	3.6	4	4.4	MHz
	Start-up time, boost mode	From enable to boost VOUT within 3% of target value. C_{OUT_BST} = 22 µF		450		µs
	Output pull-down resistance	Converter disabled		135		Ω
EXTERNAL CLOCK AND PLL						

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External input clock(6)	Nominal frequency	1		24	MHz
	Nominal frequency step size		1		
	Required accuracy from nominal frequency	–30%		10%	
External clock detection	Delay for detecting loss of external clock, nominal internal clock, clock accuracy ±10%			1.8	µs
	Delay for detecting valid external clock, nominal internal clock, clock accuracy ±10%			20	
Clock change delay (internal to external)	Delay from valid clock detection to use of external clock		600		µs
PLL output clock jitter	Cycle to cycle		300		ps, p-p
MONITORING FUNCTIONS					
VANA Voltage Monitoring	Voltage threshold, VANA_THRESHOLD = 0		3.3		V
	Voltage threshold, VANA_THRESHOLD = 1		5.0		
	Voltage window, VANA_WINDOW = 00	±3%	±4%	±5%	
	Voltage window, VANA_WINDOW = 01	±4%	±5%	±6%	
	Voltage window, VANA_WINDOW = 10 or 11	±9%	±10%	±11%	
VMON1 and VMON2 Voltage Monitoring Thresholds	VMONx_THRESHOLD = 000		0.65		V
	VMONx_THRESHOLD = 001		0.8		
	VMONx_THRESHOLD = 010		1.0		
	VMONx_THRESHOLD = 011		1.1		
	VMONx_THRESHOLD = 100		1.2		
	VMONx_THRESHOLD = 101		1.3		
	VMONx_THRESHOLD = 110		1.8		
	VMONx_THRESHOLD = 111		1.8		
VMON1 and VMON2 Voltage Monitoring Windows	VMONx_WINDOW = 00, VMONx_THRESHOLD from 000 to 111	±1%	±2%	±3%	
	VMONx_WINDOW = 01, VMONx_THRESHOLD from 000 to 111	±2%	±3%	±4%	
	VMONx_WINDOW = 10, VMONx_THRESHOLD from 000 to 111	±3%	±4%	±5%	
	VMONx_WINDOW = 11, VMONx_THRESHOLD from 000 to 111	±5%	±6%	±7%	
Buck0 and Buck1 Voltage Monitoring Windows	BUCKx_WINDOW = 00	±20	±30	±40	mV
	BUCKx_WINDOW = 01	±37	±50	±63	
	BUCKx_WINDOW = 10	±57	±70	±83	
	BUCKx_WINDOW = 11	±77	±90	±103	
Boost Voltage Monitoring	BOOST_WINDOW = 00	±0.6%	±2%	±3.4%	
	BOOST_WINDOW = 01	±2.6%	±4%	±5.4%	
	BOOST_WINDOW = 10	±4.6%	±6%	±7.4%	
	BOOST_WINDOW = 11	±6.6%	±8%	±9.4%	
Deglitch time	VANA, VMONx and BOOST monitoring	12		17	µs
	BUCKx monitoring	6		9	
PROTECTION FUNCTIONS					
Thermal warning	Temperature rising, TDIE_WARN_LEVEL = 0	115	125	135	°C
	Temperature rising, TDIE_WARN_LEVEL = 1	130	140	150	
	Hysteresis		20		

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Thermal shutdown	Temperature rising	140	150	160	°C
		Hysteresis		20		
$VANA_{OVP}$	VANA Overvoltage	Voltage rising, VANA_OVP_SEL = 0	5.6	5.8	6.1	V
		Voltage falling, VANA_OVP_SEL = 0	5.45	5.73	5.96	
		Voltage rising, VANA_OVP_SEL = 1	4.1	4.3	4.6	
		Voltage falling, VANA_OVP_SEL = 1	3.95	4.23	4.46	
		Hysteresis	40		200	mV
$VANA_{UVLO}$	VANA Undervoltage Lockout	Voltage rising	2.51	2.63	2.75	V
		Voltage falling	2.5	2.6	2.7	
	BUCKx short circuit detection	Threshold	0.32	0.35	0.45	V
	Bypass short circuit current limit			270	420	mA
LOAD CURRENT MEASUREMENT FOR BUCK CONVERTERS						
	Current measurement range	Current corresponding to maximum output code (note: maximum current for LP87702 buck is 3.5A)			10.22	A
	Resolution	LSB		20		mA
	Measurement accuracy	I_{OUT} > 1A		<10%		
	Measurement time	Auto mode (automatically changing to PWM mode for the measurement)		50		µs
		PWM mode			25	
CURRENT CONSUMPTION						
	Shutdown current consumption	NRST = 0		1		µA
	Standby current consumption, converters disabled	NRST = 1		9		µA
	Active current consumption, one buck converter enabled in Auto mode, internal RC oscillator	I_{OUT_Bx} = 0 mA, not switching		55		µA
	Active current consumption, two buck converters enabled in Auto mode, internal RC oscillator	I_{OUT_Bx} = 0 mA, not switching		90		µA
	Active current consumption during PWM operation, one buck converter enabled	I_{OUT_Bx} = 0 mA		15		mA
	Active current consumption during PWM operation, two buck converters enabled	I_{OUT_Bx} = 0 mA		27		mA
	Active current consumption, Boost converter in PWM operation	I_{OUT_BST} = 0 mA, f_{SW} = 4 MHz		18		mA
	PLL and clock detector current consumption	Additional current consumption when enabled, 2 MHz external clock		2		mA

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT SIGNALS SCL, SDA, NRST, EN1, EN2, EN3, CLKIN, WDI						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.2			
V_{HYS}	Hysteresis of Schmitt Trigger inputs		10	80	200	mV
	ENx, CLKIN, WDI pull-down resistance	ENx_PD = 1, CLKIN_PD = 1, WDI_PD = 1		500		kΩ
	NRST pull-down resistance	Always enabled		500		kΩ
DIGITAL OUTPUT SIGNALS nINT, SDA						
V_{OL}	Output low level	SDA: I_{SOURCE} = 20 mA			0.5	V
		nINT: I_{SOURCE} = 2 mA			0.4	
R_P	External pull-up resistor for nINT	To VIO Supply		10		kΩ
DIGITAL OUTPUT SIGNALS PGOOD, PG1, GPO0, GPO1, GPO2, WD_RESET						
V_{OL}	Output low level	I_{SOURCE} = 2 mA			0.4	V
V_{OH}	Output high level, configured to push-pull	I_{SINK} = 2 mA	V_{VANA} - 0.4		V_{VANA}	
V_{PU}	Supply voltage for external pull-up resistor, configured to open-drain				V_{VANA}	
R_{PU}	External pull-up resistor, configured to open-drain			10		kΩ
ALL DIGITAL INPUTS						
I_{LEAK}	Input current	All logic inputs except NRST, over pin voltage range, when PD not enabled	–1		1	µA
		NRST, over pin voltage range. Other logic inputs when PD enabled.	–1		20	µA

(1) All voltage values are with respect to network ground.
(2) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis.
(3) The maximum output current can be limited by the forward current limit $I_{LIM\ FWD}$. The maximum output current is also limited by the junction temperature and maximum average current over lifetime. The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length of the current pulse, efficiency, board and ambient temperature.
(4) The slew-rate can be limited by the current limit (forward or negative current limit), output capacitance and load current. Applies when internal oscillator is used.
(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level.
(6) The external clock frequency must be selected so that buck switching frequency is above 1.7 MHz.

7.6 I²C Serial Bus Timing Parameters

See (1).			MIN	MAX	UNIT
f_{SCL}	Serial clock frequency	Standard mode		100	kHz
		Fast mode		400	
		Fast mode +		1	MHz
		High-speed mode, C_b = 100 pF		3.4	
		High-speed mode, C_b = 400 pF		1.7	
t_{LOW}	SCL low time	Standard mode	4.7		µs
		Fast mode	1.3		
		Fast mode +	0.5		
		High-speed mode, C_b = 100 pF	160		ns
		High-speed mode, C_b = 400 pF	320		
t_{HIGH}	SCL high time	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode, C_b = 100 pF	60		ns
		High-speed mode, C_b = 400 pF	120		
$t_{SU;DAT}$	Data setup time	Standard mode	250		ns
		Fast mode	100		
		Fast mode +	50		
		High-speed mode	10		
$t_{HD;DAT}$	Data hold time	Standard mode	0.01	3.45	µs
		Fast mode	0.01	0.9	
		Fast mode +	0.01		
		High-speed mode, C_b = 100 pF	10	70	ns
		High-speed mode, C_b = 400 pF	10	150	
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard mode	4.7		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
t_{BUF}	Bus free time between a stop and start condition	Standard Mode	4.7		µs
		Fast Mode	1.3		
		Fast mode +	0.5		
$t_{SU;STO}$	Setup time for a stop condition	Standard Mode	4		µs
		Fast Mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
t_{rDA}	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	

See (1).			MIN	MAX	UNIT
t_{fDA}	Fall time of SDA signal	Standard mode		250	ns
		Fast mode	20+0.1 C_b	250	
		Fast mode +	20+0.1 C_b	120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	
t_{rCL}	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	40	
		High-speed mode, C_b = 400 pF	20	80	
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	
t_{fCL}	Fall time of a SCL signal	Standard mode		300	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +	20+0.1 C_b	120	
		High-speed mode, C_b = 100 pF	10	40	
		High-speed mode, C_b = 400 pF	20	80	
C_b	Capacitive load for each bus line (SCL and SDA)			400	pF
t_{SP}	Pulse width of spike suppressed (Spikes shorter than indicated width are suppressed)	Fast mode, Fast mode +		50	ns
		High-speed mode		10	

(1) C_b refers to the capacitance of one bus line. C_b is expressed in pF units.

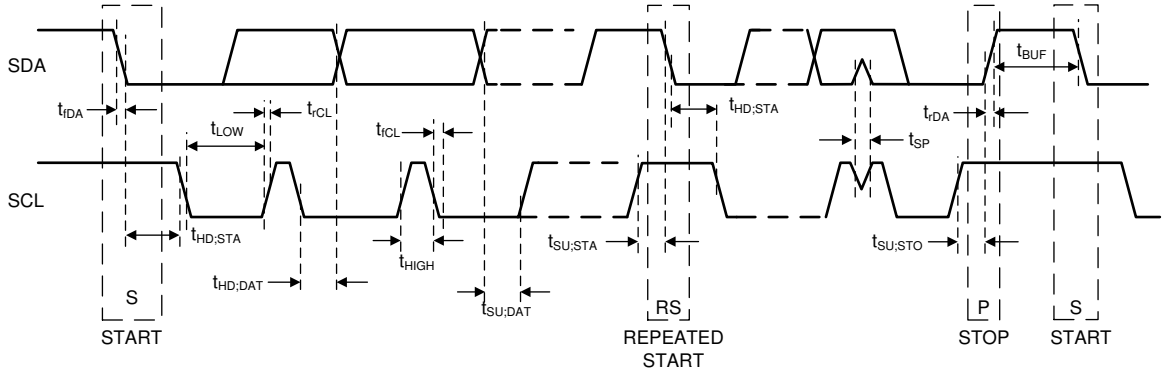


図 7-1. I²C Timing

7.7 Typical Characteristics

Unless otherwise specified: V_{IN} = 3.3 V, T_A = 25°C, f_{SW} -setting 4 MHz, L0 = L1 = 0.47 µH (TOKO DFE252012PD-R47M), L2 = 1 µH (TFM252012ALMA1R0), C_{OUT_BUCK} = 22 µF, and C_{POL_BUCK} = 22 µF, C_{OUT_BOOST} = 22 µF. Measurements are done using connections in the 図 9-1.

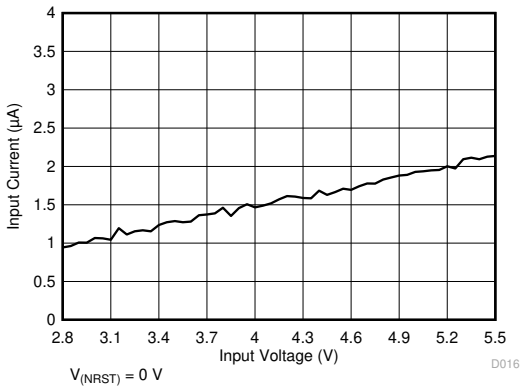


図 7-2. Shutdown Current Consumption vs Input Voltage

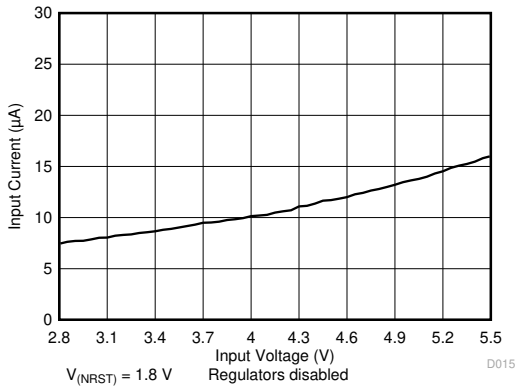


図 7-3. Standby Current Consumption vs Input Voltage

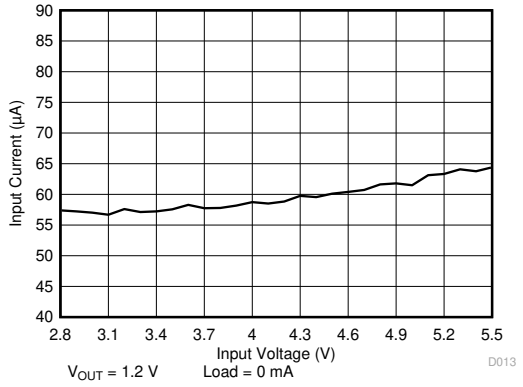


図 7-4. Active State Current Consumption vs Input Voltage, One Buck Converter Enabled in PFM Mode

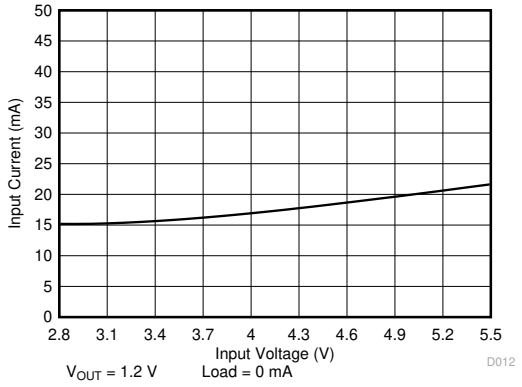


図 7-5. Active State Current Consumption vs Input Voltage, One Buck Converter Enabled in PWM Mode

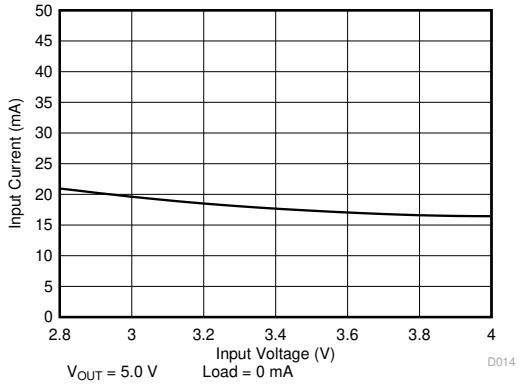


図 7-6. Active State Current Consumption vs Input Voltage, Boost Converter Enabled in PWM Mode

8 Detailed Description

8.1 Overview

The LP87702-Q1 is a high-efficiency, high-performance power supply IC with two step-down DC/DC converters (Buck0 and Buck1) and boost converter for automotive and industrial applications. The input voltage range is from 2.8 V to 5.5 V. The typical application input voltage levels are 3.3 V and 5 V. $VANA_{OVP}$ is set to 4.3 V (typical) with 3.3 V input and boost enabled. The boost can be used as a load switch and $VANA_{OVP}$ is set to 5.8 V (typical) when input voltage is 5 V. $VANA_{OVP}$ is selected in OTP by VANA_OVP_SEL and is a fixed factory setting. 表 8-1 lists the output characteristics of the various converters.

表 8-1. Supply Specification

SUPPLY	OUTPUT		
	V_{OUT} RANGE (V)	RESOLUTION (mV)	I_{MAX} MAXIMUM OUTPUT CURRENT (mA)
Boost	4.9 to 5.2	100	600
Buck0	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3500
Buck1	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3500

The LP87702-Q1 converters support switching clock synchronization to an external clock connected to CLKIN input. The external clock can be from 1 MHz to 24 MHz with 1-MHz steps. Alternatively, optional spread spectrum mode can be enabled to reduce EMI.

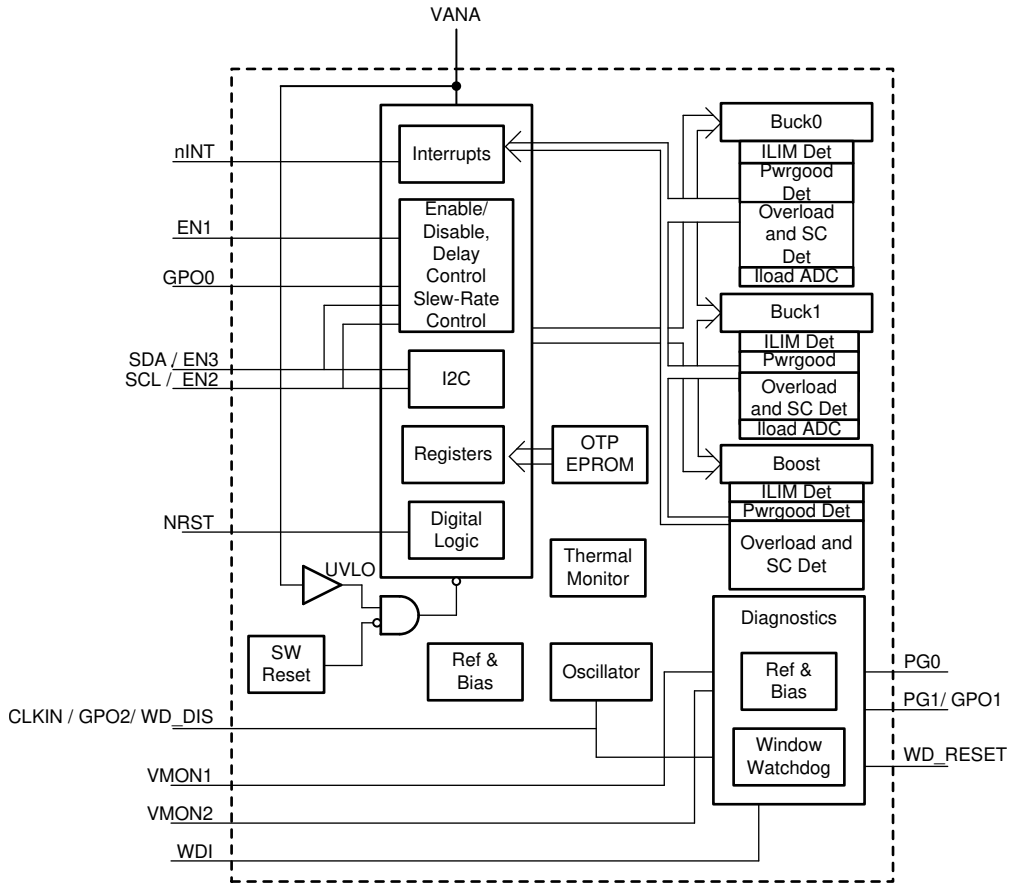
LP87702-Q1 features include diagnostics, monitoring, and protections for the devices internal and system level operation, which are the following:

- Soft start
- Input undervoltage lockout
- Programmable undervoltage or window (overvoltage and undervoltage) monitoring for the input (from VANA pin)
- Programmable undervoltage or window (overvoltage and undervoltage) monitoring for the buck and boost converter outputs
- Two inputs (VMONx) with programmable undervoltage or window (overvoltage and undervoltage) thresholds, for monitoring external rails in the system
- One dedicated power-good output (PG0) to which selected monitoring signals can be combined
- Second programmable power-good output (PG1), multiplexed with general purpose output (GPO1)
- Power good flags with maskable interrupt
- Programmable window watchdog
- Buck and boost converter overload detection
- Thermal warning with two selectable thresholds
- Thermal shutdown

LP87702-Q1 control interface:

- Up to three enable inputs (EN1, EN2, and EN3) with programmable power-up or power-down sequence control
- Optional I2C (multiplexed with EN2 and EN3 inputs)
- Interrupt signal (nINT) to host
- Reset input (NRST)
- One dedicated general purpose output (GPO0)
- Watchdog disable WD_DIS, multiplexed with CLKIN/GPO2

8.2 Functional Block Diagram



8.3 Feature Descriptions

8.3.1 Step-Down DC/DC Converters

8.3.1.1 Overview

The LP87702-Q1 includes two high-efficiency step-down DC/DC converters. The buck converters deliver 0.7-V to 3.36-V regulated voltage rails from 2.8-V to 5.5-V input-supply voltage. The converters are designed for flexibility; most of the functions are programmable, thus optimizing the converter operation for each application:

- DVS support with programmable slew rate
- Automatic mode control based on the loading (PWM or PFM mode)
- Forced PWM mode option
- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Programmable output voltage monitoring with maskable interrupt and selectable connection PG0 or PG1
- Average output current sensing (for PFM entry and load current measurement)

Some of the key parameters that can be programmed through the registers (with default values set by OTP bits):

- Output voltage
- Forced PWM operation
- Switch current limit
- Output voltage slew rate
- Enable and disable delays with ENx pin control

There are two modes of operation for the buck converters, depending on the output current required: pulse width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 520 mA or higher. Lighter output current loads will cause the converter to automatically switch into PFM mode for reduced current consumption when forced PWM mode is disabled. The forced PWM mode can be selected to maintain fixed switching frequency at all load currents. When buck is disabled, buck output is isolated from the input voltage rail. Output has an optional pulldown resistor.

図 8-1 shows a block diagram of a single buck converter.

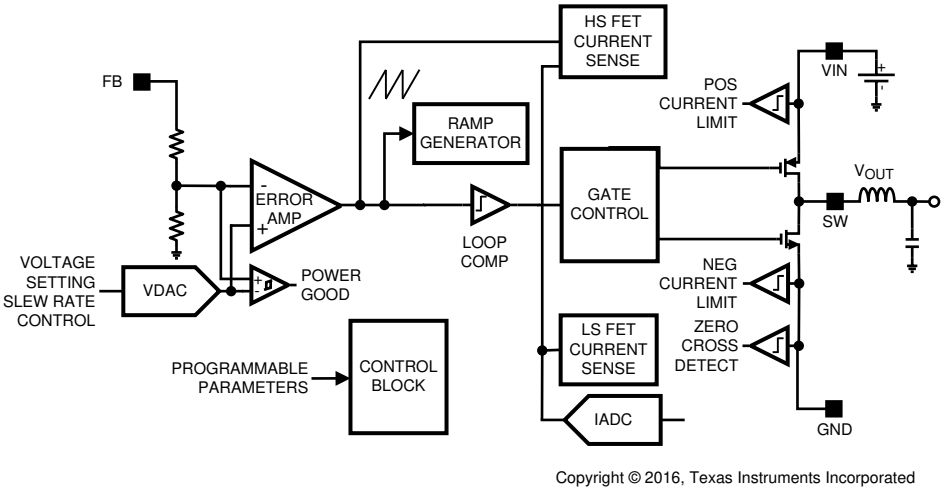


図 8-1. Detailed Block Diagram Showing One Buck Converter

8.3.1.2 Transition Between PWM and PFM Modes

The LP87702-Q1 buck converter operates in PWM mode at load current of about 520 mA or higher. The device automatically switches into PFM mode for reduced current consumption when forced PWM mode is disabled (AUTO mode operation) at lighter load current levels. A high efficiency is achieved over a wide output-load current range by combining the PFM and the PWM modes.

8.3.1.3 Buck Converter Load Current Measurement

Buck load current can be monitored through the I^2C registers. The monitored buck converter is selected with the LOAD_CURRENT_BUCK_SELECT bit in the SEL_I_LOAD register. A write to this selection register starts a current measurement sequence. The converter is forced to PWM mode during the measurement. The measurement sequence is 50 µs long at maximum. LP87702-Q1 can be configured to give out an I_MEAS_INT interrupt in the INT_TOP_1 register after the load current measurement sequence is finished. Load current measurement interrupt can be masked with I_MEAS_MASK bit in TOP_MASK_1 register. The measurement result can be read from I_LOAD_1 and I_LOAD_2 registers. The buck converter load current measurement result is 9-bit wide, with 8 LSB bits stored in I_LOAD_1 register and 1 MSB bit stored in I_LOAD_2 register. The single bit resolution is 20 mA, with a maximum load current value of 10.22 A.

8.3.2 Boost Converter

The LP87702-Q1 device integrates a boost converter with programmable output voltage from 4.9 V to 5.2 V in 0.1 V steps, and input voltage range from 2.8 V to 4 V (3 V to 4 V in P87702D). The boost converter has flexibility to support wide range of application conditions:

- Forced PWM operation
- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Programmable output voltage monitoring with maskable interrupt and selectable connection to PG0 and PG1 or both

The following parameters can be programmed through the registers, with default values set by the OTP bits (unless otherwise noted):

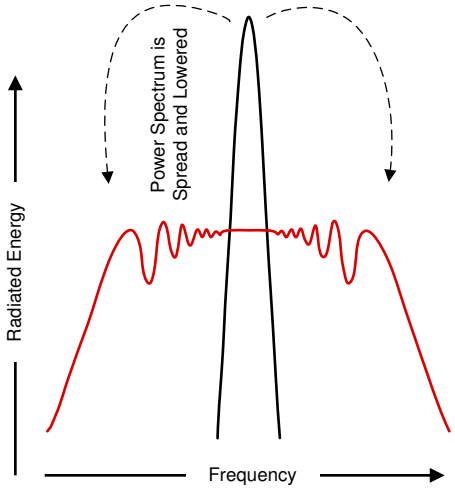
- Output voltage level (BOOST_VSET)
- Switch current limit (BOOST_ILIM)
- Enable and disable delays when ENx pin control is used (BOOST_DELAY register)
- Output pulldown resistor enable or disable when boost is disabled (BOOST_RDIS_EN bit, discharge is enabled by default)
- Output voltage monitoring enable or disable and monitoring window thresholds

The boost converter operates in forced PWM mode with fixed switching frequency across all load currents. When boost is disabled, boost output is isolated from the input voltage rail.

Boost converter supports an alternative operating mode as a bypass or load switch, with input voltage range from 4.5 V to 5.5 V. Operating mode is selected in OTP and is fixed; changing the mode on-the-fly is not supported. Bypass mode is not supported in P87702D.

8.3.3 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP87702-Q1 device supports the spread-spectrum switching frequency modulation mode that is register controlled. This mode minimizes the need for output filters, ferrite beads, or chokes. The switching frequency varies between 0.85 × f_{SW} and f_{SW} in spread spectrum mode, where f_{SW} is switching the frequency selected in the OTP. Spread Spectrum Modulation shows how the spread spectrum modulation reduces conducted and radiated emissions by the converter and associated passive components and PCB traces. This feature is available only when internal RC oscillator is used (EN_PLL is 0 in PLL_CTRL register) and it is enabled with the EN_SPREAD_SPEC bit in CONFIG register, and it affects both buck converters and the boost converter.



Where a fixed frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP87702-Q1 spreads that energy over a large bandwidth.

図 8-2. Spread Spectrum Modulation

8.3.4 Sync Clock Functionality

The LP87702-Q1 device contains a CLKIN input to synchronize buck and boost converters' switching clock with the external clock. 図 8-3 shows the block diagram of the clocking and PLL module. 表 8-2 shows how the external clock is selected and interrupt is generated depending on the EN_PLL bit in PLL_CTRL register and the external clock availability. The interrupt can be masked with SYNC_CLK_MASK bit in TOP_MASK_1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits in PLL_CTRL register and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%/ +10%) for valid clock detection.

The SYNC_CLK_INT interrupt in INT_TOP_1 register is also generated in cases the external clock is expected but it is not available. These cases are Startup (Read OTP-to-standby transition) when EN_PLL = 1 and buck or boost converter is enabled (standby-to-active transition) when EN_PLL = 1.

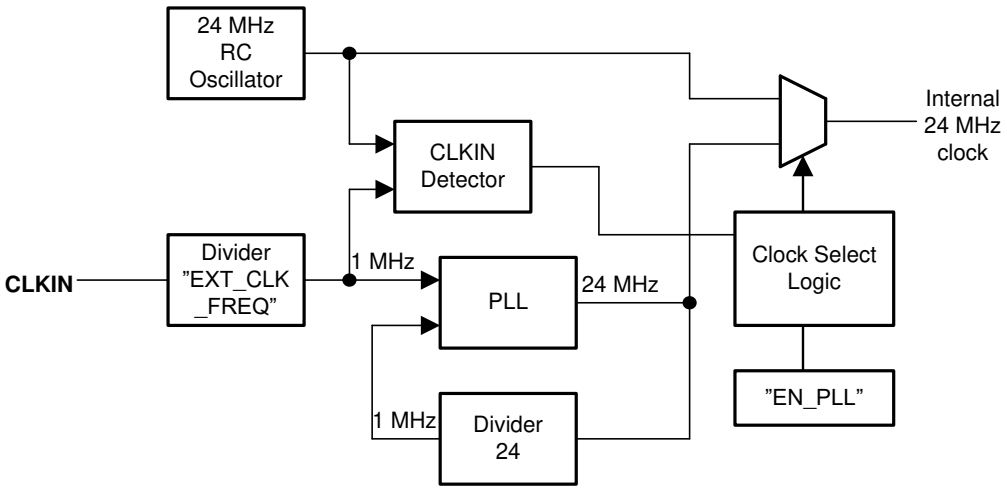


図 8-3. Clock and PLL Module

表 8-2. PLL Operation

DEVICE OPERATION MODE	EN_PLL	PLL AND CLOCK DETECTOR STATE	INTERRUPT FOR EXTERNAL CLOCK	CLOCK
STANDBY	0	Disabled	No	Internal RC
ACTIVE	0	Disabled	No	Internal RC
STANDBY	1	Enabled	When external clock disappears or appears	Automatic change to internal RC oscillator when External clock is not available
ACTIVE	1	Enabled	When external clock disappears or appears	Automatic change to internal RC oscillator when External clock is not available

8.3.5 Power-Up

The power-up sequence for the LP87702-Q1 is as follows:

- VANA (and VIN_Bx) reach minimum recommended levels (V_{VANA} > $VANA_{UVLO}$).
- Driving the NRST input high initiates OTP read and enables the system I/O interface. Minimum delay from the NRST reset input rising edge to I2C write or read access is 1.2 ms.
- Device enters STANDBY mode. Watchdog operation starts.
- The host can change the default register setting by I^2C if needed.
- The converters can be enabled or disabled and the GPOx signals can be controlled by ENx pins and by I^2C interface.

8.3.6 Buck and Boost Control

8.3.6.1 Enabling and Disabling Converters

The buck converters can be enabled when the device is in STANDBY or ACTIVE state. There are two ways to enable and disable the buck converters:

- Using BUCKx_EN bit in BUCKx_CTRL_1 register (BUCKx_EN_PIN_CTRL bit is 00 in BUCKx_CTRL_1 register)
- Using ENx control pin (BUCKx_EN bit is 1 in BUCKx_CTRL_1 register *and* BUCKx_EN_PIN_CTRL bit is not 00 in BUCKx_CTRL_1 register)

Similarly there are two ways to enable and disable the boost converter:

- Using BOOST_EN bit in BOOST_CTRL register (BOOST_EN_PIN_CTRL bit is 0 in BOOST_CTRL register)
- Using ENx control pin (BOOST_EN bit is 1 in BOOST_CTRL register *and* BOOST_EN_PIN_CTRL bit is not 00 in BOOST_CTRL register)

If the ENx control pin is used to enable and disable, then the delay from the control signal rising edge to start-up is set by BUCKx_STARTUP_DELAY[3:0] bits in BUCKx_DELAY register and BOOST_STARTUP_DELAY[3:0] bits in BOOST_DELAY register. The delay from falling edge of control signal to shutdown is set by BUCKx_SHUTDOWN_DELAY[3:0] bits in BUCKx_DELAY register and BOOST_SHUTDOWN_DELAY[3:0] bits in BOOST_DELAY register. The delays are valid only when ENx pin control is used, not when converters are enabled by I^2C write to BUCKx_EN and BOOST_EN bits.

The control of the converters (with 0-ms delays) is shown in 表 8-3.

表 8-3. Converter Control

	BUCKx_EN / BOOST_EN	BUCKx_EN_PIN_CTRL / BOOST_EN_PIN_CTRL	EN1 PIN	EN2 PIN	EN3 PIN	BUCKx OUTPUT VOLTAGE / BOOST OUTPUT VOLTAGE
Enable or disable control with BUCKx_EN/ BOOST_EN bit	0	Don't Care	Don't Care	Don't Care	Don't Care	Disabled
	1	00	Don't Care	Don't Care	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable or disable control with EN1 pin	1	01	Low	Don't Care	Don't Care	Disabled
	1	01	High	Don't Care	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable/disable control with EN2 pin	1	10	Don't Care	Low	Don't Care	Disabled
	1	10	Don't Care	High	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable or disable control with EN3 pin	1	11	Don't Care	Don't Care	Low	Disabled
	1	11	Don't Care	Don't Care	High	BUCKx_VSET[7:0] / BOOST_VSET[1:0]

図 8-4 shows how the BUCKx converter is enabled by an ENx pin or by I^2C write access. The soft-start circuit limits the in-rush current during start-up. The output voltage increase rate is typically 30 mV/µsec during soft start. The output voltage becomes slew-rate controlled when the output voltage rises to 0.35-V level. If there is a short circuit at the output and the output voltage does not increase above a 0.35-V level in 1 ms, the converter is disabled, and interrupt is set. When the output voltage rises above the undervoltage power-good threshold level the BUCKx_PG_INT interrupt flag in the INT_BUCK register is set.

Power-good thresholds are defined by BUCKx_WINDOW bits. A PGOOD_WINDOW bit in PGOOD_CTRL register sets the detection method for the valid buck output voltage, either undervoltage detection or undervoltage and overvoltage detection. The powergood interrupt flag can be masked using the BUCKx_PGR_MASK bit in the BUCK_MASK register when reaching the valid output voltage. The power-good interrupt flag can also be generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by BUCKx_PGF_MASK bit in BUCK_MASK register. When the window monitoring (under and overvoltage monitoring) is selected, the mask bits apply when voltage is crossing either threshold. A BUCKx_PG_STAT bit in BUCK_STAT register shows always the validity of the output voltage; '1' means valid, and '0' means invalid output voltage.

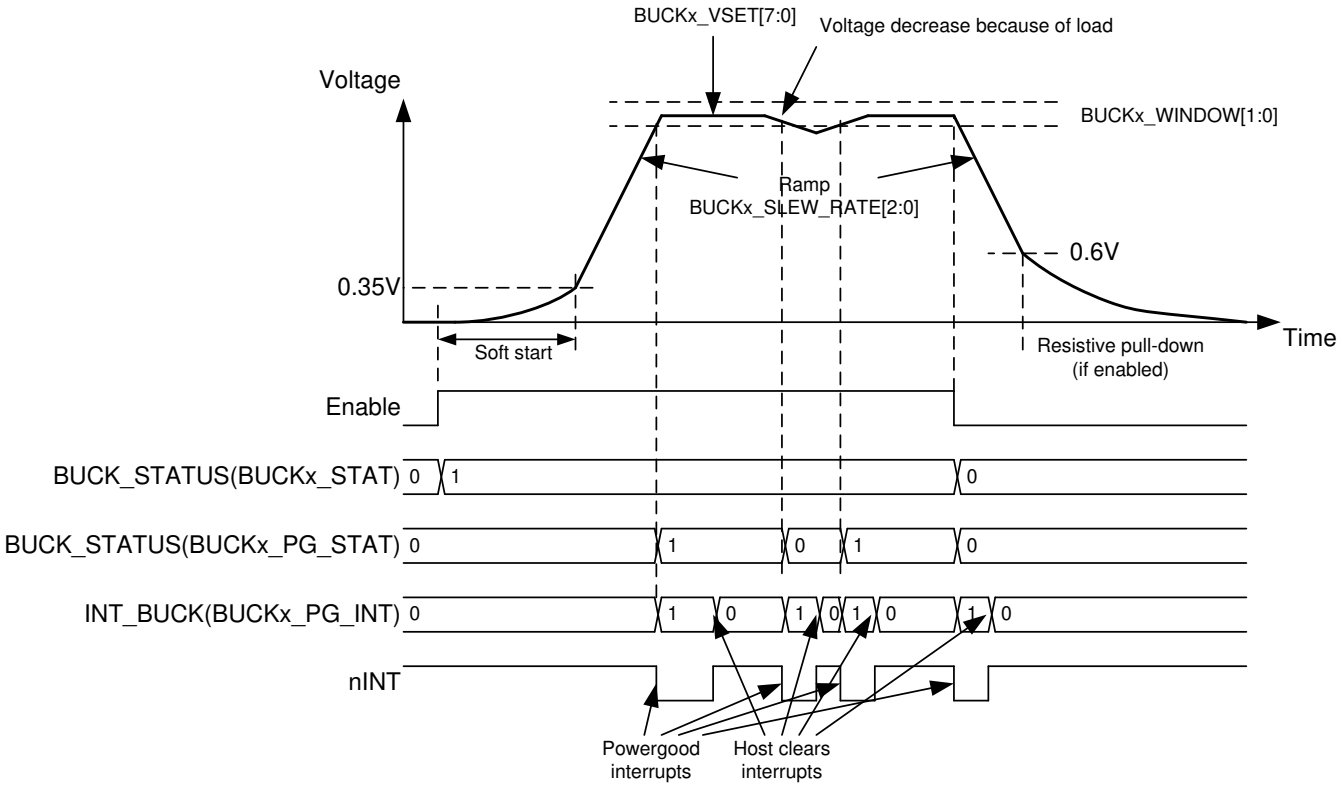


図 8-4. Buck Converter Enable and Disable

図 8-5 shows how the boost converter is enabled by an ENx pin or by I^2C write access. The soft-start circuit limits the in-rush current during start-up. The output voltage increase rate is less than 100 mV/µsec during soft start. If there is a short circuit at the output and the output voltage does not reach the input voltage level in 1 ms, the converter is disabled, and the interrupt is set. When the output voltage reaches the power-good threshold level, the BOOST_PG_INT interrupt flag in INT_BOOST register is set.

Power-good thresholds are defined by BOOST_WINDOW bits. A PGOOD_WINDOW bit in PGOOD_CTRL register sets the detection method for the valid boost output voltage, either undervoltage detection or undervoltage and overvoltage detection. The power-good interrupt flag, when reaching valid output voltage, can be masked using BOOST_PGR_MASK bit in BOOST_MASK register. The power-good interrupt flag can also be generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by the BOOST_PGF_MASK bit in BOOST_MASK register. A BOOST_PG_STAT bit in the BOOST_STAT register always shows the validity of the output voltage; '1' means valid and '0' means invalid output voltage.

The ENx input pins have integrated pulldown resistors. The pulldown resistors are enabled by default and host can disable those with ENx_PD bits in CONFIG register.

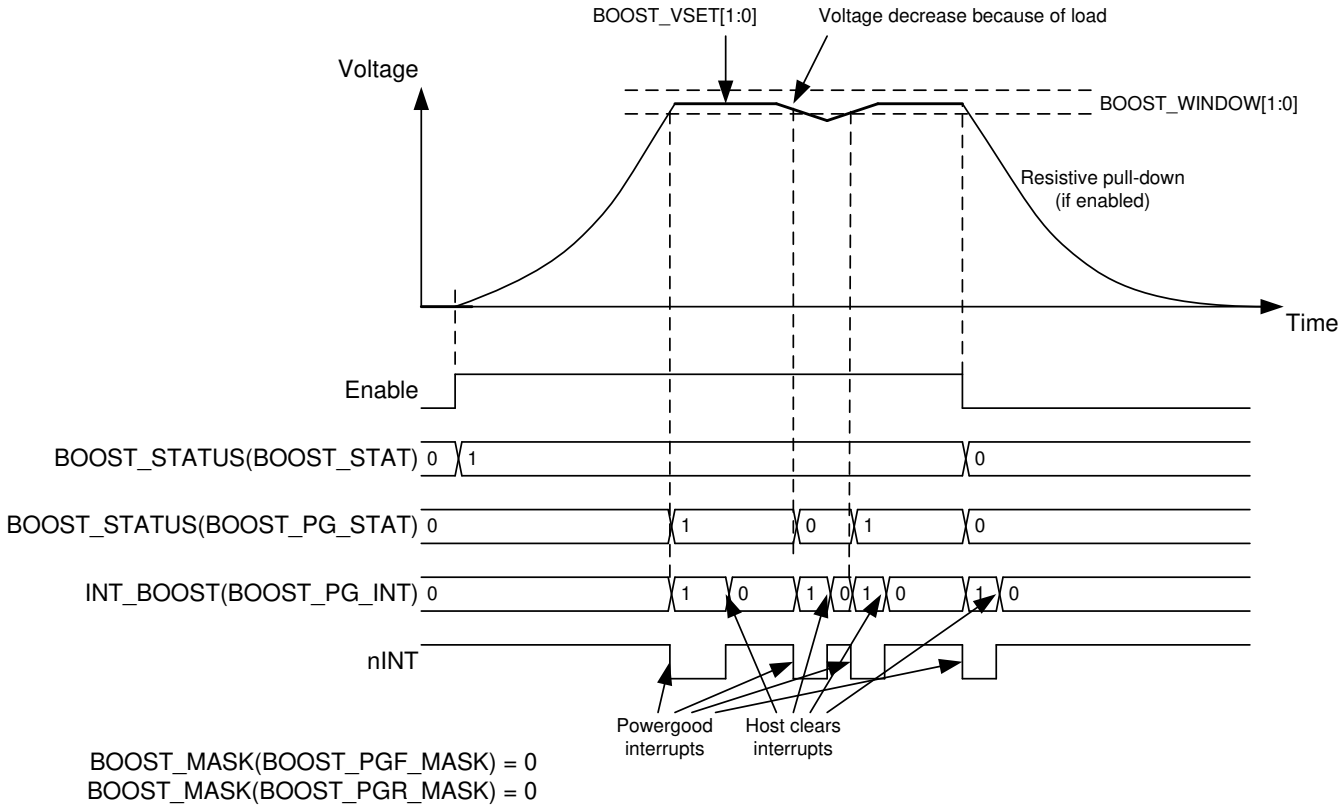


図 8-5. Boost Converter Enable and Disable

8.3.6.2 Changing Buck Output Voltage

The output voltage of BUCKx converter can be changed by writing to the BUCKx_VOUT register. The voltage change for buck converter is always slew-rate controlled, and the slew-rate is defined by the BUCKx_SLEW_RATE[2:0] bits in BUCKx_CTRL_2 register. The forced PWM mode is used automatically during a voltage change. When the programmed output voltage is achieved, the mode becomes the one defined by load current, and the BUCKx_FPWM bit.

図 8-6 shows the voltage change and power-good interrupts.

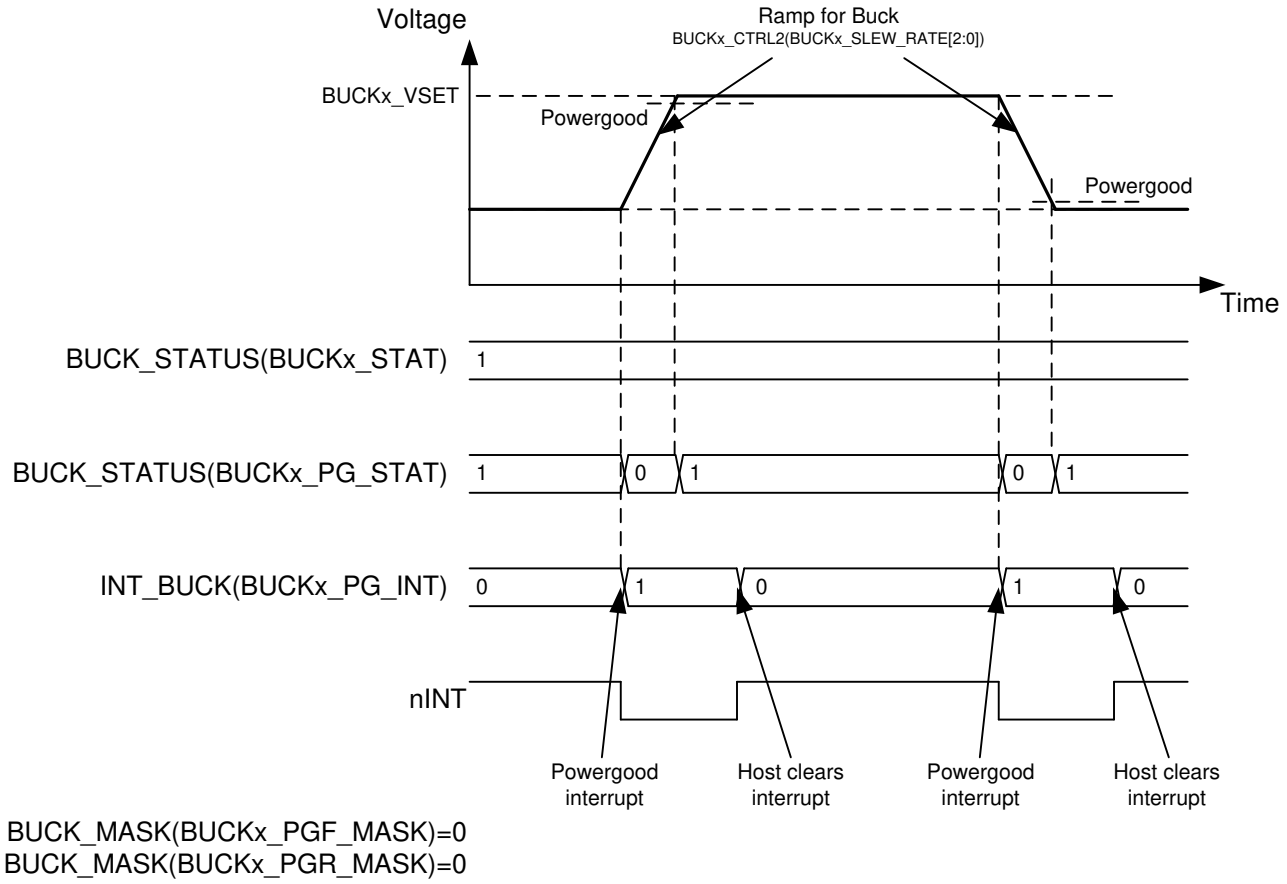


図 8-6. Buck Output Voltage Change

8.3.7 Enable and Disable Sequences

The LP87702-Q1 device supports programmable start-up and shutdown sequencing. An enable control signal is used to initiate the start-up sequence and to turn off the device according to the programmed shutdown sequence. Up to three enable inputs are available: EN1 is a dedicated enable input; EN2 and EN3 are multiplexed with I2C interface. The buck converter is selected for sequence control with:

- BUCKx_CTRL_1(BUCKx_EN) = 1
- BUCKx_CTRL_1(BUCKx_EN_PIN_CTRL) = 0x1 or 0x2 or 0x3, for EN1 or EN2 or EN3 control, respectively
- BUCKx_VOUT.(BUCKx_VSET[7:0]) = Required voltage when EN pin is high
- The delay from rising edge of EN pin to the converter enable is set by BUCKx_DELAY(BUCKx_STARTUP_DELAY[3:0]) bits and
- The delay from falling edge of EN pin to the converter disable is set by BUCKx_DELAY(BUCKx_SHUTDOWN_DELAY[3:0])

In the same way the boost converter is selected for delayed control with:

- BOOST_CTRL(BOOST_EN) = 1
- BOOST_CTRL(BOOST_EN_PIN_CTRL) = 0x1 or 0x2 or 0x3, for EN1. EN2, or EN3 control (respectively)
- BOOST_CTRL(BOOST_VSET[2:0]) = Required voltage when EN pin is high
- The delay from rising edge of EN pin to the converter enable is set by BOOST_DELAY(BOOST_STARTUP_DELAY[3:0]) bits and
- The delay from falling edge of EN pin to the converter disable is set by BOOST_DELAY(BOOST_SHUTDOWN_DELAY[3:0])

An example of start-up and shutdown sequences for buck converters are shown in 図 8-7. The start-up and shutdown delays for Buck0 converter are 1 ms and 4 ms and for Buck1 converter 3 ms and 1 ms. The delay settings are used only for enable or disable control with the EN signal.

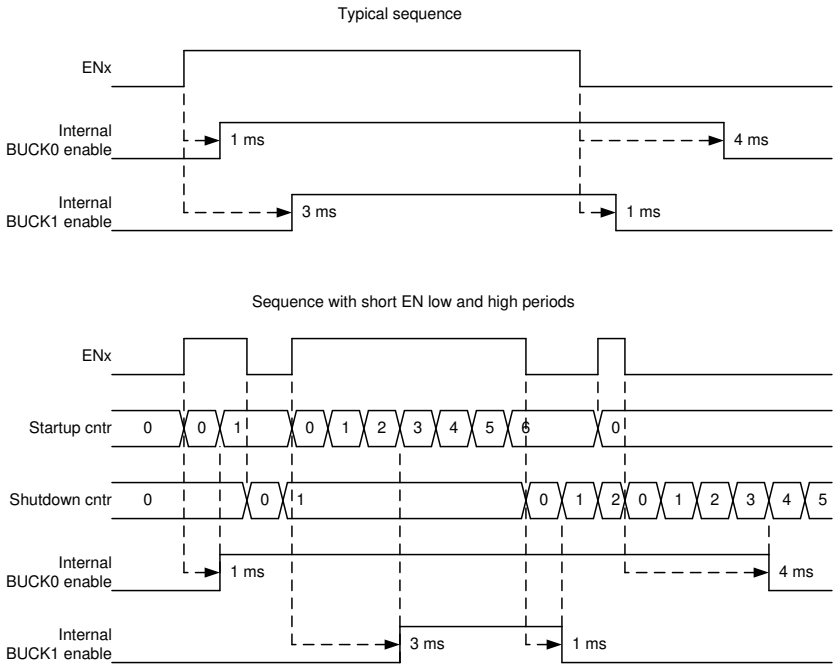


図 8-7. Start-up and Shutdown Sequencing Example

8.3.8 Window Watchdog

図 8-8 shows the LP87702-Q1 watchdog's operation (for an example, when the ENx pin is used for controlling power sequence and ENx pin is active).

WDI is the watchdog function input pin, and WD_RESET is the reset output. The WDI pin needs pulsed within a certain timing window to avoid a watchdog expiration. The minimum pulse width is 100 µs. The watchdog expiration always causes a reset pulse at WD_RESET output, otherwise the device behavior after watchdog expiration is programmable. WD_RESET output polarity and mode, push-pull or open drain, are also programmable.

Watchdog default settings are read from OTP during device start-up. Default settings in WD_CTRL_1 and WD_CTRL_2 register can be over-written through the I2C (as long as WD_LOCK bit is not set to 1). Writing WD_LOCK = 1 in WD_CTRL_2 register locks watchdog settings until NRST input is driven low, power cycle or register reset by SW_RESET.

表 8-4 shows how the long open, close, and open window periods are independently programmable. The watchdog enters the WD Reset state when the long open or open window expires before the WDI input is received. Also, the watchdog enters the WD Reset when the WDI is received during close window. Long open period can be extended by a I2C write to WD_CTRL_1 or WD_CTRL_2 register; the register access initializes the long open counter and the long open period restarts (except in Stop mode).

LP87702-Q1 behavior after WD expiration is programmable:

- When WD_RESET_CNTR_SEL = 00, system restart is disabled and converters are maintained ON. WD_RESET pin is active for 10 ms. Watchdog returns to Long Open mode.
- When WD_RESET_CNTR_SEL = 01 (restart after first reset pulse), LP87702-Q1 performs shutdown sequence followed by start-up sequence so the converters are disabled and re-enabled according to the OTP programmed sequences. The device reloads OTP defaults when WD_EN_OTP_READ = 1 during start-up. Settings valid before shutdown are maintained when the WD_EN_OTP_READ = 0. WD_RESET output pin is active for a period of (10 ms + maximum shutdown delay). Maximum shutdown delay can be selected as 7.5 ms (SHUTDOWN_DELAY_SEL = 0) or 15 ms (SHUTDOWN_DELAY_SEL = 1). After the restart watchdog returns to Long Open mode.
- The status bit (WD_SYSTEM_RESTART_FLAG) is set to indicate that a system restart has happened. The status can be cleared by writing *1* to WD_CLR_SYSTEM_RESTART_FLAG. WD_RESET_CNTR_SEL can

be set to 10 or 11 to select restart after 2 or 4 WD expirations, respectively. The current status of the reset counter is available in WD_RESET_CNTR_STATUS.[1] The reset counter can be cleared by writing WD_CLR_RESET_CNTR to 1.

- Watchdog can also be programmed to perform shutdown sequence and enter STOP mode after the second WD expiration. In STOP mode converters are OFF. WD_RESET output pin is activated for a period of (10 ms + maximum shutdown delay), in STOP mode WD_RESET is inactive. NRST, power cycle, register reset SW_RESET, writing WD_CLR_SYSTEM_RESTART_FLAG = 1 or writing WD_SYSTEM_RESTART_FLAG_MODE = 0 is required to recover. This WD operating mode is selected by setting OTP bit WD_SYS_RESTART_FLAG_MODE = 1.

Watchdog settings in WD_CTRL_1 and WD_CTRL_2 registers are locked by setting the WD_LOCK bit. WD_SYSTEM_RESTART_FLAG and WD_RESET_CNTR_STATUS can be cleared even if WD_LOCK = 1.[1]

Description above is for a case where ENx pin is used for controlling power sequence and ENx pin is active. Watchdog behavior can be slightly different depending on the OTP settings and the ENx pin state, which follows:

- When the ENx pin is used for controlling the power sequence and the ENx pin is not active, the shutdown sequence cannot be performed. WD_RESET pulse length is fixed 31 ms.
- There is no OTP defined power sequence when the ENx pins are not used for power sequence control, and all converters and GPOs are enabled through the I2C. WD expiration does not cause a converter disable or enable sequence even when the OTP settings for the watchdog enable restart. In this case WD_RESET pulse is 11 ms.

[1] WD_RESET_CNTR_STATUS is valid only when WD_RESET_CNTR_SEL is set to either 00 or 03.

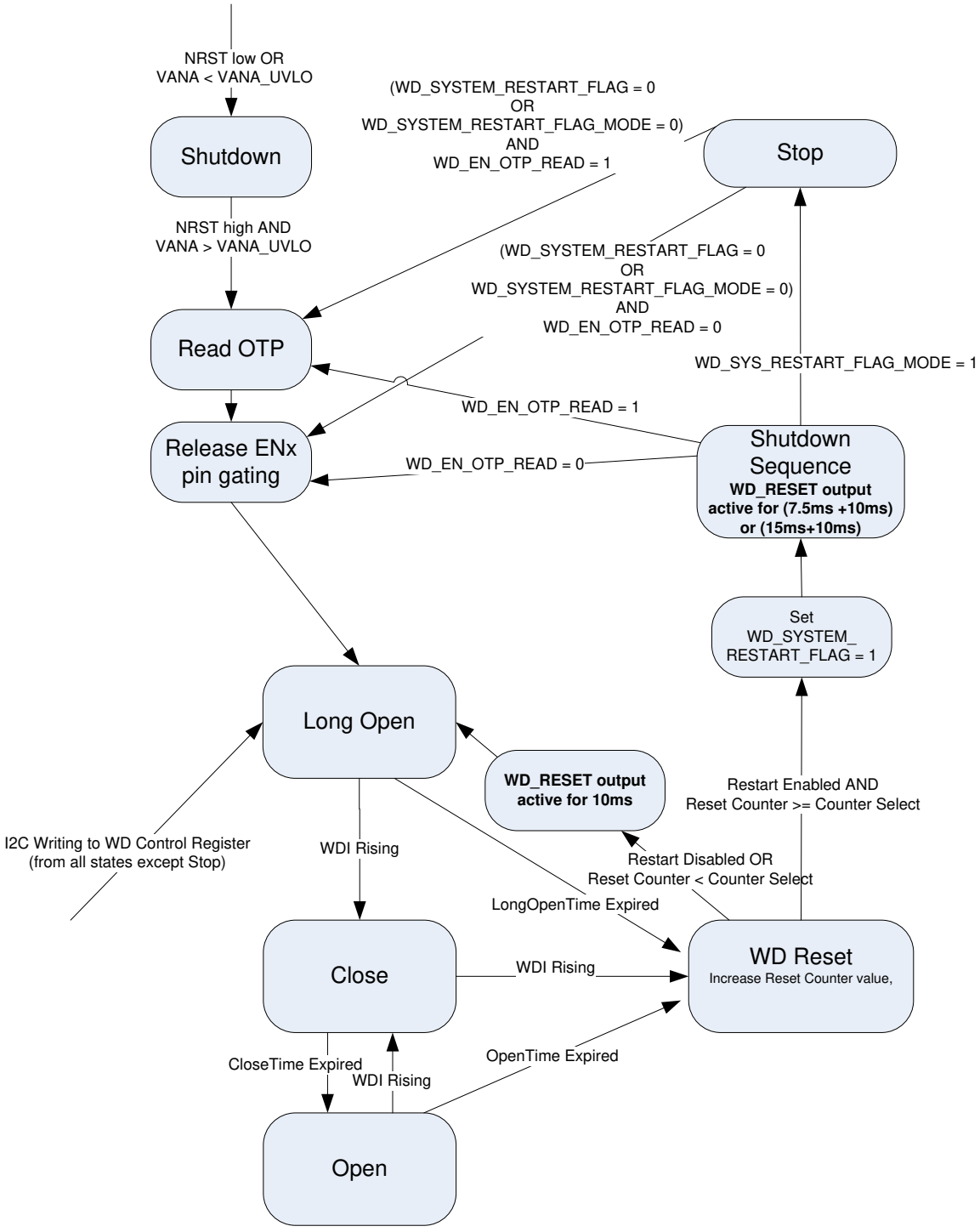


図 8-8. Watchdog Operation

表 8-4. Watchdog Window Periods

CONTROL BIT	DEFAULT	VALUES
WD_LONG_OPEN_TIME	OTP	00 – 200 ms 01 – 600 ms 10 – 2000 ms 11 – 5000 ms
WD_CLOSE_TIME	OTP	00 – 10 ms 01 – 20 ms 10 – 50 ms 11 – 100 ms
WD_OPEN_TIME	OTP	00 – 20 ms 01 – 100 ms 10 – 600 ms 11 – 2000 ms

LP87702-Q1 supports option to disable watchdog. WD_DIS pin function is multiplexed with CLKIN/GPIO2 functions. Watchdog disable option can be selected by setting register bit WD_DIS_CTRL = 1. When WD_DIS_CTRL = 1, WD is disabled if CLKIN/GPIO2/WD_DIS pin is HIGH and enabled if CLKIN/GPIO2/WD_DIS pin is LOW. If WD_DIS_CTRL is toggled to disable and re-enable WD, WD starts from Long Open window after re-enabling.

Default for WD_DIS_CTRL is set in OTP. WD_DIS_CTRL value can be changed via I2C until WD settings are locked. When WD_LOCK is set to 1, WD is enabled regardless of WD_DIS_CTRL value. WD_DIS_CTRL bit is protected by write lock. Three consecutive codes have to be written to WD_DIS_UNLOCK_CODE to open WD_DIS_CTRL for write access.

8.3.9 Device Reset Scenarios

There are four reset methods implemented on the LP87702-Q1:

- Software reset with the SW_RESET bit in the RESET register
- NRST input signal low
- Undervoltage lockout (UVLO) reset from VANA supply
- Watchdog expiration (depending on the watchdog settings)

A SW reset occurs when the SW_RESET bit is set to 1. The bit is automatically cleared after writing. 図 8-14shows how this event disables all the converters immediately, drives GPO signals low, resets all the register bits to the default values and the OTP bits are loaded. I^2C interface is not reset during a software reset. The host must wait at least 1.2 ms after writing SW reset until making a new I2C read or write to the device.

If VANA supply voltage falls below the UVLO threshold level or the NRST signal is set low, then all the converters are disabled immediately, the GPOx signals are driven low, and all the register bits are reset to the default values. When the VANA supply voltage rises above the UVLO threshold level and the NRST signal rises above the threshold level, the OTP bits are loaded to the registers and a start-up is initiated according to the register settings. The host must wait at least 1.2 ms before reading or writing to the I2C interface.

Depending on the watchdog settings, the watchdog expiration can reset the device to the OTP default values.

8.3.10 Diagnostics and Protection Features

The LP87702-Q1 provides four levels of protection features:

- Input and output voltage information. Non-valid voltage sets interrupt or PGx signal:
  - Validity of the output voltage of BUCK or BOOST converters
  - Validity of VANA, VMON1, and VMON2 input voltages
- Warnings causing interrupt:
  - Peak current limit detection in BUCK or BOOST converters
  - Thermal warning
- Protection events which are disabling the converters:
  - Short-circuit and overload protection for BUCK and BOOST converters
  - Input overvoltage protection ($VANA_{OVP}$)

  - Watchdog expiration (optional, depends on the watchdog settings)
  - Thermal shutdown
- Protection events which are causing the device to shutdown:
  - Undervoltage lockout ($VANA_{UVLO}$)
- Protections not causing interrupt or converter disable:
  - Negative current limit detection in the BUCK or BOOST converters

8.3.10.1 Voltage Monitorings

The LP87702-Q1 device has programmable voltage monitoring for the BUCKx and BOOST converter output voltages and for VANA, VMON1, and VMON2 inputs. Monitoring of each signal is independently enabled in the PGOOD_CTRL register. Voltage monitoring can be under-voltage monitoring only (PGOOD_WINDOW = 0) or overvoltage and undervoltage monitoring (PGOOD_WINDOW = 1). This selection is common for all enabled monitorings. *セクション 8.3.10.3*describes how the enabled monitoring signals are combined to generate power-good (PG0 and PG1) and interrupts. Monitoring comparators have a dedicated reference and bias block, which is independent of the main reference and bias block.

Nominal level for the output voltage of BUCKx converter is set with BUCKx_VSET in the BUCKx_VOUT register. Overvoltage and undervoltage detection levels, with respect to nominal level, are selected with BUCKx_WINDOW as ± 30 mV, ± 50 mV, ± 70 mV or ± 90 mV. Nominal level for the output voltage of the BOOST converter is set with BOOST_VSET in the BOOST_CTRL register. Available levels are 4.9 V, 5 V, 5.1 V, and 5.2 V. Overvoltage and undervoltage detection levels, with respect to nominal level, are selected with BOOST_WINDOW as ± 2%, ± 4%, ± 6% or ± 8%. Converter monitoring window selection bits are in the PGOOD_LEVEL_3 register.

Input voltage of LP87702-Q1 is monitored at the VANA pin. Nominal level can be selected as 3.3 V or 5 V with the VANA_THRESHOLD bit. Overvoltage and undervoltage detection levels are selected with VANA_WINDOW as ± 5% or ± 10% (nominal). VANA_THRESHOLD and VANA_WINDOW are set in the PGOOD_LEVEL_2 register.

VMON1 and VMON2 inputs can be used for monitoring external rails in the system. VMONx settings are defined in the PGOOD_LEVEL_1 and PGOOD_LEVEL_2 registers. Nominal value for the input level of VMONx is selected with VMONx_THRESHOLD, between 0.65 V to 1.8 V. Higher voltage levels or levels not directly supported can be monitored using an external resistor divider. In this case VMONx_THRESHOLD must be set as 0.65 V to have a high-impedance input, and the resistor divider must scale the monitored level down to 0.65 V at the VMONx pin. Overvoltage and undervoltage detection levels are selected with VMONx_WINDOW as ± 2%, ± 3%, ± 4% or ± 6%.

See *セクション 7* for more details on the accuracy of the monitoring windows and deglitch filtering.

8.3.10.2 Interrupts

The LP87702-Q1 sets the flag bits indicating what protection or warning conditions have occurred, and the nINT pin is pulled low. The nINT output pin is driven high after all the flag bits and pending interrupts are cleared.

Fault detection is indicated by the RESET_REG_INT interrupt flag bit set in the INT_TOP_2 register after the start-up event.

表 8-5. Summary of Interrupt Signals

EVENT	SAFE STATE	INTERRUPT BIT	INTERRUPT MASK	STATUS BIT	RECOVERY/INTERRUPT CLEAR
Buck current limit triggered (20-µs debounce)	No effect	BUCK_INT = 1 BUCKx_ILIM_INT = 1	BUCKx_ILIM_MASK	BUCKx_ILIM_STAT	Write 1 to the BUCKx_ILIM_INT bit Interrupt is not cleared if the current limit is active.
Boost current limit triggered	No effect	BOOST_INT = 1 BOOST_ILIM_INT = 1	BOOST_ILIM_MASK	BOOST_ILIM_STAT	Write 1 to the BOOST_ILIM_INT bit. Interrupt is not cleared if the current limit is active.
Buck short circuit (V_{VOUT} < 0.35V at 1 ms after enable) or Overload (V_{VOUT} decreasing below 0.35 V during operation, 1 ms debounce)	Converter disable	BUCKx_INT = 1 BUCKx_SC_INT = 1	N/A	N/A	Write 1 to the BUCKx_SC_INT bit.
Boost short circuit	Converter disable	BOOST_INT = 1 BOOST_SC_INT = 1	N/A	N/A	Write 1 to the BOOST_SC_INT bit.
Thermal warning	No effect	TDIE_WARN_INT) = 1	TDIE_WARN_MASK	TDIE_WARN_STAT	Write 1 to the TDIE_WARN_INT bit. Interrupt is not cleared if the temperature is above the thermal warning level.
Thermal shutdown	All converters disabled immediately and GPOx set to low	TDIE_SD_INT = 1	N/A	TDIE_SD_STAT	Write 1 to TDIE_SD_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
VANA overvoltage ($VANA_{OVP}$)	All converters disabled immediately and GPOx set to low	OVP_INT	N/A	OVP_STAT	Write 1 to the OVP_INT bit. Interrupt is not cleared if the VANA voltage is above the $VANA_{OVP}$ level.
Buck power-good, output voltage becomes valid.	No effect	BUCK_INT = 1 BUCKx_PG_INT = 1	BUCKx_PGR_MASK	BUCKx_PG_STAT	Write 1 to the BUCKx_PG_INT bit.
Buck power-good, output voltage becomes invalid	No effect	BUCK_INT = 1 BUCKx_PG_INT = 1	BUCKx_PGF_MASK	BUCKx_PG_STAT	Write 1 to the BUCKx_PG_INT bit.
Boost power-good, output voltage becomes valid.	No effect	BOOST_INT = 1 BOOST_PG_INT = 1	BOOST_PGR_MASK	BOOST_PG_STAT	Write 1 to the BOOST_PG_INT bit.
Boost power-good, output voltage becomes invalid.	No effect	BOOST_INT = 1 BOOST_PG_INT = 1	BOOST_PGF_MASK	BOOST_PG_STAT	Write 1 to the BOOST_PG_INT bit.
VMON1 power-good, input voltage becomes valid.	No effect	DIAG_INT = 1 VMON1_PG_INT = 1	VMON1_PGR_MASK	VMON1_PG_STAT	Write 1 to the VMON1_PG_INT bit.
VMON1 power-good, input voltage becomes invalid.	No effect	DIAG_INT = 1 VMON1_PG_INT = 1	VMON1_PGF_MASK	VMON1_PG_STAT	Write 1 to the VMON1_PG_INT bit.
VMON2 power-good, input voltage becomes valid.	No effect	DIAG_INT = 1 VMON2_PG_INT = 1	VMON2_PGR_MASK	VMON2_PG_STAT	Write 1 to the VMON2_PG_INT bit.
VMON2 power-good, input voltage becomes invalid.	No effect	DIAG_INT = 1 VMON2_PG_INT = 1	VMON2_PGF_MASK	VMON2_PG_STAT	Write 1 to the VMON2_PG_INT bit.
VANA power-good, input voltage becomes valid.	No effect	DIAG_INT = 1 VANA_PG_INT = 1	VANA_PGR_MASK	VANA_PG_STAT	Write 1 to the VANA_PG_INT bit.
VANA power-good, input voltage becomes invalid.	No effect	DIAG_INT = 1 VANA_PG_INT = 1	VANA_PGF_MASK	VANA_PG_STAT	Write 1 to the VANA_PG_INT bit.
External clock appears or disappears.	No effect to converters	SYNC_CLK_INT(1)	SYNC_CLK_MASK	SYNC_CLK_STAT	Write 1 to the SYNC_CLK_INT bit.
Load current measurement ready	No effect	I_MEAS_INT = 1	I_MEAS_MASK	N/A	Write 1 to the I_MEAS_INT bit.
Supply voltage $VANA_{UVLO}$ triggered (VANA falling)	Immediate shutdown, registers reset to default values	N/A	N/A	N/A	N/A
Supply voltage $VANA_{UVLO}$ triggered (VANA rising)	Start-up, registers reset to default values and OTP bits loaded	RESET_REG_INT = 1	RESET_REG_MASK	N/A	Write 1 to the RESET_REG_INT bit.

表 8-5. Summary of Interrupt Signals (continued)

EVENT	SAFE STATE	INTERRUPT BIT	INTERRUPT MASK	STATUS BIT	RECOVERY/INTERRUPT CLEAR
Software requested reset	Immediate shutdown followed by powerup, registers reset to default values	RESET_REG_INT = 1	RESET_REG_MASK	N/A	Write 1 to the RESET_REG_INT bit.

(1) Interrupt generated during the Clock Detector operation and in case the Clock is not available when the Clock Detector is enabled.

8.3.10.3 Power-Good Information to Interrupt, PG0, and PG1 Pins

LP87702-Q1 supports both interrupt based indication of the power-good levels for various voltage settings and uses two power-good signals, PG0 and PG1. The selection of monitored signals is independent for the interrupt (nINT) and PG0 and PG1 signals. Each signal can include the following:

- The output voltage of one or both BUCKx converters
- The output voltage of the BOOST converter
- Input voltage of VANA
- Input voltage of VMON1 and VMON2 or both
- Thermal warning

図 8-9 shows the block diagram for power-good connections to PG0 and PG1 pins and interrupt.

Monitored signals are enabled in the PGOOD_CTRL register. Converter output voltage monitoring (not current limit monitoring) can be selected for the indication. Monitoring is enabled by the EN_PGOOD_BUCKx and EN_PGOOD_BOOST bits. The monitoring is automatically masked to prevent it from forcing PGx inactive or causing an interrupt when a converter is disabled. Also, monitoring of VANA, VMON1, and VMON2 inputs can be independently enabled through the PGOOD_CTRL register. The type of voltage monitoring for the PGx signals and nINT is selected by the PGOOD_WINDOW bit. Only the undervoltage is monitored if the bit is 0 and the undervoltage and overvoltage are monitored if the bit is 1. See *セクション 8.3.10.1* for voltage monitoring thresholds.

Monitoring interrupts from all the output rails, input rails, and thermal warning are combined to the nINT pin. Dedicated mask bits are used to select which interrupts control the state of the nINT pin. See 表 8-5 for summary of the interrupts, mask bits, and interrupt clearing.

Similarly, enabled monitoring signals from all the output rails, input rails, and thermal warning are combined to PG0 and PG1 output pins. Register bits (SEL_PGx_x in PG0_CTRL and PG1_CTRL) select which of the signals control the state of PG0 and PG1, respectively. The polarity and the output type (push-pull or open-drain) of PG0 and PG1 are selected by the PGx_POL and PGx_OD bits in the PG_CTRL register.

PGx is only *active* or *asserted* when all monitored input voltages and all output voltages of the monitored and enabled converters are within the specified tolerance of the set target value.

PGx is *inactive* or *de-asserted* if any of the monitored input voltages or output voltages of the monitored and enabled converters are outside the specified tolerance of the set target value.

When PGx_RISE_DELAY = 1, PGx is set as *active* or *asserted* with 11 ms delay from the point of time where all the enabled power resource output voltages are within the specified tolerance for each requested or programmed output voltage.

Thermal shutdown and VANA overvoltage protection events force the PGx to the default state (the PGx are driven low, assuming the PGx polarity set in the OTP is active high).

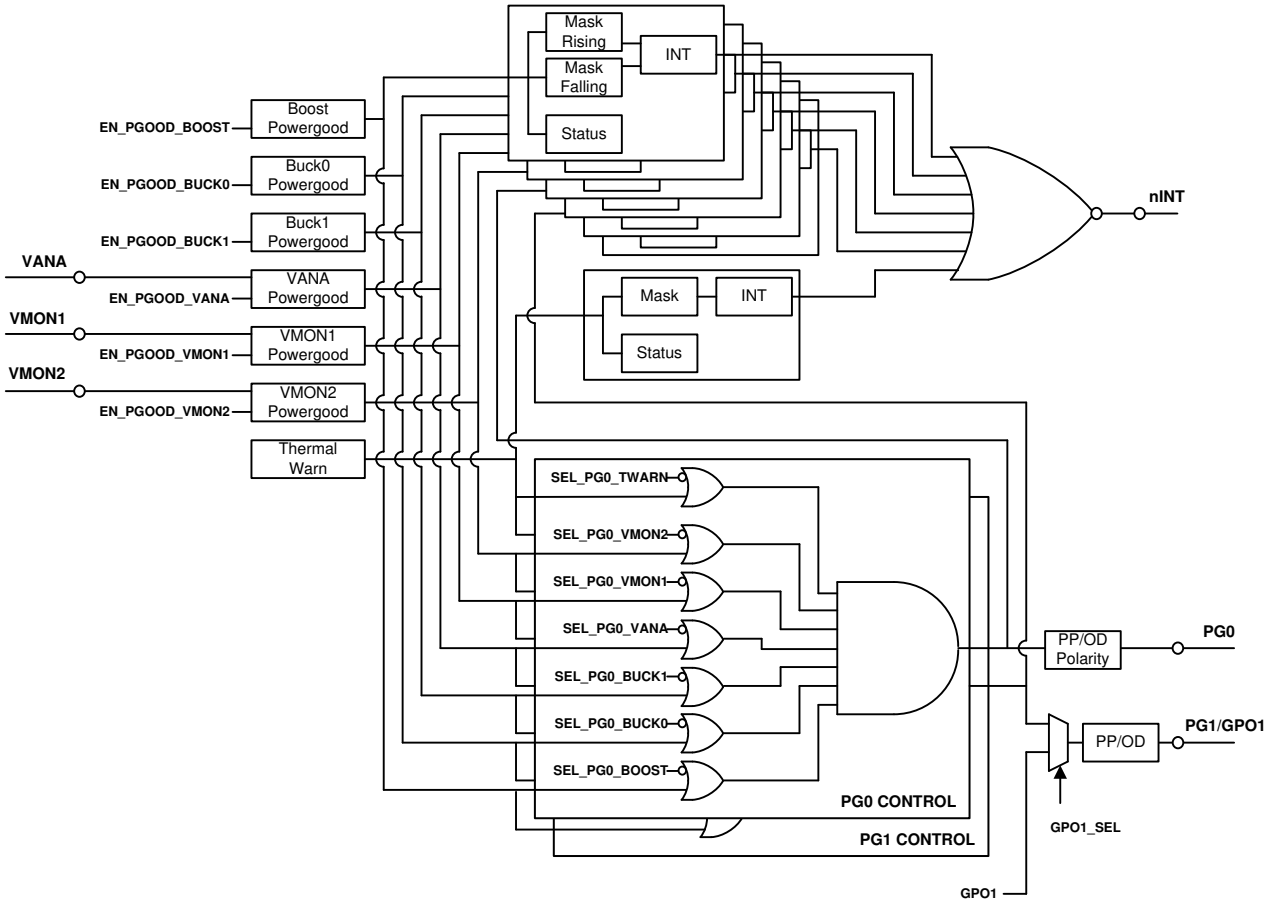


図 8-9. Block Diagram of Power-Good Connections

LP87702-Q1 power-good detection has two operating modes selected in the OTP: gated (that is, *unusual*) or continuous (that is, *invalid*) mode of operation. These modes are described in *セクション 8.3.10.3.1* and in *セクション 8.3.10.3.2*.

8.3.10.3.1 PGx Pin Gated (Unusual) Mode

The PGx signal detects unexpected or unusual situations in this mode. Mode is selected by setting the PGx_MODE bit to 0 in the PG_CTRL register.

For the gated mode of operation, the PGx behaves as follows:

- PGx is set to active or asserted state upon exiting the OTP configuration as an initial default state.
- The PGx status is *active* or *asserted* during an 800-µs gated time period from the enable activation for each enabled rail, thereby *gating-off* the status indication.
- The PGx state typically remains *active* or *asserted* for normal conditions during normal power-up sequencing and requested voltage changes.
- The PGx status could change to *inactive* or *de-asserted* after an 800-µs gated time period if any output voltage is outside of regulation range during an abnormal power-up sequencing and requested voltage changes.
- Using the gated mode of operation could allow the PGx signal to initiate an immediate power shutdown sequence if the PGx signal is wired-OR with signal connected to the EN input. This type of circuit configuration provides a smart PORz function for processor that eliminates the need for additional components to generate PORz upon start-up and to monitor voltage levels of key voltage domains.

PGx signal is set inactive if the output voltage of a monitored buck or boost converter is invalid or the output voltage is not valid at 800 µs from the enable of the converter, which should be considered when selecting the BUCKx_SLEW_RATE setting. Keep the sum of the soft start time and slew rate controlled part of the voltage

ramp below 800 µs to avoid PGx triggering at start-up. In addition, the PGx is inactive when the invalid input voltage at VANA, VMON1, or VMON2 pin is detected.

Detected fault sets the corresponding fault bit in PG0_FAULT or in PG1_FAULT register. The detected fault must be cleared to continue the PGx monitoring. The over-voltage and thermal faults are cleared by writing 1 to the corresponding interrupt bits in INT_TOP_1 register. Converter, VMONx and VANA faults are cleared by writing 1 to the corresponding register bit in INT_BUCK, INT_BOOST, and INT_DIAG register, respectively. An example of the PGx pin operation in gated mode is shown in 図 8-10 and the different use cases for the PGx signal operation are summarized in 表 8-6.

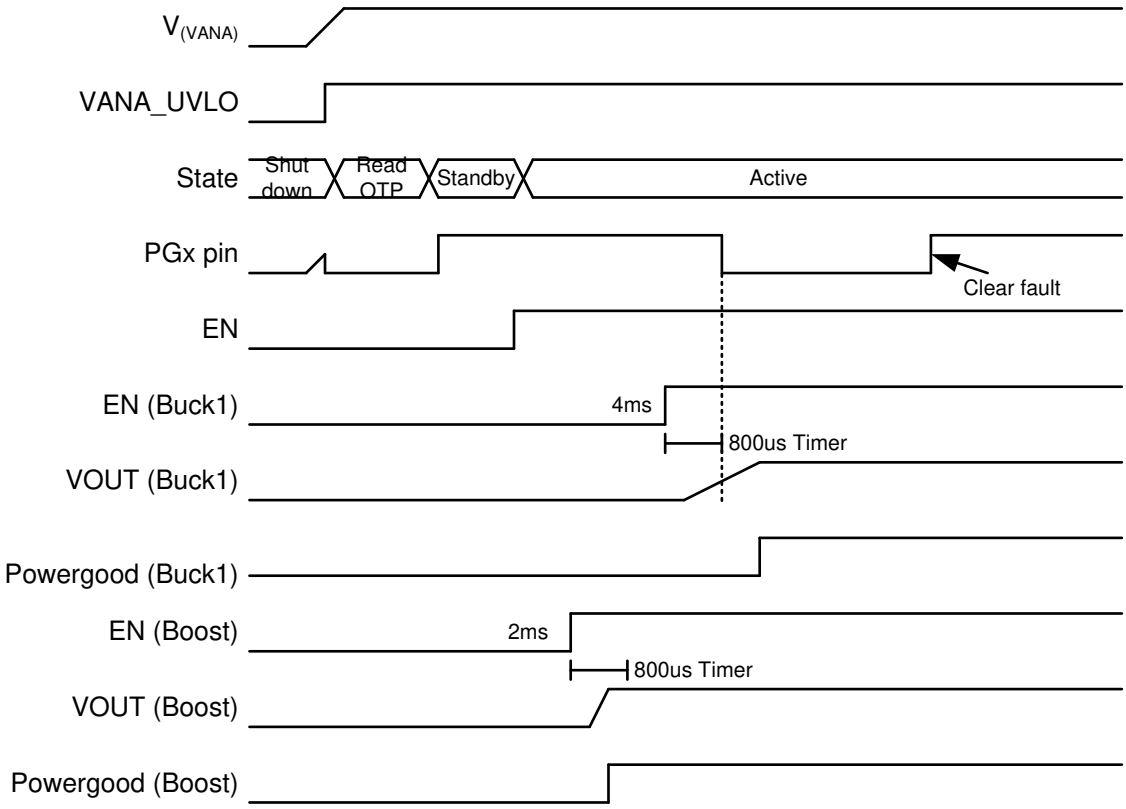


図 8-10. PGx Pin Operation in Gated Mode.

8.3.10.3.2 PGx Pin Operation in Continuous Mode

In this mode the PGx signal shows the validity of the requested voltages continuously. Mode is selected by setting the PGx_MODE bit to 1 in the PG_CTRL register.

For the continuous mode of operation, the PGx behaves as follows:

- PGx is set to *active* or *asserted* state upon exiting the OTP configuration as an initial default state.
- PGx is set to *inactive* or *de-asserted* as soon as the converter is enabled.
- PGx status begins indicating the output voltage regulation status immediately and continuously.
- PGx state changes between *inactive* or *deasserted* and active or asserted during power-up sequencing and requested voltage changes, depending on the output voltages being outside or inside of the regualtion ranges.

When an invalid output voltage of monitored converter is detected, the corresponding bit in the PG0_FAULT or PG1_FAULT register is set to 1 and the PGx signal becomes inactive. The PG0_FAULT and PG1_FAULT register bits are latched and maintain the fault information until host clears the fault bit by writing 1 to the bit. The PGx signal also indicates the interrupts from VANA, VMON1, and VMON2 inputs and thermal warning and shutdown. All are cleared by clearing the interrupt bits.

The PGx signal is set inactive when the converter voltage is transitioning from one target voltage to another.

The source for the fault can be read from PGx_FAULT register when PGx signal becomes inactive. If the invalid output voltage becomes valid again the PGx signal becomes active. Thus the PGx signal shows all the time if the monitored output voltages are valid. 図 8-11 shows an example of the PGx pin operation in continuous mode.

The PGx signal can also be configured so that it maintains the inactive state even when the monitored outputs are valid, but there are PG_FAULT_x bits pending clearance. This type of operation is selected by setting the PGOOD_FAULT_GATES_PGx bit to 1.

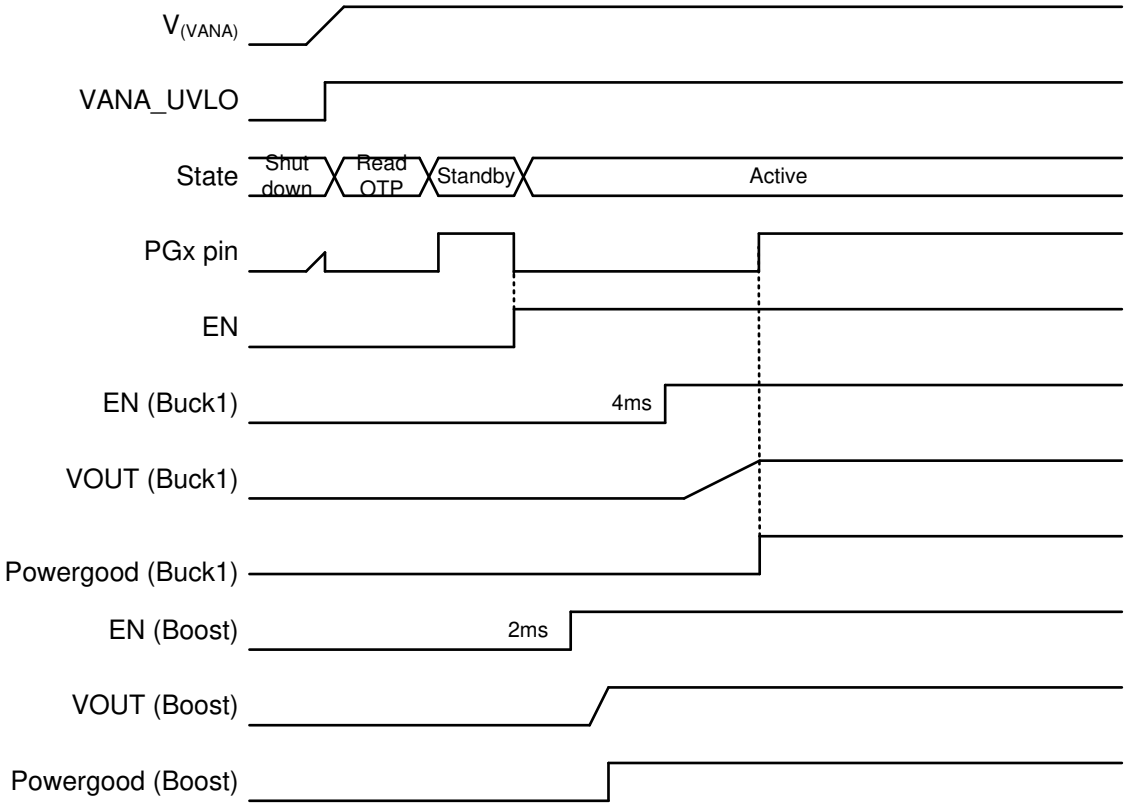


図 8-11. PGx Pin Operation in Continuous Mode

8.3.10.3.3 Summary of PG0, PG1 Gated, and Continuous Operating Modes

表 8-6 summarizes the PGx behavior in different application scenarios, for the gated and continuous operating modes.

表 8-6. PGx Operation

STATUS / USE CASE	CONDITION	PGx SIGNAL(1) (2)	
		GATED MODE PGx_MODE = 0	CONTINUOUS MODE PGx_MODE = 1
Device start-up	Until device state is STANDBY	Low	Low
Converter not selected for PGx monitoring	EN_PGOOD_x = 0	OK	OK
Converter selected for PGx monitoring and disabled by host	BUCKx_EN / BOOST_EN = 0 OR (Pin ctrl AND EN = 0)	OK	OK
Converter start-up delay ongoing	EN = 1	OK	NOK
Converter start-up until valid output voltage reached	Valid output voltage reached in 800 µs	OK	NOK
Converter start-up until valid output voltage reached	Valid output voltage not reached at 800 µs	NOK	NOK
Output voltage within window limits after start-up	Must be inside limits longer than debounce time	OK	OK
Output voltage spikes (over/ undervoltage)	If spikes are outside voltage monitoring threshold(s) longer than debounce time	NOK	NOK
Voltage setting change, output voltage ramp		OK (if new voltage reached in 800 µs) NOK after 800 µs (if new voltage not reached at 800 µs)	NOK
Output voltage within window limits after voltage change	Must be inside limits longer than debounce time	OK	OK
Converter shutdown delay ongoing		OK	OK
Buck converter disabled by host, slew-rate controlled ramp down ongoing		OK	OK
Converter disabled by host, pulldown resistor active (if selected)		OK	OK
Converter short-circuit interrupt pending (converter selected for PGx monitoring)	Faulty converter disabled by short-circuit detection BUCKx_SC_INT / BOOST_SC_INT = 1	NOK	NOK
Thermal shutdown interrupt pending	Converters disabled by thermal shutdown detection TDIE_SD_INT = 1	NOK	NOK
Input (VANA) overvoltage interrupt pending	Converters disabled by overvoltage detection OVP_INT = 1	NOK	NOK
Supply voltage below $VANA_{UVLO}$		Low	Low

(1) NOK (Not OK) means faulty situation. PGx pin is inactive if at least one NOK situation is detected.
(2) PGx pin is generated from PG_FAULT register bits and INT_TOP_1 register bits TDIE_SD_INT, OVP_INT and INT_TOP_2(RESET_REG_INT) bit.

8.3.10.4 Warning Interrupts for System Level Diagnostics

8.3.10.4.1 Output Power Limit

The buck converters have programmable output peak current limits. The limits are individually programmed for both converters with BUCKx_ILIM[2:0] bits. If the load current is increased so that the current limit is triggered, the converter continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 20 µs, the LP87702-Q1 device sets the BUCKx_ILIM_INT bit and pulls the nINT pin low. The host processor can read the

BUCKx_ILIM_STAT bits to see if the converter is still in peak current regulation mode. During startup or output voltage ramp (output voltage change has been programmed) no interrupt is generated.

If the load is so high that the output voltage decreases below a 350-mV level, the LP87702-Q1 device disables the converter and sets the BUCKx_SC_INT bit. The interrupt is cleared when the host processor writes 1 to BUCKx_SC_INT bit. 図 8-12 shows the Buck overload situation.

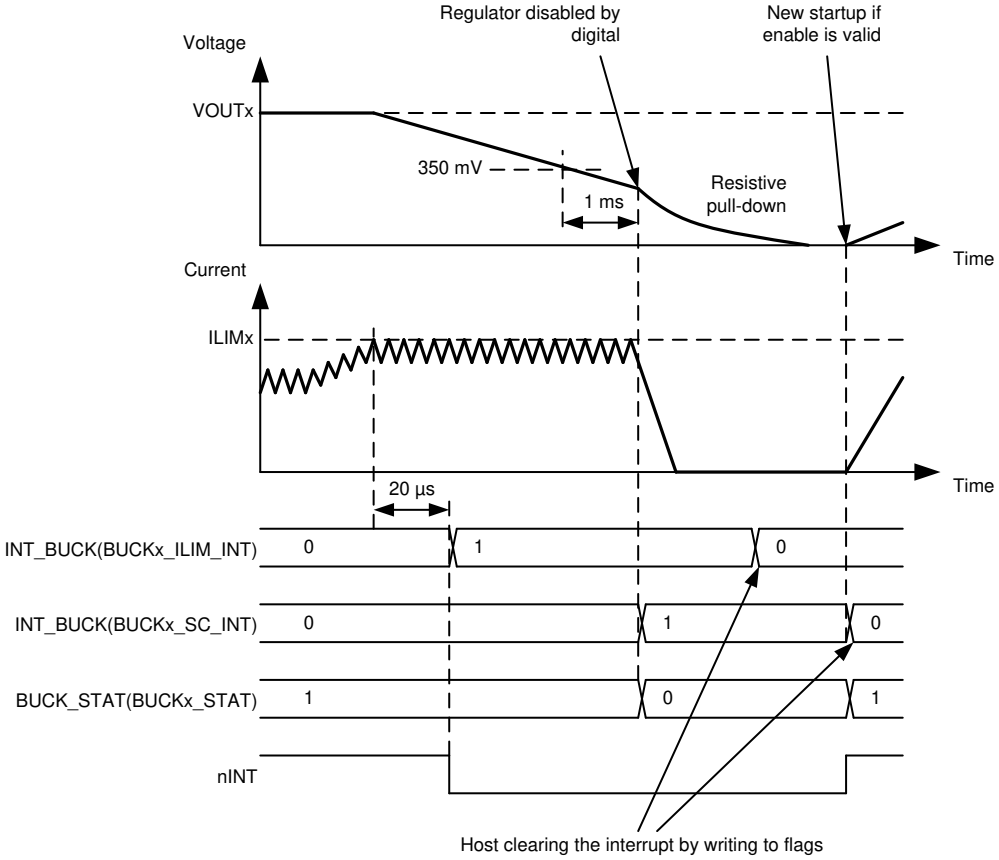


図 8-12. Buck Overload Situation

The boost converter has programmable output peak current limits. The limits are set with the BOOST_ILIM bits. If the load current is increased so that the current limit is triggered, the converter continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 64 µs, the LP87702-Q1 device sets the BOOST_ILIM_INT bit and pulls the nINT pin low. The host processor can read the BOOST_ILIM_STAT bits to see if the converter is still in peak current regulation mode.

If the load is so high that the output voltage decreases 150 mV (typical) below the input voltage level, then the converter is disabled after 1 ms. If the output voltage decreases to 2.5 V, boost stops switching. After 1 ms the deglitch time boost is fully disabled and the interrupt BOOST_SC_INT bit is set. The interrupt is cleared when the host processor writes 1 to the BOOST_SC_INT bit. 図 8-13 shows the Boost overload situation.

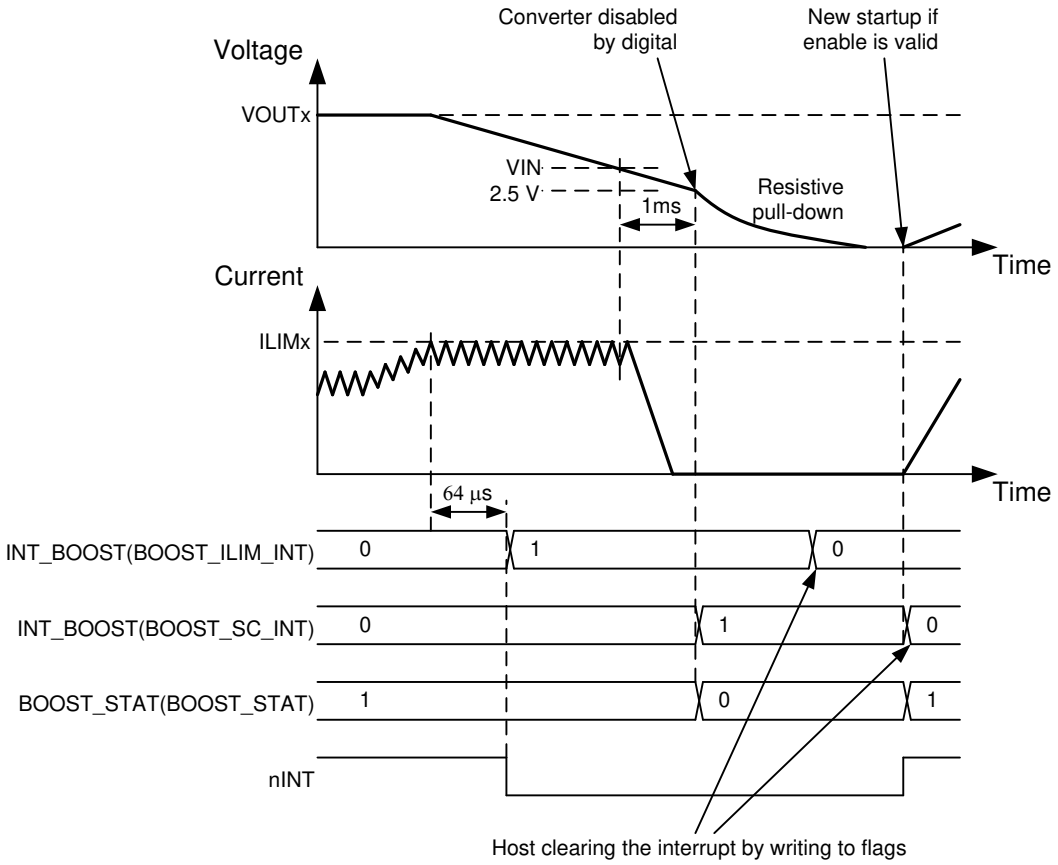


図 8-13. Boost Overload Situation

The buck converters have a fixed current limit for negative output peak current (I_{LIM_NEG}). When the negative coil current increases, it is limited below I_{LIM_NEG}, the converter continues to operate and no interrupt is generated. The boost converter's negative peak current limit operation is similar and the limit value is 1.4 A (typical).

8.3.10.4.2 Thermal Warning

The LP87702-Q1 device includes a protection feature against over-temperature by setting an interrupt for the host processor. The thermal warning's threshold level is selected with the TDIE_WARN_LEVEL bit.

If the LP87702-Q1 device temperature increases above the thermal warning level, the device sets the TDIE_WARN_INT bit and pulls the nINT pin low. The status of the thermal warning can be read from the TDIE_WARN_STAT bit and the interrupt is cleared by writing 1 to the TDIE_WARN_INT bit. The thermal warning interrupt can be masked by setting the TDIE_WARN_MASK bit to 1.

8.3.10.5 Protections Causing Converter Disable

If the converter is disabled because of protection or fault (short-circuit protection, thermal shutdown, overvoltage protection, or undervoltage lockout), the output power FETs are set to high-impedance mode, and the output pulldown resistor is enabled (if enabled with BUCKx_RDIS_EN and BOOST_RDIS_EN bits). The turnoff time of the output voltage is defined by the output capacitance, load current, and the resistance of the integrated pulldown resistor. The pulldown resistors are active as long as the VANA voltage is above the 1.2-V level (approximately).

8.3.10.5.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the LP87702-Q1 to protect itself and external components against short circuiting at the output or against overloading during start-up. A short-circuit at the buck converter output is detected during start-up when the output voltage is below 350 mV (typical) 1 ms after the buck converter is

enabled. The fault threshold is 150 mV (typical) below the input voltage level for boost. Boost converter is disabled if the output voltage is below the threshold level 1 ms after the boost converter is enabled.

In a similar way, the overload situation is protected during normal operation. If the feedback-pin voltage of the buck converter falls below 0.35 V and remains below the threshold level for 1 ms, the buck converter is disabled. If the output voltage of the boost converter decreases 150 mV below the input voltage level, the converter is disabled after 1 ms. If the output voltage decreases to 2.5 V, the boost is disabled immediately.

The BUCKx_SC_INT and the BUCK_INT bits are set to 1, the BUCKx_STAT bit is set to 0, and the nINT signal is pulled low in the buck converter, the short-circuit, and overload situations. The BOOST_SC_INT and the BOOST_INT bits are set to 1, the BOOST_STAT bit is set to 0, and the nINT signal is pulled low in the boost converter, short-circuit, and overload situations. The host processor clears the interrupt by writing 1 to the BUCKx_SC_INT or BOOST_SC_INT bit. The converter makes a new start-up attempt upon clearing the interrupt, if the converter is in the enabled state.

8.3.10.5.2 Overvoltage Protection

The LP87702-Q1 device monitors the input voltage from the VANA pin in the standby and active operation modes. If the input voltage rises above the $VANA_{OVP}$ voltage level, all the converters are disabled immediately (without switching ramp or shutdown delays), the pulldown resistors discharge the output voltages (BUCKx_RDIS_EN = 1 and BOOST_RDIS_EN = 1), the GPOs are set to the logic low level, the nINT signal is pulled low, the OVP_INT bit is set to 1, and BUCKx_STAT and BOOST_STAT bits are set to 0. The host processor clears the interrupt by writing 1 to the OVP_INT bit. If the input voltage is above over-voltage detection level, the interrupt is not cleared. The host can read the status of the overvoltage from the OVP_STAT bit. Converters cannot be enabled as long as the input voltage is above over-voltage detection level or the overvoltage interrupt is pending.

8.3.10.5.3 Thermal Shutdown

The LP87702-Q1 has an overtemperature protection function that operates to protect itself from short-term misuse and overload conditions. The converters are disabled immediately (without switching ramp or shutdown delays), the TDIE_SD_INT bit is set to 1, the nINT signal is pulled low, and the device enters STANDBY when the junction temperature exceeds around 150°C. The nINT is cleared by writing 1 to the TDIE_SD_INT bit. If the temperature is above thermal shutdown level, the interrupt is not cleared. The host can read the status of the thermal shutdown from the TDIE_SD_STAT bit. Converters cannot be enabled as long as the junction temperature is above the thermal shutdown level or the thermal shutdown interrupt is pending.

8.3.10.6 Protections Causing Device Power Down

8.3.10.6.1 Undervoltage Lockout

The buck and boost converters are disabled immediately (without switching ramp or without any shutdown delays), and the output capacitor is discharged using the pulldown resistor, and the LP87702-Q1 device enters SHUTDOWN when the input voltage falls below $VANA_{UVLO}$ at the VANA pin. The device powers up to STANDBY state when the $V_{(VANA)}$ voltage is above the $VANA_{UVLO}$ threshold level.

If the reset interrupt is unmasked by default (RESET_REG_MASK = 0 in TOP_MASK_2 register), the RESET_REG_INT interrupt in the INT_TOP_2 register indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the RESET_REG_INT bit. If the host processor reads the RESET_REG_INT flag after detecting an nINT low signal, it detects that the input supply voltage has been below the $VANA_{UVLO}$ level (or the host has requested reset with the RESET(SW_RESET) bit), and the registers are reset to the default values.

8.3.11 OTP Error Correction

LP87702-Q1 supports the OTP bit error detection and 1-bit error correction per five registers. The ECC_STATUS register bit SED is set if a single bit error was detected and corrected. DED bit is set in case two bit errors have been detected in any bank of five registers.

8.3.12 Operation of GPO Signals

The LP87702-Q1 device supports up to 3 general purpose output (GPO) signals. The GPO1 signal is multiplexed with the PG1 signal and GPO2 signal is multiplexed with the CLKIN and WD_DIS signals. The

selection between signal use are set with the GPO1_SEL and GPO2_SEL bits in the GPO_CONTROL_2 register.

The type of output, either push-pull (with $V_{(VANA)}$ level) or open drain, are set with the GPO0_OD and GPO1_PG1_OD bits in the GPO_CONTROL_1 register and the GPO2_OD bit in the GPO_CONTROL_2 register.

The logic level of the GPOx pins are is set by the GPO0_OUT and GPO1_OUT bits in the GPO_CONTROL_1 register and the GPO2_OUT bit in the GPO_CONTROL_2 register.

The control of the GPOs can be included to start-up and shutdown sequences. The GPO control for a sequence with ENx pin is selected by the GPOx_EN_PIN_CTRL bits. The delays during start-up and shutdown are set by bits in the GPOx_DELAY registers.

8.3.13 Digital Signal Filtering

The digital signals have a debounce filtering. The signal or supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

表 8-7. Digital Signal Filtering

EVENT	SIGNAL/SUPPLY	RISING EDGE	FALLING EDGE
		LENGTH	LENGTH
Enable or Disable for BUCKx, BOOST, or GPOx	ENx	3 µs(1)	3 µs(1)
VANA undervoltage lockout	VANA	Immediate (VANA voltage rising)	Immediate (VANA voltage falling)
VANA overvoltage	VANA	1 µs (VANA voltage rising)	1 µs (VANA voltage falling)
Thermal warning	TDIE_WARN_INT	20 µs	20 µs
Thermal shutdown	TDIE_SD_INT	20 µs	20 µs
Current limit, BUCKx		20 µs	20 µs
Current limit, BOOST		64 µs	64 µs
Overload	FB_B0, FB_B1, VOUT_BST	1 ms	N/V
PGx pin and power-good interrupt (voltage monitoring)	PG0, PG1 / FB_B0, FB_B1	6 µs	6 µs
PGx pin and power-good interrupt (voltage monitoring)	PG0, PG1 / VOUT_BST, VANA, VMON1, VMON2	15 µs	15 µs

(1) No glitch filtering; only synchronization.

8.4 Device Functional Modes

8.4.1 Modes of Operation

SHUTDOWN: The $V_{(VANA)}$ voltage is below the $VANA_{UVLO}$ threshold level or the NRST signal is low. All switch, reference, control, and bias circuitry of the LP87702-Q1 device are turned off.

READ OTP: The main supply voltage ($V_{(VANA)}$) is above the $VANA_{UVLO}$ level and the NRST signal is high. The converters are disabled and the reference and bias circuitry of the LP87702-Q1 are enabled. The OTP bits are loaded to the registers. I2C access is not allowed during OTP read. *セクション 8.3.8* shows how this also applies to the watchdog.

STANDBY: The main supply voltage ($V_{(VANA)}$) is above the $VANA_{UVLO}$ level and the NRST signal is high. All registers can be read or written by the host processor through the system serial interface. Watchdog is active and the WDI input is expected to toggle to avoid watchdog expiration. The converters are disabled and the LP87702-Q1's reference, control, and bias circuitry are enabled. The converters can be enabled if needed.

ACTIVE: The main supply voltage ($V_{(VANA)}$) is above the $VANA_{UVLO}$ level and the NRST signal is high. At least one converter is enabled. All registers can be read or written by the host processor through

the system's serial interface. Watchdog is active and the WDI input is expected to toggle to avoid watchdog expiration.

図 8-14 shows the operating modes and transitions between the modes. See *セクション 8.3.8* for the window watchdog detailed operation.

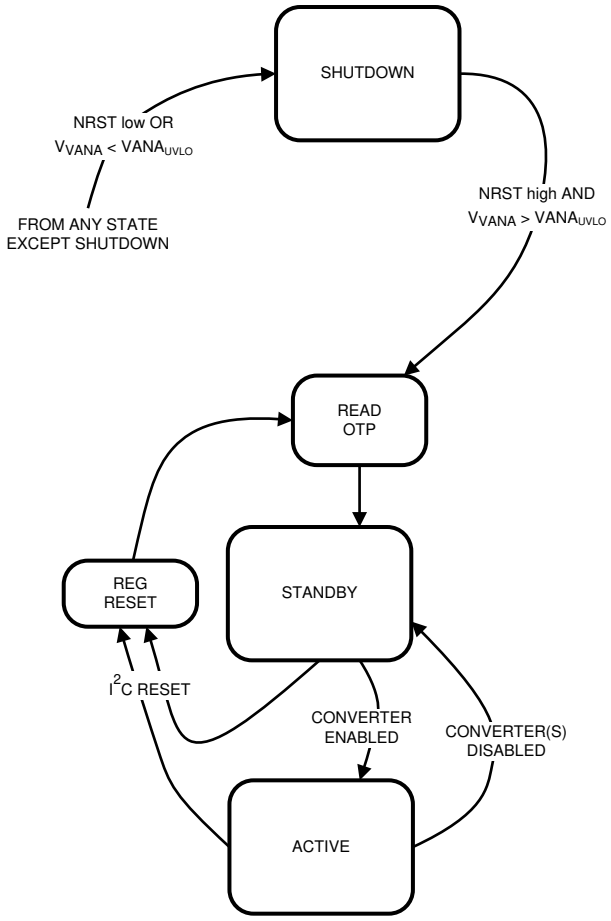


図 8-14. Device Operation Modes.

8.5 Programming

8.5.1 I²C-Compatible Interface

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the ICs connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pull-up resistor placed somewhere on the line and remain HIGH even when the bus is idle. The LP87702-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz).

8.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

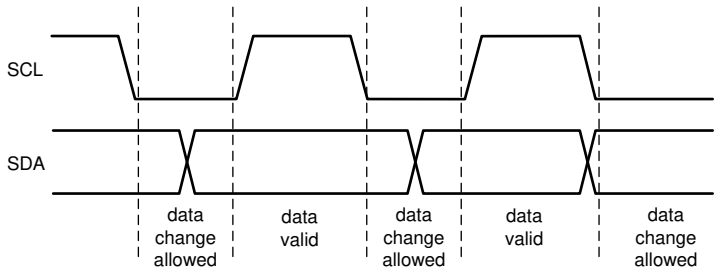


図 8-15. Data Validity Diagram

8.5.1.2 Start and Stop Conditions

The LP87702-Q1 is controlled through an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

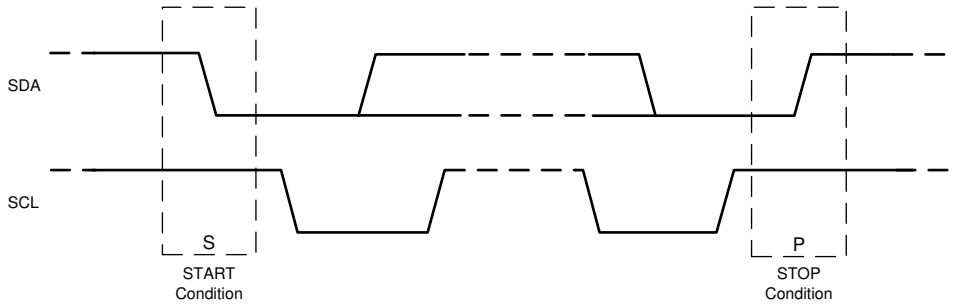


図 8-16. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. The I²C master can generate repeated START conditions during data transmission. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. 図 8-17 shows the SDA and SCL signal timing for the I²C-Compatible Bus. See セクション 7.6 for timing values.

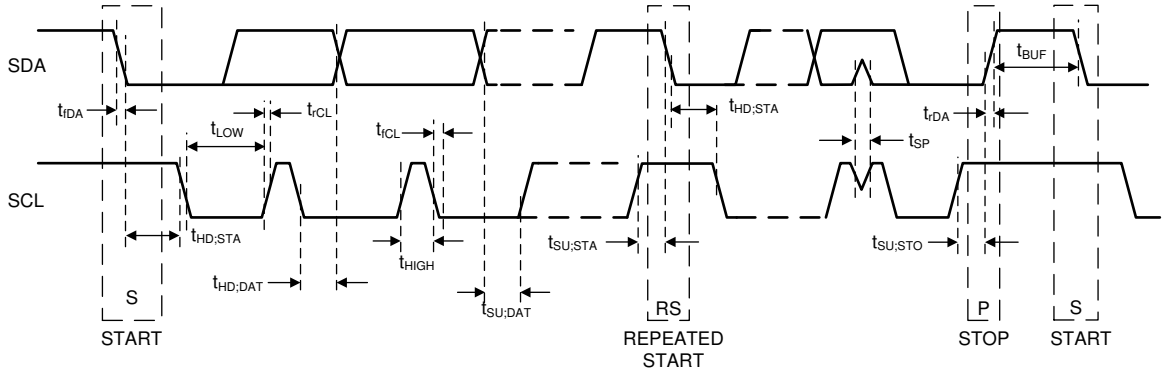


図 8-17. I²C-Compatible Timing

8.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP87702-Q1 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP87702-Q1 generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

Note

If the $V_{(VANA)}$ voltage is below the $VANA_{UVLO}$ threshold level during I²C communication, the LP87702-Q1 device does not drive the SDA line. The ACK signal and data transfer to the master is disabled at that time.

The bus master sends a chip address after the START condition. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). A 0 indicates a WRITE and a 1 indicates a READ for the eighth bit. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

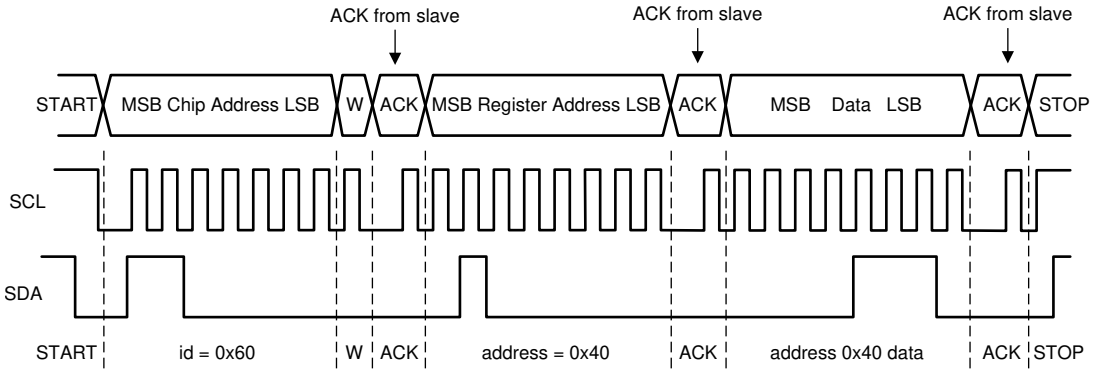
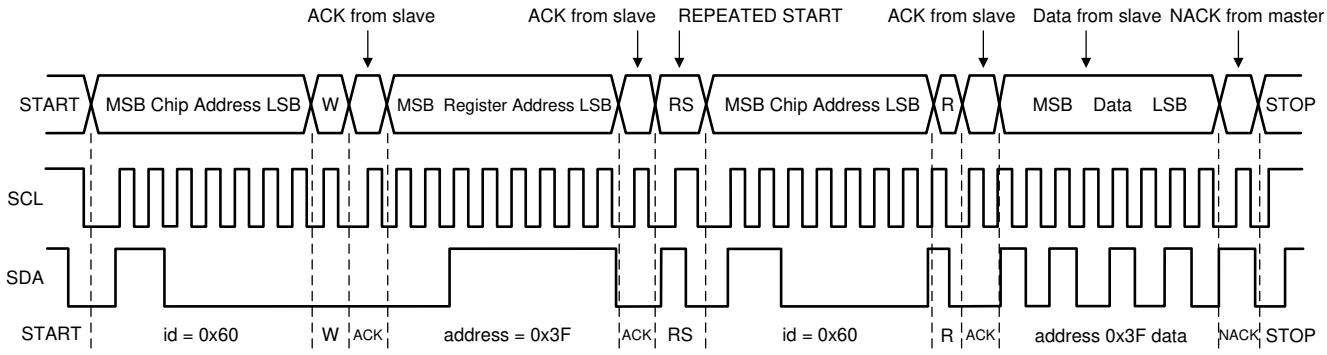


図 8-18. Write Cycle (w = write; SDA = 0), id = Device Address = 60Hex for LP87702-Q1

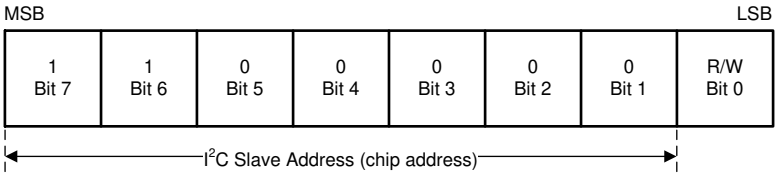


A WRITE function must precede the READ function as shown above when the READ function is accomplished.

図 8-19. Read Cycle (r = read; SDA = 1), id = Device Address = 60Hex for LP87702-Q1

8.5.1.4 I²C-Compatible Chip Address

The device address for the LP87702-Q1 is 0x60. After the START condition, the I²C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.



A. Here device address is 1100000Bin = 60Hex.

図 8-20. Device Address

8.5.1.5 Auto Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. The internal address index counter increments by one and the next register will be written every time an 8-bit word is sent to the LP87702-Q1. 表 8-8 below shows writing sequence to two consecutive registers. Note: the auto increment feature does not work for read.

表 8-8. Auto-Increment Example

MASTER ACTION	START	DEVICE ADDRESS = 60H	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
LP87702-Q1				ACK		ACK		ACK		ACK	

8.6 Register Maps

8.6.1 Register Descriptions

The LP87702-Q1 is controlled by a set of registers through the system serial interface port. This register map describes the default values for the bits which are not read from OTP memory. The asterisk (*) marking indicates the register bits which are updated from the OTP memory during the READ OTP state. OTP values for each orderable part number are described in a separate technical reference manual TRM.

8.6.1.1 LP8770_map Registers

表 8-9 lists the memory-mapped registers for the LP8770_map registers. All register offset addresses not listed in 表 8-9 should be considered as reserved locations and the register contents should not be modified.

表 8-9. LP8770_MAP Registers

Offset	Acronym	Register Name	Section
0h	DEV_REV		セクション 8.6.1.1.2
1h	OTP_CODE		セクション 8.6.1.1.3
2h	BUCK0_CTRL_1		セクション 8.6.1.1.4
3h	BUCK0_CTRL_2		セクション 8.6.1.1.5
4h	BUCK1_CTRL_1		セクション 8.6.1.1.6
5h	BUCK1_CTRL_2		セクション 8.6.1.1.7
6h	BUCK0_VOUT		セクション 8.6.1.1.8
7h	BUCK1_VOUT		セクション 8.6.1.1.9
8h	BOOST_CTRL		セクション 8.6.1.1.10
9h	BUCK0_DELAY		セクション 8.6.1.1.11
Ah	BUCK1_DELAY		セクション 8.6.1.1.12
Bh	BOOST_DELAY		セクション 8.6.1.1.13
Ch	GPO0_DELAY		セクション 8.6.1.1.14
Dh	GPO1_DELAY		セクション 8.6.1.1.15
Eh	GPO2_DELAY		セクション 8.6.1.1.16
Fh	GPO_CONTROL_1		セクション 8.6.1.1.17
10h	GPO_CONTROL_2		セクション 8.6.1.1.18
11h	CONFIG		セクション 8.6.1.1.19
12h	PLL_CTRL		セクション 8.6.1.1.20
13h	PGOOD_CTRL		セクション 8.6.1.1.21
14h	PGOOD_LEVEL_1		セクション 8.6.1.1.22
15h	PGOOD_LEVEL_2		セクション 8.6.1.1.23
16h	PGOOD_LEVEL_3		セクション 8.6.1.1.24
17h	PG_CTRL		セクション 8.6.1.1.25
18h	PG0_CTRL		セクション 8.6.1.1.26
19h	PG0_FAULT		セクション 8.6.1.1.27
1Ah	PG1_CTRL		セクション 8.6.1.1.28
1Bh	PG1_FAULT		セクション 8.6.1.1.29
1Ch	WD_CTRL_1		セクション 8.6.1.1.30
1Dh	WD_CTRL_2		セクション 8.6.1.1.31
1Eh	WD_STATUS		セクション 8.6.1.1.32
1Fh	RESET		セクション 8.6.1.1.33
20h	INT_TOP_1		セクション 8.6.1.1.34

表 8-9. LP8770_MAP Registers (continued)

Offset	Acronym	Register Name	Section
21h	INT_TOP_2		セクション 8.6.1.1.35
22h	INT_BUCK		セクション 8.6.1.1.36
23h	INT_BOOST		セクション 8.6.1.1.37
24h	INT_DIAG		セクション 8.6.1.1.38
25h	TOP_STATUS		セクション 8.6.1.1.39
26h	BUCK_STATUS		セクション 8.6.1.1.40
27h	BOOST_STATUS		セクション 8.6.1.1.41
28h	DIAG_STATUS		セクション 8.6.1.1.42
29h	TOP_MASK_1		セクション 8.6.1.1.43
2Ah	TOP_MASK_2		セクション 8.6.1.1.44
2Bh	BUCK_MASK		セクション 8.6.1.1.45
2Ch	BOOST_MASK		セクション 8.6.1.1.46
2Dh	DIAG_MASK		セクション 8.6.1.1.47
2Eh	SEL_I_LOAD		セクション 8.6.1.1.48
2Fh	I_LOAD_2		セクション 8.6.1.1.49
30h	I_LOAD_1		セクション 8.6.1.1.50
31h	FREQ_SEL		セクション 8.6.1.1.51
32h	BOOST_ILIM_CTRL		セクション 8.6.1.1.52
33h	ECC_STATUS		セクション 8.6.1.1.53
34h	WD_DIS_CTRL_CODE		セクション 8.6.1.1.54
35h	WD_DIS_CONTROL		セクション 8.6.1.1.55

Complex bit access types are encoded to fit into small table cells. 表 8-10 shows the codes that are used for access types in this section.

表 8-10. LP8770_map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

8.6.1.1.1 DEV_REV Register (Offset = 0h) [reset = 0h]

DEV_REV is shown in 図 8-19 and described in 表 8-11.

Return to 表 8-9.

図 8-19. DEV_REV Register

7	6	5	4	3	2	1	0
RESERVED		DEVICE_ID			RESERVED		
R-0h		R-0h			R-0h		

表 8-11. DEV_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-3	DEVICE_ID	R	0h	Device specific ID code. (Default from OTP memory)
2-0	RESERVED	R	0h	Reserved

8.6.1.1.2 OTP_CODE Register (Offset = 1h) [reset = 0h]

OTP_CODE is shown in 図 8-20 and described in 表 8-12.

Return to 表 8-9.

図 8-20. OTP_CODE Register

7	6	5	4	3	2	1	0
OTP_ID						OTP_REV	
R-0h						R-0h	

表 8-12. OTP_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	OTP_ID	R	0h	Identification Code of the OTP EPROM. (Default from OTP memory)
1-0	OTP_REV	R	0h	Version number of the OTP ID. (Default from OTP memory)

8.6.1.1.3 BUCK0_CTRL_1 Register (Offset = 2h) [reset = 8h]

BUCK0_CTRL_1 is shown in 図 8-21 and described in 表 8-13.

Return to 表 8-9.

図 8-21. BUCK0_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK0_FPWM_MP	BUCK0_FPWM	BUCK0_RDIS_EN	BUCK0_EN_PIN_CTRL		BUCK0_EN
R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h

表 8-13. BUCK0_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	

表 8-13. BUCK0_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	BUCK0_FPWM_MP	R/W	0h	Forces the BUCK0 converter to operate always in multi-phase and forced PWM operation mode: 0 – Automatic phase adding and shedding. 1 – Forced to multi-phase operation, 2 phases in the 2-phase configuration. (Default from OTP memory)
4	BUCK0_FPWM	R/W	0h	Forces the BUCK0 converter to operate in PWM mode: 0 – Automatic transitions between PFM and PWM modes (AUTO mode). 1 – Forced to PWM operation. (Default from OTP memory)
3	BUCK0_RDIS_EN	R/W	1h	Enable output discharge resistor when BUCK0 is disabled: 0 – Discharge resistor disabled 1 – Discharge resistor enabled.
2-1	BUCK0_EN_PIN_CTRL	R/W	0h	Enable or disable control for BUCK0: 0x0 – only BUCK0_EN bit controls BUCK0 0x1 – BUCK0_EN bit AND EN1 pin control BUCK0 0x2 – BUCK0_EN bit AND EN2 pin control BUCK0 0x3 – BUCK0_EN bit AND EN3 pin control BUCK0 (Default from OTP memory)
0	BUCK0_EN	R/W	0h	Enable BUCK0 converter: 0 – BUCK0 converter is disabled 1 – BUCK0 converter is enabled. (Default from OTP memory)

8.6.1.1.4 BUCK0_CTRL_2 Register (Offset = 3h) [reset = 1Ah]

BUCK0_CTRL_2 is shown in 図 8-22 and described in 表 8-14.

Return to 表 8-9.

図 8-22. BUCK0_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK0_ILIM			BUCK0_SLEW_RATE		
R/W-0h		R/W-3h			R/W-2h		

表 8-14. BUCK0_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK0_ILIM	R/W	3h	Sets the switch peak current limit of BUCK0. Can be programmed at any time during operation: 0x0 – 1.5 A 0x1 – 2.0 A 0x2 – 2.5 A 0x3 – 3.0 A 0x4 – 3.5 A 0x5 – 4.0 A 0x6 – 4.5 A 0x7 – Reserved (Default from OTP memory)

表 8-14. BUCK0_CTRL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BUCK0_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK0 converter (rising and falling edges): 0x0 – Reserved 0x1 – Reserved 0x2 – 10 mV/µs 0x3 – 7.5 mV/µs 0x4 – 3.8 mV/µs 0x5 – 1.9 mV/µs 0x6 – 0.94 mV/µs 0x7 – 0.47 mV/µs (Default from OTP memory)

8.6.1.1.5 BUCK1_CTRL_1 Register (Offset = 4h) [reset = 8h]

BUCK1_CTRL_1 is shown in 図 8-23 and described in 表 8-15.

Return to 表 8-9.

図 8-23. BUCK1_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK1_FPWM	BUCK1_RDIS_EN	BUCK1_EN_PIN_CTRL		BUCK1_EN
R/W-0h			R/W-0h	R/W-1h	R/W-0h		R/W-0h

表 8-15. BUCK1_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	BUCK1_FPWM	R/W	0h	Forces the BUCK1 converter to operate in PWM mode: 0 – Automatic transitions between PFM and PWM modes (AUTO mode). 1 – Forced to PWM operation. (Default from OTP memory)
3	BUCK1_RDIS_EN	R/W	1h	Enable output discharge resistor when BUCK1 is disabled: 0 – Discharge resistor disabled 1 – Discharge resistor enabled.
2-1	BUCK1_EN_PIN_CTRL	R/W	0h	Enable or disable control for BUCK1: 0x0 – only BUCK1_EN bit controls BUCK1 0x1 – BUCK1_EN bit AND EN1 pin control BUCK1 0x2 – BUCK1_EN bit AND EN2 pin control BUCK1 0x3 – BUCK1_EN bit AND EN3 pin control BUCK1 (Default from OTP memory)
0	BUCK1_EN	R/W	0h	Enable BUCK1 converter: 0 – BUCK1 converter is disabled 1 – BUCK1 converter is enabled. (Default from OTP memory)

8.6.1.1.6 BUCK1_CTRL_2 Register (Offset = 5h) [reset = 1Ah]

BUCK1_CTRL_2 is shown in 図 8-24 and described in 表 8-16.

Return to 表 8-9.

図 8-24. BUCK1_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_ILIM			BUCK1_SLEW_RATE		
R/W-0h		R/W-3h			R/W-2h		

図 8-24. BUCK1_CTRL_2 Register (continued)

表 8-16. BUCK1_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK1_ILIM	R/W	3h	Sets the switch peak current limit of BUCK1. Can be programmed at any time during operation: 0x0 – 1.5 A 0x1 – 2.0 A 0x2 – 2.5 A 0x3 – 3.0 A 0x4 – 3.5 A 0x5 – 4.0 A 0x6 – 4.5 A 0x7 – Reserved (Default from OTP memory)
2-0	BUCK1_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK1 converter (rising and falling edges): 0x0 – Reserved 0x1 – Reserved 0x2 – 10 mV/µs 0x3 – 7.5 mV/µs 0x4 – 3.8 mV/µs 0x5 – 1.9 mV/µs 0x6 – 0.94 mV/µs 0x7 – 0.47 mV/µs (Default from OTP memory)

8.6.1.1.7 BUCK0_VOUT Register (Offset = 6h) [reset = 0h]

BUCK0_VOUT is shown in 図 8-25 and described in 表 8-17.

Return to 表 8-9.

図 8-25. BUCK0_VOUT Register

7	6	5	4	3	2	1	0
BUCK0_VSET							
R/W-0h							

表 8-17. BUCK0_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK0_VSET	R/W	0h	Output voltage of BUCK0 converter: 0x00 ... 0x13, Reserved, DO NOT USE 0.7 V – 0.73 V, 10 mV steps 0x14 – 0.7 V ... 0x17 – 0.73 V 0.73 V – 1.4 V, 5 mV steps 0x18 – 0.735 V ... 0x9D – 1.4 V 1.4 V – 3.36 V, 20 mV steps 0x9E – 1.42 V ... 0xFF – 3.36 V (Default from OTP memory)

8.6.1.1.8 BUCK1_VOUT Register (Offset = 7h) [reset = 0h]

BUCK1_VOUT is shown in 図 8-26 and described in 表 8-18.

Return to 表 8-9.

図 8-26. BUCK1_VOUT Register

7	6	5	4	3	2	1	0
BUCK1_VSET							
R/W-0h							

表 8-18. BUCK1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK1_VSET	R/W	0h	Output voltage of BUCK1 converter 0x00 ... 0x13, Reserved, DO NOT USE 0.7 V – 0.73 V, 10 mV steps 0x14 – 0.7 V ... 0x17 – 0.73 V 0.73 V – 1.4 V, 5 mV steps 0x18 – 0.735 V ... 0x9D – 1.4 V 1.4 V – 3.36 V, 20 mV steps 0x9E – 1.42 V ... 0xFF – 3.36 V (Default from OTP memory)

8.6.1.1.9 BOOST_CTRL Register (Offset = 8h) [reset = 8h]

BOOST_CTRL is shown in 図 8-27 and described in 表 8-19.

Return to 表 8-9.

図 8-27. BOOST_CTRL Register

7	6	5	4	3	2	1	0
BOOST_VSET		RESERVED	RESERVED	BOOST_RDIS_EN	BOOST_EN_PIN_CTRL		BOOST_EN
R/W-0h		R/W-0h	R/W-1h	R/W-1h	R/W-0h		R/W-0h

表 8-19. BOOST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BOOST_VSET	R/W	0h	Output voltage of Boost: 0x0 – 4.9 V 0x1 – 5.0 V 0x2 – 5.1 V 0x3 – 5.2 V (Default from OTP memory)
5	RESERVED	R/W	0h	
4	RESERVED	R/W	1h	
3	BOOST_RDIS_EN	R/W	1h	Enable output discharge resistor when BOOST is disabled: 0 – Discharge resistor disabled 1 – Discharge resistor enabled.

表 8-19. BOOST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	BOOST_EN_PIN_CTRL	R/W	0h	Enable or disable control for Boost: 0x0 – only BOOST_EN bit controls Boost 0x1 – BOOST_EN bit AND EN1 pin control Boost 0x2 – BOOST_EN bit AND EN2 pin control Boost 0x3 – BOOST_EN bit AND EN3 pin control Boost (Default from OTP memory)
0	BOOST_EN	R/W	0h	Enable Boost converter: 0 – Boost converter is disabled 1 – Boost converter is enabled. (Default from OTP memory)

8.6.1.1.10 BUCK0_DELAY Register (Offset = 9h) [reset = 0h]

BUCK0_DELAY is shown in 図 8-28 and described in 表 8-20.

Return to 表 8-9.

図 8-28. BUCK0_DELAY Register

7	6	5	4	3	2	1	0
BUCK0_SHUTDOWN_DELAY				BUCK0_STARTUP_DELAY			
R/W-0h				R/W-0h			

表 8-20. BUCK0_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK0_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of BUCK0 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BUCK0_STARTUP_DELAY	R/W	0h	Startup delay of BUCK0 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

8.6.1.1.11 BUCK1_DELAY Register (Offset = Ah) [reset = 0h]

BUCK1_DELAY is shown in 図 8-29 and described in 表 8-21.

Return to 表 8-9.

図 8-29. BUCK1_DELAY Register

7	6	5	4	3	2	1	0
BUCK1_SHUTDOWN_DELAY				BUCK1_STARTUP_DELAY			
R/W-0h				R/W-0h			

表 8-21. BUCK1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK1_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of BUCK1 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BUCK1_STARTUP_DELAY	R/W	0h	Startup delay of BUCK1 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

8.6.1.1.12 BOOST_DELAY Register (Offset = Bh) [reset = 0h]

BOOST_DELAY is shown in 図 8-30 and described in 表 8-22.

Return to 表 8-9.

図 8-30. BOOST_DELAY Register

7	6	5	4	3	2	1	0
BOOST_SHUTDOWN_DELAY				BOOST_STARTUP_DELAY			
R/W-0h				R/W-0h			

表 8-22. BOOST_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BOOST_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of Boost from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BOOST_STARTUP_DELAY	R/W	0h	Startup delay of Boost from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

8.6.1.1.13 GPO0_DELAY Register (Offset = Ch) [reset = 0h]

GPO0_DELAY is shown in 図 8-31 and described in 表 8-23.

Return to 表 8-9.

図 8-31. GPO0_DELAY Register

7	6	5	4	3	2	1	0
GPO0_SHUTDOWN_DELAY				GPO0_STARTUP_DELAY			
R/W-0h				R/W-0h			

表 8-23. GPO0_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO0_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO0 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO0_STARTUP_DELAY	R/W	0h	Startup delay of GPO0 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

8.6.1.1.14 GPO1_DELAY Register (Offset = Dh) [reset = 0h]

GPO1_DELAY is shown in 図 8-32 and described in 表 8-24.

Return to 表 8-9.

図 8-32. GPO1_DELAY Register

7	6	5	4	3	2	1	0
GPO1_SHUTDOWN_DELAY				GPO1_STARTUP_DELAY			
R/W-0h				R/W-0h			

表 8-24. GPO1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO1_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO1 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15b ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO1_STARTUP_DELAY	R/W	0h	Startup delay of GPO1 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

8.6.1.1.15 GPO2_DELAY Register (Offset = Eh) [reset = 0h]

GPO2_DELAY is shown in 図 8-33 and described in 表 8-25.

Return to 表 8-9.

図 8-33. GPO2_DELAY Register

7	6	5	4	3	2	1	0
GPO2_SHUTDOWN_DELAY				GPO2_STARTUP_DELAY			
R/W-0h				R/W-0h			

表 8-25. GPO2_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO2_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO2 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO2_STARTUP_DELAY	R/W	0h	Startup delay of GPO2 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

8.6.1.1.16 GPO_CONTROL_1 Register (Offset = Fh) [reset = AAh]

GPO_CONTROL_1 is shown in 図 8-34 and described in 表 8-26.

Return to 表 8-9.

図 8-34. GPO_CONTROL_1 Register

7	6	5	4	3	2	1	0
GPO1_PG1_OD	GPO1_EN_PIN_CTRL		GPO1_OUT	GPO0_OD	GPO0_EN_PIN_CTRL		GPO0_OUT
R/W-1h	R/W-1h		R/W-0h	R/W-1h	R/W-1h		R/W-0h

表 8-26. GPO_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPO1_PG1_OD	R/W	1h	GPO1/PG1 signal type: 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)
6-5	GPO1_EN_PIN_CTRL	R/W	1h	Control for GPO1 output: 0x0 – only GPO1_OUT bit controls GPO1 0x1 – GPO1_OUT bit AND EN1 pin control GPO1 0x2 – GPO1_OUT bit AND EN2 pin control GPO1 0x3 – GPO1_OUT bit AND EN3 pin control GPO1 (Default from OTP memory)
4	GPO1_OUT	R/W	0h	Control for GPO1 signal (when configured to GPO1): 0 – Logic low level 1 – Logic high level (Default from OTP memory)
3	GPO0_OD	R/W	1h	GPO0 signal type: 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)
2-1	GPO0_EN_PIN_CTRL	R/W	1h	Control for GPO0 output: 0x0 – only GPO0_OUT bit controls GPO0 0x1 – GPO0_OUT bit AND EN1 pin control GPO0 0x2 – GPO0_OUT bit AND EN2 pin control GPO0 0x3 – GPO0_OUT bit AND EN3 pin control GPO0 (Default from OTP memory)
0	GPO0_OUT	R/W	0h	Control for GPO0 signal: 0 – Logic low level 1 – Logic high level (Default from OTP memory)

8.6.1.1.17 GPO_CONTROL_2 Register (Offset = 10h) [reset = Ah]

GPO_CONTROL_2 is shown in 図 8-35 and described in 表 8-27.

Return to 表 8-9.

図 8-35. GPO_CONTROL_2 Register

7	6	5	4	3	2	1	0
RESERVED		GPO2_SEL	GPO1_SEL	GPO2_OD	GPO2_EN_PIN_CTRL		GPO2_OUT
R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-1h		R/W-0h

表 8-27. GPO_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	GPO2_SEL	R/W	0h	CLKIN/GPO2 pin function: 0 – CLKIN 1 – GPO2 (Default from OTP memory)
4	GPO1_SEL	R/W	0h	PG1/GPO1 pin function: 0 – PG1 1 – GPO1 (Default from OTP memory)
3	GPO2_OD	R/W	1h	GPO2 signal type (when configured to GPO2): 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)
2-1	GPO2_EN_PIN_CTRL	R/W	1h	Control for GPO2 output: 0x0 – only GPO2_OUT bit controls GPO2 0x1 – GPO2_OUT bit AND EN1 pin control GPO2 0x2 – GPO2_OUT bit AND EN2 pin control GPO2 0x3 – GPO2_OUT bit AND EN3 pin control GPO2 (Default from OTP memory)
0	GPO2_OUT	R/W	0h	Control for GPO2 signal (when configured to GPO2): 0 – Logic low level 1 – Logic high level (Default from OTP memory)

8.6.1.1.18 CONFIG Register (Offset = 11h) [reset = 3Ch]

CONFIG is shown in 図 8-36 and described in 表 8-28.

Return to 表 8-9.

図 8-36. CONFIG Register

7	6	5	4	3	2	1	0
STARTUP_DELAY_SEL	SHUTDOWN_DELAY_SEL	CLKIN_PD	EN3_PD	EN2_PD	EN1_PD	TDIE_WARN_LEVEL	EN_SPREAD_SPEC
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

表 8-28. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STARTUP_DELAY_SEL	R/W	0h	Startup delays from control signal: 0 – 0 ms – 7.5 ms with 0.5ms steps 1 – 0ms – 15ms with 1ms steps (Default from OTP memory)

表 8-28. CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SHUTDOWN_DELAY_SEL	R/W	0h	Shutdown delays from from signal: 0 – 0ms – 7.5ms with 0.5ms steps 1 – 0ms – 15ms with 1ms steps (Default from OTP memory)
5	CLKIN_PD	R/W	1h	Selects the pull down resistor on the CLKIN input pin. 0 – Pull-down resistor is disabled. 1 – Pull-down resistor is enabled. (Default from OTP memory)
4	EN3_PD	R/W	1h	Selects the pull down resistor on the EN3 pin: 0 – Pull-down resistor is disabled 1 – Pull-down resistor is enabled (Default from OTP memory)
3	EN2_PD	R/W	1h	Selects the pull down resistor on the EN2 pin: 0 – Pull-down resistor is disabled 1 – Pull-down resistor is enabled (Default from OTP memory)
2	EN1_PD	R/W	1h	Selects the pull down resistor on the EN1 pin: 0 – Pull-down resistor is disabled 1 – Pull-down resistor is enabled (Default from OTP memory)
1	TDIE_WARN_LEVEL	R/W	0h	Thermal warning threshold level. 0 – 125°C 1 – 140°C. (Default from OTP memory)
0	EN_SPREAD_SPEC	R/W	0h	Enable spread spectrum feature for Buck and Boost converters. 0 – Disabled 1 – Enabled (Default from OTP memory)

8.6.1.1.19 PLL_CTRL Register (Offset = 12h) [reset = 2h]

PLL_CTRL is shown in 図 8-37 and described in 表 8-29.

Return to 表 8-9.

図 8-37. PLL_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	EN_PLL	EN_FRAC_DIV	EXT_CLK_FREQ				
R/W-0h	R/W-0h	R/W-0h	R/W-2h				

表 8-29. PLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	EN_PLL	R/W	0h	Selection of external clock and PLL operation: 0 – Forced to internal RC oscillator. PLL disabled. 1 – PLL is enabled in STANDBY and ACTIVE modes. Automatic external clock use when available, interrupt generated if external clock appears or disappears. (Default from OTP memory)
5	EN_FRAC_DIV	R/W	0h	This bit must be set to '0'.

表 8-29. PLL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	EXT_CLK_FREQ	R/W	2h	Frequency of the external clock (CLKIN): 0x00 – 1 MHz 0x01 – 2 MHz 0x02 – 3 MHz ... 0x16 – 23 MHz 0x17 – 24 MHz 0x18...0x1F – Reserved See electrical specification for input clock frequency tolerance. (Default from OTP memory) Note: To ensure proper operation of PLL, EXT_CLK_FREQ value must not be changed when PLL is enabled.

8.6.1.1.20 PGOOD_CTRL Register (Offset = 13h) [reset = 0h]

PGOOD_CTRL is shown in 図 8-38 and described in 表 8-30.

Return to 表 8-9.

図 8-38. PGOOD_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	PGOOD_WINDOW	EN_PGOOD_VANA	EN_PGOOD_VMON2	EN_PGOOD_VMON1	EN_PGOOD_BOOST	EN_PGOOD_BUCK1	EN_PGOOD_BUCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-30. PGOOD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	PGOOD_WINDOW	R/W	0h	Voltage monitoring method for PG0 and PG1 signals: 0 - Only undervoltage monitoring. 1 - Overvoltage and undervoltage monitoring. (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
5	EN_PGOOD_VANA	R/W	0h	Enable powergood diagnostics for VANA 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
4	EN_PGOOD_VMON2	R/W	0h	Enable powergood diagnostics for VMON2 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
3	EN_PGOOD_VMON1	R/W	0h	Enable powergood diagnostics for VMON1 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
2	EN_PGOOD_BOOST	R/W	0h	Enable powergood diagnostics for Boost 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
1	EN_PGOOD_BUCK1	R/W	0h	Enable powergood diagnostics for Buck1 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.

表 8-30. PGOOD_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN_PGOOD_BUCK0	R/W	0h	Enable powergood diagnostics for Buck0 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.

8.6.1.1.21 PGOOD_LEVEL_1 Register (Offset = 14h) [reset = 0h]

PGOOD_LEVEL_1 is shown in 図 8-39 and described in 表 8-31.

Return to 表 8-9.

図 8-39. PGOOD_LEVEL_1 Register

7	6	5	4	3	2	1	0
RESERVED			VMON1_WINDOW		VMON1_THRESHOLD		
R/W-0h			R/W-0h		R/W-0h		

表 8-31. PGOOD_LEVEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	VMON1_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VMON1: 0x0 – ±2% 0x1 – ±3% 0x2 – ±4% 0x3 – ±6% (Default from OTP memory)
2-0	VMON1_THRESHOLD	R/W	0h	Threshold voltage for VMON1 input: 0x0 – 0.65V (high impedance input, external resistive divider can be used) 0x1 – 0.80 V 0x2 – 1.00 V 0x3 – 1.10 V 0x4 – 1.20 V 0x5 – 1.30 V 0x6 – 1.80 V 0x7 – 1.80 V To monitor any other voltage level, select 0x0 and use an external resistive divider to scale down to 0.65 V. For other than 0x0 VMONx input is low impedance (internal resistive divider enabled). (Default from OTP memory)

8.6.1.1.22 PGOOD_LEVEL_2 Register (Offset = 15h) [reset = 0h]

PGOOD_LEVEL_2 is shown in 図 8-40 and described in 表 8-32.

Return to 表 8-9.

図 8-40. PGOOD_LEVEL_2 Register

7	6	5	4	3	2	1	0
VANA_WINDOW		VANA_THRESHOLD	VMON2_WINDOW		VMON2_THRESHOLD		
R/W-0h		R/W-0h	R/W-0h		R/W-0h		

表 8-32. PGOOD_LEVEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VANA_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VANA: 0x0 – ±4% 0x1 – ±5% 0x2 – ±10% 0x3 – ±10% (Default from OTP memory)
5	VANA_THRESHOLD	R/W	0h	Threshold voltage for VANA input: 0 – 3.3 V 1 – 5.0 V (Default from OTP memory)
4-3	VMON2_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VMON2: 0x0 – ±2% 0x1 – ±3% 0x2 – ±4% 0x3 – ±6% (Default from OTP memory)
2-0	VMON2_THRESHOLD	R/W	0h	Threshold voltage for VMON2 input: 0x0 – 0.65 V (high impedance input, external resistive divider can be used) 0x1 – 0.80 V 0x2 – 1.00 V 0x3 – 1.10 V 0x4 – 1.20 V 0x5 – 1.30 V 0x6 – 1.80 V 0x7 – 1.80 V To monitor any other voltage level, select 0x0 and use an external resistive divider to scale down to 0.65 V. For other than 0x0 VMONx input is low impedance (internal resistive divider enabled). (Default from OTP memory)

8.6.1.1.23 PGOOD_LEVEL_3 Register (Offset = 16h) [reset = 0h]

PGOOD_LEVEL_3 is shown in 図 8-41 and described in 表 8-33.

Return to 表 8-9.

図 8-41. PGOOD_LEVEL_3 Register

7	6	5	4	3	2	1	0
BOOST_WINDOW		BOOST_THRESHOLD		BUCK1_WINDOW		BUCK0_WINDOW	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

表 8-33. PGOOD_LEVEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BOOST_WINDOW	R/W	0h	Undervoltage or overvoltage threshold levels for Boost: 0x0 – ±2% 0x1 – ±4% 0x2 – ±6% 0x3 – ±8% (Default from OTP memory)
5-4	BOOST_THRESHOLD	R/W	0h	(Default from OTP memory)
3-2	BUCK1_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for Buck1: 0x0 – ±30 mV 0x1 – ±50 mV 0x2 – ±70 mV 0x3 – ±90 mV (Default from OTP memory)

表 8-33. PGOOD_LEVEL_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	BUCK0_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for Buck0: 0x0 – ±30 mV 0x1 – ±50 mV 0x2 – ±70 mV 0x3 – ±90 mV (Default from OTP memory)

8.6.1.1.24 PG_CTRL Register (Offset = 17h) [reset = 2h]

PG_CTRL is shown in 図 8-42 and described in 表 8-34.

Return to 表 8-9.

図 8-42. PG_CTRL Register

7	6	5	4	3	2	1	0
PG1_MODE	PGOOD_FAULT_GATES_PG1	RESERVED	PG1_POL	PG0_MODE	PGOOD_FAULT_GATES_PG0	PG0_OD	PG0_POL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

表 8-34. PG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG1_MODE	R/W	0h	Operating mode for PG1 signal: 0 – Detecting unusual situations 1 – Showing when requested outputs are not valid. (Default from OTP memory)
6	PGOOD_FAULT_GATES_PG1	R/W	0h	Type of operation for PG1 signal: 0 – Indicates live status of monitored voltage outputs. 1 – Indicates status of PG1_FAULT register, inactive if at least one of PG1_FAULT_x bit is inactive. (Default from OTP memory)
5	RESERVED	R/W	0h	
4	PG1_POL	R/W	0h	PG1 signal polarity. 0 – PG1 signal high when monitored outputs are valid 1 – PG1 signal low when monitored outputs are valid (Default from OTP memory)
3	PG0_MODE	R/W	0h	Operating mode for PG0 signal: 0 – Detecting unusual situations 1 – Showing when requested outputs are not valid. (Default from OTP memory)
2	PGOOD_FAULT_GATES_PG0	R/W	0h	Type of operation for PG0 signal: 0 – Indicates live status of monitored voltage outputs. 1 – Indicates status of PG0_FAULT register, inactive if at least one of PG0_FAULT_x bit is inactive. (Default from OTP memory)
1	PG0_OD	R/W	1h	PG0 signal type: 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)
0	PG0_POL	R/W	0h	PG0 signal polarity. 0 – PG0 signal high when monitored outputs are valid 1 – PG0 signal low when monitored outputs are valid (Default from OTP memory)

8.6.1.1.25 PG0_CTRL Register (Offset = 18h) [reset = 0h]

PG0_CTRL is shown in 図 8-43 and described in 表 8-35.

Return to 表 8-9.

図 8-43. PG0_CTRL Register

7	6	5	4	3	2	1	0
PG0_RISE_DELAY	SEL_PG0_TWARN	SEL_PG0_VANA	SEL_PG0_VMON2	SEL_PG0_VMON1	SEL_PG0_BOOST	SEL_PG0_BUCK1	SEL_PG0_BUCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-35. PG0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG0_RISE_DELAY	R/W	0h	0 – PG0 rise is not delayed 1 – PG0 rise is delayed 11 ms
6	SEL_PG0_TWARN	R/W	0h	PG0 control from thermal warning: 0 - Masked 1 – Affecting PGOOD (Default from OTP memory)
5	SEL_PG0_VANA	R/W	0h	PG0 signal source control from VANA 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
4	SEL_PG0_VMON2	R/W	0h	PG0 signal source control from VMON2 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
3	SEL_PG0_VMON1	R/W	0h	PG0 signal source control from VMON1 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
2	SEL_PG0_BOOST	R/W	0h	PG0 signal source control from Boost 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
1	SEL_PG0_BUCK1	R/W	0h	PG0 signal source control from Buck1 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
0	SEL_PG0_BUCK0	R/W	0h	PG0 signal source control from Buck0 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)

8.6.1.1.26 PG0_FAULT Register (Offset = 19h) [reset = 0h]

PG0_FAULT is shown in 図 8-44 and described in 表 8-36.

Return to 表 8-9.

図 8-44. PG0_FAULT Register

7	6	5	4	3	2	1	0
RESERVED	PG0_FAULT_TWARN	PG0_FAULT_VANA	PG0_FAULT_VMON2	PG0_FAULT_VMON1	PG0_FAULT_BOOST	PG0_FAULT_BUCK1	PG0_FAULT_BUCK0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-36. PG0_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PG0_FAULT_TWARN	R	0h	Source for PG0 inactive signal: 0 – TWARN has not set PG0 signal inactive. 1 – TWARN is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when TWARN is valid.
5	PG0_FAULT_VANA	R	0h	Source for PG0 inactive signal: 0 – VANA has not set PG0 signal inactive. 1 –VANA is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VANA input is valid.
4	PG0_FAULT_VMON2	R	0h	Source for PG0 inactive signal: 0 – VMON2 has not set PG0 signal inactive. 1 – VMON2 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VMON2 input is valid.
3	PG0_FAULT_VMON1	R	0h	Source for PG0 inactive signal: 0 – VMON1 has not set PG0 signal inactive. 1 – VMON1 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VMON1 input is valid.
2	PG0_FAULT_BOOST	R	0h	Source for PG0 inactive signal: 0 – Boost has not set PG0 signal inactive. 1 – Boost is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Boost output is valid.
1	PG0_FAULT_BUCK1	R	0h	Source for PG0 inactive signal: 0 – Buck1 has not set PG0 signal inactive. 1 – Buck1 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.
0	PG0_FAULT_BUCK0	R	0h	Source for PG0 inactive signal: 0 – Buck0 has not set PG0 signal inactive. 1 – Buck0 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

8.6.1.1.27 PG1_CTRL Register (Offset = 1Ah) [reset = 0h]

PG1_CTRL is shown in 図 8-45 and described in 表 8-37.

Return to 表 8-9.

図 8-45. PG1_CTRL Register

7	6	5	4	3	2	1	0
PG1_RISE_DELAY	SEL_PG1_TWARN	SEL_PG1_VANA	SEL_PG1_VMON2	SEL_PG1_VMON1	SEL_PG1_BOOST	SEL_PG1_BUCK1	SEL_PG1_BUCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-37. PG1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG1_RISE_DELAY	R/W	0h	0 – PG1 rise is not delayed 1 – PG1 rise is delayed 11ms
6	SEL_PG1_TWARN	R/W	0h	PG1 control from thermal warning: 0 – Masked 1 – Affecting PGOOD (Default from OTP memory)

表 8-37. PG1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SEL_PG1_VANA	R/W	0h	PG1 signal source control from VANA 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
4	SEL_PG1_VMON2	R/W	0h	PG1 signal source control from VMON2 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
3	SEL_PG1_VMON1	R/W	0h	PG1 signal source control from VMON1 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
2	SEL_PG1_BOOST	R/W	0h	PG1 signal source control from Boost 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
1	SEL_PG1_BUCK1	R/W	0h	PG1 signal source control from Buck1 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
0	SEL_PG1_BUCK0	R/W	0h	PG1 signal source control from Buck0 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)

8.6.1.1.28 PG1_FAULT Register (Offset = 1Bh) [reset = 0h]

PG1_FAULT is shown in 図 8-46 and described in 表 8-38.

Return to 表 8-9.

図 8-46. PG1_FAULT Register

7	6	5	4	3	2	1	0
RESERVED	PG1_FAULT_TWARN	PG1_FAULT_VANA	PG1_FAULT_VMON2	PG1_FAULT_VMON1	PG1_FAULT_BOOST	PG1_FAULT_BUCK1	PG1_FAULT_BUCK0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-38. PG1_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PG1_FAULT_TWARN	R	0h	Source for PG1 inactive signal: 0 – TWARN has not set PG1 signal inactive. 1 – TWARN is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when TWARN is valid.
5	PG1_FAULT_VANA	R	0h	Source for PG1 inactive signal: 0 – VANA has not set PG1 signal inactive. 1 – VANA is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VANA input is valid.
4	PG1_FAULT_VMON2	R	0h	Source for PG1 inactive signal: 0 – VMON2 has not set PG1 signal inactive. 1 – VMON2 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VMON2 input is valid.

表 8-38. PG1_FAULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PG1_FAULT_VMON1	R	0h	Source for PG1 inactive signal: 0 – VMON1 has not set PG1 signal inactive. 1 – VMON1 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VMON1 input is valid.
2	PG1_FAULT_BOOST	R	0h	Source for PG1 inactive signal: 0 – Boost has not set PG1 signal inactive. 1 – Boost is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Boost output is valid.
1	PG1_FAULT_BUCK1	R	0h	Source for PG1 inactive signal: 0 – Buck1 has not set PG1 signal inactive. 1 – Buck1 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.
0	PG1_FAULT_BUCK0	R	0h	Source for PG1 inactive signal: 0 – Buck0 has not set PG1 signal inactive. 1 – Buck0 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

8.6.1.1.29 WD_CTRL_1 Register (Offset = 1Ch) [reset = 0h]

WD_CTRL_1 is shown in 図 8-47 and described in 表 8-39.

Return to 表 8-9.

図 8-47. WD_CTRL_1 Register

7	6	5	4	3	2	1	0
WD_CLOSE_TIME		WD_OPEN_TIME		WD_LONG_OPEN_TIME		WD_RESET_CNTR_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

表 8-39. WD_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CLOSE_TIME	R/W	0h	Watchdog close window time select. 00 – 10 ms 01 – 20 ms 10 – 50 ms 11 – 100 ms (Default from OTP memory)
5-4	WD_OPEN_TIME	R/W	0h	Watchdog open window time select. 00 – 20 ms 01 – 100 ms 10 – 200 ms 11 – 600 ms (Default from OTP memory)
3-2	WD_LONG_OPEN_TIME	R/W	0h	Watchdog long open window time select. 00 – 200 ms 01 – 600 ms 10 – 2000 ms 11 – 5000 ms (Default from OTP memory)

表 8-39. WD_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	WD_RESET_CNTR_SEL	R/W	0h	Watchdog reset counter threshold select. After the selected number of reset (WDR) pulses system restart sequence is initiated. 00 – system restart disabled 01 – 1 10 – 2 11 – 4 (Default from OTP memory)

8.6.1.1.30 WD_CTRL_2 Register (Offset = 1Dh) [reset = 1h]

WD_CTRL_2 is shown in 図 8-48 and described in 表 8-40.

Return to 表 8-9.

図 8-48. WD_CTRL_2 Register

7	6	5	4	3	2	1	0
WD_LOCK	RESERVED		WD_SYS_RESTART_FLAG_MODE	WD_EN_OTP_READ	WDI_PD	WDR_POL	WDR_OD
R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

表 8-40. WD_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_LOCK	R	0h	Lock bit for watchdog controls. Locks all controls to watchdog in registers WD_CTRL_1, WD_CTRL_2. Lock bit also locks itself. Once lock bit is written 1 it cannot be written 0. Only reset can clear it. 0 – Not locked 1 – Locked WD_STATUS register is not affected by WD_LOCK bit. WD_SYSTEM_RESTART_FLAG and WD_RESET_CNTR_STATUS can be cleared even if WD_LOCK=1. WD_RESET_CNTR_STATUS is valid only when WD_RESET_CNTR_SEL is set to either 00 or 03.
6-5	RESERVED	R/W	0h	
4	WD_SYS_RESTART_FLAG_MODE	R/W	0h	WD_SYSTEM_RESTART_FLAG mode select. 0 - WD_SYSTEM_RESTART_FLAG is only a status bit. 1 – WD_SYSTEM_RESTART_FLAG prevents further system restarts until it is cleared. (Default from OTP memory)
3	WD_EN_OTP_READ	R/W	0h	Read OTP during system restart sequence 0 – OTP read not enabled during system restart sequence 1 – OTP read enabled during system restart sequence (Default from OTP memory)
2	WDI_PD	R/W	0h	Selects the pull down resistor on the WDI pin: 0 – Pull-down resistor is disabled 1 – Pull-down resistor is enabled (Default from OTP memory)
1	WDR_POL	R/W	0h	Watchdog reset output (WDR) polarity select 0 – Active high 1 – Active low (Default from OTP memory)
0	WDR_OD	R/W	1h	Watchdog reset output (WDR) signal type 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)

8.6.1.1.31 WD_STATUS Register (Offset = 1Eh) [reset = 0h]

WD_STATUS is shown in 図 8-49 and described in 表 8-41.

Return to 表 8-9.

図 8-49. WD_STATUS Register

7	6	5	4	3	2	1	0

図 8-49. WD_STATUS Register (continued)

RESERVED	WD_CLR_SYSTEM_RESTART_FLAG	WD_SYSTEM_RESTART_FLAG	WD_CLR_RESET_CNTR	WD_RESET_CNTR_STATUS
R/W-0h	R-0h	R-0h	R-0h	R-0h

表 8-41. WD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	WD_CLR_SYSTEM_RESTART_FLAG	R	0h	Clear bit for WD_SYSTEM_RESTART_FLAG. Write 1 to generate a clear pulse. Reg bit value returns to 0 after clearing is finished.
3	WD_SYSTEM_RESTART_FLAG	R	0h	Watchdog requested system restart has occurred. Can be cleared by writing WD_CLR_SYSTEM_RESTART_FLAG bit 1.
2	WD_CLR_RESET_CNTR	R	0h	Watchdog reset counter clear. Write 1 to generate a clear pulse.
1-0	WD_RESET_CNTR_STATUS	R	0h	Current status of watchdog reset counter. The value is valid only when WD_RESET_CNTR_SEL is set to either 00 or 03.

8.6.1.1.32 RESET Register (Offset = 1Fh) [reset = 0h]

RESET is shown in 図 8-50 and described in 表 8-42.

Return to 表 8-9.

図 8-50. RESET Register

7	6	5	4	3	2	1	0
RESERVED							SW_RESET
R/W-0h							R-0h

表 8-42. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SW_RESET	R	0h	Software commanded reset. When written to 1, the registers will be reset to default values and OTP memory is read. The bit is automatically cleared.

8.6.1.1.33 INT_TOP_1 Register (Offset = 20h) [reset = 0h]

INT_TOP_1 is shown in 図 8-51 and described in 表 8-43.

Return to 表 8-9.

図 8-51. INT_TOP_1 Register

7	6	5	4	3	2	1	0
I_MEAS_INT	DIAG_INT	BOOST_INT	BUCK_INT	SYNC_CLK_INT	TDIE_SD_INT	TDIE_WARN_INT	OVP_INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-43. INT_TOP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I_MEAS_INT	R	0h	Latched status bit indicating that the load current measurement result is available in I_LOAD_1 and I_LOAD_2 registers. Write 1 to clear interrupt.

表 8-43. INT_TOP_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DIAG_INT	R	0h	Interrupt indicating that INT_DIAG register has a pending interrupt. The reason for the interrupt is indicated in INT_DIAG register. This bit is cleared automatically when INT_DIAG register is cleared to 0x00.
5	BOOST_INT	R	0h	Interrupt indicating that BOOST have a pending interrupt. The reason for the interrupt is indicated in INT_BOOST register. This bit is cleared automatically when INT_BOOST register is cleared to 0x00.
4	BUCK_INT	R	0h	Interrupt indicating that BUCK0 or BUCK1 have a pending interrupt. The reason for the interrupt is indicated in INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.
3	SYNC_CLK_INT	R	0h	Latched status bit indicating that the external clock frequency became valid or invalid. Write 1 to clear interrupt.
2	TDIE_SD_INT	R	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The converters have been disabled if they were enabled. The converters cannot be enabled if this bit is active. The actual status of the thermal warning is indicated by TDIE_SD_STAT bit in TOP_STATUS register. Write 1 to clear interrupt. Clearing TSD interrupt automatically re-enables converters. Clearing this interrupt will also clear thermal warning status.
1	TDIE_WARN_INT	R	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TDIE_WARN_STAT bit in TOP_STATUS register. Write 1 to clear interrupt.
0	OVP_INT	R	0h	Latched status bit indicating that the input voltage has exceeded the over-voltage detection level. The actual status of the over-voltage is indicated by OVP bit in TOP_STATUS register. Write 1 to clear interrupt.

8.6.1.1.34 INT_TOP_2 Register (Offset = 21h) [reset = 0h]

INT_TOP_2 is shown in 図 8-52 and described in 表 8-44.

Return to 表 8-9.

図 8-52. INT_TOP_2 Register

7	6	5	4	3	2	1	0
RESERVED							RESET_REG_INT
R/W-0h							R-0h

表 8-44. INT_TOP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_REG_INT	R	0h	Latched status bit indicating that either VANA supply voltage has been below undervoltage threshold level or the host has requested a reset (SW_RESET bit in RESET register). The converters have been disabled, and registers are reset to default values and the normal startup procedure is done. Write 1 to clear interrupt.

8.6.1.1.35 INT_BUCK Register (Offset = 22h) [reset = 0h]

INT_BUCK is shown in 図 8-53 and described in 表 8-45.

Return to 表 8-9.

図 8-53. INT_BUCK Register

7	6	5	4	3	2	1	0
RESERVED	BUCK1_PG_INT	BUCK1_SC_INT	BUCK1_ILIM_INT	RESERVED	BUCK0_PG_INT	BUCK0_SC_INT	BUCK0_ILIM_INT
R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h

表 8-45. INT_BUCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	BUCK1_PG_INT	R	0h	Latched status bit indicating that BUCK1 powergood event has been detected. Write 1 to clear.
5	BUCK1_SC_INT	R	0h	Latched status bit indicating that the BUCK1 output voltage has fallen below 0.35 V level during operation or BUCK1 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
4	BUCK1_ILIM_INT	R	0h	Latched status bit indicating that BUCK1 output current limit has been triggered. Write 1 to clear.
3	RESERVED	R/W	0h	
2	BUCK0_PG_INT	R	0h	Latched status bit indicating that BUCK0 powergood event has been detected. Write 1 to clear.
1	BUCK0_SC_INT	R	0h	Latched status bit indicating that the BUCK0 output voltage has fallen below 0.35 V level during operation or BUCK0 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
0	BUCK0_ILIM_INT	R	0h	Latched status bit indicating that BUCK0 output current limit has been triggered. Write 1 to clear.

8.6.1.1.36 INT_BOOST Register (Offset = 23h) [reset = 0h]

INT_BOOST is shown in 図 8-54 and described in 表 8-46.

Return to 表 8-9.

図 8-54. INT_BOOST Register

7	6	5	4	3	2	1	0
RESERVED					BOOST_PG_INT	BOOST_SC_INT	BOOST_ILIM_INT
R/W-0h					R-0h	R-0h	R-0h

表 8-46. INT_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	BOOST_PG_INT	R	0h	Latched status bit indicating that Boost powergood event has been detected. Write 1 to clear.

表 8-46. INT_BOOST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BOOST_SC_INT	R	0h	Latched status bit indicating that the Boost output voltage has fallen to input voltage level or below 2.5 V level during operation or BOOST output didn't reach 2.5 V level in 1 ms from enable. Write 1 to clear.
0	BOOST_ILIM_INT	R	0h	Latched status bit indicating that Boost output current limit has been triggered. Write 1 to clear.

8.6.1.1.37 INT_DIAG Register (Offset = 24h) [reset = 0h]

INT_DIAG is shown in 図 8-55 and described in 表 8-47.

Return to 表 8-9.

図 8-55. INT_DIAG Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_PG_INT	RESERVED	VMON1_PG_INT	RESERVED	VANA_PG_INT
R/W-0h			R-0h	R/W-0h	R-0h	R/W-0h	R-0h

表 8-47. INT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	VMON2_PG_INT	R	0h	Latched status bit indicating that VMON2 powergood event has been detected. Write 1 to clear.
3	RESERVED	R/W	0h	
2	VMON1_PG_INT	R	0h	Latched status bit indicating that VMON1 powergood event has been detected. Write 1 to clear.
1	RESERVED	R/W	0h	
0	VANA_PG_INT	R	0h	Latched status bit indicating that VANA powergood event has been detected. Write 1 to clear.

8.6.1.1.38 TOP_STATUS Register (Offset = 25h) [reset = 0h]

TOP_STATUS is shown in 図 8-56 and described in 表 8-48.

Return to 表 8-9.

図 8-56. TOP_STATUS Register

7	6	5	4	3	2	1	0
RESERVED				SYNC_CLK_STAT	TDIE_SD_STAT	TDIE_WARN_STAT	OVP_STAT
R-0h				R-0h	R-0h	R-0h	R-0h

表 8-48. TOP_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	SYNC_CLK_STAT	R	0h	Status bit indicating the status of external clock (CLKIN): 0 – External clock frequency is valid 1 – External clock frequency is not valid.

表 8-48. TOP_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TDIE_SD_STAT	R	0h	Status bit indicating the status of thermal shutdown: 0 – Die temperature below thermal shutdown level 1 – Die temperature above thermal shutdown level.
1	TDIE_WARN_STAT	R	0h	Status bit indicating the status of thermal warning: 0 – Die temperature below thermal warning level 1 – Die temperature above thermal warning level.
0	OVP_STAT	R	0h	Status bit indicating the status of input overvoltage monitoring: 0 – Input voltage below overvoltage threshold level 1 – Input voltage above overvoltage threshold level.

8.6.1.1.39 BUCK_STATUS Register (Offset = 26h) [reset = 0h]

BUCK_STATUS is shown in 図 8-57 and described in 表 8-49.

Return to 表 8-9.

図 8-57. BUCK_STATUS Register

7	6	5	4	3	2	1	0
BUCK1_STAT	BUCK1_PG_STAT	RESERVED	BUCK1_ILIM_STAT	BUCK0_STAT	BUCK0_PG_STAT	RESERVED	BUCK0_ILIM_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-49. BUCK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_STAT	R	0h	Status bit indicating the enable or disable status of BUCK1: 0 – BUCK1 converter is disabled 1 – BUCK1 converter is enabled.
6	BUCK1_PG_STAT	R	0h	Status bit indicating BUCK1 output voltage validity (raw status) 0 – BUCK1 output is not valid 1 – BUCK1 output is valid.
5	RESERVED	R	0h	Reserved
4	BUCK1_ILIM_STAT	R	0h	Status bit indicating BUCK1 current limit status (raw status) 0 – BUCK1 output current is below current limit threshold level 1 – BUCK1 output current is at current limit threshold level.
3	BUCK0_STAT	R	0h	Status bit indicating the enable or disable status of BUCK0: 0 – BUCK0 converter is disabled 1 – BUCK0 converter is enabled.
2	BUCK0_PG_STAT	R	0h	Status bit indicating BUCK0 output voltage validity (raw status) 0 – BUCK0 output is not valid 1 – BUCK0 output is valid.
1	RESERVED	R	0h	Reserved
0	BUCK0_ILIM_STAT	R	0h	Status bit indicating BUCK0 current limit status (raw status) 0 – BUCK0 output current is below current limit threshold level 1 – BUCK0 output current is at current limit threshold level.

8.6.1.1.40 BOOST_STATUS Register (Offset = 27h) [reset = 0h]

BOOST_STATUS is shown in 図 8-58 and described in 表 8-50.

Return to 表 8-9.

図 8-58. BOOST_STATUS Register

7	6	5	4	3	2	1	0

図 8-58. BOOST_STATUS Register (continued)

RESERVED	BOOST_STAT	BOOST_PG_STAT	RESERVED	BOOST_ILIM_STAT
R-0h	R-0h	R-0h	R-0h	R-0h

表 8-50. BOOST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BOOST_STAT	R	0h	Status bit indicating the enable/disable status of Boost: 0 – Boost converter is disabled 1 – Boost converter is enabled.
2	BOOST_PG_STAT	R	0h	Status bit indicating Boost output voltage validity (raw status) 0 – Boost output is not valid 1 – Boost output is valid.
1	RESERVED	R	0h	Reserved
0	BOOST_ILIM_STAT	R	0h	Status bit indicating Boost current limit status (raw status) 0 – Boost output current is below current limit threshold level 1 – Boost output current is at current limit threshold level.

8.6.1.1.41 DIAG_STATUS Register (Offset = 28h) [reset = 0h]

DIAG_STATUS is shown in 図 8-59 and described in 表 8-51.

Return to 表 8-9.

図 8-59. DIAG_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_PG_STAT	RESERVED	VMON1_PG_STAT	RESERVED	VANA_PG_STAT
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

表 8-51. DIAG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	VMON2_PG_STAT	R	0h	Status bit indicating VMON2 input voltage validity (raw status) 0 – VMON2 voltage is not valid 1 – VMON2 voltage is valid.
3	RESERVED	R	0h	
2	VMON1_PG_STAT	R	0h	Status bit indicating VMON1 input voltage validity (raw status) 0 – VMON1 voltage is not valid 1 – VMON1 voltage is valid.
1	RESERVED	R	0h	
0	VANA_PG_STAT	R	0h	Status bit indicating VANA input voltage validity (raw status) 0 – VANA voltage is not valid 1 – VANA voltage is valid.

8.6.1.1.42 TOP_MASK_1 Register (Offset = 29h) [reset = 0h]

TOP_MASK_1 is shown in 図 8-60 and described in 表 8-52.

Return to 表 8-9.

図 8-60. TOP_MASK_1 Register

7	6	5	4	3	2	1	0

図 8-60. TOP_MASK_1 Register (continued)

I_MEAS_MASK	RESERVED	SYNC_CLK_MASK	RESERVED	TDIE_WARN_MASK	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-52. TOP_MASK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I_MEAS_MASK	R/W	0h	Masking for load current measurement ready interrupt I_MEAS_INT in INT_TOP_1 register. 0 – Interrupt generated 1 – Interrupt not generated. (Default from OTP memory)
6-4	RESERVED	R/W	0h	
3	SYNC_CLK_MASK	R/W	0h	Masking for external clock detection interrupt SYNC_CLK_INT in INT_TOP_1 register: 0 – Interrupt generated 1 – Interrupt not generated. (Default from OTP memory)
2	RESERVED	R/W	0h	
1	TDIE_WARN_MASK	R/W	0h	Masking for thermal warning interrupt TDIE_WARN_INT in INT_TOP_1 register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect TDIE_WARN_STAT status bit in TOP_STATUS register. (Default from OTP memory)
0	RESERVED	R/W	0h	

8.6.1.1.43 TOP_MASK_2 Register (Offset = 2Ah) [reset = 1h]

TOP_MASK_2 is shown in 図 8-61 and described in 表 8-53.

Return to 表 8-9.

図 8-61. TOP_MASK_2 Register

7	6	5	4	3	2	1	0
RESERVED							RESET_REG_MASK
R/W-0h							R/W-1h

表 8-53. TOP_MASK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_REG_MASK	R/W	1h	Masking for register reset interrupt RESET_REG_INT in INT_TOP_2 register: 0 – Interrupt generated 1 – Interrupt not generated. (Default from OTP memory)

8.6.1.1.44 BUCK_MASK Register (Offset = 2Bh) [reset = 0h]

BUCK_MASK is shown in 図 8-62 and described in 表 8-54.

Return to 表 8-9.

図 8-62. BUCK_MASK Register

7	6	5	4	3	2	1	0
BUCK1_PGF_MASK	BUCK1_PGR_MASK	RESERVED	BUCK1_ILIM_MASK	BUCK0_PGF_MASK	BUCK0_PGR_MASK	RESERVED	BUCK0_ILIM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-54. BUCK_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_PGF_MASK	R/W	0h	Masking of powergood invalid detection for BUCK1 power good interrupt BUCK1_PG_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
6	BUCK1_PGR_MASK	R/W	0h	Masking of powergood valid detection for BUCK1 power good interrupt BUCK1_PG_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
5	RESERVED	R/W	0h	
4	BUCK1_ILIM_MASK	R/W	0h	Masking for BUCK1 current monitoring interrupt BUCK1_ILIM_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK1_ILIM_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
3	BUCK0_PGF_MASK	R/W	0h	Masking of powergood invalid detection for BUCK0 power good interrupt BUCK0_PG_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
2	BUCK0_PGR_MASK	R/W	0h	Masking of powergood valid detection for BUCK0 power good interrupt BUCK0_PG_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
1	RESERVED	R/W	0h	
0	BUCK0_ILIM_MASK	R/W	0h	Masking for BUCK0 current monitoring interrupt BUCK0_ILIM_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK0_ILIM_STAT status bit in BUCK_STATUS register. (Default from OTP memory)

8.6.1.1.45 BOOST_MASK Register (Offset = 2Ch) [reset = 0h]

BOOST_MASK is shown in 図 8-63 and described in 表 8-55.

Return to 表 8-9.

図 8-63. BOOST_MASK Register

7	6	5	4	3	2	1	0
RESERVED				BOOST_PGF_MASK	BOOST_PGR_MASK	RESERVED	BOOST_ILIM_MASK
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-55. BOOST_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	BOOST_PGF_MASK	R/W	0h	Masking of powergood invalid detection for Boost power good interrupt BOOST_PG_INT in INT_BOOST register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BOOST_PG_STAT status bit in BOOST_STATUS register. (Default from OTP memory)
2	BOOST_PGR_MASK	R/W	0h	Masking of powergood valid detection for Boost power good interrupt BOOST_PG_INT in INT_BOOST register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BOOST_PG_STAT status bit in BOOST_STATUS register. (Default from OTP memory)
1	RESERVED	R/W	0h	
0	BOOST_ILIM_MASK	R/W	0h	Masking for Boost current monitoring interrupt BOOST_ILIM_INT in INT_BOOST register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BOOST_ILIM_STAT status bit in BOOST_STATUS register. (Default from OTP memory)

8.6.1.1.46 DIAG_MASK Register (Offset = 2Dh) [reset = 0h]

DIAG_MASK is shown in 図 8-64 and described in 表 8-56.

Return to 表 8-9.

図 8-64. DIAG_MASK Register

7	6	5	4	3	2	1	0
RESERVED		VMON2_PGF_MASK	VMON2_PGR_MASK	VMON1_PGF_MASK	VMON1_PGR_MASK	VANA_PGF_MASK	VANA_PGR_MASK
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-56. DIAG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	VMON2_PGF_MASK	R/W	0h	Masking of VMON2 invalid detection for powergood interrupt VMON2_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VMON2_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)

表 8-56. DIAG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	VMON2_PGR_MASK	R/W	0h	Masking of VMON2 valid detection for powergood interrupt VMON2_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VMON2_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)
3	VMON1_PGF_MASK	R/W	0h	Masking of VMON1 invalid detection for powergood interrupt VMON1_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VMON1_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)
2	VMON1_PGR_MASK	R/W	0h	Masking of VMON1 valid detection for powergood interrupt VMON1_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VMON1_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)
1	VANA_PGF_MASK	R/W	0h	Masking of VANA invalid detection for powergood interrupt VANA_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VANA_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)
0	VANA_PGR_MASK	R/W	0h	Masking of VANA valid detection for powergood interrupt VANA_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VANA_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)

8.6.1.1.47 SEL_I_LOAD Register (Offset = 2Eh) [reset = 0h]

SEL_I_LOAD is shown in 図 8-65 and described in 表 8-57.

Return to 表 8-9.

図 8-65. SEL_I_LOAD Register

7	6	5	4	3	2	1	0
RESERVED						LOAD_CURRENT_BUCK_SELECT	
R/W-0h						R/W-0h	

表 8-57. SEL_I_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	LOAD_CURRENT_BUCK_SELECT	R/W	0h	Start the current measurement on the selected Buck converter: 0 – BUCK0 1 – BUCK1 2 – BUCK0 3 – BUCK1 The measurement is started when register is written.

8.6.1.1.48 I_LOAD_2 Register (Offset = 2Fh) [reset = 0h]

I_LOAD_2 is shown in 図 8-66 and described in 表 8-58.

Return to 表 8-9.

図 8-66. I_LOAD_2 Register

7	6	5	4	3	2	1	0
RESERVED							BUCK_LOAD_CURRENT_8
R-0h							R-0h

表 8-58. I_LOAD_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	BUCK_LOAD_CURRENT_8	R	0h	This register describes the MSB bit of the average load current on selected converter with a resolution of 20 mA per LSB and maximum 10 A current.

8.6.1.1.49 I_LOAD_1 Register (Offset = 30h) [reset = 0h]

I_LOAD_1 is shown in 図 8-67 and described in 表 8-59.

Return to 表 8-9.

図 8-67. I_LOAD_1 Register

7	6	5	4	3	2	1	0
BUCK_LOAD_CURRENT_7_0							
R-0h							

表 8-59. I_LOAD_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK_LOAD_CURRENT_7_0	R	0h	This register describes 8 LSB bits of the average load current on selected converter with a resolution of 20 mA per LSB and maximum 10 A current.

8.6.1.1.50 FREQ_SEL Register (Offset = 31h) [reset = 0h]

FREQ_SEL is shown in 図 8-68 and described in 表 8-60.

Return to 表 8-9.

図 8-68. FREQ_SEL Register

7	6	5	4	3	2	1	0
RESERVED					BOOST_FREQ_SEL	BUCK_FREQ_SEL	
R/W-0h					R-0h	R-0h	

表 8-60. FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	BOOST_FREQ_SEL	R	0h	Boost switching frequency: 0 – 2 MHz 1 – 4 MHz (Default from OTP memory)

表 8-60. FREQ_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	BUCK_FREQ_SEL	R	0h	Buck0 and Buck1 switching frequency: 0x0 – 2 MHz 0x1 – 3 MHz 0x2 – 4 MHz 0x3 – 4 MHz (Default from OTP memory)

8.6.1.1.51 BOOST_ILIM_CTRL Register (Offset = 32h) [reset = 0h]

BOOST_ILIM_CTRL is shown in 図 8-69 and described in 表 8-61.

Return to 表 8-9.

図 8-69. BOOST_ILIM_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						BOOST_ILIM	
R/W-0h						R/W-0h	

表 8-61. BOOST_ILIM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	BOOST_ILIM	R/W	0h	Sets the current limit of Boost. 00 – 1.0 A 01 – 1.4 A 10 – 1.9 A 11 – 2.8 A (Default from OTP memory)

8.6.1.1.52 ECC_STATUS Register (Offset = 33h) [reset = 0h]

ECC_STATUS is shown in 図 8-70 and described in 表 8-62.

Return to 表 8-9.

図 8-70. ECC_STATUS Register

7	6	5	4	3	2	1	0
RESERVED						DED	SED
R-0h						R-0h	R-0h

表 8-62. ECC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	DED	R	0h	OTP error correction status: 0 – No dual errors detected 1 – Dual errors detected and not corrected
0	SED	R	0h	OTP error correction status: 0 – No single errors detected 1 – Single errors detected and corrected

8.6.1.1.53 WD_DIS_CTRL_CODE Register (Offset = 34h) [reset = 0h]

WD_DIS_CTRL_CODE is shown in 図 8-71 and described in 表 8-63.

Return to 表 8-9.

図 8-71. WD_DIS_CTRL_CODE Register

7	6	5	4	3	2	1	0
WD_DIS_UNLOCK_CODE							
R-0h							

表 8-63. WD_DIS_CTRL_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_DIS_UNLOCK_CODE	R	0h	Unlocking WD_DIS_CTRL bit: Set WD_DIS_CTRL_LOCK=0 by writing 0x87, 0x65, 0x1B by 3 consecutive I2C write sequences to WD_DIS_CTRL_CODE register. Locking WD_DIS_CTRL bit: Set WD_DIS_CTRL_LOCK=1 by writing anything to WD_DIS_CTRL_CODE register or write WD_LOCK=1. Reading this address returns always 0x00. WD_DIS_CTRL can be unlocked only if WD_LOCK=0.

8.6.1.1.54 WD_DIS_CONTROL Register (Offset = 35h) [reset = 0h]

WD_DIS_CONTROL is shown in 図 8-72 and described in 表 8-64.

Return to 表 8-9.

図 8-72. WD_DIS_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED						WD_DIS_CTRL_LOCK	WD_DIS_CTRL
R/W-0h						R-1h	R/W-0h

表 8-64. WD_DIS_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	WD_DIS_CTRL_LOCK	R	1h	Lock status for WD_DIS_CTRL bit. 0 – Not locked, WD_DIS_CTRL bit can be written. 1 – Locked, WD_DIS_CTRL bit is locked and cannot be changed. Lock can be opened by writing 0x87, 0x65, 0x1B by 3 consecutive I2C write sequences to WD_DIS_CTRL_CODE register if WD_LOCK=0. Lock can be closed by writing anything to WD_DIS_CTRL_CODE register or writing WD_LOCK=1.
0	WD_DIS_CTRL	R/W	0h	Watchdog disable pin control. 0 – Watchdog cannot be disabled by WD_DIS pin. 1 – Watchdog can be disabled by WD_DIS pin. (Default from OTP memory) This bit can be written 1 only if WD_LOCK=0 and WD_DIS_CTRL_LOCK=0.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LP87702-Q1 is a power-management unit including a boost converter, two step-down converters, and three general-purpose digital output signals.

9.2 Typical Application

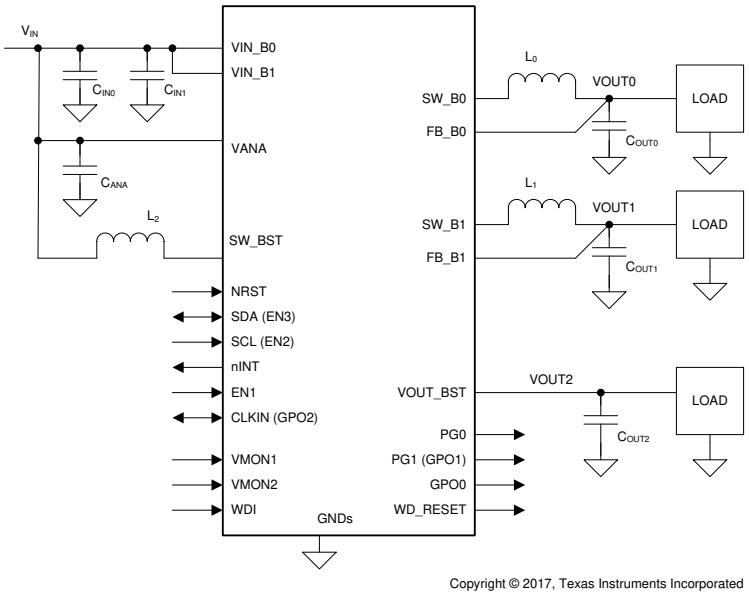


図 9-1. LP87702-Q1 Typical Application

9.2.1 Design Requirements

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Output voltages	1.8 V, 1.24 V, 5 V
Switching frequency	4 MHz

9.2.2 Detailed Design Procedure

The performance of the LP87702-Q1 device depends greatly on the care taken in designing the printed circuit board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from the system power rail while turning on the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can easily become the performance limiting items. The separate buck converter power pins VIN_Bx are not connected together internally. The VIN_Bx power connections shall be connected together outside the package using a power plane construction.

9.2.2.1 Application Components

9.2.2.1.1 Inductor Selection

セクション 9.2 shows the inductors L_0, L_1, and L_2. The inductor's inductance and DCR affects the buck and boost converter's control loop. 表 9-2 lists the recommended inductors, or similar ones, that should be used. Pay attention to the inductor's saturation current and temperature rise current. Check that the saturation current is higher than the peak current limit and the temperature rise current is higher than the maximum expected rms output current. セクション 7 shows the minimum effective inductance that ensures good performance. The inductor's DC resistance should be less than 0.05 Ω for good efficiency at high-current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Shielded inductors are preferred as they radiate less noise.

表 9-2. Recommended Inductors for Buck Converters

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS L × W x× H (mm)	RATED DC CURRENT, I_{SAT} max / I_{TEMP} max (A)	DCR typ / max (mΩ)
MURATA	DFE252012PD-R47M	0.47 µH (20%)	2.5 × 2 × 1.2	5.2 / 4.0(1)	- / 27
TDK	TFM252012ALMAR47MTAA	0.47 µH (20%)	2.5 × 2 × 1.2	5.8 / 4.9(1)	19 / 24

(1) Operating temperature range is up to 125°C including self temperature rise.

表 9-3. Recommended Inductor for Boost Converters

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS L × W x× H (mm)	RATED DC CURRENT, I_{SAT} max / I_{TEMP} max (A)	DCR typ / max (mΩ)
MURATA	DFE252012PD-1R0M	1 µH (20%)	2.5 × 2 × 1.2	3.8 / 3.2 (1)	- / 42
TDK	TFM25201ALMA1R0MTAA	1 µH (20%)	2.5 × 2 × 1.2	4.2 / 3.7 (1)	35 / 42

9.2.2.1.2 Buck Input Capacitor Selection

セクション 9.2 shows the input capacitors C_{IN0} and C_{IN1}. A ceramic input bypass capacitor of 10 µF is required for both converters. Place the input capacitor as close as possible to the device's VIN_Bx pin and PGND_Bx pin. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. The capacitor's DC bias characteristics must also be considered. Minimum effective input capacitance to ensure good performance is 1.9 µF per buck input at the maximum input voltage including tolerances and ambient temperature range. In addition, 表 9-4 shows how there must be at least 22 µF of additional capacitance common for all the power input pins on the system power rail.

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces the voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. In addition, ferrite can be used in front of the input capacitor to reduce the EMI.

表 9-4. Recommended Buck Input Capacitors (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM21BR71A106KE22	10 µF (10%)	0805	2 × 1.25 × 1.25	10 V
TDK	CGA4J3X7S1A106K125AB	10 µF (10%)	0805	2 × 1.25 × 1.25	10 V

9.2.2.1.3 Buck Output Capacitor Selection

セクション 9.2 shows the output capacitor C_{OUT0} and C_{OUT1}. A ceramic local output capacitor of 22 µF is required for both outputs. Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out the current flow from the inductor to the load, whic helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance for good performance is 15 µF for each buck, including the DC voltage roll-off, tolerances, aging, and temperature effects.

The output voltage ripple is caused by charging and discharging the output capacitor, and is also due to its R_{ESR}. 表 9-5 shows how the R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the part's switching frequency.

POL capacitors can be used to improve load transient performance and to decrease the ripple voltage. A higher output capacitance improves the load step behavior, reduces the output voltage ripple, and decreases the PFM switching frequency. Note: the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (100-µF range) output capacitors. The output voltage might be slower than the programmed ramp rate at voltage transitions for large output capacitors, because of the higher energy stored on the output capacitance. Also, the time required to charge the output capacitor to target value might be longer at start-up. The output voltage is discharged to 0.6 V level using forced-PWM operation at shutdown. This can increase the input voltage if the load current is small and the output capacitor is large compared to the input capacitor. The output capacitor is discharged by the internal discharge resistor when below the 0.6 V level, and more time is required to settle VOUT down with a large capacitor because of the increased time constant.

表 9-5. Recommended Buck Output Capacitors (X7R or X7T Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM31CR71A226KE02	22 µF (10%)	1206	3.2 × 1.6 × 1.6	10 V
TDK	CGA5L1X7S1A226M160AC	22 µF (20%)	1206	3.2 × 1.6 × 1.6	10 V

9.2.2.1.4 Boost Input Capacitor Selection

A ceramic input capacitor of 10 µF is sufficient for most applications. Place the input capacitor close to the SW_BST pin of the device. Use X7R types, do not use Y5V or F. See 表 9-6.

表 9-6. Recommended Boost Input Capacitors (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L×W×H (mm)	VOLTAGE RATING
Murata	GCM21BR71A106KE22	10 µF (10%)	0805	2.0 × 1.25 × 1.25	10 V

9.2.2.1.5 Boost Output Capacitor Selection

Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. Place the output capacitor as close as possible to the device's VOUT_BST pin and PGND_BST pin. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to support load transients. See 表 9-7.

表 9-7. Recommended Boost Output Capacitors (X7R or X7T Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L×W×H (mm)	VOLTAGE RATING
Murata	GCM31CR71A226KE02	22 µF (10%)	1206	3.2 × 1.6 × 1.6	10 V

9.2.2.1.6 Supply Filtering Components

The VANA input is used to supply analog and digital circuits in the device. See 表 9-8 recommended components from for VANA input supply filtering.

表 9-8. Recommended Supply Filtering Components

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L×W×H (mm)	VOLTAGE RATING
Murata	GCM188R71C104KA37D	100 nF (10%)	0603	1.6 × 0.8 × 0.8	16 V
Murata	GCM155R71C104KA55D	100 nF (10%)	0402	1.0 × 0.5 × 0.5	16 V

9.2.3 Current Limit vs Maximum Output Current

The current limit must be set high enough to account for the inductor ripple current on top of the maximum output current for the buck converters and boost. The forward current limit for the buck converters is set by BUCK0_ILIM, BUCK1_ILIM and for boost it is set by BOOST_ILIM.

For the buck converter the inductor current ripple can be calculated using 式 1 and 式 2:

$$D = \frac{V_{OUT}}{V_{IN(max)} \times \eta} \quad (1)$$

$$\Delta I_L = \frac{(V_{IN(max)} - V_{OUT}) \times D}{f_{SW} \times L} \quad (2)$$

Example using 式 1 and 式 2:

$V_{IN(max)}$ = 5.5 V
V_{OUT} = 1 V
η = 0.75
f_{SW} = 1.8 MHz
L = 0.38 µH
then D = 0.242 and ΔI_L = 1.59 A

Peak current is half of the current ripple. If $I_{LIM\_FWD\_SET\_OTP}$ is 3 A, the minimum forward current limit would be 2.85 A when taking the –5% tolerance into account. In this case the difference between set peak current and maximum load current = 0.795 A + 0.15 A = 0.945 A.

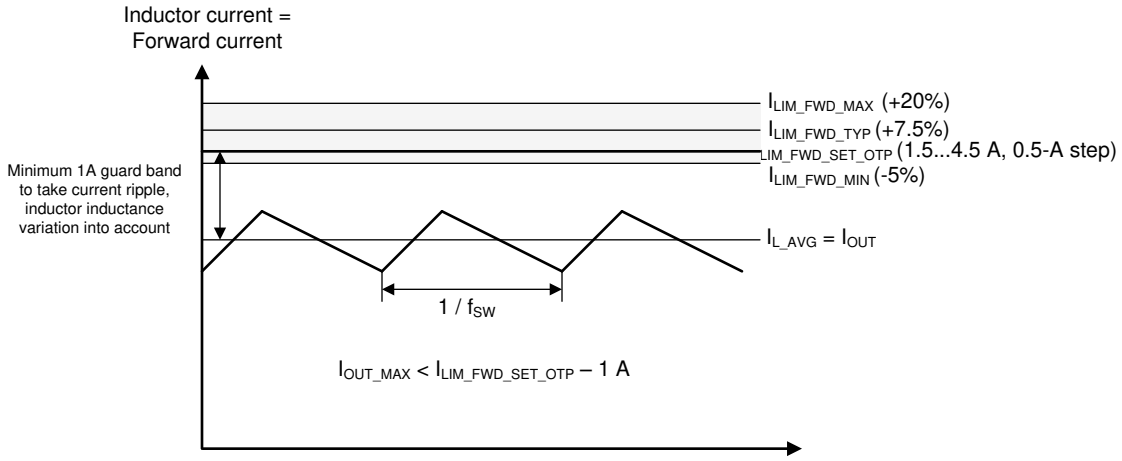


図 9-2. Current Limit vs Maximum Output Current

9.2.4 Application Curves

Unless otherwise specified: V_{IN} = 3.3 V, V_{OUT_BUCK} = 1 V, V_{OUT_BOOST} = 5 V, T_A = 25°C, f_{SW}-setting 4 MHz, L0 = L1 = 0.47 µH (TOKO DFE252012PD-R47M), L2 = 1 µH (TFM252012ALMA1R0), C_{OUT_BUCK}, C_{POL_BUCK}, and C_{OUT_BOOST} = 22 µF. Measurements are done using connections in 図 9-1.

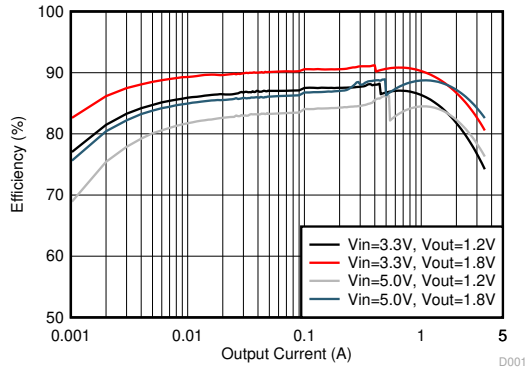
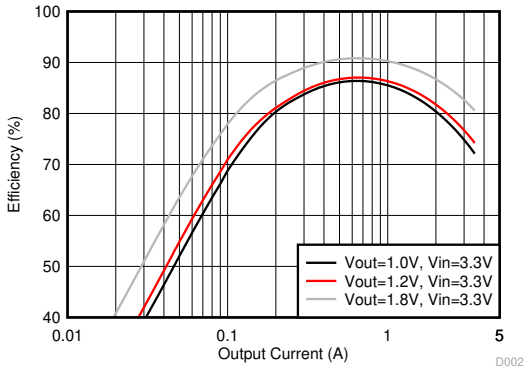
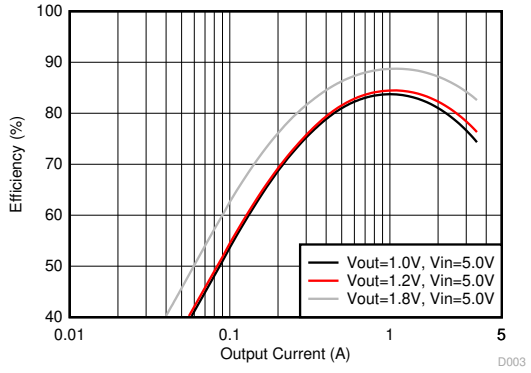


図 9-3. Buck Efficiency in AUTO (PFM/PWM) Mode



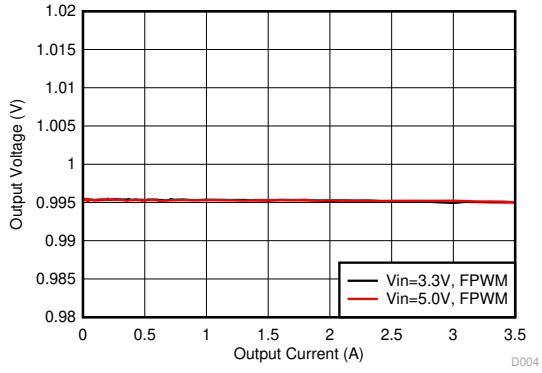
V_{IN} = 3.3 V

図 9-4. Buck Efficiency in Forced PWM Mode



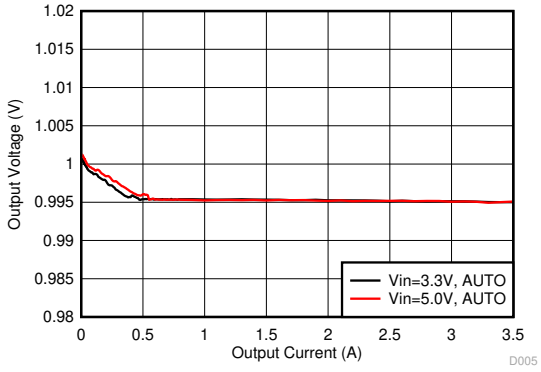
V_{IN} = 5 V

図 9-5. Buck Efficiency in Forced PWM Mode



V_{OUT} = 1 V

図 9-6. Buck Output Voltage vs Load Current in Forced PWM Mode



V_{OUT} = 1 V

図 9-7. Buck Output Voltage vs Load Current in AUTO Mode

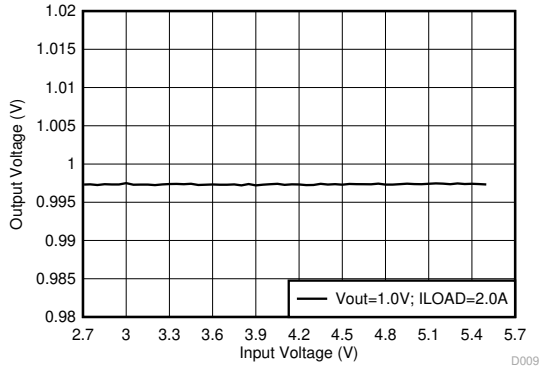


図 9-8. Buck Output Voltage vs Input Voltage in PWM Mode

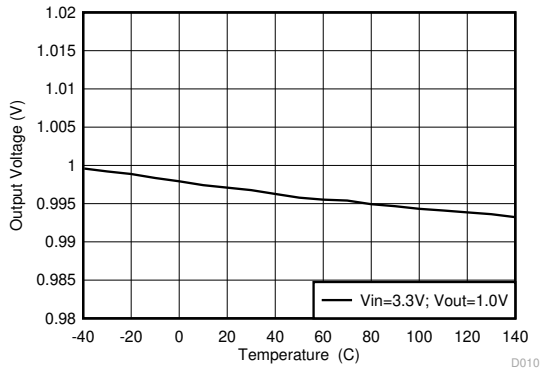
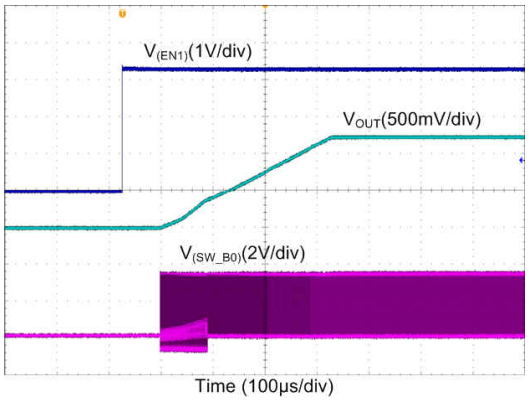
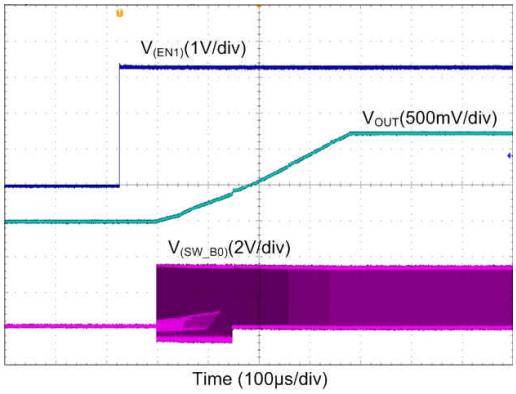


図 9-9. Buck Output Voltage vs Temperature



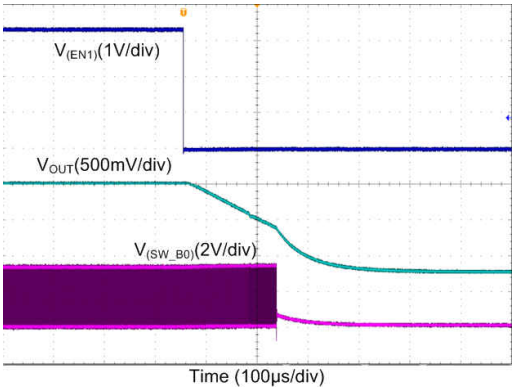
I_{OUT} = 0 A

図 9-10. Buck Start-up with EN1, Forced-PWM



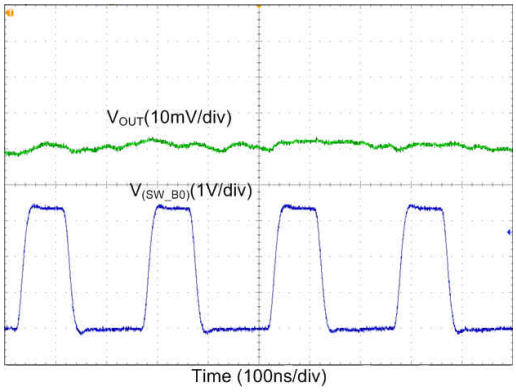
R_{LOAD} = 1 Ω

図 9-11. Buck Start-up with EN1, Forced-PWM



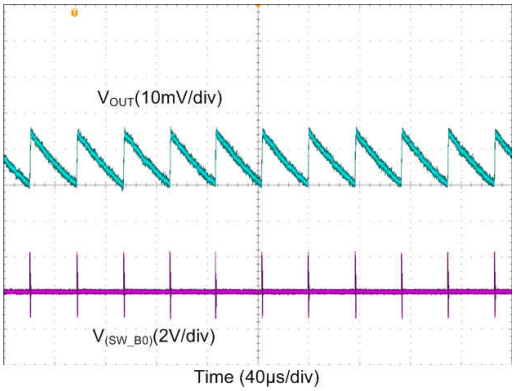
R_{LOAD} = 1 Ω

図 9-12. Buck Shutdown with EN1, Forced-PWM



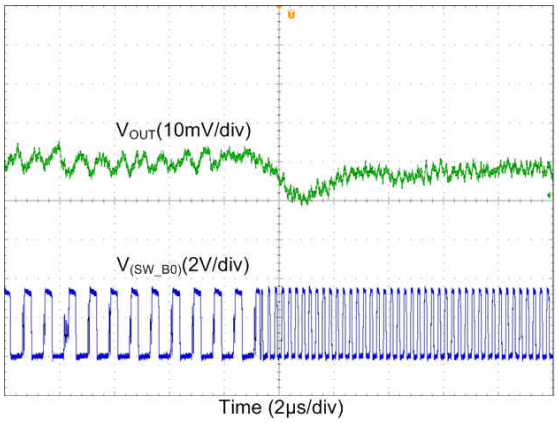
V_{OUT} = 1.2 V I_{OUT} = 500 mA

図 9-13. Buck Output Voltage Ripple, Forced-PWM Mode



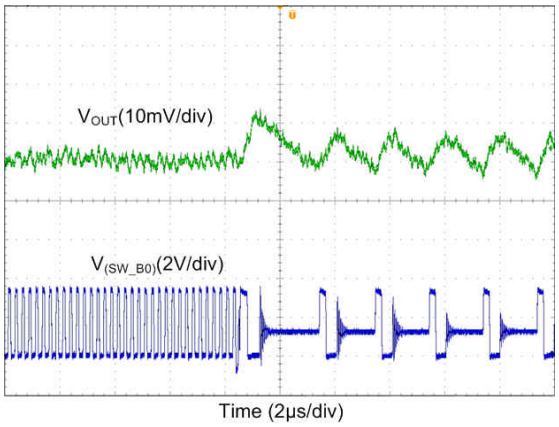
V_{OUT} = 1.2 V I_{OUT} = 10 mA

図 9-14. Buck Output Voltage Ripple, PFM Mode



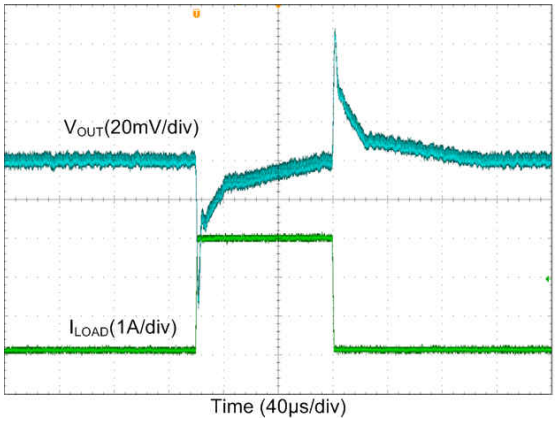
V_{OUT} = 1.2 V

図 9-15. Buck Transient from PFM-to-PWM Mode



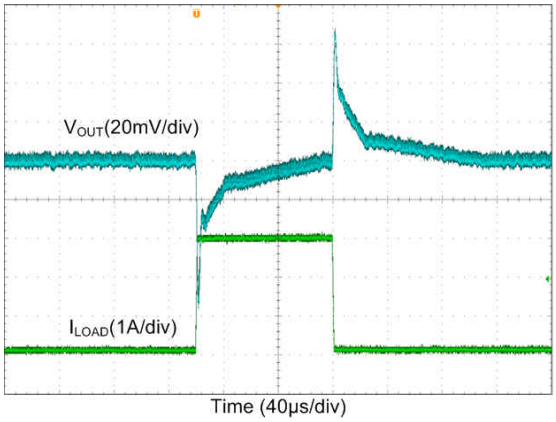
V_{OUT} = 1.2 V

図 9-16. Buck Transient from PWM-to-PFM Mode



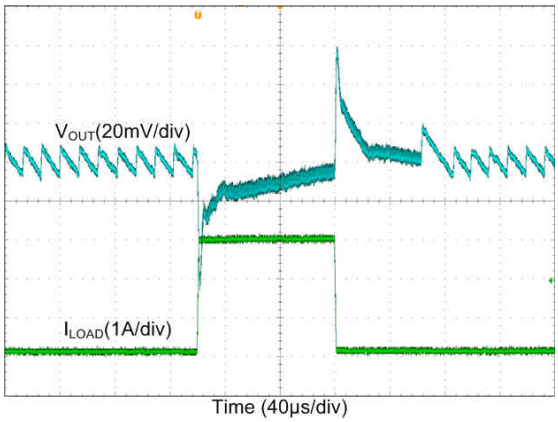
I_{OUT} = 0 A → 3 A → 0 A $T_R = T_F$ = 1 µs V_{OUT} = 1 V

図 9-17. Buck Transient Load Step Response, Forced-PWM Mode



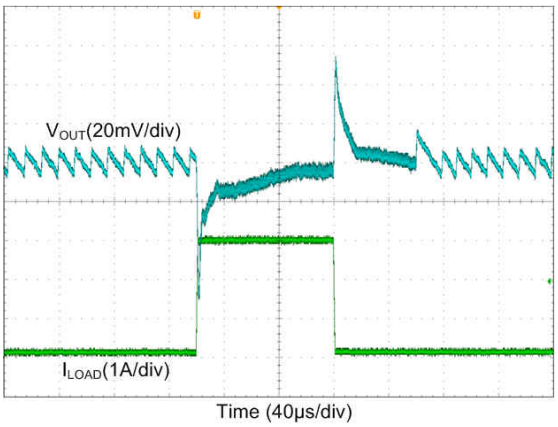
I_{OUT} = 0 A → 3 A → 0 A $T_R = T_F$ = 1 µs V_{OUT} = 1.2 V

図 9-18. Buck Transient Load Step Response, Forced-PWM Mode



I_{OUT} = 0 A → 3 A → 0 A $T_R = T_F$ = 1 µs V_{OUT} = 1 V

図 9-19. Buck Transient Load Step Response, Auto Mode



V_{OUT} = 1.2 V

図 9-20. Buck Transient Load Step Response, Auto Mode

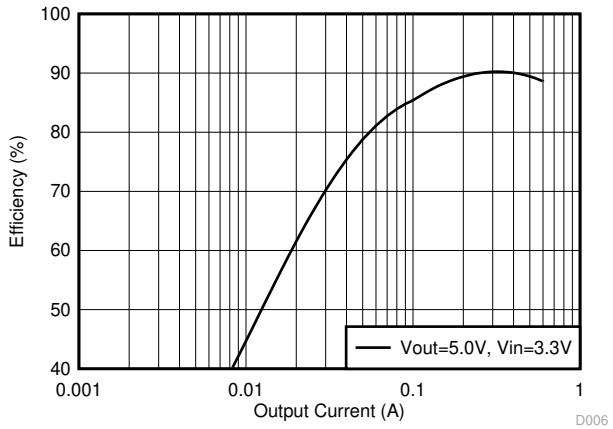


図 9-21. Boost Efficiency

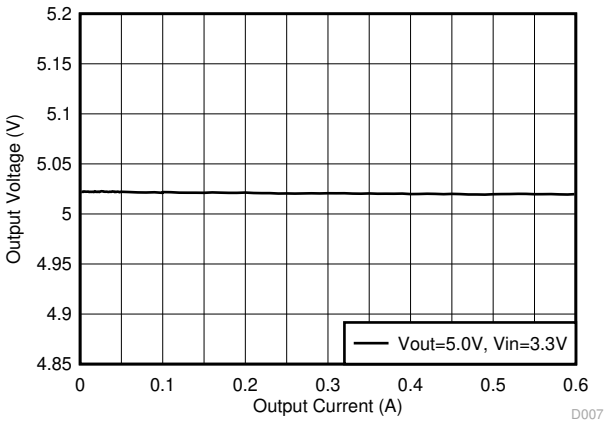
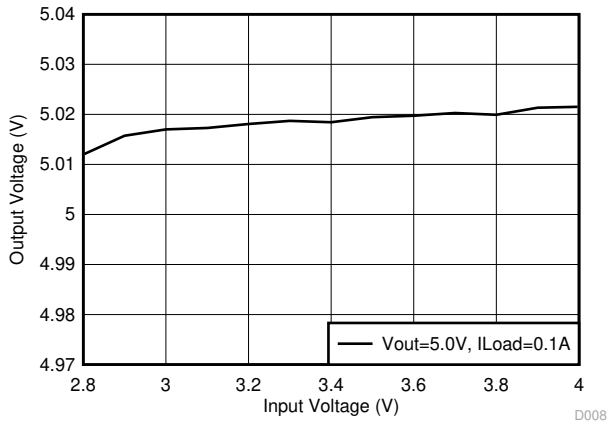
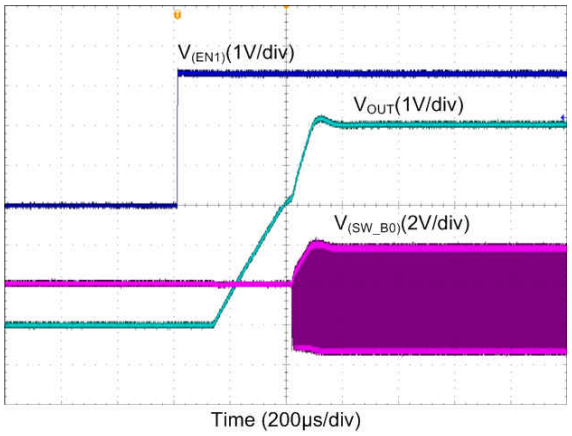


図 9-22. Boost Output Voltage vs Load Current



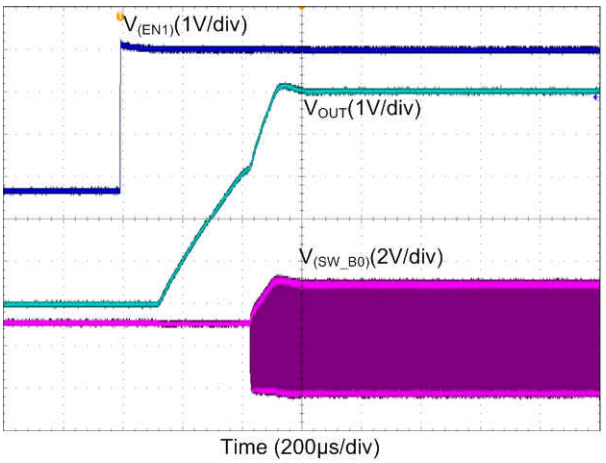
I_{OUT} = 0.1 A

図 9-23. Boost Output Voltage vs Input Voltage



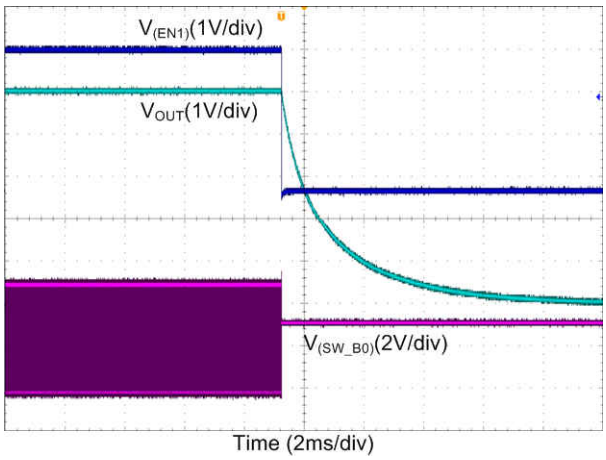
I_{OUT} = 0 A

図 9-24. Boost Start-up With EN1, Forced-PWM



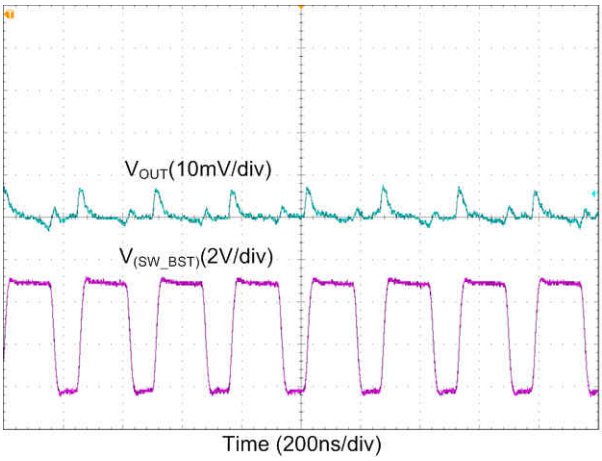
R_{LOAD} = 50 Ω

図 9-25. Boost Start-up With EN1, Forced-PWM



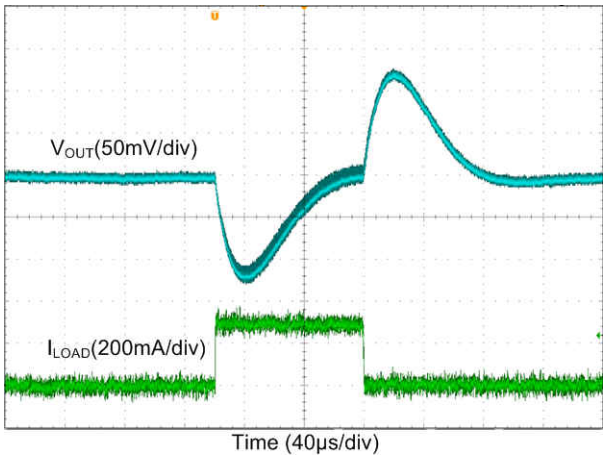
R_{LOAD} = 50 Ω

図 9-26. Boost Shutdown With EN1, Forced-PWM



I_{OUT} = 0.1 A

図 9-27. Boost Output Voltage Ripple



I_{OUT} = 0 A → 0.25 A → 0 A $T_R = T_F$ = 1 µs

図 9-28. Boost Transient Load Step Response

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.8 V and 5.5 V. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high of a drop in the LP87702-Q1 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP87702-Q1, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

The high frequency and large switching currents of the LP87702-Q1 make the choice of layout important. Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to several amps, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place C_{IN} as close as possible to the VIN_Bx pin and the PGND_Bx pin. Route the V_{IN} trace wide and thick to avoid IR drops. The trace between the input capacitor's positive node and one or more of the device VIN_Bx pins, as well as the trace between the negative node of the input capacitor and one or more of the power PGND_Bx pins must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor – parasitic inductance on these traces must be kept as tiny as possible for proper device operation.
2. The output filter, consisting of L and C_{OUT}, converts the switching signal at SW_Bx to the noiseless output voltage. It should be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the LP87702-Q1 devices output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) should be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.
4. If remote voltage sensing can be used for the load, connect the device feedback pins FB_Bx to the respective sense pins on the load capacitor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND_Bx, VIN_Bx, and SW_Bx, as well as high bandwidth signals such as the I^2C. Avoid capacitive and inductive coupling by keeping the sense lines short and direct. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane (if possible).
5. PGND_Bx, VIN_Bx and SW_Bx should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND_Bx, VIN_Bx and SW_Bx.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ($R_{\theta JA}$) and junction-to-board ($R_{\theta JB}$) thermal resistances, which reduces the device junction temperature (T_J). TI strongly recommends performing a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process, by using a thermal modeling analysis software.

11.2 Layout Example

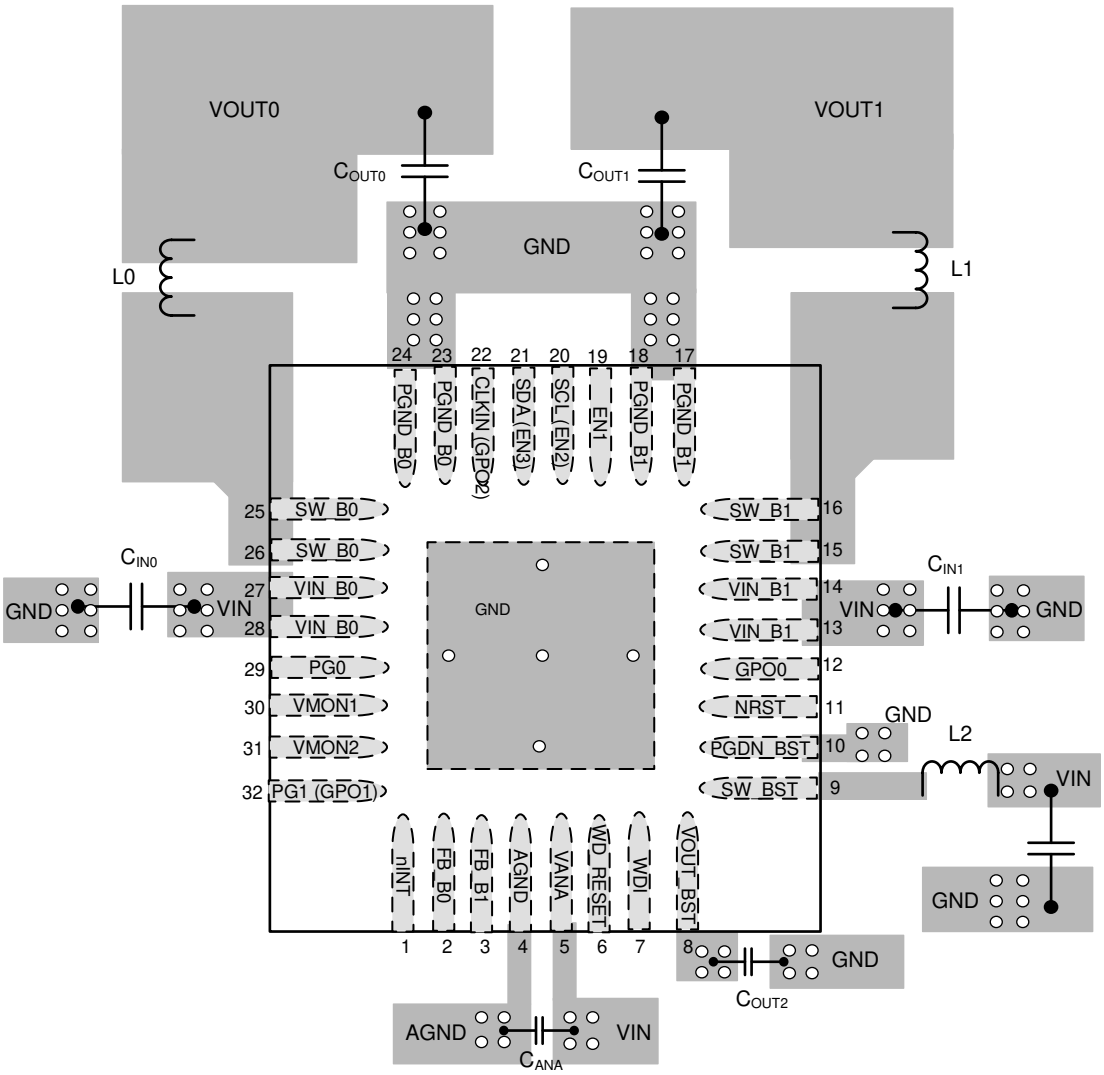


図 11-1. LP87702-Q1 Board Layout Example

12 Device and Documentation Support

12.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, go to the device product folder on ti.com. In the upper right corner, click *Alert me* to register for a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP877020RHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8770Q 20 RHB	Samples
LP877021RHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LP8770Q 21 RHB	Samples
LP87702DRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8770Q 2D RHB	Samples
LP87702DRHBTQ1	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8770Q 2D RHB	Samples
LP87702KRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8770Q 2K RHB	Samples
LP87702KRHBTQ1	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8770Q 2K RHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LP87702-Q1 :

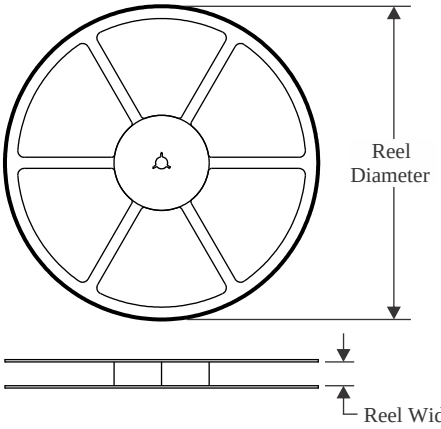
- Catalog : LP87702

NOTE: Qualified Version Definitions:

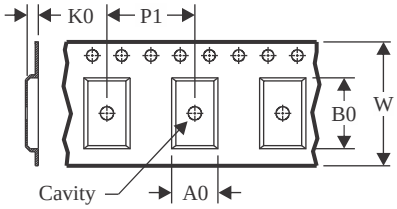
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

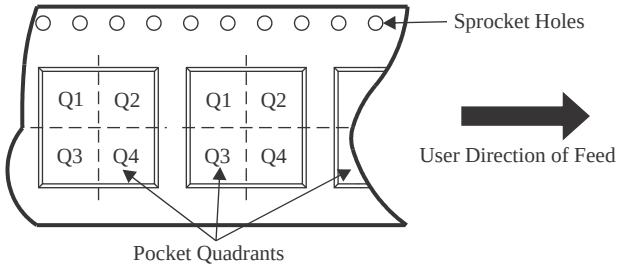


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

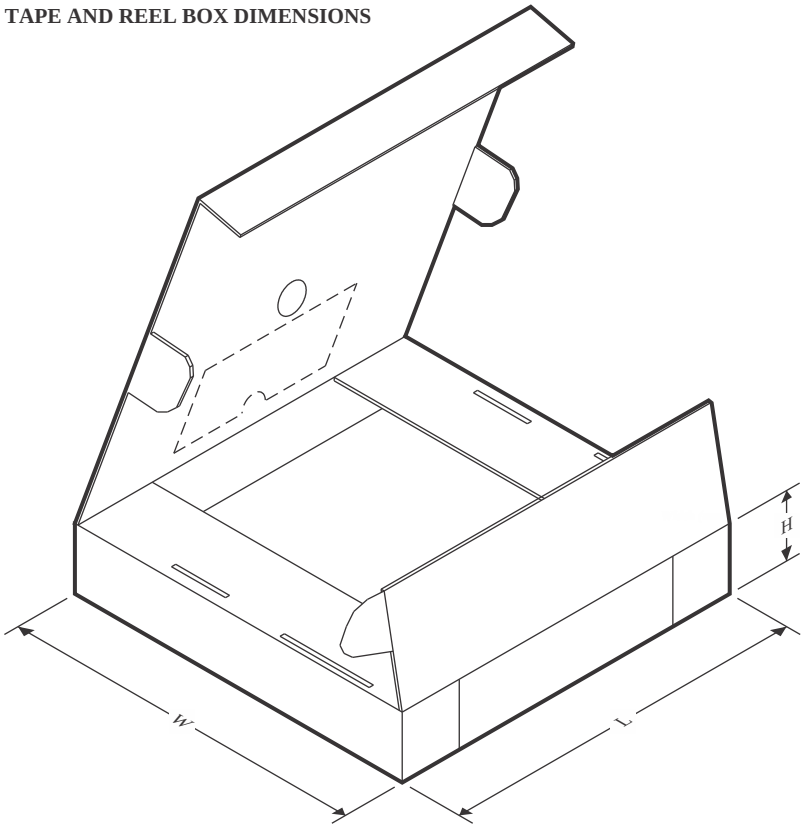
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP877020RHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LP877021RHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
LP87702DRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LP87702DRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LP87702KRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LP87702KRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP877020RHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
LP877021RHBRQ1	VQFN	RHB	32	3000	367.0	367.0	38.0
LP87702DRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
LP87702DRHBTQ1	VQFN	RHB	32	250	210.0	185.0	35.0
LP87702KRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
LP87702KRHBTQ1	VQFN	RHB	32	250	210.0	185.0	35.0

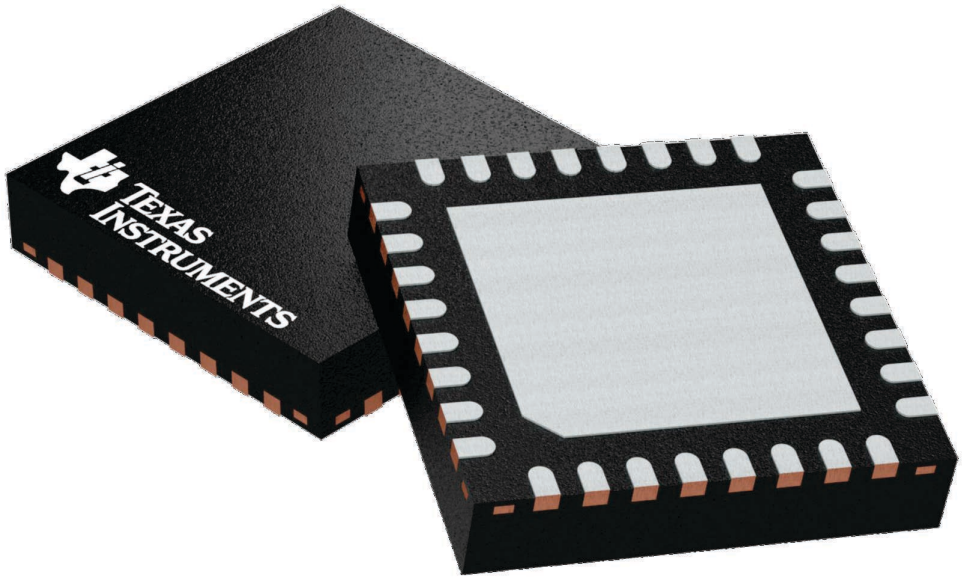
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

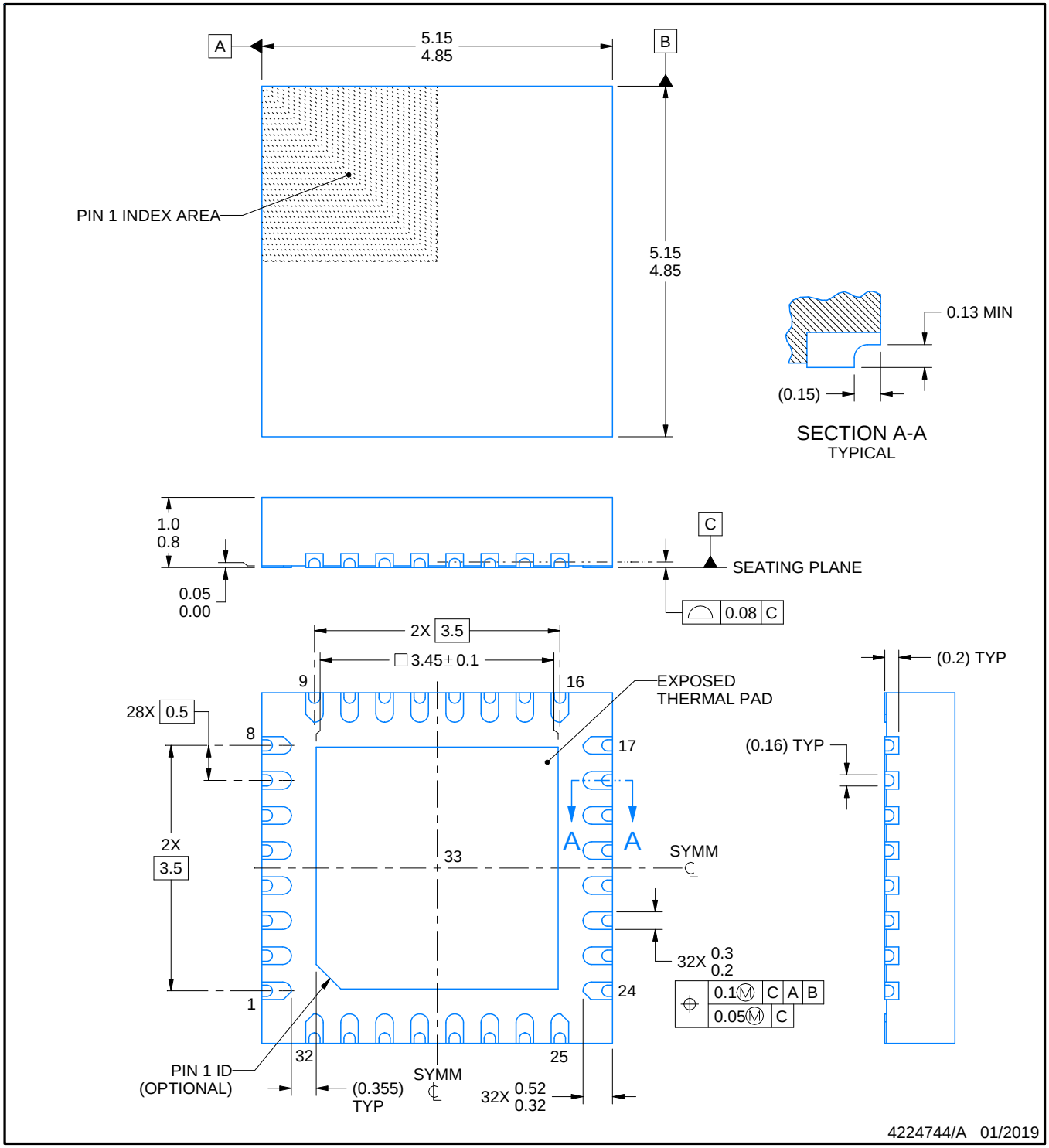
4224745/A

RHB0032T

PACKAGE OUTLINE

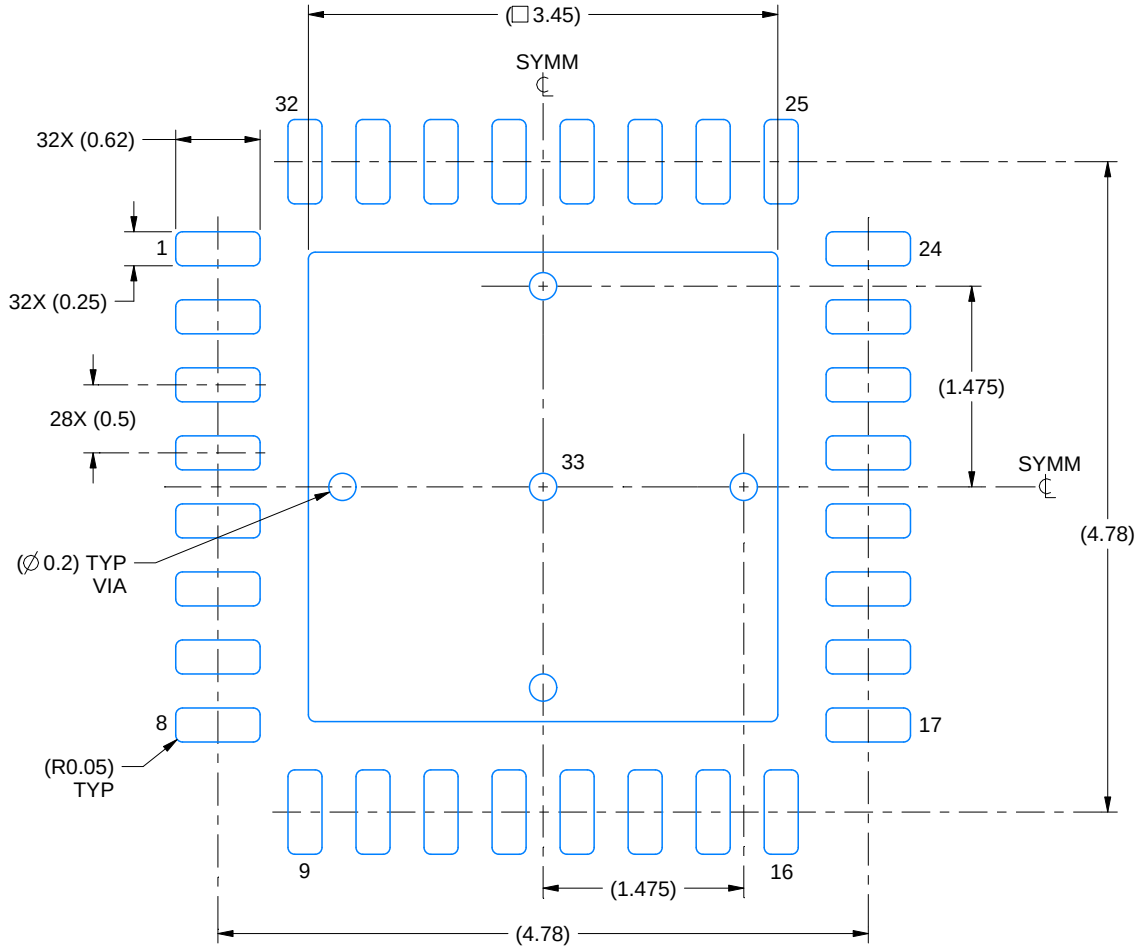
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

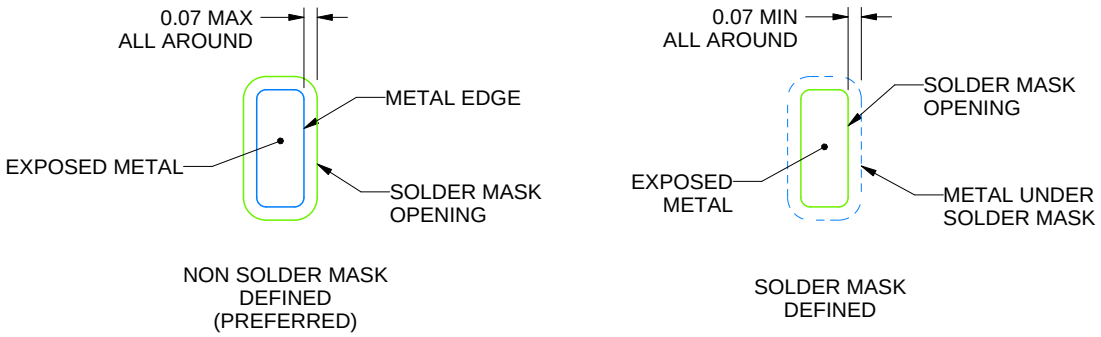
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE:18X

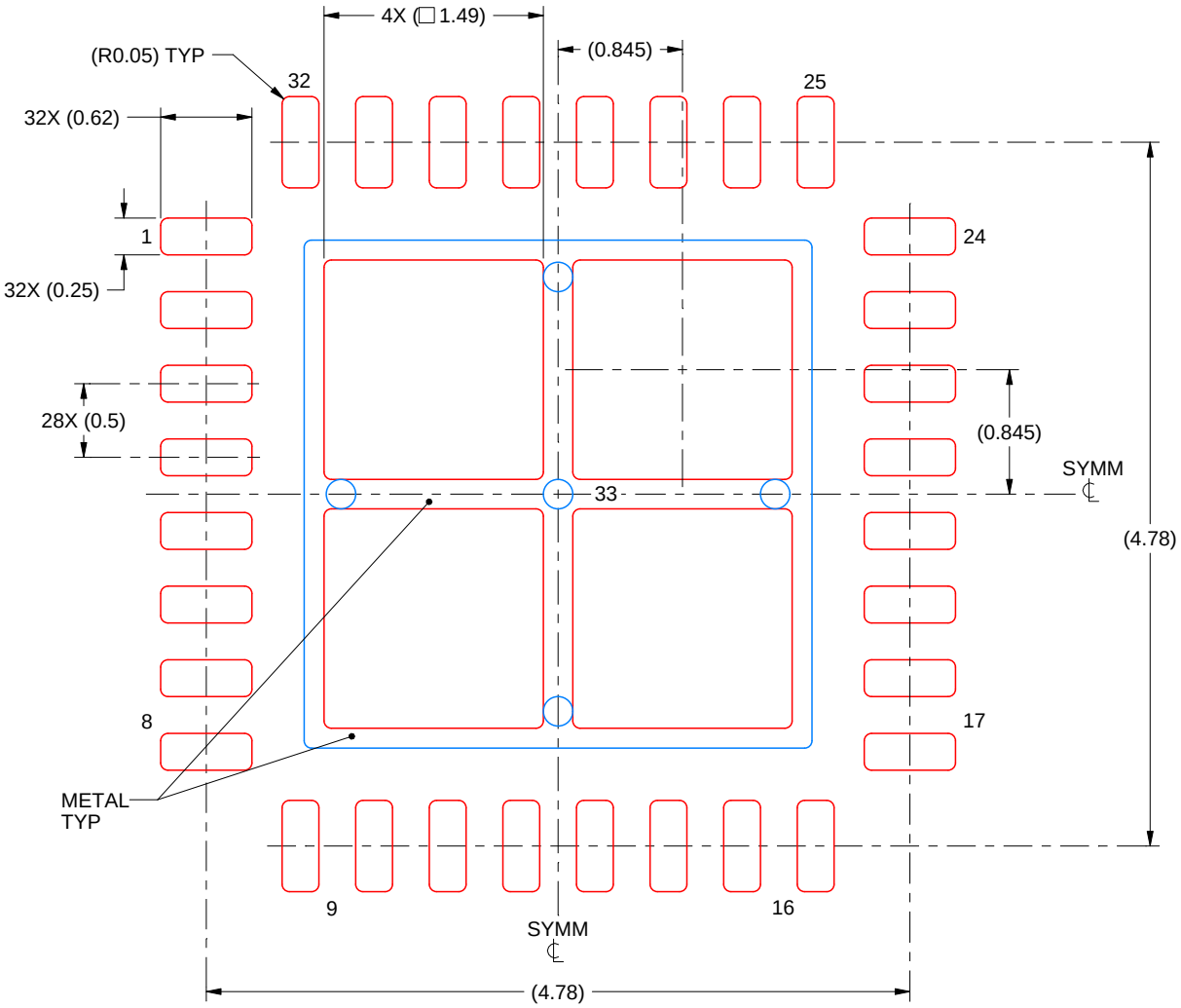


SOLDER MASK DETAILS

4224744/A 01/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4224744/A 01/2019

NOTES: (continued)

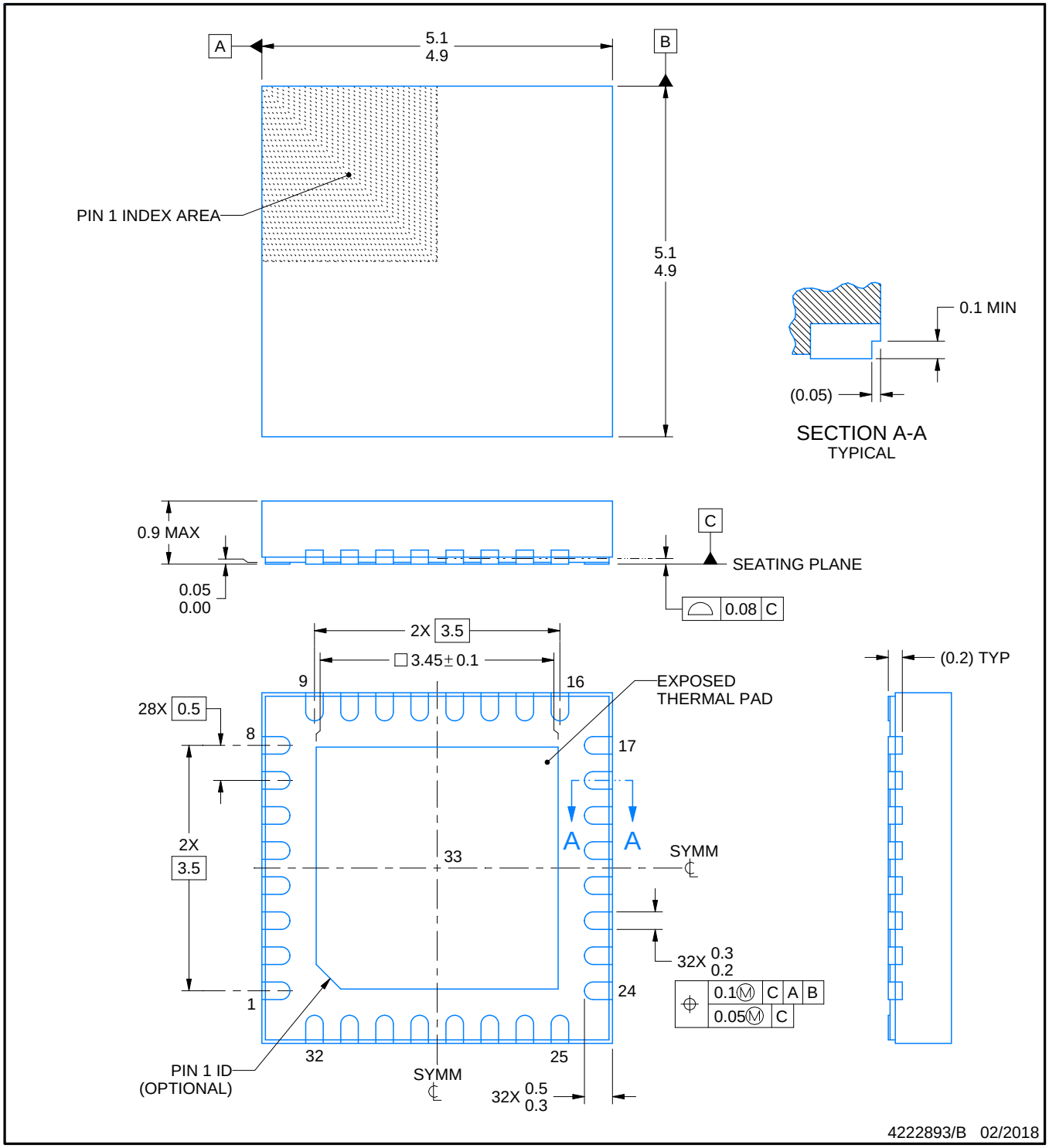
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RHB0032N

PACKAGE OUTLINE

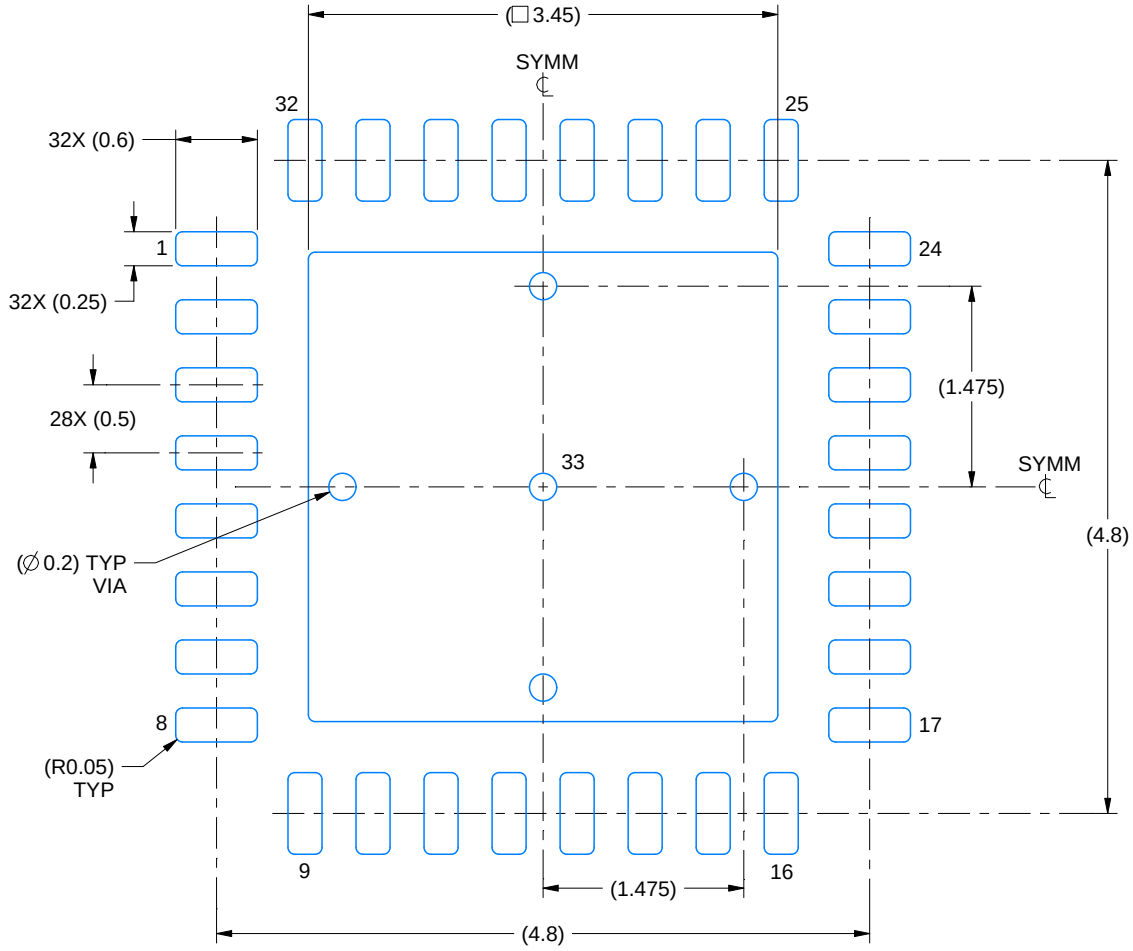
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

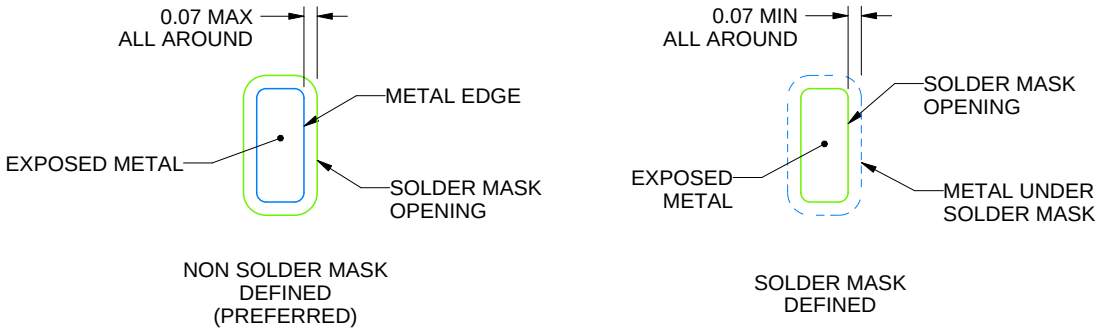


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

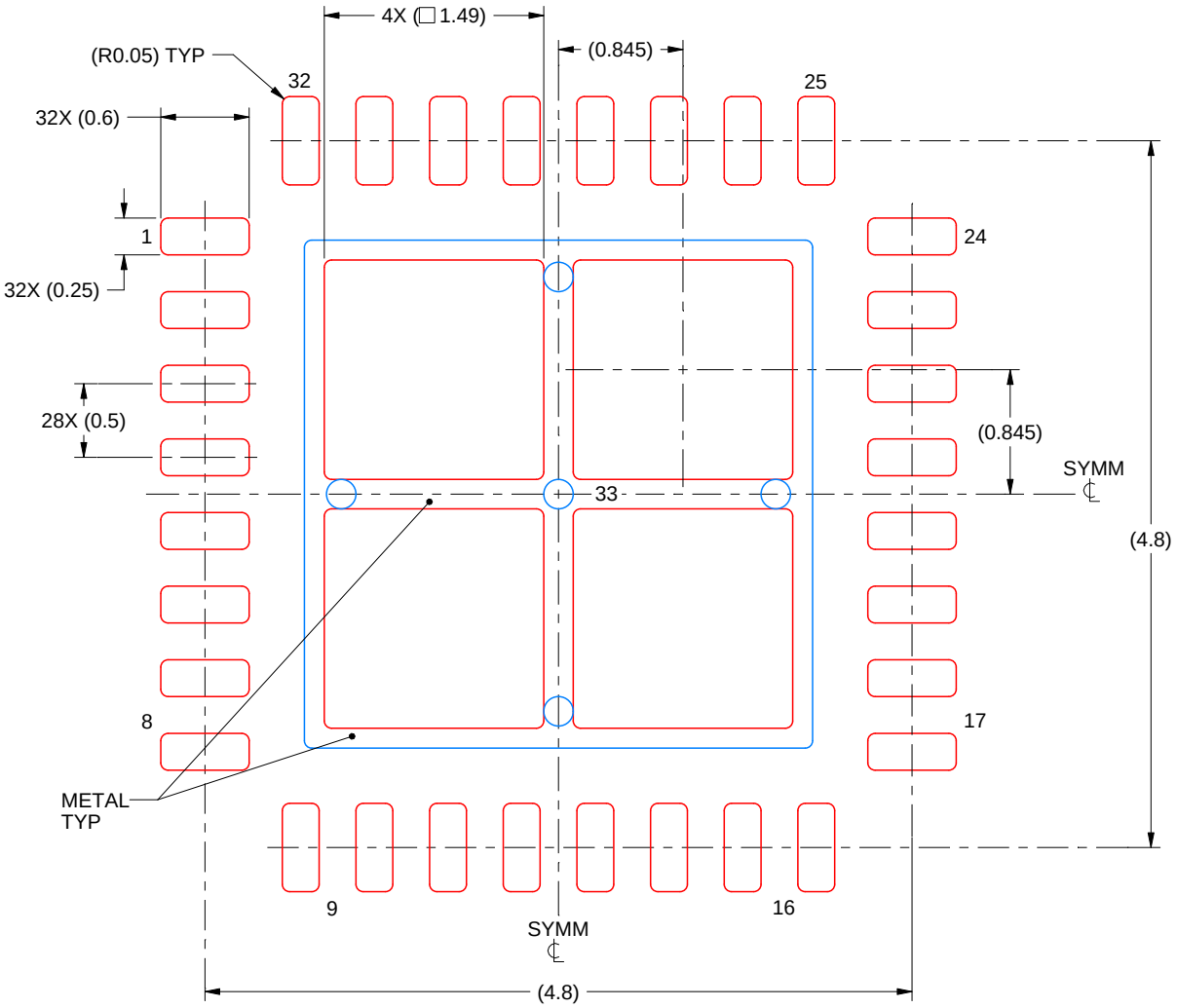


SOLDER MASK DETAILS

4222893/B 02/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222893/B 02/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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