LMX2624-SP5MHz～28GHz 広帯域 シンセサイザ、位相同期および JESD204B/C 対応

1 特長

- SMD 5962R2321001PXE
  - 総照射線量耐性：100Krad (ELDRS フリー)
  - シングル イベント ラッチアップ (SEL) 耐性：最大 75MeV-cm^2/mg
  - シングル イベント機能割り込み (SEFI) 耐性：最大 75MeV-cm^2/mg
- 広帯域周波数シンセサイザ：出力周波数：5MHz～28GHz
- 24GHz 搬送波周波数使用時に、100kHz のオフセットで -101dBc/Hz の位相ノイズ
- 24GHz でのジッタ：60fs RMS (1kHz～300MHz)
- 出力電力をプログラム可能
- 主な PLL 仕様
  - 性能指数：-236dBc/Hz
  - 正規化 1/f ノイズ：-129dBc/Hz
  - 最高 200MHz の位相検出周波数
- 複数デバイス間の出力位相の同期
- RFoutA および RFoutB 用の独立した MUTE ピンで、200ns のミュート / ミュート解除時間
- 分解能 9ps のプログラム可能な遅延による SYSREF サポート
- 3.3V 単一電源動作
- ピン モード：整数 PLL モードでピンにより構成可能な N 分周器および出力分周器
- 10×10mm² 64 リード QFP パッケージ
- 動作温度範囲：-55℃～+125℃
- PLLatinum™ シミュレータ設計ツール対応

2 アプリケーション

- Ku/Ka バンドまでの宇宙通信ペイロード
- 宇宙レーダー システム
- コマンドおよびデータの処理系
- 高速データ コンバータ クロッキング (JESD204B/C 対応)
- 28GHz までの周波数のミキサ用ローカル発振器

3 概要

LMX2624-SP は、周波数 5MHz～28GHz を出力可能な電圧制御発振器 (VCO) を内蔵した、高性能、広帯域フェーズ ロック ループ (PLL) および電圧レギュレータです。このデバイスの VCO は、1 オクターブの範囲をカバーしているため、最低 5MHz までのすべての周波数を出力できます。-236dBc/Hz という性能指数を持つ高性能 PLL と高い位相検出周波数により、帯域内ノイズと積分ジッタを非常に低く抑えることができます。

LMX2624-SP では、複数のデバイスの出力を同期できます。このため、フラクショナル エンジンまたは出力分周器を使用した場合を含めて、あらゆる使用事例でデバイスから決定性位相を取得できます。このデバイスは、SYSREF (JESD204B/C 規格に準拠) の生成および中継サポートが追加されており、高速データ コンバータ向けの低ノイズ クロック ソースとして設計されています。

このデバイスは、テキサス・インスツルメンツの高度な BiCMOS プロセスで製造され、64 リード QFP プラスチック パッケージで供給されます。

パッケージ情報

部品番号	グレード	パッケージ (1)	パッケージ サイズ (2)
LMX2624-SP	QML-P	QFP 64 ピン	10mm × 10mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

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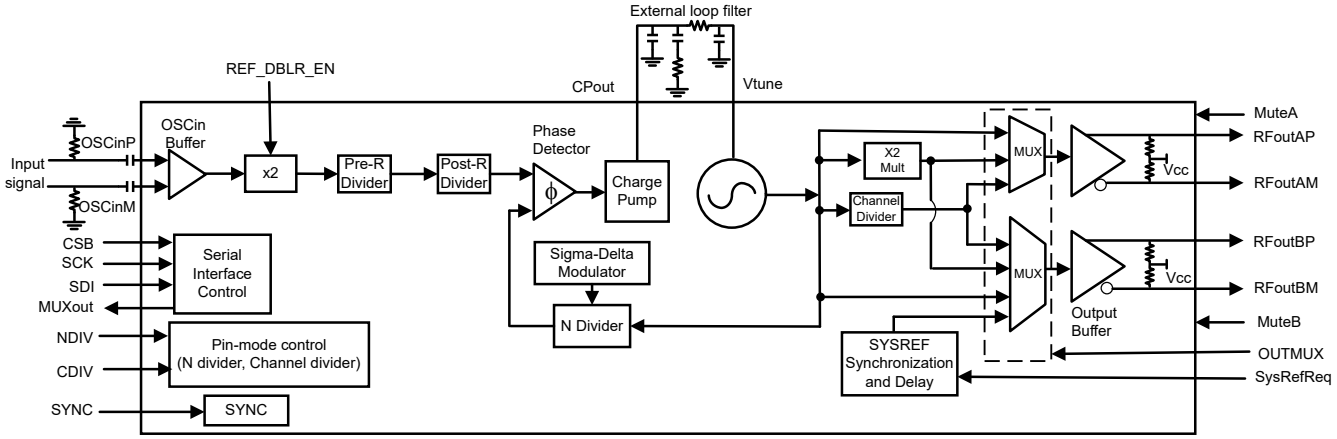

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4 Pin Configuration and Functions

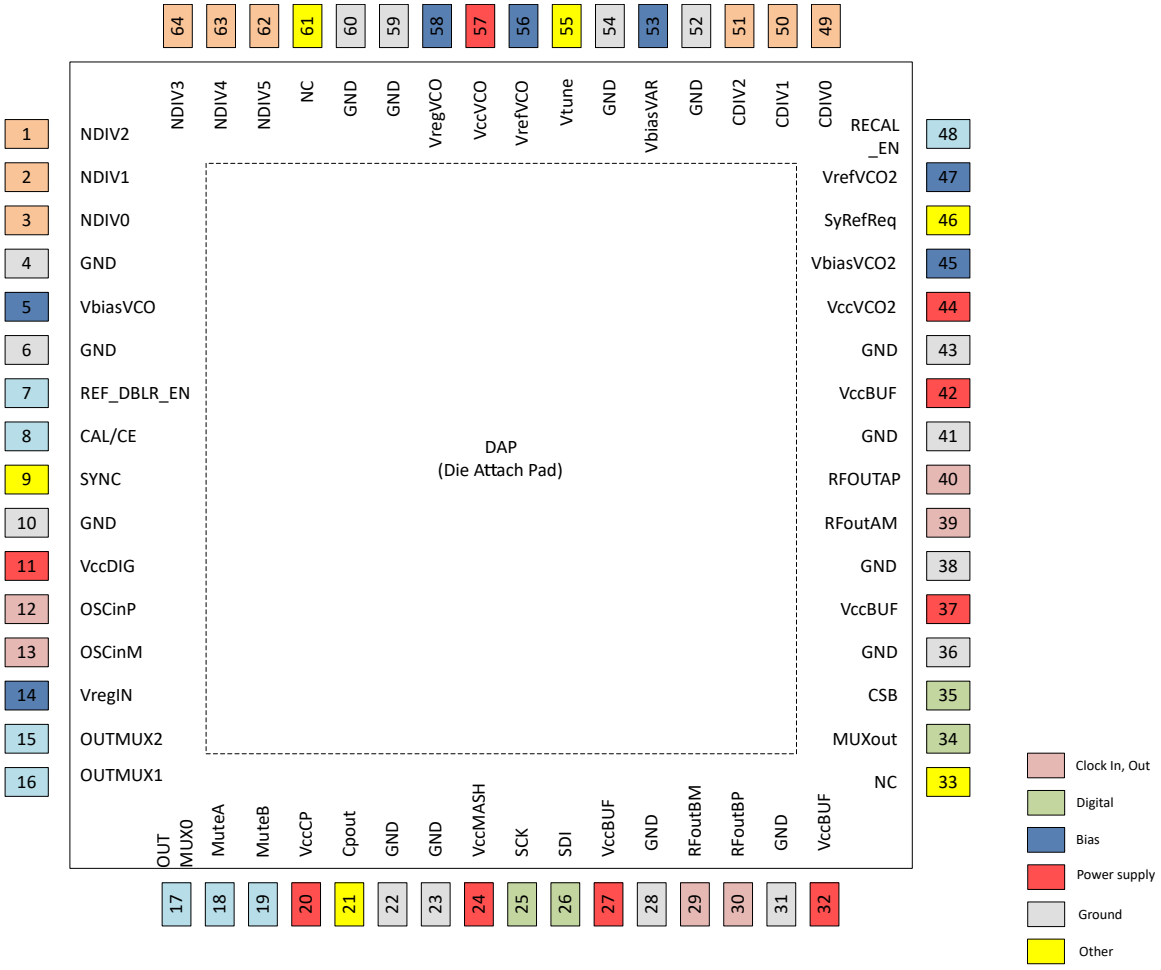

図 4-1. HBD Package 64-Pin CQFP Top View

表 4-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	NDIV2	I	4-level pin	Integer N divider bit 2 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
2	NDIV1	I	4-level pin	Integer N divider bit 1 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
3	NDIV0	I	4-level pin	Integer N divider bit 0 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
4	GND	—	—	Ground
5	VbiasVCO	—	—	VCO bias. Requires connecting 10-µF capacitor to ground. Place close to pin.
6	GND	—	—	Ground
7	REF_DBLR_EN	I	—	Input Reference Doubler enable in Pin-mode. A HIGH on this pin enables the reference doubler and LOW on this pin bypass the Input Reference Doubler. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.

表 4-1. Pin Functions (続き)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
8	CAL/CE	I	—	Chip enable. In Pin Mode (not SPI-mode), rising edges presented to this pin activate the VCO calibration. In SPI-mode, this pin acts like CE where a high on CE pin make device to enable and Low disables the device.
9	SYNC	I	—	Phase synchronization input pin.
10	GND	—	—	Ground
11	VccDIG	—	—	Digital supply. Recommend connecting 0.1-µF capacitor to ground.
12	OSCinP	I	—	Complimentary Reference input clock pins. High input impedance. Requires connecting series capacitor (0.1 µF recommended).
13	OSCinM	I	—	Complimentary pin to OSCinP.
14	VregIN	—	—	Input reference path regulator decoupling. Requires connecting 1-µF capacitor to ground. Place close to pin.
15	OUTMUX2	I	—	Controls the Output Mux selection together with OUTMUX1 and OUTMUX0 for RFOUTA and RFOUTB. The eight options include selecting VCO output, Doubler output or Channel Divider output combinations for RFOUTA and RFOUTB. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
16	OUTMUX1	I	—	Controls the Output Mux selection together with OUTMUX2 and OUTMUX0 for RFOUTA and RFOUTB. The eight options include selecting VCO output, Doubler output or Channel Divider output combinations for RFOUTA and RFOUTB. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
17	OUTMUX0	I	—	Controls the Output Mux selection together with OUTMUX2 and OUTMUX1 for RFOUTA and RFOUTB. The eight options include selecting VCO output, Doubler output or Channel Divider output combinations for RFOUTA and RFOUTB. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
18	MuteA	I	—	Output Buffer mute control. High-impedance CMOS input. RFOUTA is muted or unmuted using this MuteA pin
19	MuteB	I	—	Output Buffer mute control. High-impedance CMOS input. RFOUTB is muted or unmuted using this MuteB pin
20	VccCP	I	—	Charge pump supply. Recommend connecting 0.1-µF capacitor to ground.
21	CPout	O	—	Charge pump output. Recommend connecting C1 of loop filter close to charge pump pin.
22	GND	—	Ground	Ground
23	GND	—	Ground	Ground
24	VccMASH	—	—	Digital supply. Recommend connecting 0.1-µF and 10-µF capacitor to ground.
25	SCK	I	—	SPI input clock. High impedance CMOS input. 1.8 – 3.3V logic.
26	SDI	I	—	SPI input data. High impedance CMOS input. 1.8 – 3.3V logic.
27	VccBUF	—	—	Output buffer supply. Requires connecting 0.1-µF capacitor to ground.
28	GND	—	Ground	Ground
29	RFoutBM	O	—	Complementary pin for RFoutBP
30	RFoutBP	O	—	Differential output B Pair. Requires connecting a 50-Ω resistor pullup to V_{CC} as close as possible to pin. Can be used as a synthesizer output or SYSREF output.
31	GND	—	Ground	Ground
32	VccBUF	—	—	Output buffer supply. Requires connecting 0.1-µF capacitor to ground.
33	NC	—	—	No connection. Leave Unconnected.
34	MUXout	—	—	Multiplexed output pin. Can output: lock detect, SPI readback and diagnostics.
35	CSB	—		SPI chip select bar. High impedance CMOS input. 1.8 – 3.3-V logic.
36	GND	—	Ground	Ground
37	VccBUF	—	—	Output buffer supply. Requires connecting 0.1-µF capacitor to ground.
38	GND	—	Ground	Ground
39	RFoutAM	O	—	Differential output A Pair. 50-Ω resistor pullup to V_{CC} is integrated.

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表 4-1. Pin Functions (続き)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
40	RFoutAP	O	—	Differential output A Pair. 50-Ω resistor pullup to V_{CC} is integrated.
41	GND	—	Ground	Ground
42	VccBUF	—	—	Output buffer supply. Requires connecting 0.1-µF capacitor to ground.
43	GND	—	Ground	Ground
44	VccVCO2	—	—	VCO supply. Recommend connecting 0.1-µF and 10-µF capacitor to ground.
45	VbiasVCO2	—	—	VCO bias. Requires connecting 1-µF capacitor to ground.
46	SysRefReq	I	—	SYSREF request single ended input for JESD204B support.
47	VrefVCO2	—	—	VCO supply reference. Requires connecting 10-µF capacitor to ground.
48	RECAL_EN	I	—	Enables the automatic recalibration feature. Low on this pin does not trigger calibration. High on this means the calibration is triggered whenever the device is unlocked after certain delay.
49	CDIV0	I	4-level pin	Controls the Channel Divider along with CDIV2 and CDIV1 in Pin-mode option. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
50	CDIV1	I	4-level pin	Controls the Channel Divider along with CDIV0 and CDIV2 in Pin-mode option. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
51	CDIV2	I	4-level pin	Controls the Channel Divider along with CDIV1 and CDIV0 in Pin-mode option. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
52	GND	—	Ground	Ground
53	VbiasVARAC	—	—	VCO Varactor bias. Requires connecting 10-µF capacitor to ground.
54	GND	—	Ground	Ground
55	Vtune	I	—	VCO tuning voltage input.
56	VrefVCO	—	—	VCO supply reference. Requires connecting 10-µF capacitor to ground.
57	VccVCO	—	—	VCO supply. Recommend connecting 0.1-µF and 10-µF capacitor to ground.
58	VregVCO	—	—	VCO regulator node. Requires connecting 1-µF capacitor to ground.
59	GND	—	Ground	Ground
60	GND	—	Ground	Ground
61	NC	—	NC	No Connect
62	NDIV5	I	4-level pin	Integer N divider bit 5 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
63	NDIV4	I	4-level pin	Integer N divider bit 4 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
64	NDIV3	I	4-level pin	Integer N divider bit 3 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage(1)	–0.3	3.6	V
V_{DIG}	Digital pin voltage (SYNC, SysRefReq, RECAL_EN, CAL)	−0.3	V_{CC}+0.3	V
$\|V_{OSCin}\|$	Differential AC voltage between OSCinP and OSCinN		2.1	V_{PP}
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	3.2	3.3	3.45	V
T_C	Case temperature	–55	25	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		CQFP 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (2)	7.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) DAP

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5.5 Electrical Characteristics

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
POWER SUPPLY								
I_{CC}	Supply current (VCO output)	OUTBUFFA_PD = 0, OUTBUFFB_PD = 1 OUTBUFFA_MUXSEL = 1 OUTBUFFA_DACCTRL = 7, CPG = 7 f_{OSC} = f_{PD} = 100 MHz, f_{VCO} = f_{OUT} = 14.5 GHz				480		mA
I_{CC}	Supply current (channel divider output)	OUTBUFFA_PD = 0, OUTBUFFB_PD = 1 OUTBUFFA_MUXSEL = 0 OUTBUFFA_DACCTRL = 7, CPG = 7 f_{OSC} = f_{PD} = 100 MHz, f_{VCO} = 15Ghz, f_{OUT} = 7 GHz				640		mA
I_{CC}	Supply current (Doubler output)	OUTBUFFA_PD = 0, OUTBUFFB_PD = 1 OUTA_MUX = 2 OUTBUFFA_DACCTRL=7, CPG = 7 f_{OSC} = f_{PD} = 100 MHz, f_{VCO} = 12GHz f_{OUT} = 24 GHz				630		mA
I_{CC}	Supply current (Doubler output on both RFOUTA and RFOUTB)	OUTBUFFA_PD = 0, OUTBUFFB_PD = 0 OUTA_MUX = 2 OUTBUFFA_DACCTRL=7, CPG = 7 f_{OSC} = f_{PD} = 100 MHz, f_{VCO} = 12GHz f_{OUT} = 24 GHz				TBD		mA
I_{CC}	Power on reset current	RESET = 1 (Device wake-up)	RESET = 1 (Device wake-up)	RESET = 1 (Device wake-up)		289		mA
I_{CC}	Power down current	POWERDOWN = 1	POWERDOWN = 1	POWERDOWN = 1		14		mA
OUTPUT CHARACTERISTICS								
Fout	RF output frequency				5		28000	MHz
P_{OUT}	Differential output power	OUTx_PWR = 31	f_{OUT} = 28 GHz			TBD		dBm
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 31	f_{OUT} = 28 GHz			3		dBm
P_{OUT}	Differential output power	OUTx_PWR = 31	f_{OUT} = 26 GHz			TBD		dBm
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 31	f_{OUT} = 26 GHz			2		dBm
P_{OUT}	Differential output power	OUTx_PWR = 31	f_{OUT} = 24 GHz			TBD		dBm
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 31	f_{OUT} = 24 GHz			2		dBm
P_{OUT}	Differential output power	OUTx_PWR = 31	f_{OUT} = 22 GHz			TBD		dBm

ADVANCE INFORMATION

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 31	f_{OUT} = 22 GHz			2		dBm
P_{OUT}	Differential output power	OUTx_PWR = 31	f_{OUT} = 18 GHz			TBD		dBm
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 31	f_{OUT} = 18 GHz			3		dBm
P_{OUT}	Differential output power	OUTx_PWR = 31; VCO output	f_{OUT} = 15 GHz			TBD		dBm
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 31; VCO output	f_{OUT} = 15 GHz			3		dBm
P_{OUT}	Differential output power	OUTx_PWR = 31; VCO output	f_{OUT} = 7.5 GHz			TBD		dBm
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 31; VCO output	f_{OUT} = 7.5GHz			7		dBm
P_{OUT}	Differential output power	OUTx_PWR = 31; VCO output	f_{OUT} = 4 GHz			TBD		dBm
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 31; VCO output	f_{OUT} = 4 GHz			6		dBm
$H_{3/2}$	1/2 Harmonic, single ended measurement	F_{out} = 2 x F_{vco} = 24 GHz	Measured at 12GHz frequency;			TBD		dBc
$H_{3/2}$	1/2 Harmonic, differential ended	F_{out} = 2 x F_{vco} = 24 GHz	Measured at 12GHz frequency;			-55		dBc
$H_{3/2}$	3/2 Harmonic, single ended measurement	F_{out} = 2 x F_{vco} = 16 GHz	Measured at 24GHz frequency			TBD		dBc
$H_{3/2}$	3/2 Harmonic, differential ended measurement	F_{out} = 2 x F_{vco} = 16 GHz	Measured at 24GHz frequency			TBD		dBc
P_{mute}	Single-ended output power leakage when output is muted	Fout = 24 GHz				-50		dBm
P_{mute}	Single-ended output power leakage when output is muted	Fout = 12 GHz				-51		dBm
P_{mute}	Single-ended output power leakage when output is muted	Fout = 6 GHz				-91		dBm
t_{MUTE}	Mute enable time	Fout = 12 GHz				200		ns
t_{UNMUTE}	Mute disable time	Fout = 12 GHz				200		ns
isoCH	Channel to channel isolation (Doubler to VCO)	RFOUTA = 24 GHz; RFOUTB = 12 GHz				-39		dBC
isoCH	Channel to channel isolation (VCO to CH divider)	RFOUTA = 12 GHz; RFOUTB = 6 GHz				-53		dBC
isoCH	Channel to channel isolation (Doubler to CH divider)	RFOUTA = 24 GHz; RFOUTB = 6 GHz				-41		dBC
Phase Noise	RF Output Frequency Phase Noise	Fout = 24 GHz		1 KHz		-87		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 24 GHz		10 KHz		-99		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 24 GHz		100 KHz		-101		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 24 GHz		1 MHz		-113		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 24 GHz		10 MHz		-137		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 24 GHz		100 MHz		-151		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 15 GHz		1 KHz		-97		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 15 GHz		10 KHz		-104		dBc/Hz

ADVANCE INFORMATION

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Phase Noise	RF Output Frequency Phase Noise	Fout = 15 GHz		100 KHz		-104		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 15 GHz		1 MHz		-117		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 15 GHz		10 MHz		-140		dBc/Hz
Phase Noise	RF Output Frequency Phase Noise	Fout = 15 GHz		100 MHz		-156		dBc/Hz
Jitter	RMS Jitter	Fout = 24 GHz, Integration range 1 KHz to 100 MHz				56		fs
Jitter	RMS Jitter	Fout = 24 GHz, Integration range 1 KHz to 12 GHz; No filter in clock output				TBD		fs
Skew	Skew between RFOUTA and RFOUTB	RFOUTA = RFOUTB = 4GHz				7		ps
INPUT SIGNAL PATH								
f_{OSCin}	Reference input frequency	OSC_2X = 0	OSC_2X = 0	OSC_2X = 0	5		1200	MHz
f_{OSCin}	Reference input frequency	OSC_2X = 1	OSC_2X = 1	OSC_2X = 1	5		200	
v_{OSCin}	Reference input voltage	Single-ended AC coupled sine wave input with complementary side AC coupled to ground with 50 Ω resistor		f_{OSCin} ≥ 20 MHz	0.4		2	V_{PP}
v_{OSCin}	Reference input voltage	Single-ended AC coupled sine wave input with complementary side AC coupled to ground with 50 Ω resistor		10 MHz ≤ f_{OSCin} < 20 MHz	0.8		2	V_{PP}
v_{OSCin}	Reference input voltage	Single-ended AC coupled sine wave input with complementary side AC coupled to ground with 50 Ω resistor		5 MHz ≤ f_{OSCin} < 10 MHz	1.6		2	V_{PP}
PHASE DETECTOR AND CHARGE PUMP								
f_{PD}	Phase detector frequency(1)	MASH_ORDER = 0	MASH_ORDER = 0	MASH_ORDER = 0	0.125		250	MHz
f_{PD}	Phase detector frequency(1)	MASH_ORDER > 0	MASH_ORDER > 0	MASH_ORDER > 0	5		200	MHz
I_{CPout}	Charge-pump leakage current	CPG = 0	CPG = 0	CPG = 0		15		nA
I_{CPout}	Effective charge pump current. This is the sum of the up and down currents	CPG = 4	CPG = 4	CPG = 4		3		mA
I_{CPout}	Effective charge pump current. This is the sum of the up and down currents	CPG = 1	CPG = 1	CPG = 1		6		mA
I_{CPout}	Effective charge pump current. This is the sum of the up and down currents	CPG = 5	CPG = 5	CPG = 5		9		mA
I_{CPout}	Effective charge pump current. This is the sum of the up and down currents	CPG = 3	CPG = 3	CPG = 3		12		mA

ADVANCE INFORMATION

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CPout}	Effective charge pump current. This is the sum of the up and down currents	CPG = 7	CPG = 7	CPG = 7		15		mA
$PN_{PLL\_1/f}$	Normalized PLL 1/f noise	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(3)	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(3)	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(3)		–129		dBc/Hz
PN_{PLL_FOM}	Normalized PLL noise floor	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(3)	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(3)	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(3)		–236		dBc/Hz

ADVANCE INFORMATION

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
VCO CHARACTERISTICS								
f_{VCO}	VCO frequency				7500		15000	MHz
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8.1 GHz	VCO1 f_{VCO} = 8.1 GHz	100 kHz		–105		dBc/Hz
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8.1 GHz	VCO1 f_{VCO} = 8.1 GHz	1 MHz		–127		dBc/Hz
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8.1 GHz	VCO1 f_{VCO} = 8.1 GHz	10 MHz		–148		dBc/Hz
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8.1 GHz	VCO1 f_{VCO} = 8.1 GHz	100 MHz		–155		dBc/Hz
PN_{VCO}	VCO phase noise	VCO2 f_{VCO} = 9.3 GHz	VCO2 f_{VCO} = 9.3 GHz	100 kHz		–103		dBc/Hz
PN_{VCO}	VCO phase noise	VCO2 f_{VCO} = 9.3 GHz	VCO2 f_{VCO} = 9.3 GHz	1 MHz		–125		dBc/Hz
PN_{VCO}	VCO phase noise	VCO2 f_{VCO} = 9.3 GHz	VCO2 f_{VCO} = 9.3 GHz	10 MHz		–146		dBc/Hz
PN_{VCO}	VCO phase noise	VCO2 f_{VCO} = 9.3 GHz	VCO2 f_{VCO} = 9.3 GHz	100 MHz		–153		dBc/Hz
PN_{VCO}	VCO phase noise	VCO3 f_{VCO} = 10.4 GHz	VCO3 f_{VCO} = 10.4 GHz	100 kHz		–103		dBc/Hz
PN_{VCO}	VCO phase noise	VCO3 f_{VCO} = 10.4 GHz	VCO3 f_{VCO} = 10.4 GHz	1 MHz		–125		dBc/Hz
PN_{VCO}	VCO phase noise	VCO3 f_{VCO} = 10.4 GHz	VCO3 f_{VCO} = 10.4 GHz	10 MHz		–147		dBc/Hz
PN_{VCO}	VCO phase noise	VCO3 f_{VCO} = 10.4 GHz	VCO3 f_{VCO} = 10.4 GHz	100 MHz		–158		dBc/Hz
PN_{VCO}	VCO phase noise	VCO4 f_{VCO} = 11.4 GHz	VCO4 f_{VCO} = 11.4 GHz	100 kHz		–101		dBc/Hz
PN_{VCO}	VCO phase noise	VCO4 f_{VCO} = 11.4 GHz	VCO4 f_{VCO} = 11.4 GHz	1 MHz		–124		dBc/Hz
PN_{VCO}	VCO phase noise	VCO4 f_{VCO} = 11.4 GHz	VCO4 f_{VCO} = 11.4 GHz	10 MHz		–146		dBc/Hz
PN_{VCO}	VCO phase noise	VCO4 f_{VCO} = 11.4 GHz	VCO4 f_{VCO} = 11.4 GHz	100 MHz		–158		dBc/Hz
PN_{VCO}	VCO phase noise	VCO5 f_{VCO} = 12.5 GHz	VCO5 f_{VCO} = 12.5 GHz	100 kHz		–102		dBc/Hz
PN_{VCO}	VCO phase noise	VCO5 f_{VCO} = 12.5 GHz	VCO5 f_{VCO} = 12.5 GHz	1 MHz		–126		dBc/Hz
PN_{VCO}	VCO phase noise	VCO5 f_{VCO} = 12.5 GHz	VCO5 f_{VCO} = 12.5 GHz	10 MHz		–147		dBc/Hz
PN_{VCO}	VCO phase noise	VCO5 f_{VCO} = 12.5 GHz	VCO5 f_{VCO} = 12.5 GHz	100 MHz		–156		dBc/Hz
PN_{VCO}	VCO phase noise	VCO6 f_{VCO} = 13.6 GHz	VCO6 f_{VCO} = 13.6 GHz	100 kHz		–101		dBc/Hz
PN_{VCO}	VCO phase noise	VCO6 f_{VCO} = 13.6 GHz	VCO6 f_{VCO} = 13.6 GHz	1 MHz		–124		dBc/Hz
PN_{VCO}	VCO phase noise	VCO6 f_{VCO} = 13.6 GHz	VCO6 f_{VCO} = 13.6 GHz	10 MHz		–146		dBc/Hz
PN_{VCO}	VCO phase noise	VCO6 f_{VCO} = 13.6 GHz	VCO6 f_{VCO} = 13.6 GHz	100 MHz		–160		dBc/Hz
PN_{VCO}	VCO phase noise	VCO7 f_{VCO} = 14.7 GHz	VCO7 f_{VCO} = 14.7 GHz	100 kHz		–101		dBc/Hz
PN_{VCO}	VCO phase noise	VCO7 f_{VCO} = 14.7 GHz	VCO7 f_{VCO} = 14.7 GHz	1 MHz		–124		dBc/Hz
PN_{VCO}	VCO phase noise	VCO7 f_{VCO} = 14.7 GHz	VCO7 f_{VCO} = 14.7 GHz	10 MHz		–146		dBc/Hz
PN_{VCO}	VCO phase noise	VCO7 f_{VCO} = 14.7 GHz	VCO7 f_{VCO} = 14.7 GHz	100 MHz		–157		dBc/Hz

ADVANCE INFORMATION

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
	Lock time	No Assist mode; RFOUTA from 9.5GHz to 9.52GHz;Loop Bandwidth = 300KHz, PFD Frequency = 100MHz;				3000		µs
	Lock time	Full Assist mode, Loop Bandwidth = 300KHz, PFD Frequency = 100MHz; RFOUTA from 9.5GHz to 9.52GHz, 1PPM settling around RFOUT				16		µs
K_{VCO}	VCO Gain	8.1 GHz				94		MHz/V
K_{VCO}	VCO Gain	9.3 GHz				106		MHz/V
K_{VCO}	VCO Gain	10.4 GHz				122		MHz/V
K_{VCO}	VCO Gain	11.4 GHz				148		MHz/V
K_{VCO}	VCO Gain	12.5 GHz				185		MHz/V
K_{VCO}	VCO Gain	13.6 GHz				202		MHz/V
K_{VCO}	VCO Gain	14.7 GHz				233		MHz/V
$\lvert\Delta T_{CL}\rvert$	Allowable temperature drift when VCO is not re-calibrated	configured in SPI mode				125		°C
H2	VCO second harmonic	f_{VCO} = 8 GHz, divider disabled				–30		dBc
H3	VCO third harmonic	f_{VCO} = 8 GHz, divider disabled				−25		dBc

ADVANCE INFORMATION

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
DIGITAL INTERFACE (Applies to SCK, SDI, CSB, CAL, RECAL_EN, MUXout, SYNC, SysRefReq)								
V_{IH}	High-level input voltage				1.6			V
V_{IL}	Low-level input voltage						0.4	V
I_{IH}	High-level input current				–100		100	µA
I_{IL}	Low-level input current				–100		100	µA
V_{OH}	High-level output voltage	MUXout pin		Load current = –5 mA	V_{CC} – 0.6			V
V_{OL}	Low-level output voltage	MUXout pin		Load current = 5 mA			0.6	V
	SYSREF Output Common mode voltage					TBD		V
	SYREF Output Swing					TBD		V
	SYSREF Frequency range					TBD		MHz
	SYSREF delay step size					TBD		ps
VL	CDIV0, CDIV1, CDIV2 Voltage levels				0		0.4	V
VML	CDIV0, CDIV1, CDIV2 Voltage levels				0.8	VCC/3	1.4	V
VMH	CDIV0, CDIV1, CDIV2 Voltage levels				1.9	2*VCC/3	2.5	V
VH	CDIV0, CDIV1, CDIV2 Voltage levels				3	VCC	3.45	V
VL	NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5 Voltage levels				0		0.4	V
VML	NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5 Voltage levels				0.8	VCC/3	1.4	V
VMH	NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5 Voltage levels				1.9	2*VCC/3	2.5	V
VH	NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5 Voltage levels				3	VCC	3.45	V

(1) For lower VCO frequencies, the N divider minimum value can limit the phase-detector frequency.
(2) Single-ended output power obtained after de-embedding microstrip trace losses and matching with a manual tuner. Unused port terminated to 50-Ω load.
(3) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. PLL_flat = PLL_FOM + 20× log(Fvco/Fpd) + 10 × log(Fpd / 1Hz). PLL_flicker (offset) = PLL_1/f + 20 × log(Fvco / 1GHz) – 10× log(offset / 10kHz). After these two components are found, the total PLL noise can be calculated as PLL_Noise = 10 × log($10^{PLL\_Flat / 10}$ + $10^{PLL\_flicker /10}$)
(4) Output power, spurs, and harmonics can vary based on board layout and components.

5.6 Timing Requirements

(3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_A ≤ +125°C, except as specified. Nominal values are at V_{CC} = 3.3 V, T_A = 25°C)

			MIN	NOM	MAX	UNIT
DIGITAL INTERFACE WRITE SPECIFICATIONS						
f_{SPI}Write	SPI write speed				40	MHz
t_{CE}	Clock to enable low time	See Timing Diagram	2.5			ns
t_{CS}	Data to clock setup time		8.6			ns
t_{CH}	Data to clock hold time		0.6			ns
t_{CWH}	Clock pulse width high		5			ns
t_{CWL}	Clock pulse width low		10			ns
t_{CES}	Enable to clock setup time		6.5			ns
t_{EWH}	Enable pulse width high		5			ns
DIGITAL INTERFACE READBACK SPECIFICATIONS						
f_{SPI}Readback	SPI readback speed				40	MHz

ADVANCE INFORMATION

($3.2\ V \le V_{CC} \le 3.45\ V$, $-55°C \le T_A \le +125°C$, except as specified. Nominal values are at $V_{CC} = 3.3\ V$, $T_A = 25°C$)

			MIN	NOM	MAX	UNIT
t_{CE}	Clock to enable low time	See Timing Diagram	2.5			ns
t_{CS}	Clock to data wait time		8.6			ns
t_{CWH}	Clock pulse width high		10			ns
t_{CWL}	Clock pulse width low		10			ns
t_{CES}	Enable to clock setup time		6.5			ns
t_{EWH}	Enable pulse width high		5			ns
t_{CD}	Falling clock edge to data wait time		TBD			ns
SYNC and SYSREFREQ						

5.7 Timing Diagrams

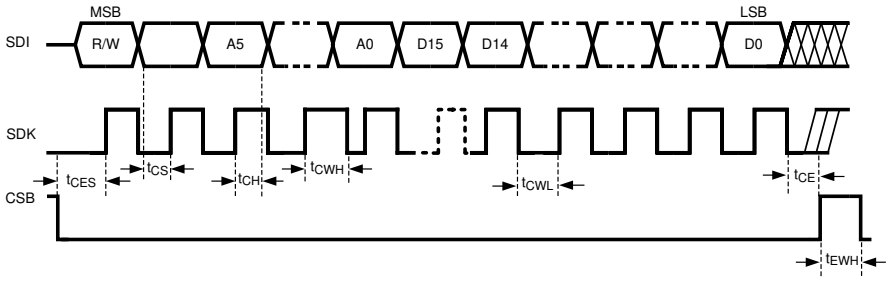

図 5-1. Serial Data Input Timing Diagram

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
- The CSB must be held low for data to be clocked. Device is ignore clock pulses if CSB is held high.
- The CSB transition from high to low must occur when SCK is low.
- When SCK and SDI lines are shared between devices, TI recommends hold the CSB line high on the device that is not to be clocked.

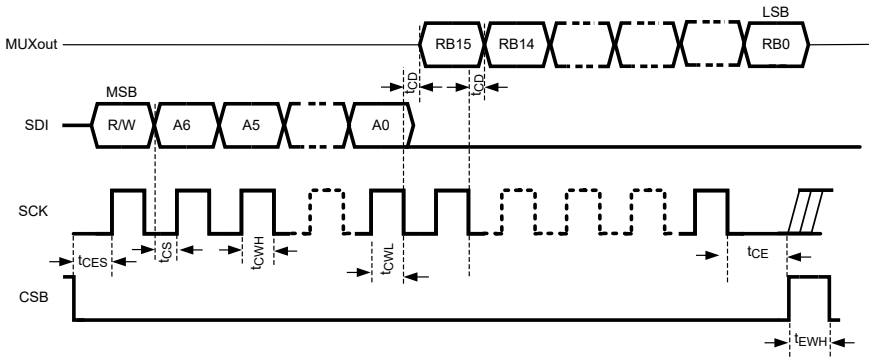

図 5-2. Serial Data Readback Timing Diagram

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXout pin is tristated for the address portion of the transaction, and when there is no transaction
- The data on MUXout becomes available momentarily after the falling edge of SCK and therefore must be read back on the rising edge of SCK.
- The data portion of the transition on the SDI line is always ignored.

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6 Detailed Description

6.1 Overview

The LMX2624-SP is a high-performance, wideband frequency synthesizer with integrated VCO, output doubler and output divider. The VCO operates from 7500 to 15000 MHz and this can be combined with the output divider and doubler to produce any frequency in the range of 5 MHz to 28 GHz.

The PLL is fractional-N PLL with programmable delta-sigma modulator up to 4^{th} order. The fractional denominator is a programmable 32-bit long, which can provide fine frequency steps easily below 1-Hz resolution as well as be used to do exact fractions like 1/3, 7/1000, and many others.

The phase detector frequency goes up to 200MHz in fractional mode and 250MHz in integer mode, although minimum N-divider values must also be taken into account. For applications where deterministic or adjustable phase is desired, the SYNC pin can be used to get the phase relationship between the OSCin and RFout pins deterministic. When this is done, the phase can be adjusted in very fine steps of the VCO period divided by the fractional denominator.

The ultra-fast VCO calibration is designed for applications where the frequency must be swept or abruptly changed. The device has both Pin-mode and SPI-mode options where the frequency can be configured manually using general purpose inputs or programmed using SPI.

The JESD204B support includes using the RFoutB output to create a differential SYSREF output that can be either a single pulse or a series of pulses that occur at a programmable distance away from the rising edges of the output signal.

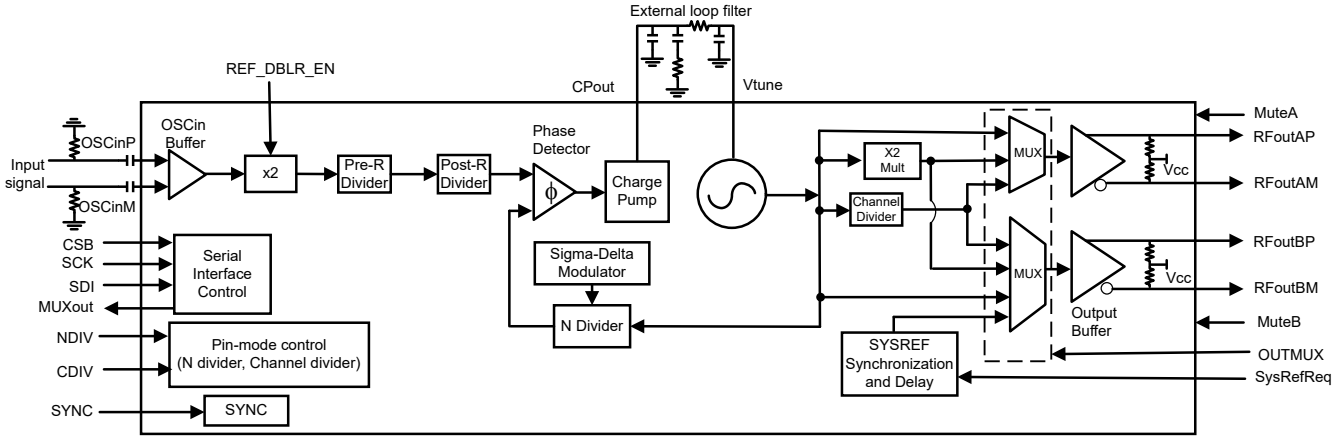
The LMX2624-SP device requires only a single 3.3-V power supply. The internal power supplies are provided by integrated LDOs, eliminating the need for high performance external LDOs.

表 6-1 shows the range of several of the doubler, dividers, and fractional settings.

表 6-1. Range of Doubler, Divider, and Fractional Settings

PARAMETER	FIELD	MIN	MAX	COMMENTS
OSCin doubler	OSC_2X	0 (1X)	1 (2X)	The low noise doubler can be used to increase the phase detector frequency to improve phase noise and avoid spurs. This is in reference to the OSC_2X bit.
Pre-R divider	PLL_R_PRE	1 (bypass)	128	Only use the Pre R divider if the input frequency is too high for the Post R divider.
Post-R divider	PLL_R	1 (bypass)	255	The maximum input frequency for the post-R divider is 250 MHz. Use the Pre R divider if necessary.
N divider	PLL_N	≥ 28	524287	The minimum divide depends on modulator order and VCO frequency. See *セクション 6.3.5* for more details.
Fractional numerator/ denominator	PLL_NUM, PLL_DEN	1 (Integer mode)	$2^{32} – 1 = 4294967295$	The fractional denominator is programmable and can assume any value between 1 and $2^{32} – 1$; the denominator is not a fixed value.
Fractional order	MASH_ORDER	0	4	Order 0 is integer mode and the order can be programmed
Channel divider	CHDIV	1 (bypass)	1536	This is the series of several dividers. Also, be aware that above 10 GHz, the maximum allowable channel divider value is 6.
Output frequency		5 MHz	28 GHz	Below 7.6 GHz, Channel Divider is used. 7.6 GHz to 15.2 GHz is from VCO. 15.2 GHz to 28 GHz is from VCO along with output doubler

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Reference Oscillator Input

The OSCin pins are used as a frequency reference input to the device. The input is high impedance and requires AC-coupling caps at the pin. The OSCin pins can be driven single-ended with a CMOS clock or XO. Differential clock input is also supported, making interfacing with high-performance system clock devices such as TI's LMK series clock devices simpler. As the OSCin signal is used as a clock for the VCO calibration, a proper reference signal must be applied at the OSCin pin at the time of programming FCAL_EN.

6.3.2 Reference Path

The reference path consists of an OSCin doubler (OSC_2X), Pre-R divider, and a Post-R divider.

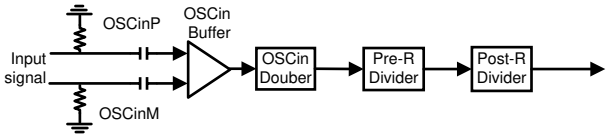


図 6-1. Reference Path Diagram

The OSCin doubler (OSC_2X) can double up low OSCin frequencies. The OSCin doubler allows one to double the input reference frequency. This doubler adds minimal noise and is useful for increasing the Phase Detector frequency and also to avoid spurs. When the phase detector frequency is increased, the flat portion of the PLL phase noise improves. Pre-R (PLL_R_PRE) and Post-R (PLL_R) dividers both divide frequency down. The phase detector frequency, f_{PD}, is calculated in 式 1

$$f_{PD} = f_{OSC} \times OSC\_2X / (PLL\_R\_PRE \times PLL\_R) \quad (1)$$

For 式 1, remember:

- If the OSCin doubler is used, the OSCin signal must have around 50% duty cycle as both the rising and falling edges are used. Otherwise the spurs are high.
- If the OSCin doubler is not used, only rising edges of the OSCin signal are used and duty cycle is not critical.

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6.3.2.1 OSCin Doubler (OSC_2X)

The OSCin doubler allows one to double the input reference frequency up to 400MHz while adding minimal noise. In some situations using the doubler can be advantageous to go to a higher frequency than the maximum phase detector frequency because the Pre-R divider is able to divide down this frequency to phase detector frequency that is advantageous for fractional spurs.

6.3.2.2 Pre-R Divider (PLL_R_PRE)

The pre-R divider is useful for reducing the input frequency to help meet the maximum 250-MHz input frequency limitation to the PLL-R divider. Otherwise, the pre-divider does not have to be used.

6.3.2.3 Post-R Divider (PLL_R)

The post-R divider can be used to further divide down the frequency to the phase detector frequency. When the divider is used (PLL_R > 1), the input frequency to this divider is limited to 250 MHz.

6.3.3 State Machine Clock

The state machine clock is a divided down version of the OSCin signal that is used internally in the device. This divide value 1, 2, 4, 8, or 16 and is determined by CAL_CLK_DIV programming word (described in the programming section). This state machine clock impacts VCO calibration. The state machine clock is calculated as fsmclk = f_{OSC} / $2^{CAL\_CLK\_DIV}$.

6.3.4 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-R divider and N divider and generates a correction current corresponding to the phase error until the two signals are aligned in phase. This charge-pump current is software programmable to many different levels, allowing modification of the closed-loop bandwidth of the PLL.

6.3.5 N Divider and Fractional Circuitry

The N divider includes fractional compensation and can achieve any fractional denominator from 1 to (2^{32} – 1). The integer portion of N is the whole part of the N divider value, and the fractional portion, N_{frac} = NUM / DEN, is the remaining fraction. In general, the total N divider value is determined by N + NUM / DEN. The N, NUM and DEN are software programmable in SPI mode. Pin-mode option has integer frequency generation and refer Pin-mode description details in Pin-mode section for more details.

The higher the denominator, the finer the resolution step of the output. For example, even when using f_{PD} = 200 MHz, the output can increment in steps of 200 MHz /(2^{32} – 1) = 0.047 Hz. 式 2 shows the relationship between the phase detector and VCO frequencies. Note that in SYNC mode, there is an extra divider that is not shown in 式 2.

$$f_{VCO} = f_{pd} \times \left(N + \frac{NUM}{DEN} \right) \quad (2)$$

The sigma-delta modulator that controls this fractional division is also programmable from integer mode to fourth order. To make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

The N divider has minimum value restrictions based on the modulator order and VCO frequency. Furthermore, the PFD_DLY_SEL bit must be programmed in accordance to the 表 6-2. In SYNC mode, IncludedDivide can be larger than one, otherwise IncludedDivide is one.

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表 6-2. Minimum N Divider Restrictions

MASH_ORDER	f_{VCO} / IncludedDivide (MHz)	MINIMUM N	PFD_DLY_SEL
0	≤ 12500	29	1
	> 12500	33	2
1	≤ 10000	30	1
	10000 – 12500	34	2
	>12250	38	3
2	≤ 4000 (SYNC Mode)	31	1
	4000-7500 (SYNC Mode)	31	2
	7500 – 10000	33	2
	>10000	37	3
3	≤ 4000 (SYNC Mode)	33	1
	4000-7500 (SYNC Mode)	37	2
	7500 – 10000	41	3
	>10000	45	4
4	≤ 4000 (SYNC Mode)	45	3
	4000-7500 (SYNC Mode)	49	4
	7500 – 10000	53	5
	>10000	57	6

6.3.6 MUXout Pin

The MUXout pin can be configured as lock detect indicator for the PLL or as an serial data output (SDO) for the SPI interface to readback registers. Field MUXOUT_LD_SEL (register R0[2]) configures this output.

表 6-3. MUXout Pin Configurations

MODE of operation	MUXOUT_SEL bit	MUXOUT pin	FUNCTION
Pin-mode	X	Lock Detect	Lock detect indicator for PLL
SPI-mode	1 (default)	Tristate	Tristated
SPI-mode	0	Lock Detect	Lock detect indicator for PLL
SPI-mode	X	SDO	When SPI_Read bit is set to 1, MUXOUT pin is used for Serial data output for reading SPI data

When lock detect indicator is selected, there are two types of indicator and the indicators can be selected with the field LD_TYPE (register R59[0]). The first indicator is called “VCOCal” (LD_TYPE=0) and the second indicator is called “Vtune and VCOCal” (LD_TYPE=1).

6.3.6.1 Serial Data Output for Readback

In spi-mode, the MUXout pin become the serial data output of the SPI. This output can be tri-stated using MUXout_SEL bit. Details of this pin operation are described with the serial interface description. Readback is useful when a device is used is full assist mode and VCO calibration data are retrieve and saved for future use. Readback can also be used to read back the lock detect status using the field rb_LD_VTUNE(register R110[10:9]).

6.3.6.2 Lock Detect Indicator Set as Type “VCOcal” or "Vtune and VCOcal"

LD_LOCK_EN bit is used to select the type of the Lock detect indication. If this bit is 0x0, "VCOcal" type is selected and if this bit is set to 0x1, then "Vtune and VCOcal" type is selected.

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When 'VCOcal' lock detect type is selected, the bit asserts a high output at MUXout pin after the VCO has finished calibration and the LD_DLY timeout counter is finished. Otherwise MUXout pin is LOW.

When 'Vtune and VCOcal" lock detect type is selected, the bit asserts a high output at MUXout pin if tuning voltage to the VCO is within acceptable levels along with the VCO calibration and LD_DLY timeout counter is finished. Otherwise MUXout pin is LOW.

The programmable timer (LD_DLY, register R60[15:0]) adds an additional delay after the VCO calibration finishes before the lock detect indicator is asserted high. LD_DLY is a 16 bit unsigned quantity that corresponds to the number of phase detector cycles in absolute delay. For example, a phase detector frequency of 100MHz and the LD_DLY=10000 adds a delay of 100µs before the indicator is asserted. The lock detector goes LOW if the PLL goes out of lock or the input reference clock is removed.

6.3.7 VCO (Voltage-Controlled Oscillator)

The LMX2624-SP includes a fully integrated VCO. The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies as shown in 式 3:

$$f_{VCO} = f_{PD} \times N\ divider \times N\ IncludedDivide \quad (3)$$

Based in this table, the VCO gain can be estimated for an arbitrary VCO frequency of f_{VCO} as 式 4:

$$Kvco = Kvco1 + (Kvco2-Kvco1) \times (f_{VCO} - f1) / (f2 - f1) \quad (4)$$

6.3.7.1 VCO Calibration

To reduce the VCO tuning gain and therefore improve the VCO phase-noise performance, the VCO frequency range is divided into several different frequency bands. The entire range, 7500MHz to 15000MHz, covers an octave that allows the divider to take care of frequencies below the lower bound. This creates the need for frequency calibration to determine the correct frequency band given a desired output frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1. A valid OSCin signal must present before VCO calibration begins.

The VCO also has an internal amplitude calibration algorithm to optimize the phase noise which is also activated any time the R0 register is programmed.

The optimum internal settings for this are temperature dependent. If the temperature is allowed to drift too much without being re-calibrated, some minor phase noise degradation can result. The maximum allowable drift for continuous lock, ΔT_{CL}, is stated in the electrical specifications. For this device, temperature of 125°C means the device never loses lock if the device is operated under recommended operating conditions.

The LMX2624-SP allows the user to assist the VCO calibration. In general, there are four kinds of assistance, as shown in 表 6-4:

表 6-4. Assisting the VCO Calibration Speed

ASSISTANCE LEVEL	DESCRIPTION	VCO_SEL	VCO_SEL_FORCE VCO_CAPCTRL_FORCE VCO_DACISET_FORCE	VCO_CAPCTRL VCO_DACISET
No assist	User does nothing to improve VCO calibration speed.	7	0	Don't Care
Partial assist	Upon every frequency change, before the FCAL_EN bit is checked, the user provides the initial starting VCO_SEL	Choose by table	0	Don't Care
Full assist	The user forces the VCO core (VCO_SEL), amplitude settings (VCO_DACISET), and frequency band (VCO_CAPCTRL) and manually sets the value. If the two frequency points are no more than 5MHz apart and on the same VCO core, the user can set the VCO amplitude and capcode for any frequency between those two points using linear interpolation	Choose by readback	1	Choose by readback

6.3.7.1.1 Double Buffering (Shadow Registers)

Double buffering—also known as "shadow registers"—allows the user to program multiple registers without having them actually take effect. Then when the R0 register is programmed, then these registers take effect. This is especially useful if one wants to change frequencies quickly and multiple register writes are required. When DBLBUF_EN = 1, the double buffering is enabled for the registers related to VCO, Doubler, PLL, Output MUX and Channel Divider. More details on the registers are available in Register map section.

For the no assist method, just set VCO_SEL=7 and this is done. For partial assist, the VCO calibration speed can be improved by changing the VCO_SEL bit according to the frequency. Note that the frequency is not the actual VCO core range, but favors choosing the VCO. This is not only optimal for VCO calibration speed, but required for reliable locking.

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表 6-5. Minimum VCO_SEL for Partial Assist

f_{VCO}	VCO CORE (MIN)
7500 - 8600MHz	VCO1
8600 - 9900MHz	VCO2
9900 - 10800MHz	VCO3
10800 -11900MHz	VCO4
11900 - 13000MHz	VCO5
13000 - 14000MHz	VCO6
14000 - 15000MHz	VCO7

For fastest calibration time, use the minimum VCO core as recommended in the previous table. The following table shows typical VCO calibration times for this choice in bold as well as showing how long the calibration time is increased if a higher than necessary VCO core is chosen. Realize that these calibration times are specific to these f_{OSC} and f_{PD} conditions specified and at the boundary of two cores, sometimes the calibration time can be increased.

表 6-6. Typical Calibration Times (µs) for f_{OSC} = 100MHz and f_{PD} = 200MHz

f_{VCO}	VCO_SEL#none#						
	VCO7	VCO6	VCO5	VCO4	VCO3	VCO2	VCO1
8.1 GHz	650	614	620	376	256	243	**191**
9.3 GHz	606	589	587	335	196	**177**	Invalid
10.4 GHz	598	579	570	338	**177**	Invalid	
11.4 GHz	543	540	530	**284**	Invalid		
12.5 GHz	396	346	**300**	Invalid			
13.6 GHz	262	**218**	Invalid				
14.7 GHz	**164**	Invalid					

表 6-7. Typical Calibration Times (µs) for f_{OSC} = 100MHz and f_{PD} = 200MHz

f_{VCO}	VCO_SEL(1)						
	VCO7	VCO6	VCO5	VCO4	VCO3	VCO2	VCO1
8.1 GHz	854	828	822	579	451	437	**393**
9.3 GHz	819	800	794	551	401	**380**	Invalid
10.4 GHz	808	786	781	551	**388**	Invalid	
11.4 GHz	767	745	743	**494**	Invalid		
12.5 GHz	603	560	**513**	Invalid			
13.6 GHz	469	**426**	Invalid				
14.7 GHz	**385**	Invalid					

(1) Based on VCO_SEL. This include Analog lock time for typical loop bandwidth.

6.3.7.2 Watchdog Feature

The watchdog feature is used to the scenario when radiation during VCO calibration from causes the VCO calibration to fail. When this feature is enabled, the watchdog timer runs during VCO calibration. If this timer runs out before the VCO calibration is finished, then the VCO calibration is restarted. The WD_DLY word sets how many times this calibration can be restarted by the watchdog feature.

6.3.7.3 RECAL Feature

The RECAL feature is used to mitigate the scenario when the VCO is in lock, but then radiation causes the VCO to go out of lock. When the RECAL_EN pin is high, if the PLL loses lock and stays out of lock for a time specified by the LD_DLY word, then triggers a VCO re-calibration.

ADVANCE INFORMATION

6.3.7.4 Determining the VCO Gain

The VCO gain can vary based on core, and this can vary over temperature and process. Table 表 6-8 provides a rough guideline of expected VCO gain values based on the VCO core.

表 6-8. VCO Gain

f1	f2	Kvco1	Kvco2
7500	8600	73	112
8600	9900	84	136
9900	10800	102	140
10800	11900	115	162
11900	13000	167	224
13000	14000	182	228
14000	15000	218	254

6.3.8 Channel Divider

To go below the VCO lower bound of 7500MHz, the channel divider can be used. The channel divider consists of six segments, and the total division value is equal to the multiplication of them. Therefore, not all values are valid.

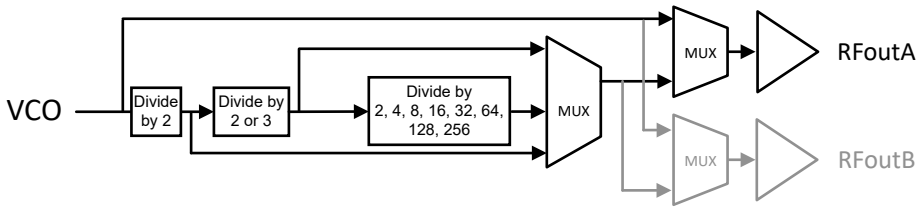

図 6-2. Channel Divider

When the channel divider is used, there are limitations on the values. 表 6-9 shows how these values are implemented.

ADVANCE INFORMATION

表 6-9. Channel Divider Segments

EQUIVALENT DIVISION VALUE	FREQUENCY LIMITATION	OutMin (MHz)	OutMax (MHz)	CHDIV[4:0]
2	None	3750	7500	1
4		1875	3750	2
6	f_{VCO} ≤ 12GHz	1250	2000	
8		937.5	1500	4
12		625	1000	5
16		468.75	750	6
24		312.5	500	7
32		234.375	375	8
48		156.25	250	9
64		117.1875	187.5	10
96		78.125	125	11
128		58.59375	93.75	12
192		39.0625	62.5	13
256		29.296875	46.875	14
384		19.53125	31.25	15
512		14.6484375	23.4375	16
768		9.765625	15.625	17
1024		7.32421875	11.71875	18
1536		4.8828125	7.8125	19

The channel divider is powered up whenever an output (OUTMUXx) is selected to the channel divider or SysRef, regardless of whether the output is powered down or not. When an output is not used, TI recommends selecting the VCO output to verify that the channel divider is not unnecessarily powered up.

表 6-10. Channel Divider

RFOUTA	RFOUTB	CHANNEL DIVIDER (CDIV) Status
Channel Divider	Channel Divider	Powered up
Channel Divider	VCO	Powered up
VCO	Channel Divider	Powered up
Doubler	Channel Divider	Powered up
VCO	VCO	Powered down
VCO	Doubler	Powered down
Doubler	VCO	Powered down
Doubler	Doubler	Powered down

6.3.9 Output Mute Pin and Ping Pong Approaches

The output buffer can be muted or unmuted using the MUTE pin. The polarity of this pin is programmable with the PINMUTE_POL bit in SPI mode. When the output is muted, the PLL stays in lock, so this can be used to combine multiple synthesizers for faster lock time. The PLL with the muted output can be accepting programming commands or even locking to a new frequency. As the output is muted, the unwanted signal is greatly attenuated and can be further attenuated with an external RF switch.

MuteA and MuteB pins are provided to Mute RFOUTA and RFOUTB independently. While One output is Muted, other output can be operated normally. MuteA and MuteB pins works in both Pin Mode as well as SPI mode. In SPI mode, MuteA and MuteB operation can be set to operate either through register settings or through MuteA and MuteB pins.

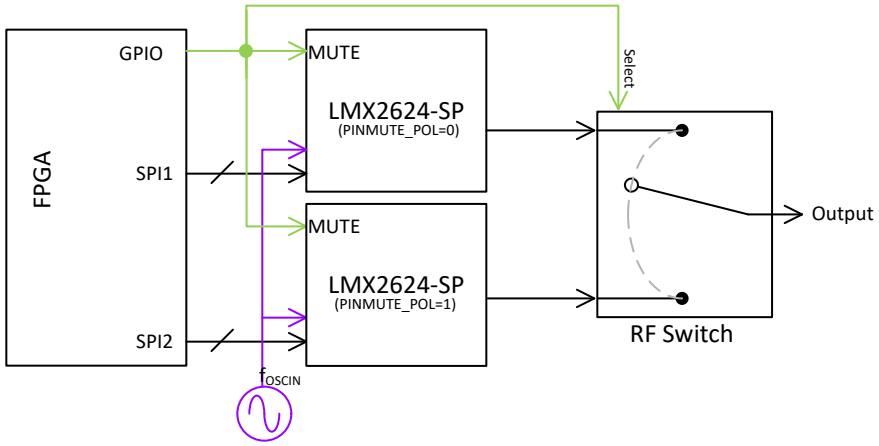

図 6-3. Output Mute implementation Using Two LMX2624-SP devices

6.3.10 Output Frequency Doubler

The frequency doubler is used to produce an output frequency that is twice the VCO frequency at RFOUTA and at RFOUTB based on OUTMUX2, OUTMUX1 and OUTMUX0 settings. When the VCO frequency is doubled, the fundamental (non-doubled) VCO frequency does leak to the output and this is the sub-harmonic (0.5X). To minimize these sub-harmonics, there is tunable filter that tracks the output frequency and filters out this sub-harmonic as well as other undesired harmonics (1.5X, 2X, 3X, ...). The calibration for this tunable filter is automatically triggered whenever the VCO calibration is done.

6.3.11 Output Buffer

The RF output buffer has internal 50 terms termination. The output power can be programmed to various levels or disabled while still keeping the PLL in lock.

OUTBUFFA and OUTBUFFB registers can be programed to increase or decrease the output buffer power level. There are 8 settings starting from 0 to 7 where 0 is for minimum power and 7 is for maximum power setting. During power on, default setting is 7.

6.3.12 Power-Down Modes

The LMX2624-SP can be powered up and down using the POWERDOWN bit or CAL pin. Setting the POWERDOWN bit to one or making the CAL pin to LOW moves the device to power down mode. To bring the device back to normal operation, either set the POWERDOWN bit to zero or pull back CAL Pin HIGH (if the device is powered down by CAL Pin). Register R0 must be programmed with FCAL_EN high again to re-calibrate the device.

6.3.13 Pin-Mode Integer Frequency Generation

The LMX2624-SP has Pin-mode option to generate fixed frequency output with out any serial programming. The output frequency is generated based on the Pin setting in the Pin-mode option. The Integer N divider and Channel Divider can be set using the Pin-mode options.

A few rules of operation for these Pin-modes are as follows:

- Set the pin-mode using CDIVx pins. All pin combinations of CDVIx pins except when connected to GROUND is consider as Pin-mode. The SPI control can not be used in Pin-mode. If CDIV2, CDIV1, and CDIV0 are tied to GROUND, the device is in SPI-mode.
- The rise time for the supply needs to be <50 ms.
- Fractional Numerator and Denominator not available in Pin-mode. Only N divider is set using the NDIV setting
- CAL pin tied to VCC. When changing between Pin-mode frequency options, after the pins are changed, the CAL pin must be toggled.

ADVANCE INFORMATION

NDIVx and CDIVx pins are four level pins. Four level pins are used to get more number of division values with less number of pins which helps to reduce the overall package size. NDIVx has total of six pins and CDIVx has three pins. 6 pins of NDIVx (NDIV5, NDIV4, NDIV3, NDIV2, NDIV1, NDIV0) with four levels can create total of 4^6 combinations, which means 4096 values. Similarly CDIVx (CDIV2, CDIV1, CDIV0) with four level pins have total of 4^3 = 64 combinations. Due to the four level pins, 9 pins are sufficient instead of 18 pins for two level pins. The four levels of pin are VL, VML, VMH and VH as shows in 図 6-4. Use three 10-kΩ resistors across VCC and GROUND which have four levels including VCC, GROUND and two mid levels called VMH (Voltage Mid High) and VML (Voltage Mid Low).

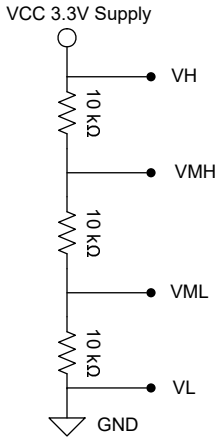

図 6-4. Four Level Pins Implementation

NDIVx provides total of 4096 integer divider options in Pin-mode. Numerator (NUM) and Denominator (DEN) is not available in Pin-mode for fractional PLL and is only possible through SPI-mode. The minimum value for N divider restriction for Pin-mode NDIVx values are similar to the SPI-mode option. Refer to 表 6-2 for the N divider minimum value setting.

All combinations of Channel Divider settings which are available in SPI-mode are also available in Pin-mode option using CDIVx pins. Refer to 表 6-11 for CDIVx settings in Pin-mode, CHDIV<4:0> settings in SPI-mode and the corresponding Channel Divider value. Based on the Channel Divider value needed, CDIV2, CDIV1, CDIV0 pins needed to be connected to one of the four levels.

表 6-11. CDIVx Pin-Mode Divider Values

CDIV2	CDIV1	CDIV0	CHDIV<4:0> EQUIVALENT IN SPI MODE	CHANNEL DIVIDER VALUE
VL	VL	VL	0	SPI mode
VL	VML	VL	1	2
VL	VMH	VL	2	4
VL	VMH	VH	3	6
VML	VL	VL	4	8
VML	VL	VH	5	12
VML	VML	VL	6	16
VML	VML	VH	7	24
VML	VMH	VL	8	32
VML	VMH	VH	9	48
VML	VH	VL	10	64
VML	VH	VH	11	96
VMH	VL	VL	12	128
VMH	VL	VH	13	192

表 6-11. CDIVx Pin-Mode Divider Values (続き)

CDIV2	CDIV1	CDIV0	CHDIV<4:0> EQUIVALENT IN SPI MODE	CHANNEL DIVIDER VALUE
VMH	VML	VL	14	256
VMH	VML	VH	15	384
VMH	VMH	VL	16	512
VMH	VMH	VH	17	768
VMH	VH	VL	18	1024
VMH	VH	VH	19	1536

OUTMUX2, OUTMUX1 and OUTMUX0 pins are used to select the RFOUTx based on 表 6-12.

表 6-12. OUTMUX Settings

OUTMUX2	OUTMUX1	OUTMUX0	RFOUTA OUTPUT	RFOUTB OUTPUT
0	0	0	Channel Divider	Channel Divider
0	0	1	Channel Divider	VCO
0	1	0	VCO	Channel Divider
0	1	1	VCO	VCO
1	0	0	Doubler	Channel Divider
1	0	1	VCO	Doubler
1	1	0	Doubler	VCO
1	1	1	Doubler	Doubler

Example Frequency Generation in Pin-mode:

Requirements:

RFOUTAx RF output frequency = 21000 MHz

Only one RF output required; No SYSREF.

Reference Input (OSCIN) frequency = 50 MHz

Mode required: Pin-mode; No software or SPI control available in the actual sub-system implementation.

For generating 21000 MHz, Doubler output needed at the output. The configuration is as below:

CDIVx pins need to be configured value other than GND. For example, connect CDIV2, CDIV1 and CDIV0 to VCC (All '1's).

OUTMUX2 = 1, OUTMUX1 = 1, OUTMUX0 = 0 (RFOUTA is configured for Doubler output).

MuteB is connected to GND for Muting the VCO path on RFOUTB.

REF_DBLR_EN is connected to VCC in this configuration for having the PFD to 100 MHz. The OSCIN 50 MHz is doubled using this input doubler to improve the phase noise performance.

VCO frequency = 10500 MHz for generating 21000 MHz after Doubler. NDIV value needs to be 10500 / 100 = 105. Connect NDIV5, NDIV4, NDIV3, NDIV2, NDIV1, NID0 pins to the resistor network equivalent to 105 value.

Convert decimal 105 into equivalent base 4 value for generating the configuration for NDIV pins.

$(105)_{10} = (001221)_4$.

The NDIVx pins need to be connected to VL, VL, VML, VMH, VMH, VML respectively using the resistor network.

MuteA and MuteB pins are available in Pin-mode and can be used as required for Mute and Unmute.

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Refer to Unused pins treatment table for configuring the connections for unused pins.

Driving 4-level Pins Using GPIOs:

Previous section described on creating VL, VML, VMH and VH levels using resistor network. This arrangement is sufficient if the RFOUTx frequency is fixed. For applications that require changes of frequency using pin-mode options, the NDIVx and CDIVx pins levels need to be changed as per the output frequency requirement. One option is to drive these 4-level pins using low speed precision DACs to create these four voltage levels which is complex.

Following arrangement can help in driving 4-level using GPIOs. See 表 6-13.

表 6-13. Driving 4-level Pins Using GPIOs in Pin-mode

NxB	NxA	Nx	Voltage level at Nx Pin
VL	VL	VL	0
VL	VH	VML	VH/3
VH	VL	VMH	2* VH/3
VH	VH	VH	VH

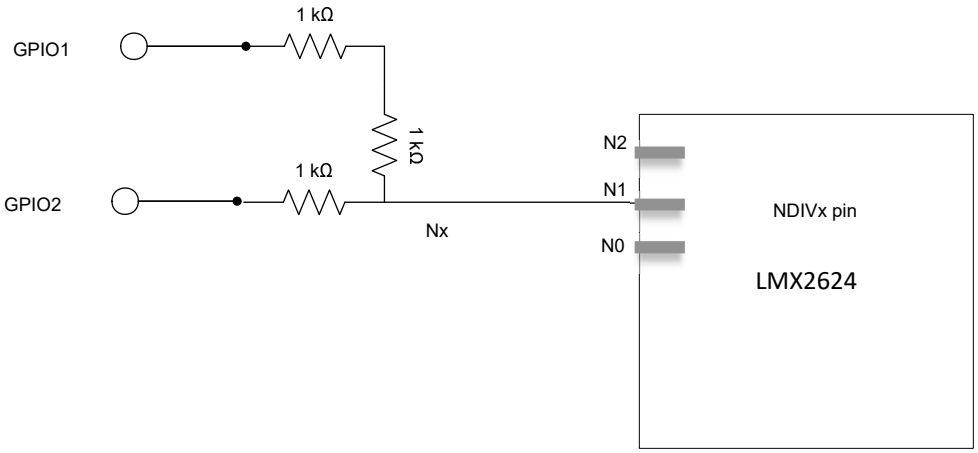

図 6-5. Driving 4 Level Pins Using GPIOs

The arrangement in 図 6-5 needs to be created for which NDIVx and CDIVx pins need to be updated based on the output frequency requirement.

6.3.14 Treatment of Unused Pins

This device has several pins for many features and there is a preferred way to treat these pins if not needed. For the input pins, a series resistor is recommend but can be directly shorted.

表 6-14. Recommended Treatment of Pins

Pins	SPI Mode	Pin Mode	Recommended Treatment if NOT Used
CDIV0, CDIV1, CDIV2	Always used	Always Used	SPI-mode: CDIV0, CDIV1, CDIV2 pins must be GND with 1 kΩ resistor. Pin-mode: CDIV0, CDVI1, CDVI2 pins must have value other than the GND for all pins at a time. Based on the value on these pins, output Divider is set.
NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5	Never used	Always Used	GND with 1 kΩ
CAL	Never Used	Sometimes Used	VCC with 1 kΩ
SYNC, SysRefReq	Sometimes Used	Never Used	GND with 1 kΩ

表 6-14. Recommended Treatment of Pins (続き)

Pins	SPI Mode	Pin Mode	Recommended Treatment if NOT Used
OSCinP,OSCinM	Always Used	Always Used	GND with 50 Ω to ground after the AC-coupling capacitor. If one side of complimentary side is used and other side is not, impedance looking out must be similar for both of these pins.
SCK, SDI	Always Used	Never Used	GND with 1 kΩ
CSB	Always Used	Never Used	VCC with 1 kΩ
RECAL_EN	Sometimes Used	Sometimes Used	Internally pulled to VCC with 200 kΩ. When RECAL function is not used, GND with 1kΩ.
RFoutAP, RFoutAM, RFoutBP, RFoutBM	Sometimes Used	Sometimes Used	If both of the differential output pins are unused, the pins can be left floating and power down using SPI-mode or Mute the pins using Pin-mode options. If only one side of complimentary output is used, connect the unused pin to GND with 50 Ω through AC coupling capacitor.
OUTMUX2, OUTMUX1, OUTMUX0	Sometimes Used	Always used	GND with 1 kΩ
REF_DBLR_EN	Never used	Some times used	GND with 1 kΩ
MuteA, MuteB	Sometimes used	Always used	GND with 1 kΩ

6.3.15 Phase Synchronization

6.3.15.1 General Concept

The SYNC pin allows one to synchronize the LMX2624-SP such that the delay from the rising edge of the OSCin signal to the output signal is deterministic. Initially, the devices are locked to the input, but are not synchronized. The user sends a synchronization pulse that is reclocked to the next rising edge of the OSCin pulse. After a given time, t_1, the phase relationship from OSCin to f_{OUT} is deterministic. This time is dominated by the sum of the VCO calibration time, the analog setting time of the PLL loop, and the MASH_RST_CNT if used in fractional mode.

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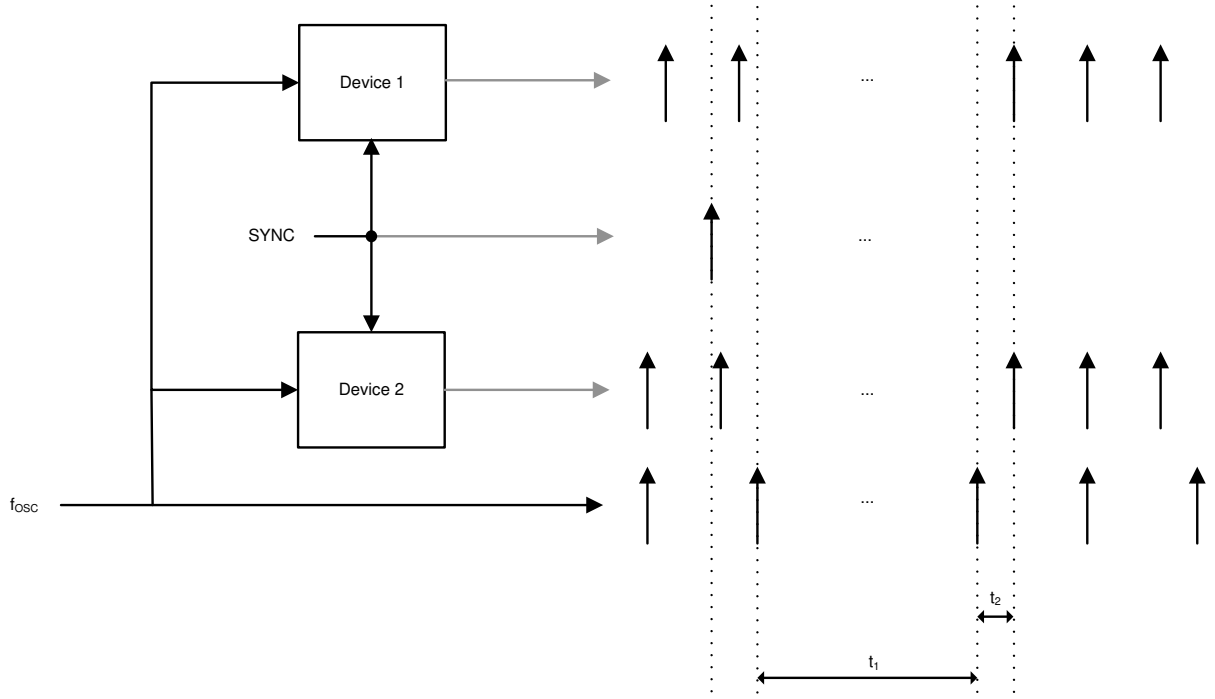

図 6-6. Devices Are Now Synchronized to OSCin Signal

When the SYNC feature is enabled, part of the channel divide can be included in the feedback path.

表 6-15. IncludedDivide With VCO_PHASE_SYNC = 1

OUTx_MUX	CHANNEL DIVIDER	IncludedDivide
OUTBUFFA_MUXSEL=1 or 2 and OUTBUFFB_MUXSEL = 1 or 2	Don't Care	1
All Other Valid Conditions	Divisible by 3	6
	All other values	4

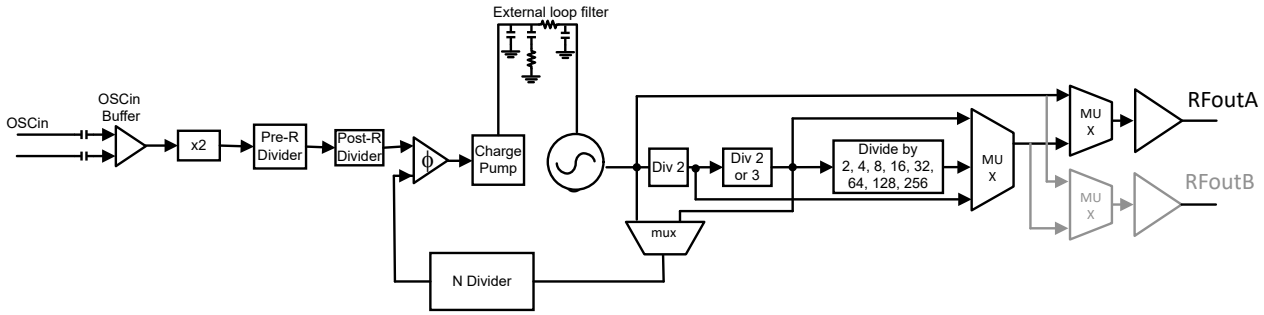

図 6-7. Phase SYNC Diagram

6.3.15.2 Categories of Applications for SYNC

The requirements for SYNC depend on certain setup conditions. In cases that the SYNC is not timing critical, the SYNC can be done through software by toggling the VCO_PHASE_SYNC bit from 0 to 1. 図 6-8 provides the different categories. When timing is critical, then SYNC must be done through the pin and the setup and hold times for the OSCin pin are critical. For timing critical sync (Category 3) ONLY, adhere to the following guidelines.

表 6-16. SYNC Pin Timing Characteristics for Category 3 SYNC

Parameter	Description	Min	Max	Unit
f_{OSC}	Input reference Frequency		40	MHz
t_{SETUP}	Setup time between SYNC and OSCin rising edges	2.5		ns
t_{HOLD}	Hold time between SYNC and OSCin rising edges	2.5		ns

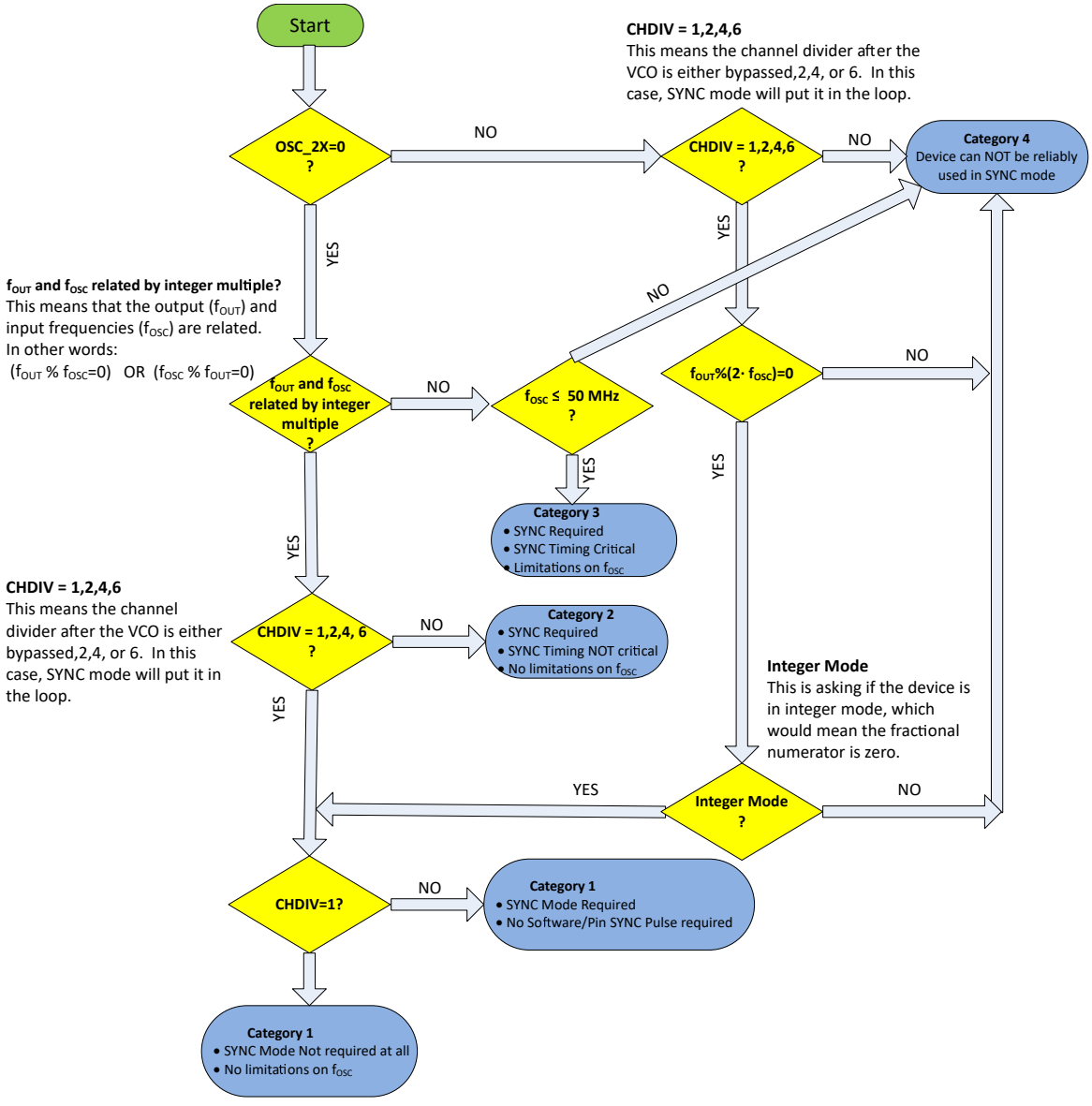

図 6-8. Determining the SYNC Category

6.3.15.3 Procedure for Using SYNC

This procedure must be used to put the device in SYNC mode.

1. Use the flowchart to determine the SYNC category.
2. Make determinations for OSCin and using SYNC based on the category
   a. If Category 4, SYNC cannot be performed in this setup.
   b. If category 3, verify that the maximum f_{OSC} frequency for SYNC is not violated and there are hardware accommodations to use the SYNC pin.
3. If the channel divide is used, determine the included channel divide value which is 2 × SEG1 of the channel divide:
   a. If OUTBUFFA_MUXSEL is not channel divider and OUTBUFFB_MUXSEL is not channel divider or SysRef, then IncludedDivide = 1.
   b. Otherwise, IncludedDivide = 6. In the case that the channel divider is 2, then IncludedDivide=4.
4. If not done already, divide the N divider and fractional values by the included channel divide to account for the included channel divide.
5. Program the device with the VCO_PHASE_SYNC = 1. Note that this does not count as applying a SYNC to device (for category 2).
6. Apply the SYNC, if required
   a. If category 2, VCO_PHASE_SYNC can be toggled from 0 to 1. Alternatively, a rising edge can be sent to the SYNC pin and the timing of this is not critical.
   b. If category 3, the SYNC pin must be used, and the timing must be away from the rising edge of the OSCin signal.
7. MASH_RST_CNT needs to be changed (increased) with reduced PFD frequency by engaging reference dividers.

6.3.15.4 SYNC Input Pin

The SYNC input pin can be driven in CMOS. However, if not using SYNC mode (VCO_PHASE_SYNC = 0), then the INPIN_IGNORE bit must be set to one, otherwise the bit causes issues with lock detect. If the pin is desired for to be used and VCO_PHASE_SYNC=1, then set INPIN_IGNORE = 0.

6.3.16 Phase Adjust

The MASH_SEED word can use the sigma-delta modulator to shift output signal phase with respect to the input reference. If a SYNC pulse is sent (software or pin) or the MASH is reset with MASH_RST_N, then this phase shift is from the initial phase of zero. If the MASH_SEED word is written to, then this phase is added. PHASE_SYNC_EN bit needs to be made 1 to allow phase shift immediately with the change in MASH SEED. Without making PHASE_SYNC_EN=1, if mash seed is changed, output edge won't move. User needs to give a sync rising edge on sync pin. The phase shift is calculated as 式 5.

$$\text{Phase shift in degrees} = 360 \times (\text{MASH\_SEED} / \text{PLL\_DEN}) \times (\text{IncludedDivide/CHDIV}) \quad (5)$$

Example:

Mash seed = 1

Denominator = 12

Channel divider = 16

Phase shift (VCO_PHASE_SYNC=0) = 360 × (1/12) × (1/16) = 1.875 degrees

Phase Shift (VCO_PHASE_SYNC=1) = 360 × (1/12) × (4/16) = 7.5 degrees

There are several considerations when using MASH_SEED

- Phase shift can be done with a FRAC_NUM = 0, but MASH_ORDER must be greater than zero. For MASH_ORDER = 1, the phase shifting only occurs when MASH_SEED is a multiple of PLL_DEN.
- For the 2nd order modulator, PLL_N ≥ 45, for the 3rd order modulator, PLL_N ≥ 49, and for the fourth order modulator, PLL_N ≥ 54.

When using MASH_SEED in the case where IncludedDivide > 1, there are several additional considerations to get the phase shift to be monotonically increasing with MASH_SEED.

- Using the MASH_ORDER ≤ 2 is recommended.
- When using the 2nd order modulator for VCO frequencies below 10 GHz (when IncludedDivide = 6) or 9 GHz (when IncludedDivide = 4), increasing the PLL_N value much higher or changing to first order modulator can be necessary. When this use case is necessary depends on the VCO frequency, IncludedDivide, and PLL_N value.

6.3.17 Fine Adjustments for Phase Adjust and Phase SYNC

Phase SYNC refers to the process of getting the same phase relationship for every power up cycle and each time assuming that a given programming procedure is followed. However, there are some adjustments that can be made to get the most accurate results. As for the consistency of the phase SYNC, the only source of variation can be if the VCO calibration chooses a different VCO core and capacitor, which can introduce a bimodal distribution with about 10 ps of variation. If this 10 ps is not desirable, then the variation can be eliminated by reading back the VCO core, capcode, and DACISET values and forcing these values to provide the same calibration settings every time. The delay through the device varies from part to part and can be on the order of 60 ps. This part to part variation can be calibrated out with the MASH_SEED. The variation in delay through the device also changes on the order of +2.5 ps/°C, but devices on the same board likely have similar temperatures. In summary, the device can be made to have consistent delay through the part and there are means to adjust out any remaining errors with the MASH_SEED. This tends only to be an issue at higher output frequencies when the period is shorter.

6.3.18 SYSREF

The LMX2624-SP can generate a SYSREF output signal that is synchronized to f_{OUT} with a programmable delay. This output can be a single pulse, series of pulses, or a continuous stream of pulses. To use the SYSREF capability, the PLL must first be placed in SYNC mode with VCO_PHASE_SYNC_EN = 1.

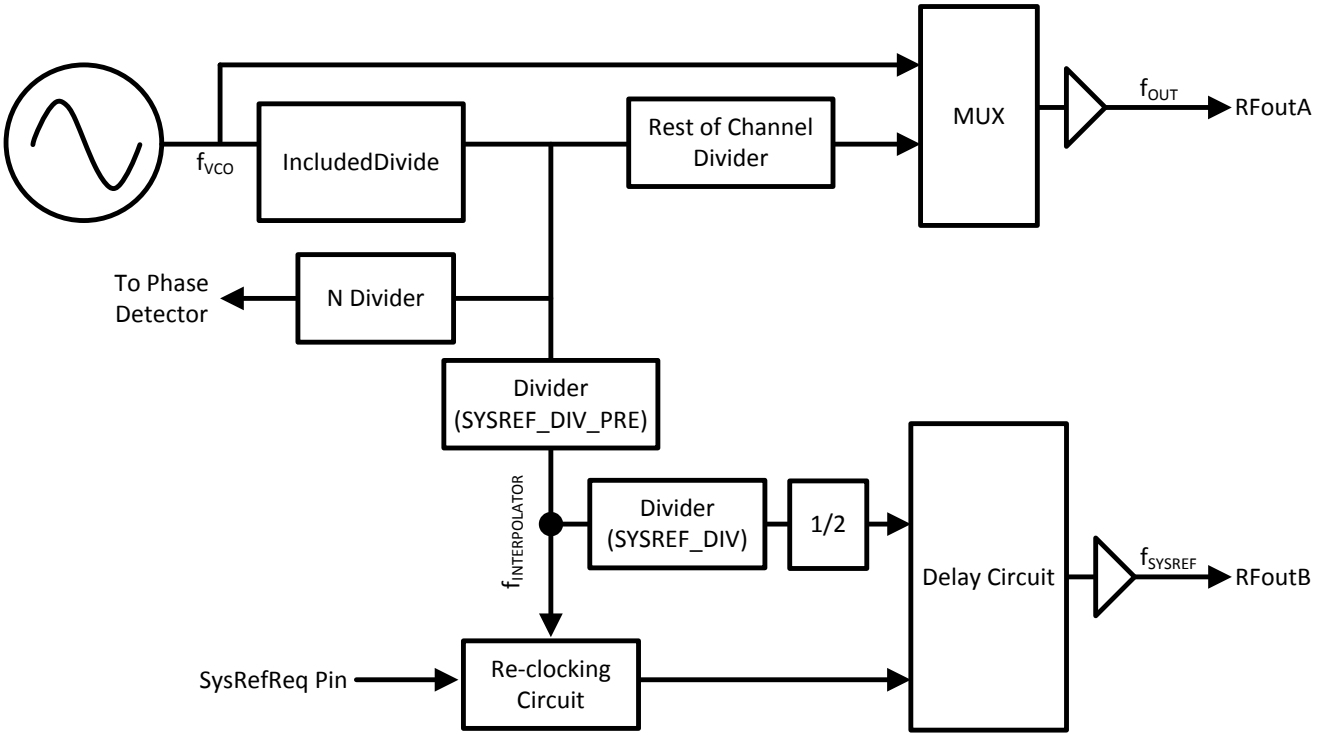

図 6-9. SYSREF Setup

As 図 6-9 shows, the SYSREF feature uses IncludedDivide and SYSREF_DIV_PRE divider to generate $f_{INTERPOLATOR}$. This frequency is used for re-clocking of the rising and falling edges at the SysRefReq pin. In SYSREF generation mode, the $f_{INTERPOLATOR}$ is further divided by 2×SYSREF_DIV to generate finite series or continuous stream of pulses.

表 6-17. SYSREF Setup

PARAMETER	MIN	TYP	MAX	UNIT
f_{VCO}	7500		15000	MHz
$f_{INTERPOLATOR}$	0.8		1.5	GHz
IncludedDivide		4 or 6		
SYSREF_DIV_PRE	1, 2, or 4			
SYSREF_DIV	4,6,8, ..., 4098			
$f_{INTERPOLATOR}$	$f_{PRESYSREF} = f_{VCO}$ /(IncludedDivide × SYSREF_DIV_PRE)			
f_{SYSREF}	$f_{SYSREF} = f_{INTERPOLATOR}$ / (2 × SYSREF_DIV)			
Delay step size		9		ps
Pulses for pulsed mode (SYSREF_PULSE_CNT)	0		15	n/a

The delay can be programmed using the JESD_DAC1_CTRL, JESD_DAC2_CTRL, JESD_DAC3_CTRL, and JESD_DAC4_CTRL fields. By concatenating these fields into a larger word called "SYSREFPHASESHIFT", the relative delay can be found. The sum of these words must always be 63.

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表 6-18. SysRef Delay

SYSREFPHASESHIFT	DELAY	JESD_DAC1	JESD_DAC2	JESD_DAC3	JESD_DAC4
0	Minimum	36	27	0	0
...				0	0
36		0	63	0	0
37		0	62	1	0
...					
99		0	0	63	0
100		0	0	62	1
...					
161		0	0	1	62
162		0	0	0	63
163		1	0	0	62
225		63	0	0	0
226		62	1	0	0
247	Maximum	41	22	0	0
> 247	Invalid	Invalid	Invalid	Invalid	Invalid

6.3.18.1 Programmable Fields

表 6-19 has the programmable fields for the SYSREF functionality.

表 6-19. SYSREF Programming Fields

FIELD	PROGRAMMING	DEFAULT	DESCRIPTION
SYSREF_EN	0 = Disabled 1 = enabled	0	Enables the SYSREF mode. SYSREF_EN must be 1 if and only if OUTB_MUX=2 (SysRef)
SYSREF_DIV_PRE	1: DIV1 2: DIV2 4: DIV4 Other states: invalid		The output of this divider is the $f_{INTERPOLATOR}$.
SYSREF_REPEAT	0 = SYSREF generation mode 1 = SYREF repeater mode	0	In SYSREF generation mode, the device creates a series of SYSREF pulses. In repeater mode, SYSREF pulses are generated with the SysRefReq pin.
SYSREF_PULSE	0 = Continuous mode 1 = Pulsed mode	0	Continuous mode continuously makes SYSREF pulses, where pulsed mode makes a series of SYSREF_PULSE_CNT pulses
SYSREF_PULSE_CNT	0 to 15	4	In the case of using pulsed mode, this is the number of pulses. Setting this to zero is an allowable, but not practical state.
SYSREF_DIV	0: Divide by 4 1: Divide by 6 2: Divide by 8 ... 2047: Divide by 4098	0	The SYSREF frequency is at the VCO frequency divided by this value.

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6.3.18.2 Input and Output Pin Formats

6.3.18.2.1 SYSREF Output Format

The SYSREF output comes in differential format through RFoutB. This has a minimum voltage of about 2.3 V and a maximum of 3.3 V. If DC coupling can not be used, there are two strategies for AC coupling.

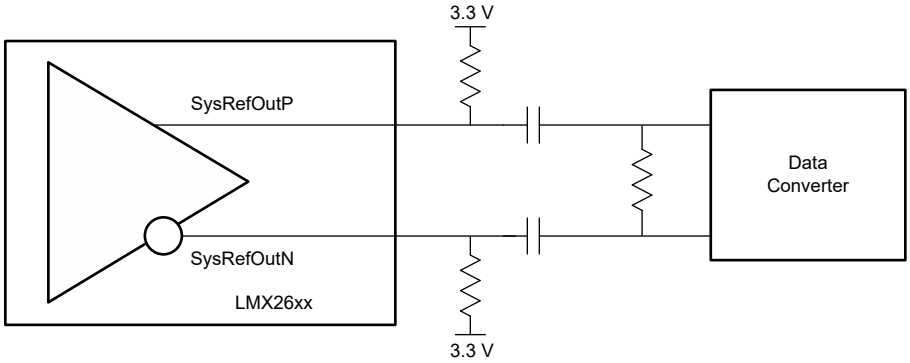

図 6-10. SYSREF Output

1. Send a series of pulses to establish a DC-bias level across the AC-coupling capacitor.
2. Establish a bias voltage at the data converter that is below the threshold voltage by using a resistive divider.

6.3.18.3 Examples

The SysRef can be used in a repeater mode, which just echos the input, after being re-clocked to the $f_{INTERPOLATOR}$ frequency and then RFout, or SysRef can be used in a repeater. In repeater mode, SysRef can repeat 1, 2, 4, 8, or infinite (continuous) pulses. The frequency for repeater mode is equal to the RFout frequency divided by the SYSREF divider.

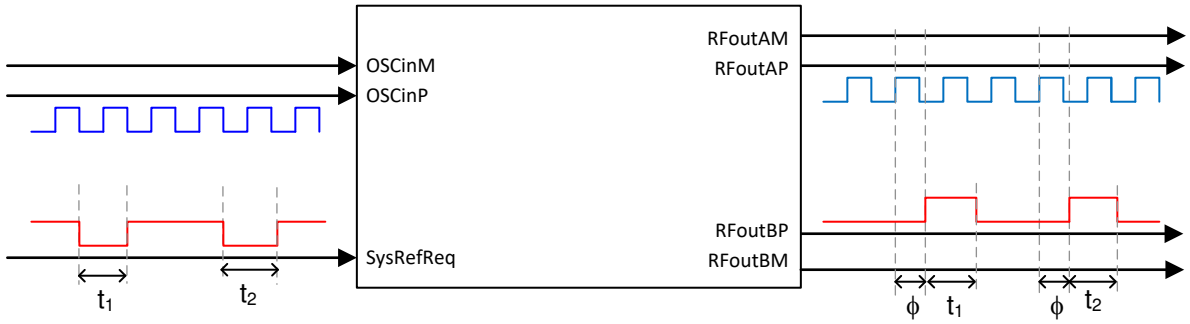

図 6-11. SYSREF Out In Repeater Mode

In SYSREF generation mode, the SysRefReq pin is pulled high to allow the SysRef output.

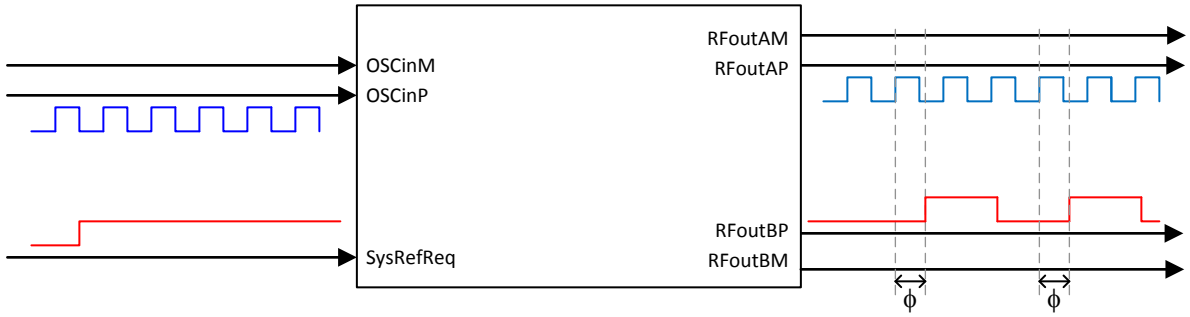

図 6-12. Figure 1. SYSREF Out In Pulsed/Continuous Mode

6.3.18.4 SYSREF Procedure

To use SYSREF, do the these steps:

1. Put the device in SYNC mode using the procedure already outlined.
2. Find out IncludedDivide in the same way SYNC mode is done.
3. Calculate the SYSREF_DIV_PRE value such that the interpolator frequency ($f_{INTERPOLATOR}$) is in the range of 800MHz to 1500MHz. $f_{INTERPOLATOR} = f_{VCO}$/IncludedDivide/SYSREF_DIV_PRE. Make this frequency a multiple of f_{OSC} if possible.
4. If using SYSREF generation mode (SYSREF_REPEAT = 0), verify that SysRefReq pin is high, verify that the SysRefReq pin is high.
5. If using SYSREF repeater mode (SYSREF_REPEAT = 1), set up the pulse count if desired. Pulses are created by toggling the SysRefReq pin.
6. Adjust the delay between the RFoutA and RFoutB signal using the JESD_DACx_CTL fields.

6.4 Device Functional Modes

表 6-20. Device Functional Modes

MODE	DESCRIPTION	SOFTWARE SETTINGS
RESET	Registers are held in the reset state. This device does have a power on reset, but good practice is to also do a software reset if there is any possibility of noise on the programming lines, especially if there is sharing with other devices. Also realize that there are registers not disclosed in the data sheet that are reset as well.	RESET = 1 POWERDOWN = 0
POWERDOWN	Device is powered down.	POWERDOWN = 1 or CAL Pin = Low
Pin-mode	Device settings are determined by pin states on CDIV.	Any one of the CDIV0, CDIV1, CDIV2 pins has value other than LOW
Normal operating mode	This is used with at least one output on as a frequency synthesizer and the device can be controlled through the SPI	All CDIV pins needs to be LOW
SYNC mode	This is used where part of the channel divider is in the feedback path to provide deterministic phase.	VCO_PHASE_SYNC = 1
SYSREF mode	In this mode, RFoutB is used to generate pulses for SYSREF.	VCO_PHASE_SYNC =1, SYSREF_EN = 1

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6.5 Programming

When not in pin mode, the LMX2624-SP is programmed using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W bit, 0 is for write, and 1 is for read. The address field ADDRESS[6:0] is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When CSB goes high, data is transferred from the data field into the selected register bank. See 図 5-1 for timing details.

6.5.1 Recommended Initial Power-Up Sequence

For the most reliable programming, TI recommends this procedure:

1. Apply power to device.
2. Program RESET = 1 to reset registers.
3. Program RESET = 0 to remove reset.
4. Program registers as shown in the register map in REVERSE order from highest to lowest.
   - Programming of registers R79 down to R0 (with FCAL_EN = 1) is required. Registers in this range that are only 1s and 0s must also be programmed in accordance to the register map. Do NOT assume that the power on reset state and the recommended value are the same. The register descriptions also list a "Reset" value. This value is actually the recommended value that must match the main register map table and is not necessarily the power on reset value.
5. Wait 10 ms
6. Program register R0 one additional time with FCAL_EN = 1 to verify that the VCO calibration runs from a stable state.

6.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. Change the N divider value.
2. Program the PLL numerator and denominator.
3. Program FCAL_EN (R0[3]) = 1.

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7 Register Maps

7.1 Device Registers

表 7-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in 表 7-1 must be considered as reserved locations and the register contents must not be modified.

表 7-1. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	R0		セクション 7.1.1
1h	R1		セクション 7.1.2
2h	R2		セクション 7.1.3
3h	R3		セクション 7.1.4
4h	R4		セクション 7.1.5
5h	R5		セクション 7.1.6
6h	R6		セクション 7.1.7
7h	R7		セクション 7.1.8
8h	R8		セクション 7.1.9
9h	R9		セクション 7.1.10
Ah	R10		セクション 7.1.11
Bh	R11		セクション 7.1.12
Ch	R12		セクション 7.1.13
Dh	R13		セクション 7.1.14
Eh	R14		セクション 7.1.15
Fh	R15		セクション 7.1.16
10h	R16		セクション 7.1.17
11h	R17		セクション 7.1.18
12h	R18		セクション 7.1.19
13h	R19		セクション 7.1.20
14h	R20		セクション 7.1.21
16h	R22		セクション 7.1.22
17h	R23		セクション 7.1.23
1Eh	R30		セクション 7.1.24
1Fh	R31		セクション 7.1.25
20h	R32		セクション 7.1.26
22h	R34		セクション 7.1.27
23h	R35		セクション 7.1.28
4Fh	R79		セクション 7.1.29

Complex bit access types are encoded to fit into small table cells. 表 7-2 shows the codes that are used for access types in this section.

表 7-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

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表 7-2. Device Access Type Codes (続き)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 R0 Register (Offset = 0h) [Reset = B3CCh]

R0 is shown in 表 7-3.

Return to the Summary Table.

表 7-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	No description
14	VCO_PHASE_SYNC_EN	R/W	0h	Phase sync enable. Rising edge on Phase Sync pin triggers Phase Sync
13	DBLR_ACAL_EN	R/W	1h	Enables Doubler Amplitude calibration 0h = Double
12	DBLR_FCAL_EN	R/W	1h	Enables Doubler Frequency calibration 0h = Double calibration is disabled 1h = Enables doubler calibration (reg0 write)
11	ADR_HOLD	R/W	0h	Holds the address for SPI block Read/Write. 0h = Address is determined by ascend 1h = Address is determined by hold (Has priority over ascend)
10	ASCEND	R/W	0h	Direction of register update for SPI block write 0h = Address Descending 1h = Address Ascending
9-8	OPBUF_MUTE	R/W	3h	For unmuting channel A or B during calibration 0h = RFOUTB is not muted during FCAL 1h = RFOUTB is muted during FCAL
7-6	FCAL_SHIFT_LEFT	R/W	3h	Reduce the Nb4R, Rb4N (calibration)frequency by $2^{FCAL\_SHIFT\_LEFT}$. Can be set according to PFD frequency (Fpd) 0h = Fpd ≤ 100MHz 1h = 100MHz < Fpd ≤ 150MHz 2h = 150MHz < Fpd ≤ 200MHz 3h = Fpd > 200MHz
5-4	FCAL_SHIFT_RIGHT	R/W	0h	Increase the Nb4R, Rb4N (calibration) frequency by $2^{FCAL\_SHIFT\_RIGHT}$ during frequency calibration. [Valid if PostR : $k*2^{FCAL\_SHIFT\_RIGHT}$] Can be set according to PFD frequency (Fpd) 0h = Fpd ≥ 10MHz 1h = 5MHz ≥Fpd< 10MHz 2h = 2.5MHz ≥Fpd< 5MHz 3h = Fpd< 2.5MHz
3	ACAL_EN	R/W	1h	Enables Amplitude calibration. This takes place only during frequency calibration 0h = No amplitude calibration 1h = Amplitude calibration along with frequency calibration
2	FCAL_EN	R/W	1h	Writing reg0 with this bit enabled as 1 triggers VCO frequency calibration 0h = Reg0 write does not trigger calibration 1h = Reg0 write triggers frequency calibration
1	RESET	R/W	0h	Reset all registers to default value 0h = Normal operation 1h = Writing 1, triggers reset. This register self returns to 0, but in TICSPro you have to write a 0 to return the register to default

表 7-3. R0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	POWERDOWN	R/W	0h	Power down the device 0h = Normal Operation 1h = Device power down

7.1.2 R1 Register (Offset = 1h) [Reset = 10CBh]

R1 is shown in 表 7-4.

Return to the Summary Table.

表 7-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.
14	PH_SYNC_EN	R/W	0h	Enable signal for fine tuning output delay through MASh seed 0h = Disable 1h = Enable
13	GLOBAL_READBACK	R/W	0h	Register readback control 0h = reads the written register values 1h = reads the state machine value of AS registers
12	LD_LOCK_EN	R/W	1h	Lock Detect Type. VCOCal lock detect asserts a high output after the VCO has finished calibration and the LD_DLY timeout counter is finished. Vtune and VCOCal lock detect asserts a high output when VCOCal lock detect asserts a signal and the tuning voltage to the VCO is within acceptable limits (continuous monitoring of Vtune voltage). 0h = VCOCal Lock Detect 1h = VCOCal and Vtune Lock Detect
11	MUTEB_POLARITY	R/W	0h	Selects if MUTEB pin is active high or active low. 0h = Mutes when pin is high 1h = Mutes when pin is low
10	MUTEA_POLARITY	R/W	0h	Selects if MUTEA pin is active high or active low. MUTEA polarity 0h = Mutes when pin is high 1h = Mutes when pin is low
9	MUTEB_SEL	R/W	0h	Select if Path B is to be muted through pin or register. 0h = pin 1h = register
8	MUTEA_SEL	R/W	0h	Select if Path A is to be muted through pin or register. 0h = pin 1h = register
7	OUTBUFFB_MUTE	R/W	1h	Mutes path B 0h = RFOUTB is not muted 1h = RFOUTB is muted
6	OUTBUFFA_MUTE	R/W	1h	Mutes path A 0h = RFOUTA is not muted 1h = RFOUTA is muted
5	OUTBUFFB_PD	R/W	0h	Powering down Path B output buffer 0h = OUTBUFFB is powered on 1h = OUTBUFFB is powered off
4	OUTBUFFA_PD	R/W	0h	Powering down Path A output buffer 0h = OUTBUFFA is powered on 1h = OUTBUFFA is powered off
3	DBLR_PD	R/W	1h	Powering down doubler 0h = Doubler is powered on 1h = Doubler is powered off

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表 7-4. R1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2-0	SMCLK_DIV	R/W	3h	Digital clock is derived from OSC_IN clock which can go up to 800MHz. This register is used to restrict the clock input to digital to maximum accept able frequency of SM_CLK = 50MHz SM_CLK = OSCIN clock/(2^<SM_CLK_DIV>) 0h = /1 (for OSCIN ≤ 50MHz) 1h = /2 (for OSCIN ≤ 100MHz) /2 2h = /4 (for OSCIN ≤ 200MHz) 3h = /8 (for OSCIN ≤ 400MHz) 4h = /16 (for OSCIN ≤ 800MHz) 5h = /32 (OSCIN ≥ 800MHz)

7.1.3 R2 Register (Offset = 2h) [Reset = 0F3Fh]

R2 is shown in 表 7-5.

Return to the Summary Table.

表 7-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	UNDISCLOSED	R/W	1h	Program this field to 0x1.
10-6	CP2P5V_IUP	R/W	1Ch	Charge pump gain (UP) 0h = Unused 1h = Unused 2h = 3mA 3h = 3mA 4h = 1.5mA
5-3	OUTBUFFB_DACCTRL	R/W	7h	Control current (daccode) in final stage of OUTBUFFB 0h = 2.5mA 1h = 5mA 2h = 7.5mA 3h = 10mA 4h = 12.5mA 5h = 15mA 6h = 17.5mA 7h = 20mA
2-0	OUTBUFFA_DACCTRL	R/W	7h	Control current (daccode) in final stage of OUTBUFFA 0h = 2.5mA 1h = 5mA 2h = 7.5mA 3h = 10mA 4h = 12.5mA 5h = 15mA 6h = 17.5mA 7h = 20mA

7.1.4 R3 Register (Offset = 3h) [Reset = 5040h]

R3 is shown in 表 7-6.

Return to the Summary Table.

表 7-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	OUTBUFFB_MUXSEL	R/W	1h	Selects OUTBUFFB configuration 0h = CHDIV 1h = VCO 2h = Invalid 3h = SYSREF
13-12	OUTBUFFA_MUXSEL	R/W	1h	Selects OUTBUFFA configuration 0h = CHDIV 1h = VCO 2h = DBLR 3h = Invalid
11	OUTMUX_PIN_CTRL	R/W	0h	Decides whether OUTMUX selection needs to be controlled through OUTMUX pins or OUTBUFFA/B_MUXSEL 0h = Controlled through pin 1h = Controlled through register
10-5	PFD_DLY	R/W	2h	Programmable phase detector delay. This must be programmed based on VCO frequency, fractional order, and N divider value DLY = (PFD_DLY_SEL + 3)*4*VCO_cycle 0h = Don't use PFD_DLY_SEL 1h = 16 VCO cycles 2h = 20 VCO cycles 3h = 24 VCO cycles 4h = ... 3Fh = 264 VCO cycles
4-0	CHDIV	R/W	0h	Channel divider (Equivalent Division) controls divider value of each segment of the channel divider 0h = NA 1h = /2 2h = /4 3h = /6 4h = /8 5h = /12 6h = /8 7h = /24 8h = /32 9h = /48 Ah = /64 Bh = /96 Ch = /128 Dh = /192 Eh = /256 Fh = /384 10h = /512 11h = /768 12h = /1024 13h = /1536

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7.1.5 R4 Register (Offset = 4h) [Reset = 0710h]

R4 is shown in 表 7-7.

Return to the Summary Table.

表 7-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.
14	VCO_CAPCTRL_FORCE	R/W	0h	Allows forcing the VCO capcode value by manually programming the VCO_CAPCTRL register
13	VCO_IDAC_FORCE	R/W	0h	Allows forcing the VCODACISET to the value programmed in VCODACISET register

表 7-7. R4 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
12	VCO_SEL_FORCE	R/W	0h	Allows forcing the VCO_SEL value to manually select the VCO
11	QUICK_STRT_EN	R/W	0h	Calibration starts with previous capcode (VCO_CAPCTRL), VCO (VCO_SEL) and idac code (VCODACISET) for quick calibration
10	FAST_ACAL_EN	R/W	1h	Fast acal enable 0h = FAST ACAL is disabled. 1h = FAST ACAL is enabled
9	FAST_FCAL_EN	R/W	1h	Fast fcal enable 0h = FAST FCAL is disabled. 1h = FAST FCAL is enabled
8-0	UNDISCLOSED	R/W	110h	Program this field to 0x110.

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7.1.6 R5 Register (Offset = 5h) [Reset = 0F2Ch]

R5 is shown in 表 7-8.

Return to the Summary Table.

表 7-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	MASH_ORDER	R/W	0h	Decides MASH order. MASH order has limitation based on 'N' value used and frequency. 0h = Mash Disable 1h = 1st order 2h = 2nd order 3h = 3rd order 4h = 4th order 6Fh = > Invalid
12	FULL_ASSIST	R/W	0h	Force VCO and Dblr settings in Full Assist mode to avoid calibration. VCO and Doubler takes user programmed value s for following registers - VCO_SEL, VCO_CAPCODE, VCODACISET, DBLR1_PD, DBLR_AMP_CAPCTRL, DBLR_AMP_DACCTRL, DBLR_PREGEN_AMP_CAPCTRL, DBLR_PREGEN_AMP_DACCTRL
11-9	VCO_SEL	R/W	7h	User specified start VCO. If no value is written, calibration starts with VCO7 (default value) else calibration always starts with VCO7 0h = > Invalid 1h = VCO1 2h = VCO2 3h = VCO3 7h = VCO7
8-0	VCO_IDAC	R/W	12Ch	Idac bit setting for VCO. Adds extra 4uA bias current

7.1.7 R6 Register (Offset = 6h) [Reset = 41BFh]

R6 is shown in 表 7-9.

Return to the Summary Table.

表 7-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.
14-13	DBLR_AMP1_DACCTRL	R/W	2h	Control daccode in Doubler Amplifiers. Code the but according to the readback after dblr calibration.
12-9	DBLR_AMP_CAPCTRL	R/W	0h	Control capcode in Doubler Amplifiers. Code the bit according to the readback after dblr calibration.

表 7-9. R6 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
8	DBLR1_PD	R/W	1h	To disable path1 for doubler. Needs override. 0h = Doubler1 path is powered on 1h = Doubler1 path is powered off
7-0	VCO_CAPCTRL	R/W	BFh	cap code for VCO0-7. Usable range is from 191 to 0.

7.1.8 R7 Register (Offset = 7h) [Reset = 7D40h]

R7 is shown in 表 7-10.

Return to the Summary Table.

表 7-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.
14-7	FASTCHG_CYCLES	R/W	FAh	Control number of SM cycles for which the fast charge is ON once reg0 is written in full_assist or double buffering mode. Recommended time = 5us 1h = 1SM clock cycle 2h = 2SM cycle FFh = 255 SM clock cycles
6-4	DBLR_PREGEN_AMP_DACCTRL	R/W	4h	Control daccode in Doubler PreDriver Amplifier. Code the bit according to the readback after dblr calibration.
3-0	DBLR_PREGEN_AMP_CAPCTRL	R/W	0h	Control capcode in Doubler PreDriver Amplifier. Code the bit according to the readback after dblr calibration.

7.1.9 R8 Register (Offset = 8h) [Reset = 0046h]

R8 is shown in 表 7-11.

Return to the Summary Table.

表 7-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_N[15:0]	R/W	46h	Integer part of NDIV (LSB)

7.1.10 R9 Register (Offset = 9h) [Reset = 0000h]

R9 is shown in 表 7-12.

Return to the Summary Table.

表 7-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	PLL_N[18:16]	R/W	0h	Upper 3 bits of N mash, total 19 bits, split as 16 + 3
12-0	RESERVED	R/W	0h	No description

7.1.11 R10 Register (Offset = Ah) [Reset = DA80h]

R10 is shown in 表 7-13.

Return to the Summary Table.

表 7-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_DEN[15:0]	R/W	DA80h	Denom of MASH Fraction (LSB)

7.1.12 R11 Register (Offset = Bh) [Reset = FD51h]

R11 is shown in 表 7-14.

Return to the Summary Table.

表 7-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_DEN[31:16]	R/W	FD51h	Denom of MASH Fraction (MSB)

7.1.13 R12 Register (Offset = Ch) [Reset = 0000h]

R12 is shown in 表 7-15.

Return to the Summary Table.

表 7-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_SEED[15:0]	R/W	0h	Mash seed (LSB) Sets the initial state of the fractional engine. Useful for producing a phase shift and fractional spur optimization.

7.1.14 R13 Register (Offset = Dh) [Reset = 0000h]

R13 is shown in 表 7-16.

Return to the Summary Table.

表 7-16. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_SEED[31:16]	R/W	0h	Mash seed (MSB)

7.1.15 R14 Register (Offset = Eh) [Reset = 0000h]

R14 is shown in 表 7-17.

Return to the Summary Table.

表 7-17. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_NUM[15:0]	R/W	0h	Numerator of MASH fraction (LSB)

7.1.16 R15 Register (Offset = Fh) [Reset = 0000h]

R15 is shown in 表 7-18.

Return to the Summary Table.

表 7-18. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_NUM[31:16]	R/W	0h	Numerator of MASH fraction (MSB)

7.1.17 R16 Register (Offset = 10h) [Reset = 0001h]

R16 is shown in 表 7-19.

Return to the Summary Table.

表 7-19. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R	0h	Program this field to 0x0.
8	DBL_BUF_EN	R/W	0h	Double buffering allows the user to program multiple registers without having them actually take effect till R0 is written 0h = Disables double buffering 1h = Enables doubler buffering
7-0	RDIV_POST	R/W	1h	Post R-divider value 1h = /1 2h = /2 FFh = /255

7.1.18 R17 Register (Offset = 11h) [Reset = 1001h]

R17 is shown in 表 7-20.

Return to the Summary Table.

表 7-20. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0h	No description
12	REF_Doubler_EN	R/W	1h	Register control for doubler in reference path. 0h = Disable REF path doubler 1h = Enable Doubler
11-0	RDIV_PRE	R/W	1h	Pre R-divider valuec(First 8 bits) All other bits are reserved. 1h = /1 2h = /2 80h = /128

7.1.19 R18 Register (Offset = 12h) [Reset = 0030h]

R18 is shown in 表 7-21.

Return to the Summary Table.

表 7-21. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	SYSREF_DIV	R/W	1h	Fout = Fin/(2*SYSREF_DIV + 4) 0h = /4 1h = /6 2h = /8 3h = /10 7FFh = /4098

ADVANCE INFORMATION

表 7-21. R18 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4-2	SYSREF_PRE_DIV	R/W	4h	SYSREF Input clock divider MUX 0h = div by 1 1h = div by 2 2h = div by 4
1	SYSREF_EN	R/W	0h	This is a master signal to enable entire sys ref module including repeater mode 0h = Disable SYSREF module 1h = Enable SYSREF module
0	SYSREF_MODE	R/W	0h	Set the device in master or repeater mode. 0h = Master mode (Internally generated sysref) 1h = Engages repeater mode (Enabled typically when a sysref signal is generated by an external device and needs to be "passed" by the device).

7.1.20 R19 Register (Offset = 13h) [Reset = 01F8h]

R19 is shown in 表 7-22.

Return to the Summary Table.

表 7-22. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.
14-9	JESD_DAC2	R/W	0h	Programmable delay for SYSREF output
8-3	JESD_DAC1	R/W	3Fh	The register bits represent DAC stages to be enabled, each reg set representing 63 stages and each code corresponds to a delay step in final output.
2	SYSREF_RPTR_NONSYNCMODE_EN	R/W	0h	Enables sysref in repeater non-sync mode 0h = Device is in sync mode 1h = Device is in Non-sync mode if repeater mode is selected.
1	UNDISCLOSED	R/W	0h	Program this field to 0x0.
0	SYSREF_PULSE_EN	R/W	0h	Sets the device for continuous sysref pulses or fixed number of pulses. The number of pulses is programmed through SYSREF_RPT_CNT register. 0h = Continuous mode 1h = Pulsed mode

7.1.21 R20 Register (Offset = 14h) [Reset = 0000h]

R20 is shown in 表 7-23.

Return to the Summary Table.

表 7-23. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	SYSREF_PULSE_CNT	R/W	0h	Used in N-shot mode to determine number of cycles SYSREF output is present. Setting this to zero is an allowable, but not practical state. 1h = 1pulses 2h = 2pulses Fh = 15 pulses
11-6	JESD_DAC4	R/W	0h	Programmable delay for SYSREF output
5-0	JESD_DAC3	R/W	0h	Programmable delay for SYSREF output

7.1.22 R22 Register (Offset = 16h) [Reset = 0001h]

R22 is shown in 表 7-24.

Return to the Summary Table.

表 7-24. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	UNDISCLOSED	R	0h	Program this field to 0x0.
7	UNDISCLOSED	R/W	0h	Program this field to 0x0.
6-0	MUXOUT_TM_SEL	R/W	1h	User Debug 0h = lock_detect 1h = lock_detect 2h = Refout Clock(divided) 3h = SM Clock

7.1.23 R23 Register (Offset = 17h) [Reset = 09C4h]

R23 is shown in 表 7-25.

Return to the Summary Table.

表 7-25. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	LD_DLY	R/W	9C4h	For the VCOCal lock detect, this is the SM cycles that is added after the calibration is finished before the VCOCal lock detect is asserted high.

7.1.24 R30 Register (Offset = 1Eh) [Reset = D6D8h]

R30 is shown in 表 7-26.

Return to the Summary Table.

表 7-26. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_RST_COUNT[15:0]	R/W	D6D8h	Mash counter for applying reset puls (lower 16 bits)

7.1.25 R31 Register (Offset = 1Fh) [Reset = 0000h]

R31 is shown in 表 7-27.

Return to the Summary Table.

表 7-27. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_RST_COUNT[31:16]	R/W	0h	Mash counter for applying reset pulse (upper 16 bits)- 16 bit unsigned integer This delay is used to verify that the reliable reset is provided to the mash circuit only after device is locked when using phase SYNC. This in turn verifies that during multi device sync scenario same Mash output sequence is maintained. The delay must be set at least four times the PLL lock time. This delay is expressed in state machine clock periods. One of these periods is equal to $2^{SM\_CLK\_DIV}$/Fosc

ADVANCE INFORMATION

7.1.26 R32 Register (Offset = 20h) [Reset = 026Fh]

R32 is shown in 表 7-28.

Return to the Summary Table.

表 7-28. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	No description
9-3	WD_DLY	R/W	4Dh	Delay for the internal watchdog timer. The timer is internally multiplied by 2^{14}. Default value is 25ms with 50MHz SM CLK.
2-0	WD_CNTRL	R/W	7h	Watchdog Control 0h = Digital Watchdog disabled. 1h = Watchdog triggers 1 time 2h = Watchdog triggers up to 2 times 3h = Watchdog triggers up to 3 times 4h = Watchdog triggers up to 4 times 5h = Watchdog triggers up to 5 times 6h = Watchdog triggers up to 6 times 7h = Watchdog retriggers as many times as necessary with no limit.

7.1.27 R34 Register (Offset = 22h) [Reset = 00F1h]

R34 is shown in 表 7-29.

Return to the Summary Table.

表 7-29. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rb_VER_ID	R	F1h	Readback: version ID

7.1.28 R35 Register (Offset = 23h) [Reset = 0000h]

R35 is shown in 表 7-30.

Return to the Summary Table.

表 7-30. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	0h	No description
5	rb_LD_VTUNELO_CMPO	R	0h	Readback: lock detect low comparator output
4	rb_LD_VTUNEHI_CMPO	R	0h	Readback: lock detect hi comparator output
3-1	rb_VCO_SELECT_RB	R	0h	Readback: indicates current VCO selected
0	rb_VCO_CT_CAL_RUNNING	R	0h	Readback: high if FCAL is running

7.1.29 R79 Register (Offset = 4Fh) [Reset = 0003h]

R79 is shown in 表 7-31.

Return to the Summary Table.

表 7-31. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.

ADVANCE INFORMATION

表 7-31. R79 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
14-0	UNDISCLOSED	R/W	3h	Program this field to 0x3.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 OSCin Configuration

OSCin supports single or differential-ended clock. There must be a AC -coupling capacitor in series before the device pin. The OSCin inputs are high impedance CMOS with internal bias voltage. TI recommends putting termination shunt resistors to terminate the differential traces (if there are 50-Ω characteristic traces, place 50-Ω resistors). The OSCin and OSCin* side must be matched in layout. A series AC-coupling capacitors must immediately follow OSCin pins in the board layout, then the shunt termination resistors to ground must be placed after.

Input clock definitions are shown in 図 8-1:

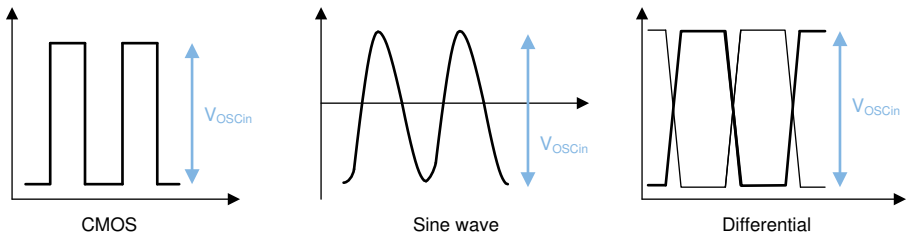

図 8-1. Input Clock Definitions

8.1.2 OSCin Slew Rate

The slew rate of the OSCin signal can have an impact on the spurs and phase noise of the LMX2624-SP if the signal is too low. In general, the best performance is for a high slew rate, but lower amplitude signal, such as LVDS.

8.1.3 RF Output Buffer Power Control

The OUTA_PWR and OUTB_PWR registers control the amount of drive current for the output. This current creates a voltage across the pullup component and load. Keeping the OUTx_PWR setting at 31 or less is generally recommended as higher settings consume more current consumption and can also lead to higher output power. Optimal noise floor is typically obtained by setting OUTx_PWR in the range of 15 to 25.

8.1.4 RF Output Buffer Pullup

The pull up resistors are integrated in this device. 50 Ω resistors to VCC pull up is there internally for each pin on the differential outputs RFOUTA and RFOUTB.

8.1.5 RF Output Treatment for the Complimentary Side

Regardless of whether both sides of the differential outputs are used, both sides must see a similar load.

8.1.5.1 Single-ended Termination of Unused Output

The unused output must have approximately the same impedance as looking out of the pin to minimize harmonics and get the best output power. If the application requirement is to use only single-ended output, for example RFOUTAP, then the user must verify that the RFOUTAM also has same impedance. For a typical 50 Ω systems with 50 Ω PCB traces, the unused pin can be terminated with 50 Ω with AC coupling capacitor.

ADVANCE INFORMATION

図 8-2. Termination of Unused Output

8.2 Typical Application

図 8-3. Typical Application Schematic (TBD)

8.2.1 Design Requirements

The design of the loop filter is complex and is typically done with software. The PLLatinum Sim software is an excellent resource for doing this and the design is shown in 図 8-4. For those interested in the equations involved, the PLL Performance, Simulation, and Design Handbook (SNAA106) goes into great detail as to theory and design of PLL loop filters.

図 8-4. PLLatinum Sim Tool

8.2.2 Detailed Design Procedure

The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. Generally, jitter is lowest if loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The tradeoff with this is that longer lock times and spurs must be considered in design as well.

ADVANCE INFORMATION

8.2.3 Application Curve

Using the settings described, the performance measured using a clean 100-MHz input reference is shown. Note the loop bandwidth is about 350 kHz, as simulations predict.

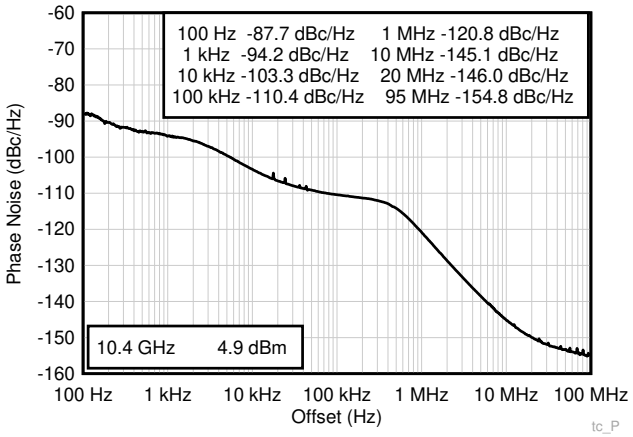

図 8-5. Results for Loop Filter Design

8.3 Power Supply Recommendations

TI recommends placement of bypass capacitors close to the pins. Consult the EVM instructions for layout examples. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree. This device has integrated LDOs, which improves the resistance to power supply noise. However, the pullup components on the RFoutA and RFoutB pins on the outputs have a direct connection to the power supply, so extra care must be made to verify that the voltage is clean for these pins.

8.4 Layout

8.4.1 Layout Guidelines

In general, the layout guidelines are similar to most other PLL devices. Here are some specific guidelines.

- GND pins can be routed on the package back to the DAP.
- The OSCin pins, these are internally biased and must be AC coupled.
- If not used, the SysRefReq can be grounded to the DAP.
- For optimal VCO phase noise in the 200kHz – 1MHz range, place the capacitor closest to the Vtune pin be at least 3.3nF. As requiring this larger capacitor can restrict the loop bandwidth, this value can be reduced (to say 1.5nF) at the expense of VCO phase noise.
- For the outputs, keep the pullup component as close as possible to the pin and use the same component on each side of the differential pair.
- If a single-ended output is needed, the other side must have the same loading and pullup. However, the routing for the used side can be optimized by routing the complementary side through a via to the other side of the board. On this side, use the same pullup and make the load look equivalent to the side that is used.
- Verify that DAP on device is well-grounded with many vias, preferably copper filled.
- Have a thermal pad that is as large as the LMX2624-SP exposed pad. Add vias to the thermal pad to maximize thermal performance.
- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.

ADVANCE INFORMATION

8.4.2 Layout Example

図 8-6. LMX2624-SP Layout Example

8.4.3 Footprint Example on PCB Layout

図 8-7. LMX2624-SP PCB Layout (TBD)

8.4.4 Radiation Environments

Careful consideration must be given to environmental conditions when using a product in a radiation environment.

8.4.4.1 Total Ionizing Dose

Radiation Hardness Assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the ordering information. Testing and qualification of these product is done on a wafer level according to MIL-STD-883, test method 1019. Wafer level TID data are available with lot shipments.

8.4.4.2 Single Event Effect

One time single event effect (SEE), including single event latch-up (SEL), single event functional interrupt (SEFI) and single event upset (SEU), testing is performed according to EIA/JEDEC Standard, EIA/JEDEC57. A test report is available upon request.

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

Texas Instruments has several software tools to aid in the development at www.ti.com. Among these tools are:

- EVM software to understand how to program the device and for programming the EVM board.
- EVM board instructions for seeing typical measured data with detailed measurement conditions and a complete design.
- PLLatinum Sim program for designing loop filters, simulating phase noise, and simulating spurs.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- *AN-1879 Fractional N Frequency Synthesis* (SNAA062)
- *PLL Performance, Simulation, and Design Handbook* (SNAA106)

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.5 Trademarks

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9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Draft

ADVANCE INFORMATION

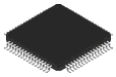
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

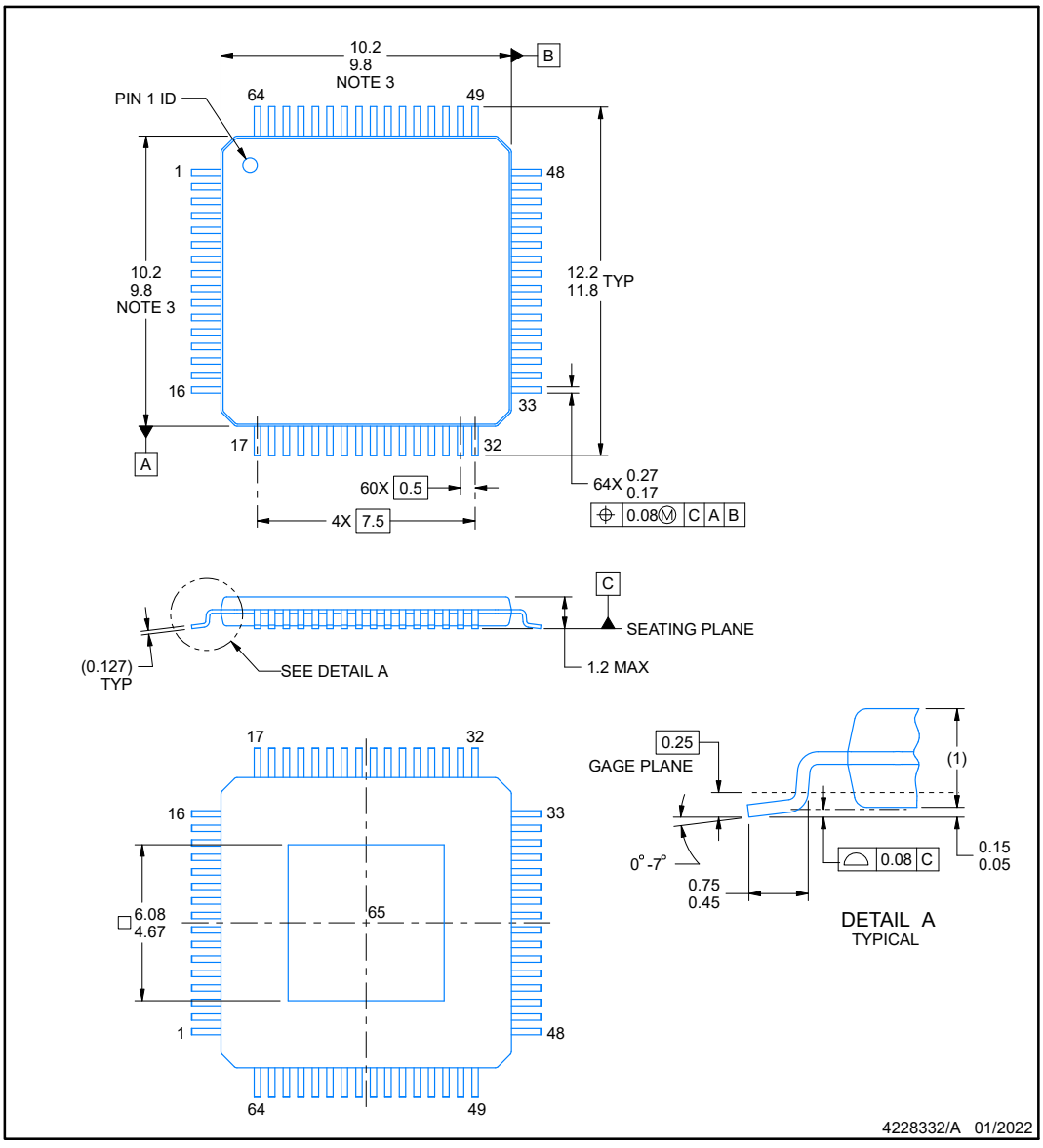
PACKAGE OUTLINE

PAP0064E



PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLAT PACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

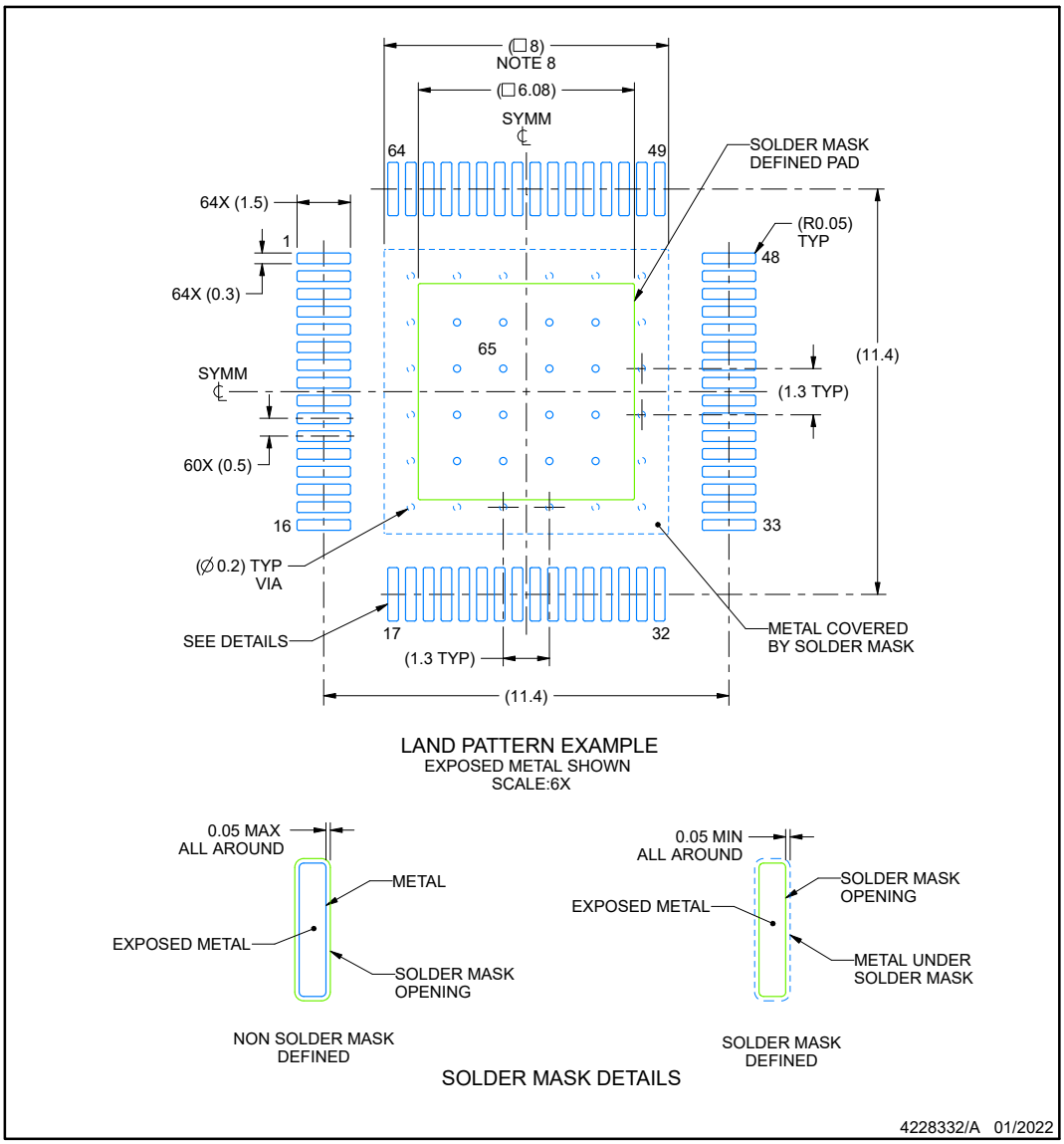
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

PAP0064E — **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

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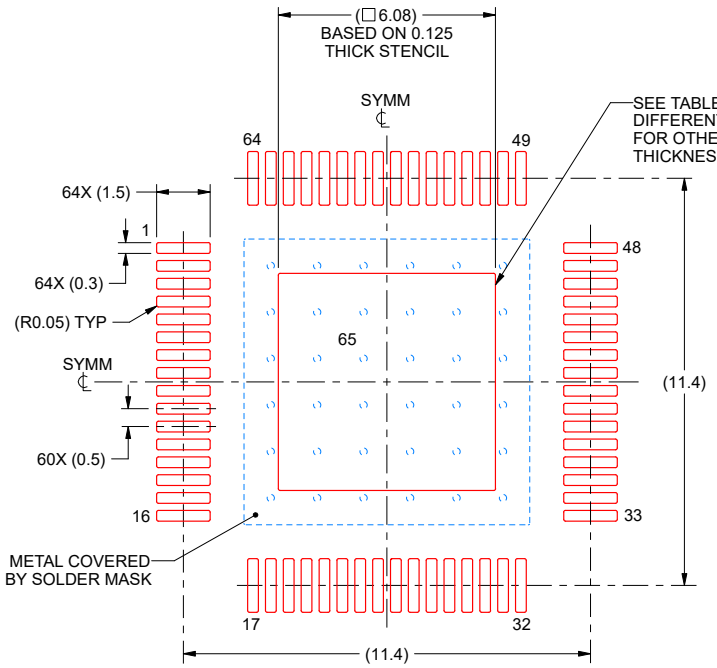
EXAMPLE STENCIL DESIGN

PAP0064E — **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.80 X 6.80
0.125	6.08 X 6.08 (SHOWN)
0.15	5.55 X 5.55
0.175	5.14 X 5.14

4228332/A 01/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

11.1 Engineering Samples

Engineering samples (LMX2624-SPW-MPR) have the same package, pinout, programming, and typical performance as the flight devices (LMX2624-SPW-MLS). The devices are tested at room temperature to meet the electrical specifications, but have not received or passed the full space production flow or testing. Engineering samples can be QCI rejects that failed full space production tests, such as radiation or reliability.

11.2 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PLMX2624PAP/EM	PREVIEW	HTQFP	PAP	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	25 to 25	PLMX2624PAPEM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

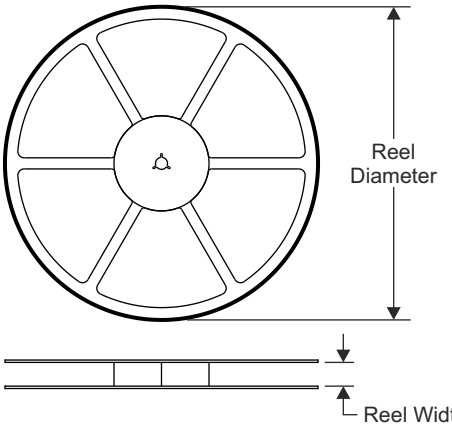
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

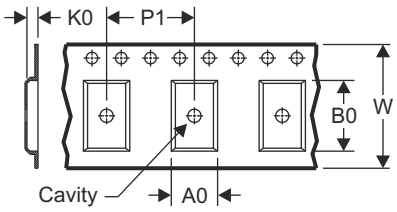
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

11.3 Tape and Reel Information

REEL DIMENSIONS

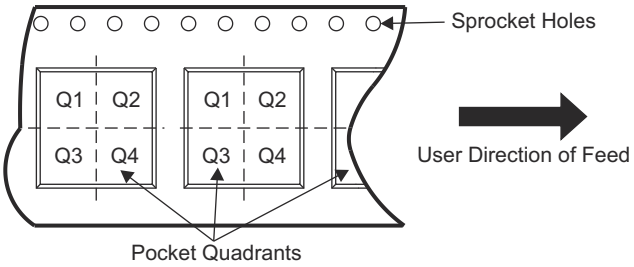


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

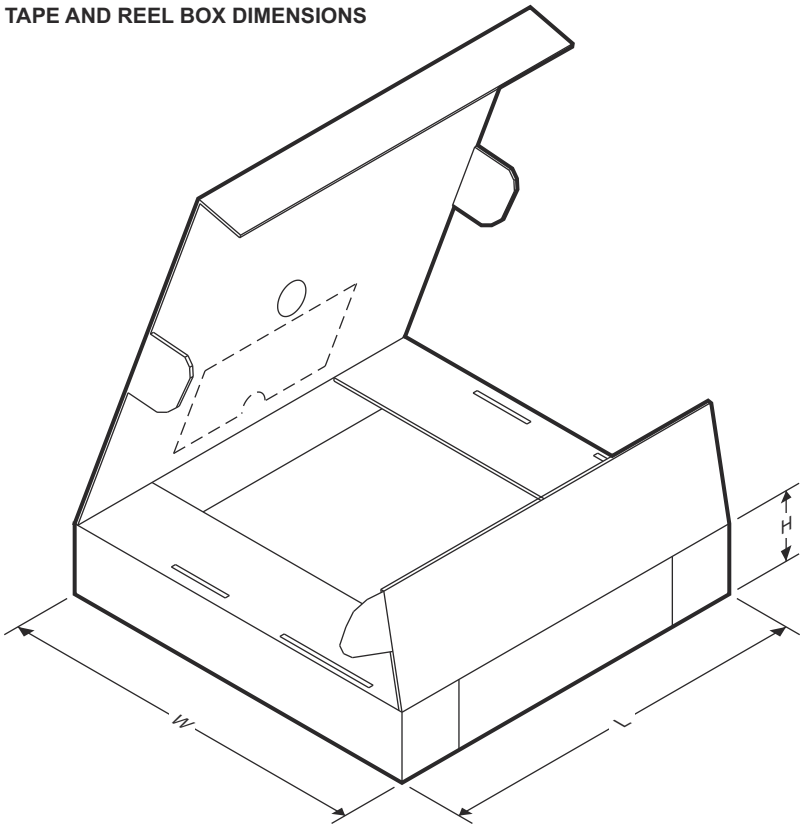


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLMX2624PAP/EM	HTQFP	PAP	64	250	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLMX2624PAP/EM	HTQFP	PAP	64	250	367.0	367.0	55.0

GENERIC PACKAGE VIEW

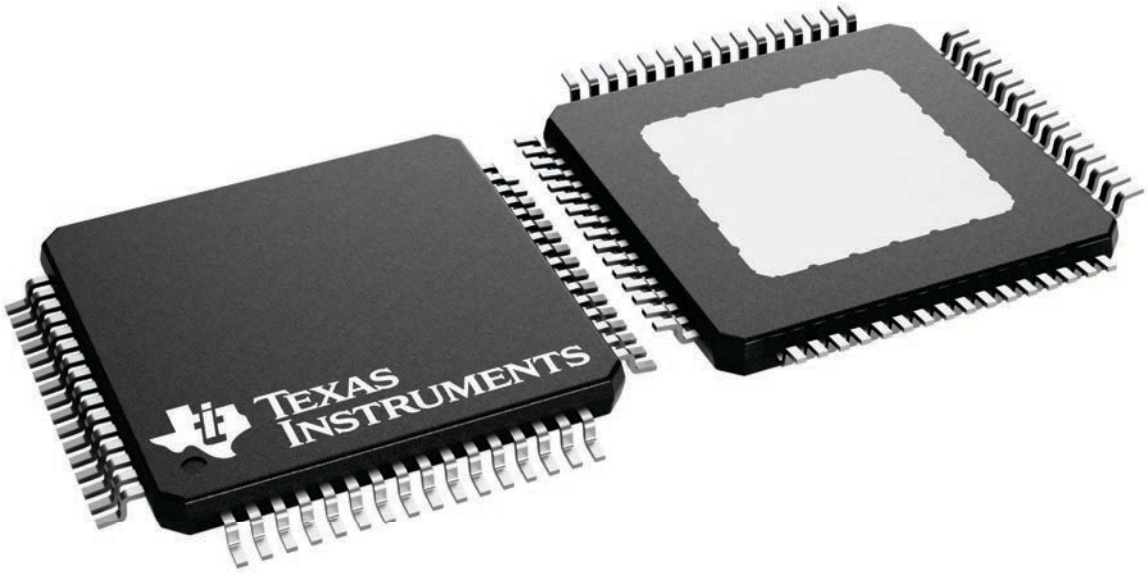
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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