TEXAS INSTRUMENTS
LMR51460-Q1
JAJSV98 – AUGUST 2024

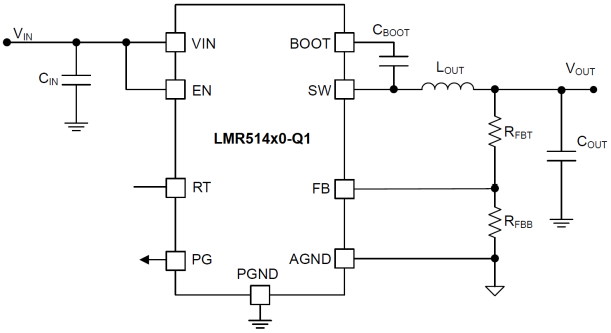
LMR51460-Q1 36V、 6A、車載用同期整流降圧コンバータ、低 I_Q

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 車載システム要件に対応:
  - 幅広い入力電圧範囲:4V～36V
  - 連続出力電流: 6A
  - 室温で許容誤差 ±1.0% の基準電圧
  - 最小限のスイッチング オンタイム:75ns (標準値)
  - 低い静止電流:25µA
  - 可変周波数:200kHz～1MHz
  - 周波数スペクトラム拡散
  - 保護機能:
    - 高精度イネーブル入力
    - オープンドレイン PGOOD
    - V_{IN} 低電圧誤動作防止 (UVLO)
    - サイクル単位の電流制限
    - ヒカップ モードによる短絡保護
    - サーマル シャットダウン
- 小型の設計サイズと使いやすさ
  - 同期整流器内蔵
  - 使いやすさを実現した内部補償
  - WSON-12 パッケージ
- ピン互換パッケージの PFM および FPWM オプション
- WEBENCH® Power Designer により、LMR51460-Q1 を使用するカスタム設計を作成

2 アプリケーション

- 車載用 ADAS およびボディ エレクトロニクス
- 車載用インフォテインメントおよびクラスタ:ヘッド ユニット、メディア ハブ、USB 充電、ディスプレイ



概略回路図

3 概要

LMR51460-Q1 は、最大 6A の負荷電流を駆動でき、V_{IN} が広く使いやすい同期整流降圧コンバータです。このデバイスは、4V～36V の広い入力電圧範囲で動作し、レギュレートされていない電源からの電源調整を行うさまざまな産業用アプリケーションに適しています。

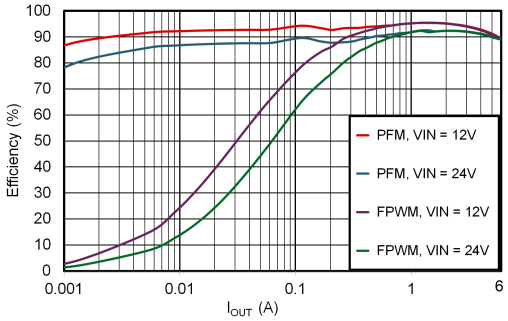
LMR51460-Q1 は、外付け抵抗により 200kHz～1MHz 可変スイッチング周波数を実現し、効率または外付け部品のサイズを最適化する柔軟性があります。このデバイスには、軽負荷時に高効率を実現するパルス周波数変調 (PFM バージョン) と、一定の周波数を維持しながら、全負荷範囲にわたって出力電圧リップルが小さい強制パルス幅変調 (FPWM バージョン) があります。ソフト スタートと補償回路が内部に実装されており、最小限の外付け部品のみでデバイスを使用できます。

このデバイスには、サイクル単位の電流制限、ヒカップ モード短絡保護、過剰な電力消費時のサーマル シャットダウンなどの保護機能が組み込まれています。LMR51460-Q1 は、WSON-12 パッケージで供給されます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
LMR51460-Q1	DRR (WSON、12)	3 mm × 3 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



効率と出力電流との関係 V_{OUT} = 5V、400kHz

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4 Device Comparison Table

ORDERABLE PART NUMBER	CURRENT	PFM OR FPWM	SPREAD SPECTRUM
LMR51460SQDRRRQ1	6A	PFM	Yes
LMR51460FSQDRRRQ1	6A	FPWM	Yes

5 Pin Configuration and Functions

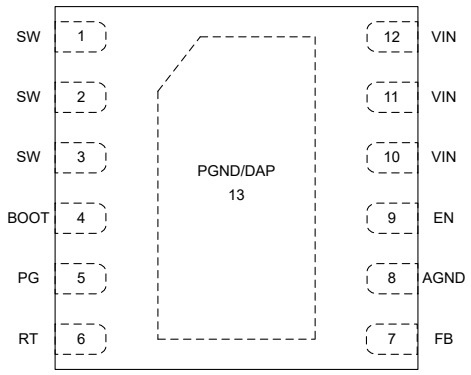


図 5-1. 12-Pin WSON DRR Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO		
SW	1, 2, 3	P	Switching output of the converter. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
BOOT	4	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
PG	5	A	Open-drain power-good monitor output that asserts low if the FB voltage is not within the specified window thresholds. A 10kΩ to 100kΩ pull up resistor to a suitable voltage is required. If not used, PG can be left open or connected to GND.
RT	6	A	Frequency setting pin used to set the switching frequency between 200kHz and by placing an external resistor from RT to AGND. RT open defaults to 440kHz and RT short to ground defaults to 1MHz.
FB	7	A	Feedback input to the converter. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
AGND	8	G	Analog ground. Zero-voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. These pins must be connected to PGND using a small net-tie.
EN	9	A	Precision enable input pin. High = On, Low = Off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable input voltage UVLO. Connect an external resistor divider between this pin, VIN and AGND to create an external UVLO. *Do not float.*
VIN	10, 11, 12	P	Input supply voltage. Connect the input supply to these pins. Connect input capacitors CIN between these pins and PGND in close proximity to the device.
PGND	13	G	Power ground terminals, connected to the source of low-side FET internally. Connect to system ground, ground side of CIN and COUT. Path to CIN must be as short as possible.

(1) A = Analog, P = Power, G = Ground.

6 Specifications

6.1 Absolute Maximum Ratings

Over junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	38	V
	EN to PGND	–0.3	V_{IN} + 0.3	V
	FB to PGND	–0.3	5.5	V
	RT to PGND	–0.3	5.5	V
Output voltage	BOOT to SW	–0.3	5.5	V
	SW to PGND	–0.3	38	V
	SW to PGND less than 10ns transients	–4.5	40	V
	PG to PGND	–0.3	20	V
Junction Temperature T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage	Input voltage range	4.0		36	V
Input voltage	EN to PGND			V_{IN}	V
Input voltage	RT to PGND			5	V
Input voltage	PGOOD to PGND			20	V
Output voltage	SW to PGND			36	V
Output voltage	Output voltage range (2)	0.8		28	V
Frequency	Frequency range	200		1000	kHz
Load current	Output DC current range, 6A version (3)	0		6	A
Temperature	Operating junction temperature T_J range (4)	–40		150	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not specify specific performance limits. For compliant specifications, see Electrical Characteristics table.
(2) Under no conditions can the output voltage be allowed to fall below zero volts.
(3) Maximum continuous DC current can be derated when operating with high switching frequency or high ambient temperature. See Application section for details.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 150°C.

6.4 Thermal Information

THERMAL METRIC[1]		LMR514X0-Q1 DRR (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.4	°C/W
$R_{\theta JA(Effecitve)}$	Junction-to-ambient thermal resistance with TI EVM board	23	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits[1] are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4V to 36V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
$I_{Q-nonSW}$	Operating quiescent current (non-switching)	V_{EN} = 3.3V (PFM variant only)		25		µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0V, V_{IN} = 24V		3	6	µA
$V_{IN\_OPERATE}$	V_{IN} UVLO threshold	V_{IN} rising, needed to start up			3.9	V
		V_{IN} falling, once operating	3.4			V
ENABLE						
V_{EN-H}	Enable input high level	EN rising, enable switching	1.1	1.25	1.4	V
V_{EN-L}	Enable input low level	EN falling, disable switching	0.8	1	1.12	V
I_{LKG-EN}	Enable input leakage current	V_{EN} = 3.3V		0.1		µA
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage	T_J = 25°C	0.792	0.8	0.808	V
I_{LKG-FB}	Feedback leakage current	FB = 1V			100	nA
CURRENT LIMITS AND HICCUP						
I_{SC}	High-side current limit[3]	6A version	7.1	8.4	9.6	A
$I_{LS-LIMIT}$	Low-side current limit[3]	6A version		5.8		A
I_{L-ZC}	Zero cross detector threshold	PFM variants only		–0.1		A
$I_{PEAK-MIN}$	Minimum inductor peak current[3]	6A version, PFM variants only		1		A
I_{L-NEG}	Negative current limit[3]	6A version, FPWM variant only		–3.5		A
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage			40%		

6.5 Electrical Characteristics (続き)

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4V to 36V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
$V_{PG-HIGH-UP}$	Power-Good upper threshold - rising	% of FB voltage	110%	112%	115%	
$V_{PG-LOW-DN}$	Power-Good lower threshold - falling	% of FB voltage	88%	90%	92%	
V_{PG-HYS}	Power-Good hysteresis (rising and falling)	% of FB voltage		2.0%		
$V_{PG-VALID}$	Minimum input voltage for proper Power-Good function				1.5	V
R_{PG}	Power-Good ON-resistance	V_{EN} = 3.3V		84		Ω
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance			78		mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance			45		mΩ
$V_{BOOT-SW-UVLO(R)}$	BOOT-SW UVLO rising threshold	$V_{BOOT-SW}$ rising		2.2		V
SWITCHING CHARACTERISTICS						
$F_{SW (CCM)}$	Switching frequency	R_T = 34.8kΩ	345	400	455	kHz
$F_{SW (CCM)}$	Switching frequency	R_T = Open or pull up to voltage >1.0V	395	440	485	kHz
$F_{SW (CCM)}$	Switching frequency	R_T = 13.3kΩ		1000		kHz
$F_{SW (CCM)}$	Switching frequency	R_T = Short to GND		1000		kHz
F_{SPREAD}	Switching frequency dithering	Frequency dithering over center frequency		±10%		
TIMING REQUIREMENT						
t_{ON-MIN}	Minimum switch on-time(2)	V_{IN} = 24V, Iout = 1A		75		ns
$t_{OFF-MIN}$	Minimum switch off-time			135		ns
t_{ON-MAX}	Maximum switch on-time			5		µs
t_{SS}	Internal soft-start time		3.2	5	7.2	ms
t_{HICCUP}	Time between current-limit hiccup burst			96		ms
THERMAL SHUTDOWN						
$T_{SD-Rising}$ (2)	Thermal shutdown	Shutdown threshold		160		℃
$T_{SD-Falling}$ (2)	Thermal shutdown	Recovery threshold		140		℃

(1) MIN and MAX limits are 100% production tested at 25℃. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Not production tested. Specified by correlation by design.
(3) The current limit values in this table are tested, open loop, in production. They can differ from those found in a closed loop application.

6.6 System Characteristics

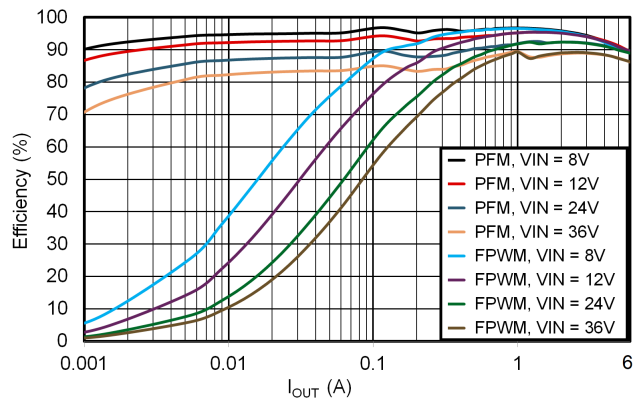
The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25℃ only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40℃ to 150℃. These specifications are not specified by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range		4		36	V
V_{OUT}	Adjustable output voltage regulation(1)	PFM operation		1.5%		
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0A, R_{FBT} = 1MΩ, PFM variant		35		μA
D_{MAX}	Maximum switch duty cycle(2)			97%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.32		V

(1) Deviation in V_{OUT} from nominal output voltage value at V_{IN} = 24V, I_{OUT} = 0A to full load
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: $F_{MIN} = 1 / (t_{ON\text{-}MAX} + t_{OFF\text{-}MIN})$. $D_{MAX} = t_{ON\text{-}MAX} / (t_{ON\text{-}MAX} + t_{OFF\text{-}MIN})$.

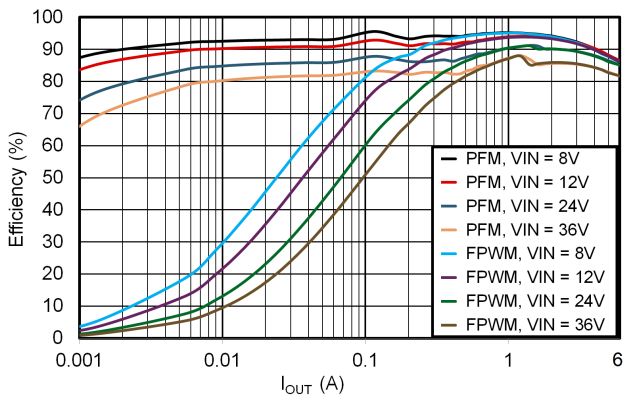
6.7 Typical Characteristics

V_{IN} = 12V, f_{SW} = 440kHz,T_A = 25°C, unless otherwise specified.



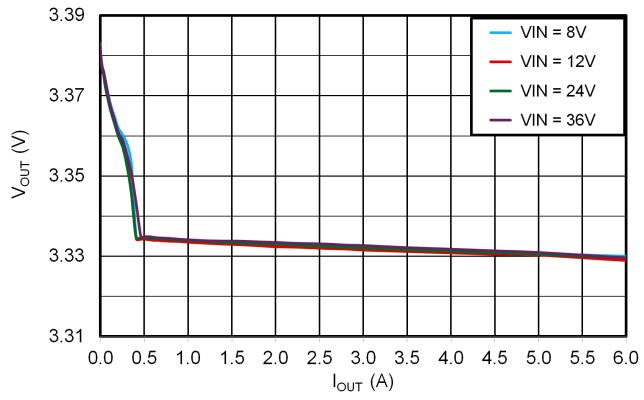
f_{SW} = 440kHz V_{OUT} = 5V LMR51460-Q1

図 6-1. 5V Efficiency versus Load Current



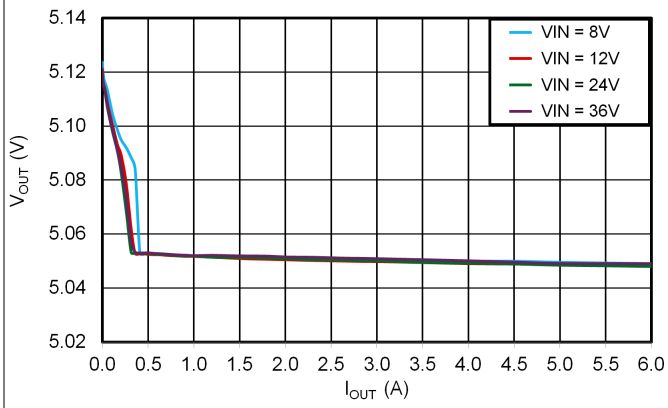
f_{SW} = 440kHz V_{OUT} = 3.3V LMR51460-Q1

図 6-2. 3.3V Efficiency versus Load Current



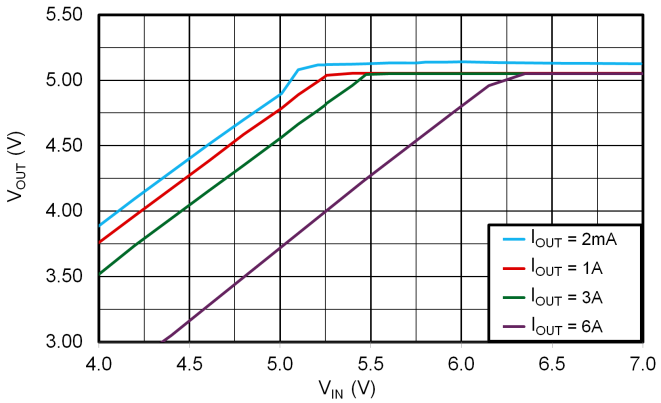
f_{SW} = 440kHz V_{OUT} = 3.3V PFM version

図 6-3. 3.3V Load Regulation



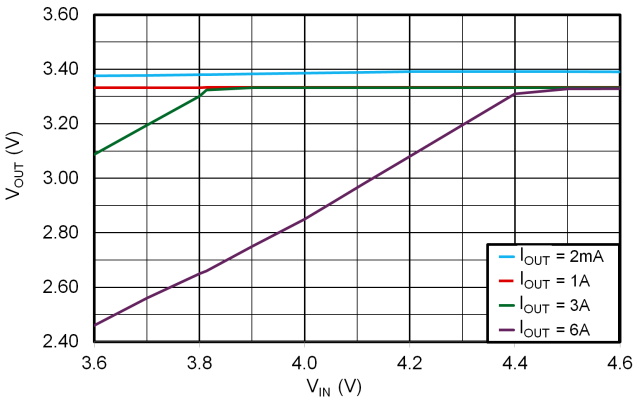
f_{SW} = 440kHz V_{OUT} = 5V PFM version

図 6-4. 5V Load Regulation



f_{SW} = 440kHz V_{OUT} = 5V PFM version

図 6-5. 5V Dropout



f_{SW} = 440kHz V_{OUT} = 3.3V PFM version

図 6-6. 3.3V Dropout

6.7 Typical Characteristics (continued)

V_{IN} = 12V, f_{SW} = 440kHz,T_A = 25°C, unless otherwise specified.

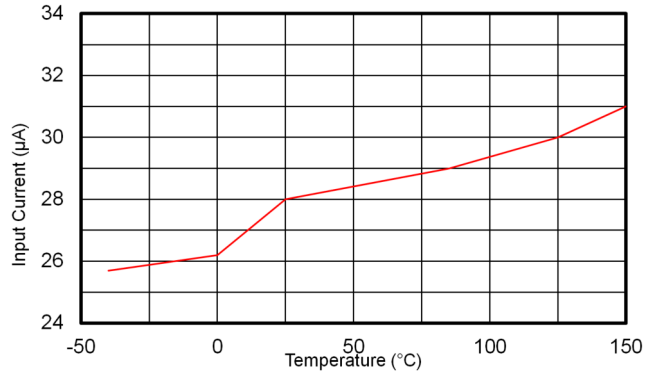


図 6-7. Non-Switching Input Supply Current

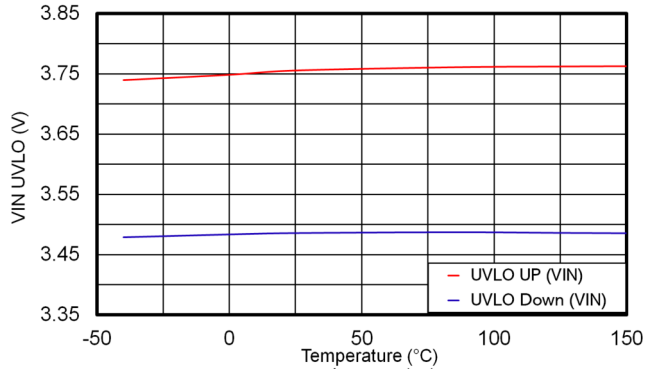


図 6-8. V_{IN} UVLO

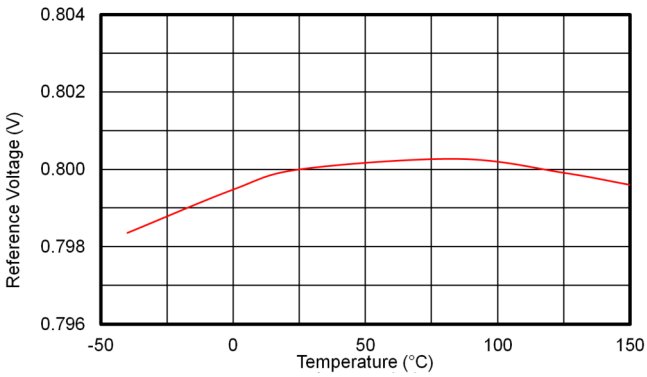


図 6-9. Reference Voltage

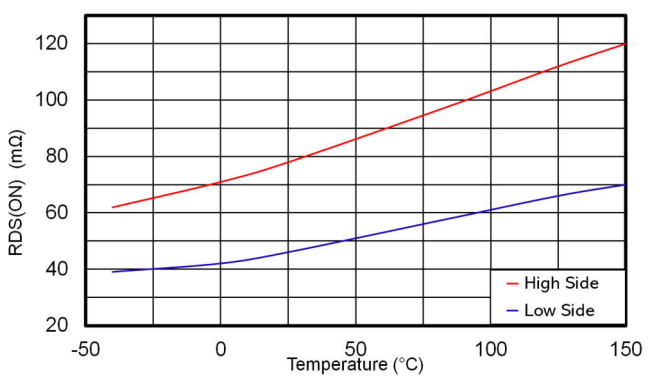


図 6-10. High Side and Low Side Switches R_{DS_ON}

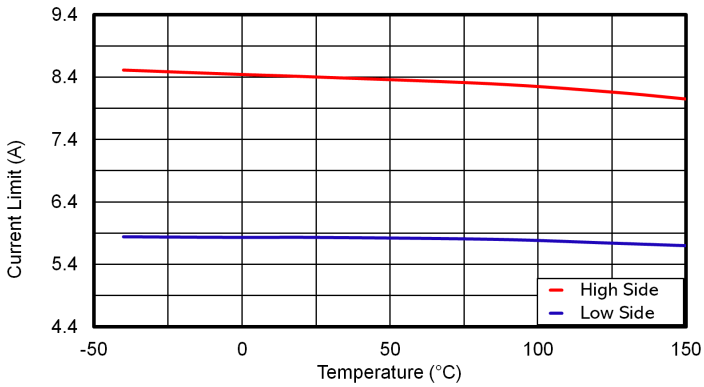


図 6-11. LMR51460-Q1 High Side and Low Side Current Limits

7 Detailed Description

7.1 Overview

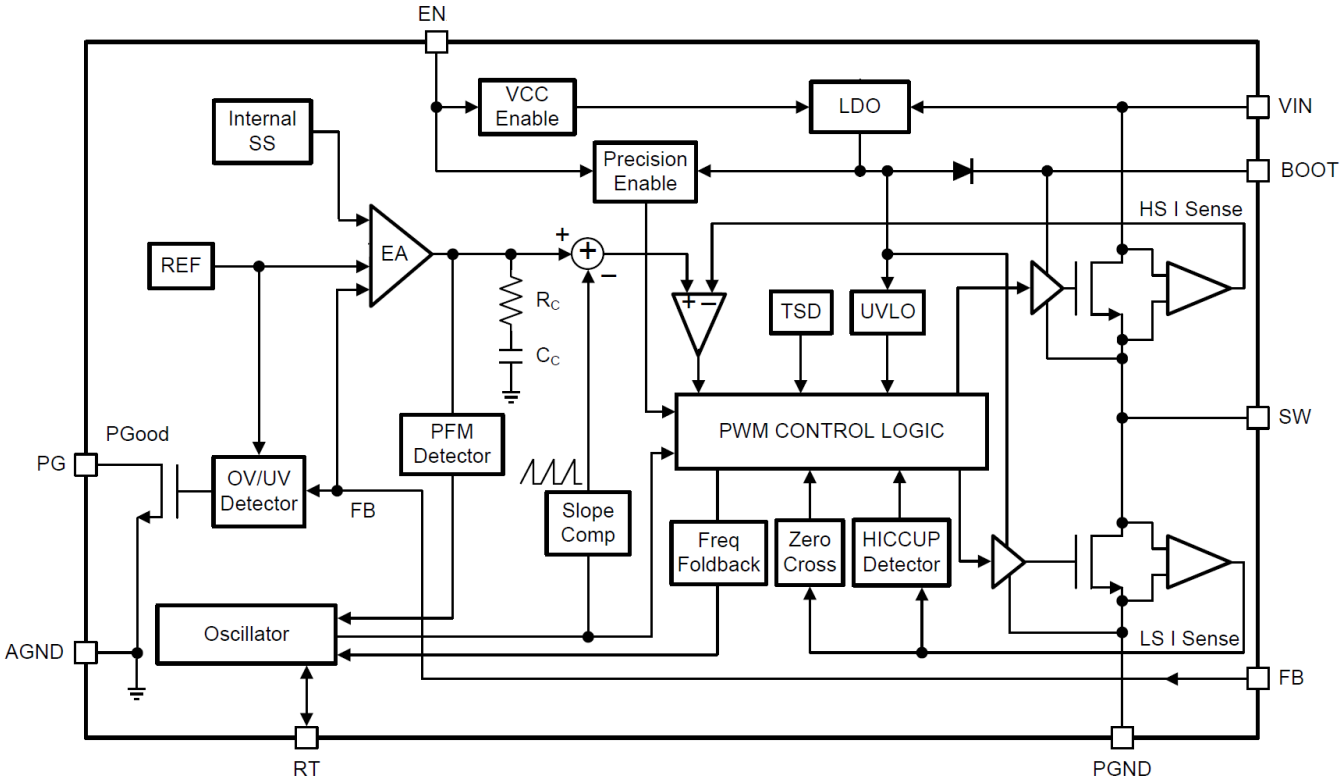
The LMR51460-Q1 converter is an easy-to-use, synchronous, step-down DC/DC converter operating from a 4V to 36V supply voltage. The device is capable of delivering up to 6A DC load current in a very small design size. The family has multiple versions applicable to various applications. See *Device Comparison Table* for detailed information.

The LMR51460-Q1 employs fixed-frequency peak-current mode control. The PFM version enters PFM mode at light load to achieve high efficiency. A FPWM version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. The device is internally compensated, which reduces design time and requires few external components.

Additional features, such as precision enable and internal soft start, provide a flexible and easy-to-use solution for a wide range of applications. Protection features include thermal shutdown, V_{IN} undervoltage lockout, cycle-by-cycle current limit, and hiccup mode short-circuit protection.

This family of devices requires very few external components and has a pinout designed for simple, optimum PCB layout.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency Peak Current Mode Control

The following operating description of the LMR51460-Q1 refers to *Functional Block Diagram* and to the waveforms in 図 7-1. The LMR51460-Q1 is a step-down synchronous buck converter with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR51460-Q1 supplies a regulated output voltage by turning on the high-side and low-side NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current, i_L, increases with linear slope (V_{IN} – V_{OUT}) / L. When the high-side switch is turned off by the control logic, the low-side switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the low-side switch with a slope of – V_{OUT} / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

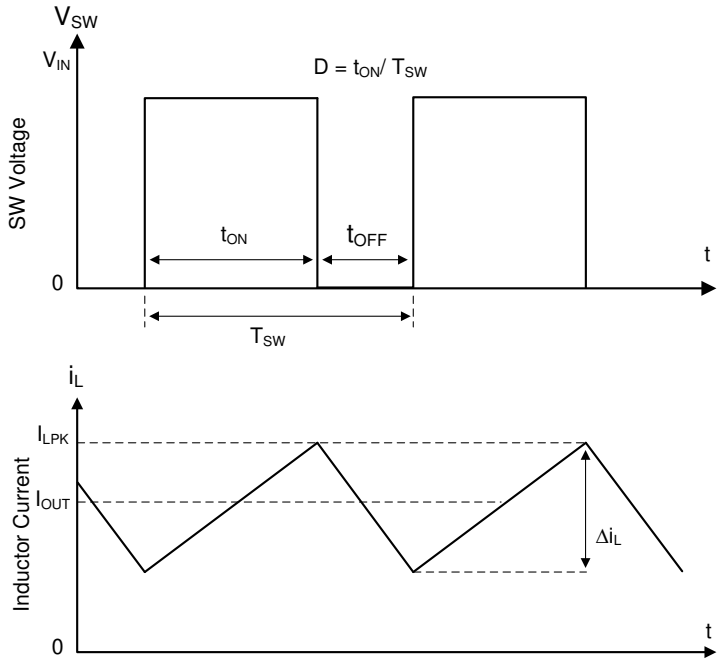


図 7-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR51460-Q1 employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally-compensated, which allows for fewer external components, making designing easy, and providing stable operation when using a variety of output capacitors. The converter operates with fixed switching frequency at normal load conditions. During light-load condition, the LMR51460-Q1 operates in PFM mode to maintain high efficiency (PFM version) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM version).

7.3.2 Adjustable Output Voltage

A precision 0.8V reference voltage (V_{REF}) is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from V_{OUT} to the FB pin. TI recommends to use 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor R_{FBB} for the desired divider current and use 式 1 to calculate top-side resistor R_{FBT}. The recommended range for R_{FBT} is 10kΩ to 100kΩ. A lower R_{FBT} value can be used if pre-loading is desired to reduce V_{OUT} offset in PFM operation. Lower R_{FBT} reduces efficiency at very light load. Less static current goes through a larger R_{FBT} and can be more desirable when light-load efficiency is critical. However, TI does not recommend R_{FBT} larger than 1MΩ because R_{FBT} larger than 1MΩ makes the feedback path more susceptible to noise. Larger R_{FBT} values require more carefully designed feedback path trace from the feedback resistors to the feedback pin of the device. The tolerance and temperature variation of the resistor divider network affect the output voltage regulation.

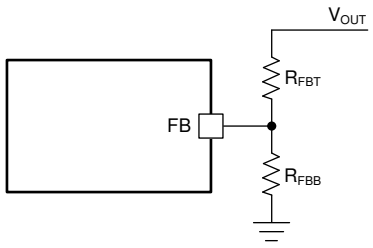


図 7-2. Output Voltage Setting

$$R_{FBT} = \frac{(V_{OUT} - V_{REF})}{V_{REF}} \times R_{FBB} \quad (1)$$

7.3.3 Enable

The voltage on the EN pin controls the ON and OFF operation of the LMR51460-Q1. A voltage of less than 0.8V shuts down the device, while a voltage of greater than 1.4V is required to start the converter. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR51460-Q1 when V_{IN} is within the operating range.

Many applications benefit from the employment of an enable divider R_{ENT} and R_{ENB} (図 7-3) to establish a precision system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. System UVLO can be used for sequencing, making sure of reliable operation or supplying protection, such as a battery discharge level. An external logic signal can also be used to drive EN input for system sequencing and protection. Note, the EN pin voltage must not to be greater than V_{IN} + 0.3V. TI does not recommend to apply EN voltage when V_{IN} is 0V.

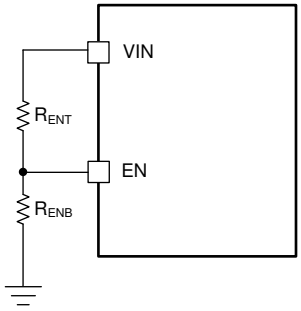


図 7-3. System UVLO by Enable Divider

7.3.4 Switching Frequency

The switching frequency of the LMR51460-Q1 can be programmed by the resistor RT from the RT pin and GND pin. The RT pin cannot be left floating or shorted to ground. To determine the timing resistance for a given switching frequency, use Equation 2 or the curve in 図 7-4. 表 7-1 gives typical R_T values for a given f_{SW}.

$$R_T(k\Omega) = 18576 \times f_{SW}(kHz)^{-1.048} \quad (2)$$

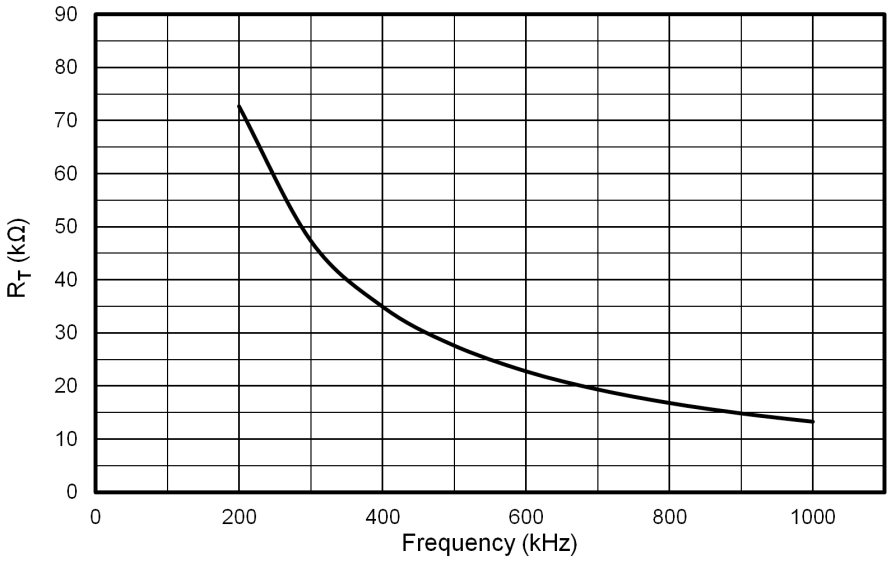


図 7-4. R_T Versus Frequency Curve

表 7-1. Typical Frequency Setting R_T Resistance

f_{SW} (kHz)	R_T (kΩ)
200	71.5
400	34.8
440	Open or pull up to voltage >1.0 V
500	27.4
750	18.0
1000	13.3
1000	Short to GND

7.3.5 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR51460-Q1 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{dg} 35µs (typical) do not trip the power-good flag. After the FB voltage has returned to the regulation value and after a delay of $t_{pg\text{-}delay}$ 3.1ms (typical) , the power-good flag goes high.

The power-good output consists of an open-drain NMOS, requiring an external pullup resistor to a suitable logic supply. It can be pulled up to power supply below 20V through a 10kΩ to 100kΩ resistor, as desired. If this function is not needed, the PG pin must be left floating. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is greater than or equal to 1.5V (typical). Limit the current into the power-good flag pin to less than 5mA D.C.

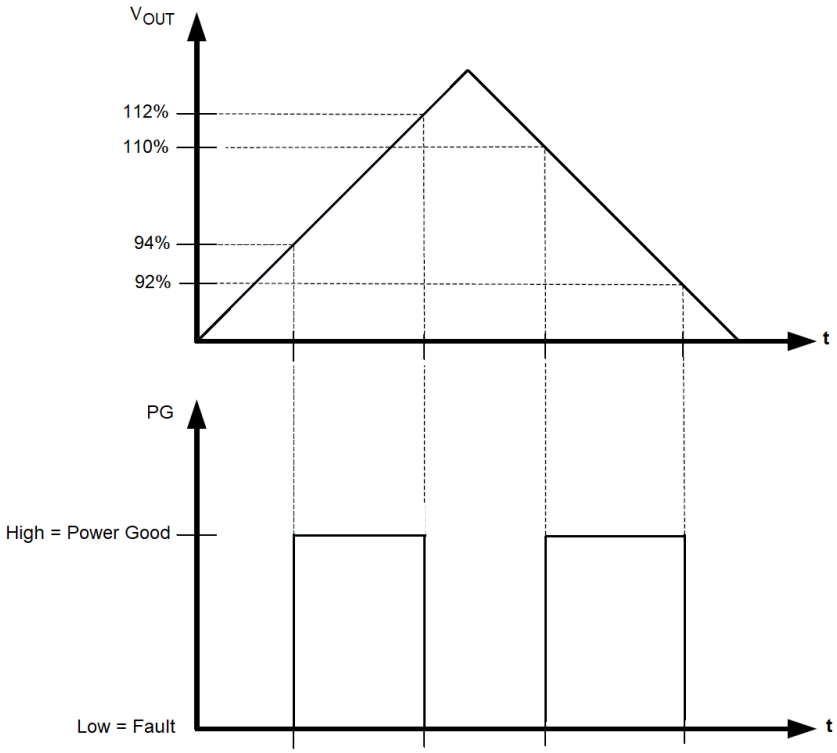


図 7-5. Static Power-Good Operation

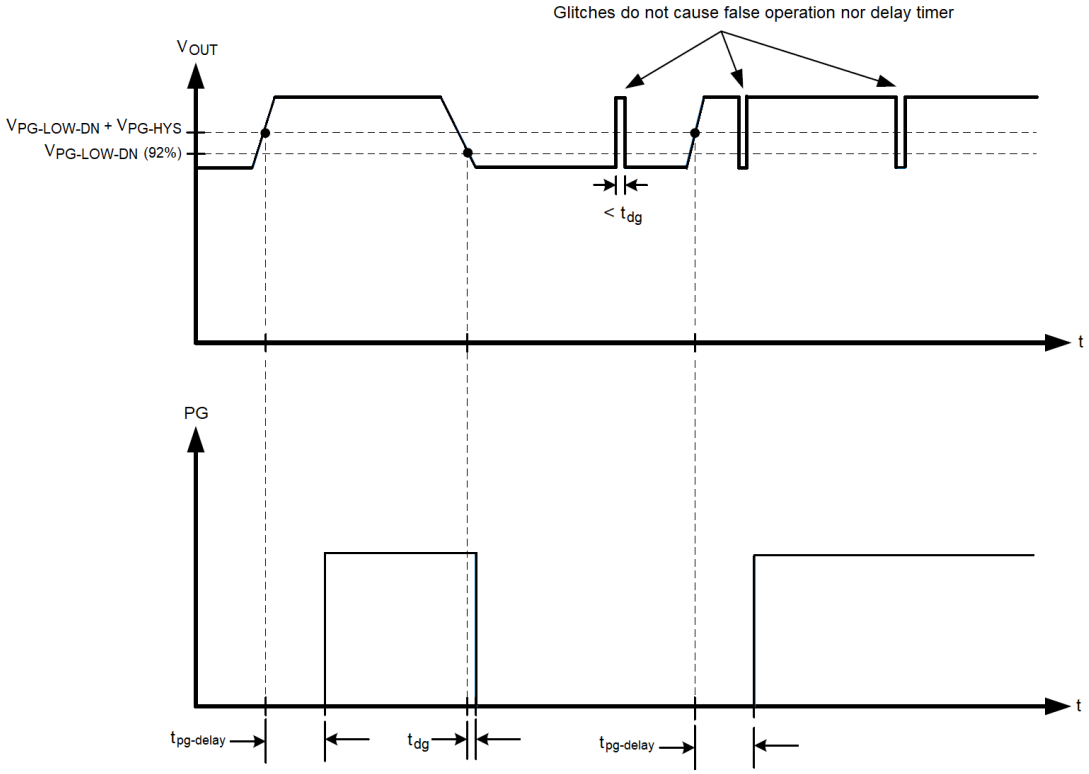


図 7-6. Power-Good Timing Behavior

7.3.6 Minimum ON-Time, Minimum OFF-Time, and Frequency Foldback

Minimum ON-time (t_{ON_MIN}) is the shortest duration of time that the high-side switch can be turned on. t_{ON_MIN} is typically 75ns for the LMR51460-Q1 . Minimum OFF-time (t_{OFF_MIN}) is the shortest duration of time that the high-side switch can be off. t_{OFF_MIN} is typically 135ns. In CCM operation, t_{ON_MIN} and t_{OFF_MIN} limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \quad (3)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \quad (4)$$

Given a required output voltage, the maximum V_{IN} without frequency foldback can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \quad (5)$$

The minimum V_{IN} without frequency foldback can be calculated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \quad (6)$$

In the LMR51460-Q1, a frequency foldback scheme is employed after the t_{ON_MIN} or t_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on-time decreases while V_{IN} voltage increases. After the on-time decreases to t_{ON_MIN}, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to Equation 5.

The frequency foldback scheme also works after larger duty cycle is needed under low V_{IN} condition. The frequency decreases after the device hits the t_{OFF_MIN}, which extends the maximum duty cycle according to Equation 6. In such condition, the frequency can be as low as approximately 200kHz. Wide range of frequency foldback allows for the LMR51460-Q1 output voltage to stay in regulation with a much lower supply voltage V_{IN}, which leads to a lower effective dropout.

With frequency foldback while maintaining a regulated output voltage, V_{IN_MAX} is raised, and V_{IN_MIN} is lowered by decreased f_{SW}.

7.3.7 Bootstrap Voltage

The LMR51460-Q1 provides an integrated bootstrap voltage converter. A small capacitor between the CB and SW pins provides the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch is on. The recommended value of the bootstrap capacitor is 0.1µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16V or higher for stable performance over temperature and voltage.

7.3.8 Overcurrent and Short-Circuit Protection

The LMR51460-Q1 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The high-side switch current is sensed when the high-side is turned on after a set blanking time. The high-side switch

current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. See *Functional Block Diagram* for more details. The peak current of high-side switch is limited by a clamped maximum peak current threshold I_{sc} which is constant.

The current going through low-side MOSFET is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down. The low-side switch is not turned OFF at the end of a switching cycle if the current is above the low-side current limit I_{LS_LIMIT} . The low-side switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the I_{LS_LIMIT}. Then the low-side switch is turned OFF and the high-side switch is turned on after a dead time. After I_{LS_LIMIT} is achieved, peak and valley current limit controls the maximum current deliver and can be calculated using the following equation.

$$I_{OUT\_MAX} = \frac{I_{LS\_LIMIT} + I_{SC}}{2} \quad (7)$$

If the feedback voltage is lower than 40% of the V_{REF}, the current of the low-side switch triggers I_{LS_LIMIT} for 128 consecutive cycles and hiccup current protection mode is activated. In hiccup mode, the converter shuts down and keeps off for a period of hiccup, T_{HICCUP} (96ms typical) before the LMR51460-Q1 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, prevents over-heating and potential damage to the device.

For FPWM version, the inductor current is allowed to go negative. When this current exceed the low-side negative current limit I_{LS_NEG}, the low-side switch is turned off and high-side switch is turned on immediately. This is used to protect the low-side switch from excessive negative current.

7.3.9 Soft Start

The integrated soft-start circuit prevents input inrush current impacting the LMR51460-Q1 and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. The typical soft-start time is 5ms.

7.3.10 Thermal Shutdown

The LMR51460-Q1 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 160°C. Both high-side and low-side FETs stop switching in thermal shutdown. After the die temperature falls below 140°C, the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMR51460-Q1. When V_{EN} is below 0.8V, the device is in shutdown mode. The LMR51460-Q1 also employs V_{IN} undervoltage lockout protection (UVLO). If V_{IN} voltage is below the UVLO threshold 3.4V, the converter is turned off.

7.4.2 Active Mode

The LMR51460-Q1 is in active mode when both V_{EN} and V_{IN} are above the respective operating threshold. The simplest way to enable the LMR51460-Q1 is to connect the EN pin to VIN pin. This allows self-start-up when the input voltage is in the operating range of 4V to 36V. See *Enable* for details on setting these operating levels.

In active mode, depending on the load current, the LMR51460-Q1 is in one of four modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is greater than half of the peak-to-peak inductor current ripple (for both PFM and FPWM versions)
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is less than half of the peak-to-peak inductor current ripple(only for PFM version)
3. Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM version)
4. Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM version)

7.4.3 CCM Mode

Continuous Conduction Mode (CCM) operation is employed in the LMR51460-Q1 when the load current is greater than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode, and the maximum output current of 6A can be supplied by the LMR51460-Q1.

7.4.4 Light-Load Operation (PFM Version)

For PFM version, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR51460-Q1 operates in Discontinuous Conduction Mode (DCM), also known as Diode Emulation Mode (DEM). In DCM operation, the low-side switch is turned off when the inductor current drops to I_{LS_ZC} (100mA typical) to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

During light load operation, Pulse Frequency Modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum high-side switch ON time t_{ON_MIN} or the minimum peak inductor current I_{PEAK_MIN} (1A for LMR51460-Q1) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to a significant drop in effective switching frequency.

7.4.5 Light-Load Operation (FPWM Version)

For FPWM version, LMR51460-Q1 is locked in PWM mode at full load range. This operation is maintained, even in no-load condition, by allowing the inductor current to reverse the normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LMR51460-Q1 is a step-down DC-to-DC converter. The device is typically used to convert a higher input voltage to a lower output DC voltage with a maximum output current of 6A. The following design procedure can be used to select components for the LMR51460-Q1. Alternately, the WEBENCH software can be used to generate complete designs. When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. Go to ti.com for more details.

注

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

8.2 Typical Application

The LMR51460-Q1 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. 図 8-1 shows a basic schematic.

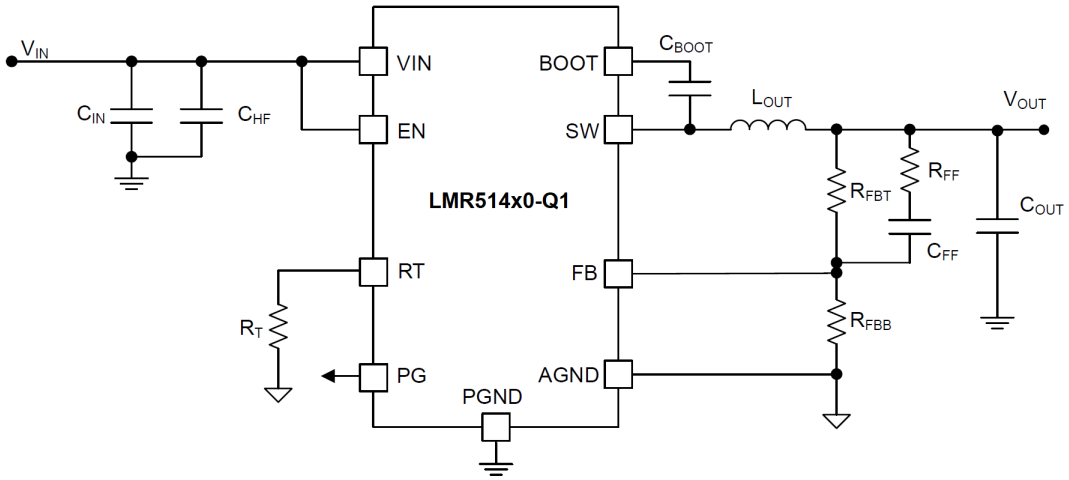


図 8-1. Application Circuit

The external components have to fulfill the needs of the application and the stability criteria of the control loop of the device. Use the following tables to simplify the output filter component selection.

表 8-1. L and C_{OUT} Typical Values for LMR51460-Q1

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (µF) (1)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{FF} (pF)	R_{FF} (kΩ)
440	3.3	3.3	2 × 68	100	31.6	33	1
	5	4.7	2 × 47	100	19.1	33	1
	12	8.2	2 × 22	100	7.15	33	1

(1) A ceramic capacitor is used in this table. All the C_{OUT} values are after derating.

8.2.1 Design Requirements

The detailed design procedure is described based on a design example. For this design example, use the parameters listed in the following table as the input parameters.

表 8-2. Design Example Parameters

PARAMETER	VALUE
Input voltage, V_{IN}	12V typical, range from 6V to 36V
Output voltage, V_{OUT}	5V ±3%
Maximum output current, I_{OUT_MAX}	6A
Output overshoot, undershoot 1.5A to 4.5A	5%
Output voltage ripple	0.5%
Operating frequency	440kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR51460-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Set-Point

The output voltage of the LMR51460-Q1 device is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Use the following equation to determine the output voltage of the converter:

$$R_{FBT} = \frac{(V_{OUT} - V_{REF})}{V_{REF}} \times R_{FBB} \quad (8)$$

Choose the value of R_{FBB} to be 19.1kΩ. With the desired output voltage set to 5V and the V_{REF} = 0.8V, the R_{FBT} value can then be calculated using 式 8. The formula yields to a value 100.28kΩ, a standard value of 100kΩ is selected.

8.2.2.3 Switching Frequency

The higher switching frequency allows for lower value inductors and smaller output capacitors, which results in smaller design size and lower component cost. However, higher switching frequency brings more switching loss, making the design less efficient and produce more heat. The switching frequency is also limited by the minimum on-time of the integrated power switch, the input voltage, the output voltage, and the frequency shift limitation as mentioned in *Minimum ON-Time, Minimum OFF-Time, and Frequency Foldback.*

For this example, a switching frequency of 440kHz is selected. RT open defaults to 440kHz.

8.2.2.4 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use 式 10 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} must be 20% to 60% of maximum I_{OUT} supported by converter. During an instantaneous overcurrent operation event, the RMS and peak inductor current can be high. The inductor saturation current must be higher than peak current limit level.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \tag{9}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{10}$$

In general, choosing lower inductance in switching power supplies is preferable because lower inductance usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. Too low of an inductance also generates more inductor core loss because the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, TI recommends to have adequate amount of inductor ripple current. A larger inductor ripple current improves the comparator signal-to-noise ratio.

For this design example, choose K_{IND} = 0.35. The minimum inductor value is calculated to be 4.66µH. Choose the nearest standard 4.7µH power inductor with a capability of 7.2A RMS current and 10A saturation current.

8.2.2.5 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. Minimize the output capacitance to keep cost and size down. The output capacitor or capacitors, C_{OUT}, must be chosen with care because capacitor or capacitors directly affects the steady state output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient. The output voltage ripple is essentially composed of two parts. One part is caused by the inductor ripple current flowing through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \tag{11}$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{12}$$

The two components of the voltage ripple are not in-phase, therefore, the actual peak-to-peak ripple is less than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rates. When a large load step occurs, output capacitors provide the required charge before the inductor current can slew to an appropriate level. The control loop of the converter usually requires eight or more clock cycles to regulate the inductor current equal to the new load level during this time. The output capacitance must be large enough to supply the current difference for 6 clock cycles to maintain the output voltage within the specified range. The following equation shows the minimum output capacitance needed for a specified V_{OUT} overshoot and undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{6 \times (I_{OH} - I_{OL})}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \tag{13}$$

where

- K_{IND} = Ripple ratio of the inductor current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{OUT_SHOOT} = Target output voltage overshoot or undershoot

For this design example, the target output ripple is 25mV. Assuming $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 25mV, choose K_{IND} = 0.35. 式 11 yields ESR no larger than 11.9mΩ and 式 12 yields C_{OUT} no smaller than 23.9µF. For the target overshoot and undershoot limitation of this design, ΔV_{OUT_SHOOT} is 250mV. The C_{OUT} can be calculated to be no less than 81.8µF by 式 13. In summary, the most stringent criteria for the output capacitor is 81.8µF. Considering derating, two 47µF, 16V, X7R ceramic capacitor with 10mΩ ESR is used.

8.2.2.6 Input Capacitor Selection

The LMR51460-Q1 device requires a high frequency input decoupling capacitor or capacitor. The typical recommended value for the high frequency decoupling capacitor is 10µF or higher. TI recommends a high-quality ceramic type X5R or X7R with sufficiency voltage rating. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage. For this design, two 4.7µF, X7R dielectric capacitor rated for 50V is used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 10mΩ. Include a capacitor with a value of 0.1µF for high-frequency filtering and place as close as possible to the device pins.

8.2.2.7 Bootstrap Capacitor

Every LMR51460-Q1 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.1µF and rated at 16V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.8 Undervoltage Lockout Setpoint

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. The following equation can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{EBT} + R_{ENB}}{R_{ENB}} \tag{14}$$

The EN rising threshold (V_{ENH}) for LMR51460-Q1 is set to be 1.25V (typical). Choose a value of 21.5kΩ for R_{ENB} to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6.0V, then the value of R_{ENT} can be calculated using the following equation:

$$R_{EBT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1\right) \times R_{ENB} \tag{15}$$

The above equation yields a value of 81.7kΩ, a standard value of 82kΩ is selected. The resulting falling UVLO threshold, equals 4.8V, can be calculated by the following equation where EN hysteresis voltage, V_{EN_HYS}, is 0.25V (typical).

$$V_{IN\_FALLING} = \left(V_{ENH} - V_{ENH\_HYS}\right) \times \frac{R_{EBT} + R_{ENB}}{R_{ENB}} \tag{16}$$

8.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 440kHz, L = 4.7µH, C_{OUT} = 2 × 47µF, T_A = 25°C.

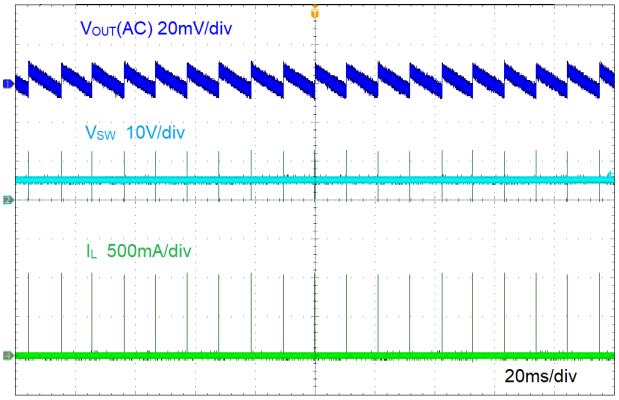


図 8-2. Ripple at No Load

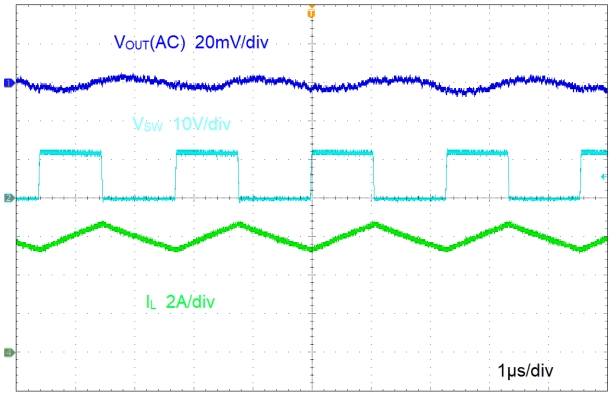


図 8-3. Ripple at Full Load

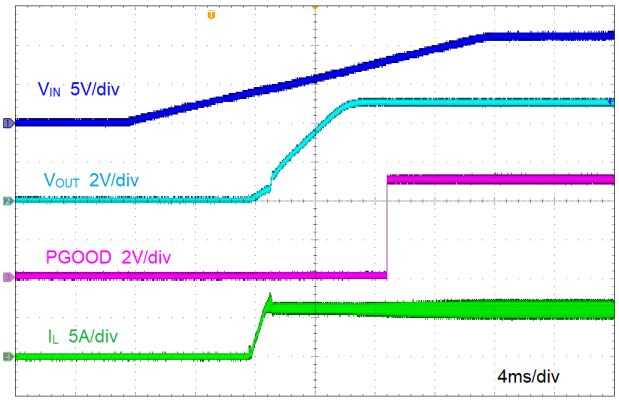


図 8-4. Start-Up by V_{IN}

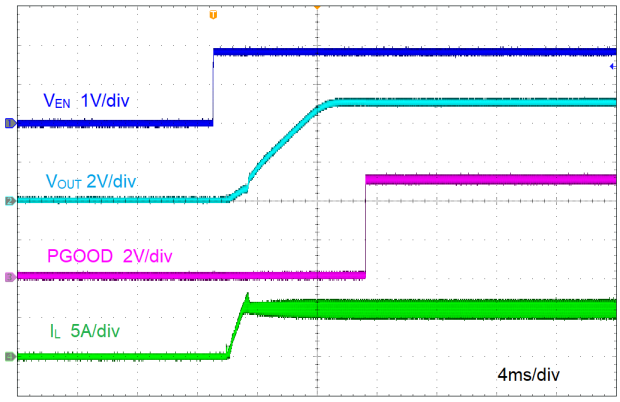


図 8-5. Start-Up by EN

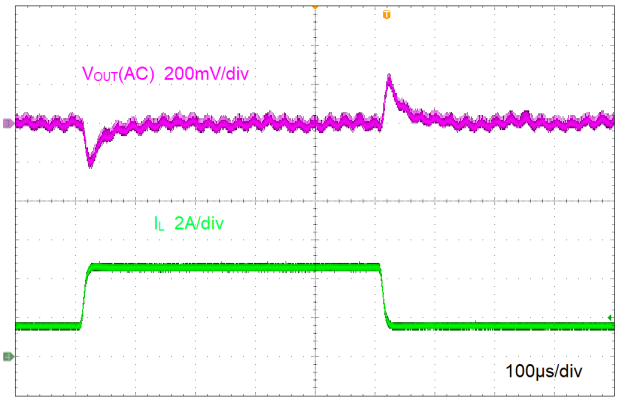


図 8-6. Load Transient

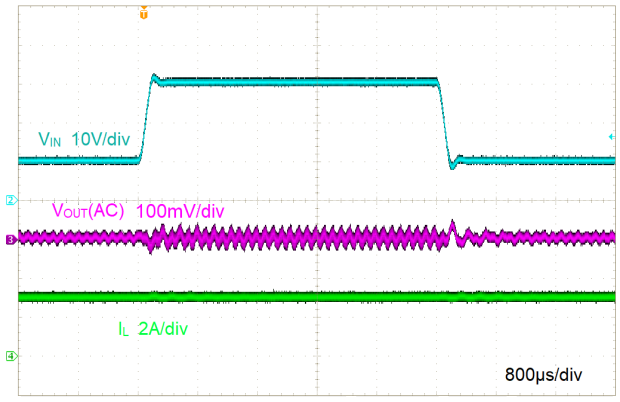


図 8-7. Line Transient

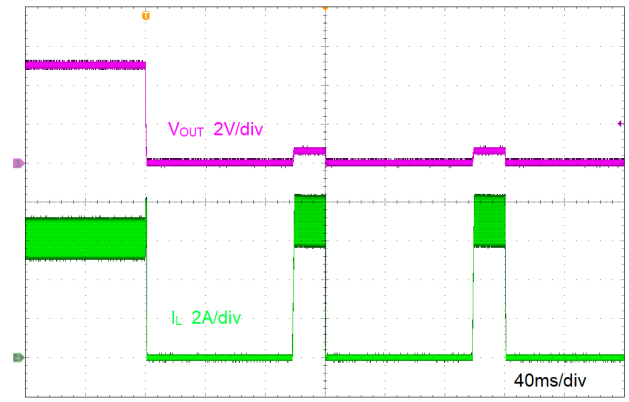


図 8-8. Short Protection

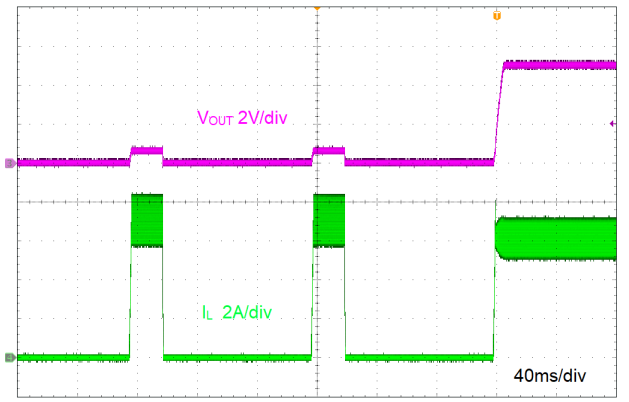


図 8-9. Short Recovery

8.3 Power Supply Recommendations

The LMR51460-Q1 is designed to operate from an input voltage supply range between 4V and 36V. This input supply must be well-regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR51460-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR51460-Q1 additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47µF to 100µF electrolytic capacitor is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Place the input bypass capacitor C_{IN} as close as possible to the VIN and PGND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the PGND pin.
2. Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB}, must be located close to the FB pin. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
3. Use ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
4. Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
5. Provide adequate device heat-sinking. Use an array of heat-sinking vias to connect the top side ground plane to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Make sure enough copper area is used for heat-sinking to keep the junction temperature below 150°C.

8.4.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing a ceramic bypass capacitor or capacitors as close as possible to the VIN and PGND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{OUT} end of the inductor and closely grounded to PGND pin.

8.4.1.2 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, make sure to place the resistor divider close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so the FB pin is a high impedance node and very sensitive to noise. Placing the resistor divider closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provides the best output accuracy. The voltage sense trace from the load to the feedback resistor divider must be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high value resistors are used to set the output voltage. TI recommends to route the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This action provides further shielding for the voltage feedback path from EMI noises.

8.4.2 Layout Example

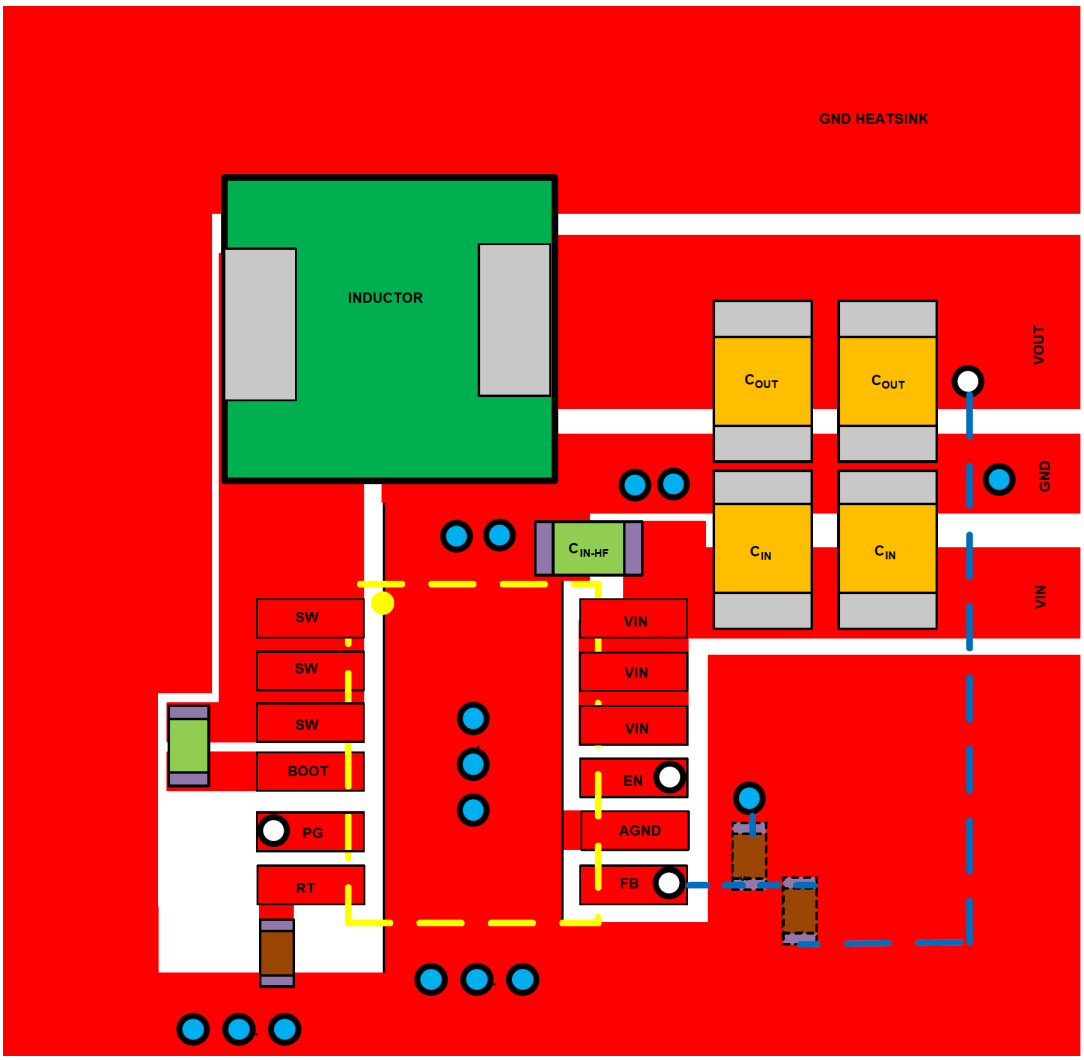


図 8-10. Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR51460-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Layout Guidelines for Switching Power Supplies* application note
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- Texas Instruments, *How to Properly Evaluate Junction Temperature with Thermal Metrics* application note

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

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この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

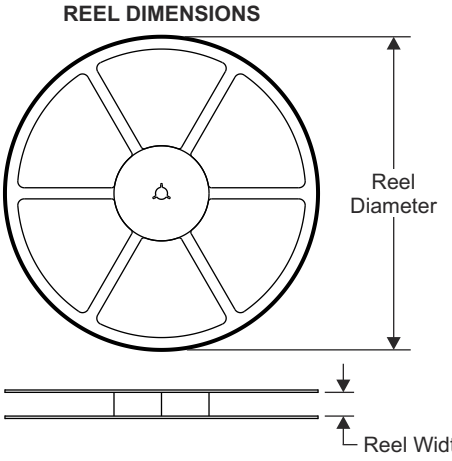
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

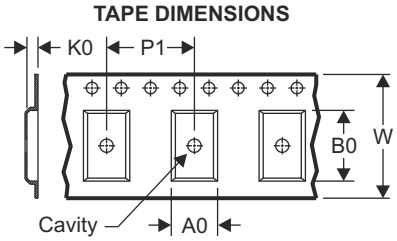
DATE	REVISION	NOTES
August 2024	*	Initial release

11 Mechanical, Packaging, and Orderable Information

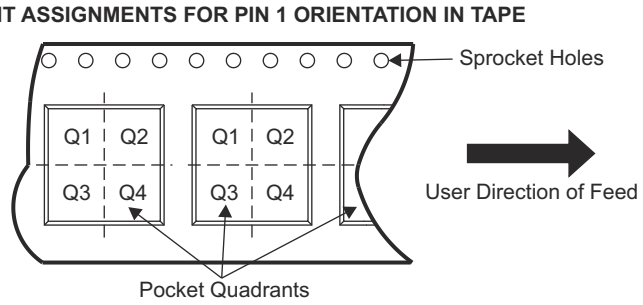
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information



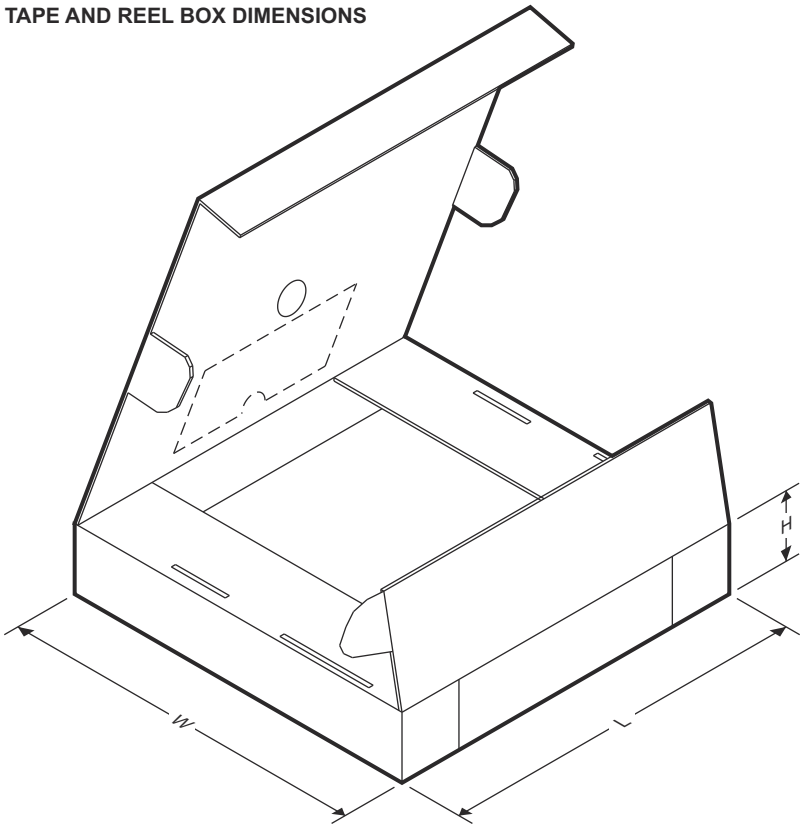


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR51460SQDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMR51460FSQDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



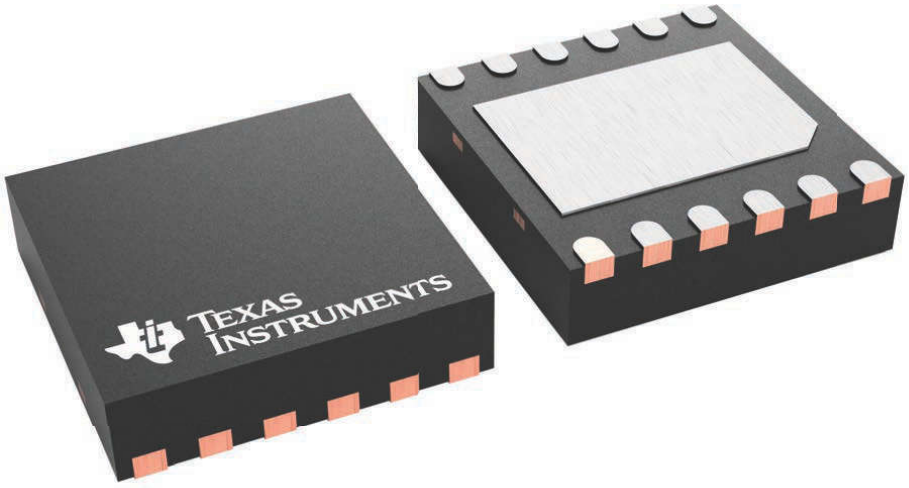
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR51460SQDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0
LMR51460FSQDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

DRR 12 — **WSON - 0.8 mm max height**

3 x 3, 0.5 mm pitch — PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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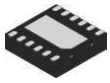
TEXAS INSTRUMENTS
www.ti.com

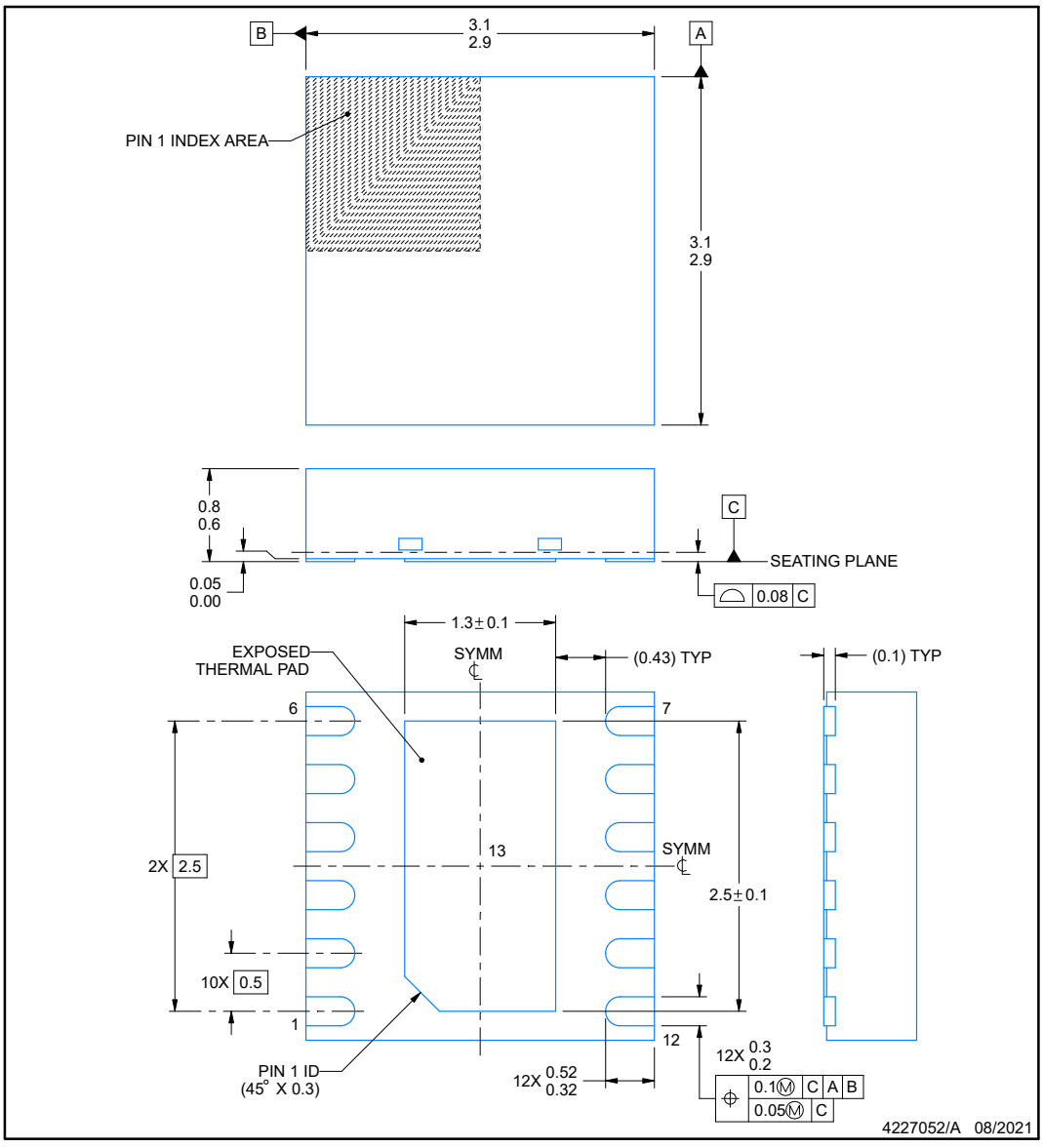
PACKAGE OUTLINE

DRR0012G



WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



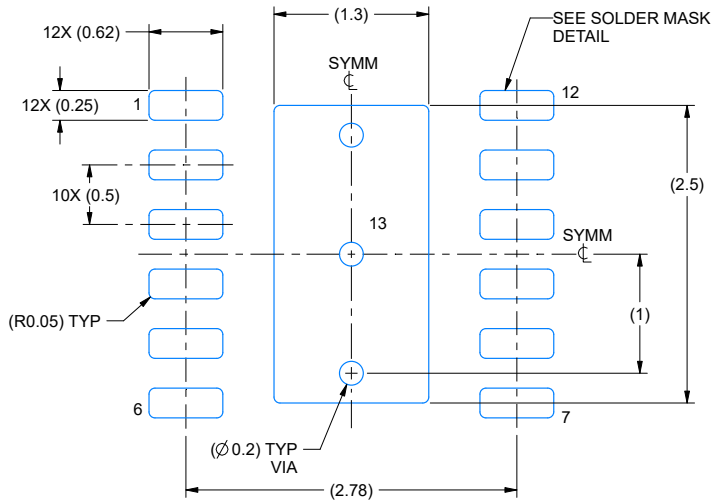
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

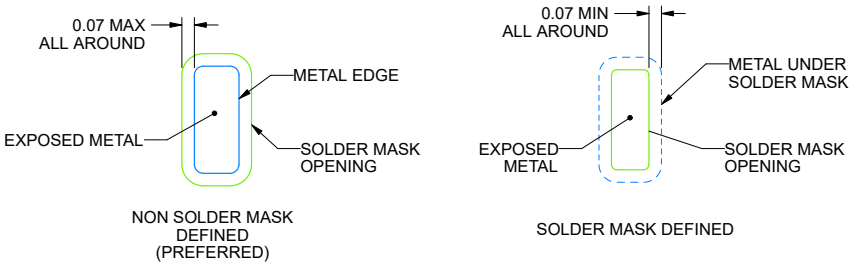
EXAMPLE BOARD LAYOUT

DRR0012G — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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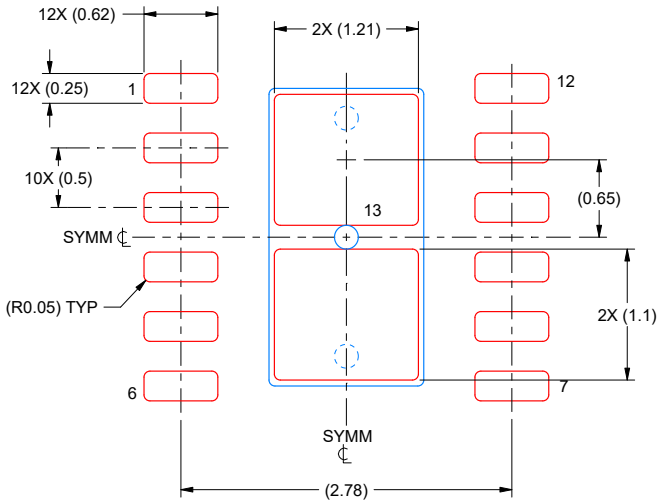
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRR0012G — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 13
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227052/A 08/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR51460FSQDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L146FQ	Samples
LMR51460SQDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L146SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

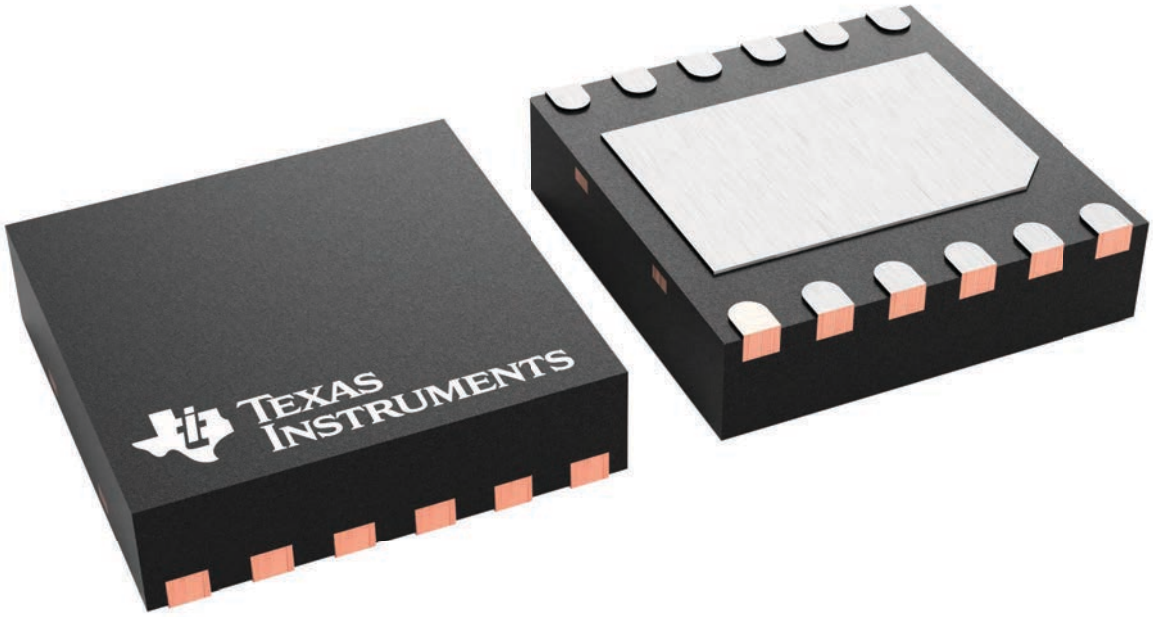
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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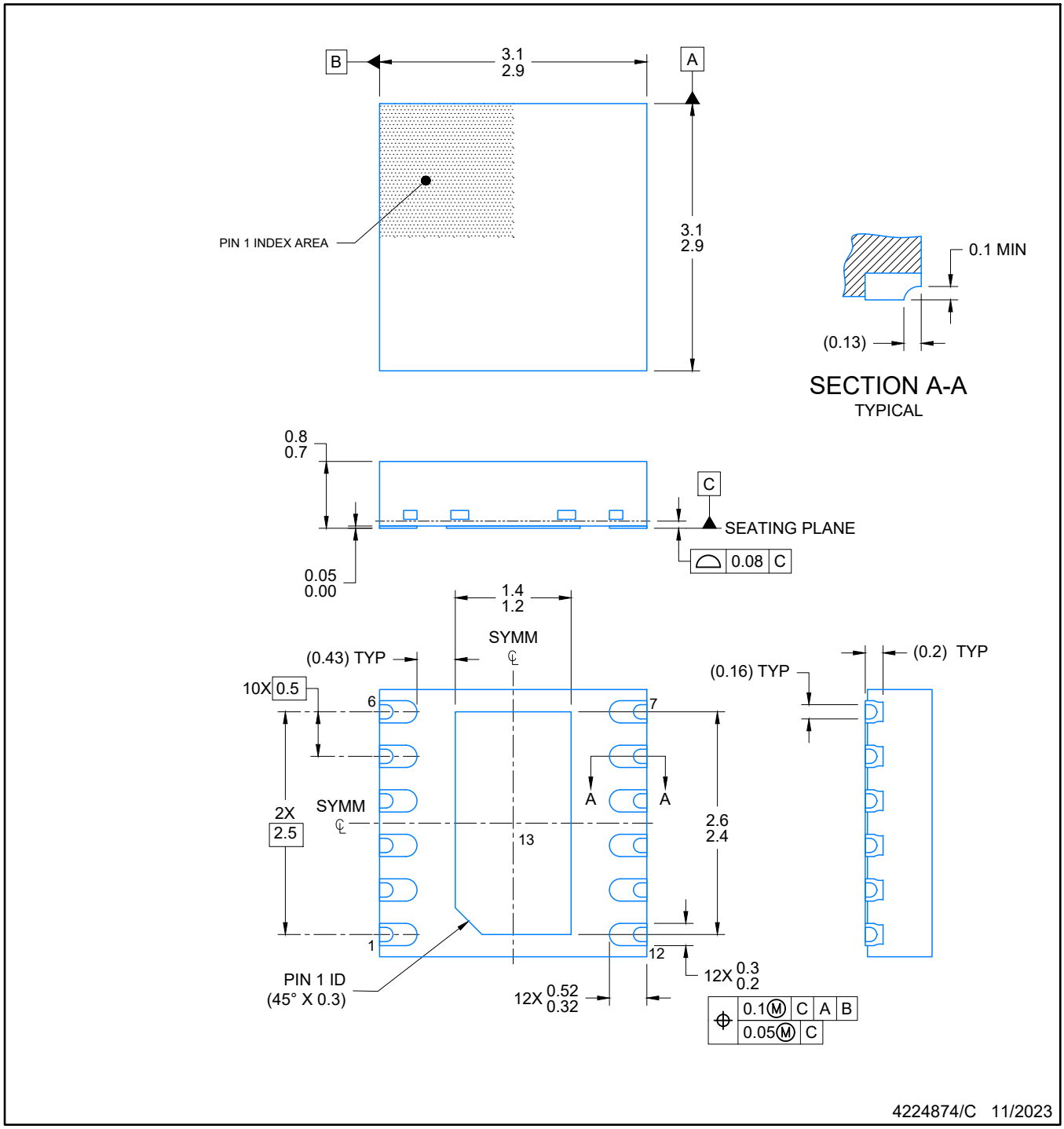
PACKAGE OUTLINE

DRR0012E

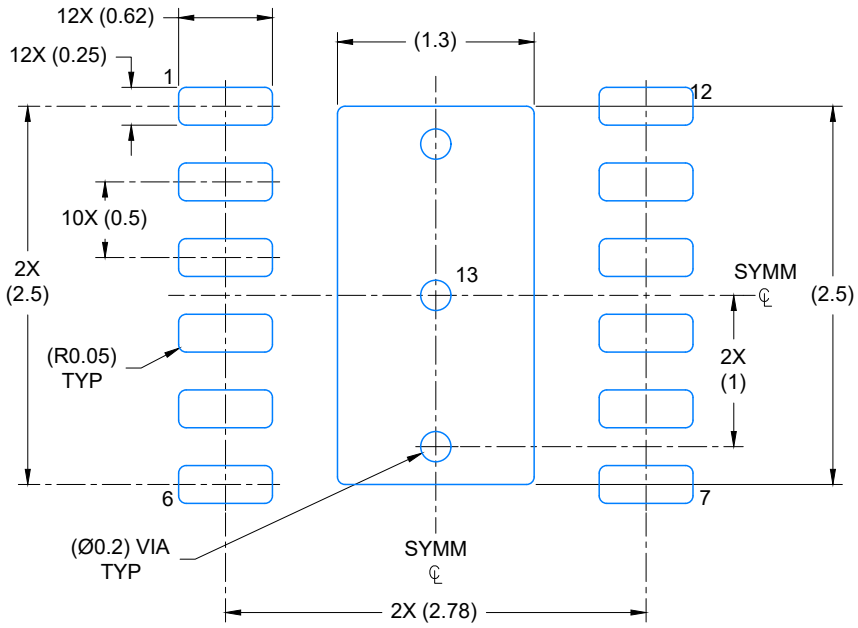
WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

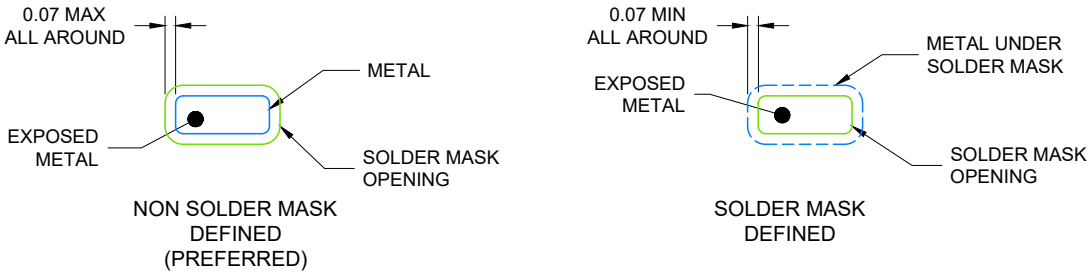


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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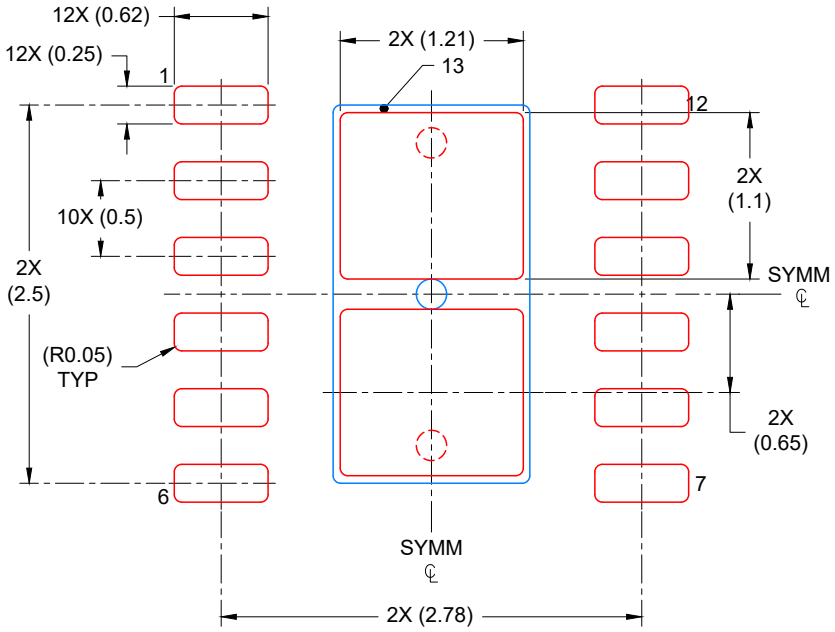
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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