LMR50410-Q1 SIMPLE SWITCHER® 4V～36V、1A 降圧コンバータ、SOT-23-6 パッケージ

1 特長

- AEC-Q100 準拠
  - 温度グレード 1:-40℃～125℃ の動作時周囲温度範囲
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 堅牢な車載アプリケーション向けの構成
  - 入力電圧範囲:4V～36V
  - 1A の連続出力電流
  - 最小限のスイッチング・オンタイム:60ns
  - 固定スイッチング周波数:2.1MHz
  - 接合部温度範囲:–40℃～150℃
  - 最大デューティ・サイクル:98%
  - あらかじめ出力にバイアスが印加された状態でも単調にスタートアップ
  - ヒカップ・モードによる短絡保護を内蔵
  - 基準電圧の許容誤差:±1%
  - 高精度のイネーブル
- 小型のソリューションと使いやすさ
  - 同期整流器内蔵
  - 設計を容易にする内部補償
  - SOT-23-6 パッケージ
- TPS560430-Q1 とピン互換
- ピン互換パッケージの各種オプション
  - PFM および強制 PWM (FPWM) オプション
  - 5V および 3.3V 固定出力オプション
- WEBENCH® Power Designer により、LMR50410-Q1 を使用するカスタム設計を作成

2 アプリケーション

- ボディ・エレクトロニクス / 照明
- インフォテインメントとクラスタ
- 先進運転支援システム (ADAS)
- V_{IN} が広い汎用電源

3 説明

LMR50410-Q1 は、最大 1A の負荷電流を駆動でき、V_{IN} が広く使いやすい同期整流式降圧コンバータです。このデバイスは 4V～36V の広い入力電圧範囲で動作し、非レギュレーション電源からの電源調整を行うさまざまな車載用アプリケーションに適しています。

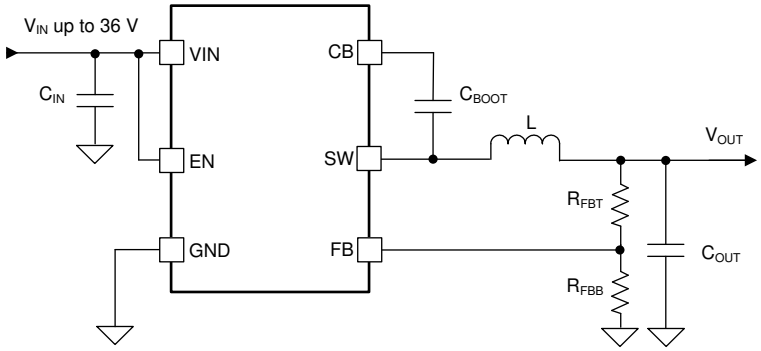
LMR50410-Q1 は 2.1MHz のスイッチング周波数で動作するため、比較的小型のインダクタを使用でき、ソリューション・サイズの最適化が可能です。PFM バージョンにより軽負荷時に高効率を実現し、FPWM バージョンにより一定の周波数を維持しながら、全負荷範囲にわたって出力電圧リップルを小さくできます。ソフトスタートと補償回路が内部に実装されており、最小限の外付け部品のみでデバイスを使用できます。

このデバイスには、サイクル単位の電流制限、ヒカップ・モード短絡保護、過剰な電力消費時のサーマル・シャットダウンなどの保護機能が組み込まれています。LMR50410-Q1 は、SOT-23-6 パッケージで供給されます。

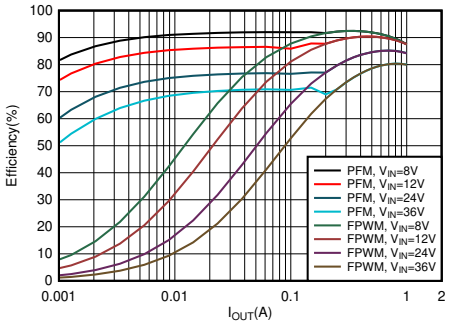
製品情報

型番	パッケージ(1)	本体サイズ (公称)
LMR50410-Q1	SOT-23-6	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



効率と出力電流との関係 V_{OUT} = 5V、2.1kHz

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (July 2020) to Revision A (November 2020)	Page
• Added FPWM OPNs	3
• Added $V_{OUT\text{-}3.3V\text{-}Fixed}$, $V_{OUT\text{-}5V\text{-}Fixed}$, $I_{LKG\text{-}VOUT\text{-}3.3V\text{-}Fixed}$, and $I_{LKG\text{-}VOUT\text{-}5V\text{-}Fixed}$ for new OPNs	5
• Updated *Overview* with FPWM version	10
• Updated *Overcurrent and Short Circuit Protection* with FPWM version	14
• Updated *Active Mode* with FPWM version	16

5 Device Comparison Table

ORDERABLE PART NUMBER	FREQUENCY	PFM OR FPWM	OUTPUT
LMR50410YQDBVRQ1	2.1 MHz	PFM	Adjustable
LMR50410YFQDBVRQ1	2.1 MHz	FPWM	Adjustable
LMR50410Y3FQDBVRQ1	2.1 MHz	FPWM	3.3 V
LMR50410Y5FQDBVRQ1	2.1 MHz	FPWM	5.0 V

6 Pin Configuration and Functions

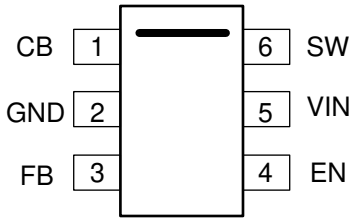


図 6-1. 6-Pin SOT-23-6 DBV Package (Top View)

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO		
CB	1	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100-nF capacitor from this pin to the SW pin.
GND	2	G	Power ground terminals, connected to the source of low-side FET internally. Connect to system ground, ground side of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
FB	3	A	Feedback input to the converter. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation. For fixed output version, directly connect to output point.
EN	4	A	Precision enable input to the converter. Do not float. High = on, low = off. Can be tied to VIN. Precision enable input allows adjustable UVLO by external resistor divider.
VIN	5	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
SW	6	P	Switching output of the converter. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.

(1) A = Analog, P = Power, G = Ground.

7 Specifications

7.1 Absolute Maximum Ratings

Over junction temperature range of -40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to GND	–0.3	38	V
	EN to GND	–0.3	V_{IN}+0.3	V
	FB to GND	–0.3	5.5	V
Output voltage	SW to GND	–0.3	V_{IN}+0.3	V
	SW to GND less than 10-ns transients	–3.5	38	V
	CB to SW	–0.3	5.5	V
Junction Temperature T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)(1)	Human body model (HBM)(1)	±2500	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM)	Charged device model (CDM)	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40 °C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to GND	4	36	V
	EN to GND(2)	0	VIN	V
Output voltage	V_{OUT} (3) (4)	1	28	V
Output current	I_{OUT}	0	1	A

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) Under no conditions should the output voltage be allowed to fall below zero volts.
(4) Maximum V_{OUT} ensured up to 90% of V_{IN} in final production.

7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, with a 2-layer PCB, a $R_{\theta JA}$ = 80°C/W can be achieved. For design information see Maximum Output Current versus Ambient Temperature.

THERMAL METRIC(1)		LMR50410 DBV(SOT-23-6) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	173	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	116	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20	°C/W

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, with a 2-layer PCB, a $R_{\theta JA}$ = 80°C/W can be achieved. For design information see Maximum Output Current versus Ambient Temperature.

THERMAL METRIC(1)		LMR50410 DBV(SOT-23-6) 6 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	30	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4 V to 36 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN_UVLO}	Undervoltage lockout thresholds	Rising threshold	3.55	3.75	4	V
		Falling threshold	3.25	3.45	3.65	V
		Hysteresis		0.3		V
$I_{Q\text{-}nonSW}$	Operating quiescent current (non-switching)(2)	V_{EN} = 3.3 V, VFB=1.1V (PFM variant only)		80	120	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0 V		3	10	µA
ENABLE (EN PIN)						
$V_{EN\text{-}VOUT\text{-}H}$	Enable input high-level for V_{OUT}	V_{ENABLE} rising	1.1	1.23	1.36	V
$V_{EN\text{-}VOUT\text{-}L}$	Enable input low-level for V_{OUT}	V_{ENABLE} falling	0.95	1.1	1.22	V
$V_{EN\text{-}VOUT\text{-}HYS}$	Enable input hysteresis for V_{OUT}	Hysteresis		130		mV
$I_{LKG\text{-}EN}$	Enable input leakage current	V_{EN} = 3.3V		10	200	nA
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage		0.99	1	1.01	V
$V_{OUT\text{-}3.3V\text{-}Fixed}$	Output voltage	Vin=12V	3.25	3.3	3.35	V
$V_{OUT\text{-}5V\text{-}Fixed}$	Output voltage	Vin=12V	4.925	5.0	5.075	V
$I_{LKG\text{-}FB}$	Feedback leakage current	FB = 1.2 V		0.2		nA
$I_{LKG\text{-}VOUT\text{-}3.3V\text{-}Fixed}$	Feedback leakage current	V_{OUT} = 3.3 V (Fixed Option)		1.7		µA
$I_{LKG\text{-}VOUT\text{-}5V\text{-}Fixed}$	Feedback leakage current	V_{OUT} = 5V (Fixed Option)		2.6		µA
CURRENT LIMITS AND HICCUP						
I_{SC}	High-side current limit(3)	Vin=12V	1.25	1.6	1.9	A
$I_{LS\text{-}LIMIT}$	Low-side current limit(3)	Vin=12V	0.9	1.1	1.3	A
$I_{L\text{-}ZC}$	Zero cross detector threshold	PFM variants only		0.02		A
$I_{L\text{-}NEG}$	Negative current limit(3)	FPWM variant only		–0.6		A
MOSFETS						
$R_{DS\text{-}ON\text{-}HS}$	High-side MOSFET ON-resistance	T_J=25 °C, V_{IN} = 12 V		450		mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low-side MOSFET ON-resistance	T_J=25 °C, V_{IN} = 12 V		240		mΩ
THERMAL SHUTDOWN						
$T_{SD\text{-}Rising}$ (1)	Thermal shutdown	Shutdown threshold		170		°C

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4 V to 36 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{SD-Falling}$ (1)	Thermal shutdown	Recovery threshold		158		°C

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range verified through correlation using
Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

7.6 Timing Requirements

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4 V- 36 V.

PARAMETER		TEST CONDTIONS	MIN	TYP	MAX	UNIT
t_{ON-MIN}	Minimum switch on-time	I_{OUT}=1A		60		ns
$t_{OFF-MIN}$	Minimum switch off-time	I_{OUT}=1A		110		ns
t_{ON-MAX}	Maximum switch on-time			7.5		µs
t_{SS}	Internal soft-start time			1.8		ms
t_{HC}	Time between current-limit hiccup burst			135		ms

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range verified through correlation using
Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

7.7 Switching Characteristics

T_J = -40°C to 150°C, V_{IN} = 4 V-36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
F_{OSC}	Internal oscillator frequency	2.1-MHz variant	1.8	2.1	2.4	MHz

7.8 System Characteristics

The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to TJ = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of TJ = -40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range		4		36	V
V_{OUT}	Adjustable output voltage regulation(1)	PFM operation	–1.5%		2.5%	
V_{OUT}	Adjustable output voltage regulation(1)	FPWM operation	–1.5%		1.5%	
I_{SUPPLY}	Input supply current when in regulation	V_{IN} =12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, R_{FBT} = 1 MΩ, PFM variant		90		µA
D_{MAX}	Maximum switch duty cycle(2)			98%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_D	Switch voltage dead time			2		ns
T_{SD}	Thermal shutdown temperature	Shutdown temperature		170		°C

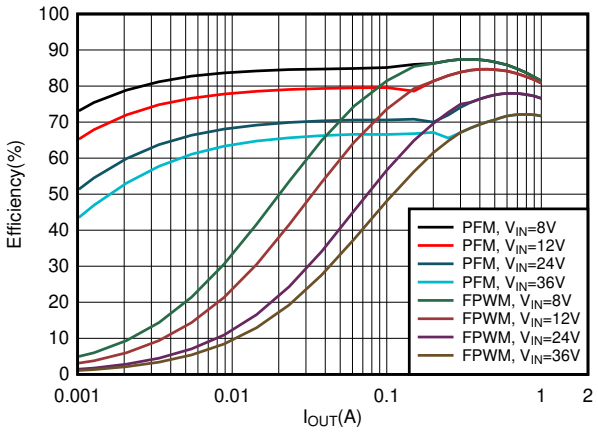
The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to TJ = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of TJ = -40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown temperature	Recovery temperature		158		°C

(1) Deviation in V_{OUT} from nominal output voltage value at V_{IN} = 24 V, I_{OUT} = 0 A to full load
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: $F_{MIN} = 1 / (t_{ON-MAX} + t_{OFF-MIN})$. $D_{MAX} = t_{ON-MAX} / (t_{ON-MAX} + t_{OFF-MIN})$.

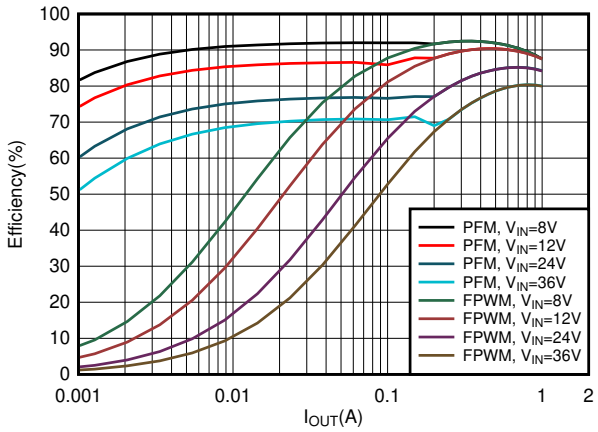
7.9 Typical Characteristics

V_{IN} = 12 V, f_{SW}= 2.1 Mhz ,T_A = 25°C, unless otherwise specified.



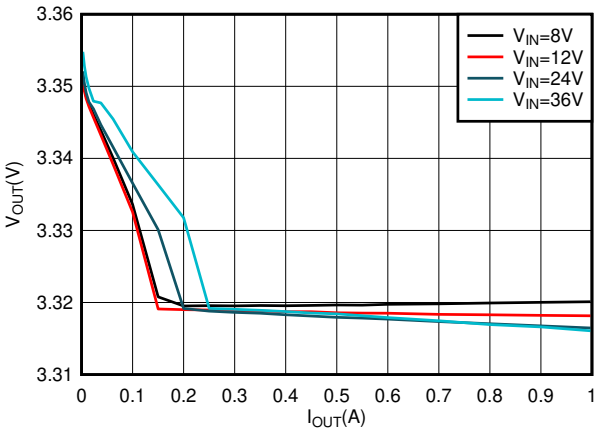
f_{SW} = 2.1 MHz V_{OUT} = 3.3 V

図 7-1. 3.3-V Efficiency versus Load Current



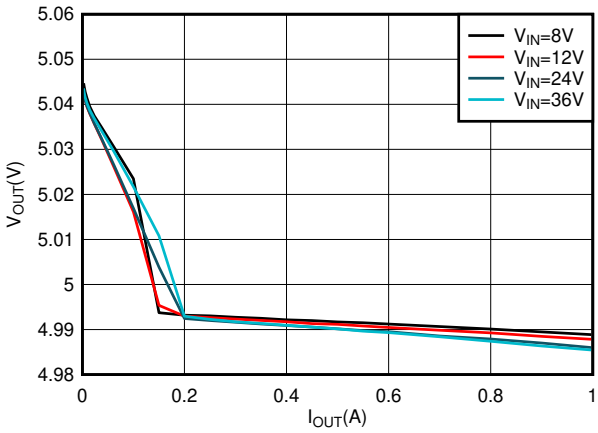
f_{SW} = 2.1 MHz V_{OUT} = 5 V

図 7-2. 5-V Efficiency versus Load Current



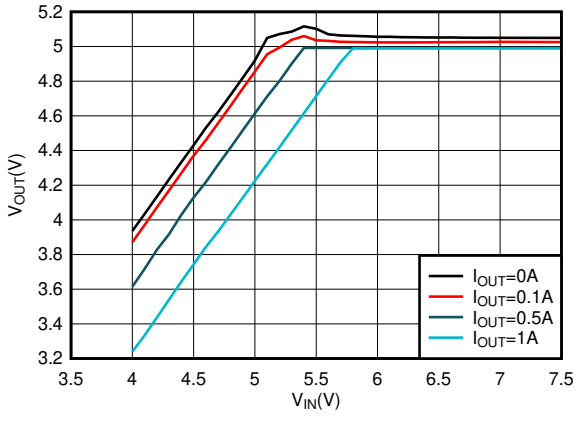
f_{SW} = 2.1 MHz V_{OUT} = 3.3 V PFM version

図 7-3. 3.3-V Load Regulation



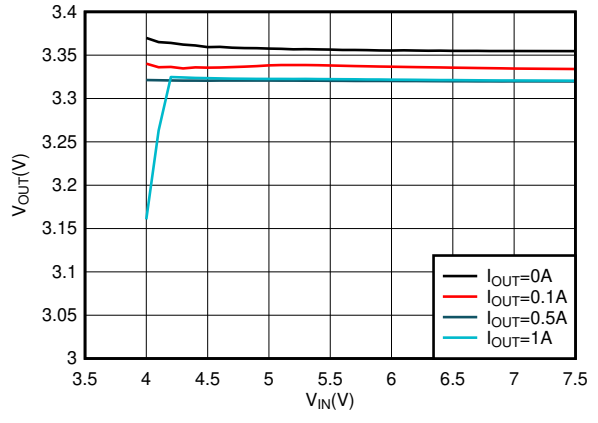
f_{SW} = 2.1 MHz V_{OUT} = 5 V PFM version

図 7-4. 5-V Load Regulation



f_{SW} = 2.1 MHz V_{OUT} = 5 V PFM version

図 7-5. 5-V Dropout



f_{SW} = 2.1 MHz V_{OUT} = 3.3 V PFM version

図 7-6. 3.3-V Dropout

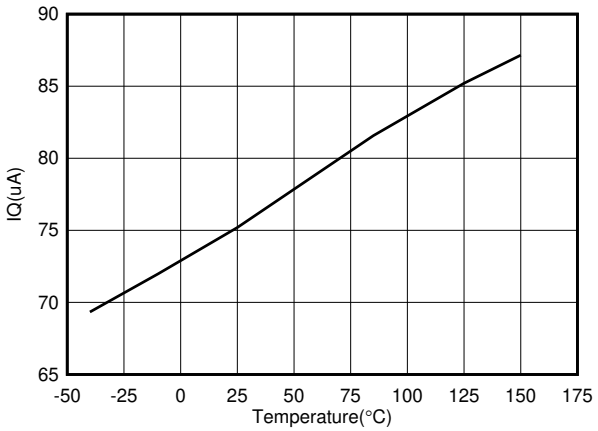


図 7-7. I_Q versus Temperature

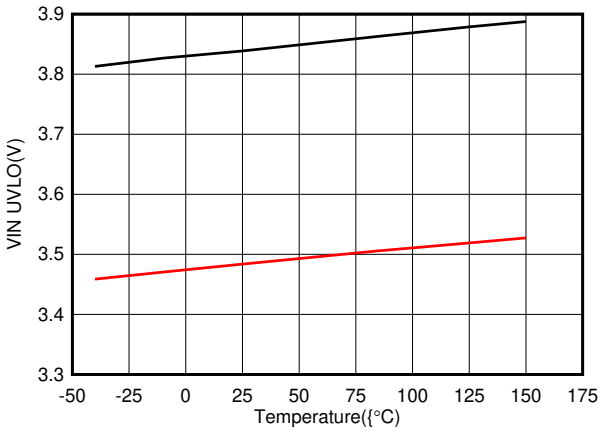


図 7-8. V_{IN} UVLO versus Temperature

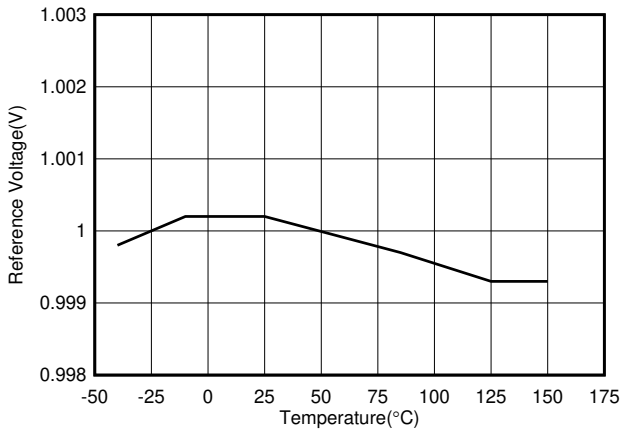


図 7-9. Reference Voltage versus Temperature

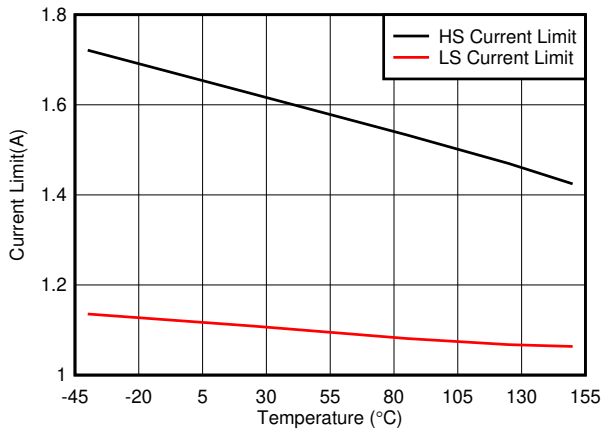


図 7-10. HS and LS Current Limit versus Temperature

8 Detailed Description

8.1 Overview

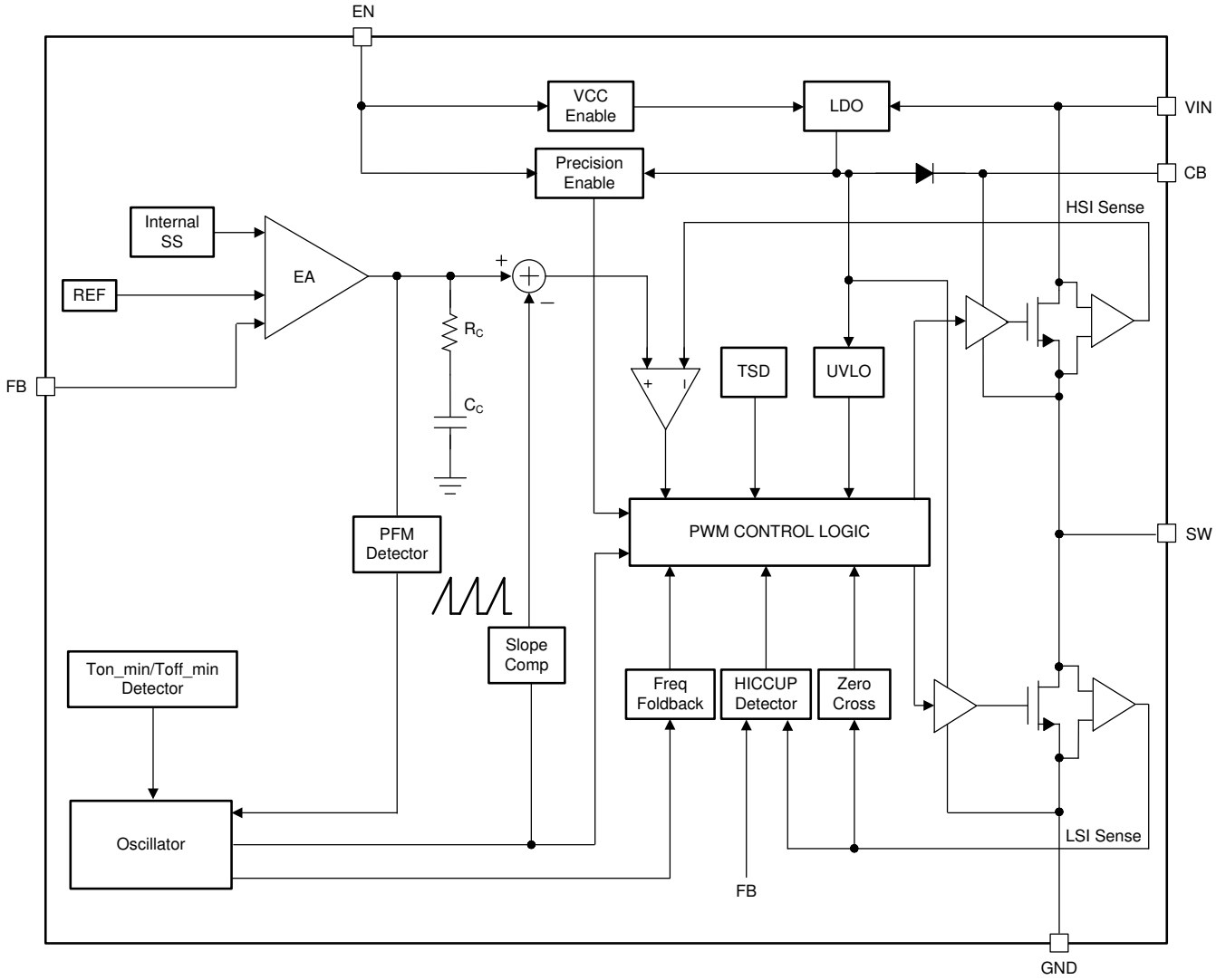
The LMR50410-Q1 converter is an easy-to-use synchronous step-down DC-DC converter operating from a 4-V to 36-V supply voltage. It is capable of delivering up to 1-A DC load current in a very small solution size. The family has multiple versions applicable to various applications. See セクション 5 for detailed information.

The LMR50410-Q1 employs fixed-frequency peak-current mode control. The PFM version enters PFM Mode at light load to achieve high efficiency. A FPWM version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. The device is internally compensated, which reduces design time and requires few external components.

Additional features such as precision enable and internal soft start provide a flexible and easy-to-use solution for a wide range of applications. Protection features include thermal shutdown, V_{IN} undervoltage lockout, cycle-by-cycle current limit, and hiccup mode short-circuit protection.

This family of devices requires very few external components and has a pin-out designed for simple, optimum PCB layout.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency Peak Current Mode Control

The following operating description of the LMR50410-Q1 refers to *セクション 8.2* and to the waveforms in 図 8-1. The LMR50410-Q1 is a step-down synchronous buck converter with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR50410-Q1 supplies a regulated output voltage by turning on the high-side and low-side NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current, i_L, increases with linear slope (V_{IN} – V_{OUT}) / L. When the high-side switch is turned off by the control logic, the low-side switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the low-side switch with a slope of –V_{OUT} / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

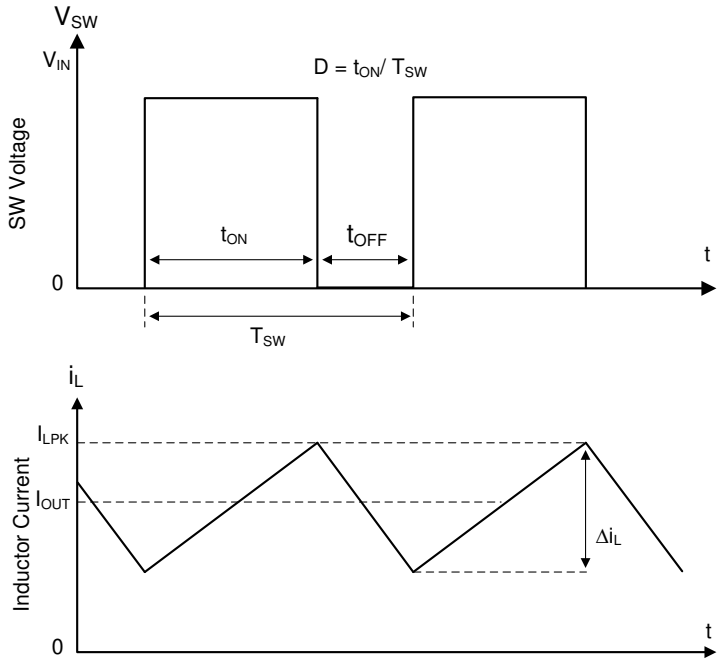


図 8-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR50410-Q1 employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally-compensated, which allows for fewer external components, making designing easy, and providing stable operation when using a variety of output capacitors. The converter operates with fixed switching frequency at normal load conditions. During light-load condition, the LMR50410-Q1 operates in PFM mode to maintain high efficiency (PFM version) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM version).

8.3.2 Adjustable Output Voltage

A precision 1.0-V reference voltage (V_{REF}) is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from V_{OUT} to the FB pin. It is recommended to use 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor R_{FBB} for the desired divider current and use 式 1 to calculate top-side resistor R_{FBT}. The recommend range for R_{FBT} is 10 kΩ to 100 kΩ. A lower R_{FBT} value can be used if pre-loading is desired to reduce V_{OUT} offset in PFM operation. Lower R_{FBT} reduces efficiency at very light load. Less static current goes through a larger R_{FBT} and can be more desirable when light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended because it makes the feedback path more susceptible to noise. Larger R_{FBT} values require more carefully designed feedback path trace from the feedback resistors to the feedback pin of the device. The tolerance and temperature variation of the resistor divider network affect the output voltage regulation.

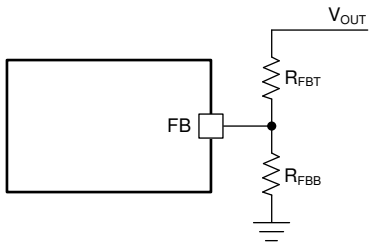


図 8-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

8.3.3 Enable

The voltage on the EN pin controls the ON/OFF operation of the LMR50410-Q1. A voltage of less than 0.95 V shuts down the device, while a voltage of greater than 1.36 V is required to start the converter. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR50410-Q1 is to connect the EN to VIN. This allows self-start-up of the LMR50410-Q1 when V_{IN} is within the operating range.

Many applications benefit from the employment of an enable divider R_{ENT} and R_{ENB} (図 8-3) to establish a precision system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, ensuring reliable operation, or supplying protection, such as a battery discharge level. An external logic signal can also be used to drive EN input for system sequencing and protection. Note, the EN pin voltage must not to be greater than V_{IN} + 0.3 V. It is not recommended to apply EN voltage when V_{IN} is 0 V.

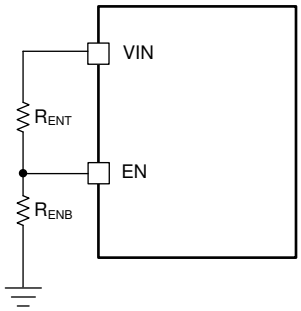


図 8-3. System UVLO by Enable Divider

8.3.4 Minimum ON-Time, Minimum OFF-Time, and Frequency Foldback

Minimum ON-time (T_{ON_MIN}) is the shortest duration of time that the high-side switch can be turned on. T_{ON_MIN} is typically 60 ns for the LMR50410-Q1. Minimum OFF-time (T_{OFF_MIN}) is the shortest duration of time that the high-side switch can be off. T_{OFF_MIN} is typically 110 ns. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \quad (2)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \quad (3)$$

Given a required output voltage, the maximum V_{IN} without frequency foldback can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times T_{ON\_MIN}} \quad (4)$$

The minimum V_{IN} without frequency foldback can be calculated by:

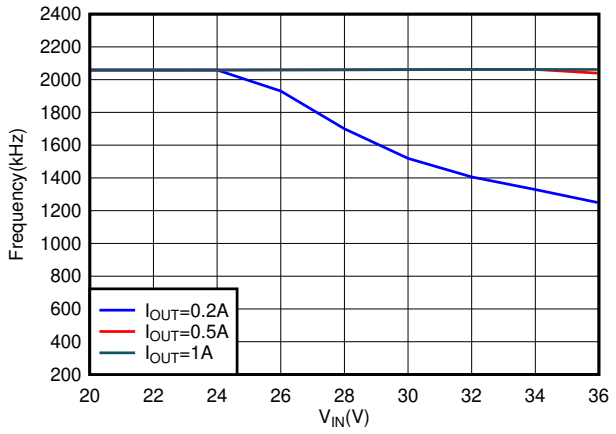
$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times T_{OFF\_MIN}} \quad (5)$$

In the LMR50410-Q1, a frequency foldback scheme is employed once the T_{ON_MIN} or T_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on-time decreases while V_{IN} voltage increases. Once the on-time decreases to T_{ON_MIN}, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to Equation 2.

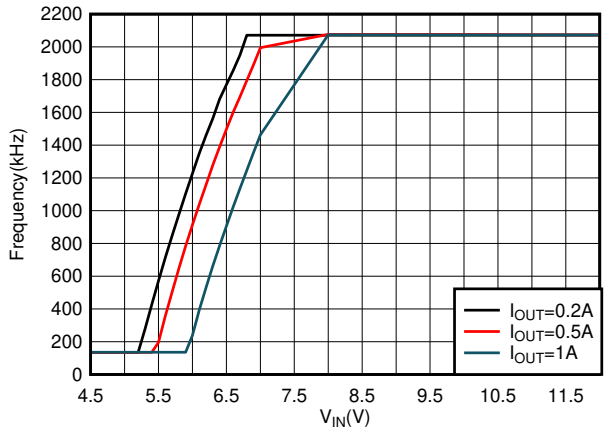
The frequency foldback scheme also works once larger duty cycle is needed under low V_{IN} condition. The frequency decreases once the device hits its T_{OFF_MIN}, which extends the maximum duty cycle according to Equation 3. In such condition, the frequency can be as low as approximately 133 kHz. Wide range of frequency foldback allows for the LMR50410-Q1 output voltage to stay in regulation with a much lower supply voltage V_{IN}, which leads to a lower effective dropout.

With frequency foldback while maintaining a regulated output voltage, V_{IN_MAX} is raised, and V_{IN_MIN} is lowered by decreased f_{SW}.



V_{OUT} = 3.3 V f_{SW} = 2.1 MHz

図 8-4. Frequency Foldback at T_{ON_MIN}



V_{OUT} = 5 V f_{SW} = 2.1 MHz

図 8-5. Frequency Foldback at T_{OFF_MIN}

8.3.5 Bootstrap Voltage

The LMR50410-Q1 provides an integrated bootstrap voltage converter. A small capacitor between the CB and SW pins provides the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch is on. The recommended value of the bootstrap capacitor is 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or higher is recommended for stable performance over temperature and voltage.

8.3.6 Overcurrent and Short Circuit Protection

The LMR50410-Q1 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits.

High-side MOSFET overcurrent protection is implemented by the nature of the Peak Current Mode control. The high-side switch current is sensed when the high-side is turned on after a set blanking time. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. See *セクション 8.2* for more details. The peak current of high-side switch is limited by a clamped maximum peak current threshold I_{sc} (see *セクション 7.5*), which is constant.

The current going through low-side MOSFET is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down. The low-side switch is not turned OFF at the end of a switching cycle if its current is above the low-side current limit I_{LS_LIMIT} (see *セクション 7.5*). The low-side switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the I_{LS_LIMIT}. Then the low-side switch is turned OFF and the high-side switch is turned on after a dead time. After I_{LS_LIMIT} is achieved, peak and valley current limit controls the max current deliver and it can be calculated using Equation 6.

$$I_{OUT}\big|_{max} = \frac{I_{LS\_LIMIT} + I_{SC}}{2} \tag{6}$$

If the feedback voltage is lower than 40% of the V_{REF}, the current of the low-side switch triggers I_{LS_LIMIT} for 256 consecutive cycles and hiccup current protection mode is activated. In hiccup mode, the converter shuts down and keeps off for a period of hiccup, T_{HICCUP} (135 ms typical) before the LMR50410-Q1 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, prevents over-heating and potential damage to the device.

For FPWM version, the inductor current is allowed to go negative. When this current exceed the low-side negative current limit I_{LS_NEG}, the low-side switch is turned off and high-side switch is turned on immediately. This is used to protect the low-side switch from excessive negative current.

8.3.7 Soft Start

The integrated soft-start circuit prevents input inrush current impacting the LMR50410-Q1 and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. The typical soft-start time is 1.8 ms.

The LMR50410-Q1 also employs overcurrent protection blanking time, T_{OCP_BLK} (33 ms typical), at the beginning of power up. Without this feature, in applications with a large amount of output capacitors and high V_{OUT}, the inrush current is large enough to trigger the current-limit protection, which can cause a false start as the device entering into hiccup mode. This results in a continuous recycling of soft start without raising up to the programmed output voltage. The LMR50410 is able to charge the output capacitor to the programmed V_{OUT} by controlling the average inductor current during the start-up sequence in the blanking time T_{OCP_BLK}.

8.3.8 Thermal Shutdown

The LMR50410-Q1 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170°C. Both high-side and low-side FETs stop switching in thermal shutdown. Once the die temperature falls below 158°C, the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON/OFF control for the LMR50410-Q1. When V_{EN} is below 0.95 V, the device is in shutdown mode. The LMR50410-Q1 also employs V_{IN} undervoltage lock out protection (UVLO). If V_{IN} voltage is below its UVLO threshold 3.25 V, the converter is turned off.

8.4.2 Active Mode

The LMR50410-Q1 is in Active Mode when both V_{EN} and V_{IN} are above their respective operating threshold. The simplest way to enable the LMR50410-Q1 is to connect the EN pin to VIN pin. This allows self-start-up when the input voltage is in the operating range of 4.0 V to 36 V. See *セクション 8.3.3* for details on setting these operating levels.

In Active Mode, depending on the load current, the LMR50410-Q1 is in one of four modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is greater than half of the peak-to-peak inductor current ripple (for both PFM and FPWM versions)
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is less than half of the peak-to-peak inductor current ripple(only for PFM version)
3. Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM version)
4. Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM version).

8.4.3 CCM Mode

Continuous Conduction Mode (CCM) operation is employed in the LMR50410-Q1 when the load current is greater than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current of 1 A can be supplied by the LMR50410-Q1.

8.4.4 Light-Load Operation (PFM Version)

For PFM version, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR50410-Q1 operates in Discontinuous Conduction Mode (DCM), also known as Diode Emulation Mode (DEM). In DCM operation, the low-side switch is turned off when the inductor current drops to I_{LS_ZC} (20 mA typical) to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

During light load operation, Pulse Frequency Modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum high-side switch ON time t_{ON_MIN} or the minimum peak inductor current I_{PEAK_MIN} (300 mA typical) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to a significant drop in effective switching frequency.

8.4.5 Light-Load Operation (FPWM Version)

For FPWM version, LMR50410-Q1 is locked in PWM mode at full load range. This operation is maintained, even in no-load condition, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The LMR50410-Q1 is a step-down DC-to-DC converter. It is typically used to convert a higher input voltage to a lower output DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LMR50410-Q1. Alternately, the WEBENCH® software can be used to generate complete designs. When generating a design, the WEBENCH® software utilizes iterative design procedure and accesses comprehensive databases of components. Go to ti.com for more details.

9.2 Typical Application

The LMR50410-Q1 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. 図 9-1 shows a basic schematic.

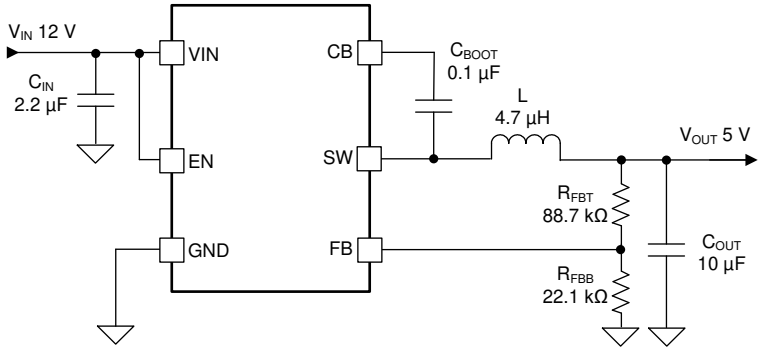


図 9-1. Application Circuit

The external components have to fulfill the needs of the application and the stability criteria of the control loop of the device. 表 9-1 can be used to simplify the output filter component selection.

表 9-1. L and C_{OUT} Typical Values

f_{SW} (MHz)	V_{OUT} (V)	L (µH)	C_{OUT} (µF) (1)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
2.1	3.3	3.3	10 µF / 10 V	51	22.1
	5	4.7	10 µF / 10 V	88.7	22.1
	12	10	22 µF / 25 V	243	22.1

(1) Ceramic capacitor is used in this table.

9.2.1 Design Requirements

The detailed design procedure is described based on a design example. For this design example, use the parameters listed in the following table as the input parameters.

表 9-2. Design Example Parameters

PARAMETER	VALUE
Input voltage, V_{IN}	12 V typical, range from 6 V to 36 V
Output voltage, V_{OUT}	5 V ±3%
Maximum output current, I_{OUT_MAX}	1 A
Output overshoot/undershoot (0 A to 1 A)	5%
Output voltage ripple	0.5%
Operating frequency	2.1 MHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR50410-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Output Voltage Set-Point

The output voltage of the LMR50410-Q1 device is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 7 is used to determine the output voltage of the converter:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \tag{7}$$

Choose the value of R_{FBB} to be 22.1 kΩ. With the desired output voltage set to 5 V and the V_{REF} = 1.0 V, the R_{FBT} value can then be calculated using Equation 7. The formula yields to a value 88.4 kΩ, a standard value of 88.7 kΩ is selected.

9.2.2.3 Switching Frequency

The higher switching frequency allows for lower value inductors and smaller output capacitors, which results in smaller solution size and lower component cost. However, higher switching frequency brings more switching loss, making the solution less efficient and produce more heat. The switching frequency is also limited by the minimum on-time of the integrated power switch, the input voltage, the output voltage, and the frequency shift limitation as mentioned in *セクション 8.3.4*. For this example, a switching frequency of 2.1 MHz is selected.

9.2.2.4 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 9 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} must be 20% to 60% of maximum I_{OUT} supported by converter. During an instantaneous overcurrent operation event, the RMS and peak inductor current can be high. The inductor saturation current must be higher than peak current limit level.

$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT} \right)}{V_{IN\_MAX} \times L \times f_{SW}} \tag{8}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{9}$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. It also generates more inductor core loss since the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, it is recommended to have adequate amount of inductor ripple current. A larger inductor ripple current improves the comparator signal-to-noise ratio.

For this design example, choose K_{IND} = 0.4. The minimum inductor value is calculated to be 5.16 µH. Choose the nearest standard 4.7-µH ferrite inductor with a capability of 1.5-A RMS current and 2.5-A saturation current.

9.2.2.5 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. It is generally desired to minimize the output capacitance to keep cost and size down. The output capacitor or capacitors, C_{OUT}, must be chosen with care since it directly affects the steady state output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient. The output voltage ripple is essentially composed of two parts. One part is caused by the inductor ripple current flowing through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \tag{10}$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{11}$$

The two components of the voltage ripple are not in-phase, therefore, the actual peak-to-peak ripple is less than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rates. When a large load step occurs, output capacitors provide the required charge before the inductor current can slew to an appropriate level. The control loop of the converter usually requires eight or more clock cycles to regulate the inductor current equal to the new load level during this time. The output capacitance must be large enough to supply the current difference for 8 clock cycles to maintain the output voltage within the specified range. Equation 12 shows the minimum output capacitance needed for a specified V_{OUT} overshoot and undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times \left(I_{OH} - I_{OL}\right)}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \tag{12}$$

where

- K_{IND} = Ripple ratio of the inductor current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{OUT_SHOOT} = Target output voltage overshoot or undershoot

For this design example, the target output ripple is 30 mV. Assuming ΔV_{OUT_ESR} = ΔV_{OUT_C} = 30 mV, choose K_{IND} = 0.4. Equation 10 yields ESR no larger than 75 mΩ and Equation 11 yields C_{OUT} no smaller than 0.79 µF. For the target overshoot and undershoot limitation of this design, ΔV_{OUT_SHOOT} = 8% × V_{OUT} = 400 mV. The C_{OUT} can be calculated to be no less than 4.76 µF by Equation 12. In summary, the most stringent criteria for the output capacitor is 4.76 µF. Considering derating, one 10-µF, 10-V, X7R ceramic capacitor with 10-mΩ ESR is used.

9.2.2.6 Input Capacitor Selection

The LMR50410-Q1 device requires a high frequency input decoupling capacitor or capacitor. The typical recommended value for the high frequency decoupling capacitor is 2.2 µF or higher. A high-quality ceramic type X5R or X7R with sufficiency voltage rating is recommended. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. For this design, one 2.2-µF, X7R dielectric capacitor rated for 50 V is used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 10 mΩ, and the current rating is 1 A. Include a capacitor with a value of 0.1 µF for high-frequency filtering and place it as close as possible to the device pins.

9.2.2.7 Bootstrap Capacitor

Every LMR50410-Q1 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.1 µF and rated at 16 V or higher. The bootstrap capacitor is located between the SW pin and the CB pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

9.2.2.8 Undervoltage Lockout Set-Point

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. Equation 13 can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{13}$$

The EN rising threshold (V_{ENH}) for LMR50410-Q1 is set to be 1.23 V (typical). Choose a value of 200 kΩ for R_{ENB} to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6.0 V, then the value of R_{ENT} can be calculated using Equation 14:

$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1 \right) \times R_{ENB} \tag{14}$$

The above equation yields a value of 775.6 kΩ, a standard value of 768 kΩ is selected. The resulting falling UVLO threshold, equals 5.3 V, can be calculated by Equation 15 where EN hysteresis voltage, V_{EN_HYS}, is 0.13 V (typical).

$$V_{IN\_FALLING} = \left(V_{ENH} - V_{EN\_HYS} \right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{15}$$

9.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the LMR50410-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum internal die temperature for the LMR50410-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 16 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in セクション 7.4 is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (16)$$

where

- η = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Number of thermal vias under the package
- Adjacent component placement

図 9-2 shows the typical curves of maximum output current versus ambient temperature. This data was taken with a device and PCB combination, giving an $R_{\theta JA}$ which is 80°C/W. It must be remembered that the data given in these graphs are for illustration purposes only and the actual performance in any given application depends on all of the previously mentioned factors.

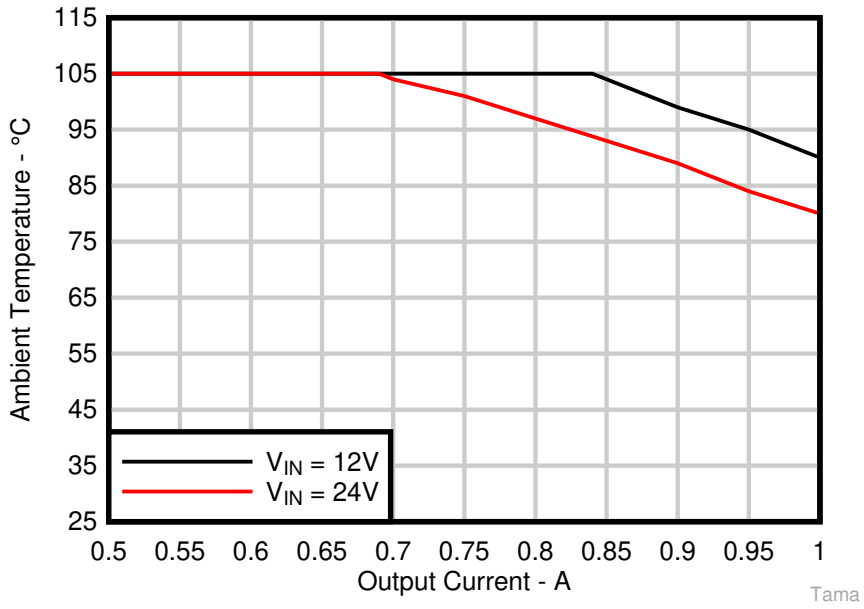


図 9-2. Maximum Output Current versus Ambient Temperature

Use the following resources as a guide to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight Application Report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *PowerPAD™ Thermally Enhanced Package Application Report*
- *PowerPAD™ Made Easy Application Report*
- *Using New Thermal Metrics Application Report*

9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} =2.1 MHz, L = 4.7 µH, C_{OUT} = 10 µF, T_A = 25°C.

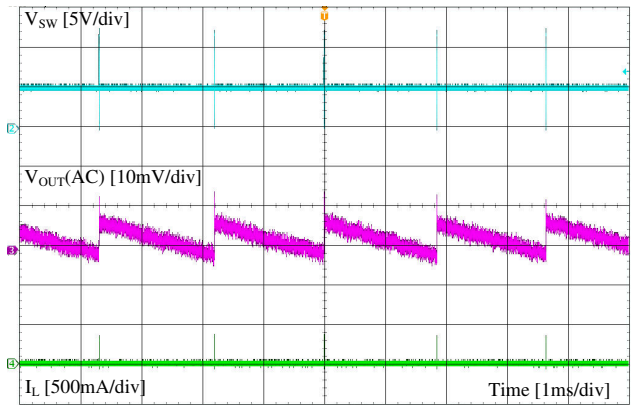


図 9-3. Ripple at No Load

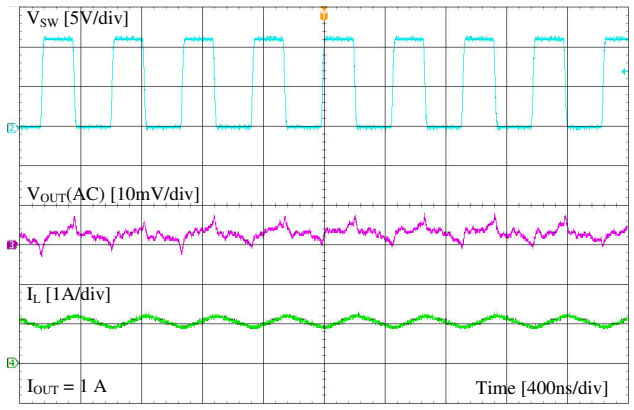


図 9-4. Ripple at Full Load

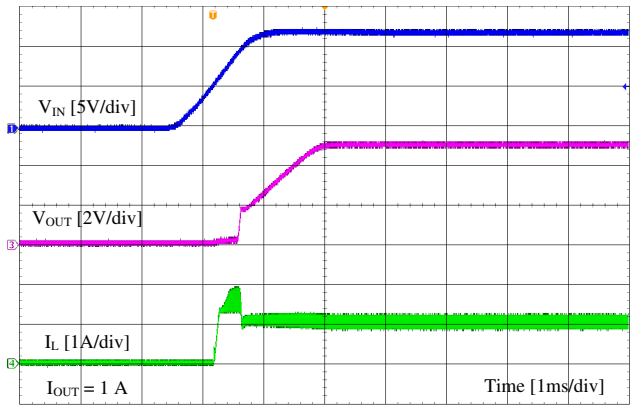


図 9-5. Start Up by V_{IN}

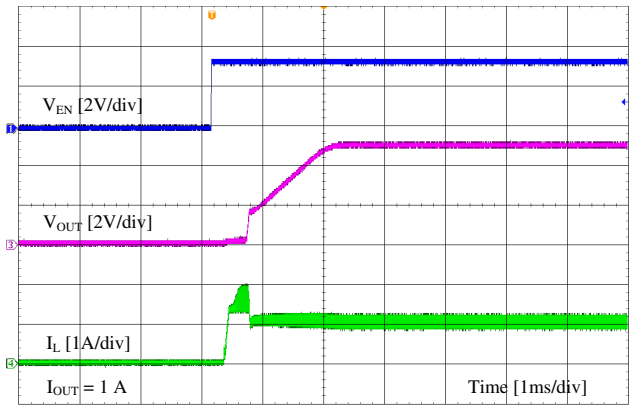


図 9-6. Start-Up by EN

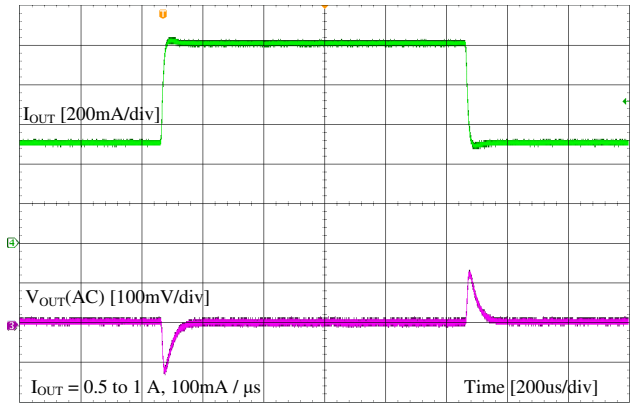


図 9-7. Load Transient

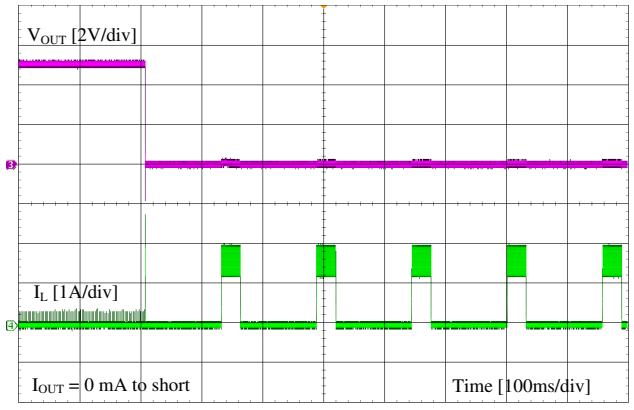


図 9-8. Short Protection

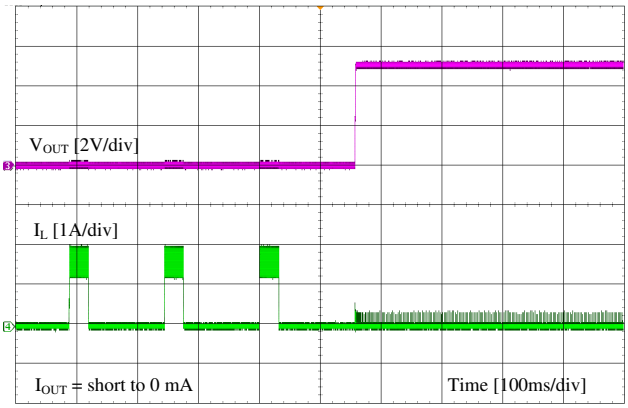


図 9-9. Short Recovery

10 Power Supply Recommendations

The LMR50410-Q1 is designed to operate from an input voltage supply range between 4.0 V and 36 V. This input supply must be well-regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR50410-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR50410-Q1 additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 10-µF or 22-µF electrolytic capacitor is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN and GND pins. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin.
2. Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB}, must be located close to the FB pin. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
3. Use ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
4. Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
5. Provide adequate device heat-sinking. GND, VIN, and SW pins provide the main heat dissipation path, make the GND, VIN, and SW plane area as large as possible. Use an array of heat-sinking vias to connect the top side ground plane to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

11.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing a ceramic bypass capacitor or capacitors as close as possible to the VIN and GND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{OUT} end of the inductor and closely grounded to GND pin.

11.1.2 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, it is important to place the resistor divider close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so it is a high impedance node and very sensitive to noise. Placing the resistor divider closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provides the best output accuracy. The voltage sense trace from the load to the feedback resistor divider must be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high value resistors are used to set the output voltage. It is recommended to route the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This provides further shielding for the voltage feedback path from EMI noises.

11.2 Layout Example

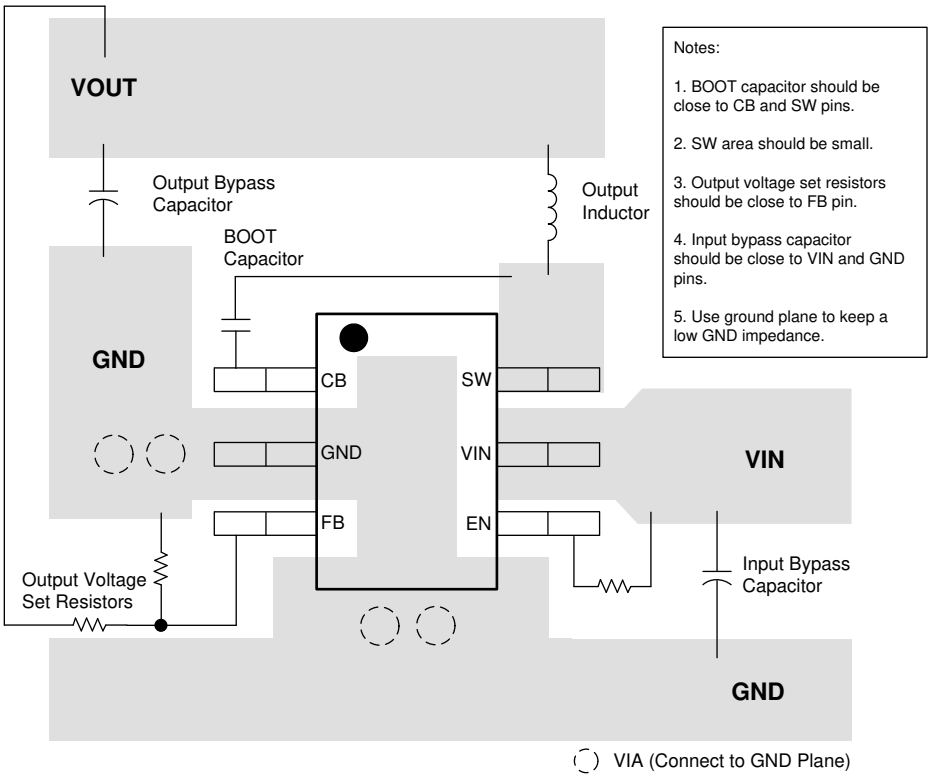


図 11-1. Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR50410-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*

12.3 ドキュメントの更新通知を受け取る方法

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12.7 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR50410Y3FQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	4AY3	Samples
LMR50410Y5FQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 150	4AY5	Samples
LMR50410YFQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	4AYF	Samples
LMR50410YQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	4AYA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMR50410-Q1 :

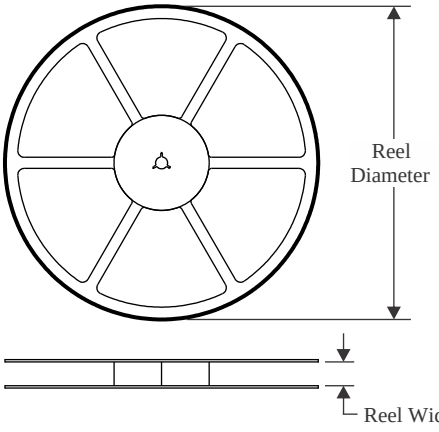
- Catalog : LMR50410

NOTE: Qualified Version Definitions:

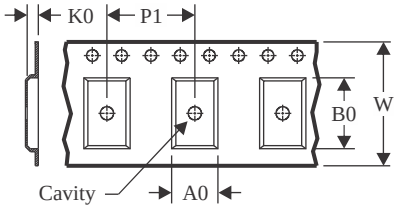
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

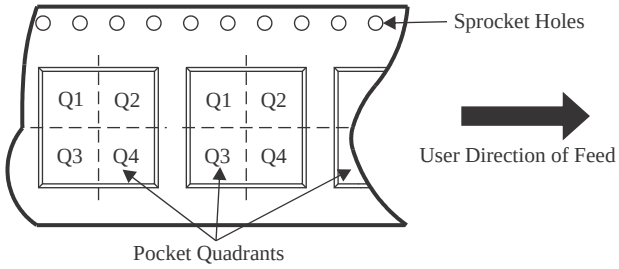


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

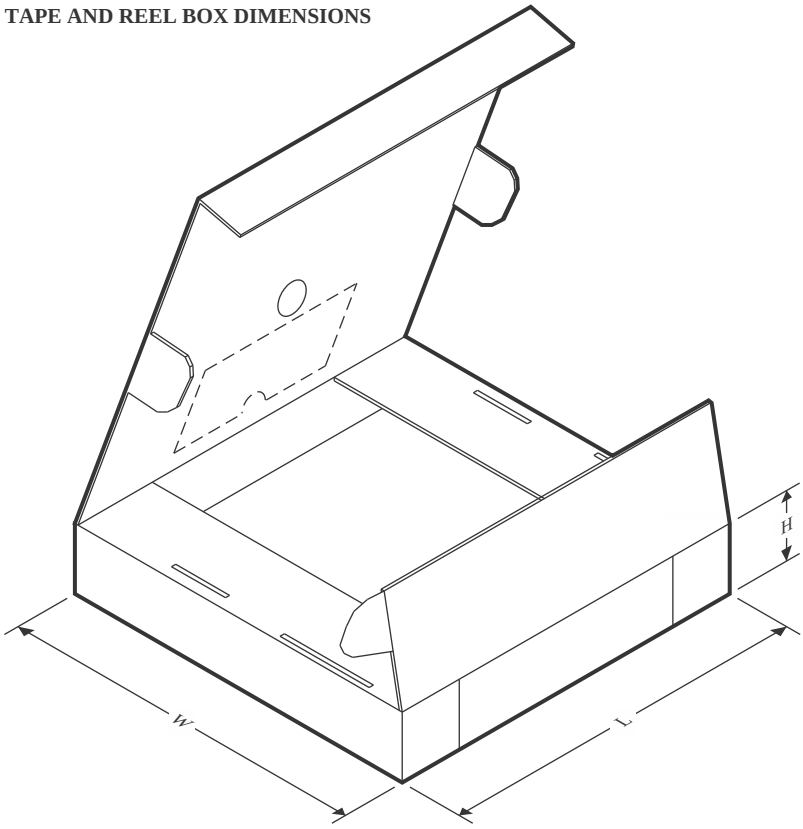
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR50410Y3FQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR50410Y5FQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR50410YFQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR50410YQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

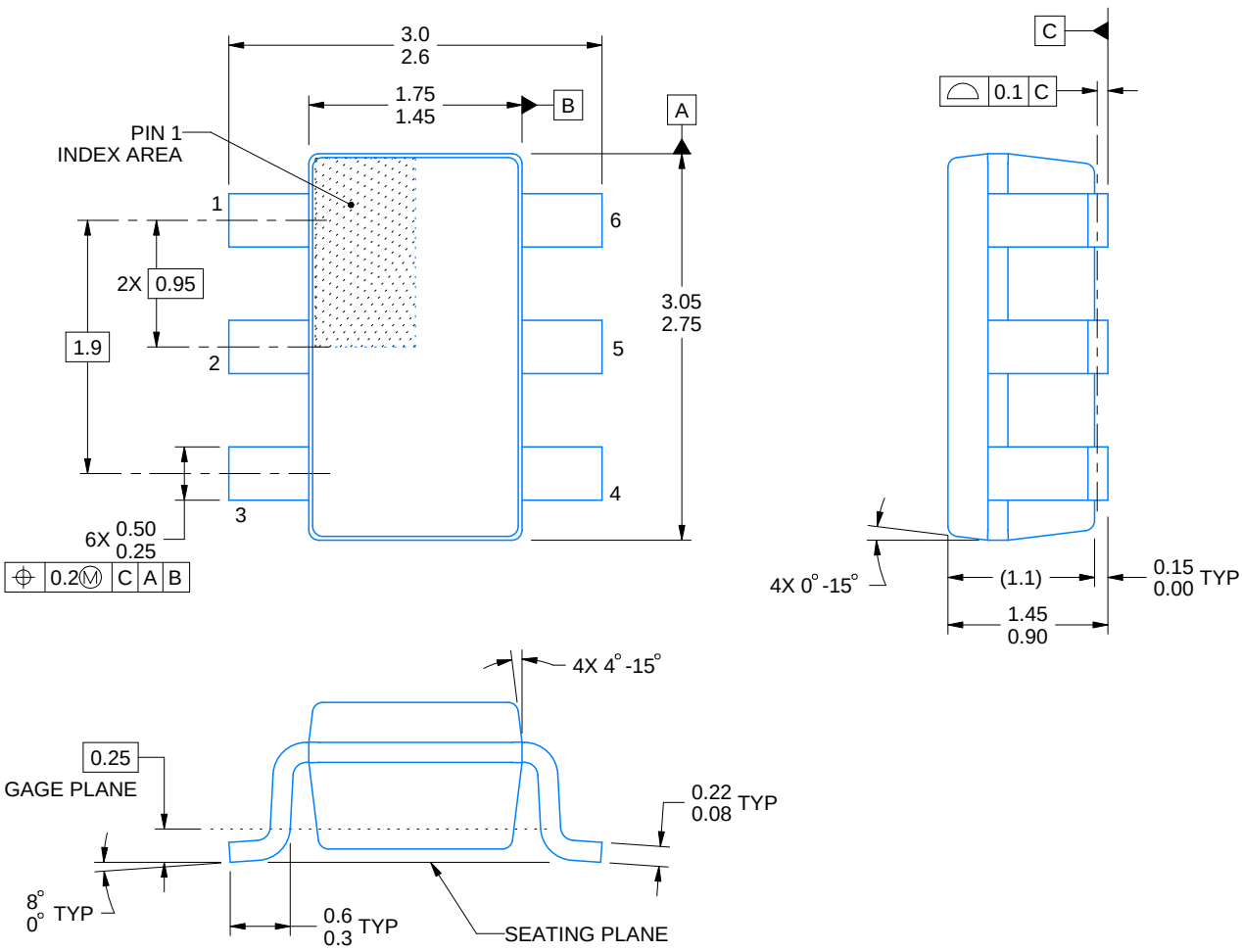
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR50410Y3FQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
LMR50410Y5FQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
LMR50410YFQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
LMR50410YQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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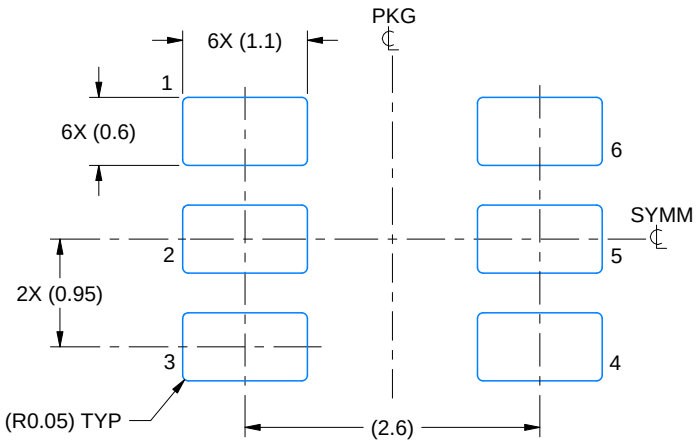
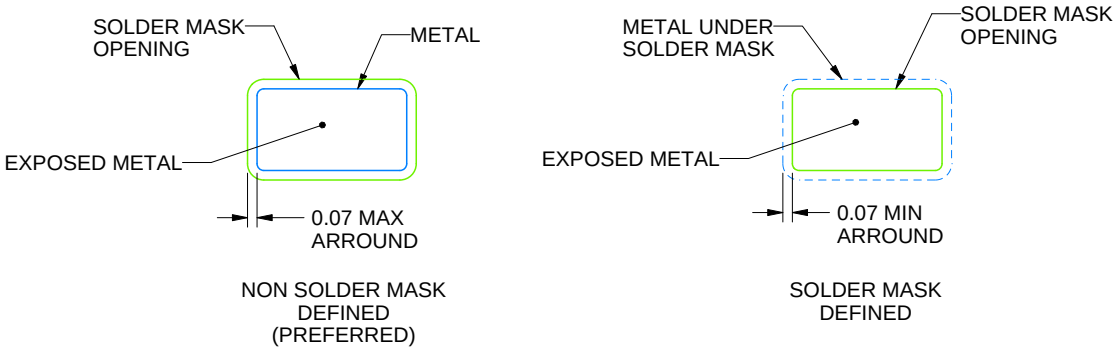
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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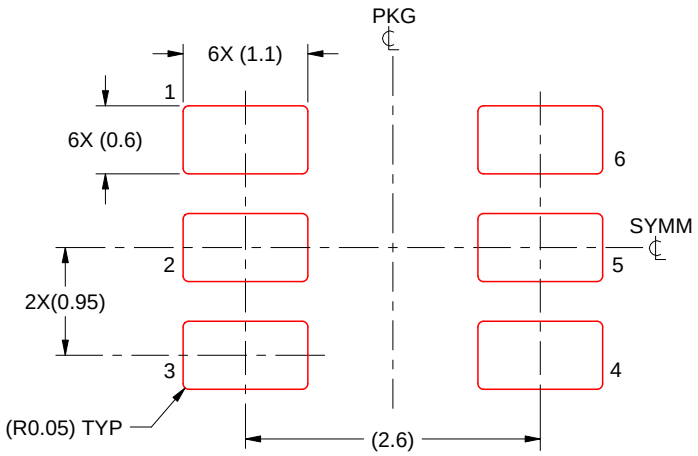
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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