

# LMP91002 Sensor AFE System: Configurable AFE Potentiostat for Low-Power Chemical Sensing Applications

## 1 Features

- Typical Values,  $T_A = 25^\circ\text{C}$
- Supply Voltage 2.7 V to 3.6 V
- Supply Current (Average Over Time)  $< 10\ \mu\text{A}$
- Cell Conditioning Current Up to 10 mA
- Reference Electrode Bias Current (85°C) 900-pA (Maximum)
- Output Drive Current 750  $\mu\text{A}$
- Complete Potentiostat Circuit to Interface to Most Not Biased Gas Sensors
- Low Bias Voltage Drift
- Programmable TIA Gain 2.75 k $\Omega$  to 350 k $\Omega$
- I<sup>2</sup>C-Compatible Digital Interface
- Ambient Operating Temperature  $-40^\circ\text{C}$  to  $85^\circ\text{C}$
- Package 14-pin WSON
- Supported by Webench Sensor AFE Designer

## 2 Applications

- Gas Detectors
- Amperometric Applications
- Electrochemical Blood Glucose Meters

## 3 Description

The LMP91002 device is a programmable Analog Front End (AFE) for use in micro-power electrochemical-sensing applications. It provides a complete signal path solution between a not biased gas sensor and a microcontroller generating an output voltage proportional to the cell current.

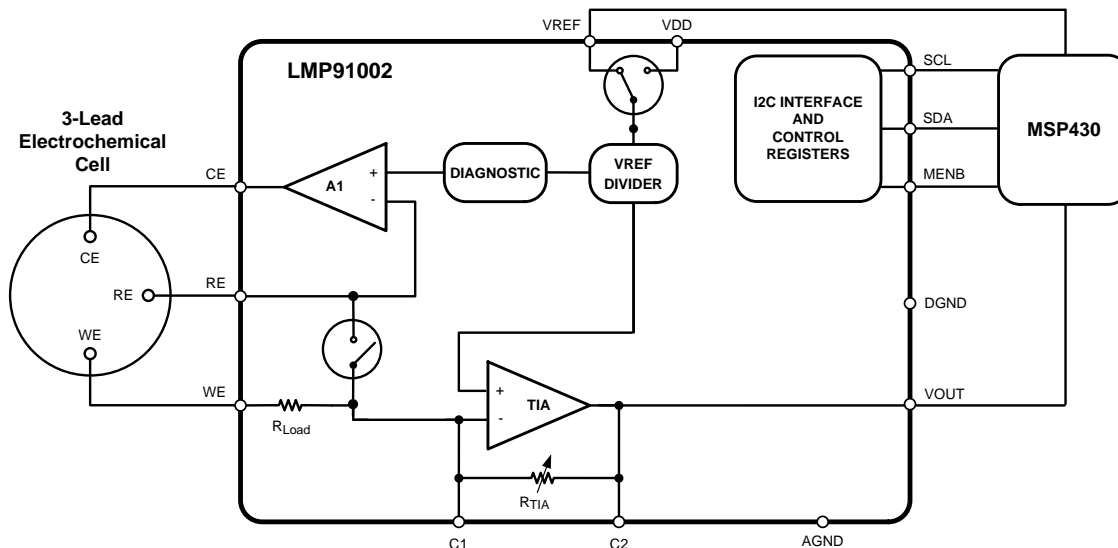
The LMP91002's programmability enables it support not biased electro-chemical gas sensor with a single design. The LMP91002 supports gas sensitivities over a range of 0.5 nA/ppm to 9500 nA/ppm. It also allows for an easy conversion of current ranges from 5  $\mu\text{A}$  to 750  $\mu\text{A}$  full scale. The LMP91002's transimpedance amplifier (TIA) gain is programmable through the I<sup>2</sup>C interface. The I<sup>2</sup>C interface can also be used for sensor diagnostics. The LMP91002 is optimized for micro-power applications and operates over a voltage range of 2.7 V to 3.6 V. The total current consumption can be less than 10  $\mu\text{A}$ . Further power savings are possible by switching off the TIA amplifier and shorting the reference electrode to the working electrode with an internal switch.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP91002	WSON (14)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Application



## Table of Contents

<b>1</b>	<b>Features</b> .....	<b>1</b>	7.4	Device Functional Modes .....	<b>12</b>
<b>2</b>	<b>Applications</b> .....	<b>1</b>	7.5	Programming .....	<b>12</b>
<b>3</b>	<b>Description</b> .....	<b>1</b>	7.6	Register Maps .....	<b>14</b>
<b>4</b>	<b>Revision History</b> .....	<b>2</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>17</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	8.1	Application Information .....	<b>17</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	8.2	Typical Application .....	<b>19</b>
6.1	Absolute Maximum Ratings .....	<b>4</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>22</b>
6.2	ESD Ratings .....	<b>4</b>	9.1	Power Consumption .....	<b>22</b>
6.3	Recommended Operating Conditions .....	<b>4</b>	<b>10</b>	<b>Layout</b> .....	<b>22</b>
6.4	Thermal Information .....	<b>4</b>	10.1	Layout Guidelines .....	<b>22</b>
6.5	Electrical Characteristics .....	<b>5</b>	10.2	Layout Example .....	<b>23</b>
6.6	I <sup>2</sup> C Interface .....	<b>6</b>	<b>11</b>	<b>Device and Documentation Support</b> .....	<b>25</b>
6.7	Timing Characteristics .....	<b>7</b>	11.1	Community Resources .....	<b>25</b>
6.8	Typical Characteristics .....	<b>8</b>	11.2	Trademarks .....	<b>25</b>
<b>7</b>	<b>Detailed Description</b> .....	<b>10</b>	11.3	Electrostatic Discharge Caution .....	<b>25</b>
7.1	Overview .....	<b>10</b>	11.4	Glossary .....	<b>25</b>
7.2	Functional Block Diagram .....	<b>10</b>	<b>12</b>	<b>Mechanical, Packaging, and Orderable Information</b> .....	<b>25</b>
7.3	Feature Description .....	<b>10</b>			

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision A (March 2013) to Revision B

Page

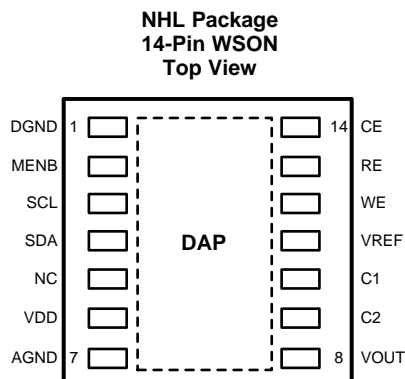
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**

### Changes from Original (March 2013) to Revision A

Page

- Changed layout of National Data Sheet to TI format ..... **18**

## 5 Pin Configuration and Functions



**Pin Functions<sup>(1)</sup>**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DGND	G	Connect to ground
2	MENB	D	Module Enable. Active Low
3	SCL	D	I <sup>2</sup> C Clock
4	SDA	D	I <sup>2</sup> C Data
5	NC	—	Do not connect. Not internally connected
6	VDD	P	Voltage supply
7	AGND	GND	Analog GND
8	VOUT	A	Analog voltage representing sensor output
9	C2	A	Optional External component node 2 for TIA (filter capacitor or gain resistor)
10	C1	A	Optional External component node 1 for TIA (filter capacitor or gain resistor)
11	VREF	A	External Reference voltage input
12	WE	A	Working Electrode of the sensor.
13	RE	A	Reference Electrode of the sensor.
14	CE	A	Counter Electrode of the sensor.
—	DAP	GND	Die attached pad. Connect to GND.

(1) A = analog, D = digital, P = power, G = GND

## 6 Specifications

### 6.1 Absolute Maximum Ratings

See <sup>(1)(2)(3)</sup>

	MIN	MAX	UNIT
Voltage between any two pins		6	V
Current through VDD or VSS		50	mA
Current sunk and sourced by CE pin		10	mA
Current out of other pins <sup>(4)</sup>		5	mA
Junction temperature <sup>(5)</sup>		150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) For soldering specifications, see [SNOA549](#).
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) All non-power pins of this device are protected against ESD by snapback devices. Voltage at such pins will rise beyond absmax if current is forced into pin.
- (5) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>DMAX</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PCB.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)(2)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>	±1000
		Machine Model (MM)	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field- Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage V <sub>S</sub> = (VDD - AGND)	2.7	3.6	V
Temperature <sup>(1)</sup>	-40	85	°C

- (1) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>DMAX</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PCB.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMP91002	UNIT
		NHL (WSON)	
		14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	44	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>DMAX</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PCB.

## 6.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_{DD} - \text{AGND})$ ,  $V_S = 3.3\text{ V}$  and  $\text{AGND} = \text{DGND} = 0\text{ V}$ ,  $V_{\text{REF}} = 2.5\text{ V}$ , Internal Zero = 20%  $V_{\text{REF}}$ .<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
<b>POWER SUPPLY SPECIFICATION</b>						
$I_S$	Supply current	3-lead amperometric cell mode MODECN = 0x03	$T_A = 25^\circ\text{C}$	10	13.5	$\mu\text{A}$
			At the temperature extremes		15	
		Standby mode MODECN = 0x02	$T_A = 25^\circ\text{C}$	6.5	8	
			At the temperature extremes		10	
Deep sleep mode MODECN = 0x00	$T_A = 25^\circ\text{C}$	0.6	0.85			
	At the temperature extremes		1			
<b>POTENTIOSTAT</b>						
$I_{\text{RE}}$	Input bias current at RE pin	VDD = 2.7 V; Internal zero 50% VDD	$T_A = 25^\circ\text{C}$	-90	90	$\mu\text{A}$
			At the temperature extremes	-800	800	
		VDD = 3.6 V; Internal zero 50% VDD	$T_A = 25^\circ\text{C}$	-90	90	
			At the temperature extremes	-900	900	
$I_{\text{CE}}$	Minimum operating current capability	Sink		750	$\mu\text{A}$	
		Source		750		
	Minimum charging capability <sup>(4)</sup>	Sink		10	mA	
		Source		10		
AOL_A1	Open-loop voltage gain of control loop operational amplifier (A1)	$300\text{ mV} \leq V_{\text{CE}} \leq V_S - 300\text{ mV}$ , $-750\text{ }\mu\text{A} \leq I_{\text{CE}} \leq 750\text{ }\mu\text{A}$	$T_A = 25^\circ\text{C}$	120		dB
		At the temperature extremes	104			
en_RW	Low frequency integrated noise between RE pin and WE pin	0.1 Hz to 10 Hz <sup>(5)</sup>		3.4		$\mu\text{Vpp}$
$V_{\text{OS\_RW}}$	WE voltage offset referred to RE	0% VREF, internal zero = 20% VREF, at the temperature extremes		-550	550	$\mu\text{V}$
		0% VREF, internal zero = 50% VREF, at the temperature extremes		-550	550	
		0% VREF, internal zero = 67% VREF, at the temperature extremes		-550	550	
$TcV_{\text{OS\_RW}}$	WE voltage offset drift referred to RE from $-40^\circ\text{C}$ to $85^\circ\text{C}$ <sup>(6)</sup>	0% VREF, internal zero = 20% VREF		-4	4	$\mu\text{V}/^\circ\text{C}$
		0% VREF, internal zero = 50% VREF		-4	4	
		0% VREF, internal zero = 67% VREF		-4	4	

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (4) At such currents no accuracy of the output voltage can be expected.
- (5) This parameter includes both A1 and TIA's noise contribution.
- (6) Offset voltage temperature drift is determined by dividing the change in VOS at the temperature extremes by the total temperature change. Starting from the measured voltage offset at temperature T1 ( $V_{\text{OS\_RW}}(T1)$ ), the voltage offset at temperature T2 ( $V_{\text{OS\_RW}}(T2)$ ) is calculated according the following formula:  $V_{\text{OS\_RW}}(T2) = V_{\text{OS\_RW}}(T1) + \text{ABS}(T2 - T1) * TcV_{\text{OS\_RW}}$ .

## Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_{DD} - \text{AGND})$ ,  $V_S = 3.3\text{ V}$  and  $\text{AGND} = \text{DGND} = 0\text{ V}$ ,  $V_{\text{REF}} = 2.5\text{ V}$ , Internal Zero = 20%  $V_{\text{REF}}$ .<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
TIA_GAIN	Transimpedance gain accuracy			5%		
	Linearity			±0.05%		
	Programmable TIA gains	7 programmable gain resistors		2.75 3.5 7 14 35 120 350		kΩ
			Maximum external gain resistor		350	
TIA_ZV	Internal zero voltage	3 programmable percentages of VREF		20% 50% 67%		
		3 programmable percentages of VDD		20% 50% 67%		
	Internal zero voltage accuracy			±0.04%		
RL	Load resistor			10		Ω
	Load accuracy			5%		
PSRR	Power supply rejection ratio at RE pin	2.7 V ≤ VDD ≤ 5.25 V	Internal zero 20% VREF	80	110	dB
			Internal zero 50% VREF	80	110	
			Internal zero 67% VREF	80	110	
<b>EXTERNAL REFERENCE SPECIFICATION<sup>(7)</sup></b>						
VREF	External voltage reference range		1.5		VDD	V
	Input impedance			10		MΩ

(7) In case of external reference connected, the noise of the reference has to be added.

## 6.6 I<sup>2</sup>C Interface

Unless otherwise specified, all limits ensured for at  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_{DD} - \text{AGND})$ ,  $2.7\text{ V} < V_S < 3.6\text{ V}$  and  $\text{AGND} = \text{DGND} = 0\text{ V}$ ,  $V_{\text{REF}} = 2.5\text{ V}$ .<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
V <sub>IH</sub>	Input High Voltage	At the temperature extremes	0.7*VDD			V
V <sub>IL</sub>	Input Low Voltage	At the temperature extremes			0.3*VDD	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> = 3 mA, at the temperature extremes			0.4	V
	Hysteresis <sup>(4)</sup>	At the temperature extremes	0.1*VDD			V
C <sub>IN</sub>	Input Capacitance on all digital pins	At the temperature extremes		0.5		pF

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (4) This parameter is specified by design or characterization.

### 6.7 Timing Characteristics

Unless otherwise specified, all limits ensured for  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_{DD} - AGND)$ ,  $V_S = 3.3\text{ V}$  and  $AGND = DGND = 0\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , Internal Zero = 20%  $V_{REF}$ . All limits apply at the temperature extremes. Refer to timing diagram in Figure 1<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SCL}$	Clock Frequency	At the temperature extremes	10		100	kHz
$t_{LOW}$	Clock Low Time	At the temperature extremes	4.7			$\mu\text{s}$
$t_{HIGH}$	Clock High Time	At the temperature extremes	4			$\mu\text{s}$
$t_{HD;STA}$	Data valid	After this period, the first clock pulse is generated at the temperature extremes	4			$\mu\text{s}$
$t_{SU;STA}$	Set-up time for a repeated START condition	At the temperature extremes	4.7			$\mu\text{s}$
$t_{HD;DAT}$	Data hold time <sup>(2)</sup>	At the temperature extremes	0			ns
$t_{SU;DAT}$	Data Set-up time	At the temperature extremes	250			ns
$t_f$	SDA fall time <sup>(3)</sup>	$I_L \leq 3\text{ mA}$ , $C_L \leq 400\text{ pF}$ , at the temperature extremes			250	ns
$t_{SU;STO}$	Set-up time for STOP condition	At the temperature extremes	4			$\mu\text{s}$
$t_{BUF}$	Bus free time between a STOP and START condition	At the temperature extremes	4.7			$\mu\text{s}$
$t_{VD;DAT}$	Data valid time	At the temperature extremes			3.45	$\mu\text{s}$
$t_{VD;ACK}$	Data valid acknowledge time	At the temperature extremes			3.45	$\mu\text{s}$
$t_{SP}$	Pulse width of spikes that must be suppressed by the input filter <sup>(3)</sup>	At the temperature extremes			50	ns
$t_{timeout}$	SCL and SDA Timeout	At the temperature extremes	25		100	ms
$t_{EN;START}$	I <sup>2</sup> C Interface Enabling	At the temperature extremes	600			ns
$t_{EN;STOP}$	I <sup>2</sup> C Interface Disabling	At the temperature extremes	600			ns
$t_{EN;HIGH}$	time between consecutive I <sup>2</sup> C interface enabling and disabling	At the temperature extremes	600			ns

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) LMP91002 provides an internal 300ns minimum hold time to bridge the undefined region of the falling edge of SCL.
- (3) This parameter is specified by design or characterization.

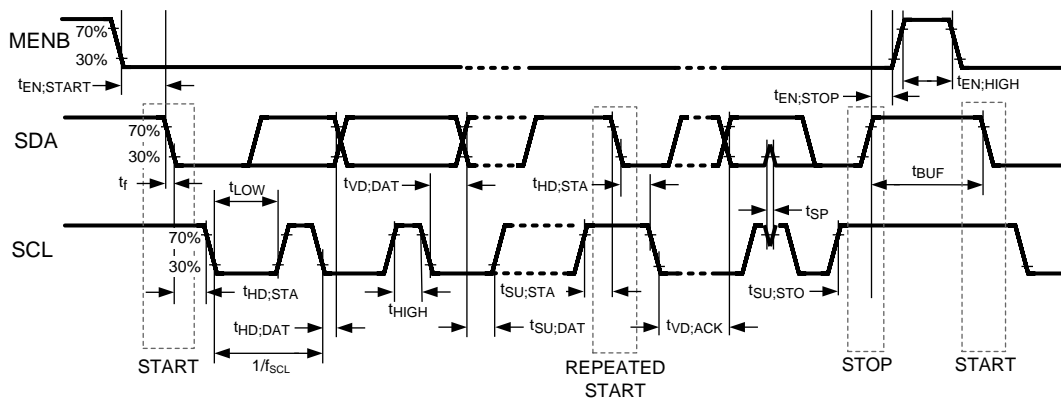


Figure 1. I<sup>2</sup>C Interface Timing Diagram

### 6.8 Typical Characteristics

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_{DD} - AGND)$ ,  $2.7\text{ V} < V_S < 3.6\text{ V}$  and  $AGND = DGND = 0\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ .

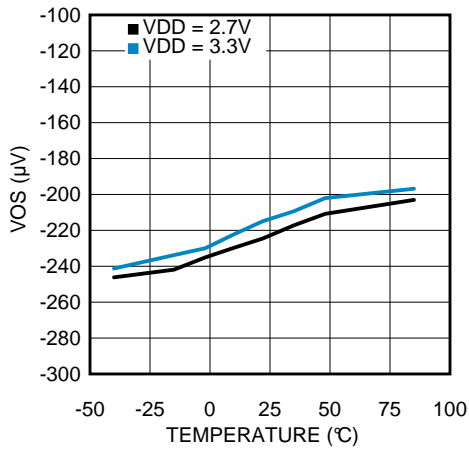


Figure 2. Input  $V_{OS\_RW}$  vs Temperature

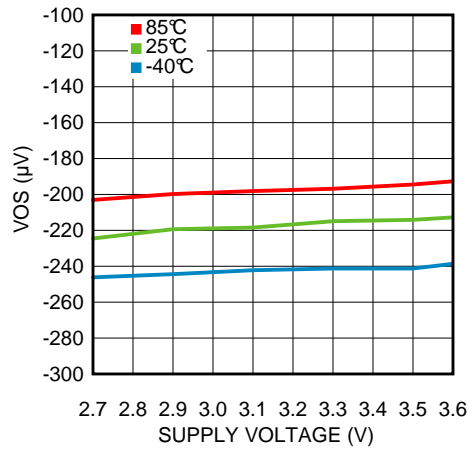


Figure 3. Input  $V_{OS\_RW}$  vs VDD

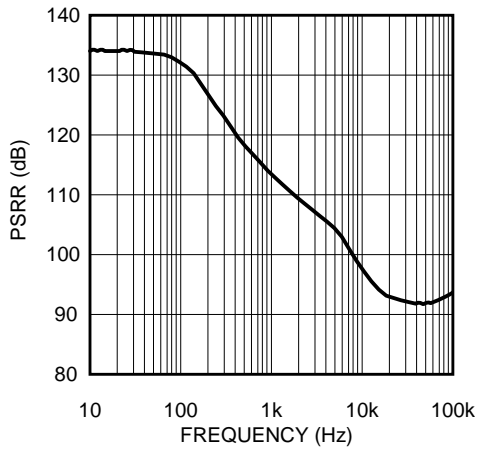


Figure 4. AC PSRR vs Frequency

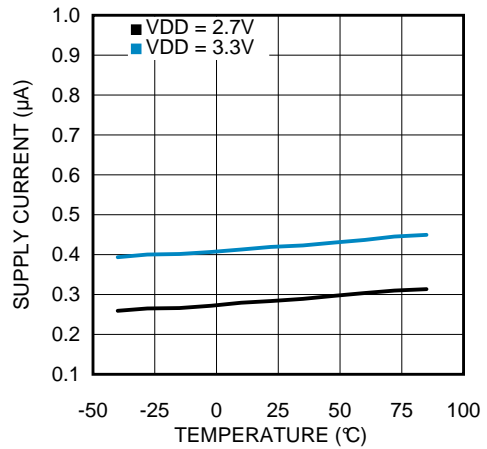


Figure 5. Supply Current vs Temperature (Deep Sleep Mode)

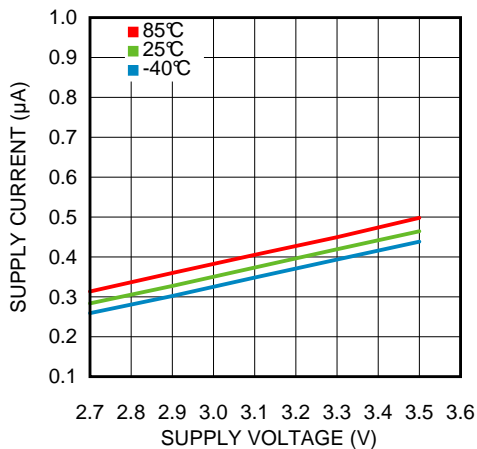


Figure 6. Supply Current vs VDD (Deep Sleep Mode)

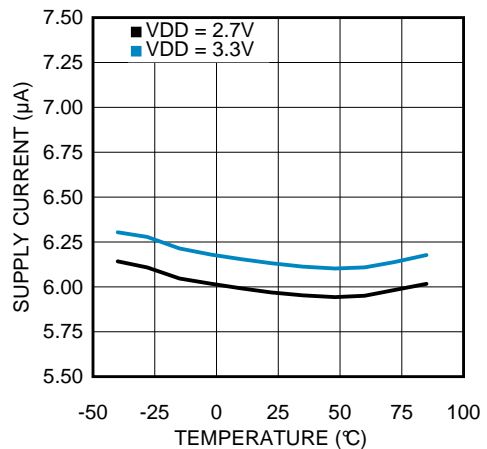


Figure 7. Supply Current vs Temperature (Standby Mode)



Typical Characteristics (continued)

Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V_S = (V_{DD} - \text{AGND})$ ,  $2.7\text{ V} < V_S < 3.6\text{ V}$  and  $\text{AGND} = \text{DGND} = 0\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ .

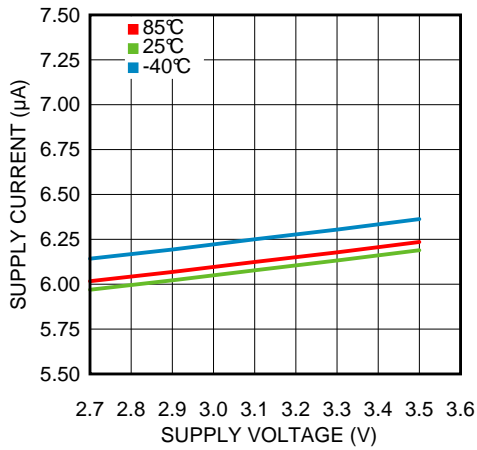


Figure 8. Supply Current vs VDD (Standby Mode)

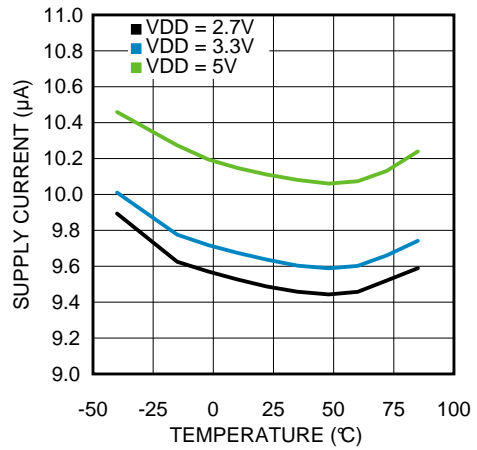


Figure 9. Supply Current vs Temperature (3-Lead Amperometric Mode)

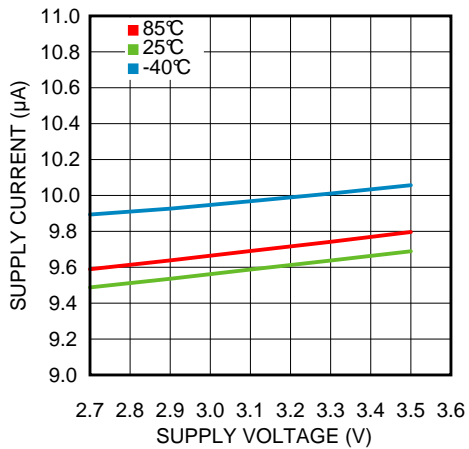


Figure 10. Supply Current vs VDD (3-Lead Amperometric Mode)

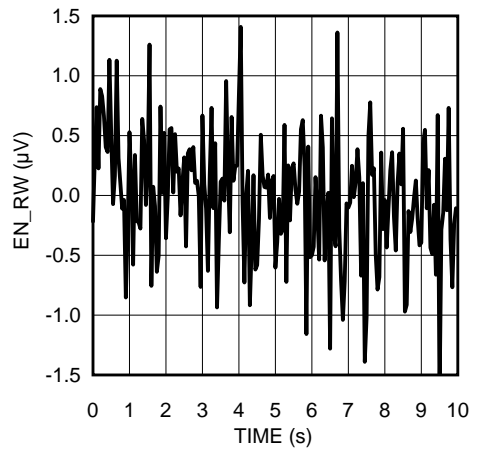


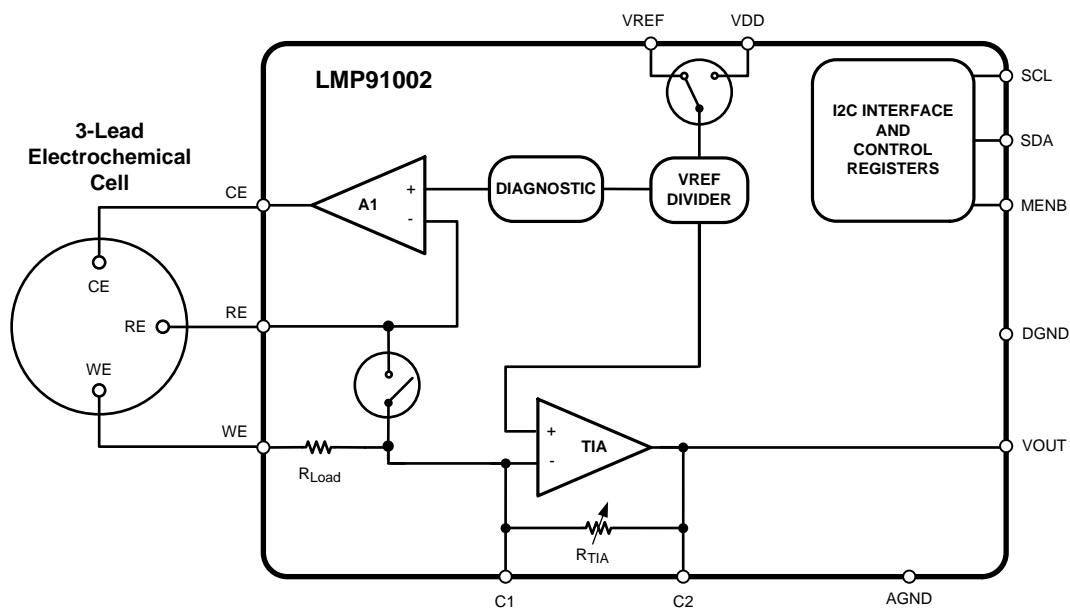
Figure 11. 0.1-Hz to 10-Hz Noise

## 7 Detailed Description

### 7.1 Overview

The LMP91002 is a programmable AFE for use in micropower chemical sensing applications. The LMP91002 is designed for 3-lead non-biased gas sensors and for 2 leads galvanic cell. This device provides all of the functionality for detecting changes in gas concentration based on a delta current at the working electrode. The LMP91002 generates an output voltage proportional to the cell current. Transimpedance gain is user programmable through an I<sup>2</sup>C compatible interface from 2.75k $\Omega$  to 350k $\Omega$  making it easy to convert current ranges from 5 $\mu$ A to 750 $\mu$ A full scale. Optimized for micro-power applications, the LMP91002 AFE works over a voltage range of 2.7V to 3.6 V. The cell voltage is user selectable using the on board programmability. In addition, it is possible to connect an external transimpedance gain resistor. Depending on the configuration, total current consumption for the device can be less than 10 $\mu$ A. For power savings, the transimpedance amplifier can be turned off and instead a load impedance equivalent to the TIA's inputs impedance is switched in.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Potentiostat Circuitry

The core of the LMP91002 is a potentiostat circuit. It consists of a differential input amplifier used to compare the potential between the working and reference electrodes to a zero bias potential. The error signal is amplified and applied to the counter electrode (through the **Control Amplifier - A1**). Any changes in the impedance between the working and reference electrodes will cause a change in the voltage applied to the counter electrode, in order to maintain the constant voltage between working and reference electrodes. A **Transimpedance Amplifier** connected to the working electrode, is used to provide an output voltage that is proportional to the cell current. The working electrode is held at virtual ground (**Internal ground**) by the transimpedance amplifier. The potentiostat will compare the reference voltage to the desired bias potential and adjust the voltage at the counter electrode to maintain the proper working-to-reference voltage.

#### 7.3.2 Transimpedance Amplifier

The transimpedance amplifier (TIA in [Functional Block Diagram](#)) has 7 programmable internal gain resistors. This accommodates the full scale ranges of most existing sensors. Moreover an external gain resistor can be connected to the LMP91002 between C1 and C2 pins. The gain is set through the I<sup>2</sup>C interface.

## Feature Description (continued)

### 7.3.3 Control Amplifier

The control amplifier (A1 op amp in *Functional Block Diagram*) provides initial charge to the sensor. A1 has the capability to drive up to 10mA into the sensor in order to provide a fast initial conditioning. A1 is able to sink and source current according to the connected gas sensor (reducing or oxidizing gas sensor). It can be powered down to reduce system power consumption. However powering down A1 is not recommended, as it may take a long time for the sensor to recover from this situation.

### 7.3.4 Internal Zero

The internal Zero is the voltage at the non-inverting pin of the TIA. The internal zero can be programmed to be either 67%, 50% or 20%, of the supply, or the external reference voltage. This provides both sufficient headroom for the counter electrode of the sensor to swing, in case of sudden changes in the gas concentration, and best use of the ADC's full scale input range.

The Internal zero is provided through an internal voltage divider (Vref divider box in *Functional Block Diagram*). The divider is programmed through the I<sup>2</sup>C interface.

### 7.3.5 2-Lead Galvanic Cell in Potentiostat Configuration

When the LMP91002 is interfaced to a galvanic cell (for instance to an Oxygen gas sensor) referred to a reference, the Counter and the Reference pin of the LMP91002 are shorted together and connected to negative electrode of the galvanic cell. The positive electrode of the galvanic cell is then connected to the Working pin of the LMP91002.

The LMP91002 is then configured in 3-lead amperometric cell mode (as for amperometric cell). In this configuration the Control Amplifier (A1) is ON and provides the internal zero voltage. The transimpedance amplifier (TIA) is also ON, it converts the current generated by the gas sensor in a voltage, according to the transimpedance gain:

$$\text{Gain} = R_{TIA}$$

If different gains are required, an external resistor can be connected between the pins C1 and C2. In this case the internal feedback resistor should be programmed to "external".

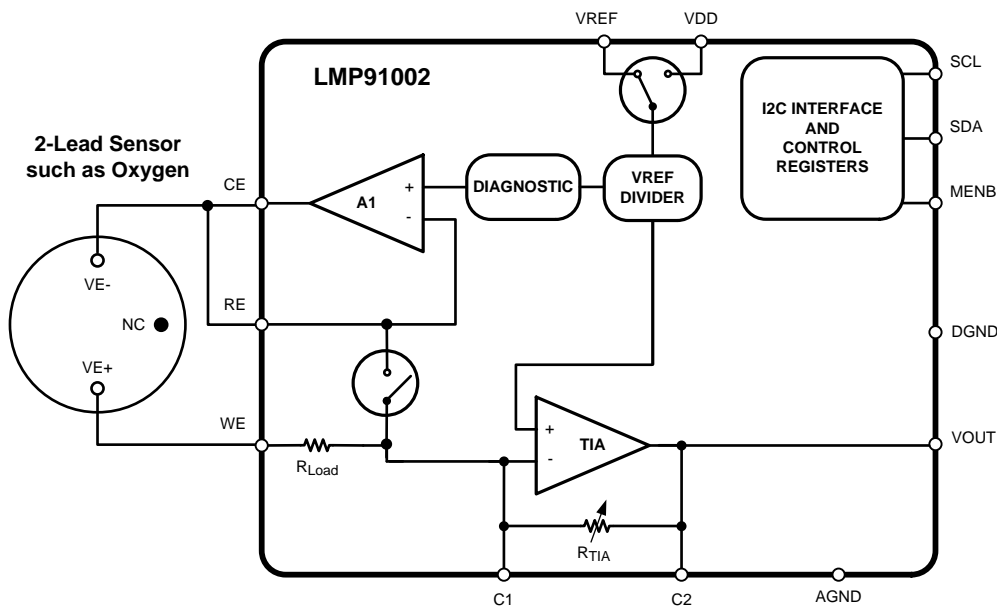


Figure 12. Two-Lead Sensor Connections

## 7.4 Device Functional Modes

### 7.4.1 Timeout Feature

The timeout is a safety feature to avoid bus lockup situation. If SCL is stuck low for a time exceeding  $t_{\text{timeout}}$ , the LMP91002 will automatically reset its I<sup>2</sup>C interface. Also, in the case the LMP91002 hangs the SDA for a time exceeding  $t_{\text{timeout}}$ , the LMP91002's I<sup>2</sup>C interface will be reset so that the SDA line will be released. Since the SDA is an open-drain with an external resistor pull-up, this also avoids high power consumption when LMP91002 is driving the bus and the SCL is stopped.

## 7.5 Programming

### 7.5.1 I<sup>2</sup>C Interface

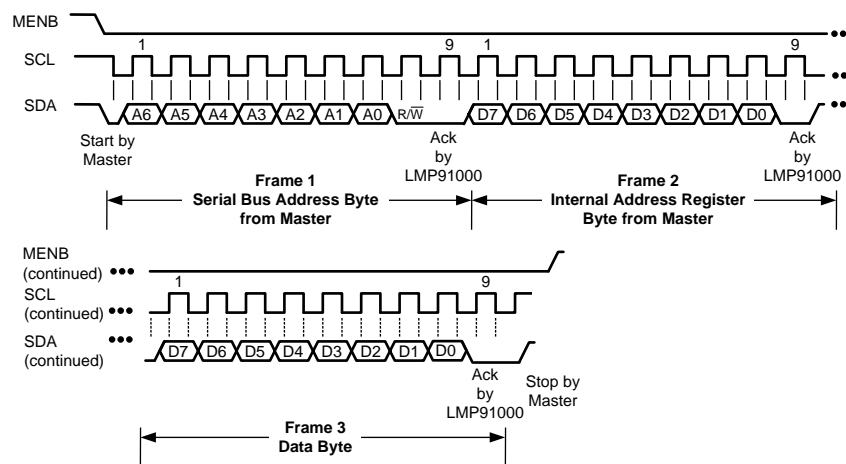
The I<sup>2</sup>C compatible interface operates in Standard mode (100kHz). Pull-up resistors or current sources are required on the SCL and SDA pins to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The LMP91002 comes with a 7 bit bus fixed address: 1001 000.

### 7.5.2 Write and Read Operation

In order to start any read or write operation with the LMP91002, MENB needs to be set low during the whole communication. Then the master generates a start condition by driving SDA from high to low while SCL is high. The start condition is always followed by a 7-bit slave address and a Read/Write bit. After these 8 bits have been transmitted by the master, SDA is released by the master and the LMP91002 either ACKs or NACKs the address. If the slave address matches, the LMP91002 ACKs the master. If the address doesn't match, the LMP91002 NACKs the master. For a write operation, the master follows the ACK by sending the 8-bit register address pointer. Then the LMP91002 ACKs the transfer by driving SDA low. Next, the master sends the 8-bit data to the LMP91002. Then the LMP91002 ACKs the transfer by driving SDA low. At this point the master should generate a stop condition and optionally set the MENB at logic high level (refer to [Figure 15](#)).

A read operation requires the LMP91002 address pointer to be set first, also in this case the master needs setting at low logic level the MENB, then the master needs to write to the device and set the address pointer before reading from the desired register. This type of read requires a start, the slave address, a write bit, the address pointer, a Repeated Start (if appropriate), the slave address, and a read bit (refer to [Figure 15](#)). Following this sequence, the LMP91002 sends out the 8-bit data of the register.

When just one LMP91002 is present on the I<sup>2</sup>C bus the MENB can be tied to ground (low logic level).



**Figure 13. (a) Register Write Transaction**

Programming (continued)

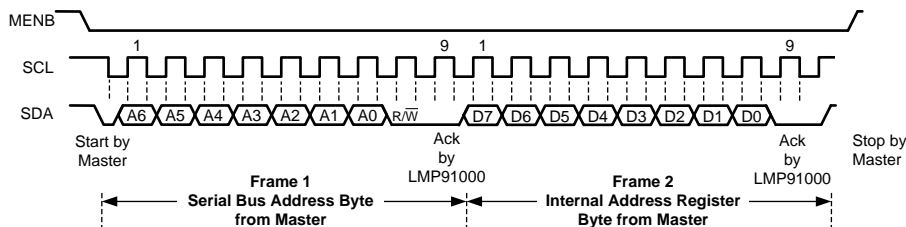
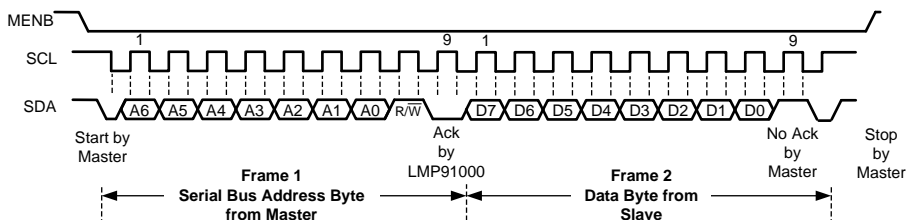


Figure 14. (b) Pointer Set Transaction



(c) Register read transaction

Figure 15. READ and WRITE Transaction

7.5.3 Connection of More Than One LMP91002 to the I<sup>2</sup>C Bus

The LMP91002 comes out with a unique and fixed I<sup>2</sup>C slave address. It is still possible to connect more than one LMP91002 to an I<sup>2</sup>C bus and select each device using the MENB pin. The MENB simply enables/disables the I<sup>2</sup>C communication of the LMP91002. When the MENB is at logic level low all the I<sup>2</sup>C communication is enabled, it is disabled when MENB is at high logic level.

In a system based on a  $\mu$ controller and more than one LMP91002 connected to the I<sup>2</sup>C bus, the I<sup>2</sup>C lines (SDA and SCL) are shared, while the MENB of each LMP91002 is connected to a dedicate GPIO port of the  $\mu$ controller.

The  $\mu$ controller starts communication asserting one out of N MENB signals where N is the total number of LMP91002s connected to the I<sup>2</sup>C bus. Only the enabled device will acknowledge the I<sup>2</sup>C commands. After finishing communicating with this particular LMP91002, the microcontroller de-asserts the corresponding MENB and repeats the procedure for other LMP91002s. Figure 16 shows the typical connection when more than one LMP91002 is connected to the I<sup>2</sup>C bus.

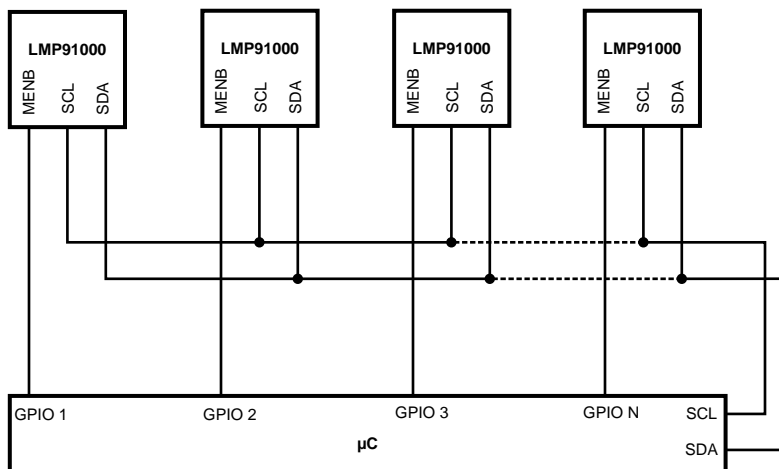


Figure 16. More than one LMP91002 on I<sup>2</sup>C bus

## 7.6 Register Maps

The registers are used to configure the LMP91002.

If writing to a reserved bit, user must write only 0. Readback value is unspecified and should be discarded.

**Table 1. Register Map**

Offset	Name	Power on Default	Access <sup>(1)</sup>	Lockable?	Section
00h	STATUS	0x00	Read only	N	<a href="#">Go</a>
01h	LOCK	0x01	R/W	N	<a href="#">Go</a>
02h through 09h	RESERVED				
10h	TIACN	0x03	R/W	Y	<a href="#">Go</a>
11h	REFCN	0x20	R/W	Y	<a href="#">Go</a>
12h	MODECN	0x00	R/W	N	<a href="#">Go</a>
13h through FFh	RESERVED				

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### 7.6.1 STATUS Register (Offset = 00h)

Status Register. The status bit is an indication of the LMP91002's power-on status. If its readback is "0", the LMP91002 is not ready to accept other I<sup>2</sup>C commands.

**Figure 17. STATUS Register**

7	6	5	4	3	2	1	0
Reserved							STATUS
R							R

**Table 2. STATUS Register Field Descriptions**

Bit	Name	Function
7-1	RESERVED	
0	STATUS	Status of Device 0h = Not Ready (default) 1h = Ready

### 7.6.2 LOCK Register (Offset = 01h)

Protection Register. The lock bit enables and disables the writing of the TIACN and the REFCN registers. To change the content of the TIACN and the REFCN registers, the lock bit must be set to "0".

**Figure 18. LOCK Register**

7	6	5	4	3	2	1	0
Reserved							LOCK
							R/W

**Table 3. LOCK Register Field Descriptions**

Bit	Name	Function
7-1	RESERVED	
0	LOCK	Write protection 0h = Registers 0x10, 0x11 in write mode 1h = Registers 0x10, 0x11 in read only mode (default)

### 7.6.3 TIACN Register (Offset = 10h)

TIA Control Register. The parameters in the TIA control register allow the configuration of the transimpedance gain ( $R_{TIA}$ ).

**Figure 19. TIACN Register**

7	6	5	4	3	2	1	0
Reserved			TIA_GAIN			Reserved	

**Table 4. TIACN Register Field Descriptions**

Bit	Name	Function
7-5	RESERVED	RESERVED
4-2	TIA_GAIN	TIA feedback resistance selection 000h = External resistance (default) 001h = 2.75 kΩ 010h = 3.5 kΩ 011h = 7 kΩ 100h = 14 kΩ 101h = 35 kΩ 110h = 120 kΩ 111h = 350 kΩ
1-0	RESERVED	RESERVED

### 7.6.4 REFCN Register (Offset = 11h)

Reference Control Register. The parameters in the Reference control register allow the configuration of the Internal zero, and reference source. When the reference source is external, the reference is provided by a reference voltage connected to the VREF pin. In this condition the internal zero is defined as a percentage of VREF voltage instead of the supply voltage.

**Figure 20. REFCN Register**

7	6	5	4	3	2	1	0
REF_SOURCE	INT_Z		Reserved	DIAGNOSTIC			

**Table 5. REFCN Register Field Descriptions**

BIT	NAME	FUNCTION
7	REF_SOURCE	Reference voltage source selection 0h = Internal (default) 1h = external
6-5	INT_Z	Internal zero selection (Percentage of the source reference) 00h = 20% 01h = 50% (default) 10h = 67%
4	RESERVED	RESERVED
3-0	DIAGNOSTIC	Diagnostic step (Percentage of the source reference) 0000h = 0% (default) 0001h = 1%

### 7.6.5 MODECN Register (Offset = 12h)

Mode Control Register. The parameters in the mode register allow the configuration of the operation mode of the LMP91002.

**Figure 21. MODECN Register**

7	6	5	4	3	2	1	0
FET_SHORT	Reserved				OP_MODE		

**Table 6. MODECN Register Field Descriptions**

BIT	NAME	FUNCTION
7	FET_SHORT	Shorting FET feature 0h = Disabled (default) 1h = Enabled
6-3	RESERVED	RESERVED
2-0	OP_MODE	Mode of Operation selection 000h = Deep Sleep (default) 010h = Standby 011h = 3-lead amperometric cell



## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Gas Sensor Interface

The LMP91002 supports both 3-lead and 2-lead gas sensors. Most of the toxic gas sensors are amperometric cells with 3 leads (Counter, Worker and Reference). These leads should be connected to the LMP91002 in the potentiostat topology.

##### 8.1.1.1 3-Lead Amperometric Cell In Potentiostat Configuration

Most of the amperometric cell have 3 leads (Counter, Reference and Working electrodes). The interface of the 3-lead gas sensor to the LMP91002 is straightforward. The leads of the gas sensor should be connected to the LMP91002 pins which have the matching name

The LMP91002 is then configured in 3-lead amperometric cell mode; in this configuration the Control Amplifier (A1) is ON and provides the internal zero voltage and bias in case of biased gas sensor. The transimpedance amplifier (TIA) is ON, it converts the current generated by the gas sensor in a voltage, according to the transimpedance gain:

$$\text{Gain} = R_{TIA}$$

If different gains are required, an external resistor can be connected between the pins C1 and C2. In this case the internal feedback resistor should be programmed to "external". The  $R_{Load}$  together with the output capacitance of the gas sensor acts as a low pass filter.

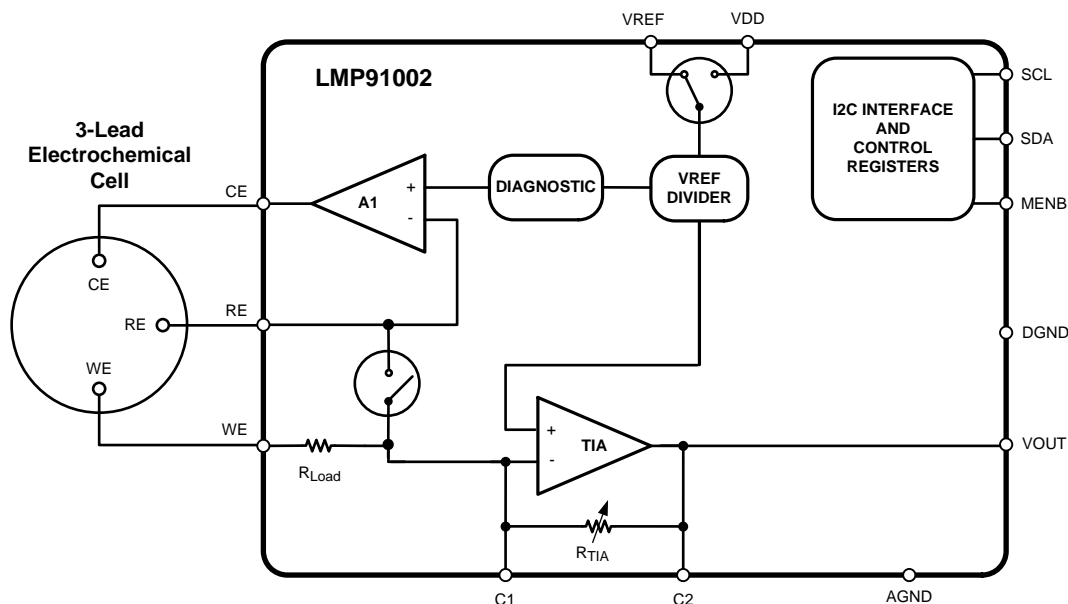


Figure 22. 3-Lead Amperometric Cell

## Application Information (continued)

### 8.1.2 Sensor Test Procedure

The LMP91002 has all the hardware and programmability features to implement some test procedures. The purpose of the test procedure is to:

- a. test proper function of the sensor (status of health)
- b. test proper connection of the sensor to the LMP91002

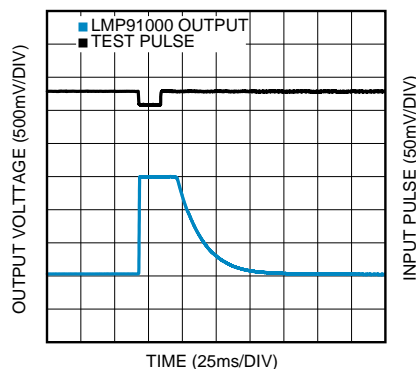
The test procedure is very easy. The diagnostic block is user programmable through the digital interface. A step voltage can be applied by the end user to the positive input of A1. As a consequence a transient current will start flowing into the sensor (to charge its internal capacitance) and it will be detected by the TIA. If the current transient is not detected, either a sensor fault or a connection problem is present. The slope and the aspect of the transient response can also be used to detect sensor aging (for example, a cell that is drying and no longer efficiently conducts the current). After it is verified that the sensor is working properly, the LMP91002 needs to be reset to its original configuration. It is not required to observe the full transient in order to contain the testing time. All the needed information are included in the transient slopes (both edges). [Figure 23](#) shows an example test procedure, a Carbon Monoxide sensor is connected to the LMP91002, a 25-mVpp pulse is applied between Reference and Working pin.

The following procedure shows how to implement the sensor test. Preliminary conditions:

The LMP91002 is unlocked and it is in 3-Lead Amperometric Cell Mode

1. Put in the [3:0] bit of the register REFCN (0x11) the 0001b value, leaving the other bit unchanged. This operation will apply a potential ( $V_{RW}$ ) between RE and WE pin ( $V_{RE} > V_{WE}$ ),  $V_{RW} = 1\%$  Source reference.
2. Put in the [3:0] bit of the register REFCN (0x11) the 0000b value, leaving the other bit unchanged. This operation will remove the potential ( $V_{RW}$ ) between RE and WE pin ( $V_{RE} > V_{WE}$ ),  $V_{RW} = 0$  V.

The width of the pulse is simply the time between the two writing operation.



**Figure 23. Test Procedure Example**

## 8.2 Typical Application

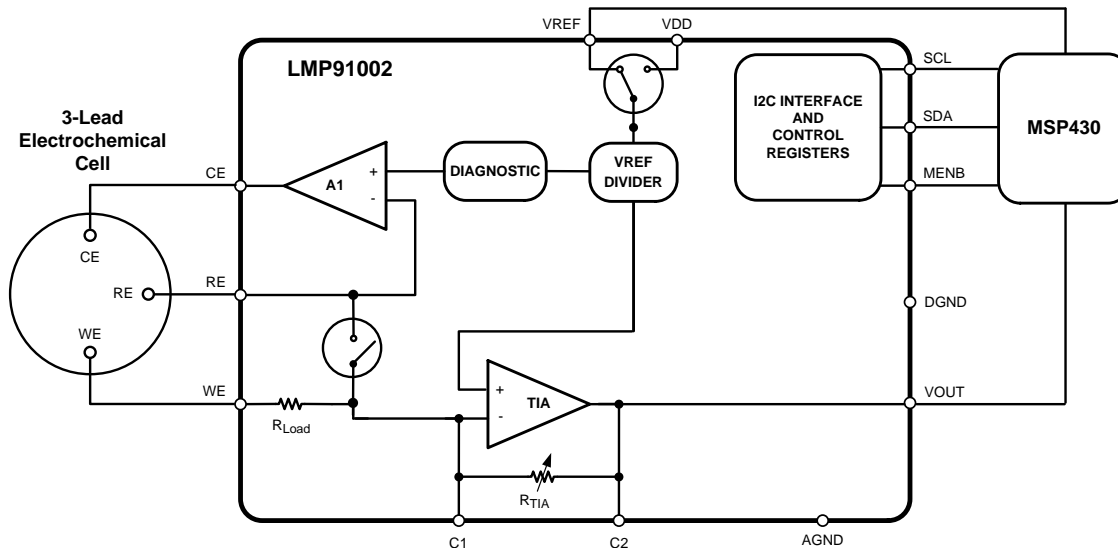


Figure 24. AFE Gas Detector

### 8.2.1 Design Requirements

The primary design requirement is selecting the appropriate TIA gain for the expected range of current over the operating range of the sensor. This gain should set the VOUT range to fall within the limits of the full-scale voltage for the ADC that is sampling the signal. For example, assume the current output range of the sensor is 0 to 100,000 nA, and the full scale ADC input range is 0 to 1 V. Because  $\text{Gain} = R_{TIA}$ , the appropriate relationship is:

$$I_{\text{SENSOR}} \times \text{Gain} = R_{TIA} \times 10^{-4} \text{ A} \leq 1 \text{ V} \quad (1)$$

Hence,  $R_{TIA} < 10^4 \Omega$ . In this case, the closest programmed gain value is 7 k $\Omega$  (see Table 4). However, if optimization of the full-scale range is desired, then alternatively,  $R_{TIA}$  can be programmed to 350 k $\Omega$ , and a 10-k $\Omega$  resistor connected between pins C1 and C2. This will give an equivalent resistance of 9.7 k $\Omega$ .

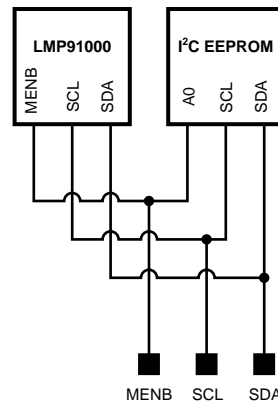
### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Smart Gas Sensor Analog Front End

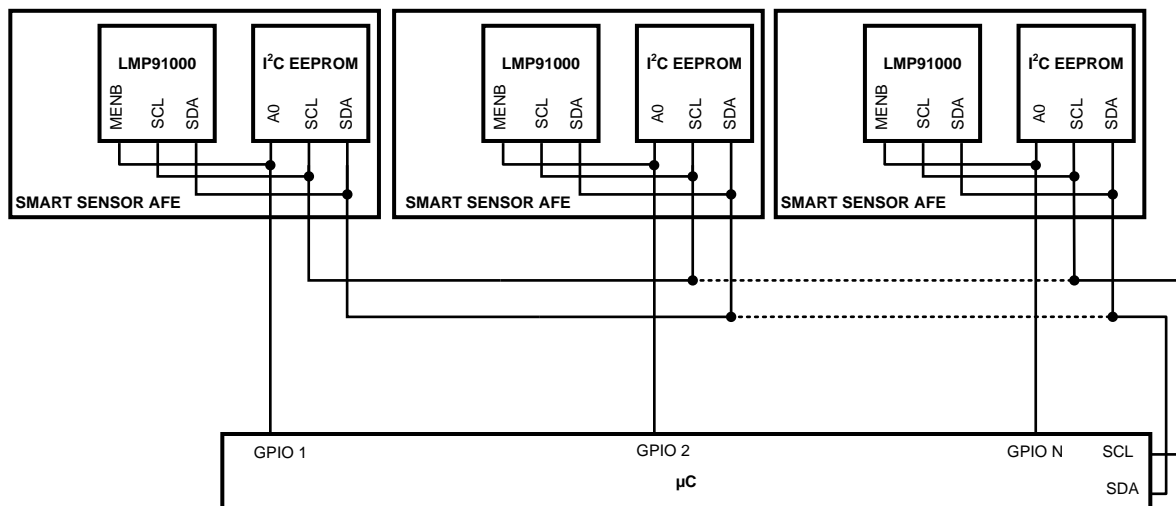
The LMP91002 together with an external EEPROM represents the core of a SMART GAS SENSOR AFE. In the EEPROM it is possible to store the information related to the GAS sensor type, calibration and LMP91002's configuration (content of registers 10h, 11h, 12h). At startup the microcontroller reads the EEPROM's content and configures the LMP91002. A typical smart gas sensor AFE is shown in Figure 25. The connection of MENB to the hardware address pin A0 of the EEPROM allows the microcontroller to select the LMP91002 and its corresponding EEPROM when more than one smart gas sensor AFE is present on the I<sup>2</sup>C bus.

#### NOTE

Only EEPROM I<sup>2</sup>C addresses with A0 = 0 should be used in this configuration.

**Typical Application (continued)**

**Figure 25. Smart Gas Sensor AFE**
**8.2.2.2 Smart Gas Sensor AFES on I<sup>2</sup>C Bus**

The connection of Smart gas sensor AFEs on the I<sup>2</sup>C bus is the natural extension of the previous concepts. Also in this case the microcontroller starts communication asserting 1 out of N MENB signals where N is the total number of smart gas sensor AFE connected to the I<sup>2</sup>C bus. Only one of the devices (either LMP91002 or its corresponding EEPROM) in the smart gas sensor AFE enabled will acknowledge the I<sup>2</sup>C commands. When the communication with this particular module ends, the microcontroller de-asserts the corresponding MENB and repeats the procedure for other modules. [Figure 26](#) shows the typical connection when several smart gas sensor AFEs are connected to the I<sup>2</sup>C bus.


**Figure 26. Smart Gas Sensor AFEs on I<sup>2</sup>C Bus**

Typical Application (continued)

8.2.3 Application Curves

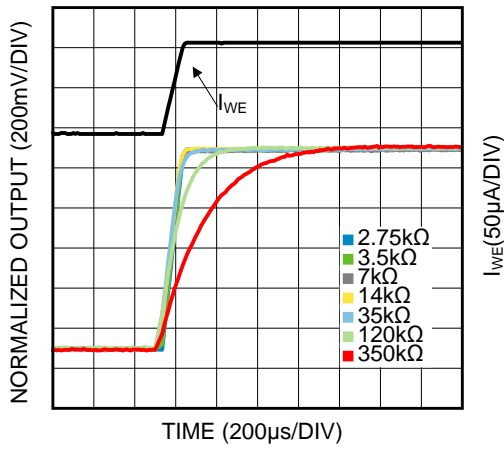


Figure 27.  $I_{WE}$  Step Current Response (Rise)

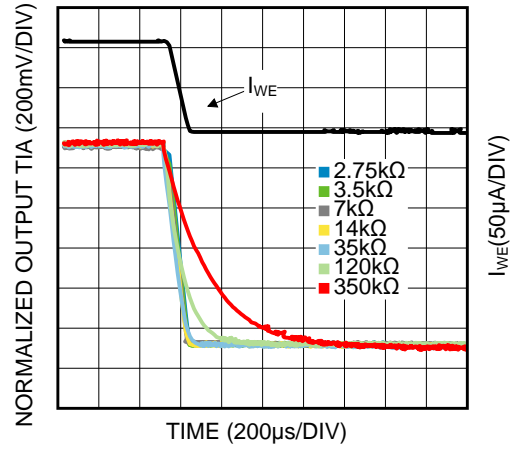


Figure 28.  $I_{WE}$  Step Current Response (Fall)

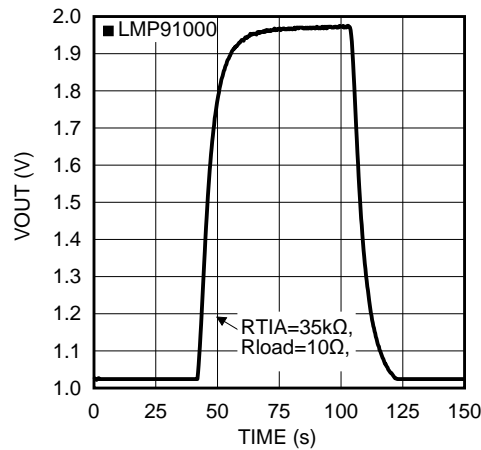


Figure 29. A  $V_{OUT}$  Step Response 100 ppm to 400 ppm CO (CO Gas Sensor Connected to LMP91002)

## 9 Power Supply Recommendations

### 9.1 Power Consumption

The LMP91002 is intended for use in portable devices, so the power consumption is as low as possible in order to ensure a long battery life. The total power consumption for the LMP91002 is below 10  $\mu\text{A}$  at 3.3-V average over time, (this excludes any current drawn from any pin). A typical usage of the LMP91002 is in a portable gas detector and its power consumption is summarized in [Table 7](#). This has the following assumptions:

- Power On only happens a few times over life, so its power consumption can be ignored
- Deep Sleep mode is not used
- The system is used about 8 hours a day, and 16 hours a day it is in Standby mode.

This results in an average power consumption of approximately 7.8  $\mu\text{A}$ . This can potentially be further reduced, by using the Standby mode between gas measurements. It may even be possible, depending on the sensor used, to go into deep sleep for some time between measurements, further reducing the average power consumption.

**Table 7. Power Consumption Scenario**

	DEEP SLEEP	STANDBY	3-LEAD AMPEROMETRIC CELL	TOTAL
Current consumption ( $\mu\text{A}$ ) typical value	0.6	6.5	10	
Time ON (%)	0	60	39	
Average ( $\mu\text{A}$ )	0	3.9	3.9	7.8
Notes				
A1	OFF	ON	ON	
TIA	OFF	OFF	ON	
I <sup>2</sup> C interface	ON	ON	ON	

## 10 Layout

### 10.1 Layout Guidelines

[Figure 30](#) and [Figure 31](#) show an example layout for the LMP91002. [Figure 30](#) shows the top layer, and [Figure 31](#) shows the bottom layer. [Figure 30](#) shows that the sensor electrodes may be arranged around the LMP91002 so that the sensor sets directly over the LMP91002, creating a compact layout. There are very few components needed for the LMP91002: one or more bypass capacitors attached to VDD, and one or two optional external components attached to pins C1 or C2 of the TIA that can provide extra filtering or gain. In the layout shown here, the VDD bypass capacitor is on the top layer, close to the LMP91002, while the optional components for the TIA are placed on the bottom layer. However, these components may also be placed on the top layer.

## 10.2 Layout Example

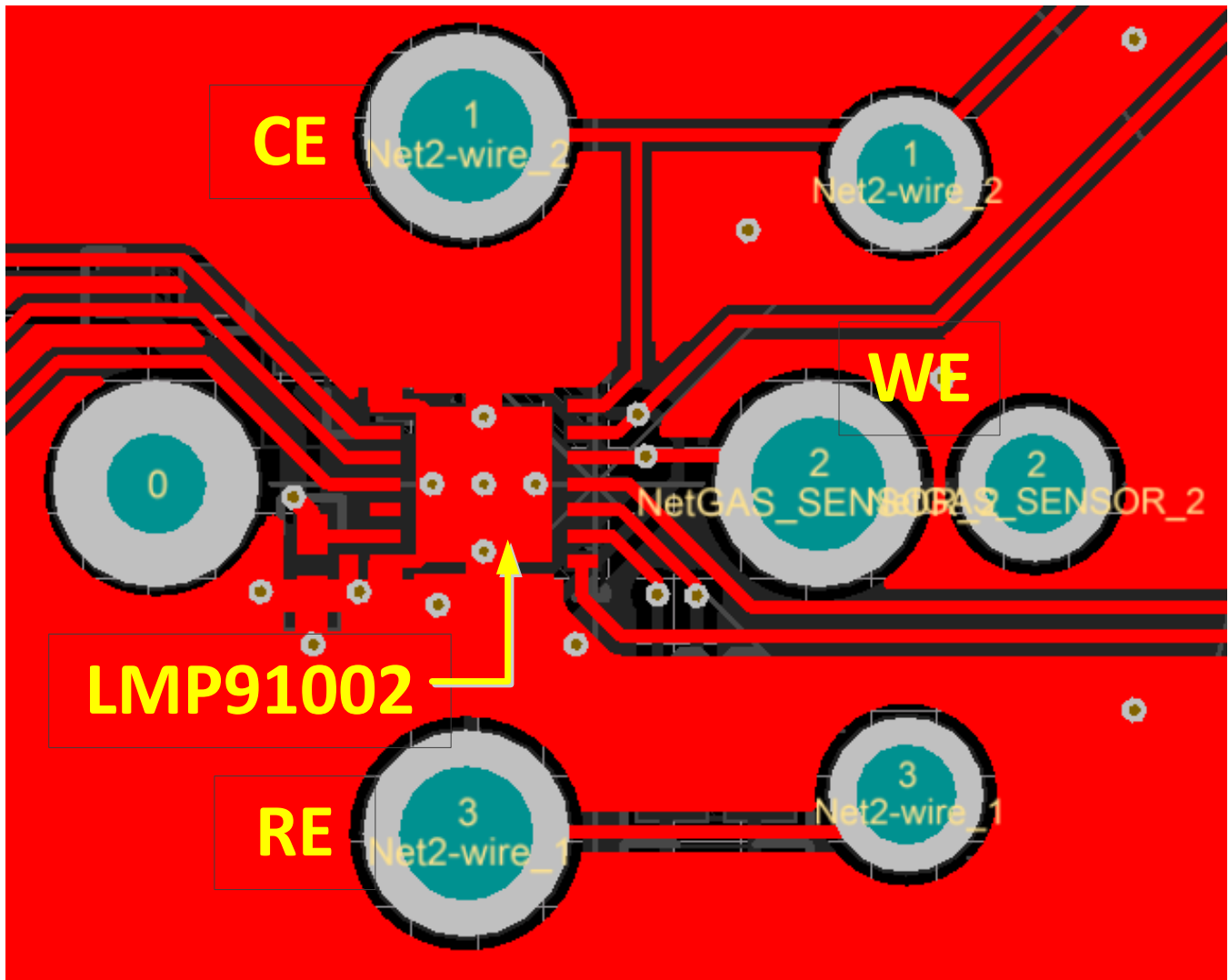


Figure 30. Layout Example – Top Layer

Layout Example (continued)

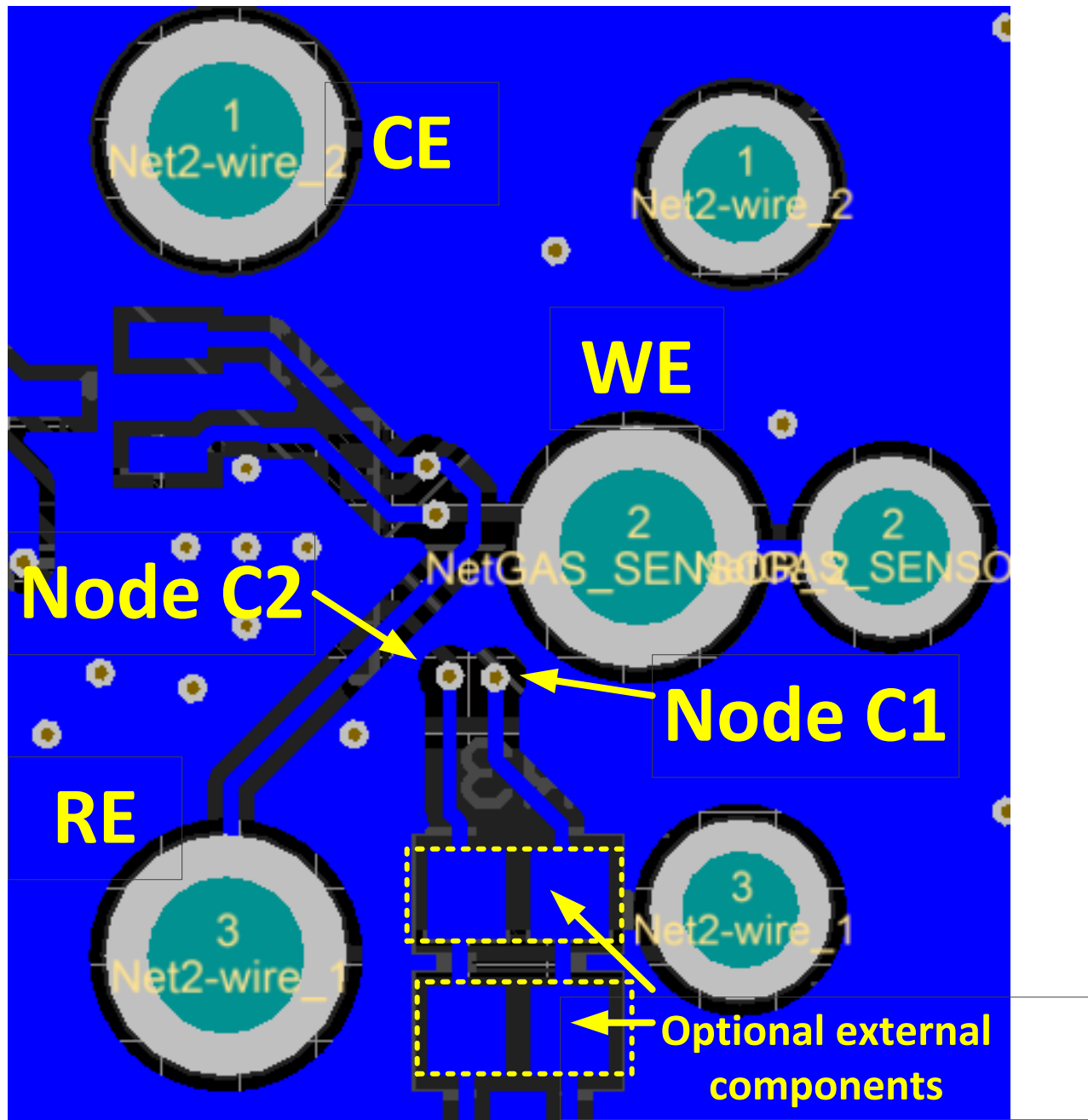


Figure 31. Layout Example – Bottom Layer



## 11 Device and Documentation Support

### 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP91002SD/NOPB	OBSOLETE	WSON	NHL	14		TBD	Call TI	Call TI	-40 to 85	L91002	
LMP91002SDE/NOPB	OBSOLETE	WSON	NHL	14		TBD	Call TI	Call TI	-40 to 85	L91002	
LMP91002SDX/NOPB	ACTIVE	WSON	NHL	14	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L91002	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

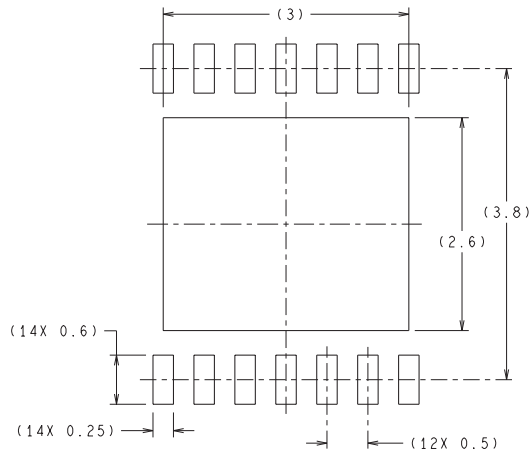
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP91002SDX/NOPB	WSO	NHL	14	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

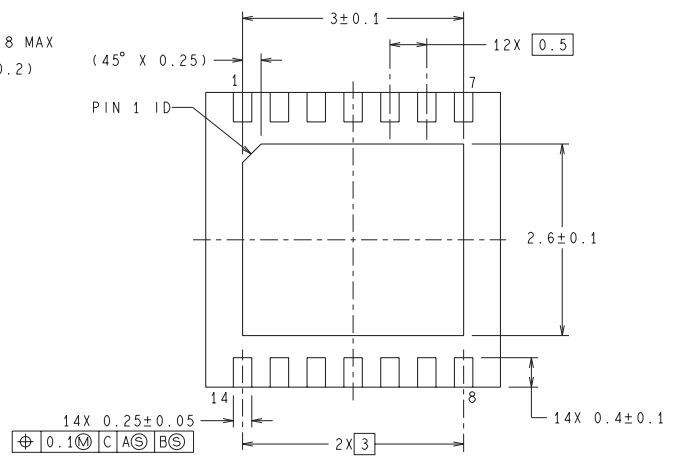
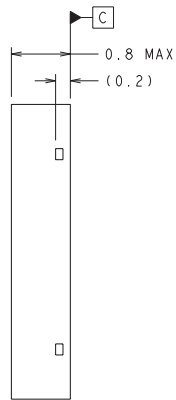
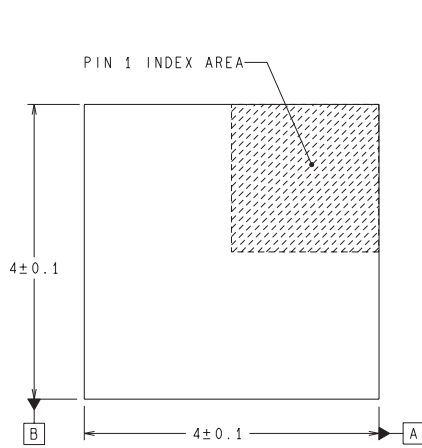
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP91002SDX/NOPB	WSON	NHL	14	4500	356.0	356.0	36.0

NHL0014B



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



SDA14B (Rev A)

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated