TEXAS INSTRUMENTS
LMK5B33414
JAJSN00 – SEPTEMBER 2022

LMK5B33414 3DPLL、3-APLL、4 入力、14 出力ネットワーク・シンクロナイザ 、BAW VCO 内蔵、イーサネット・ベースのネットワーク・アプリケーション用

1 特長

- 超低ジッタ BAW VCO ベースのイーサネット・クロック
  - 42fs (標準値) / 60fs (最大値) の RMS ジッタ (312.5MHz 時)
  - 47fs (標準値) / 65fs (最大値) の RMS ジッタ (156.25MHz 時)
- アナログ位相ロック・ループ (APLL) と対になった 3 つの高性能デジタル位相ロック・ループ (DPLL)
  - 1mHz～4kHz にプログラム可能な DPLL ループ帯域幅
  - 1ppt 未満の DCO 周波数調整ステップ・サイズ
- 4 差動またはシングルエンド DPLL 入力
  - 1Hz (1PPS)～800MHz の入力周波数
  - デジタル・ホールドオーバーおよびヒットレス・スイッチング
- 14 の差動出力、プログラム可能な HSDS/LVPECL、LVDS、および HSCL 出力形式
  - 最大 18 の合計周波数出力 (OUT0_P/N、OUT1 P/N、GPIO1、GPIO2 の 6 つの LVCMOS 周波数出力と 12 の差動出力で構成した場合)
  - 1Hz (1PPS)～1250MHz の出力周波数、プログラム可能なスイングおよび同相範囲
  - PCIe Gen 1～6 準拠
- I^2C または 3 線式 / 4 線式 SPI インターフェイス

2 アプリケーション

- 有線ネットワーク
  - データセンター間 / データセンター内相互接続
  - タイミング・カード
  - ライン・カード
  - 固定カード (ピザ・ボックス)
- SyncE (G.8262)、SONET/SDH (Stratum 3/3E、G.813、GR-1244、GR-253)、IEEE 1588 PTP セカンダリ・クロック
- 56G/112G PAM-4 SerDes 用ジッタ・クリーニング、ワンダ減衰、基準クロック生成
- 100G～800G データ・センター・スイッチ、コア・ルータ、エッジ・ルータ、WLAN
- データ・センターおよびエンタープライズ・コンピューティング
  - スマート・ネットワーク・インターフェイス・カード (NIC)
- 光伝送ネットワーク (OTN G.709)
- ブロードバンド固定回線アクセス
- 産業用
  - 試験 / 測定機器
  - 医療用画像処理

3 概要

LMK5B33414 は、タイミング精度が 5ns 未満 (クラス D) のイーサネット・ベースのネットワーキング・アプリケーションの厳しい要件を満たすように設計された、高性能ネットワーク・シンクロナイザおよびジッタ・クリーナです。

ネットワーク・シンクロナイザは、ヒットレス・スイッチングとジッタ減衰を実現するために、プログラマブルなループ帯域幅、外部ループ・フィルタ不要を特長とする 3 つの DPLL を内蔵しており、最大限の柔軟性と使いやすさを備えています。各 DPLL は、対になった APLL を DPLL リファレンス入力に位相固定します。

APLL3 は、テキサス・インスツルメンツ独自のバルク弾性波 (BAW) 技術を採用した超高性能 PLL を特長としており、DPLL の基準入力周波数にもジッタ特性にも無関係に、42fs (標準値) / 60fs (最大値) の RMS ジッタで 312.5MHz の出力クロックを生成できます。APLL2 および APLL1 には、2 番目または 3 番目の周波数ドメイン、同期ドメインのオプションがあります。

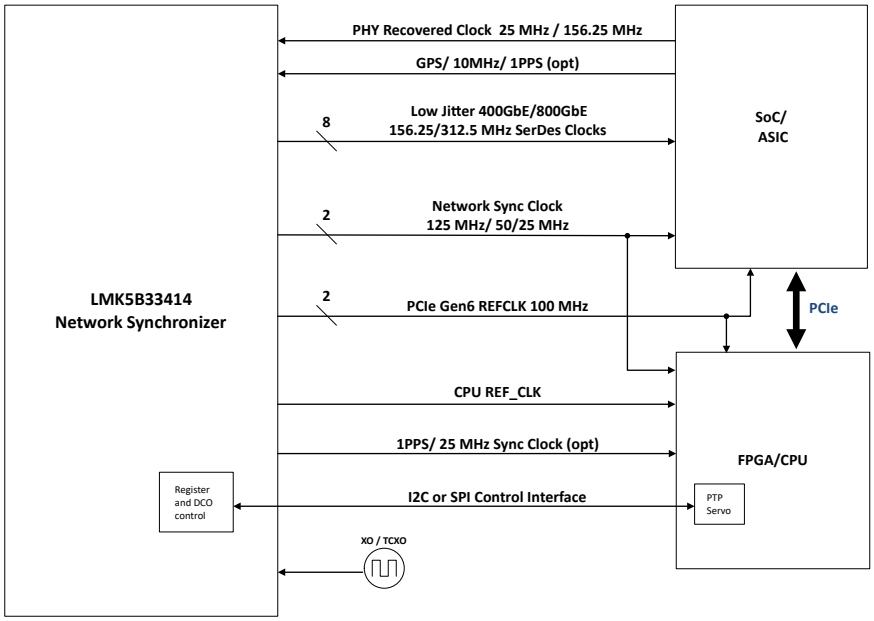
リファレンス検証回路は、DPLL 基準クロックを監視し、スイッチオーバー・イベントを検出するとクロック間でヒットレス・スイッチングを実行します。ゼロ遅延と位相キャンセルを有効にすることで、入力と出力の位相関係を制御できます。

本デバイスは、I^2C または SPI インターフェイスを介して完全にプログラム可能です。オンボード EEPROM を使用して、システムの起動クロックをカスタマイズできます。また、このデバイスには出荷時デフォルトの ROM プロファイルもフォールバック・オプションとして用意されています。

パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
LMK5B33414	VQFN (64)	9.00mm × 9.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



LMK5B33414 代表的なシステム・ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2022	*	Initial Release

5 Pin Configuration and Functions

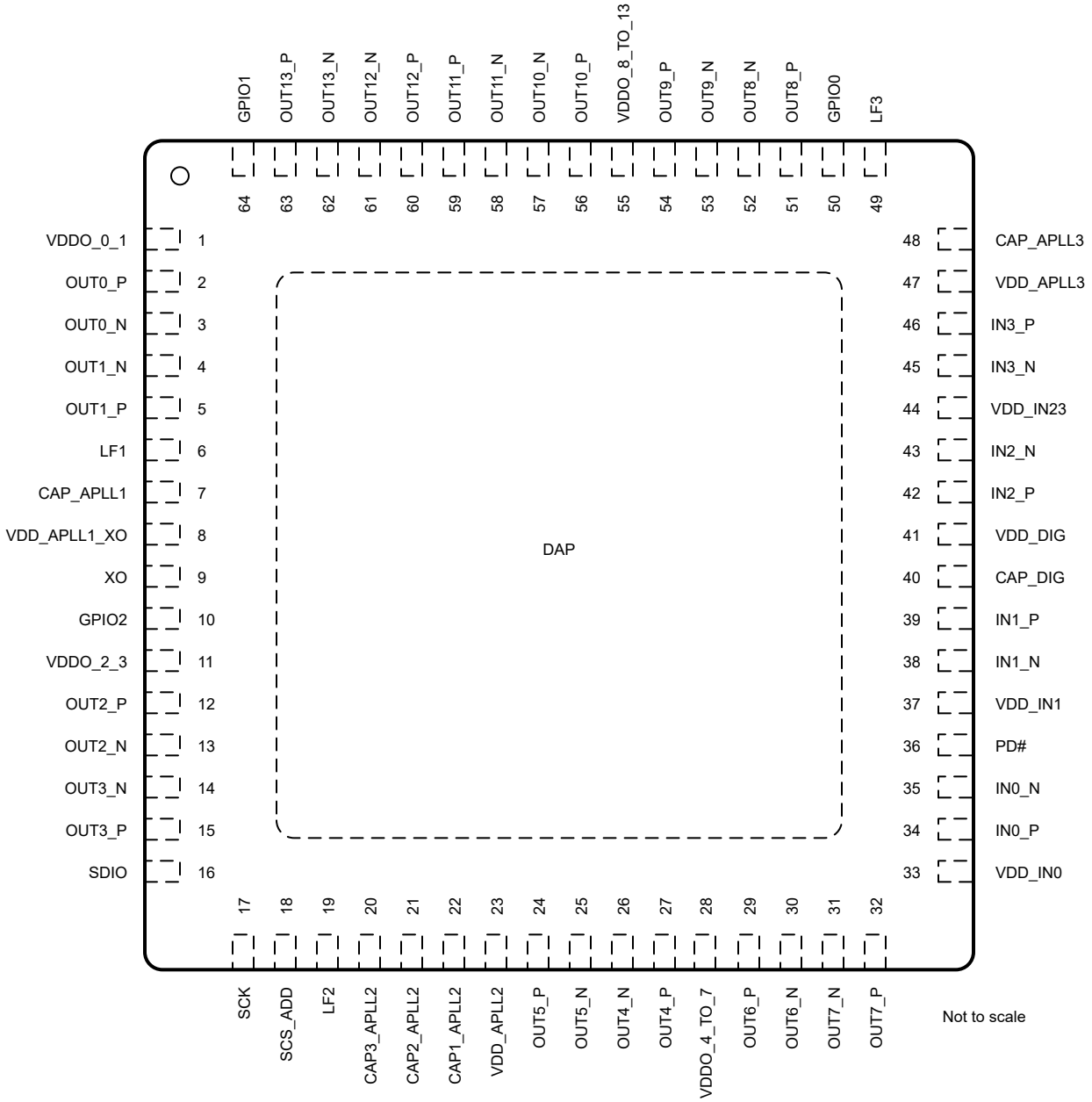


図 5-1. LMK5B33414 RGC Package 64-Pin VQFN Top View

表 5-1. LMK5B33414 Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
POWER			
VDDO_0_1	1	P	Power supply for OUT0 and OUT1
VDD_APLL1_XO	8	P	Power supply for XO and APLL1
VDDO_2_3	11	P	Power supply for OUT2 and OUT3
VDD_APLL2	23	P	Power supply for APLL2
VDDO_4_TO_7	28	P	Power supply for OUT4 to OUT7
VDD_IN0	33	P	Power supply for IN0 DPLL reference

表 5-1. LMK5B33414 Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VDD_IN1	37	P	Power supply for IN1 DPLL reference
VDD_DIG	41	P	Power supply for digital
VDD_IN23	44	P	Power supply for IN2 and IN3 reference inputs
VDD_APLL3	47	P	Power supply for APLL3
VDDO_8_TO_13	55	P	Power supply for OUT8 to OUT13
DAP	N/A	G	Ground
CORE BLOCKS (2)			
LF1	6	A	External loop filter cap for APLL1 (100 nF)
CAP_APLL1	7	A	LDO bypass capacitor for APLL1 VCO (10 µF)
LF2	19	A	External loop filter cap for APLL2 (100 nF)
CAP3_APLL2	20	A	Internal bias bypass capacitor for APLL2 VCO (10 µF)
CAP2_APLL2	21	A	Internal bias bypass capacitor for APLL2 VCO (10 µF)
CAP1_APLL2	22	A	LDO bypass capacitor for APLL2 VCO (10 µF)
CAP_DIG	40	A	LDO bypass capacitor for Digital Core Logic (100 nF)
CAP_APLL3	48	A	Internal bias bypass capacitor for APLL3 (10 µF)
LF3	49	A	External loop filter cap for APLL3 (470 nF)
INPUT BLOCKS			
XO	9	I	XO/TCXO/OCXO input pin
IN0_P	34	I	First input reference to DPLLx or buffered to OUT0 or OUT1
IN0_N	35	I	
IN1_N	38	I	Second input reference to DPLLx or buffered to OUT0 or OUT1
IN1_P	39	I	
IN2_P	42	I	Third input reference to DPLLx or buffered to OUT0 or OUT1.
IN2_N	43	I	
IN3_N	45	I	Fourth input reference to DPLLx or buffered to OUT0 or OUT1
IN3_P	46	I	
OUTPUT BLOCKS			
OUT0_P	2	O	Clock Output 0. Sources from all DPLL references, XO, all VCO post-dividers. Supports 1-PPS output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL, 1.8-V LVCMOS, or 2.65-V LVCMOS.
OUT0_N	3	O	
OUT1_N	4	O	Clock Output 1. Sources from all DPLL references, XO, all VCO post-dividers. Supports 1-PPS output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL, 1.8-V LVCMOS, or 2.65-V LVCMOS.
OUT1_P	5	O	
OUT2_P	12	O	Clock Output 2. Sources from APLL1, APLL2 and APLL3. No 1-PPS output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT2_N	13	O	
OUT3_N	14	O	Clock Output 3. Sources from same output mux as OUT2 from APLL1, APLL2 or APLL3. No 1-PPS output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL
OUT3_P	15	O	
OUT5_P	24	O	Clock Output 5. Sources from APLL2 and APLL3.Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT5_N	25	O	
OUT4_N	26	O	Clock Output 4. Sources from APLL2 and APLL3. Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT4_P	27	O	
OUT6_P	29	O	Clock Output 6. Sources from APLL2 and APLL3. Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT6_N	30	O	
OUT7_N	31	O	Clock Output 7. Sources from APLL2 and APLL3. Supports 1-PPS output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT7_P	32	O	

表 5-1. LMK5B33414 Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OUT8_P	51	O	Clock Output 8. Sources from APLL2 and APLL3. Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT8_N	52	O	
OUT9_N	53	O	Clock Output 9. Sources from APLL2 and APLL3. Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT9_P	54	O	
OUT10_P	56	O	Clock Output 10. Sources from APLL2 and APLL3. Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL
OUT10_N	57	O	
OUT11_N	58	O	Clock Output 11. Sources from APLL2 and APLL3. Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT11_P	59	O	
OUT12_P	60	O	Clock Output 12. Sources from APLL2 and APLL3. Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT12_N	61	O	
OUT13_N	62	O	Clock Output 13. Sources from APLL2 and APLL3. Capable of supporting 1-PPS or SYSREF output. Programmable formats: AC-LVPECL, HSDS, LVDS, HCSL.
OUT13_P	63	O	
LOGIC CONTROL/STATUS			
GPIO2(3)	10	I/O, S	POR: ROM page select Normal Operation: GPIO input or output (see description)
SDIO(4)	16	I/O	SPI or I^2C Data (SDA)
SCK(4)	17	I	SPI or I^2C Clock (SCL)
SCS_ADD(3)	18	I, S	SPI Chip Select (2-state) or POR: I^2C address select, LSB (3-state)
PD#	36	I	Device power down (Active low), internal 200-kΩ pullup to V_{CC}
GPIO0(3)	50	I/O, S	POR: ROM page select Normal Operation: GPIO input or output (see description)
GPIO1(3)	64	I/O, S	POR: I^2C or SPI select Normal Operation: GPIO input or output (see description)

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input or Output, A = Analog, S = Configuration.
(2) Do not apply external stimulus to core pins. These performance critical pins are not designed to meet normal latch up testing compliance levels. For best filtering performance, capacitors should be placed close to the IC.
(3) When 3 level mode is enabled during power supply ramp or when PD# is LOW: internal voltage divider of 555 kΩ to V_{CC} and 201 kΩ to GND. When 2 level input mode is enabled: internal 408-kΩ pulldown to GND.
(4) 670-kΩ pullup to internal 2.6-V LDO.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD(2)	Core supply voltages	–0.3	3.6	V
VDDO(3)	Output supply voltages	–0.3	3.6	V
V_{IN}	Input voltage range for clock and logic inputs	–0.3	VDD+0.3	V
V_{OUT_LOGIC}	Output voltage range for logic outputs	–0.3	VDD+0.3	V
V_{OUT}	Output voltage range for clock outputs	–0.3	VDDO+0.3	V
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before the PD# is pulled high to trigger the internal power-on reset (POR).
(3) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD(1)	Core supply voltages	3.135	3.3	3.465	V
VDDO_x(2)	Output supply voltages(3)	3.135	3.3	3.465	V
VDD_{OD}	Output voltage range for open drain outputs	1.71		3.465	V
T_J	Junction temperature			135	°C
$T_{CONT-LOCK}$	Continuous lock over temperature - no VCO recalibration needed			125	°C
t_{VDD}	Power supply ramp time(4)	0.01		100	ms

(1) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before internal power-on reset (POR).
(2) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.
(3) CMOS output voltage levels are determined by internal programming of the CMOS output LDO to support either 1.8 V or 2.65 V.
(4) Time for VDD to ramp monotonically above 2.7 V for proper internal power-on reset. For slower or non-monotonic VDD ramp, hold PD# low until after VDD voltages are valid.

6.4 Thermal Information

THERMAL METRIC(1) (2) (3)		LMK5B33xxx RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The thermal information is based on a 10-layer 200 mm x 250 mm board with 49 thermal vias (7 x 7 pattern, 0.3 mm holes).
(3) Ψ_{JB} can allow the system designer to measure the board temperature (T_{PCB}) with a fine-gauge thermocouple and back-calculate the device junction temperature, $T_J = T_{PCB} + (\Psi_{JB} \times \text{Power})$. Measurement of Ψ_{JB} is defined by JESD51-6.

6.5 Electrical Characteristics

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Consumption Characteristics						
I_{DD_TOT}	Total current consumption with specified configuration	312.5 MHz from OUT0 to OUT13 LVDS outputs, APLL3 post-divider = 8, channel dividers bypassed, DPLL1/2 and APLL1/2 disabled.		710	800	mA
		ROM page 6, 312.5 MHz from OUT0 to OUT13, HSDS outputs, channel dividers enabled , APLL3 post divider bypassed, DPLL1/2 and APLL1/2 disabled		980	1090	mA
		ROM page 0, APLL1/2/3 enabled		1275	1410	mA
$I_{DD\text{-}XO}$	XO input current consumption	XO		3.5		mA
$I_{DD\text{-}XO2X}$	Current consumption per XO doubler	XO doubler(1)		0.3		mA
$I_{DD\text{-}INX}$	Core current consumption per block	IN2 and IN3		5		mA
$I_{DD\text{-}DPLL}$	Current consumption per DPLL	DPLL(2)		55		mA
$I_{DD\text{-}APLL1}$	APLL1 current consumption	APLL1		90		mA
$I_{DD\text{-}APLL2}$	APLL2 current consumption	APLL2		160		mA
$I_{DD\text{-}APLL3}$	APLL3 current consumption	APLL3		120		mA
$I_{DD\text{-}ANA}$	Analog bias current consumption	Analog circuitry from VDD_APLL1_XO supply pin. Always on when device is enabled.		42		mA
$I_{DD\text{-}DIG}$	Digital control current consumption	Digital control circuitry from VDD_DIG supply pin., Always on when device is enabled.		34		mA
$I_{DDO\text{-}CHDIV}$	Current consumption per channel divider block	12-bit channel divider		20		mA
$I_{DDO\text{-}1PPSDIV}$	Current consumption per 1-PPS/ SYSREF divider block	20-bit 1-PPS/SYSREF divider		12		mA
$I_{DDO\text{-}DELAY}$	Current consumption per 1-PPS/ SYSREF analog delay block	Analog delay function enabled		10		mA

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DDO-HSDS}$	HSDS current consumption per output driver	HSDS buffer (VCM level = s1, I_{out} = 4 mA, 100-Ω termination)		19		mA
		HSDS buffer (VCM level = s1, I_{out} = 7 mA, 100-Ω termination)		22		mA
		HSDS buffer (VCM level = s1, I_{out} = 10 mA, 100-Ω termination)		25		mA
$I_{DDO-HCSL}$	HCSL current consumption per output driver	HCSL output (50-Ω termination per side)		30.5		mA
I_{DD_PD}	Power-down current consumption	Device powered-down, PD# = LOW		90	110	mA
Reference Input Characteristics (INx)						
f_{IN}	INx frequency range	Single-ended input	0.5		200e6	Hz
		Differential input	5		800	
V_{IH}	Single-ended input high voltage	DC-coupled input mode (3)	1.2		VDD + 0.3	V
V_{IL}	Single-ended input low voltage				0.5	V
$V_{IN-SE-PP}$	Single-ended input voltage swing	AC-coupled input mode (4)	0.4		2	V_{pp}
$V_{IN-DIFF-PP}$	Differential input voltage swing	AC- or DC- coupled input (5)	0.4		2	V_{pp}
V_{ICM}	Input Common Mode	DC- coupled differential input (6)	0.1		2	V
dV/dt	Input slew rate	Single-ended input	0.2	0.5		V/ns
		Differential input	0.2	0.5		V/ns
IDC	Input Clock Duty Cycle	Non 1-PPS signal	40		60	%
$t_{PULSE-1PPS}$	1-PPS pulse width for input	1-PPS or pulsed signal	100			ns
I_{IN-DC}	DC input leakage current	Single pin INx_P or INx_N, 50-Ω and 100-Ω internal terminations disabled, AC coupled mode enabled or disabled	–350		350	µA
C_{IN}	Input capacitance	Single-ended, each pin		2		pF
XO/TCXO Input Characteristics (XO)						
f_{CLK}	XO input frequency range (7)		10		156.25	MHz
V_{IH}	LVCMOS Input high voltage	DC-coupled input mode (8)	1.4		VDD + 0.3	V
V_{IL}	LVCMOS Input low voltage				0.8	V
V_{IN-SE}	Single-ended input voltage swing	AC-coupled input mode (9)	0.4		VDD + 0.3	V_{pp}
dV/dt	Input slew rate		0.2	0.5		V/ns
IDC	Input duty cycle		40		60	%
I_{IN-DC}	DC Input leakage current	Single pin XO_P, 50-Ω and 100-Ω internal terminations disabled	–350		350	µA
C_{IN}	Input capacitance on each pin			1		pF
C_{EXT}	External AC coupling cap			10		nF
APLL/VCO Characteristics						
f_{PFD}	PFD frequency range	APLL3 Fractional feedback divider			110	MHz
		APLL1, APLL2 Fractional feedback divider			125	MHz
f_{VCO1}	VCO1 Frequency range		4800		5350	MHz
f_{VCO2}	VCO2 Frequency range		5595		5950	MHz
f_{VCO3}	VCO3 Frequency range		2499.75	2500	2500.25	MHz
$t_{APLL1-LOCK}$	APLL1 lock time	Time between soft or hard reset and stable APLL1 output.		20	35	ms
$t_{APLL2-LOCK}$	APLL2 lock time	Time between soft or hard reset and stable APLL2 output.		350	460	ms
$t_{APLL3-LOCK}$	APLL3 lock time.	Time between soft or hard reset and stable APLL3 output.		12.5	13	ms

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HSDS Output Characteristics (OUTx)						
f_{OUT}	Output frequency range		1E–6		1250	MHz
$V_{OUT-DIFF}$	Differential output swing			$2\times V_{OD-HSDS}$		mVpp
$V_{OD-HSDS}$	HSDS output voltage swing	f_{out} < 100 MHz, I_{out} = 4 mA	350	400	440	mV
		f_{out} < 100 MHz, I_{out} = 7 mA	625	700	750	mV
		f_{out} < 100 MHz, I_{out} = 10 mA	900	975	1050	mV
		100 MHz ≤ f_{out} ≤ 325 MHz, I_{out} = 4 mA	335	400	445	mV
		100 MHz ≤ f_{out} ≤ 325 MHz, I_{out} = 5 mA	425	500	575	mV
		100 MHz ≤ f_{out} ≤ 325 MHz, I_{out} = 6 mA	510	600	690	mV
		100 MHz ≤ f_{out} ≤ 325 MHz, I_{out} = 7 mA	595	700	805	mV
		100 MHz ≤ f_{out} ≤ 325 MHz, I_{out} = 8 mA	680	800	920	mV
		100 MHz ≤ f_{out} ≤ 325 MHz, I_{out} = 9 mA	765	900	1035	mV
		100 MHz ≤ f_{out} ≤ 325 MHz, I_{out} = 10 mA	850	1000	1150	mV
		325 MHz < f_{out} ≤ 800 MHz, I_{out} = 4 mA	300	350	400	mV
		325 MHz < f_{out} ≤ 800 MHz, I_{out} = 7 mA	580	640	700	mV
		325 MHz < f_{out} ≤ 800 MHz, I_{out} = 10 mA	800	865	940	mV
		800 MHz < f_{out} ≤ 1250 MHz, I_{out} = 4 mA	235	320	400	mV
		800 MHz < f_{out} ≤ 1250 MHz, I_{out} = 7 mA	480	625	740	mV
		800 MHz < f_{out} ≤ 1250 MHz, I_{out} = 10 mA	600	800	1000	mV
V_{OH}	Output voltage high			$V_{OL} + V_{OD}$		mVpp
V_{OL}	Output voltage low	VCM level = s1	50	150	250	mV
		VCM level = s2+3	300	470	720	mV
V_{CM}	Output common mode voltage	VCM level = s1 or s2+3		$V_{OL} + V_{OD}/2$		V
		VCM level = s2, I_{out} = 4 mA	0.6	0.7	0.8	V
		VCM level = s3, I_{out} = 4 mA	1.125	1.25	1.375	V
t_{SKEW}	Output skew (13)	Same APLL, same post divider and channel divider values, same bank			50	ps
		Same APLL, same post divider and channel divider values, between banks			80	ps
t_R/t_F	Rise/Fall time	f_{OUT} < 100 MHz, 20% to 80%, OUT_x_CAP_EN = 0, C_L = 2 pF	200	250	350	ps
		100 MHz ≤ f_{OUT} ≤ 325 MHz, 20% to 80%, I_{out} ≥ 8 mA, OUT_x_CAP_EN = 0, C_L = 2 pF	165	225	260	ps
		100 MHz ≤ f_{OUT} ≤ 325 MHz, 20% to 80%, OUT_x_CAP_EN = 0, C_L = 2 pF	175	230	300	ps
		325 MHz < f_{OUT} ≤ 800 MHz, 20% to 80%, OUT_x_CAP_EN = 0, C_L = 2 pF	150	215	285	ps
		800 MHz < f_{OUT} ≤ 1250 MHz, 20% to 80%, OUT_x_CAP_EN = 0, C_L = 2 pF	120	205	250	ps
ODC	Output duty cycle		48		52	%
HCSL Output Characteristics (OUTx)						
f_{OUT}	Output frequency range	HSCL output mode	25	100	400	MHz
V_{OL}	Output voltage low		–150	0	150	mV
V_{OH}	Output voltage high		600	750	900	mV
VMIN	Output voltage minimum	Including undershoot	–300	0	150	mV

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VMAX	Output voltage maximum	Including overshoot	600	750	1150	mV
dV/dt	Differential output slew rate	±150 mV around center point, OUT_x_CAP_EN = 1, C_L= 2 pF	2		4	V/ns
dV/dt	Differential output slew rate	±150 mV around center point,OUT_x_CAP_EN = 0, C_L= 2 pF	3		5	V/ns
t_{SKEW}	Output skew (13)	Same APLL, same post divider and channel divider values, same bank			50	ps
		Same APLL, same post divider and channel divider values, between banks			80	ps
V_{CROSS}	Absolute voltage crossing point	f_{OUT} = 100 MHz	300		500	mV
ΔV_{CROSS}	Voltage crossing point variation	f_{OUT} = 100 MHz			75	mV
ODC	Output duty cycle		45		55	%
1.8-V LVCMOS Output Characteristics (OUT0/1)						
f_{OUT}	Output frequency range		1E–6		200	MHz
V_{OH}	Output high voltage	I_{OH} = -2 mA	1.5			V
V_{OL}	Output low voltage	I_{OL} = 2 mA			0.2	V
t_R/t_F	Output rise/fall time	20% to 80%		150		ps
t_{SK}	Output-to-output skew	OUT0_P, OUT0_N, OUT1_P, OUT1_N with same polarity, same APLL post divider and output divider values. Same polarity and output type (LVCMOS)			60	ps
		Same APLL, same post divider and output divider values. Skew between LVCMOS and differential outputs	0.7	1	1.3	ns
ODC	Output duty cycle		45		55	%
R_{OUT}	Output impedance		54	64	75	Ω
2.65-V LVCMOS Output Characteristics (OUT0/1)						
f_{OUT}	Output frequency range		1E–6		200	MHz
V_{OH}	Output high voltage	I_{OH} = -2 mA	2.3			V
V_{OL}	Output low voltage	I_{OL} = 2 mA			0.2	V
t_R/t_F	Output rise/fall time	20% to 80%		150		ps
t_{SK}	Output-to-output skew	OUT_P, OUT0_N, OUT1_P, OUT1_N with same polarity, same APLL post divider and output divider values. Same polarity and output type (LVCMOS)			60	ps
		Same APLL, same post divider and output divider values. Skew between LVCMOS and differential outputs	0.7	1.0	1.3	ns
PN_{FLOOR}	Output phase noise floor (f_{OFFSET} > 10 MHz)	25 MHz		–155		dBc/Hz
ODC	Output duty cycle		45		55	%
R_{OUT}	Output impedance		40	50	65	Ω
3.3-V LVCMOS GPIO Clock Output Characteristics (GPIO0/1/2)						
f_{OUT}	Maximum output frequency	GPIO1, GPIO2			25	MHz
V_{OH}	Output high voltage	I_{OH}= 2 mA	2.4			V
V_{OL}	Output low voltage	I_{OL}= 2 mA			0.4	V
I_{IH}	Input high current	V_{IN} = V_{DD}			100	µA
I_{IL}	Output low current	V_{IN} = 0V	-100			µA
t_R/t_F	Output rise/fall time	20% to 80%, 1 kΩ to GND	0.5	1.3	2.6	ns

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SK}	Output-to-output skew	GPIO1, GPIO2 output skew compared to OUT0_P, OUT0_N, OUT1_P, OUT1_N CMOS outputs. GPIOx_SEL = 115 fout = 100 kHz		7.5	11	ns
ODC	Output duty cycle		45		55	%
R_{OUT}	Output impedance		35	42	50	Ω
PLL Output Clock Noise Characteristics						
RJ_{APLL3}	12 kHz to 20 MHz integrated RMS jitter for APLL3 outputs	XO = 48 MHz, fout = 1250 MHz, post divider $P1_{APLL3}$ = 2, HSDS output VOD ≥ 800 mV (10)		33	45	fs
		XO = 48 MHz, fout = 625 MHz, post divider $P1_{APLL3}$ = 4, HSDS output VOD ≥ 800 mV (10)		35	50	fs
		XO = 48 MHz, fout = 500 MHz, post divider $P1_{APLL3}$ = 5, HSDS output VOD ≥ 800 mV (10)		37	50	fs
		XO = 48 MHz, fout = 312.5 MHz, post divider $P1_{APLL3}$ = 8, HSDS output VOD ≥ 800 mV (10)		42	60	fs
		XO = 48 MHz, fout = 156.25 MHz, post divider $P1_{APLL3}$ = 16, HSDS output VOD ≥ 800 mV (10)		47	65	fs
		XO = 48 MHz, fout = 312.5 MHz, bypass post divider $P1_{APLL3}$ = 1, HSDS output VOD ≥ 800 mV (11)		47	65	fs
		XO = 48 MHz, fout = 156.25 MHz, bypass post divider $P1_{APLL3}$ = 1, HSDS output VOD ≥ 800 mV (11)		55	73	fs
		XO = 48 MHz, f_{out} = 312.5 MHz, HSDS output, all VOD levels		50	80	fs
		XO = 48 MHz, f_{out} = 156.25 MHz, HSDS output, all VOD levels		60	90	fs
RJ_{APLL2}	12 kHz to 20 MHz integrated RMS jitter for APLL2 outputs	XO = 48 MHz, f_{out} = 153.6 MHz (VCO2 = 5836.8 MHz), 155.52 MHz (VCO2 = 5598.72 MHz), 174.703084 MHz (VCO2 = 5765.2 MHz) or 184.32 MHz (VCO2 = 5898.24 MHz) from APLL2. HSDS output , VOD ≥ 800 mV from OUT4, OUT5, OUT6 and OUT7 or OUT2 and OUT3. 156.25 MHz from APLL3 output in all other output banks.		110	150	fs
		XO = 48 MHz, f_{out} = 161.1328125 MHz or 322.265625 MHz (VCO2 = 5800.78125 MHz), or 212.5 MHz (VCO2 = 5950 MHz) from APLL2. HSDS output , VOD ≥ 800 mV from OUT4, OUT5, OUT6 and OUT7. 156.25 MHz from APLL3 output in all other output banks.		110	150	fs
		XO = 48 MHz, f_{out} = 245.76 MHz or 122.88 MHz (VCO2 = 5898.24 MHz) from APLL2. HSDS output , VOD ≥ 800 mV from OUT4, OUT5, OUT6 and OUT7 or OUT2 and OUT3. 156.25 MHz from APLL3 output in all other output banks.		110	150	fs
RJ_{APLL1}	12 kHz to 20 MHz integrated RMS jitter for APLL1 outputs	XO = 48 MHz, fout ≥ 100 MHz, HSDS output buffer VOD ≥ 800 mV		200	300	fs

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PSNR_{VDDO\_0\_1}$	Power supply noise rejection VDD_0_1	Vcc = 3.3V, V_N = 50 mVpp, HSDS, LVDS or LVPECL outputs. (12)		-105		dBc
$PSNR_{VDDO\_2\_3}$	Power supply noise rejection VDD_2_3	Vcc = 3.3V, V_N = 50 mVpp, HSDS, LVDS or LVPECL outputs. (12)		-105		dBc
$PSNR_{VDDO\_4\_7}$	Power supply noise rejection VDDO_4_7	Vcc = 3.3V, V_N = 50 mVpp, HSDS, LVDS or LVPECL outputs. (12)		-110		dBc
$PSNR_{VDDO\_8\_13}$	Power supply noise rejection VDDO_8_13	Vcc = 3.3V, V_N = 50 mVpp, HSDS, LVDS or LVPECL outputs. (12)		-110		dBc
$PSNR_{VDD\_APLL1\_XO}$	Power supply noise rejection VDD_APLL1_XO	Vcc = 3.3V, V_N = 50 mVpp, HSDS, LVDS or LVPECL outputs. (12)		-100		dBc
$PSNR_{VDD\_APLL2}$	Power supply noise rejection VDD_APLL2	Vcc = 3.3V, V_N = 50 mVpp, HSDS, LVDS or LVPECL outputs. (12)		-105		dBc
$PSNR_{VDD\_APLL3}$	Power supply noise rejection VDD_APLL3	Vcc = 3.3V, V_N = 50 mVpp, HSDS, LVDS or LVPECL outputs. (12)		-105		dBc
$PSNR_{VDD\_DIG}$	Power supply noise rejection VDD_DIG	Vcc = 3.3V, V_N = 50 mVpp, HSDS, LVDS or LVPECL outputs. (12)		-120		dBc
PCIe Jitter Characteristics						
$J_{PCIE-Gen1-CC}$	PCIe Gen 1 (2.5 GT/s) Common Clock jitter	APLL3, APLL2 or APLL1 output, 3x noise folding		0.8	5	ps p-p
$J_{PCIE-Gen2-CC}$	PCIe Gen 2 (5.0 GT/s) Common Clock jitter	APLL3, APLL2 or APLL1 output, 3x noise folding		85	250	fs RMS
$J_{PCIe-Gen3-CC}$	PCIe Gen 3 (8 GT/s) Common Clock jitter	APLL3, APLL2 or APLL1 output, 3x noise folding		25	100	fs RMS
$J_{PCIe-Gen4-CC}$	PCIe Gen 4 (16 GT/s) Common Clock jitter	APLL3, APLL2 or APLL1 output, 3x noise folding		25	100	fs RMS
$J_{PCIe-Gen5-CC}$	PCIe Gen 5 (64 GT/s) Common Clock jitter	APLL3, APLL2 or APLL1 output, 3x noise folding		9	50	fs RMS
$J_{PCIe-Gen6-CC}$	PCIe Gen 6 (32 GT/s) Common Clock jitter	APLL3, APLL2 or APLL1 output, 3x noise folding		6	40	fs RMS
DPLL Characteristics						
f_{TDC}	TDC rate range for DPLL1/ DPLL2/DPLL3		1E–6		26	MHz
dφ/dt	Phase slew during switchover	Programmable range		695		ns/s
DPLL-BW	DPLL loop bandwidth	Programmable loop bandwidth	0.001		4000	Hz
J_{PK}	DPLL closed-loop jitter peaking			0.1		dB
J_{TOL}	Jitter tolerance	Compliant with G.8262 Options 1 and 2. Jitter modulation = 10 Hz, 25.78152 Gbps line rate		6455		UI p-p
DCO Characteristics						
$f_{DCO-DPLL}$	DPLL DCO frequency tuning range	DPLL3, DPLL2, DPLL1	-200		200	ppm
$f_{DCO-APLL}$	DCO frequency tuning range	APLL3 in holdover or APLL only operation.	-200		200	ppm
$f_{DCO-APLL}$	DCO frequency tuning range	APLL2 in holdover or APLL only operation.	-1000		1000	ppm
Zero Delay Mode (ZDM) Characteristics						
$f_{OUT-ZDM}$	Output frequency range with ZDM enabled	DPLL3: OUT0 or OUT10	1E–6		1250	MHz
		DPLL2: OUT0 or OUT4	1E–6		700	MHz
		DPLL1: OUT0	1E–6		1250	MHz
$t_{DLY-ZDM}$	Input-to-output propagation delay with ZDM enabled	OUT0, $f_{IN} \le f_{TDC\_MAX}$, $f_{OUT} \le f_{TDC\_MAX}$, DPLLx_PH_OFFSET = 172500		150		ps

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DLY-VAR-ZDM}$	Input-to-output propagation delay variation with ZDM enabled	OUT0, $f_{IN} \le f_{TDC\_MAX}$, $f_{OUT} \le f_{TDC\_MAX}$, DPLLx_PH_OFFSET = 0			65	±ps
1-PPS Reference Characteristics						
t_{DPLL_FL}	DPLL frequency lock time with 1-PPS reference	XO = 48 MHz, initial error = ±25 ppb, -180° ≤ Θ ≤ 180°. DPLL LBW = 10 mHz, frequency lock $\Delta f_{out} \le$ ±4.6 ppm		5	6	s
t_{DPLL_PL}	DPLL phase lock time with 1-PPS reference	XO = 48 MHz, initial error = ±25 ppb, -180° ≤ Θ ≤ 180°. DPLL LBW = 10 mHz, DPLL LBW = 10 mHz, phase lock ≤ ±100 ns		34	38	s
Hitless Switching Characteristics						
t_{HIT}	Phase transient during switchover	INx = 1 Hz, INy = 1 Hz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 10 mHz.		4		± ps
		INx = 8 kHz, INy = 8 kHz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 1 Hz		19		± ps
		Nx = 25 MHz, INy = 25 MHz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 1 Hz		1.8		± ps
f_{HIT}	Frequency transient during switchover	INx = 1 Hz, INy = 1 Hz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 10 mHz		0.85		± ppb
		INx = 8 kHz, INy = 8 kHz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 1 Hz		0.45		± ppb
		INx = 25 MHz, INy = 25 MHz, frequency locked. INx and INy relative phase offset -180° ≤ Θ ≤ 180°. DPLL LBW = 1 Hz		0.63		± ppb
Programmable Output Delay Characteristics						
$t_{ANA-DLY}$	Analog delay step size (14)	APLL3 = 2500.0 MHz VCO post-divider = 2, 0.5x range scale, 1 Hz ≤ OUTx ≤ 156.25 MHz, ANA_DELAY_LINEARITY_CODE = 2		12.9		ps
		APLL3 = 2500.0 MHz , VCO post divider = 1, 2x range scale, 1 Hz ≤ OUTx ≤ 156.25 MHz, ANA_DELAY_LINEARITY_CODE = 5		25.8		ps
		APLL2 = 5625.0 MHz, VCO post-divider = 3, 1x range scale, 1 Hz ≤ OUTx ≤ 156.25 MHz, ANA_DELAY_LINEARITY_CODE = 3		17.2		ps
		APLL2= 5625.0 MHz, VCO post-divider = 4; 1x range scale, 1 Hz ≤ OUTx ≤ 156.25 MHz, ANA_DELAY_LINEARITY_CODE = 4		22.9		ps

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ANA-DLY-ERR}$	Analog delay step size error	APLL3 = 2500.0 MHz, VCO post-divider = 2, 0.5x range scale, 1 Hz ≤ OUTx ≤ 156.25 MHz, ANA_DELAY_LINEARITY_CODE = 2	-6.5		6.5	ps
		APLL3 = 2500.0 MHz, VCO post divider = 1, 2x range scale, 1 Hz ≤ OUTx ≤ 156.25 MHz, ANA_DELAY_LINEARITY_CODE = 5	-12.9		12.9	ps
		APLL2 = 5625.0 MHz, VCO post-divider = 3, 1x range scale, 1 Hz ≤ OUTx ≤ 156.25 MHz, ANA_DELAY_LINEARITY_CODE = 3	-8.6		8.6	ps
		APLL2 = 5625.0 MHz, VCO post-divider = 4; 1x range scale, 1 Hz ≤ OUTx ≤ 156.25 MHz, ANA_DELAY_LINEARITY_CODE = 4	-11.45		11.45	ps
$t_{ANA-DLY-RANGE}$	Analog delay range			31 × $t_{ANA-DLY}$		ps
$t_{ANA-DLY-ACC}$	Analog delay accuracy	Analog delay absolute accuracy for any setting N = 0 to 31 across analog delay range. Worst case error of actual value relative to expected value N × $t_{ANA-DLY-STEP}$ for ANA_DELAY_LINEARITY_CODE = 3, 4, 5	-25		25	ps
$t_{ANA-DLY-LIN}$	Analog delay linearity (15)	ANA_DELAY_LINEARITY_CODE = 2	333		450	ps
		ANA_DELAY_LINEARITY_CODE = 3	450		600	ps
		ANA_DELAY_LINEARITY_CODE = 4	600		750	ps
		ANA_DELAY_LINEARITY_CODE = 5	750		1050	ps
$t_{DIG-DLY}$	Digital delay step size	VCO post-divider frequency output = 2500 MHz , half step setting		200		ps
		VCO post-divider frequency output = 1250 MHz, full step setting		800		ps
3-Level Logic Input Characteristics (GPIO0, GPIO1, GPIO2, SCS_ADD)						
V_{IH}	Input high voltage		1.4			V
V_{IM}	Input mid voltage		0.6		0.95	V
V_{IM}	Input mid voltage self-bias	Input floating with internal bias and PD# pulled low	0.7		0.9	V
R_{IM-PD}	Internal pulldown resistor for mid level self-bias (16)		145	163	180	kΩ
R_{IM-PU}	Internal pullup for mid level self-bias (16)		470	526	580	kΩ
V_{IL}	Input low voltage				0.4	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF
2-Level Logic Input Characteristics (PD#, SCK, SDIO, SCS_ADD; GPIO0, GPIO1 and GPIO2 after power up)						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.4	V
I_{IH}	Input high current	V_{IH} = VDD, except PD#	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND, except PD#	–40		40	µA
I_{IH}	Input high current	V_{IH} = VDD, PD# with internal 200 kΩ pull-up	–57		24	µA

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input low current	V_{IL} = GND, PD# with internal 200 kΩ pull-up	–57		24	µA
t_{WIDTH}	Input pulse width for GPIO SYNC, SYSREF request, TEC trigger, DPLL input selection, FDEV trigger and FDEV_dir	Monotonic edges	200			ns
C_{IN}	Input capacitance			2		pF
Logic Output Characteristics (GPIO0, GPIO1, GPIO2, SDIO)						
V_{OH}	Output high voltage	I_{OH} = 1 mA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.4	V
t_R/t_F	Output rise/fall time	20% to 80%, LVCMOS mode, 1 kΩ to GND		500		ps
Open Drain Output (GPIO0, GPIO1, GPIO2, SDA)						
V_{OL}	Output Low Level	I_{OL} = 3 mA			0.3	V
		I_{OL} = 6 mA			0.6	V
I_{OH}	Output Leakage Current		-15		15	µA
SPI Timing Requirements (SDIO, SCK, SCS_ADD)						
f_{SCK}	SPI clock rate				20	MHz
	SPI clock rate; during SRAM read and write operations			5	10	MHz
t_1	SCS to SCK setup time (start communication cycle)		10			ns
t_2	SDI to SCK setup time		10			ns
t_3	SDI to SCK hold time		10			ns
t_4	SCK high time		25			ns
t_5	SCK low time		25			ns
t_6	SCK to SDO valid read-back data				20	ns
t_7	SCS pulse width		20			ns
t_8	SCK to SCS setup time (end communication cylce)		10			ns
I^2C Timing Requirements (SDA, SCL)						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.5	V
I_{IH}	Input leakage		–15		15	µA
C_{IN}	Input capacitance			2		pF
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.3	V
V_{OL}	Output low voltage	I_{OL} = 6 mA			0.6	V
f_{SCL}	I^2C clock rate	Standard			100	kHz
		Fast mode			400	
$t_{SU(START)}$	START condition setup time	SCL high before SDA low	0.6			µs
$t_{H(START)}$	START condition hold time	SCL low after SDA low	0.6			µs
$t_{W(SCLH)}$	SCL pulse width high		0.6			µs
$t_{W(SCLL)}$	SCL pulse width low		1.3			µs
$t_{SU(SDA)}$	SDA setup time		100			ns
$t_{H(SDA)}$	SDA hold time	SDA valid after SCL low	0		0.9	µs
$t_{R(IN)}$	SDA/SCL input rise time				300	ns
$t_{F(IN)}$	SDA/SCL input fall time				300	ns
$t_{F(OUT)}$	SDA output fall time	C_{BUS} ≤ 400 pF			300	ns

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU(STOP)}$	STOP condition setup time		0.6			µs
t_{BUS}	Bus free time between STOP and START		1.3			µs
t_{VD-DAT}	Data valid time				0.9	µs
t_{VD-ACK}	Data valid achnowledge time				0.9	µs
EEPROM Characteristics						
n_{EE-CYC}	EEPROM programming cycles				100	cycle
$t_{SRAM-R/W}$	EEPROM SRAM read/write time delay between bytes		0			ms

(1) This is the current consumption of one XO doubler. Each of the three XO doublers consume the same current.
(2) This is the current consumption of one DPLL. Each of the three DPLLs consume the same current.
(3) REFx_ITYPE = 8 or 12.
(4) REFx_ITYPE = 1, 3 or 5, non-driven input directly tied to GND, capacitor to GND or 50-Ω to GND.
(5) REFx_ITYPE = 1, 3 or 5.
(6) Combination of common mode voltage and DC coupled different input voltage must not exceed Absolute Maximum Ratings.
(7) When XO input frequency is greater than the APLL phase detector maximum supported comparison frequency, the APLL R divider must be set to minimum of divide by 2.
(8) Register XO_ITYPE = 8 or 12.
(9) Register XO_ITYPE = 1, 3 or 5
(10) OUT0 to OUT13 sourced from APLL3 post divider.
(11) APLL3 post divider bypassed by setting $P1_{APLL3}$ = 1. OUT0 to OUT13 sourced from channel dividers.
(12) PSNR is the single-sideband spur level measured in dBc when sinusoidal noise with amplitude V_N and frequency between 100 kHz and 10 MHz is injected onto VDD and VDDO pins with 1.0 µF decoupling capacitance.
(13) Output dividers are synchronized. SYNC status achieved from power up or SYNC_SW.
(14) Typical analog delay step size based on APLL post-divider output period divided by 31, times the analog delay range scale value 0.5, 1 or 2.
(15) Analog delay linearity typically selected based on the period of the analog delay range, $t_{ANA-DLY-RANGE}$.
(16) Variation of internal pullup resistor will track variation of pulldown resistor to maintain a consistent med voltage self-bias ratio.

6.6 Timing Diagrams

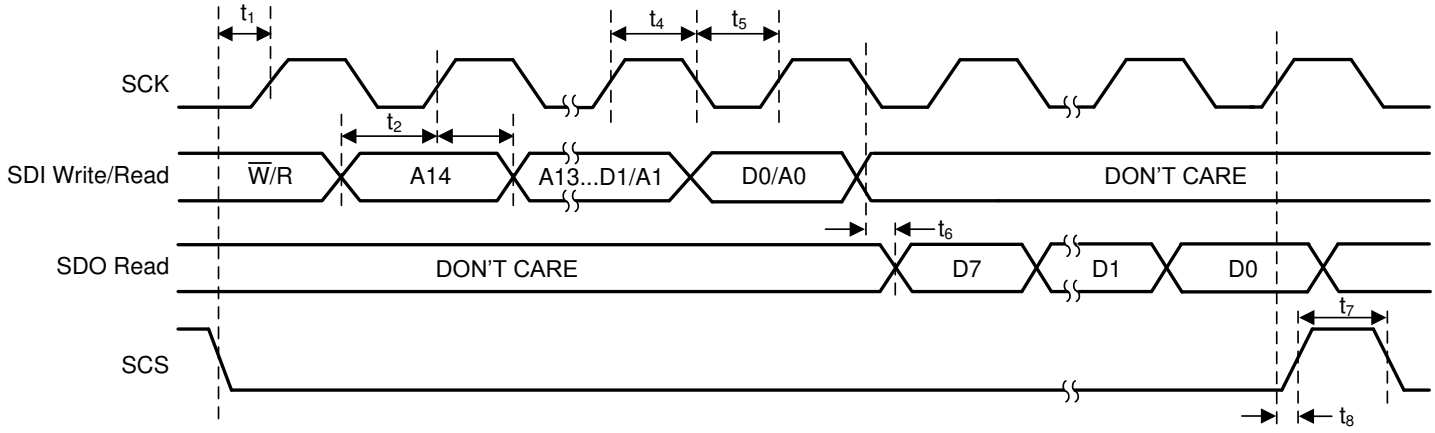


図 6-1. SPI Write Timing Diagram

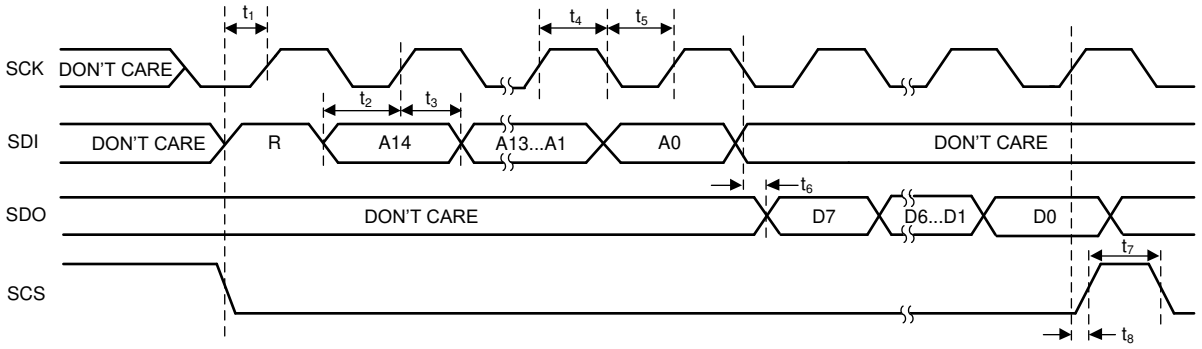


図 6-2. SPI 4-Wire Read Timing Diagram

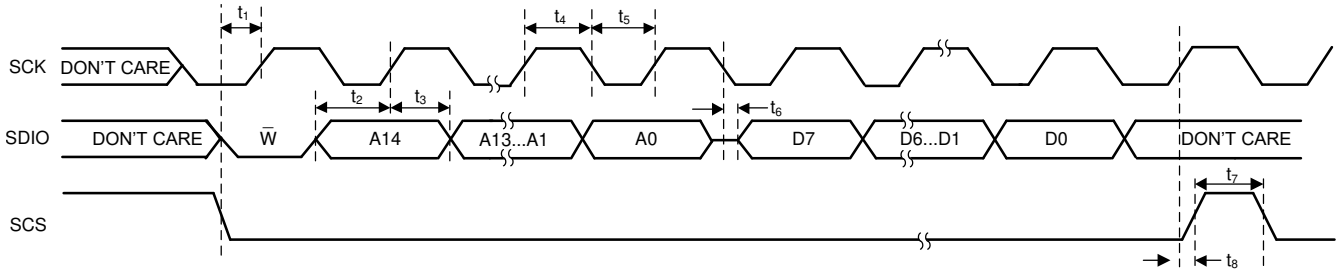


図 6-3. SPI 3-Wire Read Timing Diagram

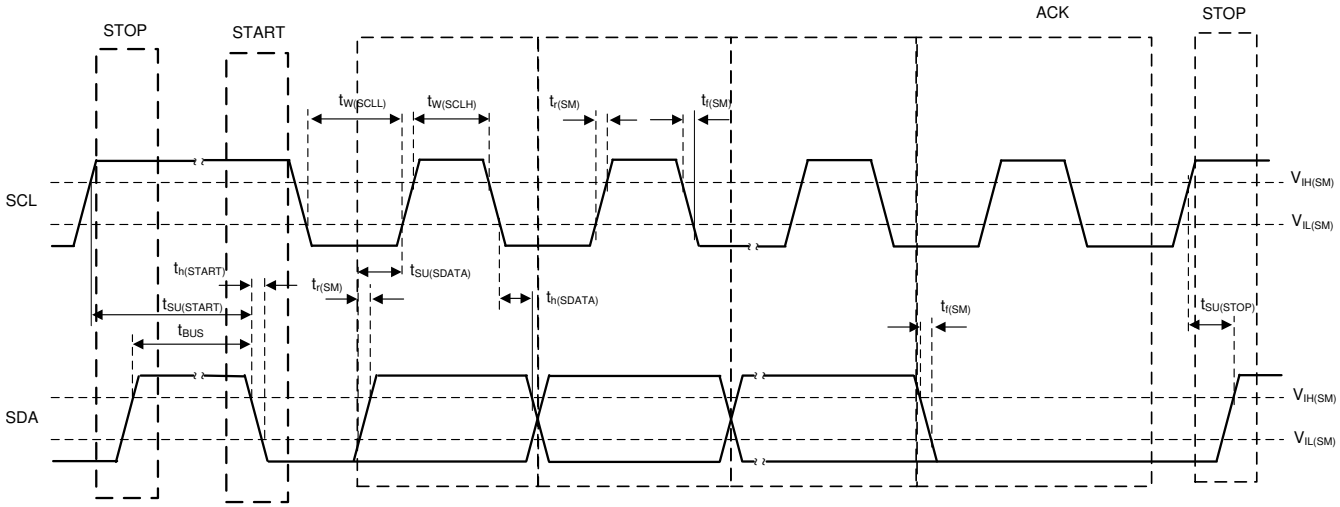


図 6-4. I²C Timing Diagram

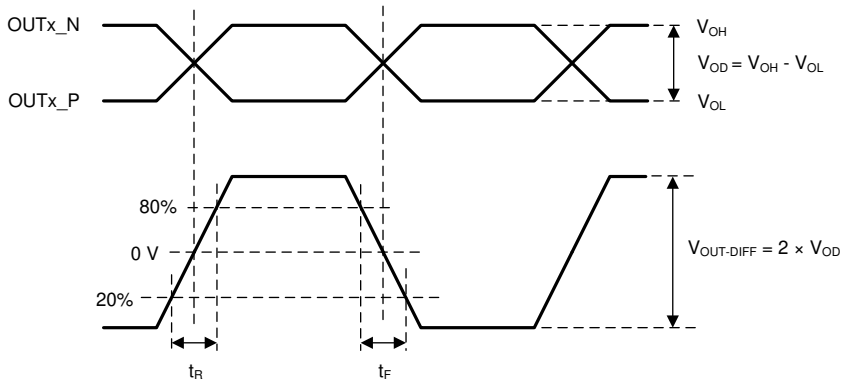


図 6-5. Differential Output Voltage and Rise/Fall Time

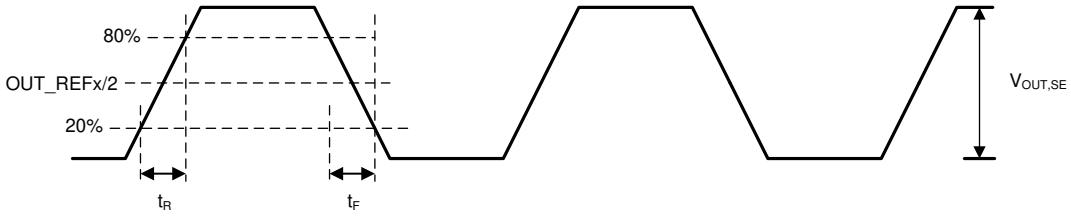


図 6-6. Single-Ended Output Voltage and Rise/Fall Time

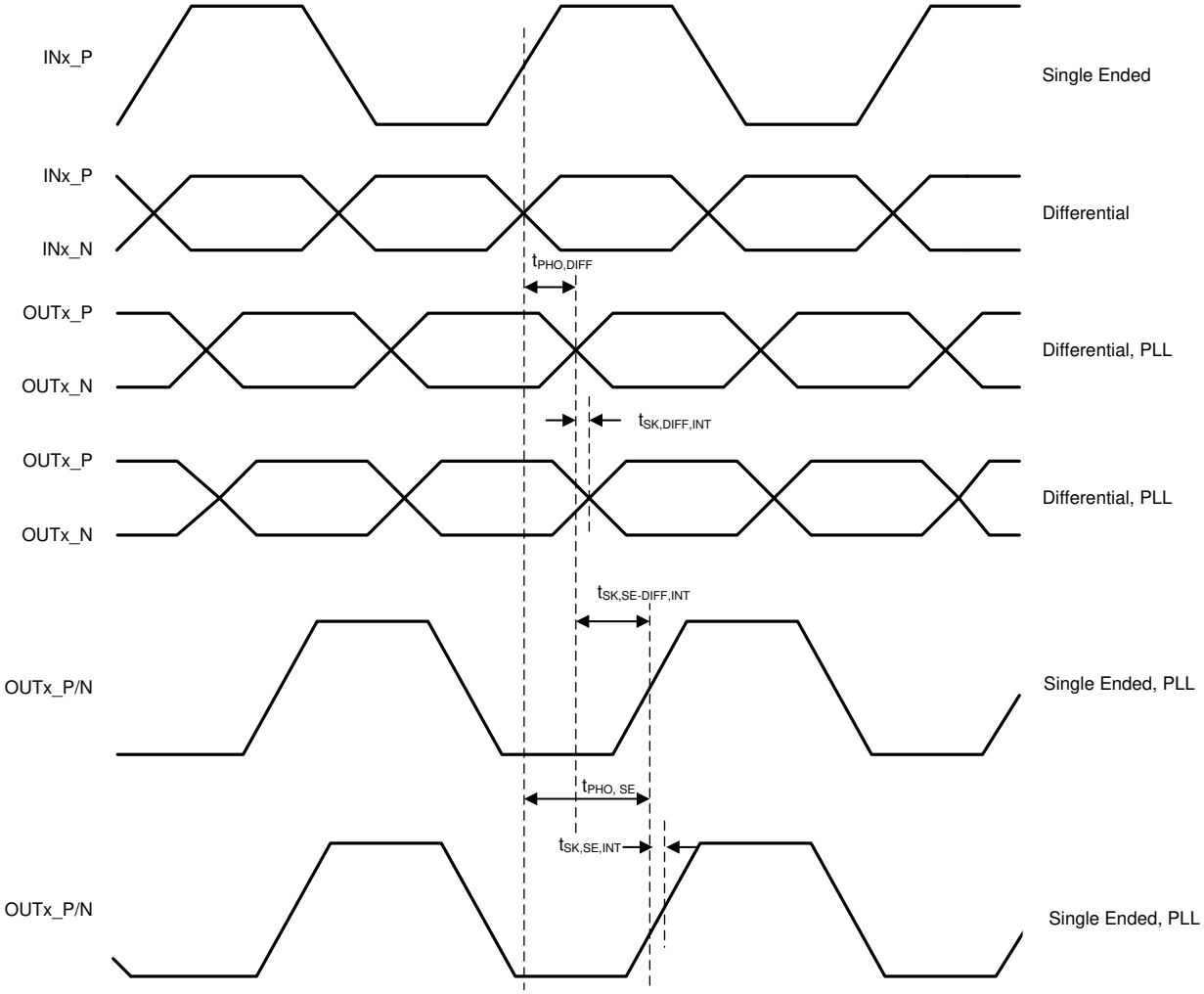
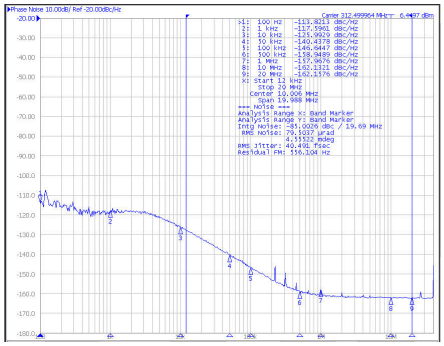


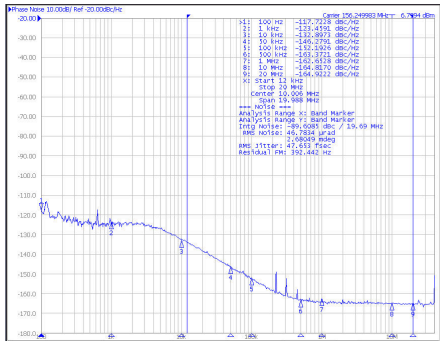
図 6-7. Differential and Single-Ended Output Skew and Phase Offset

6.7 Typical Characteristics



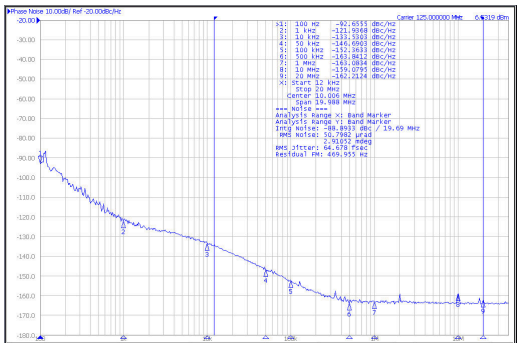
Jitter = 41 fs RMS (12 kHz to 20 MHz)
f_{APLL3} =2500 MHz (APLL3 post-divider = 8)

図 6-8. 312.5 MHz Output Phase Noise (APLL3 BAW)



Jitter = 47 fs RMS (12 kHz to 20 MHz)
f_{APLL3} =2500 MHz (APLL3 post-div = 8, div2 enabled)

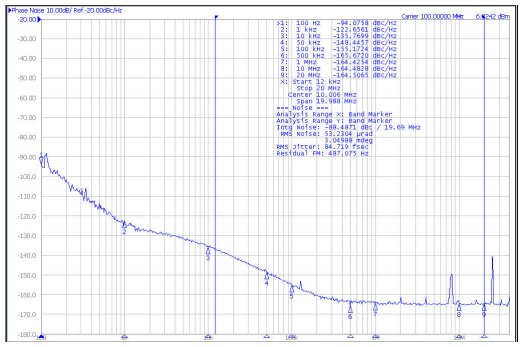
図 6-9. 156.25-MHz Output Phase Noise (APLL3 BAW)



Jitter = 65 fs RMS (12 kHz to 20 MHz)

f_{APLL3} =2500 MHz (APLL3 post-div = 5, Channel-div = 4)

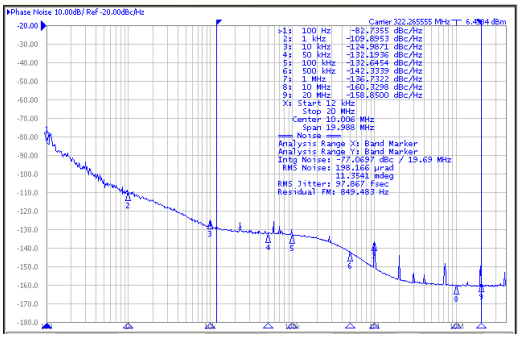
図 6-10. 125-MHz Output Phase Noise (APLL3 BAW)



Jitter = 85 fs RMS (12 kHz to 20 MHz)

f_{APLL3} =2500 MHz (APLL3 post-div = 5, Channel-div = 5)

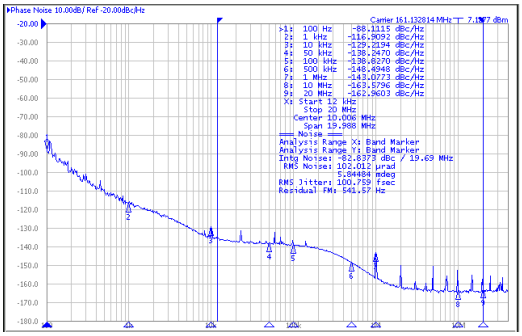
図 6-11. 100 MHz Output Phase Noise (APLL3 BAW)



Jitter = 98 fs RMS (12 kHz to 20 MHz)

f_{APLL2} = 5800.78125 MHz

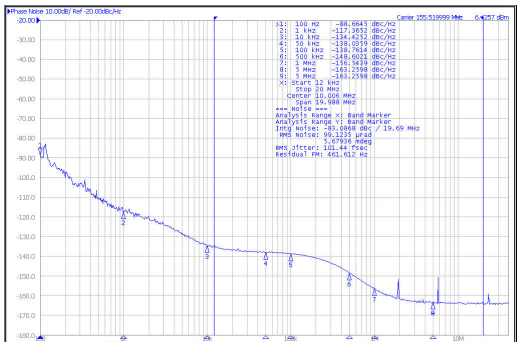
図 6-12. 322.265625 MHz Output Phase Noise (APLL2)



Jitter = 101 fs RMS (12 kHz to 20 MHz)

f_{APLL2} = 5800.78125 MHz

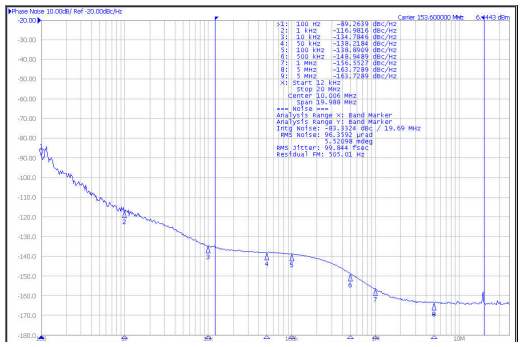
図 6-13. 161.1328125-MHz Output Phase Noise (APLL2)



Jitter = 101 fs RMS (12 kHz to 20 MHz)

f_{APLL2} = 5598.72 MHz

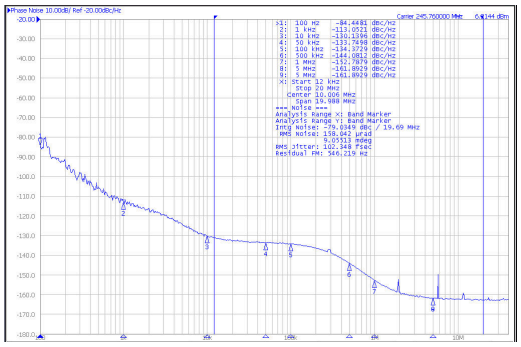
図 6-14. 155.52 MHz Output Phase Noise (APLL2)



Jitter = 100 fs RMS (12 kHz to 20 MHz)

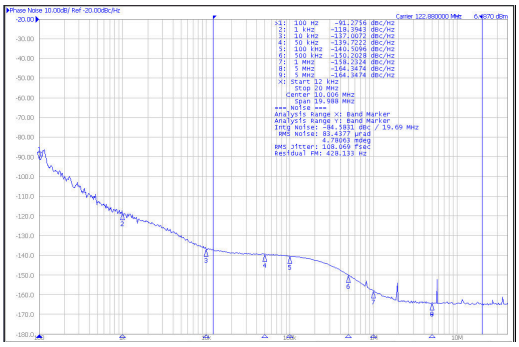
f_{APLL2} = 5836.8 MHz

図 6-15. 153.6 MHz Output Phase Noise (APLL2)



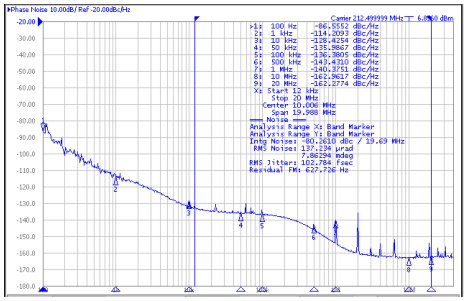
Jitter = 102 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5898.24 MHz

図 6-16. 245.76-MHz Output Phase Noise (APLL2)



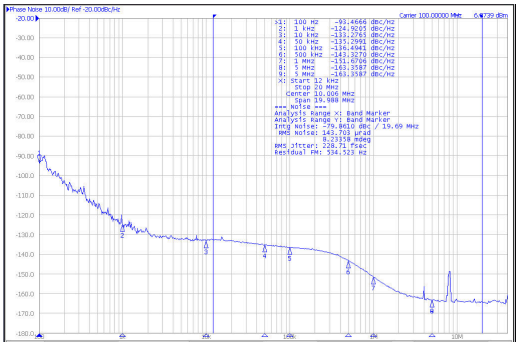
Jitter = 108 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5898.24 MHz

図 6-17. 122.88 MHz Output Phase Noise (APLL2)



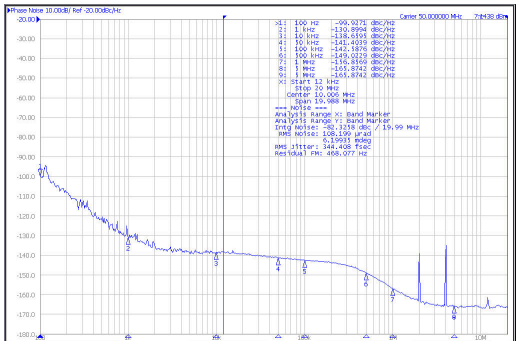
Jitter = 103 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5950 MHz

図 6-18. 212.5-MHz Output Phase Noise (APLL2)



Jitter = 230 fs RMS (12 kHz to 20 MHz)
f_{APLL1} = 5200 MHz

図 6-19. 100 MHz Output Phase Noise (APLL1)



Jitter = 345 fs RMS (12 kHz to 20 MHz)
f_{APLL1} = 5200 MHz

図 6-20. 50-MHz Output Phase Noise (APLL1)

7 Parameter Measurement Information

7.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions, causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader is able to understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

図 7-1 shows the two different definitions side-by-side for inputs and 図 7-2 shows the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

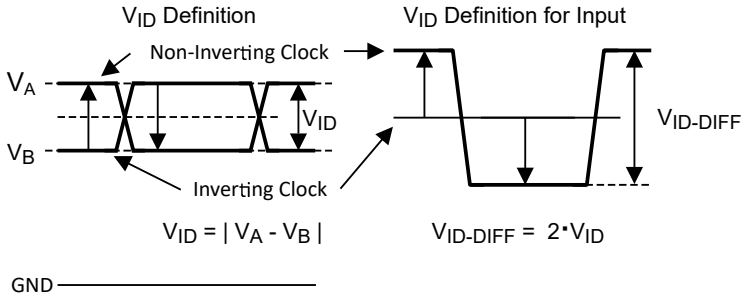


図 7-1. Two Different Definitions for Differential Input Signals

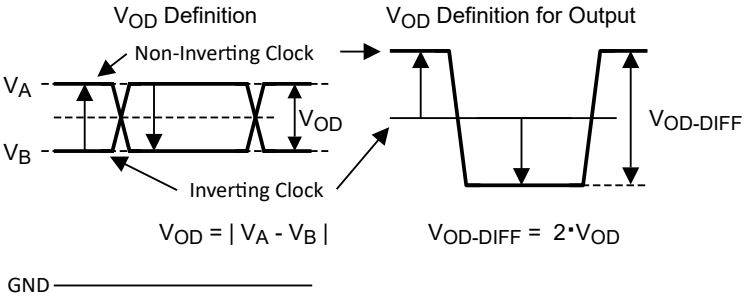


図 7-2. Two Different Definitions for Differential Output Signals

7.2 Output Clock Test Configurations

This section describes the characterization test setup for different output formats.

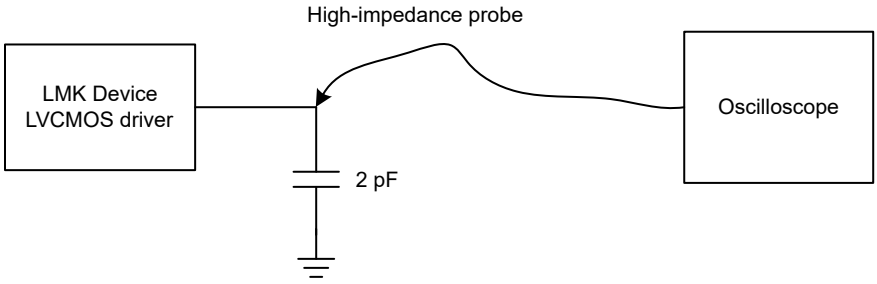


図 7-3. LVCMOS Output Time Domain Test Configuration

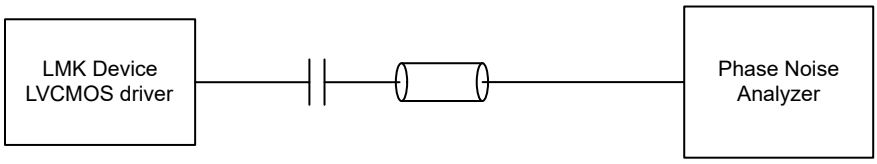


図 7-4. LVCMOS Output Phase Domain Test Configuration

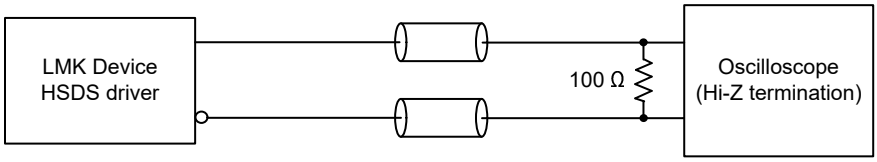


図 7-5. HSDS Output Time Domain Test Configuration

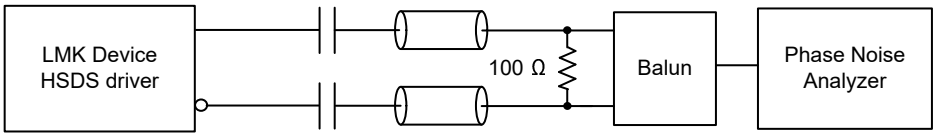


図 7-6. HSDS Output Phase Domain Test Configuration

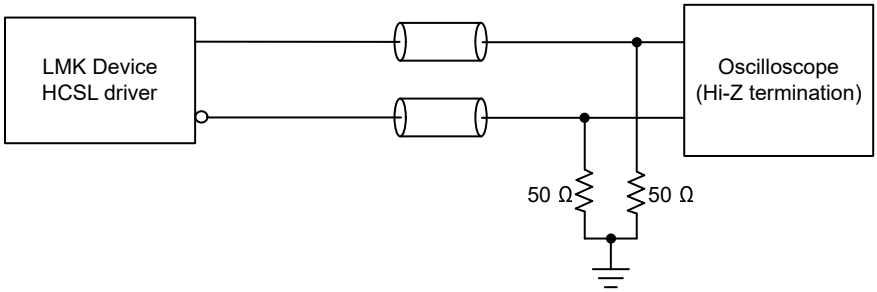


図 7-7. HCSL Output Time Domain Test Configuration

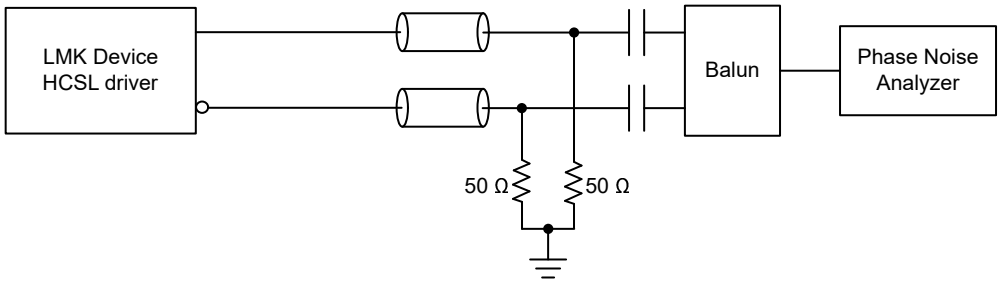
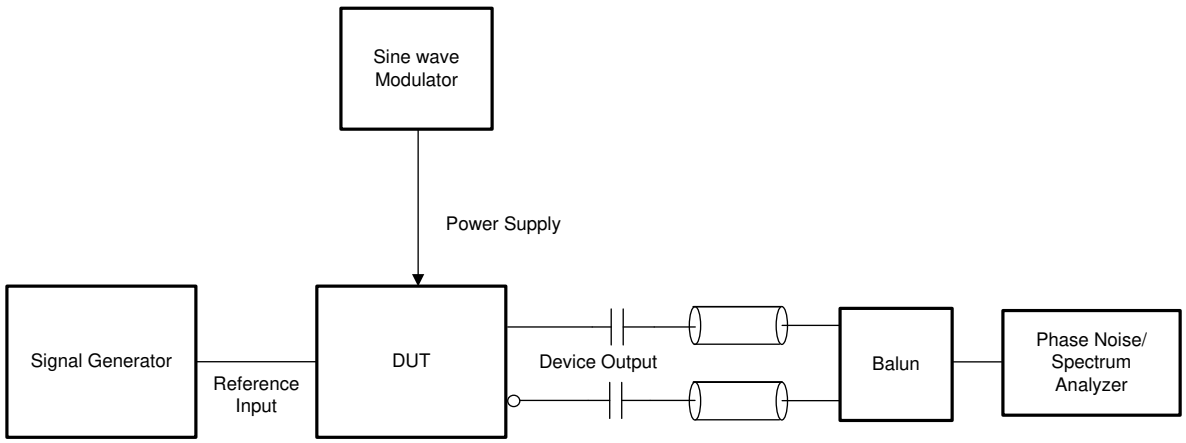


図 7-8. HCSL Output Time Domain Test Configuration



Single-side band spur level measured in dBc with a known noise amplitude and frequency injected onto the device power supply.

図 7-9. Power Supply Noise Rejection (PSNR) Test Configuration

8 Detailed Description

8.1 Overview

The LMK5B33414 has 4 reference inputs, 3 digital PLLs (DPLLs), 3 analog PLLs (APLLs) with integrated VCOs, and 14 output clocks. APLL3 uses an ultra-high performance BAW VCO (VCBO) with a very high quality factor, and thus minimizes dependency on the phase noise or frequency of the external oscillator (XO) input clock. TI's VCBO technology reduces the overall solution cost to meet the free-run and holdover frequency stability requirements. An XO, TCXO, or OCXO should be selected based on system holdover stability requirements. Each APLL can be controlled by the corresponding DPLL, allowing the APLL domain to be locked to the DPLL reference input for synchronous clock generation. Each APLL can select a reference from XO port or another APLL divided clock. Each DPLL can select a synchronization input reference from reference inputs INx or align to another APLL domain by selecting feedback from one of the cascade dividers.

The DPLL reference input mux supports automatic input selection based on priority and reference signal monitoring criteria. Manual input selection is also possible through software or pin control. The device provides hitless switching between reference sources with proprietary phase cancellation and phase slew control for superior phase buildout and transient performance. The reference clock input monitoring block monitors the clock inputs and will perform a hitless switchover or holdover when a loss of reference (LOR) is detected. A LOR condition will be detected upon any violation of the threshold limits set for the input monitors, which include frequency, missing and early pulse, runt pulse, and 1-PPS (pulse-per-second) detectors. The threshold limits for each input detector can be set and enabled per reference clock input. The tuning word history monitor feature determines the initial output frequency accuracy upon entry into holdover based on the historical average frequency when locked, thereby minimizing the frequency and phase disturbance during a LOR condition.

The LMK5B33414 has fourteen outputs with programmable output driver types, allowing up to fourteen differential clocks, or a combination of differential and single-ended clocks. Up to four single-ended 1.8-V or 2.65-V LVCMOS clocks (each from _P and _N outputs from OUT0 and OUT1). Each output clock derives from one of three APLL/VCO domains through the output muxes. Output 0 (OUT0) and Output 1 (OUT1) are the most flexible and may select their source from the XO, reference input, or any APLL domain. A 1-PPS output can be supported on Output 0 (OUT0) and Output 1 (OUT1). The output dividers have a SYNC feature to allow multiple outputs to be phase-aligned. Deterministic phase alignment can also be achieved through the zero-delay mode (ZDM) synchronization. ZDM achieve a deterministic phase alignment between a clock from any DPLL presented to OUT0 and the selected reference input. ZDM feedback paths are also available on OUT10 for DPLL3 and OUT4 for DPLL2.

To support IEEE 1588 PTP secondary clock or other clock steering applications, the DPLL supports DCO mode with less than 1-ppt (part per trillion) frequency resolution for precise frequency and phase adjustment through software or pin control.

The device is fully programmable through I^2C or SPI and supports start-up frequency configuration with factory pre-programmed internal ROM pages. A programmable EEPROM overlay, which allows POR configuration of registers related to APLL and output configuration, provides flexible power up output clocks. Internal LDO regulators provide excellent PSNR to reduce the cost and complexity of the power delivery network. The clock input and PLL monitoring status are visible through the GPIO status pins and interrupt registers readback for full diagnostic capability.

8.2 Functional Block Diagram

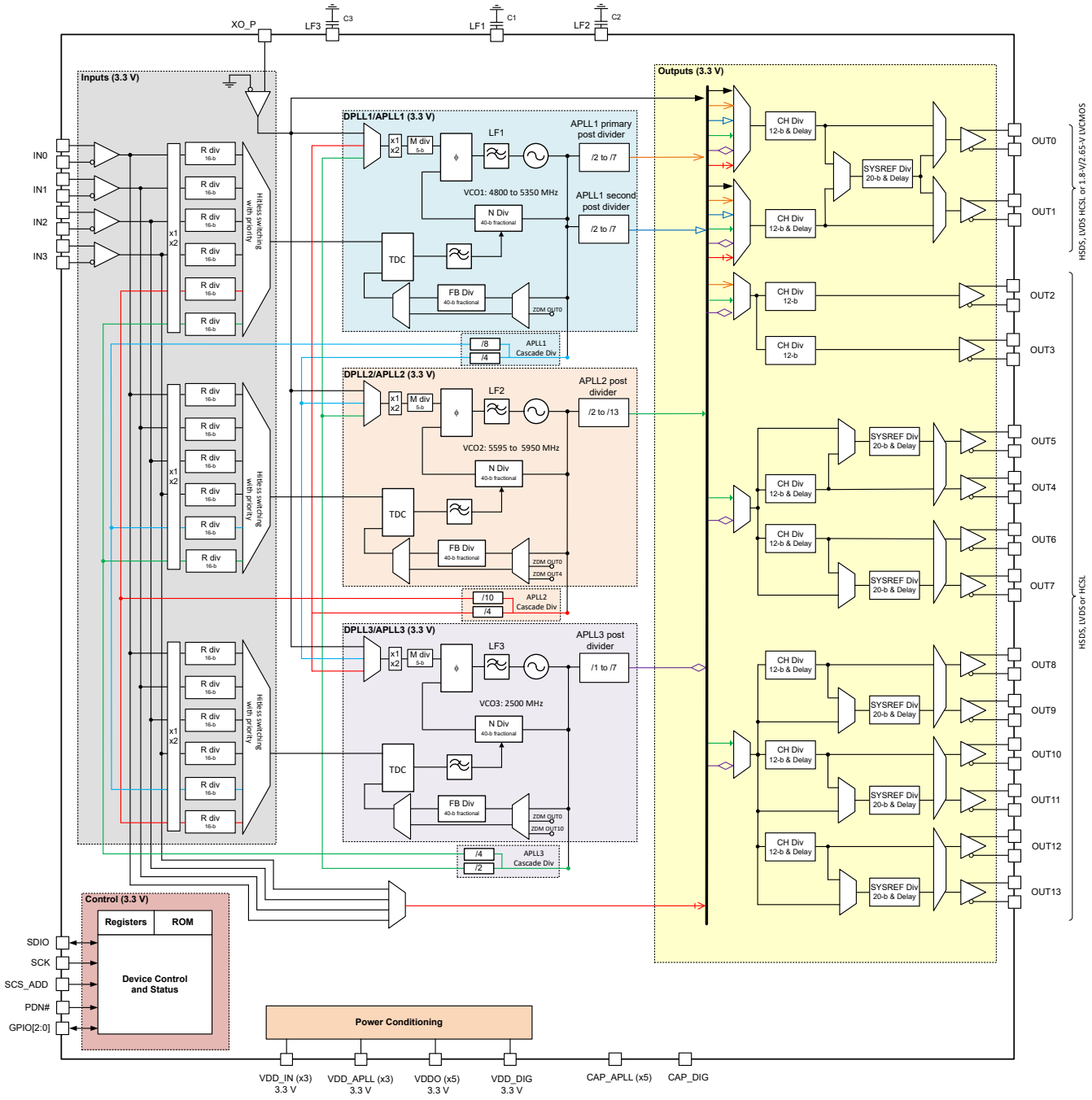


図 8-1. Top-Level Block Diagram

8.2.1 PLL Architecture Overview

The DPLL is comprised of a time-to-digital converter (TDC), digital loop filter (DLF), and programmable 40-bit fractional feedback (FB) divider with sigma-delta-modulator (SDM). The APLLs are comprised of a reference (R) divider, phase-frequency detector (PFD), loop filter (LF), fractional feedback (N) divider with SDM, and VCO.

Each DPLL has a reference selection mux that allows the DPLL to be either locked to any reference input or another APLL's cascade divider output. TI's cascading architecture provides unique flexibility for hybrid synchronization of frequency and phase control across multiple clock domains.

Each APLL has a reference selection mux that allows the APLL to be either locked to the XO input, or another APLL's cascade divider output.

Each APLL has a fixed 40-bit denominator controllable by the DPLL when locked to an input reference. When one or more of the APLL are operating without DPLL control in APLL only mode, a programmable 24-bit denominator is also available for selection to synthesize exact frequency ratios. TI recommends the programmable 24-bit denominator when implementing hybrid synchronization or cascading between frequency domains in order to maintain 0 ppm frequency error without DPLL control.

Do not cascade one VCO output to both the DPLL reference and APLL reference of the same DPLL/APLL pair.

Any unused DPLL or APLL should be disabled (powered-down) to save power. Each APLL's VCO drives the clock distribution blocks through their respective VCO post-dividers. If the post-divider setting is 1 for VCO3, the post-divider is bypassed and VCO3 feeds the output clock distribution blocks directly.

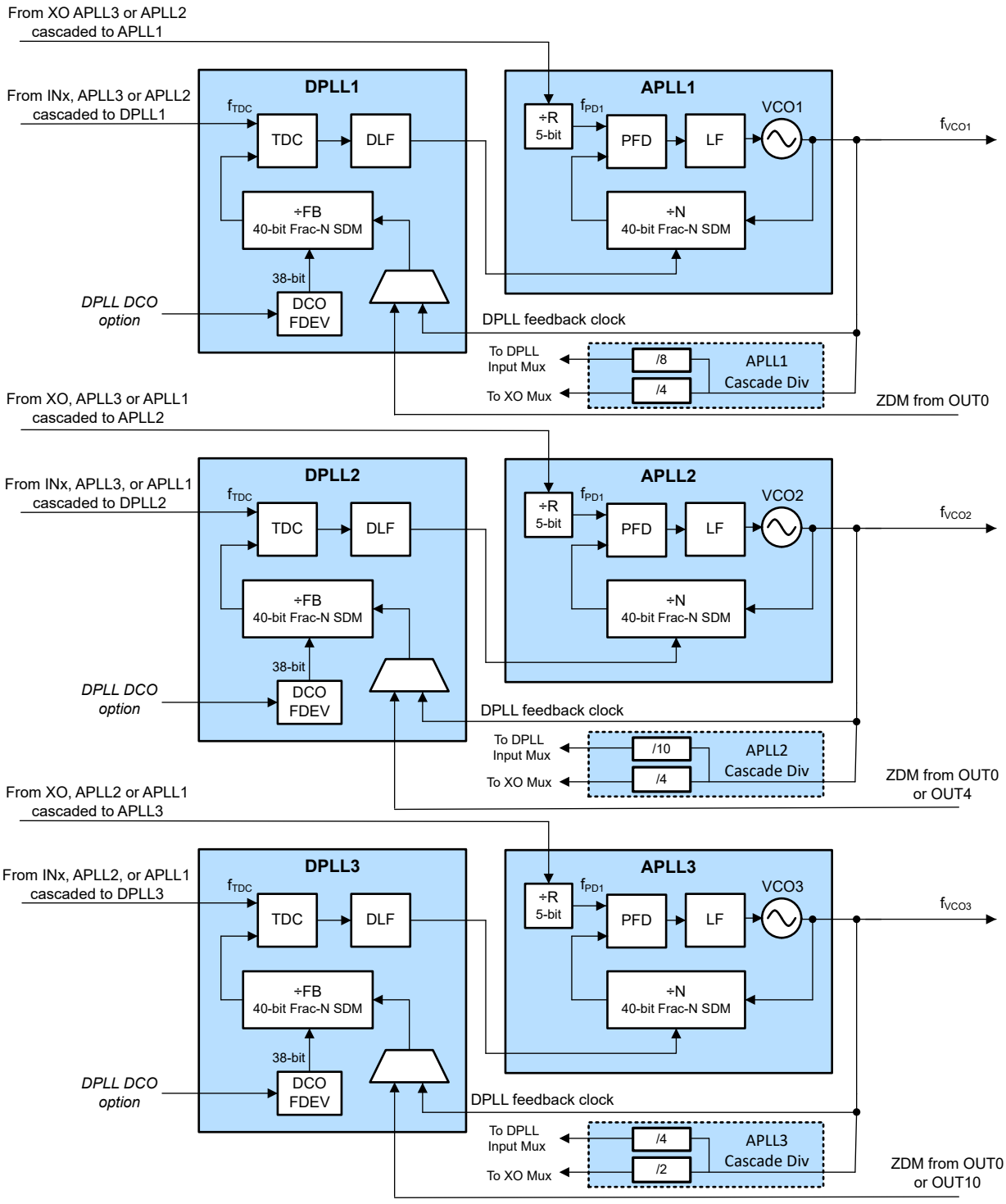


図 8-2. PLL Architecture

The following sections describe the basic principles of DPLL and APLL operation. See *DPLL Operating States* for more details on the PLL modes of operation including holdover.

8.2.2 DPLL

When DPLL operation is enabled, the clock source on the XO pin determines the free-run and holdover frequency stability and accuracy of the output clocks. The VCBO determines the APLL3 output clock phase noise and jitter performance over the 12-kHz to 20-MHz integration band, regardless of the frequency and jitter

of the XO pin input. This increased immunity from reference noise degradation allows the APLL3 to use a cost-effective, low-frequency TCXO or OCXO as the external XO input while still maintaining standards-compliant frequency stability and low loop bandwidth (≤10 Hz) required for SyncE and PTP synchronization applications. APLL1 and APLL2 with standard LC type VCOs can be optimized for best jitter performance over the DC to 100-kHz integration band by using a wide loop bandwidth with a clean reference and a high phase detector frequency. When encountering system performance limitations arising from XO frequency or phase noise, there are unique cascading options to provide a clean high frequency reference for APLL1 and APLL2. The LMK5B33414 allows selecting the divided output from the VCBO (APLL3 Cascaded) which can significantly reduce APLL1 and APLL2 output RMS jitter.

If DCO mode is enabled on a DPLL, a frequency deviation step value (FDEV) can be programmed and used to adjust (increment or decrement) the DPLL's FB divider numerator. The DCO frequency adjustment effectively propagates through the APLL domain to the output clocks and any cascaded DPLL/APLL domains.

The programmed DPLL loop bandwidth (BW_{DPLL}) should be lower than all of the following:

1. 1/100th of the DPLL TDC rate.
2. 1/10th the APLL loop bandwidth.
3. The maximum DPLL bandwidth setting of 4 kHz.

8.2.2.1 Independent DPLL Operation

In the independent mode, each DPLL can select a reference as preferred. DPLL's can share the same reference, or each select a different reference. At start-up, each APLL will lock to the XO input after initialization and operate in free-run mode. When a valid DPLL reference input is detected, each DPLL begins lock acquisition on independent reference priority. Each DPLL's TDC compares the phase of the selected reference input clock to the FB divider clock from the respective VCO and generates a digital correction word corresponding to the phase error. The correction word is filtered by the digital loop filter (DLF), and the DLF output adjusts the APLL N divider numerator to pull the VCO frequency into lock with the reference input.

Since each DPLL can work independently in this mode, the DPLLs can lock or unlock without impacting other channels.

When selecting an XO frequency, TI recommends to avoid ratios falling near integer or half integer boundaries to minimize spurious noise. Ideally, it is best to select a XO frequency that results in an APLL fractional N divider ratio (NUM/DEN) between the range of 0.125 to 0.45 and 0.55 to 0.875. Choosing a higher frequency XO is better for jitter performance, especially for APLL1 and APLL2 outputs. If the XO frequency or phase noise performance has gap to what performance is required for APLL1 or APLL2 outputs, there is an option to adopt cascaded mode using APLL3 as the reference to APLL1 or APLL2.

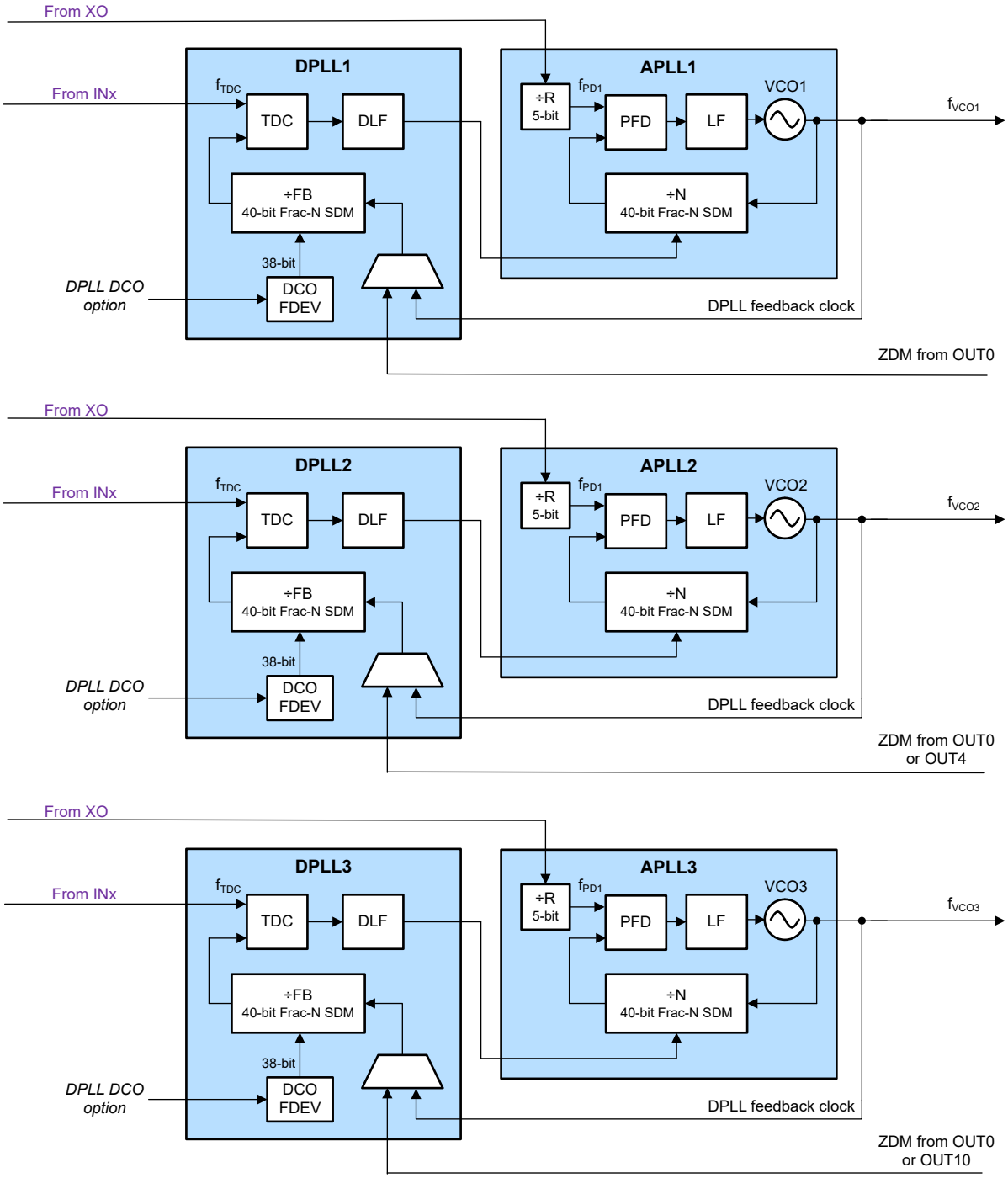


図 8-3. DPLL Independent Mode

8.2.2.2 Cascaded DPLL Operation

図 8-4 shows an example where DPLL1 and DPLL2 are in cascaded mode from DPLL3/APLL3. In this example, DPLL3 is the main synchronization DPLL, DPLL1, and DPLL2 are cascaded DPLLs.

Cascading of DPLLs provides clean, low jitter output clocks synchronized with DPLL3. When all enabled DPLLs and APLLs are locked, all enabled outputs will be synchronized to the reference selected by the main synchronization DPLL.

When no valid reference input is present, APLL1, APLL2, and APLL3 lock their VCO frequencies to the external XO input and operate in free-run mode .

When a valid DPLL reference input is detected, the main synchronization DPLL3 begins lock acquisition. The DPLL3 TDC compares the phase of the selected reference input clock with the FB divider clock from the respective VCO3 and generates a digital correction word corresponding to the phase error. The correction word is filtered by the DLF, and the DLF output adjusts the APLL N divider numerator to pull the VCO frequency into lock with the reference input.

DPLL3 lock status may not necessarily impact DPLL1 and DPLL2 lock status. If APLL3 is in free-run mode or holdover mode, and the VCBO frequency offset ppm value is still withing the valid reference conditions for DPLL1 and DPLL2, then cascaded DPLL1, APLL1, DPLL2, and APLL2 are able to maintain lock status while tracking the same frequency offset as APLL3. Note in cascaded DPLL mode, the best jitter performance and frequency stability will be achieved after DPLL3 has locked.

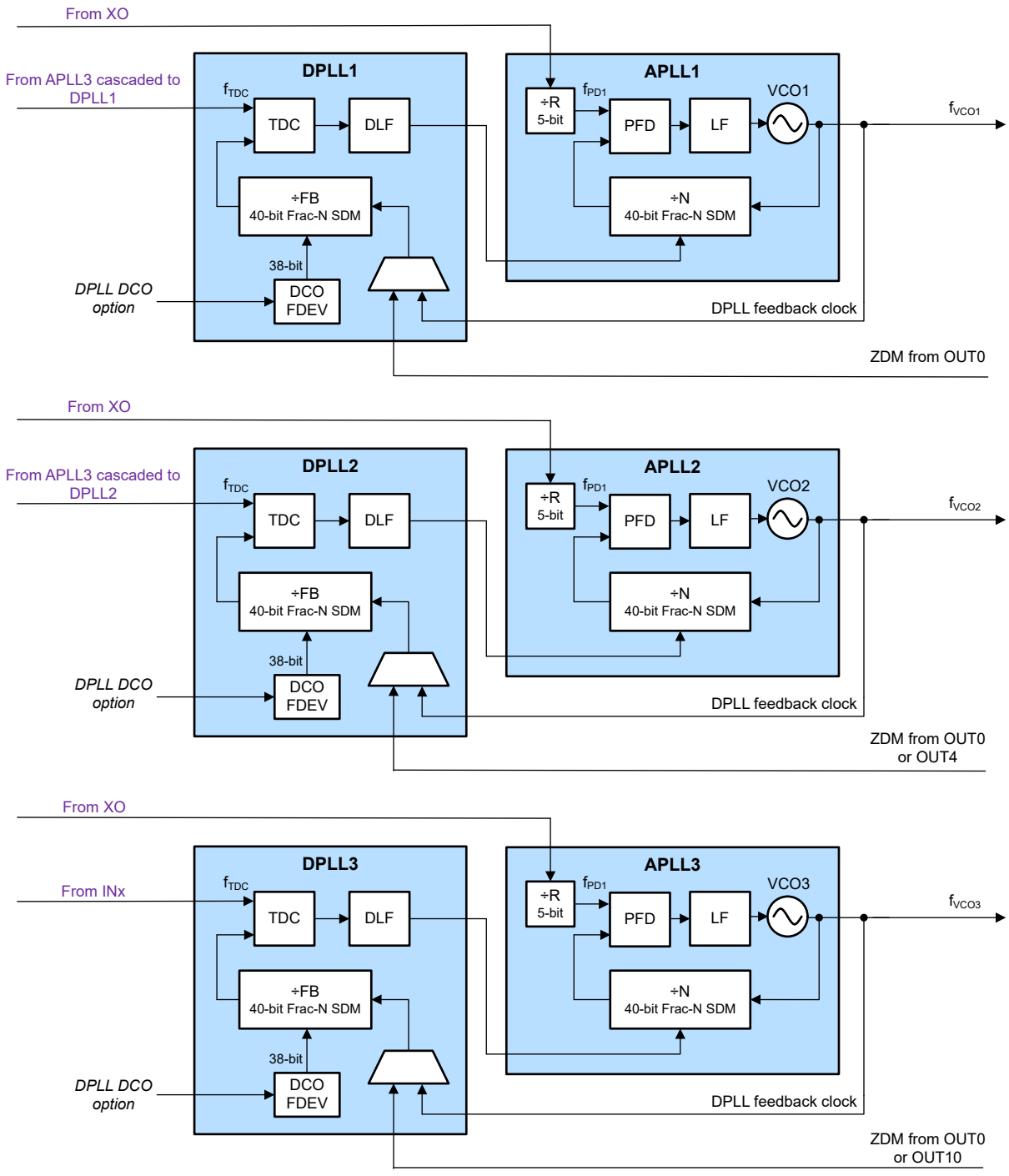


図 8-4. DPLL Cascaded Mode

8.2.2.3 APLL Cascaded With DPLL

Using the VCBO as a cascade source to APLL1 or APLL2 provides the APLL a high-frequency, ultra-low-jitter reference clock. This unique cascading feature can provide improved close in phase noise performance if the XO/TCXO/OCXO is a low frequency or has poor phase noise performance. Note that in cascaded DPLL operation the best jitter performance and frequency stability will be achieved after DPLL3 has locked.

DPLL3 lock status will impact DPLL1 and DPLL2 lock status. If APLL3 is in free-run mode or holdover mode, the VCBO frequency offset ppm value could introduce a similar frequency offset at APLL1 and APLL2 outputs even though DPLL1 and DPLL2 can stay in the locked state. In this configuration example, ensure DPLL3 and APLL3 are locked first, toggle PLL1 or PLL2 enable cycle (APLLx_EN bit = 0 → 1) to calibrate VCO1 or VCO2, and then double check PLL1 or PLL2 lock status.

In above example, APLL3 is upstream PLL, while APLL1 and APLL2 are downstream PLLs. If there are system start-up requirements on the clock sequencing, APLL1 or APLL2 also can be configured as the upstream PLL.

When cascading PLLs, the downstream APLL may use the DPLL or bypass and power down the DPLL depending on performance requirements. If DPLL1 and DPLL2 are disabled from above APLL cascaded mode, then DPLL3-only cascade mode may be used (see 図 8-6). In this case, VCO1 or VCO2 can track the VCO3 domain during DPLL3 lock acquisition and locked modes, allowing APLL1 or APLL2's clock domain to be synchronized to the DPLL3 reference input.

When a DPLL is disabled, it is recommended to use the 24-bit numerator and programmable 24-bit denominator instead of the fixed 40-bit denominator to eliminate frequency error from APLL reference to output.

Do not cascade one VCO output to both the DPLL reference and APLL reference of the same DPLL/APLL pair.

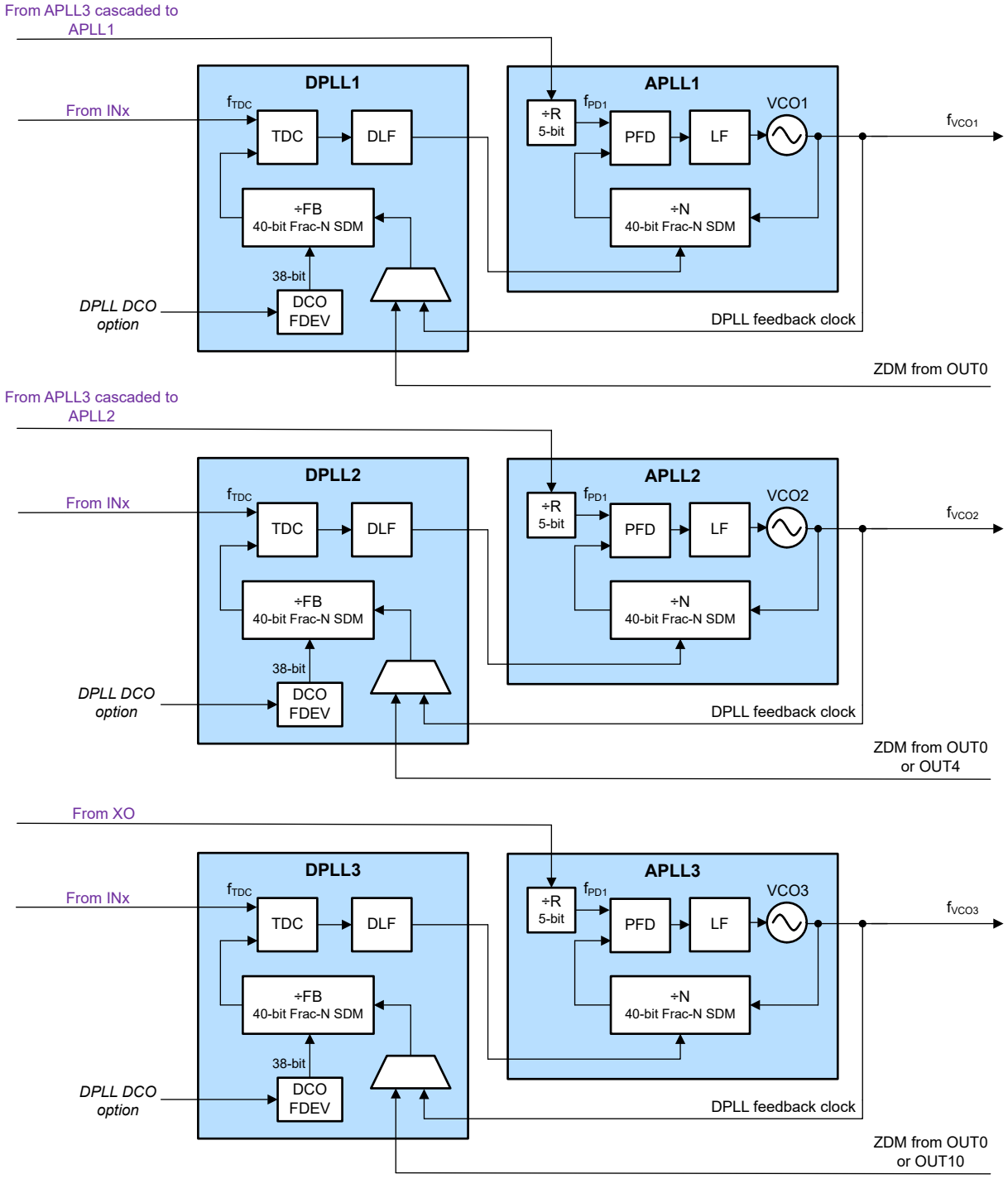


図 8-5. APLL Cascaded With DPLLs Enabled Example

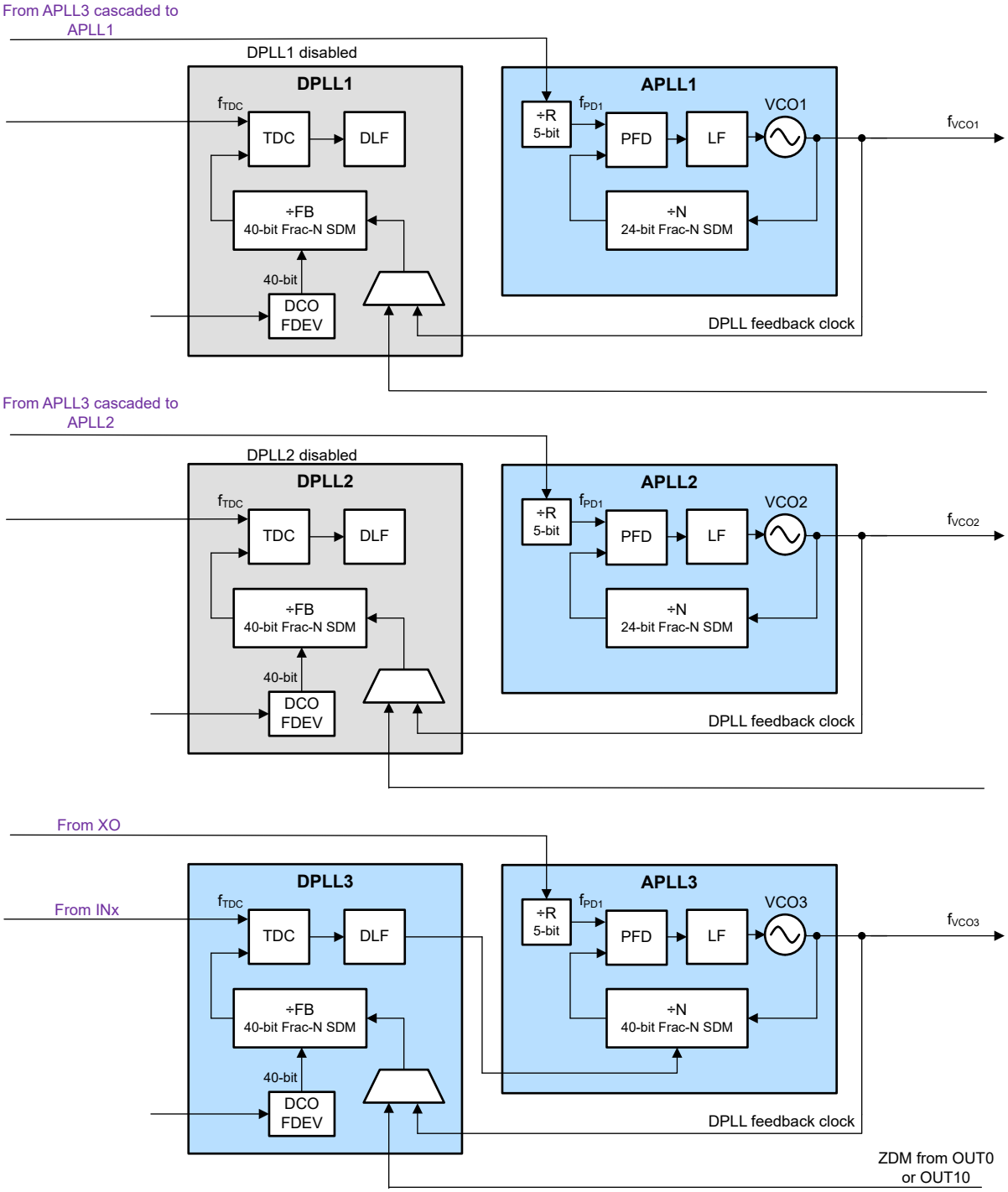


図 8-6. APLL Cascaded With DPLLs Disabled Example

8.2.3 APLL-Only Mode

In APLL-only mode, the external XO input source determines the free-run frequency stability and accuracy of the output clocks. The DPLL blocks are not used and do not affect the APLLs. APLLs still can operate in cascaded mode or non-cascaded mode and also have DCO option through control register writes.

The principle of operation for APLL-only mode after power-on reset and initialization is as follows. If APLL1 or APLL2 is in cascaded mode as shown in 図 8-6 (DPLL3 also is not used), VCO1 or VCO2 will track the VCO3 domain. APLLs lock in APLL priority order using bits: APLLx_STRT_PRTY. Cascading APLL1 or APLL2 from VCO3 provides a high-frequency, ultra-low-jitter reference clock to minimize the in-band phase noise/jitter degradation that could otherwise occur from a lower performance XO/TCXO/OCXO.

If APLL1 or APLL2 is not cascaded as shown in 図 8-7, VCO1 or VCO2 will lock to the XO input in APLLx_STRT_PRTY order after initialization and operate independent of the APLL3 domain.

When operating in APLL-Only mode without DPLL control, TI recommends selecting the programmable 24-bit denominator (PLLx_MODE = 0) instead of a fixed 40-bit denominator (PLLx_MODE = 1) to synthesize exact frequency ratios and maintain 0 ppm frequency error.

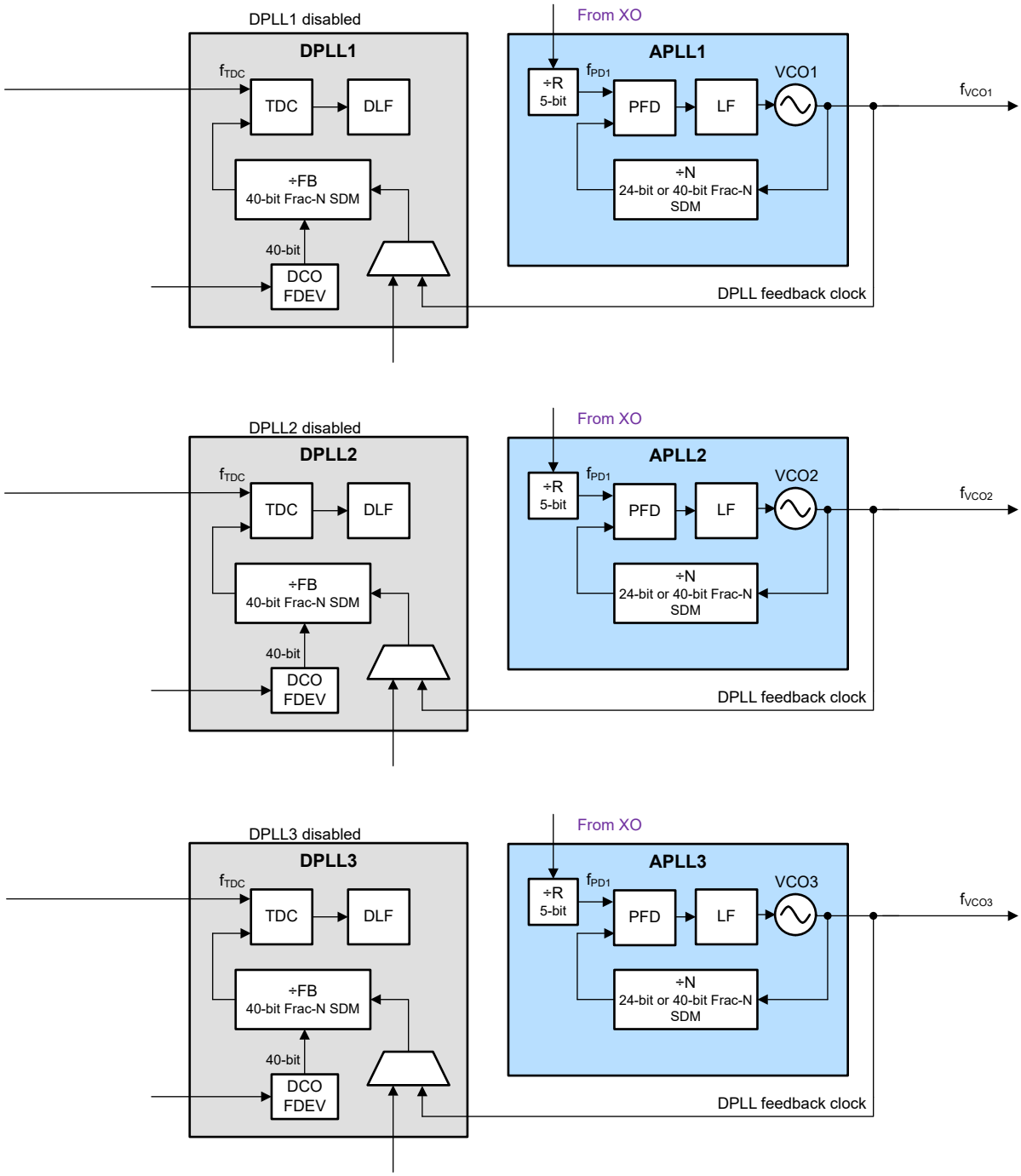


図 8-7. APLL-Only Independent Mode

8.3 Feature Description

8.3.1 Oscillator Input (XO)

The XO input is the reference clock for the fractional-N APLLs when the APLLs are not used in cascade mode. The XO input determines the output frequency accuracy and stability in free-run or holdover modes.

For proper DPLL operation, the XO frequency must have a **non-integer relationship** with the VCO frequency so the respective APLL N divider has a fractional divider ratio. For APLL-only mode, the XO frequency can have an integer or fractional relationship with the VCOs frequencies.

For applications requiring DPLL functionality, such as SyncE and PTP/IEEE-1588 for eCPRI, the XO input can be driven by a TCXO, OCXO, or external traceable clock that conforms to the frequency accuracy and holdover stability required by the applicable synchronization standard. TCXO and OCXO frequencies of 13, 14.4, 19.2, 19.44, 24, 25, 27, 38.88, 48, 49.152 and 54 MHz are commonly available and cost-effective options that allow the APLL3 to operate in fractional mode for a VCBO frequency of 2500 MHz.

An XO/TCXO/OCXO source with low frequency or high phase jitter/noise floor will have no impact on the APLL3 output jitter performance because the VCBO determines the jitter and phase noise over the 12-kHz to 20-MHz integration bandwidth. An XO doubler increasing the PFD frequency can be enabled for each APLL to further optimize close in phase noise performance.

The XO input buffer has programmable input on-chip termination and AC-coupled input biasing configurations as shown in 図 8-8. The buffered XO path also drives the input monitoring blocks.

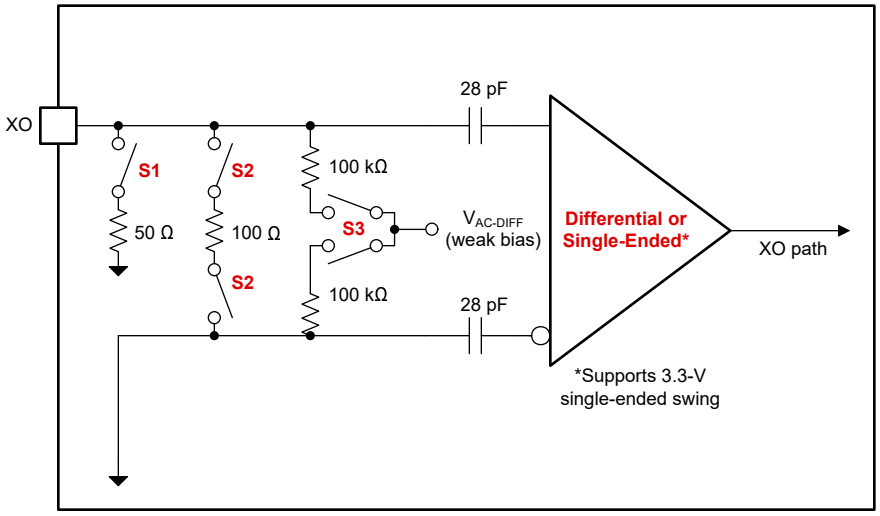


図 8-8. XO Input Buffer

表 8-1 lists the typical XO input buffer configurations for common clock interface types.

表 8-1. XO Input Buffer Modes

XO_TYPE	INPUT TYPES	INTERNAL SWITCH SETTINGS	
		INTERNAL TERM. (S1, S2)(1)	INTERNAL BIAS (S3)(2)
0x00	DC (external termination)	OFF	OFF
0x01	AC (external termination)	OFF	ON (1.3 V)
0x03	AC (internal 100-Ω to GND)	100 Ω	ON (1.3 V)
0x04	DC (internal 50-Ω to GND)	50 Ω	OFF
0x05	AC (internal 50-Ω to GND)	50 Ω	ON (1.3 V)
0x08	LVCMOS	OFF	OFF
0x0C	LVCMOS (internal 50-Ω to GND)	50 Ω	OFF

(1) S1, S2: OFF = External termination is assumed.
(2) S3: OFF = External input bias or DC coupling is assumed.

8.3.2 Reference Inputs

The reference inputs (IN0, IN1, IN2 and IN3) can accept differential or single-ended clocks. Each input has programmable input type, termination, and DC-coupled or AC-coupled input biasing configurations as shown in 図 8-9. Each input buffer drives the reference input mux of the DPLL block. The DPLL input mux can select from any of the reference inputs. The DPLL can switch between inputs with different frequencies provided they can be divided-down to a common frequency by DPLL R dividers. The reference input paths also drive the various detector blocks for reference input monitoring and validation. DC-path switch can bypass internal AC-coupling capacitors to make low frequency input work robustly.

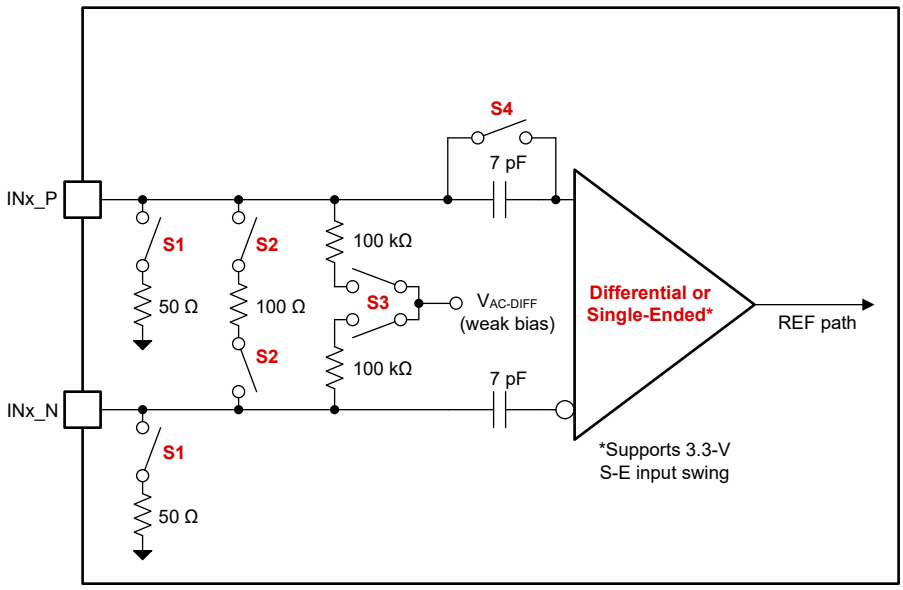


図 8-9. Reference Input Buffer

表 8-2 lists the reference input buffer configurations for common clock interface types.

表 8-2. Reference Input Buffer Modes

REFx_DC_COUPLED_EN, REFx_TYPE	INPUT TYPES	INTERNAL SWITCH SETTINGS			
		INTERNAL SINGLE-END TERM. (S1)(2)	INTERNAL DIFFERENTIAL TERM. (S2) (2)	INTERNAL BIAS (S3)(3)	LVCMOS/DIFF INTERNAL AC CAPACITOR BYPASS MODE (S4) (1)
0x00, 0x00	DC-Differential (external termination)	OFF	OFF	OFF	OFF
0x00, 0x01	AC-Differential (external termination)	OFF	OFF	ON (1.3 V)	OFF
0x00, 0x02	DC-Differential (internal termination)	OFF	100 Ω	OFF	OFF
0x00, 0x03	LVDS / HSDS, AC-Differential (internal termination)	OFF	100 Ω	ON (1.3 V)	OFF
0x00, 0x04	HCSL,DC-Differential (internal termination 50-Ω)	50 Ω	OFF	OFF	OFF
0x00, 0x05	LVPECL,AC-Differential (internal termination 50-Ω)	50 Ω	OFF	ON (1.3 V)	OFF
0x00, 0x08	LVCMOS(External DC-coupling, internal AC coupling)	OFF	OFF	OFF	OFF

表 8-2. Reference Input Buffer Modes (continued)

REFx_DC_COUPLED_EN, REFx_TYPE	INPUT TYPES	INTERNAL SWITCH SETTINGS			
		INTERNAL SINGLE-END TERM. (S1)(2)	INTERNAL DIFFERENTIAL TERM. (S2) (2)	INTERNAL BIAS (S3)(3)	LVCMOS/DIFF INTERNAL AC CAPACITOR BYPASS MODE (S4) (1)
0x01, 0x08	LVCMOS (External DC-coupling, internal DC coupling)	OFF	OFF	OFF	ON
0x01, 0x0C	LVCMOS(External DC-coupling, internal DC coupling, internal termination 50-Ω)	50 Ω	OFF	OFF	ON

(1) S4: OFF = Differential input amplitude detector is used for all input types except LVCMOS or single-ended.
(2) S1, S2: OFF = External termination is assumed.
(3) S3: OFF = External input bias or DC coupling is assumed.

8.3.3 Clock Input Interfacing and Termination

図 8-10 through 図 8-13 show the recommended input interfacing and termination circuits. Unused clock inputs can be left floating or pulled down.

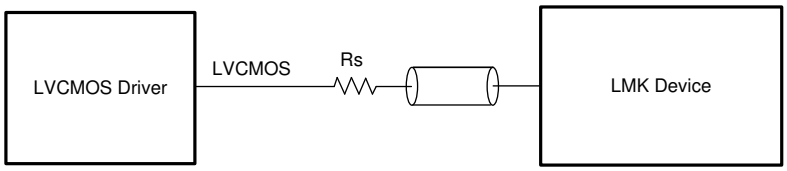


図 8-10. Single-Ended LVCMOS (1.8 V, 2.5 V, 3.3 V) to Reference (INx_P) or XO Input (XO)

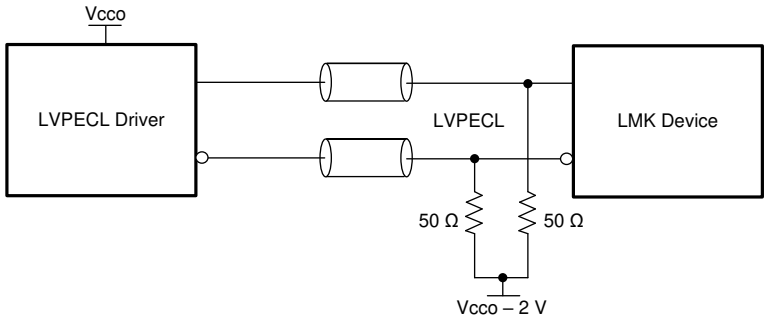


図 8-11. DC-Coupled LVPECL to Reference (INx)

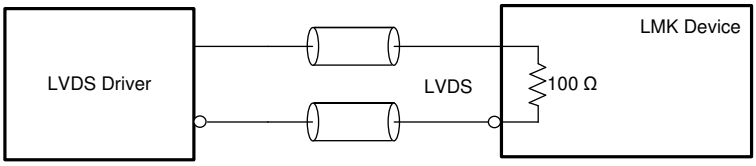


図 8-12. DC-Coupled HSDS/LVDS to Reference (INx)

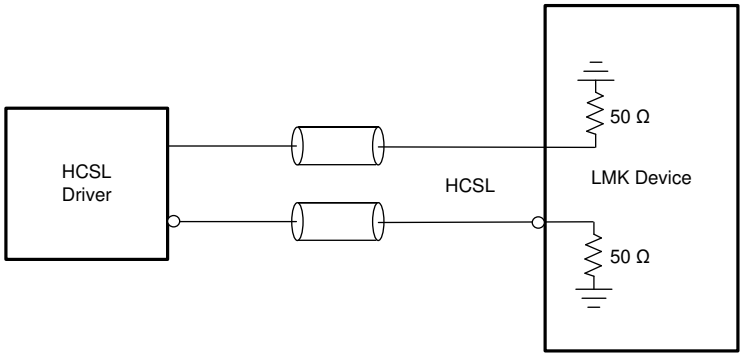


図 8-13. HCSL (Load Terminated) to Reference (INx)

8.3.4 Reference Input Mux Selection

8.3.4.1 Automatic Input Selection

There are two automatic input selection modes that can be set by register: Auto Revertive and Auto Non-Revertive.

- *Auto Revertive:* In this mode, the DPLL automatically selects the valid input with the highest configured priority. If a clock with higher priority becomes valid, the DPLL will automatically switch over to that clock immediately.
- *Auto Non-Revertive:* In this mode, the DPLL automatically selects the highest priority input that is valid. If a higher priority input because valid, the DPLL will not switch over until the currently selected input becomes invalid.

8.3.4.2 Manual Input Selection

There are two manual input selection modes that can be set by a register: Manual with Auto-Fallback and Manual with Auto-Holdover. In either manual mode, the input selection can be done through register control (Register DPLLx_MAN_REF_SEL) or hardware pin control (GPIOs).

- *Manual with Auto-Fallback:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically fallback to the highest priority input that is valid or qualified. If no prioritized inputs are valid, the DPLL will enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.
- *Manual with Auto-Holdover:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.

The reference input selection flowchart is shown in 図 8-14.

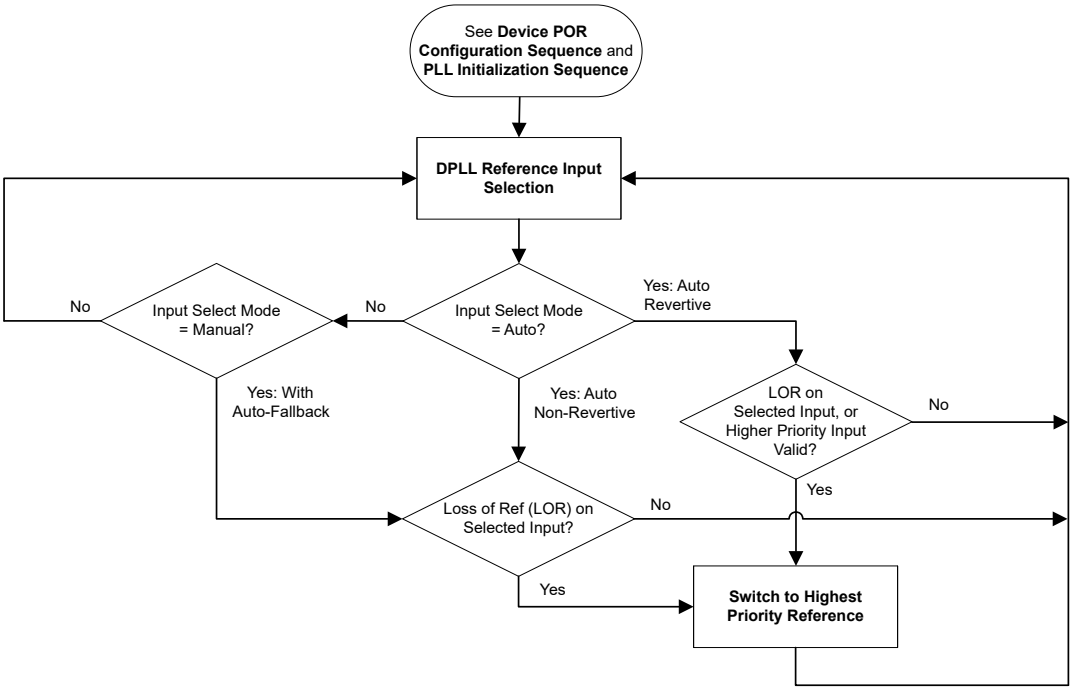


図 8-14. DPLL Reference Input Selection Flowchart

Also see 図 8-36, 図 8-37, and 図 8-38.

8.3.5 Hitless Switching

The DPLL supports hitless switching through TI's proprietary phase cancellation scheme or phase slew control scheme. When hitless switching is disabled, a phase hit equal to the phase offset between the two inputs will be propagated to the output at a rate determined by the filtering of the DPLL bandwidth.

8.3.5.1 Hitless Switching With Phase Cancellation

Typically phase cancellation will be enabled during hitless switching to prevent a phase transient (phase hit) from immediately propagating to the outputs when switching between two frequency-locked reference inputs with a fixed phase offset. The phase cancellation persists indefinitely in the use case scenario when phase slew is not enabled commonly referred to as phase buildout. The inputs are frequency-locked when they have same exact frequency (0-ppm offset), or have frequencies that are integer-related and can each be divided to a common frequency by integers. The hitless switching specifications ($t_{HITLESS}$ and $f_{HITLESS}$) are valid for reference inputs with no wander. In the case where two inputs are switched but are not frequency-locked, the output smoothly transitions to the new frequency with reduced transient.

8.3.5.2 Hitless Switching With Phase Slew Control

Enabling Phase Slew Control will constrain the output phase transient or phase hit during hitless switching and holdover exit. Users can select DPLLx_PHS1_EN to enable Phase Slew Control to follow the step limits set in DPLLx_PHS1_THRESH and DPLLx_PHS1_TIMER. When during hitless switching it is desired to transition slowly to tracking the new input phase, enabling phase slew control will remove the phase cancellation or phase build out based on the programmed timer value and step limits. Similarly when the DPLL switches from APLL-only mode or holdover mode to DPLL Lock Acquisition mode, or hitless switching with two inputs are not frequency-locked the phase slew limits would then be applied. When both Phase Cancellation function and Phase Slew Control function are disabled, a phase hit equal to the phase offset between XO and selected input or between the two inputs at the moment of switching will be propagated to the output at a rate determined by the DPLL loop bandwidth. In the case where two inputs are switched but are not frequency-locked Phase Slew Control function can ensure the output smoothly transitions to the new frequency as the rate the defined by the step limits.

8.3.5.3 Hitless Switching With 1-PPS Inputs

Hitless switching between 1-PPS inputs is supported when zero-delay mode (ZDM) synchronization is disabled, but the switchover event should only occur after the DPLL has acquired lock. If a switchover occurs before the DPLL has locked initially, the switchover will not be hitless and the DPLL will take an indeterminate amount of time to lock. In this case, a soft-reset should be issued for the DPLL to lock to the selected input. In an application, the system host can monitor the DPLL lock status through a STATUS pin or bit to determine when the DPLL has locked before allowing a switchover between 1-PPS inputs. The DPLL lock time is governed by the DPLL bandwidth (typically 10 mHz for a 1-PPS input).

Hitless switching between 1-PPS inputs is not supported when ZDM synchronization is enabled.

8.3.6 Gapped Clock Support on Reference Inputs

The DPLL supports locking to an input clock that has missing periods and is referred to as a gapped clock. Gapping severely increases the jitter of a clock, so the DPLL provides the high input jitter tolerance and low loop bandwidth necessary to generate a low-jitter periodic output clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. The gapped clock width cannot be longer than the reference clock period after the R divider (R_{INx} / f_{INx}). The reference input monitors should be configured to avoid any flags due to the worst-case clock gapping scenario to achieve and maintain lock. Reference switchover between two gapped clock inputs may violate the hitless switching specification if the switch occurs during a gap in either input clock.

8.3.7 Input Clock and PLL Monitoring, Status, and Interrupts

The following section describes the input clock and PLL monitoring, status, and interrupt features. The reference input frequency detector and phase valid detector can not be used at the same time on a single input.

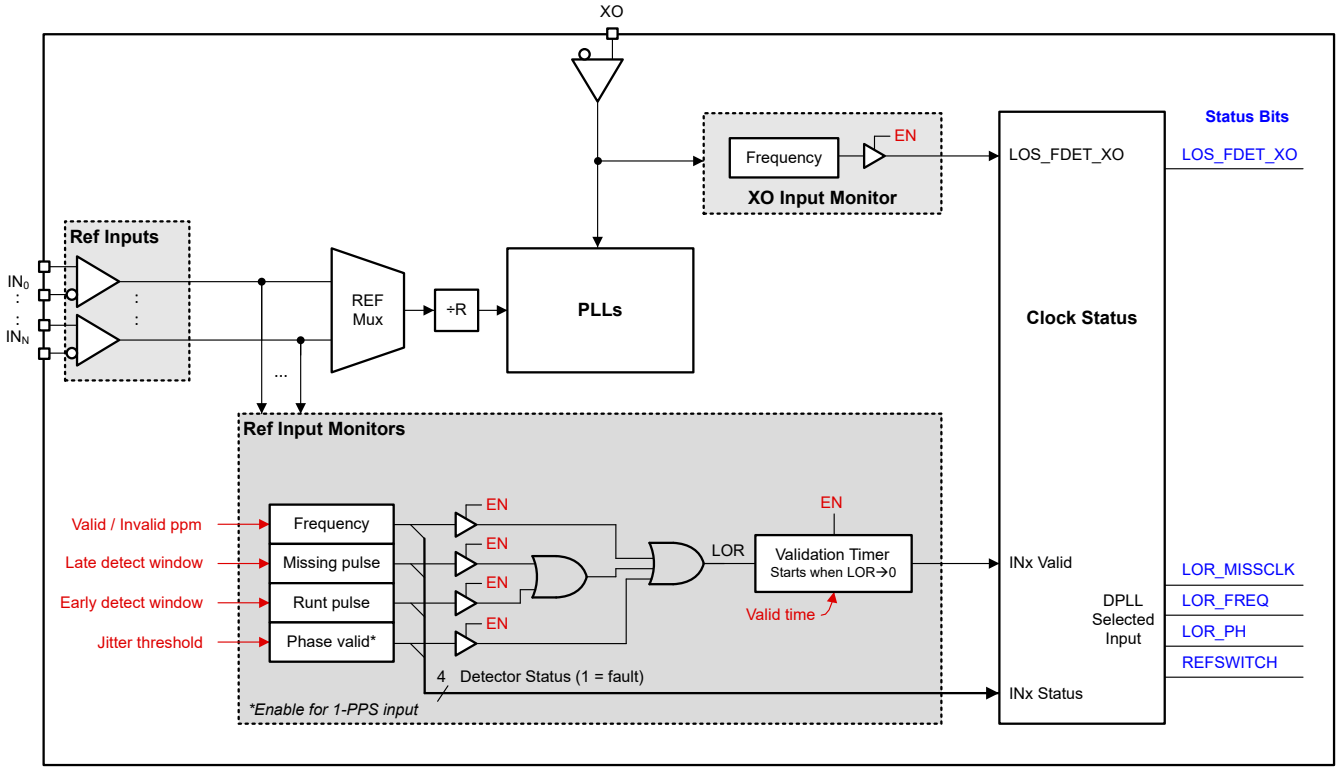


図 8-15. Clock Monitors for Reference and XO Inputs

8.3.7.1 XO Input Monitoring

The XO input has a coarse frequency monitor to help qualify the input before it is used to lock the APLLs.

The XO frequency detector clears the LOS_FDET_XO flag when the input frequency is detected within the range of 9 MHz to 160 MHz to cover the supported XO input frequency range. The XO frequency monitor uses a RC-based detector and therefore cannot precisely determine whether XO input clock has sufficient frequency stability. A stable XO input will ensure successful VCO calibration of APLL2 or APLL1 during the PLL start-up. When the external XO clock has a slow or delayed start-up behavior TI recommends to force a calibration on APLL2 and APLL1 once the XO input is stable. See *Slow or Delayed XO Start-Up* for more information.

The XO frequency detector can be bypassed by setting the XO_FDET_BYP bit (shown as $\overline{\text{EN}}$ in 図 8-15) so that the XO input is always considered valid by the PLL control state machine. The user can observe the LOS_FDET_XO status flag through the status pins and status bit. Setting XO_FDET_BYP bit will bypass the detect, but will not reflect any change to LOS_FDET_XO status flag.

8.3.7.2 Reference Input Monitoring

Each DPLL reference clock input is independently monitored for input validation before the clock is qualified and available for selection by the DPLL. The reference monitoring blocks include frequency, missing pulse, and runt pulse monitors. For a 1-PPS input, the phase valid monitor is supported, while the frequency, missing pulse, and runt pulse monitors are not supported and must be disabled. A validation timer sets the minimum time for all enabled reference monitors to be clear of flags before an input is qualified.

The enablement and valid threshold for all reference monitors and validation timers are programmable per input. The reference monitors and validation timers are optional to enable, but are critical to achieve reliable DPLL lock and optimal transient performance during holdover or switchover events, and are also used to avoid selection of an unreliable or intermittent clock input. If a given detector is not enabled, it will not set a flag and will be ignored. The status flag of any enabled detector can be observed through the status pins for any reference input (selected or not selected). The status flags of the enabled detectors can also be read through the status bits for the selected input of the DPLL.

8.3.7.2.1 Reference Validation Timer

The validation timer sets the amount of time required for each reference to be clear of flags from all enabled input monitors before the reference is qualified and valid for selection. The validation timer and enable settings are programmable.

8.3.7.2.2 Frequency Monitoring

The precision frequency detector measures the frequency offset or error (in ppm) of all input clocks relative to the XO input's frequency, which is considered as the 0-ppm reference clock for frequency comparison. The valid and invalid ppm frequency thresholds are configurable through the registers. The monitor will clear the REFx_FDET_STATUS flag when the relative input frequency error is less than the valid ppm threshold. Otherwise, the monitor will set the REFx_FDET_STATUS flag when the relative input frequency error is greater than the invalid ppm threshold. The ppm delta between the valid and invalid thresholds provides hysteresis to prevent the REFx_FDET_STATUS flag from toggling when the input frequency offset is crossing these thresholds.

A measurement accuracy (ppm) and averaging factor are used in computing the frequency detector register settings. A higher measurement accuracy (smaller ppm) or higher averaging factor will increase the measurement delay to set or clear the flag, which allows more time for the input frequency to settle, and can also provide better measurement resolution for an input with high drift or wander. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

8.3.7.2.3 Missing Pulse Monitor (Late Detect)

The missing pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period plus a programmable late window threshold (T_{LATE}). When an input pulse arrives before T_{LATE}, the pulse is considered valid and the missing pulse flag will be cleared if set. When an input pulse does not arrive before T_{LATE} (due to a missing or late pulse), the missing pulse flag is set to disqualify the input.

Typically, T_{LATE} should be set higher than the input's longest clock period (including cycle-to-cycle jitter), or higher than the gap width for a gapped clock. The missing pulse monitor can act as a coarse frequency detector

with faster detection than the ppm frequency detector. The missing pulse monitor is supported for input frequencies between 2 kHz and f_{VCO}/12 and should be disabled when outside this range.

The missing pulse and runt pulse monitors operate from the same window detector block for each reference input. The status flags for both these monitors are combined by logic-OR gate and can be observed through status pin. The window detector flag for a reference can also be observed through the corresponding REFx_MISSCLK_STATUS bit.

8.3.7.2.4 Runt Pulse Monitor (Early Detect)

The runt pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period minus a programmable early window threshold (T_{EARLY}). When an input pulse arrives after T_{EARLY}, the pulse is considered valid and the runt pulse flag will be cleared. When an early or runt input pulse arrives before T_{EARLY}, the monitor will set the flag immediately to disqualify the input.

Typically, T_{EARLY} should be set lower than the input's shortest clock period (including cycle-to-cycle jitter). The early pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The early pulse monitor is supported for input frequencies between 2 kHz and f_{VCO}/12 and should be disabled when outside of this range.

Users must enable missing clock detect in order to use early clock detect. Early clock detect cannot be enabled alone.

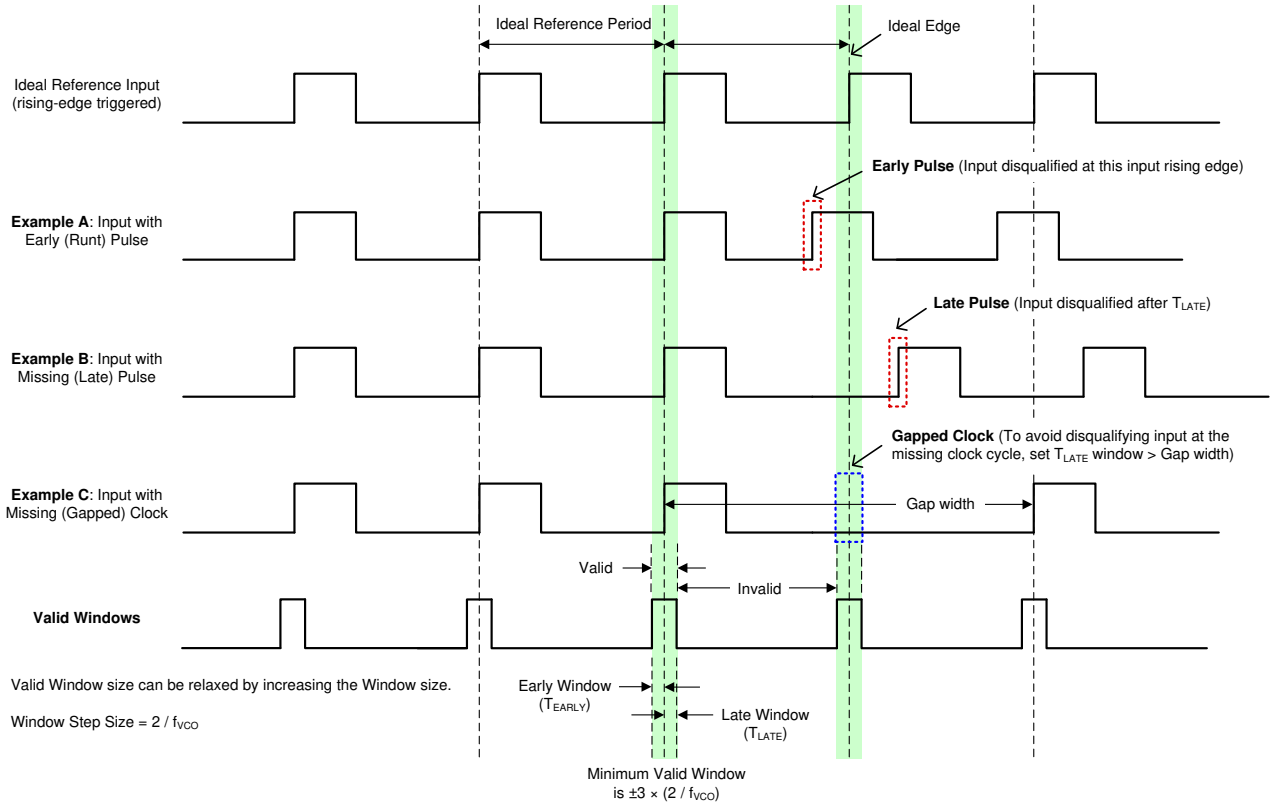


図 8-16. Early and Late Window Detector Examples

8.3.7.2.5 Phase Valid Monitor for 1-PPS Inputs

The phase valid monitor is designed specifically for 1-PPS input validation because the frequency and window detectors do not support this low frequency. The phase valid monitor uses a window detector to validate 1-PPS input pulses that arrive within the nominal clock period (T_{IN}) plus a programmable jitter threshold (T_{JIT}). When the input pulse arrives within the counter window (T_V), the pulse is considered valid and the phase valid flag is

cleared. When the input pulse does not arrive before T_V (due to a missing or late pulse), the flag is set immediately to disqualify the input. T_{JIT} should be set higher than the worst-case input cycle-to-cycle jitter.

The phase valid register settings also are valid for 1-PPS ppm error threshold detect. Notice the T_{JIT} also impacts the worst case ppm error allowed. For example: High_Jitter_Freq = 1/(T_{IN} - T_{JIT}), then Max input allowable ppm error = (High_Jitter_Freq - Expected_Freq) / Expected_Freq × 1e6.

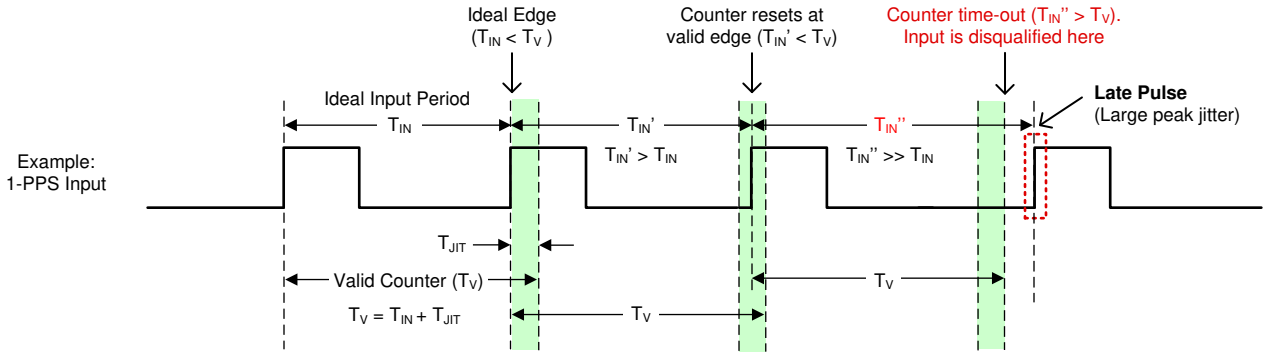


図 8-17. 1-PPS Input Window Detector Example

8.3.7.3 PLL Lock Detectors

The loss-of-lock (LOL) status is available for APLL1, APLL2, APLL3, DPLL1, DPLL2, and DPLL3. The APLLs are monitored for loss-of-frequency lock only. The DPLL can be monitored for both loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL). The DPLL lock threshold and loss-of-lock threshold are programmable for both LOPL and LOFL detectors. In the case when APLL3 loss-of-frequency lock is selected, then DPLL3 is monitored for LOPL only. DPLL3 must be enabled for the digital monitoring of APLL3 VCBO lock detect.

The DPLL frequency lock detector will clear its LOFL flag when the DPLL's frequency error relative to the selected reference input is less than the lock ppm threshold. Otherwise, the lock detector will set the LOFL flag when the DPLL's frequency error is greater than the unlock ppm threshold. The ppm delta between the lock and unlock thresholds provides hysteresis to prevent the LOFL flag from toggling when the DPLL frequency error is crossing these thresholds.

The APLL3 frequency digital lock detector will clear its LOFL flag when the APLL3 VCBO frequency error relative to the XO reference input is less than the lock ppm threshold. Otherwise, the lock detector will set the LOFL flag when the VCBO's frequency error is greater than the unlock ppm threshold. Ensure to take the ppm frequency tolerance of the XO input reference into account when setting the VCBO frequency lock and unlock thresholds. The ppm delta between the lock and unlock thresholds provides hysteresis to prevent the LOFL flag from toggling when the VCBO frequency error is crossing these thresholds.

A measurement accuracy (ppm) and averaging factor are used in computing the frequency lock detector register settings. A higher measurement accuracy (smaller ppm) or higher averaging factor will increase the measurement delay to set or clear the LOFL flag. Higher averaging may be useful when locking to an input with high wander or when the PLL is configured with a narrow loop bandwidth. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

The DPLL phase lock detector will clear its LOPL flag when the phase error of the DPLL is less than the phase lock threshold. Otherwise, the lock detector will set the LOPL flag when the phase error is greater than the phase unlock threshold.

Users can observe the APLL and DPLL lock detector flags through the status pins and the status bits.

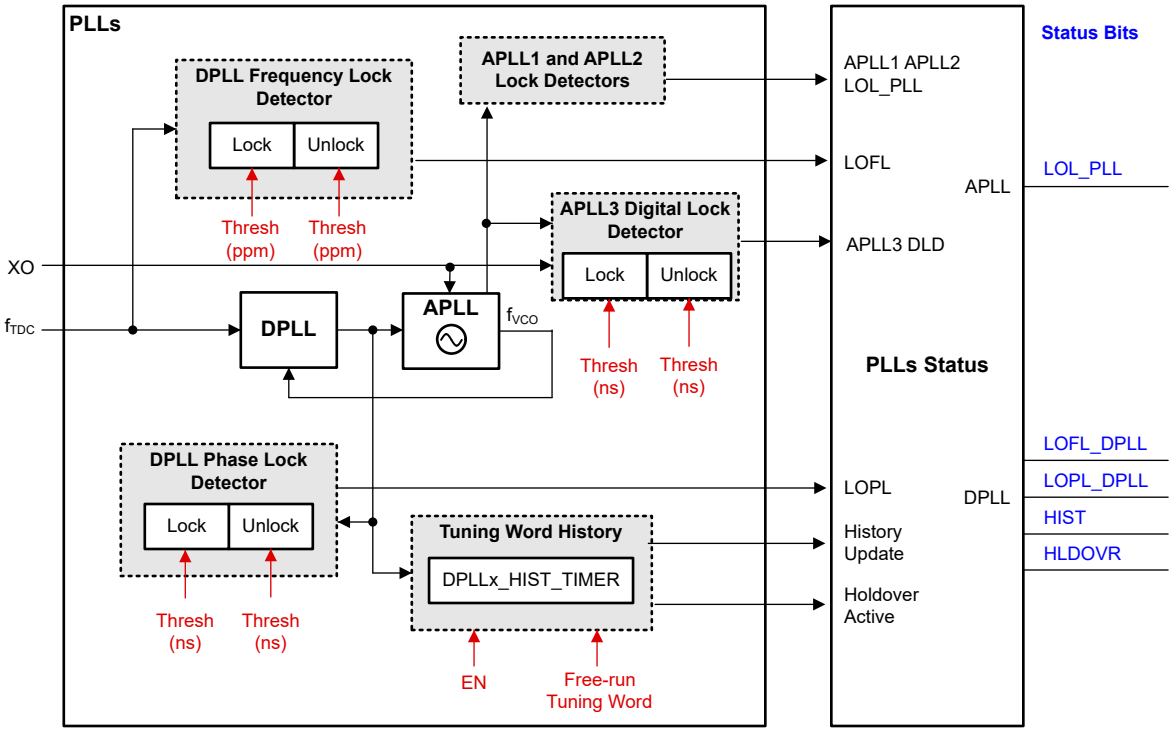


図 8-18. PLL Lock Detectors and History Monitor

8.3.7.4 Tuning Word History

The DPLL domain has a tuning word history monitor block that determines the initial output frequency accuracy upon entry into holdover. When in holdover, the stability of the reference clock (on XO input) determines the long-term stability and accuracy of the output frequency. The tuning word can be updated from one of three sources depending on the DPLL operating mode:

1. Locked Mode: from the output of the digital loop filter when locked
2. Holdover Mode: from the final output of the history monitor
3. Free Run Mode: from the free-run tuning word register (user defined)

When the history monitor is enabled and the DPLL is locked, the device averages the reference input frequency by accumulating history from the digital loop filter output during a programmable averaging time (T_{AVG}) set by DPLLx_HIST_TIMER. When a valid reference input becomes invalid, the final tuning word value is stored to determine the initial holdover frequency accuracy. Generally, a longer T_{AVG} time will produce a more accurate initial holdover frequency.

If the input reference clock fails and becomes invalid, the history data can be corrupted if the tuning word continues to update before the fail state is indicated by one of the reference input validation monitors. To avoid this scenario, any in progress accumulation is ignored and the recent history data is ignored. The most recent collected average data is discarded such that the actual history used is greater than T_{AVG} but less than 2 × T_{AVG}.

The tuning word history is initially cleared after a device hard reset or soft reset. After the DPLL locks to a new reference, the history monitor waits for the first T_{AVG} timer to expire before storing the first tuning word value and begins to accumulate history. The history monitor will not clear the previous history value during reference switchover or holdover exit. The history can be manually cleared or reset by toggling the history enable bit (DPLLx_HIST_EN = 1 → 0 → 1), if needed.

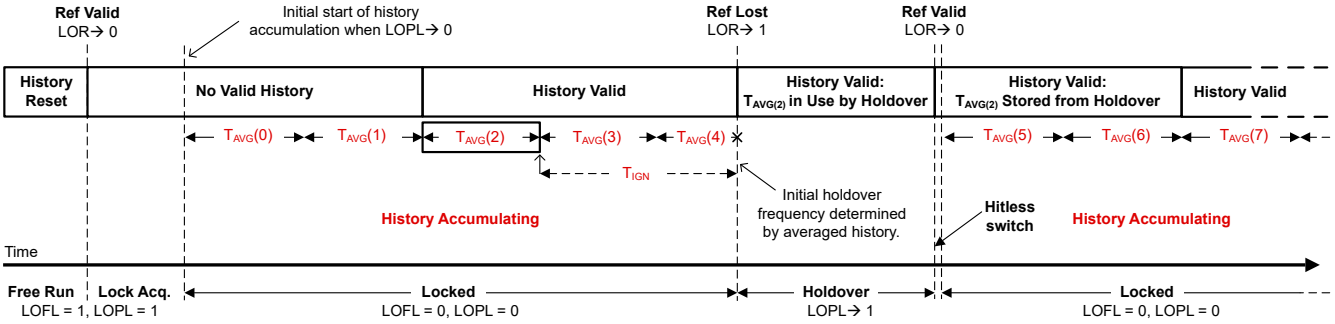


図 8-19. Tuning Word History Windows

When no tuning word history exists, the free-run tuning word value (DPLLx_FREE_RUN) is used and determines the initial holdover output frequency accuracy.

8.3.7.5 Status Outputs

The GPIO pins can be configured to output various status signals and interrupt flags for device diagnostic and debug purposes. The status signal, output driver type, and output polarity settings are programmable.

8.3.7.6 Interrupt

Any GPIO pin can be configured as a device interrupt output pin. The interrupt logic configuration is set through registers. When the interrupt logic is enabled, the interrupt output can be triggered from any combination of interrupt status indicators, including LOS for the XO, LOR for the selected DPLL input, LOL for APLL1, APLL2, and the DPLLs, and holdover and switchover events for the DPLLs. When the interrupt polarity is set high, a rising edge on the live status bit asserts its interrupt flag (sticky bit). Otherwise, when the polarity is set low, a falling edge on the live status bit asserts its interrupt flag. Any individual interrupt flag can be masked so the flag does not trigger the interrupt output. The unmasked interrupt flags are combined by the AND/OR gate to generate the interrupt output, which can be selected on either status pin.

When a system host detects an interrupt from the device, the host can read the interrupt flag or *sticky* registers to identify which bits were asserted to resolve the fault conditions in the system. After the system faults have been resolved, the host can clear the interrupt output by writing 1 to the self-clearing INT_CLR field.

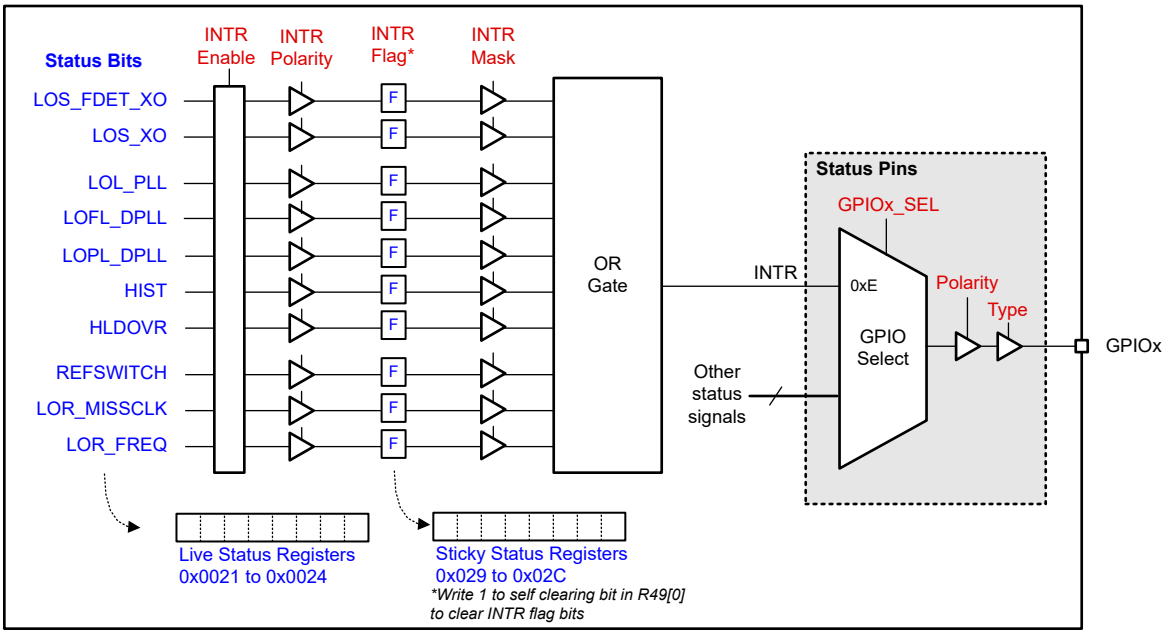


図 8-20. Status and Interrupt

8.3.8 PLL Relationships

When a DPLL combines with an APLL in a feedback loop, the APLL must use the fixed 40-bit denominator. When the APLL works in an independent loop, like APLL1 and APLL3 in 図 8-6 or APLLs in 図 8-7, TI recommends selecting the 24-bit programmable denominator.

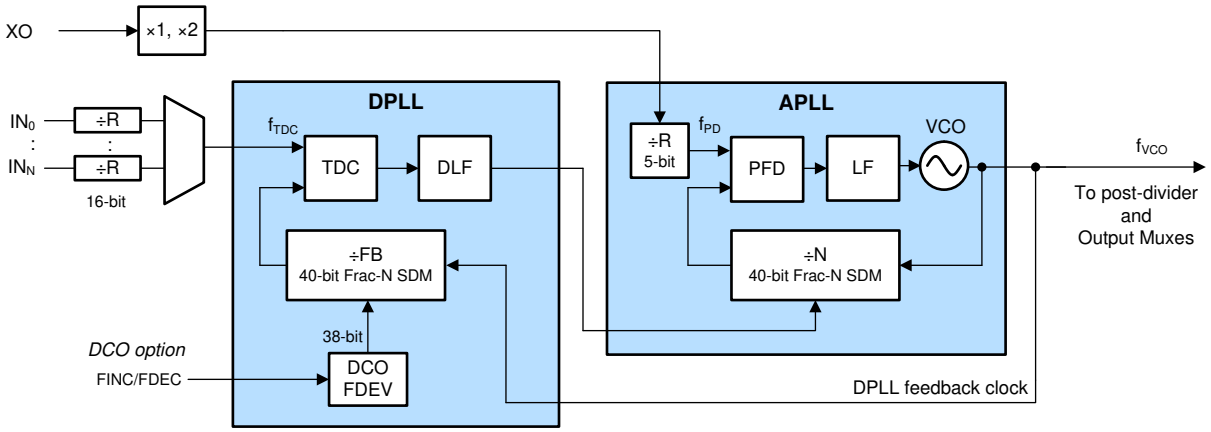


図 8-21. PLL Architecture

8.3.8.1 PLL Frequency Relationships

The following equations provide the APLL and DLL frequency relationships required to achieve closed-loop operation. The TICS Pro programming software can be used to generate valid divider settings based on the desired frequency plan.

Note that any divider in the following equations refers to the actual divide value (or range) and not its programmable register value.

When DPLL operation is enabled, the calculated DPLL frequency and APLL frequency must be nominally the same. The DPLL adjustments to the paired APLL N divider 40-bit fixed denominator will track the selected input reference source to synthesize the actual clock output desired frequency and phase.

When the APLL operates independently from its paired DPLL, TI recommends the programmable 24-bit denominator for hybrid synchronization or cascading between frequency domains in order to maintain 0 ppm frequency error without DPLL control. In this scenario the APLL will which track the cascade feedback divider reference from another APLL output.

When using ZDM (zero delay mode) for a PLL, the clock output divider must be accounted for in the VCO frequency calculations.

8.3.8.1.1 APLL Phase Detector Frequency

式 1 calculates the phase detector frequency which is used to find the VCO frequency in the APLL VCO Frequency calculation in 式 2.

$$f_{PD} = f_{XO} \times D_{XO} / R_{XO} \quad (1)$$

where

- f_{PD} = APLL phase detector frequency
- f_{XO}: APLL reference is XO frequency or cascaded reference frequency from another APLL.
- D_{XO}: XO input doubler (1 = disabled, 2 = enabled)
- R_{XO}: APLL XO Input R divider value (1 to 32)

8.3.8.1.2 APLL VCO Frequency

The APLL phase locks the APLL VCO to the APLL reference using the applied APLL numerator. Use 式 2 to calculate the VCO frequency.

$$f_{VCO} = f_{PD} \times (INT_{APLL} + NUM_{APLL} / DEN_{APLL}) \quad (2)$$

- f_{VCO}: VCO frequency
- f_{PD} = APLL phase detector frequency
- INT_{APLL}: APLL N divider integer value (12 bits, 1 to $2^{12} – 1$)
- NUM_{APLL}: APLL N divider numerator value (40 bits, 0 to $2^{40} – 1$, or 24 bits, 0 to $2^{24} – 1$)
- DEN_{APLL}: APLL N divider denominator value (fixed 2^{40}, or programmable 1 to 2^{24})
  - Avoid integer boundary spurs by keeping the NUM/DEN ratio away from an integer value.
  - $0.125 < NUM_{APLL} / DEN_{APLL} < 0.875$ (In DPLL Mode, avoid 0.5)

8.3.8.1.3 DPLL TDC Frequency

式 3 calculates the TDC frequency which is used to find the VCO frequency in the DPLL VCO Frequency calculation in 式 5. Two different TDC frequencies are possible for each DPLL to enable switching between non-integer related frequencies while keeping the TDC rate high.

$$f_{TDC} = f_{INx} \times D_{INx} / R_{INx} \quad (3)$$

$$f_{TDC} = f_{INy} \times D_{INy} / R_{INy} \quad (4)$$

where

- f_{TDC}: DPLL TDC input frequency (see 式 3)
- f_{INx} or f_{INy}: INx or INy input frequency or cascaded reference frequency from another APLL.
- R_{INx} or R_{INy}: INx or INy R divider value (16 bits, 1 to $2^{16} – 1$)
- D_{INx} or D_{INy}: INx or INy input doubler (2 = disabled and 1 = enabled)

8.3.8.1.4 DPLL VCO Frequency

The DPLL phase locks the APLL VCO to the DPLL VCO frequency by updating the actual APLL numerator value. Use 式 5 to calculate the VCO frequency. Each DPLL can have two different values for DPLL N to allow locking to the same VCO frequency using two different TDC frequencies. DPLLx_REF#_FB_SEL register selects which DPLL N value is used.

$$f_{VCO} = f_{TDC} \times (INT_{DPLL} + NUM_{DPLL} / DEN_{DPLL}) \quad (5)$$

where

- INT_{DPLL}: DPLL FB divider integer value (33 bits, 1 to $2^{33} – 1$)
- NUM_{DPLL}: DPLL FB divider numerator value (40 bits, 0 to $2^{40} – 1$)
- DEN_{DPLL}: DPLL FB divider denominator value (40 bits, 1 to 2^{40})
- N: $INT_{DPLL} + NUM_{DPLL} / DEN_{DPLL}$

8.3.8.1.5 Clock Output Frequency

Each APLL has a post divider which will provide a VCO post divider frequency calculated in 式 6, 式 7, or 式 8. The final output frequency is calculated by dividing from the VCO post divider frequency and the output divide (see 式 9). For each output, the output frequency depends on the selected APLL clock source and output divider value.

APLL1 selected: $f_{POST\_DIV} = f_{VCO1} / Pn_{APLL1}$ (6)

APLL2 selected: $f_{POST\_DIV} = f_{VCO2} / P1_{APLL2}$ (7)

APLL3 selected: $f_{POST\_DIV} = f_{VCO3} / P1_{APLL3}$ (8)

OUT[0:15]: $f_{OUTx} = f_{POST\_DIV} / OD_{OUTx}$ (9)

where

- f_{POST_DIV}: Output mux source frequency (APLL1, APLL2 or APLL3 post-divider clock)
- Pn_{APLL1}: APLL1 primary P1 or secondary P2 post-divide value (2 to 7)
- $P1_{APLL2}$: APLL2 primary P1 post-divide value (2 to 13)
- $P1_{APLL3}$: APLL3 post-divide value = div8 (2 to 8) , div8 times 2 (10, 12, 14, 16) , or bypass (1)
- f_{OUTx}: Output clock frequency (x = 0 to 15)
- OD_{OUTx}: OUTx output bypass or divider value. All outputs have a 12-bit divider with values 1 to ($2^{12} – 1$). All outputs except OUT2 and OUT3 have the option to follow the 12-bit divider with a 20-bit SYSREF divider that can be used to produce 1-PPS or other frequencies below 1 Hz when the SYSREF output is set for continuous output.

8.3.8.2 Analog PLLs (APLL1, APLL2, APLL3)

Each APLL has a 40-bit fractional-N divider to support high-resolution frequency synthesis and very low phase noise and jitter. Each APLL also has the ability to tune its VCO frequency through sigma-delta modulator (SDM) control in DPLL mode. In cascaded mode, each APLL has the ability to lock its VCO frequency to another VCO frequency.

In free-run mode, APLL3 uses the XO input as an initial reference clock to its VCO3. The PFD of APLL3 compares the fractional-N divided clock with its reference clock and generates a control signal. The control signal is filtered by the APLL3 loop filter to generate a control voltage to set VCO3's output frequency. The SDM modulates the N divider ratio to get the desired fractional ratio between the PFD input and the VCO3 output. APLL1 or APLL2 operates similar to APLL3. User can select the reference from either the VCO3 clock or XO clock.

In DPLL mode, the APLL fractional SDM is controlled by the DPLL loop to pull the VCO frequency into lock with the DPLL reference input. For example, 図 8-6 shows how the APLL1 or APLL2 can derive their references from the VCO3 if their respective DPLL1 or DPLL2 are disabled. The VCO1 or VCO2 will then be effectively locked to the DPLL3 reference input, assuming there is no synthesis error introduced by the fractional N divide ratio of APLL1 or APLL2.

8.3.8.3 APLL Reference Paths

8.3.8.3.1 APLL XO Doubler

The APLL XO doubler can be enabled to double the PFD frequency for the APLL reference. Enabling the XO doubler adds minimal noise and can be useful to increase the PFD frequency to optimize phase noise, jitter, and fractional spurs. The flat portion of the APLL phase noise can improve when the PFD frequency is increased.

8.3.8.3.2 APLL XO Reference (R) Divider

Each APLL has a 5-b XO reference (R) divider that can be used to meet the maximum APLL PFD frequency specification. It can also be used to ensure the APLL fractional-N divide ratio (NUM/DEN) is between 0.125 to 0.875 (avoid 0.5), which is recommended to support the DPLL frequency tuning range. Otherwise, the R divider can be bypassed (divide by 1).

8.3.8.4 APLL Phase Frequency Detector (PFD) and Charge Pump

APLL1 has programmable charge pump settings of 1.6, 3.2, 4.8, or 6.4 mA. APLL2 or APLL3 has programmable charge pump settings from 0 to 5.8 mA in 0.4-mA steps. Best performance from APLL3 is achieved with a charge pump currents of 0.8 mA or higher.

8.3.8.5 APLL Feedback Divider Paths

The VCO output of each APLL is fed back to its PFD block through the fractional feedback (N) divider. The VCO output is also fed back to the DPLL feedback path in DPLL mode. For hybrid synchronization or cascaded frequency domain architectures each VCO output also can source to the DPLL input reference selection muxes or as an XO input for other APLLs or through fixed feedback dividers.

8.3.8.5.1 APLL N Divider With SDM

The APLL fractional N divider includes a 12-b integer portion (INT), a 40-b numerator portion (NUM), a fixed 40-b or a programmable 24-b denominator portion (DEN), and a sigma-delta modulator. The INT and NUM are programmable. When an APLL works with a DPLL in a loop, the APLL uses a fixed 40-bit denominator for very high frequency resolution on the VCO clock. When the APLL works in an independent loop, like APLL1 and APLL2 in 図 8-6 or the APLLs in 図 8-7, TI recommends a 24-bit programmable denominator. The total APLL N divider value is: N = INT + NUM / 2^{40} or INT + NUM / 2^{24} .

In APLL free-run mode, the PFD frequency and total N divider for the APLL determine the VCO frequency, which can be computed with 24-b denominator by 式 2.

8.3.8.6 APLL Loop Filters (LF1, LF2, LF3)

APLL3 supports a programmable loop bandwidth from 100 Hz to 10 kHz (typical range), and APLL1 or APLL2 supports a programmable loop bandwidth from 100 kHz to 1 MHz (typical range). The loop filter components can be programmed to optimize the APLL bandwidth depending on the reference input frequency and phase noise. The LF1, LF2, and LF3 pins each require an external C2 capacitor to ground. See the suggested values for the LF1, LF2, and LF3 capacitors in *Pin Configuration and Functions*.

図 8-22 shows the APLL loop filter structure between the PFD/charge pump output and VCO control input.

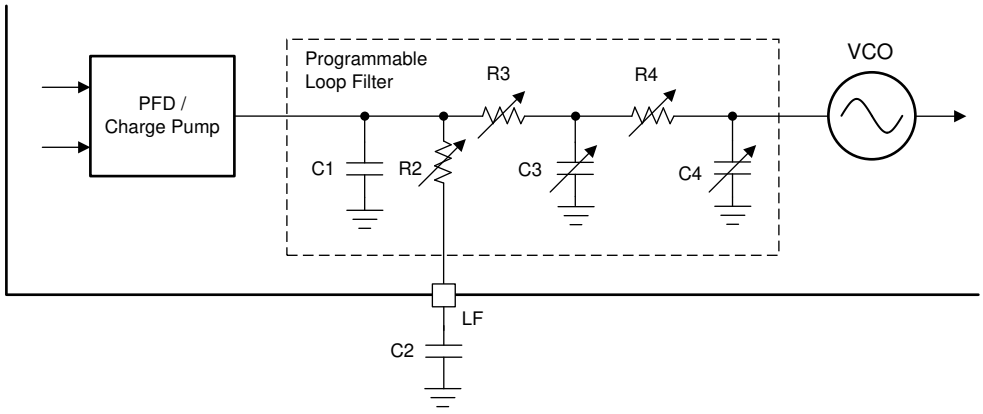


図 8-22. Loop Filter Structure of Each APLL

8.3.8.7 APLL Voltage-Controlled Oscillators (VCO1, VCO2, VCO3)

8.3.8.7.1 VCO Calibration

Each APLL VCO must be calibrated to ensure that the PLL can achieve lock and deliver optimal phase noise performance. VCO calibration establishes an optimal operating point within the VCO tuning range. VCO calibration is executed automatically during initial PLL start-up after device power-on, hard-reset, or soft-reset when the XO input is detected by its input monitor. To ensure successful calibration and APLL lock, it is critical

for the XO clock to be stable in amplitude and frequency before the start of calibration; otherwise, the calibration can fail and prevent PLL lock and output clock start-up. Before VCO calibration and APLL lock, the output drivers are typically held in the mute state (configurable per output) to prevent spurious output clocks.

A VCO calibration can be triggered manually for a single APLL by toggling a PLL enable cycle (APLLx_EN bit = 0 → 1) through host programming. This may be needed after the APLL N divider value (VCO frequency) is changed dynamically through programming.

8.3.8.8 APLL VCO Clock Distribution Paths

Each APLL VCO post-divider supports an independently programmable divider.

APLL2 has one VCO post-divider clock (P1: ÷2 to ÷13) available for distribution to all outputs.

APLL1 has two VCO post-dividers. The primary VCO post-divider clock (P1: ÷2 to ÷7) is distributed for OUT0, OUT1, OUT2 and OUT3 in LMK5B33414. The secondary APLL1 VCO post-divider clock (P2: ÷2 to ÷7) is distributed for OUT0 and OUT1 in the LMK5B33414.

APLL3 has one VCO post-divider paired with an optional divide by 2. The VCO3 post-divider is comprised of a programmable divide by 8 followed by an optional divide by 2. The APLL3 post-divider clock div8 (÷2 to ÷8) or div8 & div2 (÷10, ÷12,÷14, ÷16) can be distributed to all 4 output banks in LMK5B33414. If the system use case requires sourcing multiple frequencies from APLL3 that cannot be supported from a single post-divider value, then bypass the VCO3 post-divider by setting VCO3 post-divider = 1 and program the individual channel dividers to obtain the desired output frequencies.

8.3.8.9 DPLL Reference (R) Divider Paths

Each reference input clock has its own 16-b reference divider to the DPLL TDC block. The R divider output of the selected reference sets the TDC input frequency. To support hitless switching between inputs with different frequencies, the R dividers can be used to divide the clocks to a single common frequency to the DPLL TDC input.

8.3.8.10 DPLL Time-to-Digital Converter (TDC)

The TDC input compares the phase of the R divider clock of the selected reference input and the DPLL feedback divider clock from VCO. The TDC output generates a digital correction word corresponding to the phase error which is processed by the DPLL loop filter.

8.3.8.11 DPLL Loop Filter (DLF)

The DPLL supports a programmable loop bandwidth from 10 mHz to 4 kHz and can achieve jitter peaking below 0.1 dB (typical). The low-pass jitter transfer characteristic of the DPLL attenuates its reference input noise with up to 60-dB/decade roll-off above the loop bandwidth.

The DPLL loop filter output controls the fractional numerator of APLL to steer the VCO frequency into lock with the selected DPLL reference input.

8.3.8.12 DPLL Feedback (FB) Divider Path

The DPLL feedback path has a programmable prescaler (33 bits, 1 to $2^{33} - 1$) and a fractional feedback (FB) divider. The programmable DPLL FB divider includes a 33-b integer portion (INT), 40-b numerator portion (NUM), and 40-b denominator portion (DEN). The total DPLL FB divider value is: FB_{DPLL} = INT + NUM / DEN.

In DPLL mode, the TDC frequency and total DPLL feedback divider and prescalers determine the VCO frequency. Use 式 5 to calculate the VCO frequency.

8.3.9 Output Clock Distribution

The output clock distribution blocks include six output muxes, eleven output dividers, and fourteen programmable differential output drivers in LMK5B33414. The output dividers support output synchronization (SYNC) to allow phase synchronization between two or more output channels. Also, the channels OUT0, OUT4, or OUT10 have an optional internal zero-delay mode (ZDM) synchronization feature to support deterministic input-to-output phase alignment (typically for 1-PPS clocks) with programmable offset.

8.3.10 Output Channel Muxes

The LMK5B33414 employs 6 output multiplexers or muxes to distribute frequency sources to the respective output banks. OUT0 and OUT1 each have a separate 6:1 mux to individually select a source. OUT2 and OUT3 output channels share one 3:1 mux . The output bank OUT4 to OUT7 share one 2:1 mux and a second 2:1 mux is shared across the output bank OUT8 to OUT13.

The 6:1 MUX on OUT0 and OUT1 are the most flexible providing selection among APLL3 post divider, APLL2 post divider, the APLL1 primary post divider, APLL secondary post divider, buffered XO or reference input as a frequency source. The 3:1 MUX feeding the OUT2 and OUT3 can select a source between the APLL3 post divider, APLL2 post divider or the APLL1 primary post divider. OUT4 to OUT7 bank or OUT8 to OUT13 bank can each select a frequency source from the APLL3 post divider or the APLL2 post divider. The two 2:1 muxes for the

8.3.11 Output Dividers (OD)

There are one or more output dividers after each output mux. Each channel in OUT[0:1] has an individual 12-bit channel divider cascaded an optional 20-bit SYSREF divider. Each channel in OUT[2:3] has an individual 12-bit output divider. The OUT[4:5], OUT[6:7], OUT[8:9], OUT[10:11], and OUT[12:13] channels each have a single 12-bit output divider cascaded with an optional SYSREF divider. The output dividers are used to generate the final clock output frequency from the source selected by the output mux.

The OUT0 or OUT1 channel combines a 12-bit output channel divider (CD) and a 20-bit SYSREF divider to support output frequencies from 1-Hz (1-PPS) to 1250-MHz. From VCO to output, the total divide value is the product of the PLL post-divider (P), output channel divider (CD)and SYSREF divider (SD) values (P × CD × SD).

For example, with the APLL3 post-divider bypassed each 12-bit channel divider (CD) supports output frequencies from 100-kHz to 1250-MHz (or up to the maximum frequency supported by the configured output driver type). It is possible to then cascade the SYSREF divider (SD) to achieve lower clock frequencies down to 1-Hz (1-PPS).

Each output divider is powered from the same VDDO_x supply used for the clock output drivers. The output divider can be powered down if not used to save power. For each output group in OUT[2:3], OUT[4:5], OUT[6:7], OUT[8:9], OUT[10:11], or OUT[12:13], the output divider is automatically powered down when both output drivers are disabled. For OUT0 or OUT1 channel, the output divider is automatically powered down when its output driver is disabled.

8.3.12 SYSREF/1-PPS

LMK5B33414 can support system reference clocks from 1-PPS to 25-MHz including JEDEC JESD204B or JESD204C SYSREF clocks. Any 12-bit output channel divider except OUT2 or OUT3 can be cascaded with an individual 20-bit SYSREF divider. Set flexible SYSREF divider values to generate the same 1-PPS/SYSREF frequency on multiple outputs or different frequency multiples of 1-PPS/SYSREF based on application requirements. When aligning multiple SYSREF outputs TI recommends setting SYSREF_REQ_MODE 0x1A[5:4] = 11 for resampling of the SYSREF request. The 1PPS/SYSREF can also be replicated on GPIO1 or GPIO2 if additional single ended outputs are needed. The SYSREF request sample source SYSREF_REQ_SEL 0x1A[3:2] must be set to the same source as desired for SYSREF/1PPS Output Replication.

8.3.13 Output Delay

LMK5B33414 have the ability to tune output clock phase with delay function. In each channel divider path, there is a programmable static offset digital delay. With the SYSREF divider selected, the output clock can have additional programmable static offset digital delay, SYSREF digital delay and analog delay.

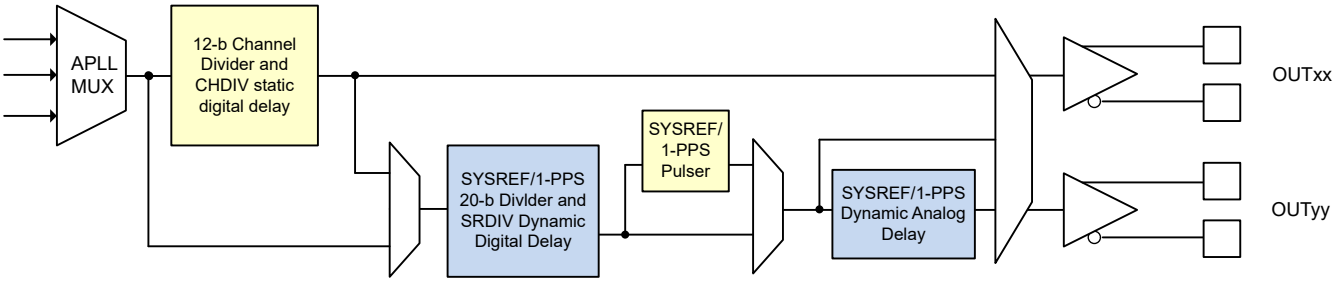


図 8-23. Programmable Static and Dynamic Output Delay

8.3.14 Clock Outputs (OUTx_P/N)

Each clock output can be individually configured as a differential driver (AC-LVPECL/HSDS/LVDS/HCSL). The HSDS driver has the capability to program output voltage swing and common mode voltage. Unused clock outputs can be disabled to save power.

Each output channel has its own internal LDO regulator to provide excellent PSNR and minimize jitter and spurs induced by supply noise. For differential modes, the output clock specifications (such as output swing, phase noise, and jitter) are not sensitive to the VDDO_x voltage because of the channel's internal LDO regulator.

The OUT0 and OUT1 channel (mux, divider, and drivers) are powered through a single output supply pin (VDDO_0_1), and similarly for the OUT2 and OUT3 channel (VDDO_2_3). Output banks OUT4 to OUT7 and OUT8 to OUT13 each have their own output supply pin (VDDO_4_TO_7) and (VDDO_8_TO_13) respectively. Each output supply pin should be powered by 3.3-V and always connected to the supply even if not used.

OUT0 or OUT1 has the additional capability for two 1.8-V or 2.65-V LVCMOS drivers per output pair. CMOS output voltage levels are determined by internal programming of the CMOS output LDO to support either 1.8-V or 2.65-V LVCMOS.

For additional low frequency single ended clock outputs GPIO1 and GPIO2 may be configured to replicate any 1PPS/SYSREF divider output from another differential output pair.

8.3.14.1 Differential Output

The differential HSDS driver can be programmed to achieve V_{OD} swing (single-ended peak-to-peak amplitude) compatible with LVDS, CML, LVPECL and other differential receivers. V_{OD} ranges from 0.4 V to 1 V with a step size of roughly 100 mV. The HSDS driver can be DC-coupled or AC-coupled. There are two common-mode options for each of the V_{OD} settings. See the *Electrical Characteristics* table for more information.

The traditional HCSL output driver is PCIe compliant and requires 50-Ω external termination. TI recommends placing the termination close to the receiver side.

8.3.14.2 LVCMOS Output

The LVCMOS drivers available for selection on OUT0 and OUT1 have two outputs per P and N pair. Each output on P and N can be configured for normal polarity, inverted polarity, or disabled as Hi-Z or static low level. The LVCMOS output high level (V_{OH}) is determined by the internal programmable LDO regulator voltage of 1.8 V or 2.65 V for rail-to-rail LVCMOS output voltage swing. LVCMOS mode is only supported on channel outputs 0 and 1 and is primarily to support ASIC or processor clocks which do not have as stringent phase noise or jitter requirements.

An LVCMOS output clock is an unbalanced signal with large voltage swing, therefore it can be a strong aggressor and couple noise onto other jitter-sensitive differential output clocks. If an LVCMOS clock is required from an output pair, configure the pair with both outputs enabled but with opposite polarity (+/– or –/+) and leave the unused output floating with no trace connected.

8.3.14.3 SYSREF/1-PPS Output Replication

The SYSREF divider output signals can be replicated on either GPIO1 and GPIO2 to provide additional single ended 3.3V CMOS clocks after start-up if desired. To configure the SYSREF/1-PPS output replication the GPIO

must be enabled as an output (GPIOx_OUTEN = 1) and one of the SYSREF output to GPIO replication sources must be active. The SYSREF replication source comes from any one of the SYSREF dividers in use from OUT0/1, OUT4/5, OUT6/7, OUT/9, OUT10/11 or OUT12/13 by register programming (OUT_x_y_SR_GPIO_EN = 1). The GPIOx replicated SYSREF output is after static digital delay but before the analog and digital delay and pulser. The output will be a continuous frequency as pulsed SYSREF mode is not supported for the GPIOx replica.

There will be some small fixed delay skew between the normal SYSREF and GPIO replicated SYSREF. An LVCMOS output clock is an unbalanced signal with large voltage swing, therefore it can be a strong aggressor and couple noise onto other jitter-sensitive differential output clocks.

8.3.14.4 Output Auto-Mute During LOL

Each output driver can automatically mute its clock when the selected output mux clock source is invalid, as configured by its MUTE enable field. The source can be invalid based on the LOL status of each PLL by configuring the APLL and DPLL mute control bits (MUTE_APLLx_LOCK, MUTE_DPLLx_LOCK, MUTE_DPLLx_PHLOCK). When auto-mute is disabled or bypassed (OUT_x_y_MUTE_EN = 0), the output clock can have incorrect frequency or be unstable before and during the VCO calibration.

8.3.15 Glitchless Output Clock Start-Up

When APLL auto-mute is enabled, the outputs will start up in synchronous fashion without clock glitches when an APLL lock is achieved after any of the following events: device power-on, exiting hard-reset or deasserting output SYNC.

8.3.16 Clock Output Interfacing and Termination

This section shows the recommended output termination. Unused clock outputs can be left floating and powered down by programming.

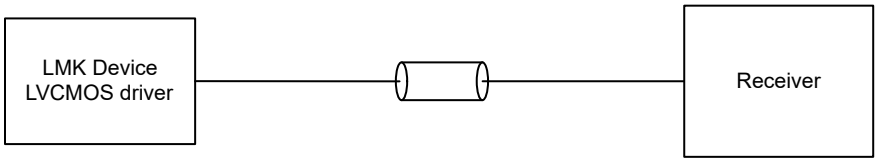


図 8-24. LVCMOS Output Termination

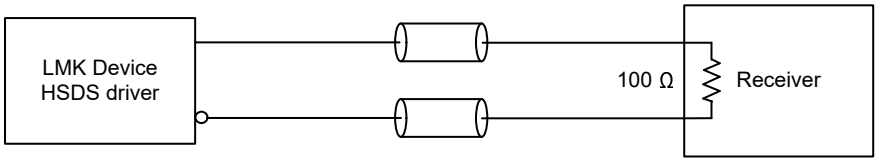


図 8-25. DC-Coupled HSDS Output Termination

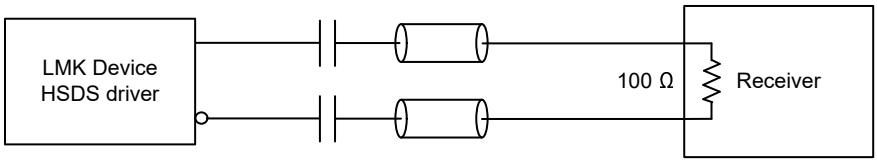


図 8-26. AC-Coupled HSDS Output Termination Method 1

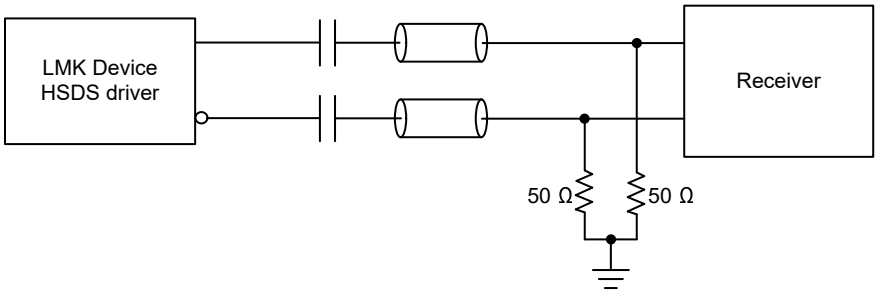


図 8-27. AC-Coupled HSDS Output Termination Method 2

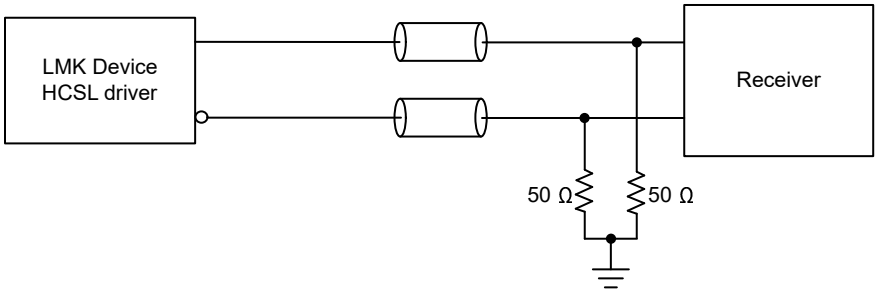


図 8-28. DC-Coupled HCSL Output Termination

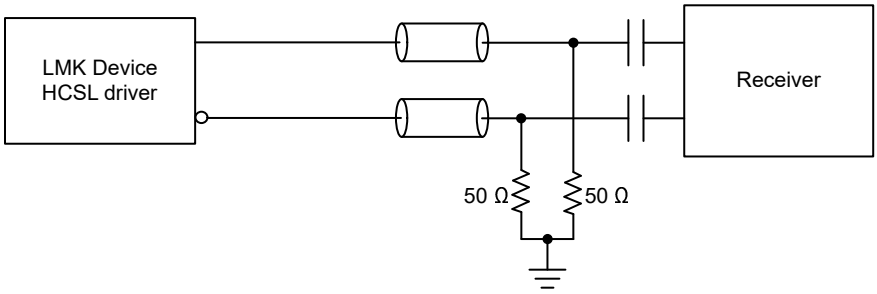


図 8-29. AC-Coupled HCSL Output Termination

8.3.17 Output Synchronization (SYNC)

Output SYNC can be used to phase-align two or more output clocks with a common rising edge by allowing the output dividers to exit reset on the same PLL output clock cycle. Any output dividers selecting the same PLL output can be synchronized together as a SYNC group by triggering a SYNC event through the hardware pin or software bit.

The following requirements must be met to establish a SYNC group for two or more output channels:

- Output dividers have their respective sync enable bit set (OUT_x_y_DIV_SYNC_EN = 1)
- SYSREF dividers have their additional respective sync enable bit set (OUT_x_y_SR_DIV_SYNC_EN = 1), work with above set (OUT_x_y_DIV_SYNC_EN = 1)
- Output dividers have their output mux selecting the same PLL output
- The PLL (post-divider) output has its sync enable bit set (for example, PLL1_PRI_DIV_SYNC_EN = 1)
- SYNC_EN = 1

A SYNC event can be asserted by either a GPIOx pin programmed for SYNC input with GPIOx_MODE = 31 or the SYNC_SW register bit (active high). When SYNC is asserted, the SYNC-enabled dividers are held in reset and clock outputs are low. When SYNC is deasserted, the outputs from a common PLL will start with their initial clock phases synchronized or aligned. SYNC can also be used to set a low state on any SYNC-enabled outputs to prevent output clocks from being distributed to downstream devices until the receiver inputs are configured and ready to accept the incoming clock.

Output channels with their sync disabled (OUT_x_y_DIV_SYNC_EN = 0) will not be affected by a SYNC event and will continue normal output operation as configured. VCO post-divider clocks must be enabled for synchronization to ensure the dividers they drive are synchronized accurately. However, any output deriving a clock from a reset VCO post-divider will not be valid during SYNC, even if the channel divider is not selected for SYNC. VCO post-dividers not selected for synchronization do not stop running during the SYNC so they can continue to source output channels that do not require synchronization. Output dividers with divide-by-1 (divider bypass mode) are not gated during the SYNC event.

表 8-3. Output Synchronization

GPIOx as SYNC PIN GPIOx_MODE = 31		SYNC_SW R21[6]	OUTPUT DIVIDER AND DRIVER STATE
GPIOx_POL = 0	GPIOx_POL = 1		
1	0	1	Output driver(s) muted and output divider(s) reset
1 → 0	0 → 1	1 → 0	SYNCed outputs are released with synchronized phase
0	1	0	Normal output driver/divider operation as configured

8.3.18 Zero-Delay Mode (ZDM)

Zero-delay mode synchronization can be enabled to achieve *zero* phase delay between the selected DPLL reference input clock and the selected zero-delay feedback clock. 図 8-30 shows how the OUT0 clock can internally feedback to any DPLL as the zero-delay output clock. Zero-delay mode is primarily implemented to achieve deterministic phase relationship between an input and selected outputs such as 1-PPS input to 1-PPS outputs or 156.25-MHz input to 156.25-MHz outputs.

There is no need to route external clock signals from output to input as the zero-delay feedback clock from OUT0 is routed internally to the device. Alternatively to OUT0, OUT4 may be used for DPLL2 internal ZDM feedback and OUT10 may be used for DPLL3 internal ZDM feedback.

1-PPS phase alignment is able to re-establish with the phase slew control and ZDM. For 1-PPS and ZDM, hitless switching must be enabled to prevent the DPLL from becoming unlocked. After performing hitless switching, the phase slew control can reduce the phase build-out back to 0 at a controlled rate. To lock to a 1-PPS signal using ZDM mode, the output static delay or DPLLx_PH_OFFSET must be programmed to zero out the phase error between the 1-PPS input and 1-PPS feedback clock. See DPLL Programmable Phase Delay for an example of how input to output phase error in the DPLLx_PH_OFFSET field is calculated to apply fine adjustments less than 1-ps.

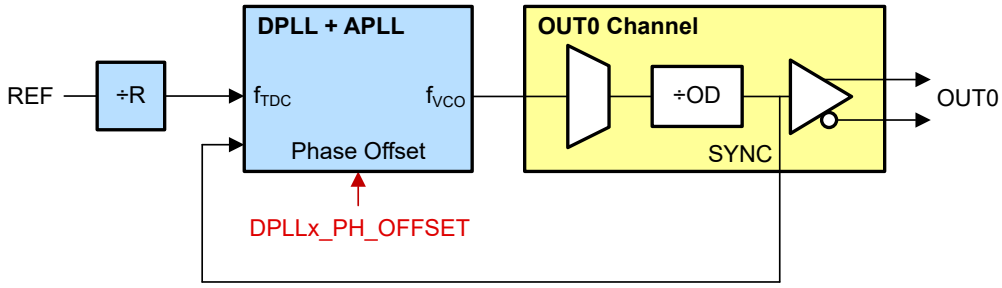


図 8-30. DPLL ZDM Synchronization Between Reference Input and OUT0

8.3.19 Time Elapsed Counter (TEC)

The Time Elapsed Counter (TEC) allows the user to make a precise time measurement between two (or more) events. The events may be either a rising or falling edge of a GPIO pin or a falling edge of the SPI SCS pin. Any GPIO pin can be programmed for TEC input. Rising or falling polarity can be chosen using the GPIO polarity invert register. After each TEC event, the counter values is captured and the application may read back a 40-bit value. The elapsed time is calculated based on the difference in the read back values. The accuracy of the measurement is better than 7.5 ns with a total measurement time over 59 minutes depending on exact

configuration. It is necessary to read back at least the LSB of the TEC_CNTR to re-arm the TEC counter capture.

The TEC counter is clocked at a frequency based on PLL3 VCO frequency ÷8 or PLL2 VCO frequency ÷ 20. A time measurement is made by below steps.

1. Reset the TEC counter value. Recommended to reduce chance of counter roll-over between TEC capture events, but optional. If the reset is not done the user would need to detect roll-over of counter register which will complicate 式 10 for elapsed time calculation.
2. Trigger TEC capture event and read back the TEC registers containing the stored counter value.
3. Trigger the TEC capture event a second time and read back the TEC registers containing the stored counter value.
4. Use 式 10 to calculate the elapsed time. The worst-case error is twice the TEC counter clock period. 表 8-4 lists some common TEC clock frequencies/periods and roll-over times.

Elapsed Time = (2nd captured TEC value - 1st captured TEC value) / TEC Clock Rate (10)

The TEC_CNTR register is split across five registers.

表 8-4. Common TEC Clock Frequencies and Roll-Over Times

PLL SOURCE	VCO FREQUENCY	TEC CLOCK FREQUENCY	TEC CLOCK PERIOD (t)	ROLL-OVER TIME
PLL3	2500 MHz	312.5 MHz	~3.17 ns	~58.6 minutes
PLL2	5950 MHz	297.5 MHz	~3.361 ns	~61.6 minutes
PLL2	5898.24 MHz	294.912 MHz	~3.391 ns	~62.1 minutes
PLL2	5625 MHz	281.25 MHz	~3.556 ns	~65.1 minutes
PLL2	5600 MHz	280 MHz	~3.571 ns	~65.4 minutes

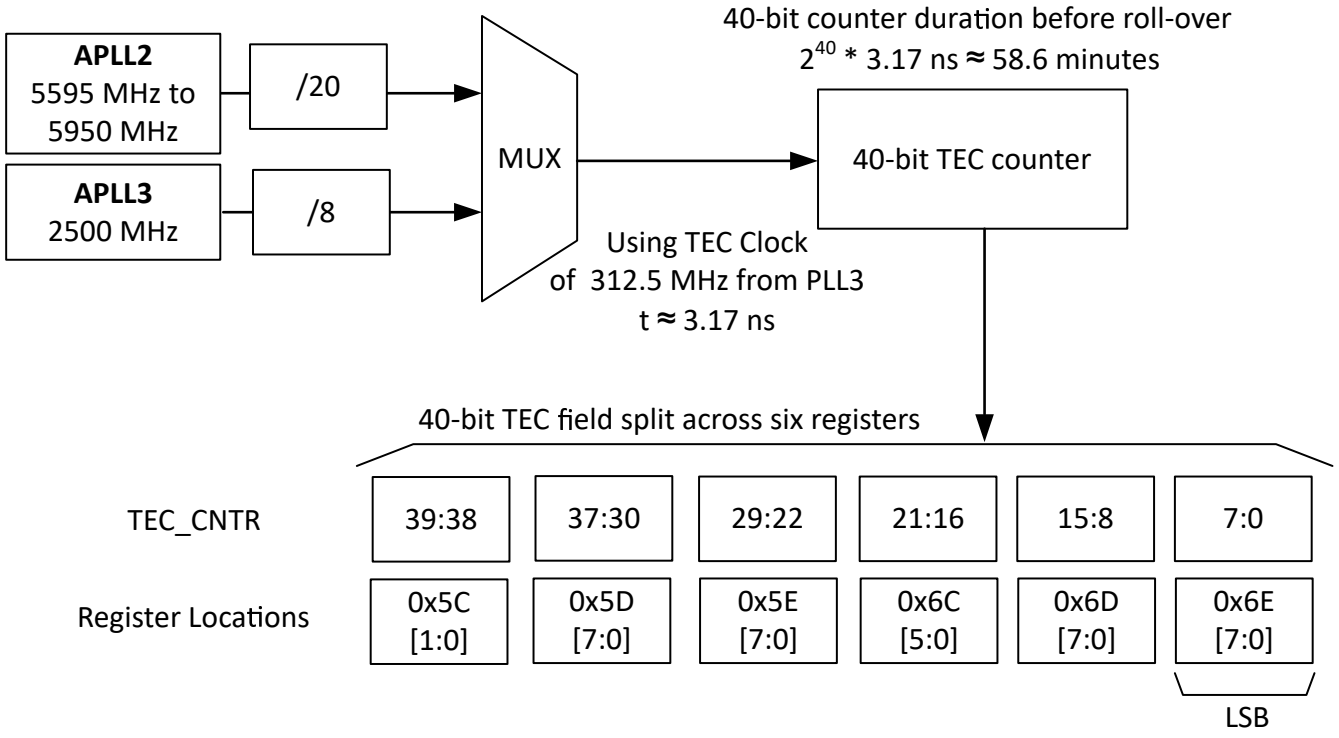


図 8-31. TEC Clock and Counter

図 8-32 illustrates the states of the Time Elapsed Counter function.

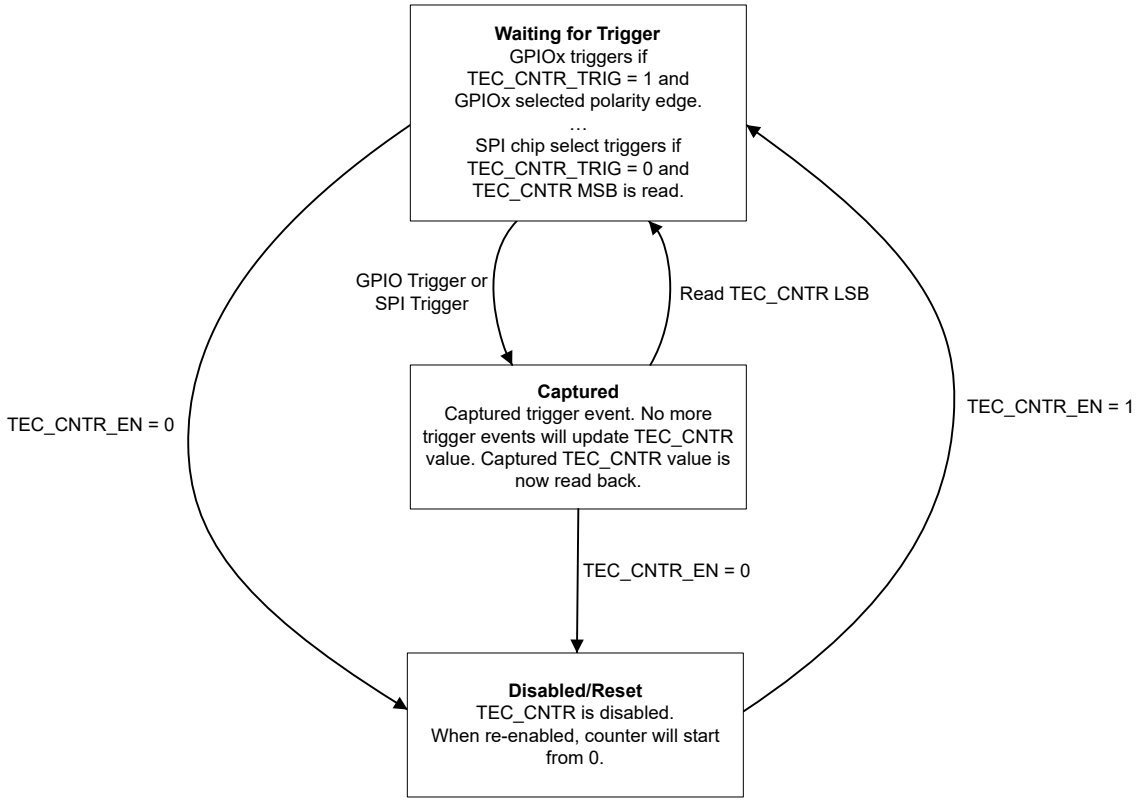


図 8-32. State Diagram of TEC

8.3.19.1 Configuring TEC Functionality

1. Select the PLL to drive the Time Elapsed Counter (TEC). PLL3 will offer the highest accuracy time measurement due to the highest TEC clock frequency, however PLL2 provides slightly longer roll-over times.
   - PLL3 source is selected by setting REF0_MISSCLK_VCOSEL to 0.
   - PLL2 source is selected by setting REF0_MISSCLK_VCOSEL to 1.
2. Select GPIO or SPI chip select as a trigger to capture the TEC counter value to TEC_CNTR field. Using a GPIO does not require any special timing for the SPI SCS pin. It is possible to use the GPIO pin for other purposes, then enable the TEC functionality when required.
   - GPIO trigger is selected by setting TEC_CNTR_TRIG to 1.
   - SPI chip select trigger is selected by setting TEC_CNTR_TRIG to 0.
3. Enable the TEC counter by setting TEC_CNTR_EN to 1.

8.3.19.2 SPI as a Trigger Source

When TEC_CNTR_EN = 1, each SCS falling edge the TEC counter will be captured to the TEC_CNTR field. Subsequent to a SPI transaction which reads from the MSB of the TEC_CNTR field, no falling edge of SCS will capture the TEC counter to the TEC_CNTR field until the LSB of the TEC_CNTR field is read.

図 8-33 shows when the TEC is latched during single register reads and 図 8-34 for a multibyte read.

図 8-33 shows that the TEC counter is captured every falling SCS edge until TEC_CNTR MSB is read.

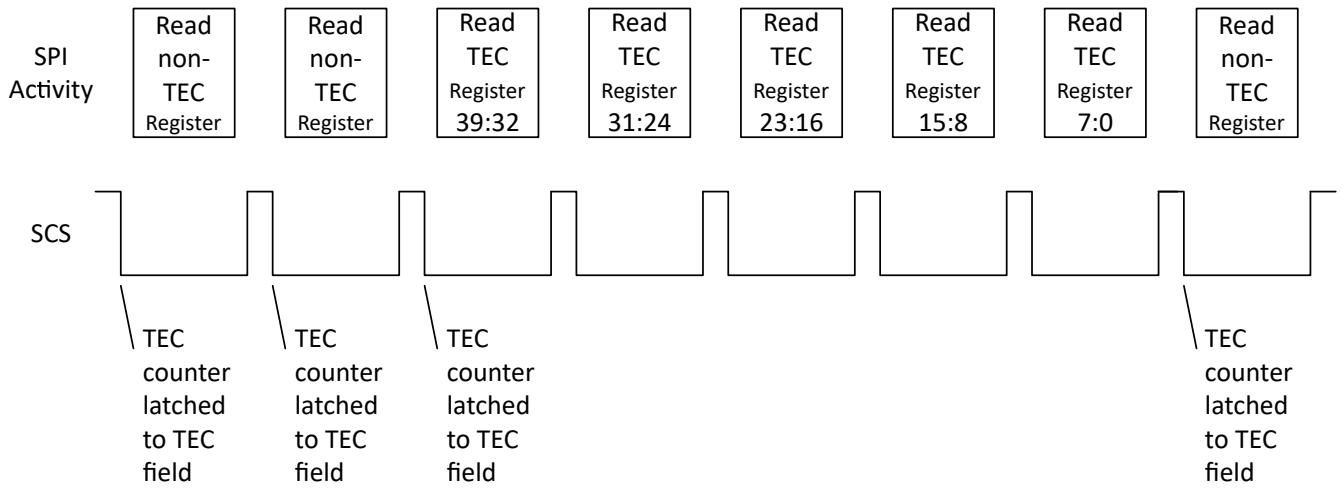


図 8-33. TEC Single Byte Read

図 8-34 shows that the TEC counter value can be captured and re-armed for capture during a single multibyte read, even if the first register read is not the TEC_CNTR registers.

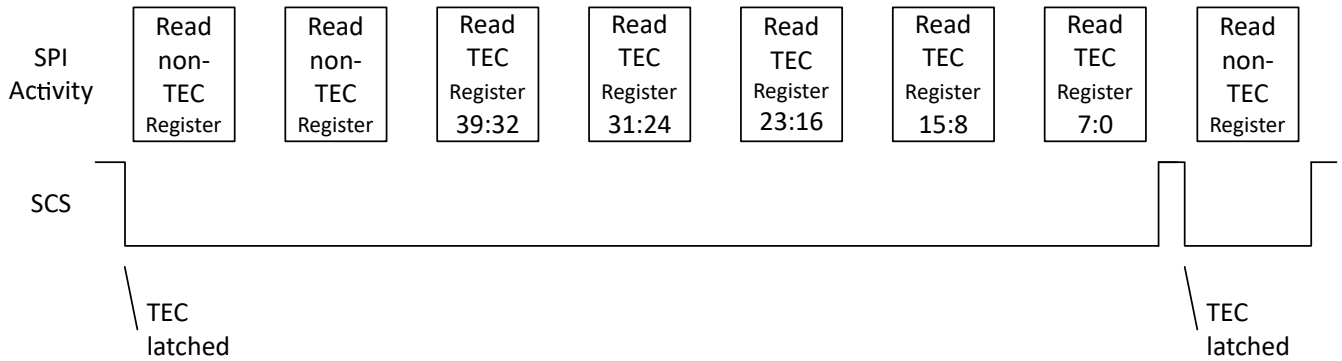


図 8-34. TEC Multibyte Read

8.3.19.3 GPIO Pin as a TEC Trigger Source

A rising edge of a GPIO pin selected for TEC functionality with GPIOx_MODE = 0x27 (TEC_TRIG_SEL) will capture the TEC value to the TEC_CNTR field upon an edge of the selected polarity (GPIOx_POL). No further updates to the TEC_CNTR field will be made by subsequent GPIOx pin edges until the LSB of the TEC_CNTR field is read. 図 8-35 shows the timing of using a GPIO to capture TEC values.

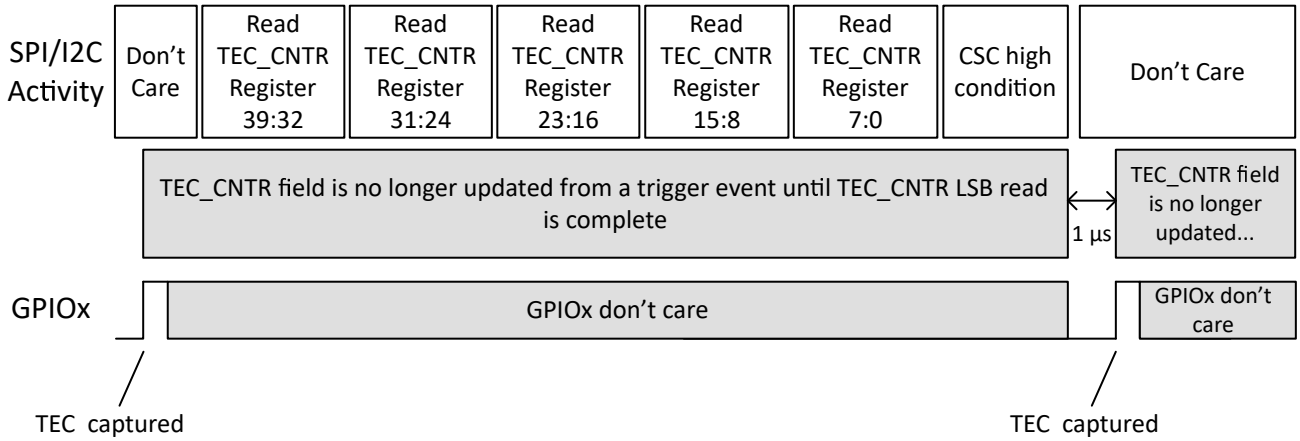


図 8-35. TEC Captured Using GPIO

8.3.19.3.1 An Example: Making a Time Elapsed Measurement Using TEC and GPIO1 as Trigger

1. Configure TEC registers as desired. In this example:
   - REF0_MISSCLK_VCOSEL is 0 so that VCO3 frequency / 8 is used for TEC clock rate
   - TEC_CNTR_TRIG = 1 for GPIO1 trigger
   - TEC_CNTR_CLR = 0 for normal operation
2. Set GPIO1_MODE = 0x27 (TEC_TRIG_SEL) and GPIO1_POL as desired, 0 in this example for active high input.
3. Provide rising edge on GPIO1 to capture current TEC counter value into the TEC_CNTR field.
4. Read and store the TEC_CNTR field for the first time.
   - Example: 1st_captured_TEC_value = 204 354.
5. Provide rising edge on GPIO1.
6. Read and store the TEC_CNTR field for the second time.
   - Example: 2nd_captured_TEC_value = 76 516 568

8.3.19.4 TEC Timing

When TEC_CNTR_TRIG is 1 (GPIO pin):

- Timing accuracy of 1 TEC cycle + 2 ns requires a 20% to 80% rise time of less than or equal to 1 ns.
- GPIOx rising edge should not occur within 10 ns of rising SCS which sets TEC_CNTR_EN from 0 to 1.
- GPIOx should remain high for 10 ns.
- A new GPIOx trigger should not arrive within 1 µs of the rising edge of the SPI SCS after reading the LSB of the TEC_CNTR.

When TEC_CNTR_TRIG is 0 (SPI):

- Timing accuracy of 1 TEC cycle + 2 ns requires an 80% to 20% fall time of less than or equal to 1 ns.
- The TEC counter is captured to the TEC_CNTR registers at the falling edge of SPI SCS. No additional time to read back or pre-latching of register is required.

8.3.19.5 Other TEC Behavior

The TEC counter continually counts up and periodically rolls over from $2^{40} – 1$ to 0.

- The user software must determine if the counter has rolled over in between TEC reads. TI recommends resetting the TEC counter accordingly by toggling the TEC_CNTR_EN bit before a prospective starting trigger event, if known.

The REF0_MISSCLK_VCOSEL field also selects which VCO is used by all inputs for the early and missing reference clock validation, therefore the early and missing input validation registers may need to be re-calculated if REF0_MISSCLK_VCOSEL is changed. Changing REF0_MISSCLK_VCOSEL or validation calculations during operation may result in references using the missing pulse or both missing and runt pulse detectors to be momentarily disqualified and send the DPLL into holdover.

While TEC_CNTR_EN = 0, the TEC counter is held in reset, which is counter value 0. It is possible to make an absolute time measurement from the moment that TEC_CNTR_EN transitions from 0 to 1 to a future trigger event. However the accuracy of this measurement is less than performing a relative measurement caused by two GPIO or two SPI CSC triggers.

8.4 Device Functional Modes

8.4.1 Device Start-Up

The device can start up using I^2C or SPI selected as the control interface depends on the 2-level input level sampled on the GPIO1 pin during power-on reset (POR). Internal register default settings after POR depend on the value of the ROM_PLUS_EE field stored in EEPROM.

- **GPIO1 = 0:** I^2C communication interface selected
- **GPIO1 = 1:** SPI communication interface selected

After start-up, the I^2C or SPI interface is enabled for register access to monitor the device status and control (or reconfigure) the device if needed. The register map configurations are the same for I^2C and SPI.

The state of GPIO1 during POR determines:

- The serial interface (I^2C or SPI) used for register access.
- The functionality of the SCS_ADD pin for device control and status.

The state of the EEPROM field EE_ROM_PAGE_SEL plus the GPIO0 and GPIO2 pins select the ROM page which will be used at start-up. If the field ROM_PLUS_EE is 0, then the device is started with just the ROM settings. If the field ROM_PLUS_EE is 1, then an EEPROM overlay is loaded and many fields controlling APLL and output clock configuration will be loaded from the EEPROM. This allows the user flexibility to select start-up clocks frequencies and output formats.

図 8-36 shows the device power-on reset configuration sequence.

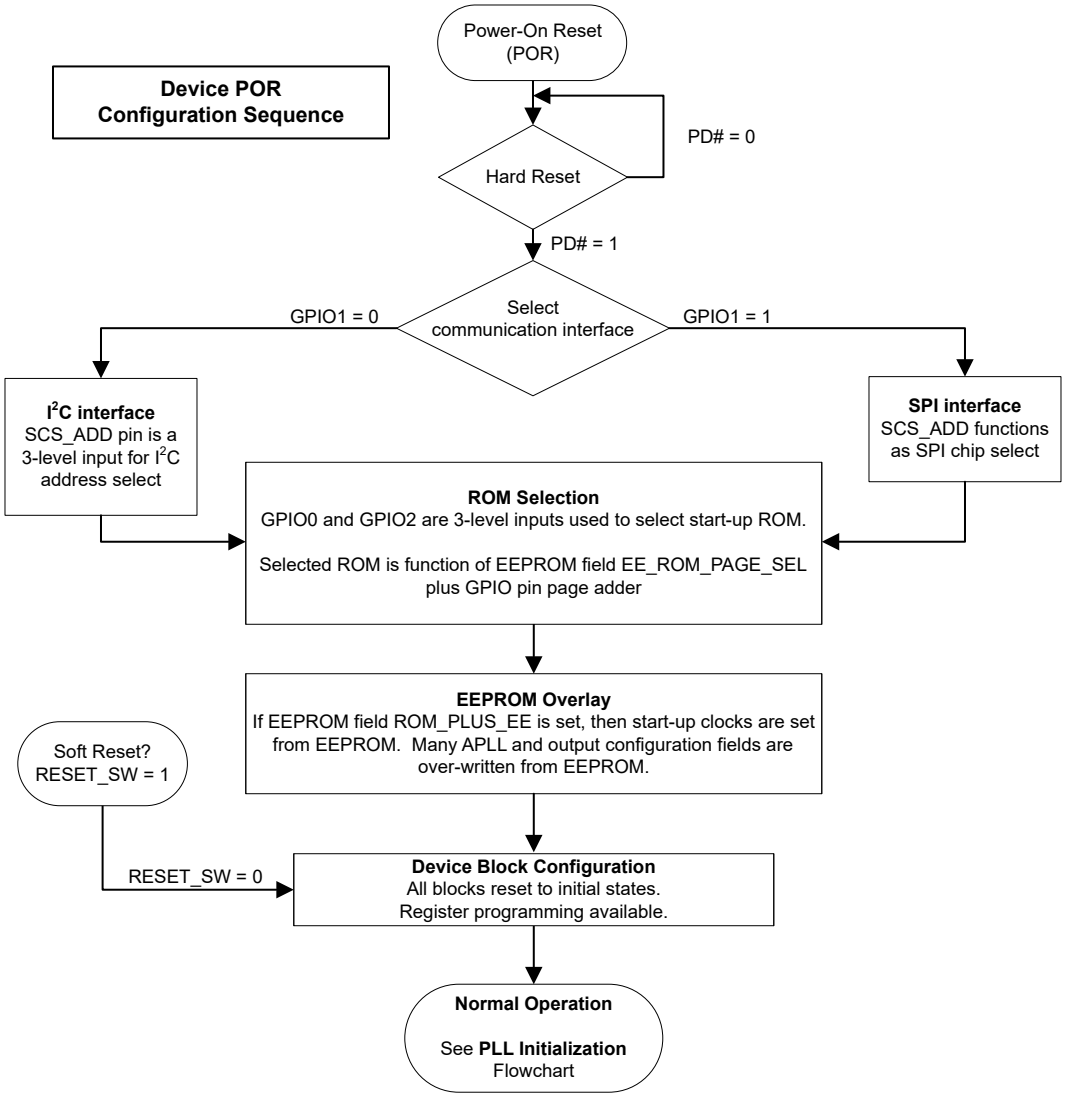


図 8-36. Device POR Configuration Sequence

Also see 図 8-14, 図 8-37, and 図 8-38.

8.4.1.1 ROM Selection

At POR the GPIO0 and GPIO2 pin state select a ROM page in conjunction with the EEPROM stored field EE_ROM_PAGE_SEL. The default EEPROM setting is EE_ROM_PAGE_SEL = 0. All register pages in the ROM image are factory-set in hardware (mask ROM) and are not software programmable. For more details on the device configuration refer to the LMK5B33xxx programming guide.

表 8-5. ROM Page Selection

GPIO2 at POR	GPIO0 at POR	ROM page with EE_ROM_PAGE_SEL = 0
L	L	ROM page 0. XO= 48 MHz, REFCLK = 25MHz, outputs 25 MHz, 100 MHz, 155.52 MHz, 156.25 MHz, 161.128125 MHz, 312.5MHz.
L	H	ROM page 1. XO = 48MHz, outputs 25 MHz, 50 MHz, 100 MHz.
H	L	ROM page 2. XO= 48 MHz, REFCLK = 25MHz, all outputs 156.25 MHz.
H	H	ROM page 3. Low power mode. All PLLs off, all outputs off.
L	M	ROM page 4. XO = 49.152 MHz, REFCLK = 19.44 MHz, outputs 100MHz, 312.5 MHz, 800 MHz.

表 8-5. ROM Page Selection (continued)

GPIO2 at POR	GPIO0 at POR	ROM page with EE_ROM_PAGE_SEL = 0
M	L	ROM page 5. XO= 48 MHz, REFCLK = 156.25MHz, outputs 100 MHz, 125 MHz, 156.25 MHz
M	M	ROM page 6. XO= 48 MHz, REFCLK = 25MHz, all outputs 312.5 MHz.
M	H	ROM page 7. XO= 48 MHz, REFCLK = 156.25MHz, outputs 100MHz, 125 MHz, 156.25 MHz.
H	M	ROM page 8. XO= 48.008 MHz, REFCLK = 156.25MHz, outputs 25 MHz, 50 MHz, 100 MHz, 156.25 MHz

8.4.1.2 EEPROM Overlay

An integrated EEPROM supports user-customized output clocks on start-up when the ROM pages will not meet start-up clocking requirements.

At POR if the EEPROM field ROM_PLUS_EE = 1, after the ROM settings are loaded the EEPROM will overwrite APLL and clock output registers to provide the user programmed EEPROM start-up clocks. If the ROM based DPLL configuration is not valid, the APLLs will simply lock to the XO reference frequency until the DPLL is configured at which time the DPLL will validate the DPLL reference input and proceed to lock.

The factory default setting for the EEPROM field ROM_PLUS_EE = 0.

8.4.2 DPLL Operating States

The following sections describe the DPLL states of operation shown in 図 8-37.

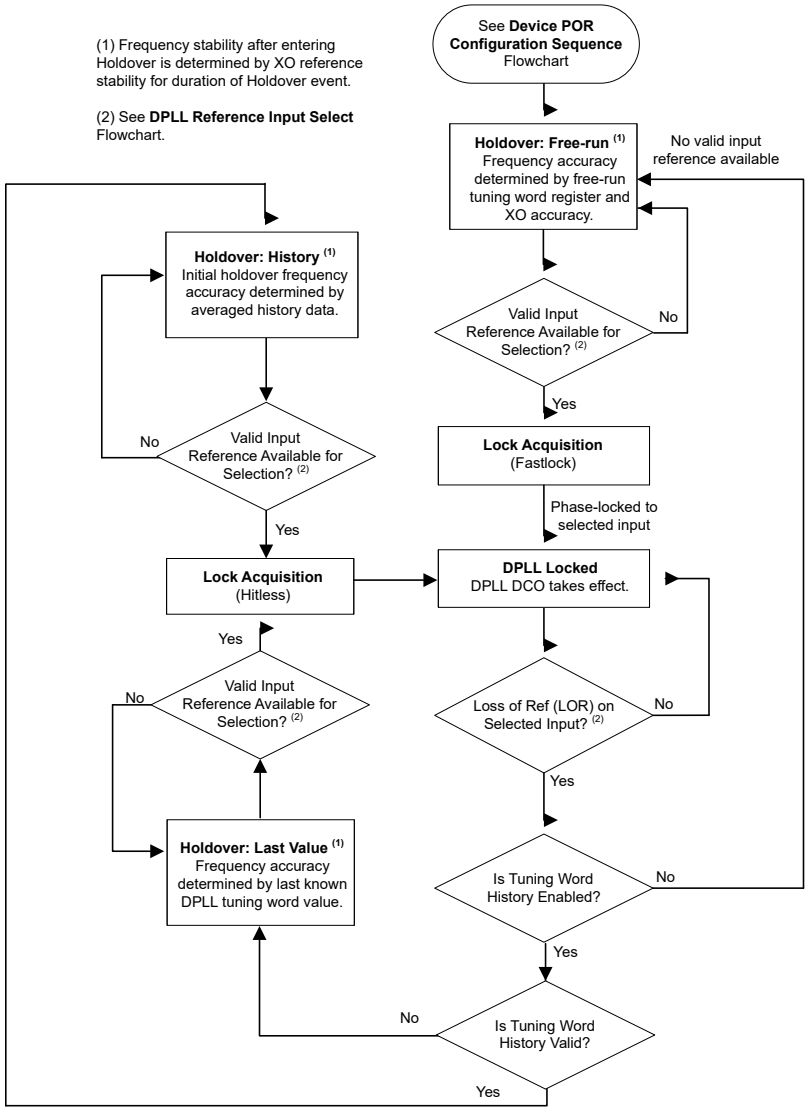


図 8-37. DPLL Operating States

Diagram assumes holdover is enabled. Also see 図 8-14, 図 8-36, and 図 8-38.

8.4.2.1 Free-Run

After device POR configuration and initialization, APLL will automatically lock to the XO clock when the XO input signal is valid. The output clock frequency accuracy and stability in free-run mode track the frequency accuracy and stability of the XO input. The reference inputs remain invalid (unqualified) during free-run mode. If the DPLL has locked, but not yet accumulated a valid history word and the reference is lost, then Free-Run is entered.

8.4.2.2 Lock Acquisition

The DPLL constantly monitors its reference inputs for a valid input clock. When at least one valid input clock is detected, the PLL channel will exit free-run mode or holdover mode and initiate lock acquisition through the DPLL. The LMK5B33414 supports the Fastlock feature where the DPLL temporarily engages a wider loop bandwidth to reduce the lock time. When the lock acquisition is done, the loop bandwidth is set to its normal configured loop bandwidth setting (BW_{DPLL}).

8.4.2.3 DPLL Locked

When the DPLL locks, the APLL output clocks are frequency and phase locked to the selected DPLL reference input clock. While the DPLL is locked, the APLL output clocks will not be affected by frequency drift on the XO input. The DPLL has a programmable frequency lock detector and phase lock detectors to indicate loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL) status flags, which can be observed through the status pins or status bits. When the frequency lock is detected (LOFL → 0), the tuning word history monitor (if enabled) will begin to accumulate historical averaging data used to determine the initial output frequency accuracy upon entry into holdover mode.

8.4.2.4 Holdover

When a loss-of-reference (LOR) condition is detected and no valid input is available the DPLL enters holdover.

If history is disabled (DPLLx_HIST_EN = 0) the DPLL will use the 2s complement DPLLx_FREE_RUN[39:0] field which sets holdover frequency relative to the DPLL numerator. Short-term frequency accuracy is based on the accuracy of the DPLLx_FREE_RUN field.

If history is enabled (DPLLx_HIST_EN = 1) but the tuning history is not yet valid, then the DPLLx_FREE_RUN field is used as if DPLLx_HIST_EN was disabled. If the tuning history is valid, the DPLL enters holdover using historical data to minimize holdover frequency error. See *Tuning Word History*. In general, the longer the historical average time, the more accurate the initial holdover frequency assuming the 0-ppm reference clock (XO input) is drift-free. The stability of the XO reference clock determines the long-term stability and accuracy of the holdover output frequency.

Upon entry into holdover, the LOPL flag will be asserted (LOPL → 1). The LOFL flag reports DPLL frequency versus reference frequency is in tolerance. In holdover LOFL will remain unchanged in holdover and not update until a valid reference is once again selected.

When a valid input becomes available for selection, the DPLL will exit holdover mode and automatically phase lock with the new input clock without any output glitches.

8.4.3 PLL Start-Up Sequence

図 8-38 shows the general sequence for PLL start-up after device configuration. This sequence also applies after a device soft-reset or individual PLL soft-reset. To ensure proper VCO calibration, it is critical for the external XO clock to be stable in amplitude and frequency prior to the start of VCO calibration otherwise the VCO calibration can fail and prevent start-up of the PLL and its output clocks.

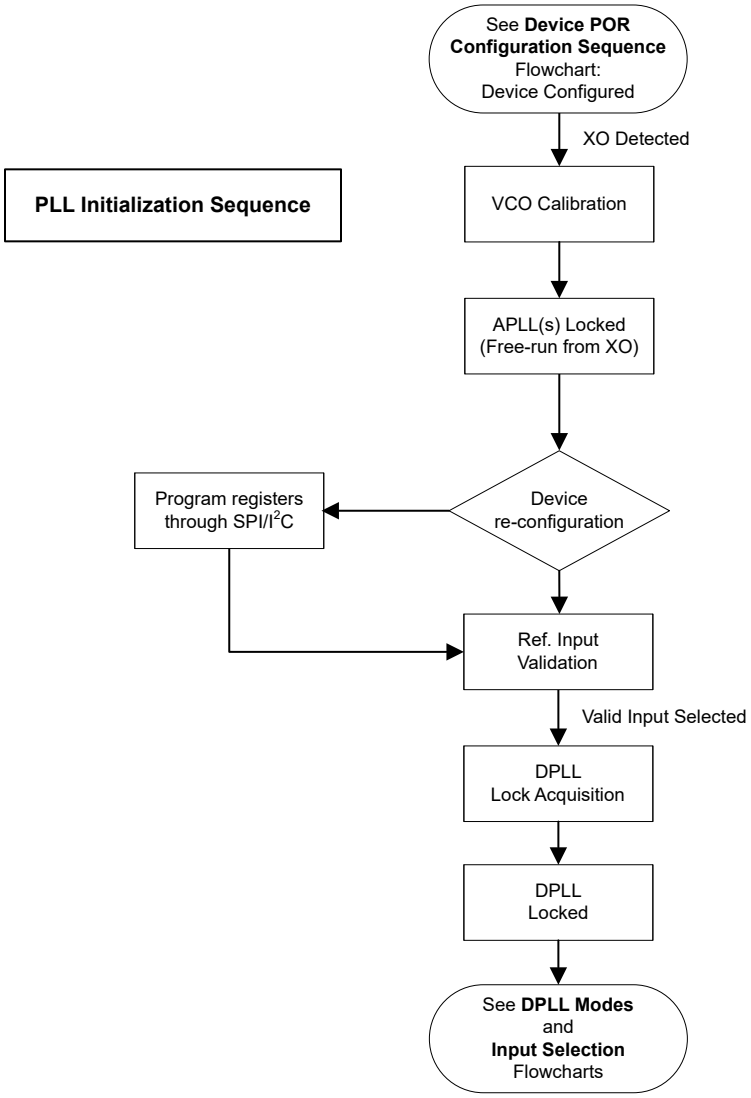


図 8-38. PLL Initialization Sequence

Also see 図 8-14, 図 8-36, and 図 8-37.

8.4.4 Digitally-Controlled Oscillator (DCO) Frequency and Phase Adjustment

To support IEEE 1588 and other clock steering applications, the DPLL supports DCO mode to allow precise output clock frequency adjustment of less than 0.001 ppb/step. DCO may be implemented using DPLL DCO control or APLL DCO control. While the DPLL is operating in closed-loop mode, DPLL DCO modifies the effective DPLL numerator. While the DPLL is in holdover or not used, APLL DCO adjusts the effective APLL numerator.

8.4.4.1 DPLL DCO Control

DCO mode can be enabled (DPLLx_FB_FDEV_EN = 1) when the DPLL is locked.

There are three methods to steer frequency when using the DPLL DCO.

- Register relative adjustment
  - Preset the deviation amount in DPLL_FDEV
  - Write an 8-bit register to enable increment/decrement by the deviation amount
- GPIO relative adjustment
  - Step/Direction GPIOx trigger
  - Adjust DPLLx_FB_NUM by programming a deviation amount for each step in pin set direction.
- Register absolute adjustment
  - Write the DPLLx_FB_NUM [39:0] based on the frequency control word (FCW)

The DCO frequency step size can be programmed through a 38-bit frequency deviation word register (DPLL_FDEV bits). The DPLL_FDEV value is an offset added to or subtracted from the current numerator value of the DPLL fractional feedback divider and determines the DCO frequency offset at the VCO output.

The DCO frequency increment (FINC) or frequency decrement (FDEC) updates can be controlled through software control (DPLLx_FB_FDEV_UPDATE) or user selectable pin control (GPIOx). DCO updates through software control are always available through I^2C or SPI by writing to the DPLLx_FB_FDEV_UPDATE register bit. Writing a 0 will increment the DCO frequency by the programmed step size, and writing a 1 will decrement the DCO frequency by the step size. SPI can achieve faster DCO update rates than I^2C because the SPI has faster write speed.

When DPLL pin control is selected (FDEV_TRIG_DPLLx and FDEV_DIR_DPLLx on GPIOs), a rising edge on the GPIO pin defined in FDEV_TRIG_DPLLx will apply a corresponding DCO update to the DPLL, another GPIO defined in FDEV_DIR_DPLLx will determine the direction of the FDEV trigger. FDEV_DIR_DPLLx = 0 means positive, FDEV_DIR_DPLLx = 1 means negative. In this way, the GPIO pins will function as the FINC or FDEC input. The minimum positive pulse width applied to the trigger pins should be greater than 100 ns to be captured by the internal sampling clock. The DCO update rate should be limited to less than 5 MHz when using pin control.

When DCO control is disabled (DPLLx_FB_FDEV_EN = 0), the DCO frequency offset will be cleared and the VCO output frequency will be determined by the original numerator value of the DPLL fractional feedback divider.

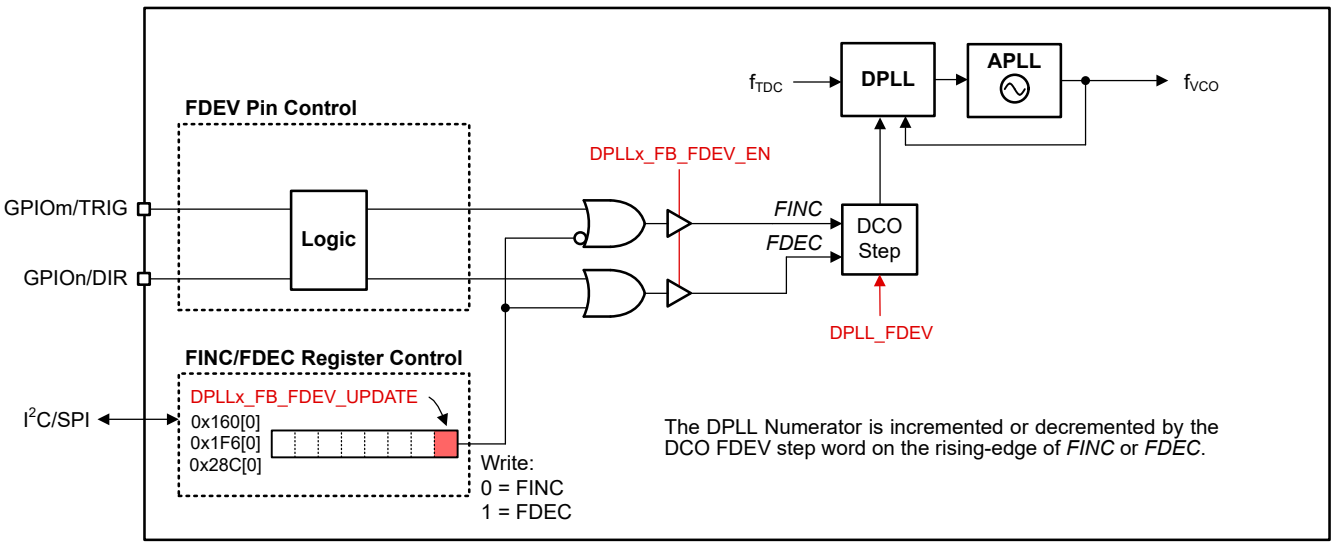


図 8-39. DCO Mode Control Options

8.4.4.1.1 DPLL DCO Relative Adjustment Frequency Step Size

式 11 shows the formula to compute the DPLLx_FB_FDEV register value required to meet the specified DCO frequency step size in ppb (part-per-billion) when DCO mode is enabled for the DPLL.

$$DPLLx\_FB\_FDEV = (Reqd\_ppb / 10^9) \times DPLL_{DEN} \times f_{VCOx} / f_{TDCx} \quad (11)$$

where

- DPLLx_FB_FDEV: Frequency deviation value (0 to 2^{38}– 1)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- $DPLL_{DEN}$: DPLL FB divider denominator value (1 to 2^{40}, register value of 0 = 2^{40})
- f_{VCOx}: VCOx frequency
- f_{TDCx}: TDCx frequency

8.4.4.1.2 APLL DCO Frequency Step Size

Users must write to the DPLLx_FREE_RUN register field to adjust the APLL DCO. When DPLLx_HIST_EN = 1, the relative adjustments are performed. When DPLLx_HIST_EN = 0 the DPLLx_FREE_RUN value is used for the APLLx DCO numerator. The effective APLLx numerator can be read back from APLLx_NUM_STAT.

式 12 shows the formula to compute the DPLLx_FREE_RUN field value required to meet the specified DCO frequency step size in ppb (part-per-billion) when relative APLL DCO mode is enabled. DPLLx_FREE_RUN is a signed value and the actual programmed value for a negative number can be calculated as the 2s complement.

$$DPLLx\_FREE\_RUN = (Reqd\_ppb / 10^9) \times APLLx_{DEN} \times f_{VCOx} / f_{PDFx} \quad (12)$$

where

- DPLLx_FREE_RUN: Frequency deviation value (–2^{39} to 2^{39}– 1)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- $APLLx_{DEN}$: APLL FB divider denominator value (2^{40})
- f_{VCOx}: VCOx frequency
- f_{PDFx}: PLLx phase detector frequency

8.4.5 APLL Frequency Control

The device can also support APLL frequency and phase control through writing the 40-bit register DPLLx_FREE_RUN[39:0] while the DPLL is in holdover or not used. If the reference clock in a free-run mode or disabled, DPLL will disconnect with APLL, but users can still adjust frequency and phase accuracy.

To enable APLL DCO control, set DPLLx_LOOP_EN = 1, and PLLx_MODE = 1 for 40-bit fractional denominator. DPLLx_EN may be set = 0.

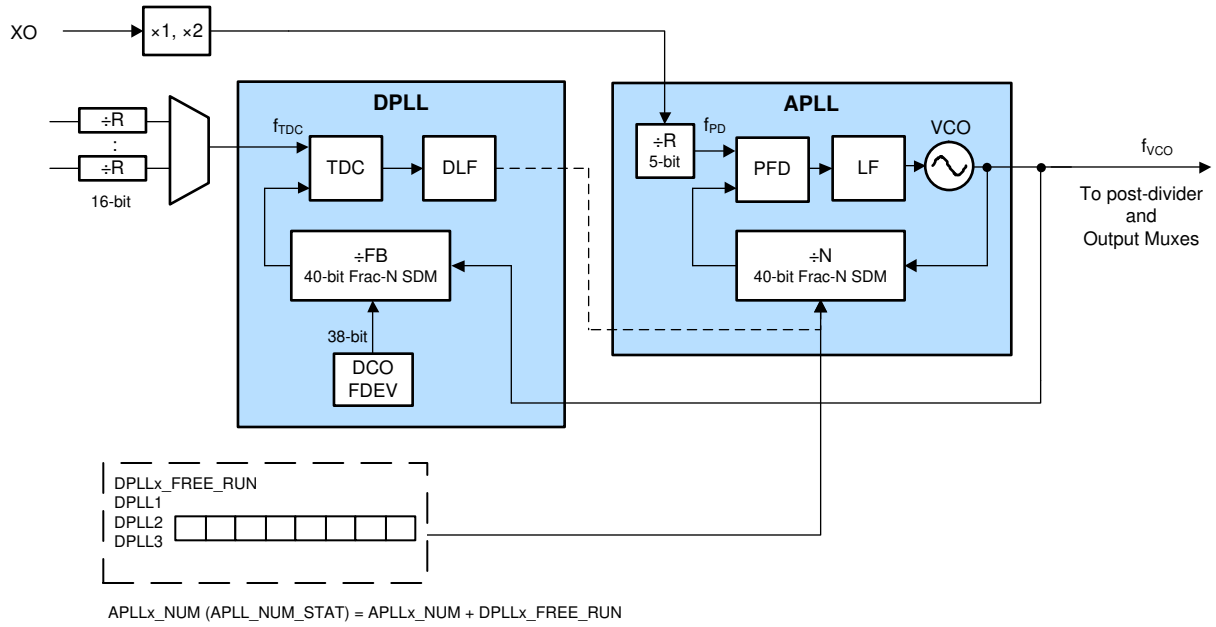


図 8-40. APLL DCO Mode

There are two alternative methods in adjusting the APLL DCO.

- Absolute frequency adjustment
  - Set DPLLx_HIST_EN = 0
  - Effective APLLx_NUM (APLLx_NUM_STAT) = APLLx_NUM + DPLLx_FREE_RUN
    - The APLLx_NUM_STAT is a read-only register and can be read back.
    - The DPLL loop filter block will modify the APLLx_NUM_STAT based on DPLLx_FREE_RUN value.
  - DPLLx_FREE_RUN is a 40-bit 2s complement number
- Relative frequency adjustment
  - Set DPLLx_HIST_EN = 1
  - DPLLx_FREE_RUN value is fed into the APLLx_NUM at a controlled rate defined by a step size register and step period register.
  - If another DPLLx_FREE_RUN write occurs before the LMK is complete in making the last adjustment, any remaining steps are lost and the new value begins to feed the APLL numerator.
  - A flag is set when the DPLLx_FREE_RUN word is fully fed into the effective APLLx_NUM (APLL_NUM_STAT).

8.4.6 Zero-Delay Mode Synchronization

The DPLL supports an internal zero-delay mode (ZDM) synchronization option to achieve a known and deterministic phase relationship between the selected DPLL reference input and OUT0, OUT4, or OUT10 clock depending on configuration and selected DPLL for ZDM. See *Zero-Delay Mode (ZDM)*.

8.4.7 DPLL Programmable Phase Delay

Users may write to the DPLLx_PH_OFFSET[44:0] register fields to adjust the DPLL phase offset. The phase offset is a signed 2-s complement value with a default setting of 0 and offsets the phase relationship of the

feedback clock to reference clock at the TDC. The phase adjustment is common to all outputs derived from the DPLLx synchronization domain.

式 13 shows the formula to compute the DPLLx_PH_OFFSET field value to vary the output phase in fine adjustment steps. DPLLx_PH_OFFSET is related to the APLLx VCO period with a scaling factor for decimation and digital gain.

$$DPLLx\_PH\_OFFSET = (Desired\_Phase\_Offset \times f_{VCOx} \times 2 \times SCALING_{DEC} \quad (13)$$

where

- DPLLx_PH_OFFSET: Programmable register value adjusting DPLL output phase
- Desired_Phase_Offset: Desired DPLL phase adjustment step size (in seconds)
- f_{VCOx}: VCOx frequency
- $SCALING_{DEC}$: Scaling factor accounting for decimation and digital gain components (2 +1) × 958 = 2874

For example, if the user wants to introduce a phase offset of 38.5 ps into the DPLL3/APLL3 synchronization domain

- Desired_Phase_Offset = 38.5 ps
- f_{VCOx}: = 2500 MHz
- $SCALING_{DEC}$ = 2874
- DPLL_PH_OFFSET = 38.5e-12 × 2500e6 × 2 x 2874 = 558

8.5 Programming

8.5.1 Interface and Control

A system host device (MCU or FPGA) can use either I²C or SPI to access the register. The register configurations are the same for I²C and SPI. The device can be initialized, controlled, and monitored through register access during normal operation (when PD# is deasserted). Some device features can also be controlled and monitored through the external logic control and status pins. A 2-byte address and 1-byte data interface is used.

8.5.2 I²C Serial Interface

When (GPIO1 = 0), the device operates as an I²C client and supports bus rates of 100 kHz (standard mode) and 400 kHz (fast mode). Slower bus rates can work as long as the other I²C specifications are met. When operating with I²C communication interface the SCS_ADD pin selects one of three LSBs for the I²C device address. GPIO0 and GPIO2 input states determine device settings to load from ROM.

When using I²C communication the LMK5B33414 can support up to three different I²C addresses depending on the state of the CSC_ADD pin on power up, or any I²C address if the user re-programs the EEPROM. The five MSBs of the 7-bit I²C address are initialized from the EEPROM and the two LSBs are defined by the SCS_ADD pin state. 表 8-6 shows the default EEPROM results in the I²C addresses.

表 8-6. I²C Addresses

SCS_ADD PIN STATE	I²C ADDRESS LSB	I²C ADDRESS
Low	0	0x64
Vmid	2	0x66
High	1	0x65

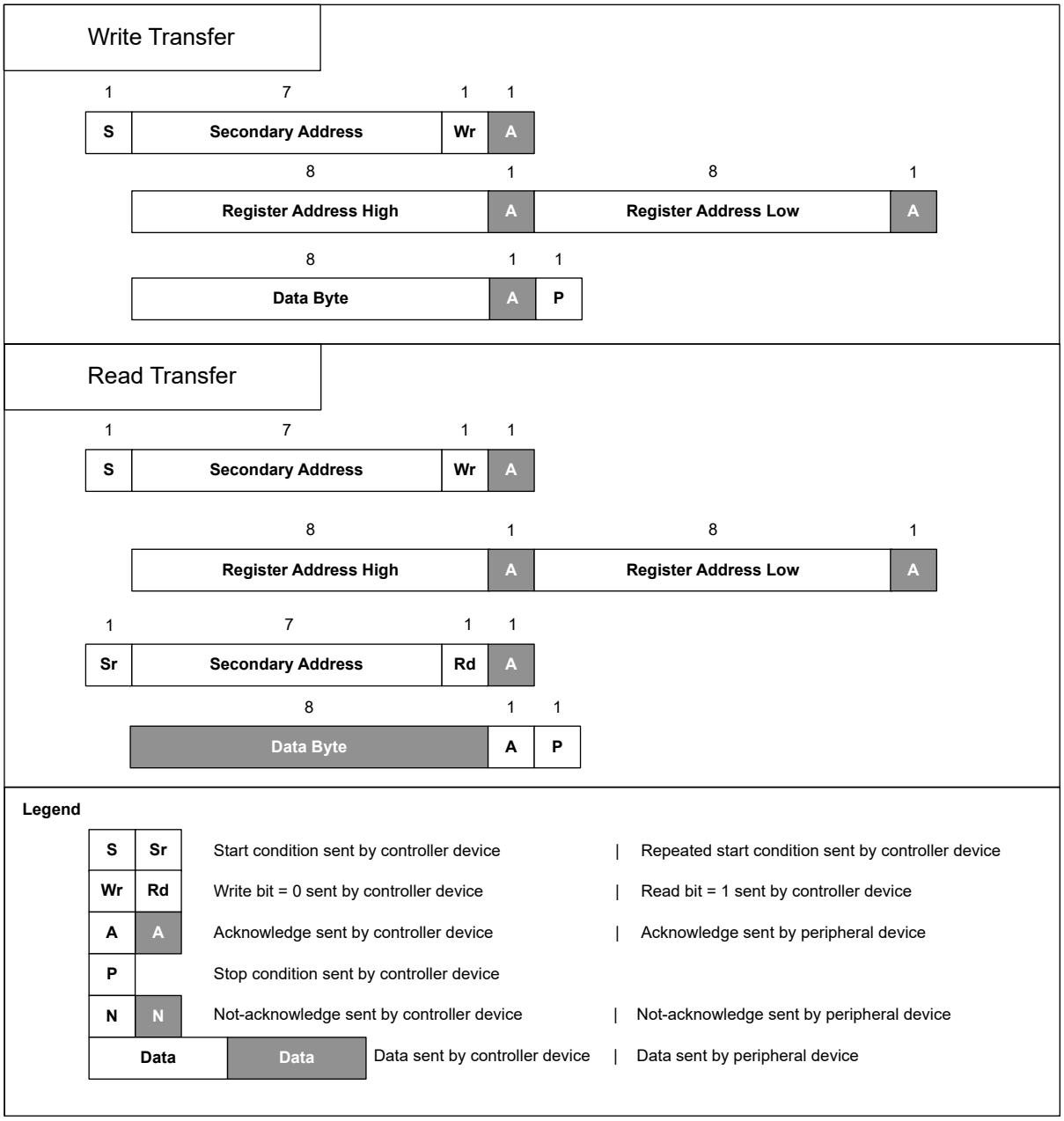


図 8-41. I²C Byte Write and Read Transfers

8.5.2.1 I²C Block Register Transfers

図 8-42 shows that the device supports I²C block write and block read register transfers.

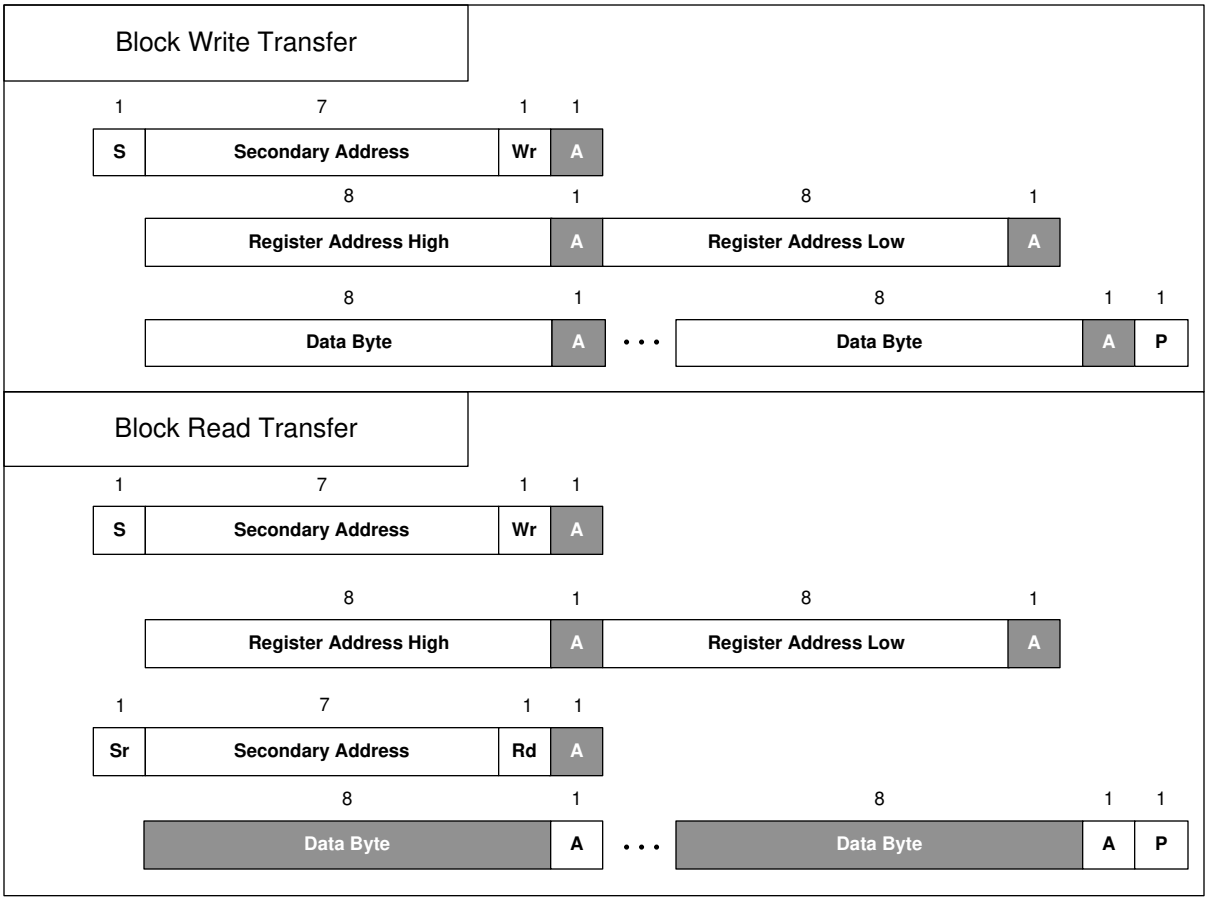


図 8-42. I²C Block Register Transfers

8.5.3 SPI Serial Interface

When SPI control interface is selected, the device uses a 3-wire SPI interface with SDIO, SCK, and SCS signals (SPI_3WIRE_DIS = 0). When using SPI interface SCS_ADD also can act as a Time Elapsed Counter (TEC) trigger. When set SPI_3WIRE_DIS = 1, any GPIO may be selected as SDO to support readback with 4-wire SPI.

The host device must present data to the device MSB first. A message includes a transfer direction bit ($\overline{W}$/R), a 15-bit address field (A14 to A0), and a 8-bit data field (D7 to D0) as shown in 図 8-43. The $\overline{W}$/R bit is 0 for a SPI write and 1 for a SPI read.

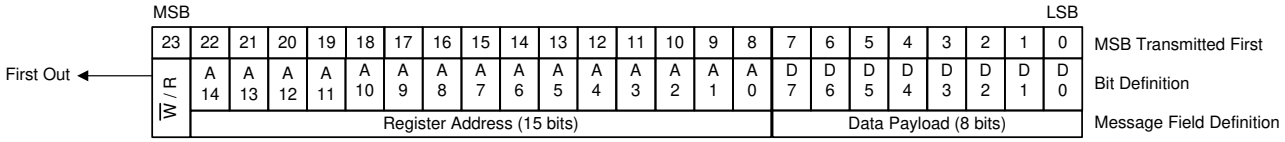


図 8-43. SPI Message Format

A message frame is initiated by asserting SCS low. The frame ends when SCS is deasserted high. The first bit transferred is the $\overline{W}$/R bit. The next 15 bits are the register address, and the remaining eight bits are data. On write transfers, data is committed in bytes as the final data bit (D0) is clocked in on the rising edge of SCK. If the write access is not an even multiple of eight clocks, the trailing data bits are not committed. On read transfers, data bits are clocked out from the SDO pin on the falling edges of SCK.

8.5.3.1 SPI Block Register Transfer

8.5.4 Register Map Generation

The TICS Pro software tool for EVM programming has a step-by-step design flow to enter the user-selected clock design parameters, calculate the frequency plan, and generate the device register settings for the desired configuration. The register map data (registers hex dump in text format) can be exported to enable host programming of the device on start-up.

8.5.5 General Register Programming Sequence

For applications that use a system host to program the initial configuration after power up, this general procedure can be followed from the register map data generated and exported from TICS Pro:

1. Apply power to the device to start in I^2C or SPI mode.
2. Write the register settings exported from TICS Pro while applying the following register mask (do not modify mask bits = 1):
   - Mask R23 = 0xFF (Device reset/control register)
3. Write 1 to R21[6] to assert SYNC. Clocks which should not be synced should have the SYNC functionality in their divider path disabled.
4. Write 0 to R21[6] to deassert SYNC and release all clocks to start-up synchronized.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Device Start-Up Sequence

図 8-36 and 図 8-38 show the device start-up sequence.

9.1.2 Power Down (PD#) Pin

The PD# pin (active low) can be used for device power down and used to initialize the POR sequence. When PD# is pulled low, the entire device is powered down and the serial interface is disabled. When PD# is pulled high, the device POR sequence is triggered to begin the device start-up sequence and normal operation as depicted in 図 8-36. If the PD# pin is toggled to issue a momentary hard-reset, the negative pulse applied to the PD# pin should be greater than 200 ns to be captured by the internal digital system clock.

表 9-1. PD# Control

PD# PIN STATE	DEVICE OPERATION
0	Device is disabled
1	Normal operation

9.1.3 Strap Pins for Start-Up

At start-up, voltage level on GPIOs determine the operation mode of the device. GPIO1 selects SPI or I^2C mode. GPIO2 and GPIO0 select ROM page.

9.1.4 Pin States

表 9-2 shows the different pin states of the device.

表 9-2. Pin States in Different Stages

PIN NAME	POWER DOWN	STATES	POR (SPI)	STATES	POR (I^2C)	STATES	NORMAL OPERATION	STATES	SOFT RESET	STATES
PD#	LOW	2-level input	PD# transitions LOW to HIGH		PD# transitions LOW to HIGH		HIGH	2-level input	HIGH	2-level input
GPIO0	Ready for POR	3-level input	EEPROM/ ROM select	3-level input	EEPROM/ ROM select	3-level input	See table	GPIO	N/A	
GPIO1	Ready for POR	2-level input	VDD	2-level input	GND	2-level input	See table	GPIO	N/A	
GPIO2	Ready for POR	3-level input	EEPROM/ ROM select	3-level input	EEPROM/ ROM select	3-level input	See table	GPIO	N/A	
SCS_A DD	Ready for POR	3-level input	SCS	2-level input	I^2C address select	3-level input	2-level or 3-level input based on POR		N/A	
SDIO	N/A		SDIO	Data I/O	SDA	Data I/O	SDIO or SDA control interface serial data input/ output based on POR			

表 9-2. Pin States in Different Stages (continued)

PIN NAME	POWER DOWN	STATES	POR (SPI)	STATES	POR (I^2C)	STATES	NORMAL OPERATION	STATES	SOFT RESET	STATES
SCK	N/A		SCK	Clock input	SCL	Clock input	SCK or SCL control interface serial clock input based on POR			

9.1.5 ROM and EEPROM

Some applications need start-up clocks to operate their entire system at power on. Others may need only a valid clock for the logic device (CPU, ASIC, or FPGA) at power on which may then program the LMK5B33414 with custom settings if the default ROM configuration does not meet the application requirements. The LMK5B33414 provides ROM pages to support default output clocks on start-up and an EEPROM to allow customization of the start-up clocks if the ROM pages do not meet the application requirements. See *ROM Selection* and *EEPROM Overlay* for more information.

9.1.6 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains

9.1.6.1 Power-On Reset (POR) Circuit

The LMK5B33414 integrates a built-in power-on reset (POR) circuit that holds the device in reset until all of the following conditions have been met:

- All V_{DD} core supplies have ramped above 2.72 V
- PD# pin has ramped above 1.2 V (minimum V_{IH})

9.1.6.2 Powering Up From a Single-Supply Rail

As long as all VDD and VDDO supplies are driven by the same 3.3-V supply rail that ramp in a monotonic manner from 0 V to 3.135 V, and the time between decision point 2 and stabilized supply voltage is less than 1 ms, then there is no requirement to add a capacitor on the PD# pin to externally delay the device power-up sequence. 図 9-1 shows that the PD# pin can be left floating or otherwise driven by a system host to meet the clock sequencing requirements in the system.

If time between decision point 2 and stabilized supply voltage is greater than 1 ms, then the PD# pin must be delayed. Refer to *Power Up From Split-Supply Rails*.

As described in *Slow or Delayed XO Start-Up*, it is necessary for the XO reference to be valid after PD# decision point 1 to ensure successful VCO1 and VCO2 calibration.

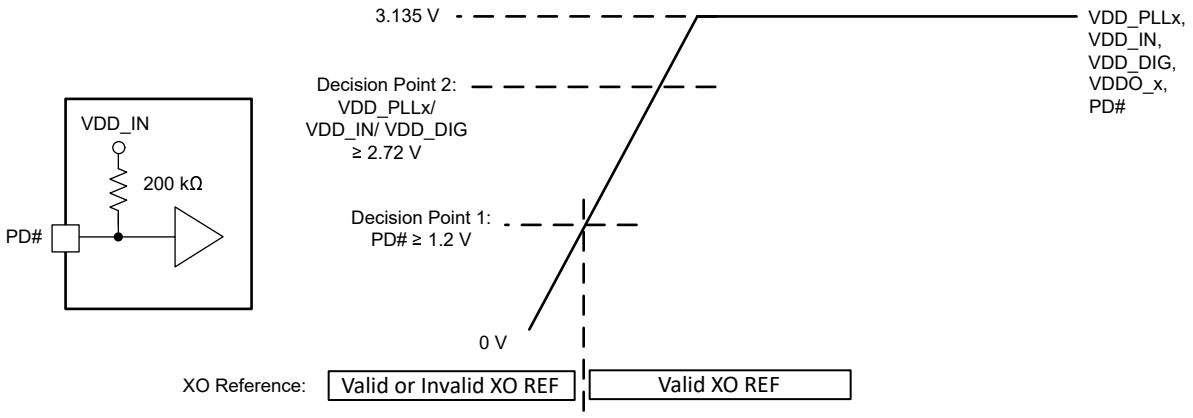


図 9-1. Recommendation for Power Up From a Single-Supply Rail

9.1.6.3 Power Up From Split-Supply Rails

If VDD or VDDO supplies are driven from different supply sources, TI recommends to start the PLL calibration after all of the supplies have ramped above 3.135 V. This can be realized by delaying the PD# low-to-high transition. The PD# input incorporates a 200-kΩ resistor to VDD_IN and as shown in 図 9-2. A capacitor from the PD# pin to GND can be used to form an RC time constant with the internal pullup resistor. This RC time constant

can be designed to delay the low-to-high transition of PD# until all the core supplies have ramped above 3.135 V. TI recommends to ramp up VDDO supply pins before VDD supply pins.

Alternatively, the PD# pin can be driven high by a system host or power management device to delay the device power-up sequence until all supplies have ramped.

As described in *Slow or Delayed XO Start-Up*, it is necessary for the XO reference to be valid after PD# decision point 2 to ensure successful APLL1/VCO1 and APLL2/VCO2 calibration, or DPLL3 valid reference.

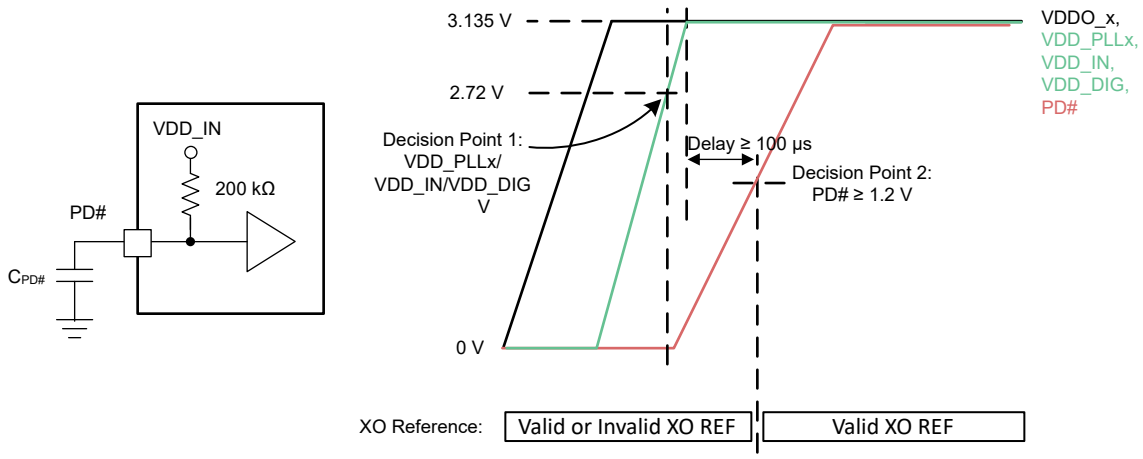


図 9-2. Recommendation for Power Up From Split-Supply Rails

9.1.6.4 Non-Monotonic or Slow Power-Up Supply Ramp

In case the VDD core supplies ramp with a non-monotonic manner or with a slow ramp time from 0 V to 3.135 V of over 100 ms, TI recommends to delay the VCO calibration until after all of the core supplies have ramped above 3.135 V. This could be achieved by delaying the PD# low-to-high transition with one of the methods described in *Power Up From Split-Supply Rails*.

If any core supply cannot ramp above 3.135 V before the PD# low-to-high transition, it is acceptable to issue a device soft-reset after all core supplies have ramped to manually trigger the VCO calibration and PLL start-up sequence.

9.1.7 Slow or Delayed XO Start-Up

Because the external XO clock input is used as the reference input for the APLL1/VCO1 and APLL2/VCO2 calibration, the XO input amplitude and frequency must be stable before the start of VCO calibration to ensure successful PLL lock and output start-up. If the XO clock is not stable prior to VCO calibration, the VCO calibration can fail and prevent PLL lock and output clock start-up.

If the XO clock has a slow start-up time or has glitches on power-up (due to a slow or non-monotonic power supply ramp, for example), TI recommends to delay the start of VCO calibration until after the XO is stable. This could be achieved by delaying the PD# low-to-high transition until after the XO clock has stabilized using one of the methods described in *Power Up From Split-Supply Rails*. It is also possible to issue a device soft-reset after the XO clock has stabilized to manually trigger the VCO calibration and PLL start-up sequence.

APLL3/VCO3 is factory calibrated and is not sensitive to an invalid XO reference start-up. Upon valid XO reference, APLL3/VCO3 will be able to acquire lock. When APLL3/VCO3 is used in conjunction with DPLL3, it is necessary for the XO to be valid before a DPLL3 reference is validated.

9.2 Typical Application

図 9-3 shows a reference schematic to help implement the LMK5B33414 and its peripheral circuitry. Power filtering examples are given for the core supply pins and independent output supply pins. Single-ended LVCMOS, LVDS, HSDS, LVPECL, and HCSL clock interfacing examples are shown for the clock input and output pins. An external CMOS oscillator drives an AC-coupled voltage divider network as an example to interface the 3.3-V LVCMOS output to meet the input voltage swing specified for the XO input. The XO pin of the LMK5B33414 can accept 3.3-V LVCMOS input. The required external capacitors are placed close to the LMK5B33414 and are shown with the suggested values. External pullup and pulldown resistor options at the logic I/O pins set the default input states. The I^2C or SPI pins and other logic I/O pins can be connected to a host device (not shown) to program and control the LMK5B33414 and monitor its status.

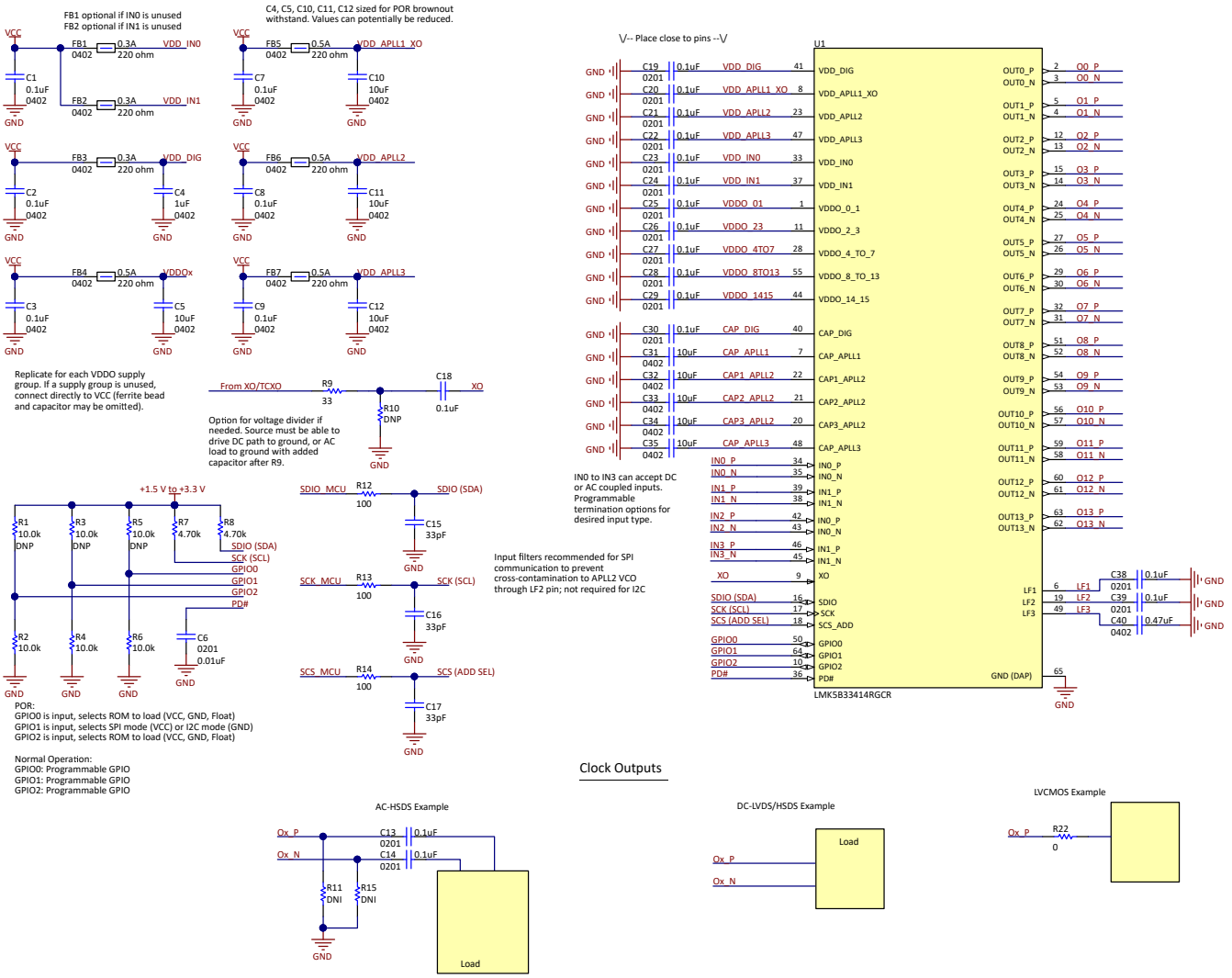


図 9-3. Reference Schematic Example

9.2.1 Design Requirements

In a typical application, consider the following design requirements or parameters to implement the overall clock solution:

1. Device initial configuration. The device should be configured as either host programmed (MCU or FPGA) or factory pre-programmed.
2. Device interface, set GPIO1 as desired for I^2C or SPI communications interface.
3. XO frequency, signal type, and frequency accuracy and stability. Consider a high-stability TCXO or OCXO for the XO input if any of the following is required:
   - Standard-compliant frequency stability (such as SyncE, SONET/SDH, IEEE 1588)
   - Lowest possible close-in phase noise at offsets ≤ 100 Hz
   - Narrow DPLL bandwidth ≤ 10 Hz
4. For each DPLL/APLL domain, determine the following:
   - Input clocks: frequency, buffer mode, priority, and input selection mode
   - APLL reference: another VCO with Cascaded mode, or XO for Non-cascaded mode
   - Output clocks: frequency, buffer mode
   - DPLL loop bandwidth and maximum TDC frequency
   - If the DCO Mode or Zero-Delay Mode is required
5. Input clock and PLL monitoring options
6. Status outputs and interrupt flag
7. Power supply rails

9.2.2 Detailed Design Procedure

In a typical application, TI recommends the following steps:

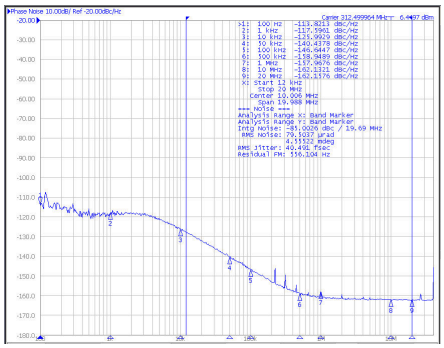
1. Use the device GUI in the TICS Pro programming software for a step-by-step design flow to enter the design parameters, calculate the frequency plan for each PLL domain, and generate the register settings for the desired configuration. The register settings can be exported (registers hex dump in txt format) to enable host programming.
   - A host device can program the register settings through the serial interface after power-up and issue a soft-reset (by SWRST bit) to start the device. Set SW_SYNC before, and clear after SWRST.
2. Tie the GPIO1 pin to ground to select the I^2C communications interface, or pull up GPIO1 high to VDD_DIG through an external resistor to select the SPI communications interface. Determine the logic I/O pin assignments for control and status functions. See 図 8-36.
   - Connect I^2C/SPI and logic I/O pins (1.8-V compatible levels) to the host device pins with the proper I/O direction and voltage levels.
3. Select an XO frequency by following *Oscillator Input (XO)*.
   - Choose an XO with target phase jitter performance that meets the frequency stability and accuracy requirements required for the output clocks during free-run or holdover.
   - For a 3.3-V LVCMOS driver, LMK5B33414 can accept it directly. Power the XO from a low-noise LDO regulator or optimize its power filtering to avoid supply noise-induced jitter on the XO clock.
   - **TICS Pro:** Configure the XO frequency to match the XO port input.

4. Wire the clock I/O for each APLL domain in the schematic and use TICS Pro to configure the device settings as follows:
   - Reference inputs: Follow the LVCMOS or differential clock input interface examples in 図 9-3 or セクション 8.3.3.
     - **TICS Pro:** For DPLL mode, configure the reference input buffer modes to match the reference clock driver interface requirements. See *Reference Inputs*.
   - **TICS Pro:** For DPLL mode, configure the DPLL input selection modes and input priorities. See *Reference Input Mux Selection*.
   - **TICS Pro:** Configure each APLL reference from other VCO domain (Cascaded mode) or XO clock (Non-cascaded mode).
   - **TICS Pro:** Configure each output with the required clock frequency and APLL domain. TICS Pro can calculate the VCO frequencies and divider settings for the APLL and outputs. Consider the following output clock assignment guidelines to minimize crosstalk and spurs:
     - OUT[0:1] bank can select any APLL clocks, XO, and references.
     - OUT[2:3] bank is preferred for APLL1 or APLL2 clocks.
     - OUT[4:7] bank is preferred for APLL2 or APLL3 clocks.
     - OUT[8:13] bank is preferred for APLL3 or APLL2 clocks.
     - Group identical output frequencies (or harmonic frequencies) on adjacent channels, and use the output pairs with a single divider (for example, OUT2/3) when possible to minimize power.
     - Separate clock outputs when the difference of the two frequencies, $|f_{OUTx} – f_{OUTy}|$, falls within the jitter integration bandwidth (for example, 12 kHz to 20 MHz). Any outputs that are potential aggressors should be separated by at least four static pins (power pin, logic pin, or disabled output pins) to minimize potential coupling. If possible, separate these clocks by the placing them on opposite output banks, which are on opposite sides of the chip for best isolation.
     - Avoid or isolate any LVCMOS output (strong aggressor) from other jitter-sensitive differential output clocks. If an LVCMOS output is required, use dual complementary LVCMOS mode (+/- or -/+) with the unused LVCMOS output left floating with no trace.
     - If not all outputs pairs are used in the application, consider connecting an unused output to a pair of RF coaxial test structures for testing purposes (such as SMA, SMP ports).
   - **TICS Pro:** Configure the output drivers.
     - Configure the output driver modes to match the receiver clock input interface requirements. See *Clock Outputs (OUTx_P/N)*.
     - Configure any output SYNC groups that need their output phases synchronized. See *Output Synchronization (SYNC)*.
     - Configure the output auto-mute modes, and APLL and DPLL mute options. See *Output Auto-Mute During LOL*.
   - Clock output Interfacing: Follow the single-ended or differential clock output interface examples in 図 9-3 or *Clock Output Interfacing and Termination*.
     - Differential outputs can be AC-coupled and terminated and biased at the receiver inputs, or DC-coupled with proper receivers
     - LVCMOS outputs have internal source termination to drive 50-Ω traces directly. LVCMOS V_{OH} level is determined by internal LDO programmed voltage (1.8 V or 2.65 V).
   - **TICS Pro:** Configure the DPLL loop bandwidth.
     - Below the loop bandwidth, the reference noise is added to the TDC noise floor and the XO/TCXO/OCXO noise. Above the loop bandwidth, the reference noise will be attenuated with roll-off up to 60 dB/decade. The optimal bandwidth depends on the relative phase noise between the reference input and the XO. APLL's loop bandwidth can be configured to provide additional attenuation of the reference input, TDC, and XO phase noise above APLL's bandwidth.
   - **TICS Pro:** Configure the maximum TDC frequency to optimize the DPLL TDC noise contribution for the desired use case.
     - *Wired*: A 400 kHz maximum TDC rate is commonly specified. This supports SyncE and other use cases using a narrow loop bandwidth (≤10 Hz) with a TCXO/OCXO/XO to set the frequency stability and wander performance.

  - *Wireless*: A 26 MHz maximum TDC rate is commonly specified for lowest in-band TDC noise contribution. This supports wireless and other use cases where close-in phase noise is critical.
- **TICS Pro:** If clock steering is needed (such as for IEEE 1588 PTP), enable DCO mode for the DPLL loop and enter the frequency step size (in ppb). The FDEV step register will be computed according to *APLL DCO Frequency Step Size*. Enable the FDEV_TRIG and FDEV_DIR pin control on the GPIO pins if needed.
- **TICS Pro:** If deterministic input-to-output clock phase is needed, enable the ZDM as required on OUT0, OUT4, or OUT10. See *Zero-Delay Mode (ZDM)*.

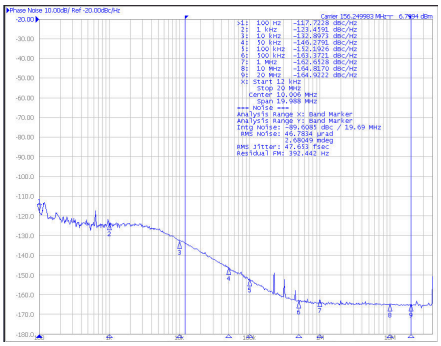
5. **TICS Pro:** Configure the reference input monitoring options for each reference input. Disable the monitor when not required or when the input operates beyond the monitor's supported frequency range. See *Reference Input Monitoring*.
   - *Frequency monitor*: Set the valid and invalid thresholds (in ppm).
   - *Missing pulse monitor*: Set the late window threshold (T_{LATE}) to allow for the longest expected input clock period, including worst-case cycle-to-cycle jitter. For a gapped clock input, set T_{LATE} based on the number of allowable missing clock pulses.
   - *Runt pulse monitor*: Set the early window threshold (T_{EARLY}) to allow for the shortest expected input clock period, including worst-case cycle-to-cycle jitter.
   - *1-PPS Phase validation monitor*: Set the phase validation jitter threshold, including worst-case input cycle-to-cycle jitter.
   - *Validation timer*: Set the amount of time the reference input must be qualified by all enabled input monitors before the input is valid for selection.
6. **TICS Pro:** Configure the DPLL lock detect and tuning word history monitoring options for each channel. See *PLL Lock Detectors* and *Tuning Word History*.
   - *DPLL frequency lock and phase lock detectors*: Set the lock and unlock thresholds for each detector.
7. **TICS Pro:** Configure each status output pin and interrupt flag as needed. See *Status Outputs* and *Interrupt*.
   - Select the desired status signal selection, status polarity, and driver mode (3.3-V LVCMOS or open-drain). Open-drain requires an external pullup resistor.
   - If the Interrupt is enabled and selected as a status output, configure the flag polarity and the mask bits for any interrupt source, and the combinational OR gate, as needed.
8. Consider the following guidelines for designing the power supply:
   - Outputs with identical frequency or integer-related (harmonic) frequencies can share a common filtered power supply.
     - Example: 156.25-MHz and 312.5-MHz outputs on OUT[4:5] and OUT[6:7] can share a filtered VDDO supply, while 100-MHz, 50-MHz, and 25-MHz outputs on OUT[0:1] and OUT[2:3] can share a separate VDDO supply.
   - See *Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains*.

9.2.3 Application Curves



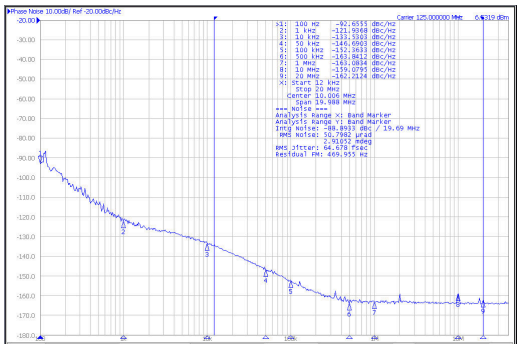
Jitter = 41 fs RMS (12 kHz to 20 MHz)
f_{APLL3} =2500 2500 MHz (APLL3 post-divider = 8)

図 9-4. 312.5 MHz Output Phase Noise (APLL3 BAW)



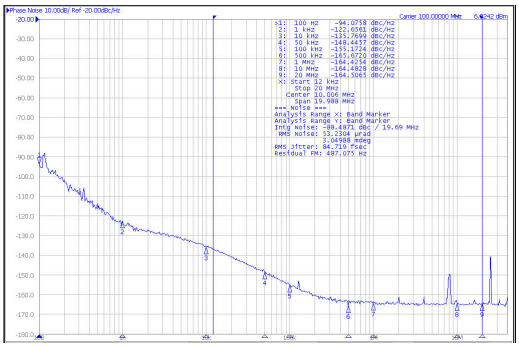
Jitter = 47 fs RMS (12 kHz to 20 MHz)
f_{APLL3} =2500 MHz (APLL3 post-div = 8, div2 enabled)

図 9-5. 156.25-MHz Output Phase Noise (APLL3 BAW)



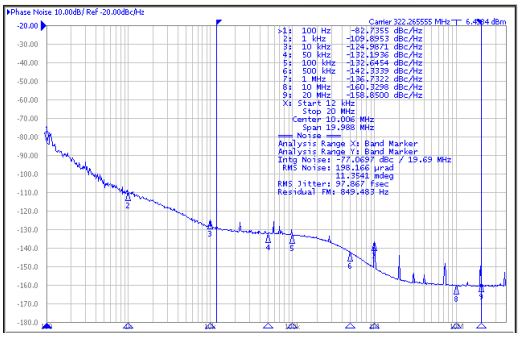
Jitter = 65 fs RMS (12 kHz to 20 MHz)
f_{APLL3} =2500 MHz (APLL3 post-div = 5, Channel-div = 4)

図 9-6. 125-MHz Output Phase Noise (APLL3 BAW)



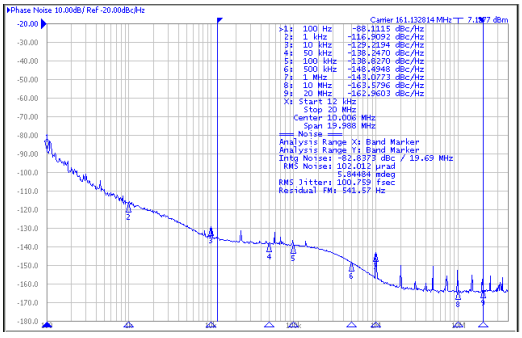
Jitter = 85 fs RMS (12 kHz to 20 MHz)
f_{APLL3} =2500 MHz (APLL3 post-div = 5, Channel-div = 5)

図 9-7. 100-MHz Output Phase Noise (APLL3 BAW)



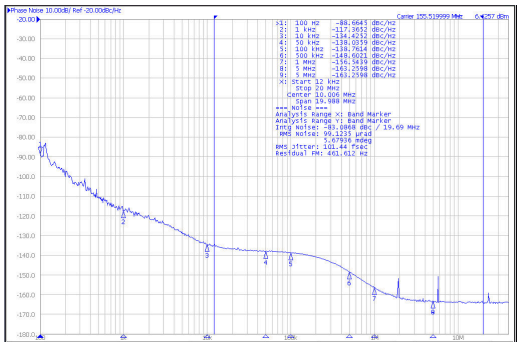
Jitter = 97 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5800.78125 MHz

図 9-8. 322.265625 MHz Output Phase Noise (APLL2)



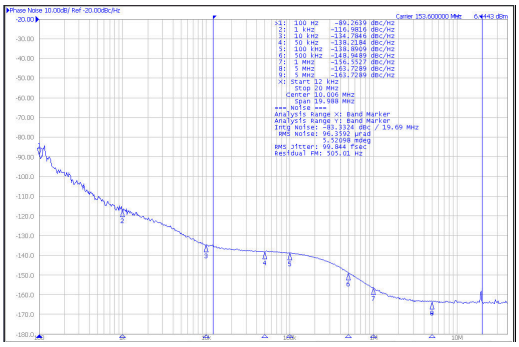
Jitter = 105 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5800.78125 MHz

図 9-9. 161.1328125-MHz Output Phase Noise (APLL2)



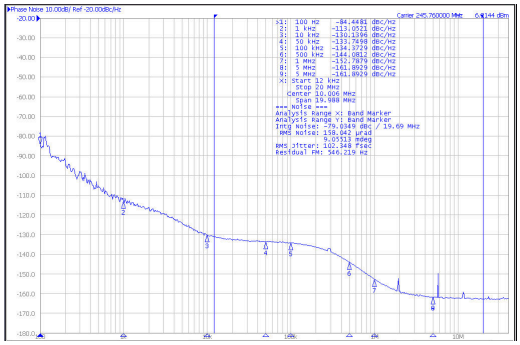
Jitter = 101 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5598.72 MHz

図 9-10. 155.52 MHz Output Phase Noise (APLL2)



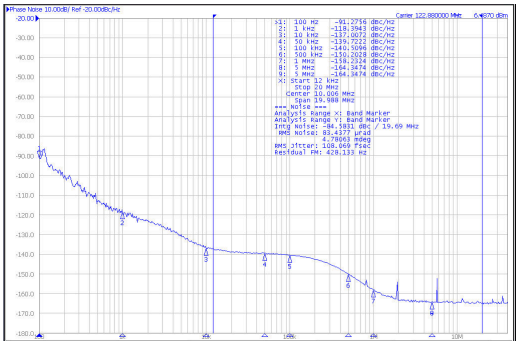
Jitter = 100 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5836.8 MHz

図 9-11. 153.6 MHz Output Phase Noise (APLL2)



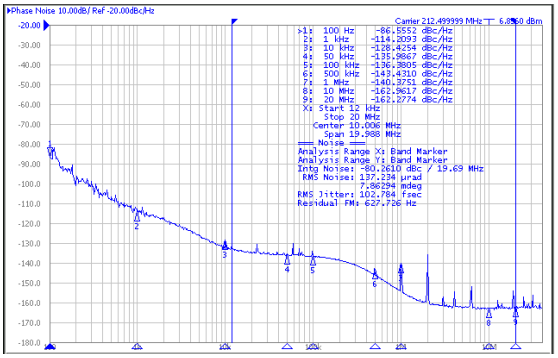
Jitter = 102 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5898.24 MHz

図 9-12. 245.76-MHz Output Phase Noise (APLL2)



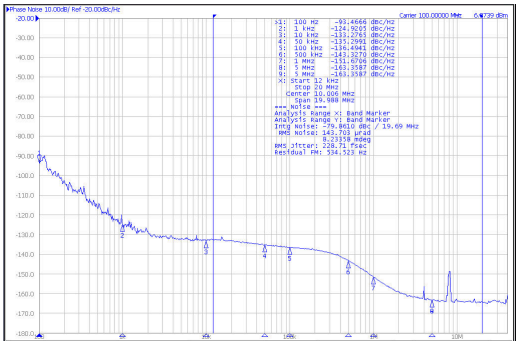
Jitter = 109 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5898.24 MHz

図 9-13. 122.88 MHz Output Phase Noise (APLL2)



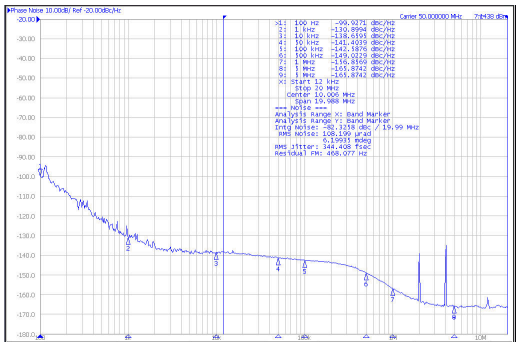
Jitter = 103 fs RMS (12 kHz to 20 MHz)
f_{APLL2} = 5950 MHz

図 9-14. 212.5-MHz Output Phase Noise (APLL2)



Jitter = 230 fs RMS (12 kHz to 20 MHz)
f_{APLL1} = 5200 MHz

図 9-15. 100 MHz Output Phase Noise (APLL1)



Jitter = 345 fs RMS (12 kHz to 20 MHz)
f_{APLL1} = 5200 MHz

図 9-16. 50-MHz Output Phase Noise (APLL1)

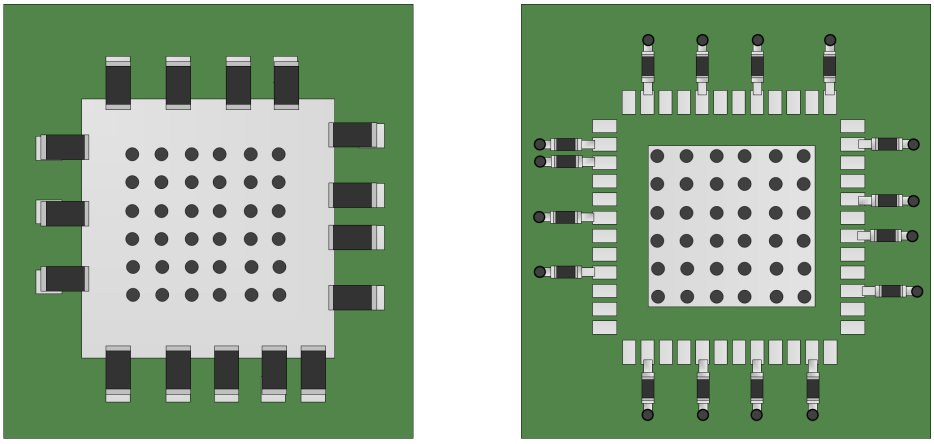
9.3 Do's and Don'ts

- Power all the VDD pins with proper supply decoupling and bypassing connect as shown in 図 9-3.
- Power down unused blocks through registers to minimize power consumption.
- Use proper source or load terminations to match the impedance of input and output clock traces for any active signals to/from the device.
- Leave unused clock outputs floating and powered down through register control.
- Leave unused clock inputs floating.
- If needed, external biasing resistors (10-kΩ pullup to 3.3 V or 10-kΩ pulldown) can be connected on each GPIO pin to select device operation mode during POR.
- Consider routing each GPIO pin to a test point or high-impedance input of a host device to monitor device status outputs.
- Consider using a LDO regulator to power the external XO/TCXO/OCXO source.
  - High jitter and spurious on the oscillator clock are often caused by high spectral noise and ripple on its power supply.
- Include dedicated header or test points to access the I^2C or SPI interface of the device, as well as a ground connection.
  - This can enabled off-board programming for device bring-up, prototyping, and diagnostics using the TI USB2ANY interface and TICS Pro software tools.

9.4 Power Supply Recommendations

9.4.1 Power Supply Bypassing

図 9-17 shows two general placements of power supply bypass capacitors on either the back side or the component side of the PCB. If the capacitors are mounted on the back side, 0402 components can be employed. For component side mounting, use 0201 body size capacitors to facilitate signal routing. A combination of component side and back side placement can be used. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.



(**Does not** indicate actual location of the device supply pins)

図 9-17. Generalized Placement of Power Supply Bypass Capacitors

9.5 Layout

9.5.1 Layout Guidelines

- Isolate input, XO/OCXO/TCXO and output clocks from adjacent clocks with different frequencies and other nearby dynamic signals.
- Consider the XO/OCXO/TCXO placement and layout in terms of the supply/ground noise and thermal gradients from nearby circuitry (for example, power supplies, FPGA, ASIC) as well as system-level vibration and shock. These factors can affect the frequency stability/accuracy and transient performance of the oscillator.
- Avoid impedance discontinuities on controlled-impedance 50-Ω single-ended (or 100-Ω differential) traces for clock and dynamic logic signals.
- Place bypass capacitors close to the VDD and VDDO pins on the same side as the IC, or directly below the IC pins on the opposite side of the PCB. Larger decoupling capacitor values can be placed further away.
- Place external capacitors close to the CAP_x and LFx pins.
- Use multiple vias to connect wide supply traces to the respective power islands or planes if possible.
- Use at least a 6×6 through-hole via pattern to connect the IC ground/thermal pad to the PCB ground planes.
- See the Land Pattern Example, Solder Mask Details, and Solder Paste Example in *Mechanical, Packaging, and Orderable Information*.

9.5.2 Layout Example

Below are printed circuit board (PCB) layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB.

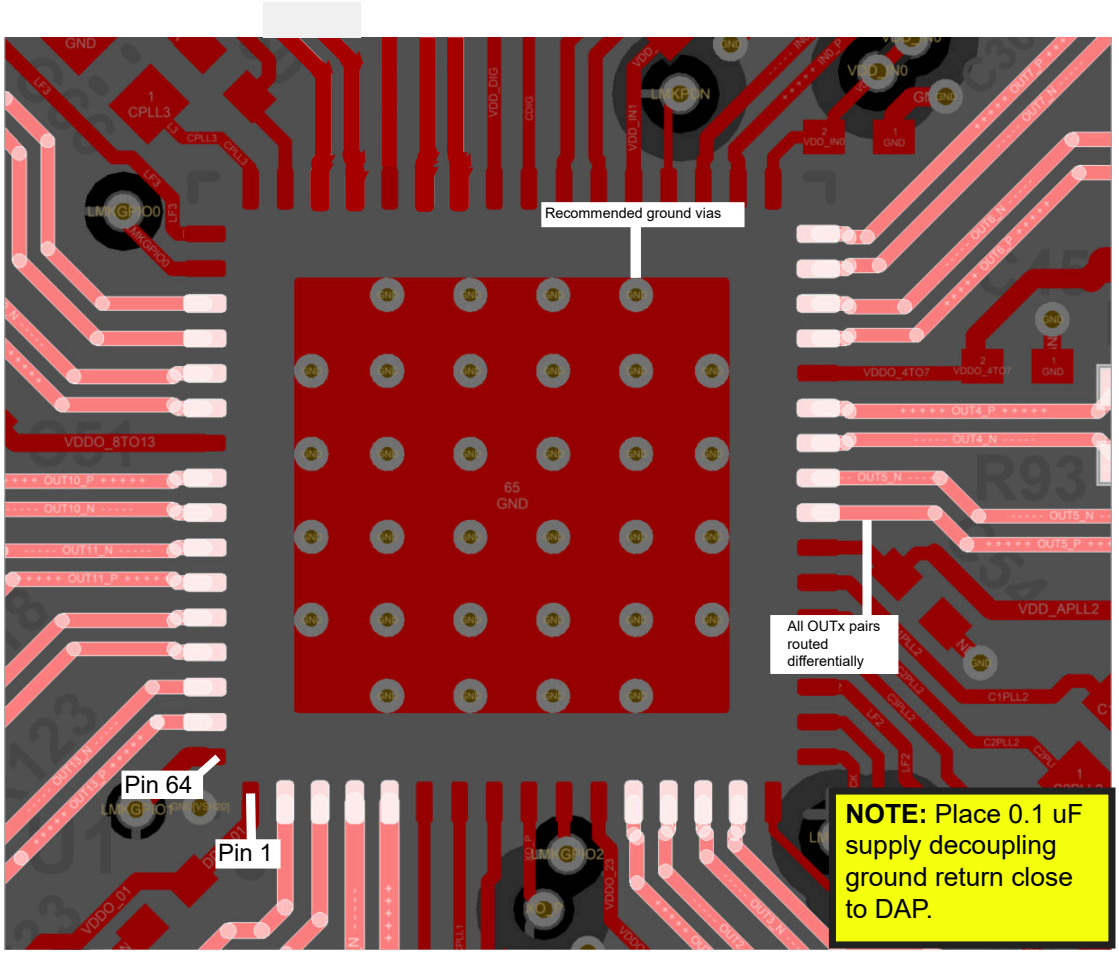


図 9-18. PCB Layout Example for LMK5B33414, Top Layer

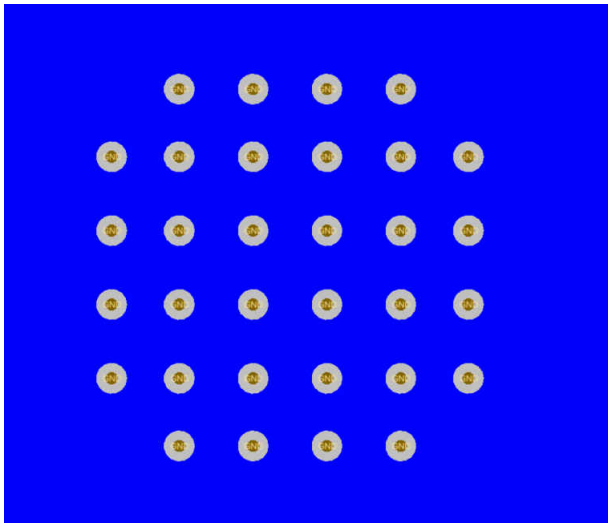


図 9-19. PCB Layout Example for LMK5B33414, Bottom Layer

9.5.3 Thermal Reliability

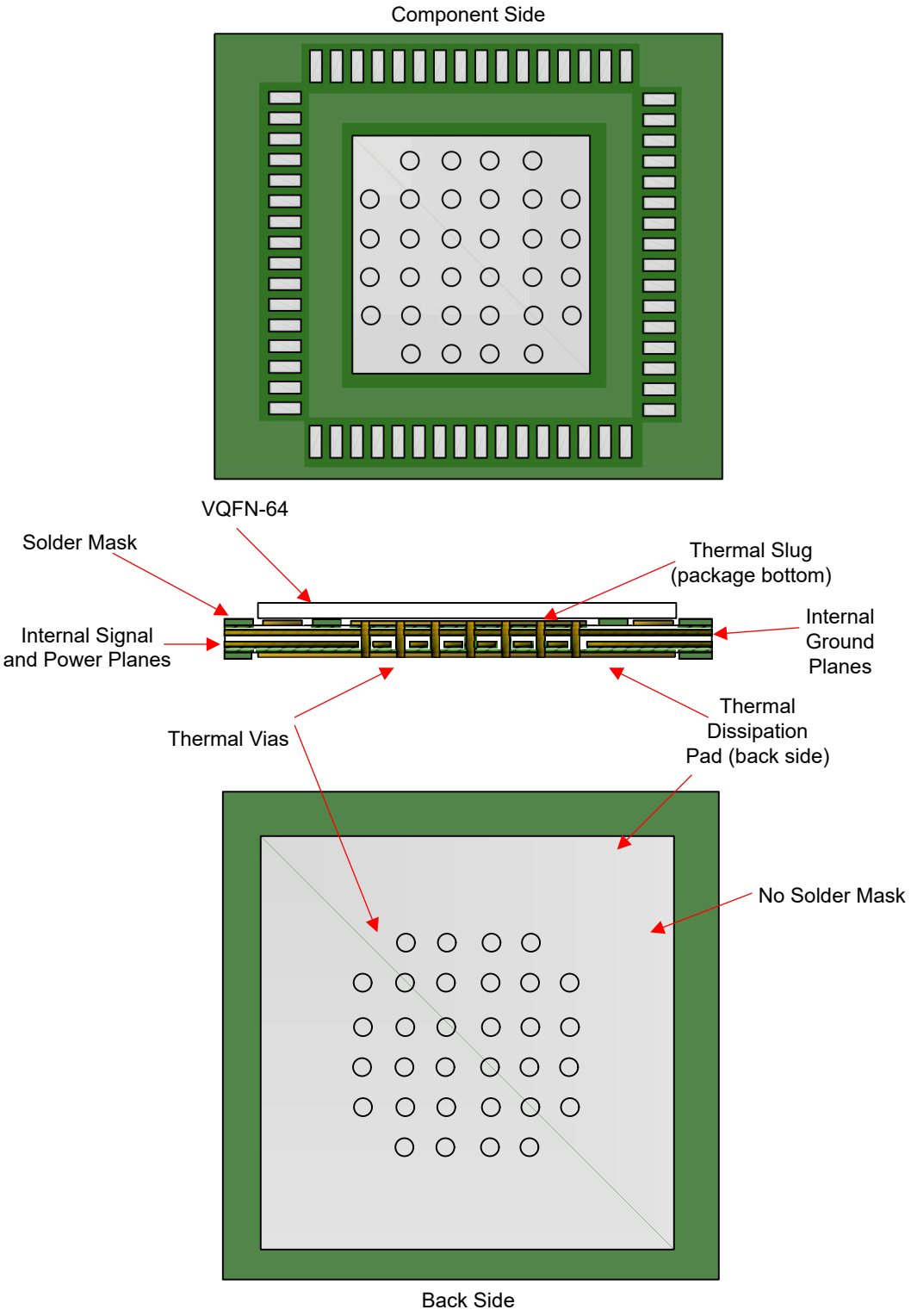


図 9-20. General PCB Ground Layout for Thermal Reliability (8+ Layers Recommended)

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Clock Tree Architect Programming Software

The clock tree architect is a clock tree synthesis tool that streamlines your design process by generating clock tree solutions based on your system requirements. The tool pulls data from an extensive database of clocking products to generate a system-level multi-chip clocking solution.

10.1.1.2 Texas Instruments Clocks and Synthesizers (TICS) Pro Software

The Texas Instruments clocks and synthesizers (TICS) pro software is used to program the evaluation modules (EVMs) for product numbers with these prefixes: CDC, LMK and LMX. These products include phase-locked loops and voltage-controlled oscillators (PLL+VCO), synthesizers and clocking devices.

10.1.1.3 PLLatinum™ Simulation Tool

PLLATINUMSIM-SW PLLatinum™ simulation tool that allows users to create detailed designs and simulations of our PLLatinum™ integrated circuits, which include the LMK and LMX series of phase-locked loops (PLLs) and synthesizers.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *LMK5B33414EVM User's Guide*
- Texas Instruments, *LMK5B33414 Programmer's Guide*

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10.7 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK5B33414RGCR	ACTIVE	VQFN	RGC	64	4000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	K5B33414	Samples
LMK5B33414RGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	K5B33414	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

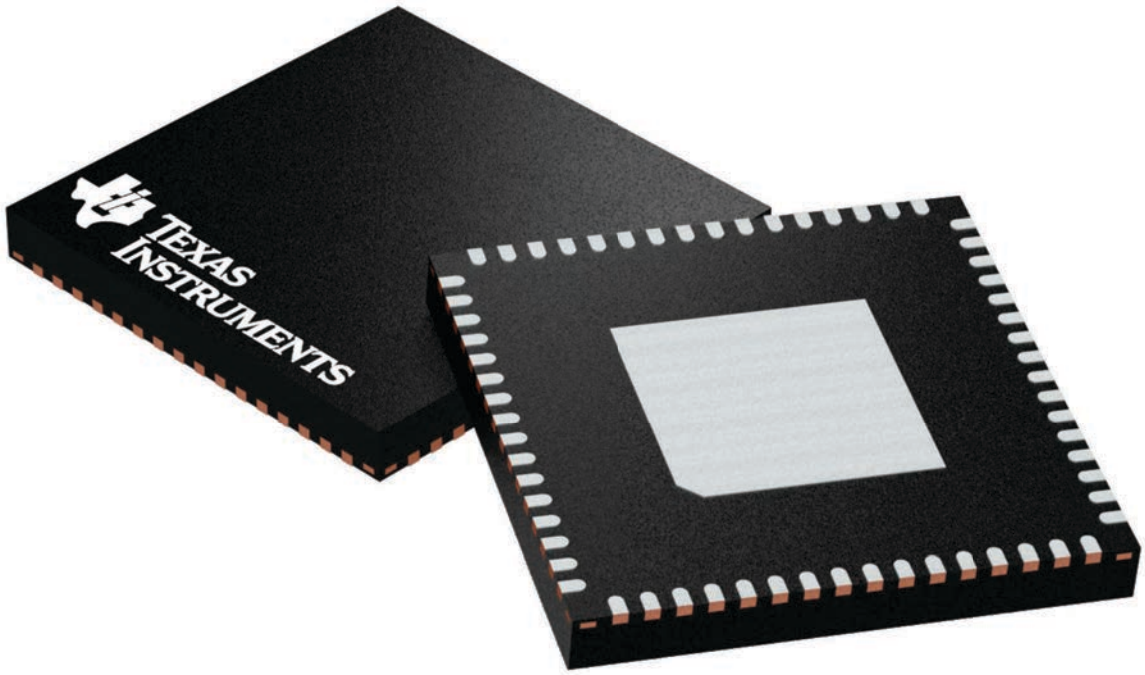
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

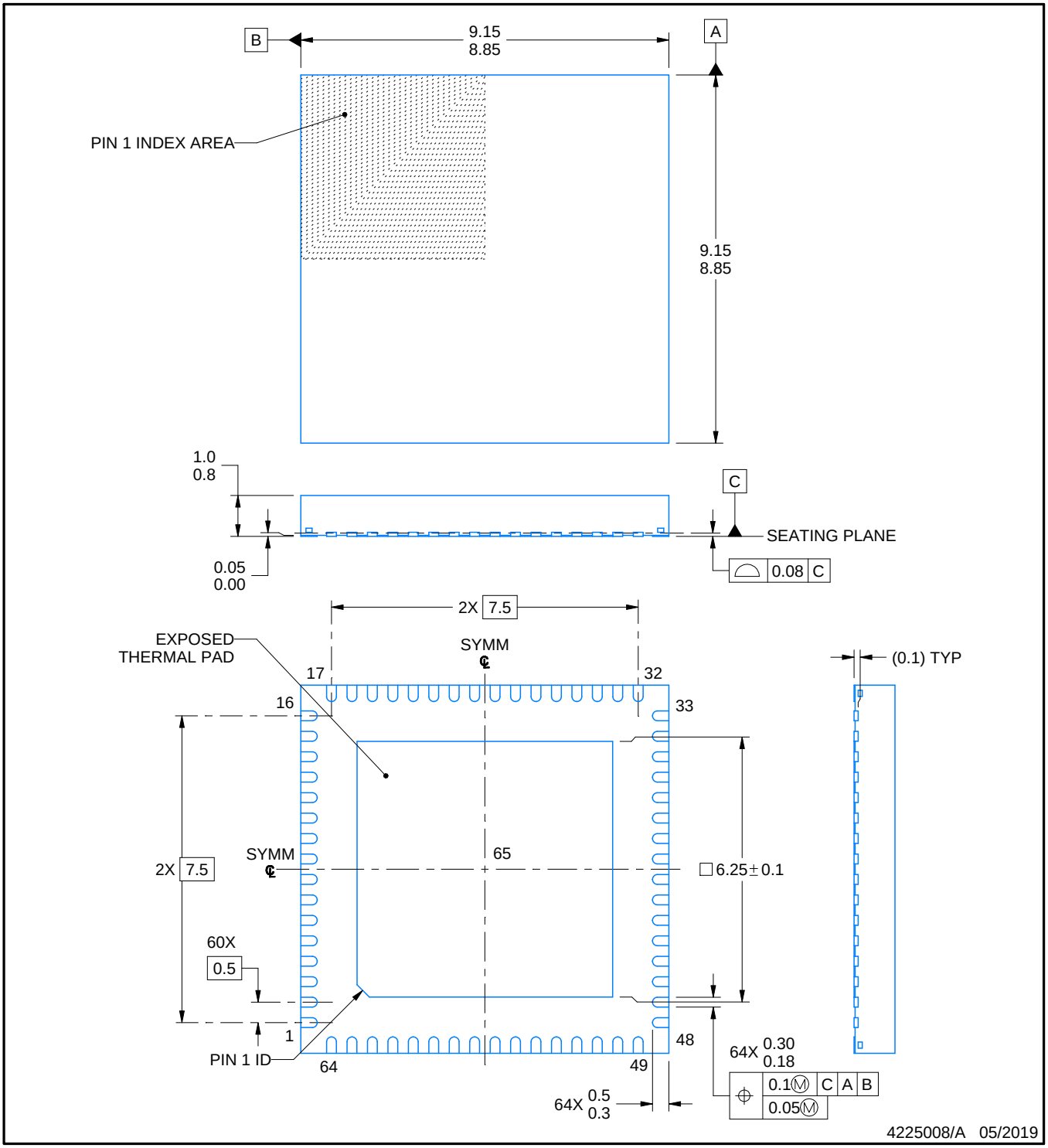
4224597/A

RGC0064E

PACKAGE OUTLINE

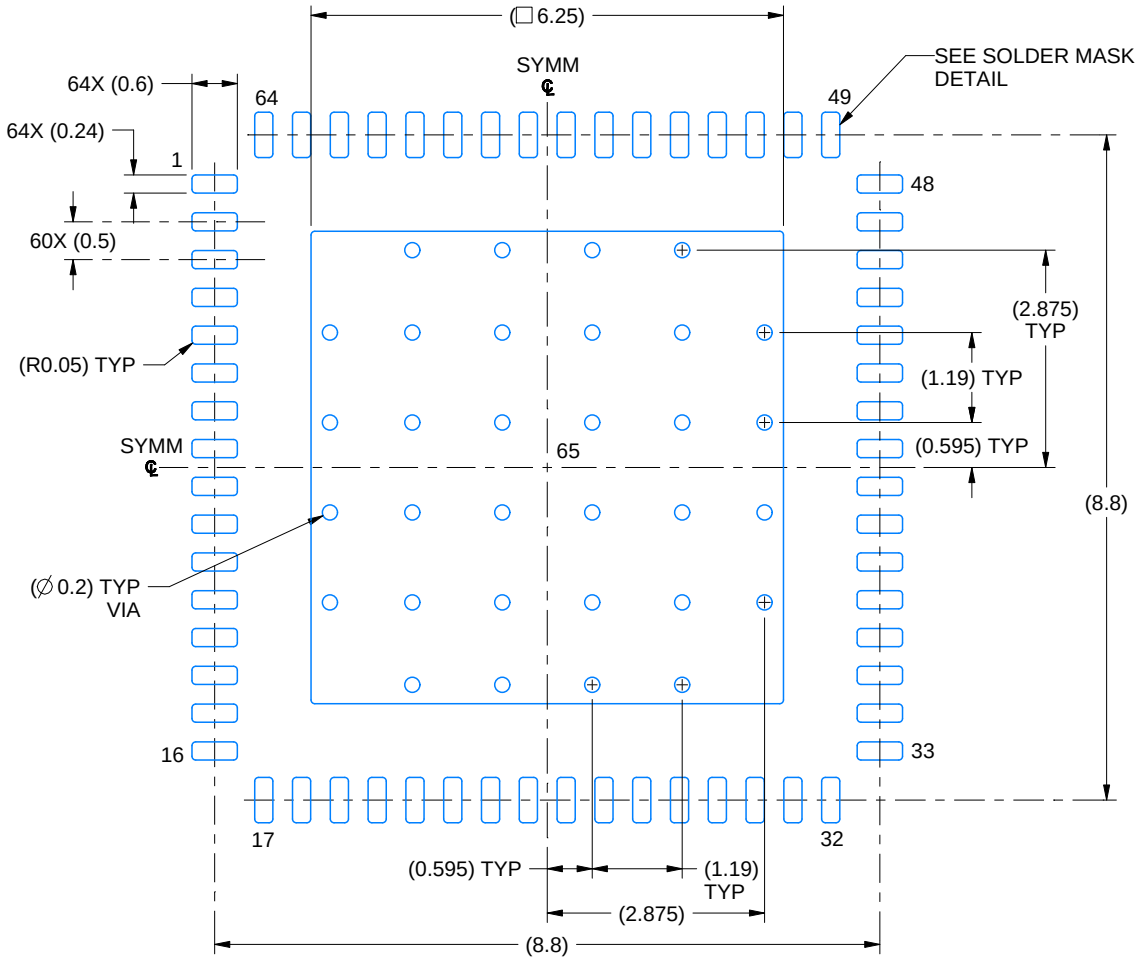
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

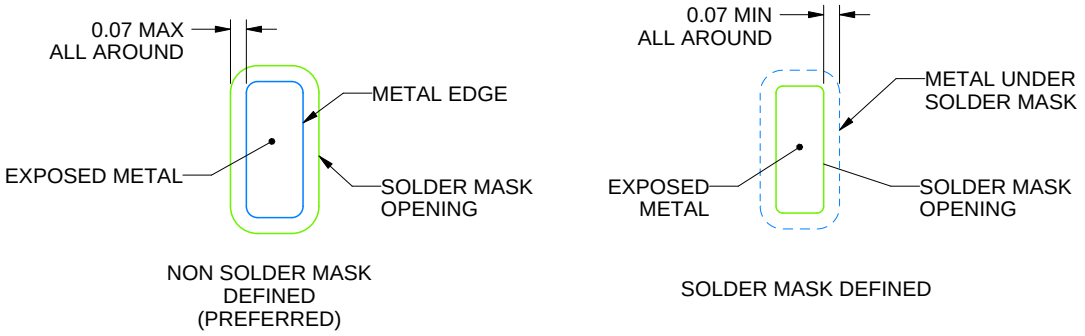


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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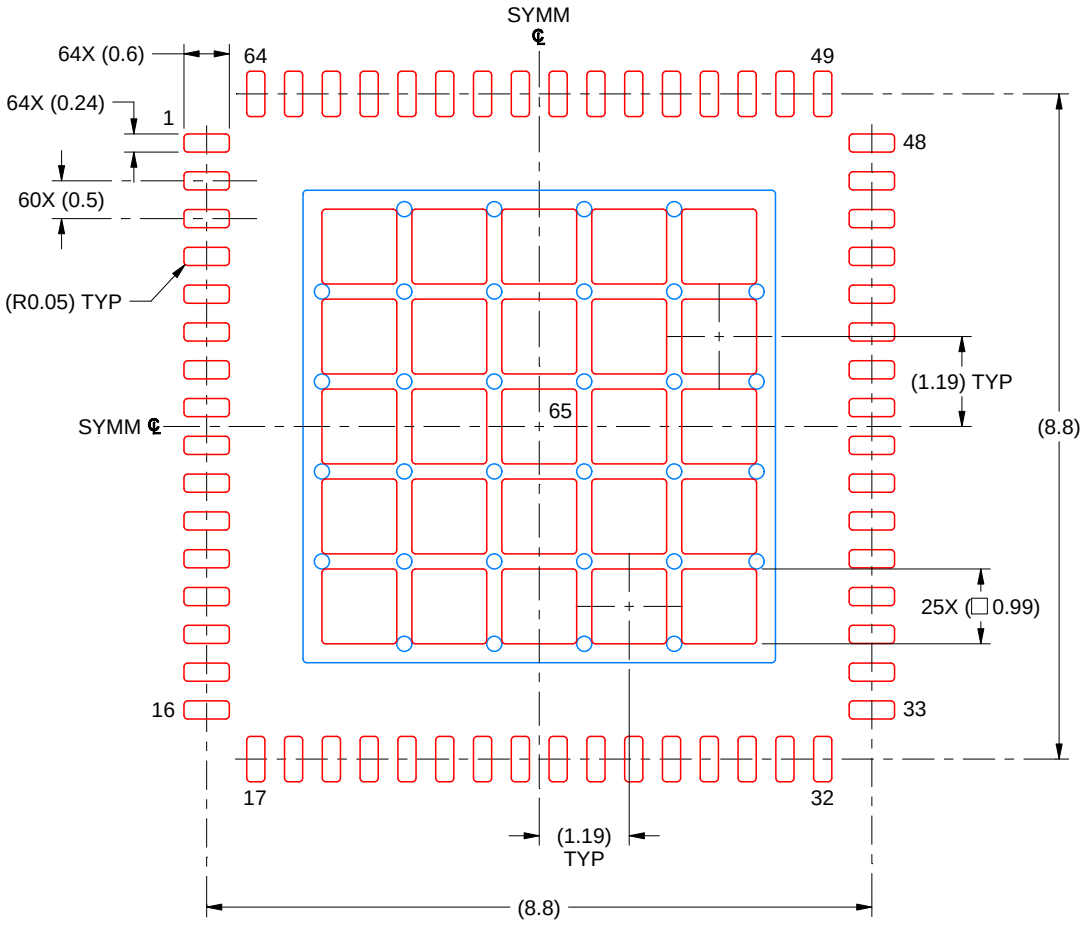
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225008/A 05/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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