LMK3C0105 リファレンスレス、5 LVCMOS 出力、プログラマブル BAW クロック ジェネレータ

1 特長

- BAW 共振器を内蔵、外部リファレンスは不要
- フレキシブルな周波数生成:
  - 100MHz から 400MHz へのデュアル フラクショナル出力分周器 (FOD)
  - 2 チャネル分圧器:2.5MHz～200MHz の範囲で最大 3 つの異なる出力周波数
    - 例:OUTA/B/C/D/E = 25MHz
    - 例:OUTA/B = 100MHz、OUTC/D = 50MHz、OUTE = 25MHz
  - 1.8V/2.5V/3.3V の LVCMOS 出力を 200MHz までサポート
  - OUTA ピン経由で最大 5 つの LVCMOS クロックを OUTA に生成
- 合計出力周波数安定性 ±25ppm
- 2 つの機能モード:I2C または事前にプログラムされた OTP
- –40°C から 85°C 周囲温度。
- SSC 出力と非 SSC 出力の混合をサポート
- プログラム可能な SSC 変調深度
  - 事前プログラム済み:-0.1%、-0.25%、-0.3%、および -0.5% のダウン スプレッド
  - 抵抗によるプログラミングが可能:-0.1%～-3% のダウン スプレッド、または ±0.05%～±1.5% のセンター スプレッド
- VDD = VDDO = 1.8V/2.5V/3.3V ± 5%
- スタートアップ時間 5ms 未満
- 出力が同じ FOD からの場合、出力間スキューは 50ps 未満
- フェイルセーフ 入力および VDD ピン

2 アプリケーション

- 水晶振動子の代替 (最大 5 つのシングルエンド クロック)
- ASIC、FPGA、MCU のリファレンス クロック供給
- 産業用通信
- 産業用 PC
- ヒューマン マシン インターフェイス (HMI)
- 有線ネットワーク

3 概要

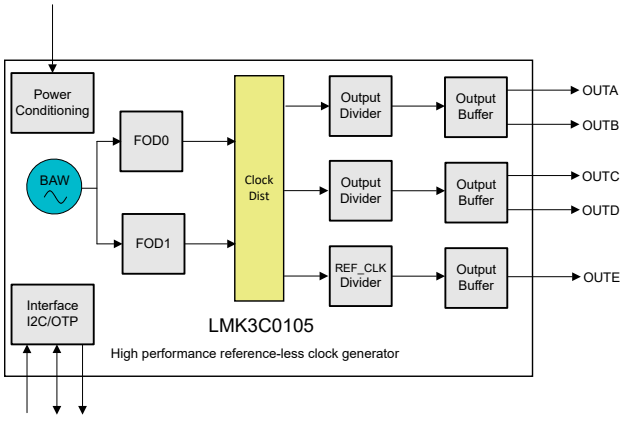
LMK3C0105 は、SSC 対応の 5 出力リファレンスレス クロック ジェネレータです。このデバイスは、テキサス・インスツルメンツ独自のバルク弾性波 (BAW) 技術に基づいており、水晶振動子や外部クロック リファレンスを用いることなく、±25ppm のクロック出力を供給します。このデバイスは、5 つの SSC クロック、5 つの非 SSC クロック、または SSC クロックと非 SSC クロックのミックスを同時に供給できます。5 つの出力に対して、最大 3 つの異なる出力周波数を生成できます。各出力チャネルは、いずれかの FOD を周波数ソースとして選択し、4 つの LVCMOS クロックを生成できます。REF_CTRL ピンは 5 番目の LVCMOS クロック出力として機能し、いずれかの FOD をソースとして選択できます。

このデバイスは、GPIO ピンまたは I2C インターフェイスを介して簡単に構成できます。LMK3C0105 は PSNR が非常に優れており、外部 LDO は不要です。電源のフィルタ処理と DC/DC 回路からの電源供給に関する詳細なガイドラインについては、「電源に関する推奨事項」を参照してください。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LMK3C0105	RER (VQFN、16)	3.0mm × 3.0mm

(1) 詳細については、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略ブロック図

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4 Pin Configuration and Functions

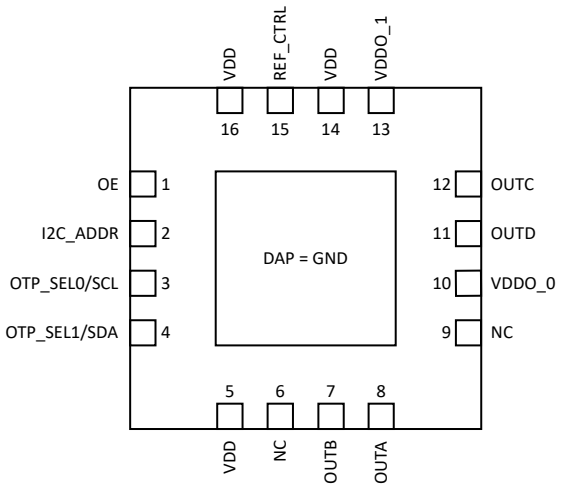

図 4-1. LMK3C0105 16-Pin TQFN Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OUTA, OUTB, OUTC, OUTD	8, 7, 12, 11	O	LVCMOS clock outputs. Supports 1.8V/2.5V/3.3V LVCMOS.
REF_CTRL (OUTE)	15	I/O	Multifunctional pin. At power-up, the state of this pin is latched to select the functionality of Pin 2, Pin 3 and Pin 4. Pull low for I2C mode or high for OTP mode prior to power-up. After power-up, this pin can be programmed as an additional LVCMOS output (OUTE), active-high CLK_READY signal (default), or disabled. See REF_CTRL Operation for more details. This pin has an 880kΩ internal pull-down resistor.
OE	1	I	Global Output Enable. Active low. 2-state logic input pin. This pin has a 75kΩ internal pull-down resistor. See Output Enable for more details. • Low: Outputs are enabled • High: Outputs are disabled
I2C_ADDR	2	I	This pin, in I2C Mode, can be used to set the I2C address from one of four options at power-up. See I2C Mode for more details. This pin has a 75kΩ internal pull-down resistor. • I2C Mode: This pin selects the I2C address.
OTP_SEL0/SCL, OTP_SEL1/SDA	3, 4	I, I/O	Multifunctional pin. Functionality is determined by REF_CTRL (pin 15) at power-up. See OTP Mode and I2C Mode for details. • I2C Mode: These pins are the I2C clock and data connections. • OTP Mode: These pins select the OTP page.
VDD	5, 14, 16	P	1.8V, 2.5V or 3.3V device power supply. A 0.1µF capacitor must be placed as close to each of the pins as possible.
VDDO_0	10	P	1.8V, 2.5V or 3.3V OUTA and OUTB power supply. If VDD is 1.8V or 2.5V, the VDDO pins must be the same voltage as VDD. A 0.1µF capacitor must be placed as close to the pin as possible.
VDDO_1	13	P	1.8V, 2.5V or 3.3V OUTC and OUTD power supply. If VDD is 1.8V or 2.5V, the VDDO pins must be the same voltage as VDD. A 0.1µF capacitor must be placed as close to the pin as possible.

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表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
NC	6, 9	N/A	No connect. Pins can be connected to GND, VDD, or otherwise tied to any potential within the Supply Voltage range stated in the Absolute Maximum Ratings.
DAP	17	G	GND

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Device supply voltage	–0.3	3.9	V
V_{DDO}	Output supply voltage	–0.3	3.9	V
V_{IN}	Logic input voltage (V_{DD} = V_{DDO} = –0.3V to 3.465V)	–0.3	3.465	V
V_{OUT}	Voltage applied to OUTx_P and OUTx_N pins (when outputs are high or low)	–0.3	V_{DDO_x} + 0.3	V
	Voltage applied to OUTx_P and OUTx_N pins (when outputs are LVCMOS tri-state)	–0.3	1.89	V
T_J	Junction temperature		105	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

V_{DD} = V_{DDO} = 1.8V, 2.5V or 3.3V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
V_{DDO}	Output supply voltage	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		105	°C
t_{ramp}	Power supply ramp time. V_{DD} = 1.8 V	0.05		5	ms
t_{ramp}	Power supply ramp time. V_{DD} = 2.5 V or 3.3 V	0.05		5	ms

5.4 Thermal Information

THERMAL METRIC(1)		LMK3C0105 RER (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.5	°C/W

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THERMAL METRIC(1)		LMK3C0105 RER (QFN) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

V_{DD} = V_{DDO} = 1.8V, 2.5V or 3.3V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY STABILITY						
Δf_{total}	Total frequency stability	All factors included: temperature variation, 10-year aging, solder shift, hysteresis and initial frequency accuracy	–25		25	ppm
LVCMOS CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		200	MHz
dV/dt	Output slew rate	V_{DDO} = 3.3V ± 5%, measured from 20% to 80%, 4.7pF load	2.6		4.7	V/ns
		V_{DDO} = 2.5V ± 5%, measured from 20% to 80%, 4.7pF load	2.6		3.7	V/ns
		V_{DDO} = 1.8V ± 5%, measured from 20% to 80%, 4.7pF load	1.5		3.2	V/ns
V_{OH}	Output high voltage	I_{OH} = –15mA at 3.3V	0.8 x V_{DDO}		V_{DDO}	V
		I_{OH} = –12mA at 2.5V				
		I_{OH} = –8mA at 1.8V				
V_{OL}	Output low voltage	I_{OL} = 15mA at 3.3V			0.4	V
		I_{OL} = 12mA at 2.5V				
		I_{OL} = 8mA at 1.8V				
I_{leak}	Output leakage current	Output tri-stated. V_{DD} = V_{DDO} = 3.465V	–5	0	5	µA
R_{out}	Output impedance			17		Ω
ODC	Output duty cycle	f_{out} ≤ 156.25MHz	45		55	%
		f_{out} > 156.25MHz	40		60	%
t_{skew}	Output-to-output skew	Same FOD, LVCMOS output			50	ps
C_{load}	Maximum load capacitance				15	pF
LVCMOS REFCLK CHARATERISTICS						
f_{out}	Output frequency	See(1)	12.5(2)		200	MHz
dV/dt	Output slew rate	V_{DDO} = 3.3V ± 5%, measured from 20% to 80%, 4.7pF load(1)	2.6		6.7	V/ns
		V_{DDO} = 2.5V ± 5%, measured from 20% to 80%, 4.7pF load(1) (3)	1.8		4.5	V/ns
		V_{DDO} = 1.8V ± 5%, measured from 20% to 80%, 4.7pF load(1) (3)	1		3.2	V/ns
I_{leak}	Output leakage current	Output tri-stated. V_{DD} = V_{DDO} = 3.465V(1) (3)	–5		5	µA
R_{out}	Output impedance			17		Ω
ODC	Output duty cycle	f_{out} ≤ 156.25MHz(1)	45		55	%
ODC	Output duty cycle	f_{out} > 156.25MHz(1)	40		60	%
C_{load}	Maximum load capacitance	See(1)			15	pF
RJ	Random jitter	12kHz to 20MHz integrated jitter at 50MHz(1)			0.5	ps

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V_{DD} = V_{DDO} = 1.8V, 2.5V or 3.3V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SSC CHARACTERISTICS						
f_{out}	Output frequency range that supports SSC (any output format)		2.5		200	MHz
f_{SSC}	SSC modulation frequency		30	31.5	33	kHz
$f_{SSC-deviation}$	SSC deviation (modulation depth)	Down spread (programmable)	–3		–0.1	%
		Center spread (programmable)	±0.05		±1.5	%
$f_{SSC-deviation-accuracy}$	SSC deviation accuracy	f_{out} ≤ 100MHz, down spread	0		0.01	%
		100MHz < f_{out} ≤ 200MHz, down spread	0		0.05	%
		f_{out} ≤ 100MHz, center spread	0		0.01	%
		100MHz < f_{out} ≤ 200MHz, center spread	0		0.05	%
df/dt	max SSC frequency slew rate	0 < $f_{SSC-deviation}$ ≤ –0.5%			1250	ppm/µs
TIMING CHARACTERISTICS						
$t_{startup}$	Start-up time	V_{DD} = 2.5V or 3.3V. Time elapsed from all V_{DD} pins reach 2.1V until first output clock rising edge. Output clock is always within specification			1	ms
		V_{DD} = 1.8V. Time elapsed from all V_{DD} pins reach 1.6V until first output clock rising edge. Output clock is always within specification			1.5	ms
t_{OE}	Output enable time.	After CLOCK_READY status is '1', time elapsed between OE assertion and first output clock rising edge. Output is not tristated when disabled.			7	output clock cycles
t_{OD}	Output disable time.	Time elapsed between OE deassertion and last output clock falling edge.			7	output clock cycles
POWER CONSUMPTION CHARACTERISTICS						
I_{DD}	Core supply current, not including output drivers	One FOD enabled, 100MHz ≤ f_{FOD} ≤ 200MHz		57.5	79.9	mA
		One FOD enabled, 200MHz < f_{FOD} ≤ 400MHz		67	90.7	mA
		Two FODs enabled, 100MHz ≤ f_{FOD} ≤ 200MHz		81.1	105.8	mA
		Two FODs enabled, 200MHz < f_{FOD} ≤ 400MHz		97.8	125.8	mA
I_{DDO}	Output supply current, per output channel	1.8V LVCMOS. f_{out} = 50MHz		4.2	5	mA
		1.8V LVCMOS. f_{out} = 200MHz		11.7	13.4	mA
		2.5V LVCMOS. f_{out} = 50MHz		5.6	6.4	mA
		2.5V LVCMOS. f_{out} = 200MHz		15.3	17.3	mA
		3.3V LVCMOS. f_{out} = 50MHz		6.8	7.7	mA
		3.3V LVCMOS. f_{out} = 200MHz		19.2	21.7	mA
I_{DDREF}	REFCLK supply current	1.8V LVCMOS. f_{out} = 50MHz		3.4	3.9	mA
		1.8V LVCMOS. f_{out} = 200MHz		9.5	11.7	mA
		2.5V LVCMOS. f_{out} = 50MHz		4.7	5.3	mA
		2.5V LVCMOS. f_{out} = 200MHz		12.8	15.8	mA
		3.3V LVCMOS. f_{out} = 50MHz		5.9	6.6	mA
		3.3V LVCMOS. f_{out} = 200MHz		16.6	20.2	mA
PSNR CHARACTERISTICS						

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V_{DD} = V_{DDO} = 1.8V, 2.5V or 3.3V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PSNR_{LVCMOS}$	Power Supply Noise Rejection for LVCMOS outputs(3)	10kHz		–76.7	-58.1	dBc
		50kHz		–80.9	-57.9	dBc
		100kHz		–81.8	-57	dBc
		500kHz		–84.3	-61.7	dBc
		1MHz		–97.6	-78.1	dBc
		5MHz		–104.3	-79	dBc
		10MHz		–108.7	-89.5	dBc
2-STATE LOGIC INPUT CHARACTERISTICS						
$V_{IH-Pin2}$	Input high voltage for Pin 2		0.7 × V_{DD}		V_{DD} + 0.3	V
$V_{IL-Pin2}$	Input low voltage for Pin 2		GND – 0.3		0.3 × V_{DD}	V
$V_{IH-Pin1}$	Input high voltage for Pin 1		1.15		V_{DD} + 0.3	V
$V_{IL-Pin1}$	Input low voltage for Pin 1		–0.3		0.65	V
$V_{IH-Pin3,4}$	Input voltage high for OTP_SEL[1:0]		0.7 × V_{DD}		V_{DD} + 0.3	V
$V_{IL-Pin3,4}$	Input voltage low for OTP_SEL[1:0]		GND - 0.3		0.8	V
$V_{IH-Pin15}$	Input voltage high for Pin 15		0.65 × V_{DD}		V_{DD} + 0.3	V
$V_{IL-Pin15}$	Input voltage low for Pin 15		–0.3		0.4	V
$R_{ext-up/down-Pin1,2}$	Recommended external pullup or pulldown resistor for Pin 1, 2		0	1	10	kΩ
$R_{ext-up/down-Pin3,4,15}$	Recommended external pullup or pulldown resistor for Pin 3, 4, 15		0	10	60	kΩ
t_R/t_F	OE signal rise or fall time				10	ns
C_{in}	Input capacitance				3	pF

(1) Tested with 10kΩ external pullup or pulldown resistor
(2) REFCLK can be /2, /4, /8 from either FOD0 or FOD1. Both FODs support 100MHz to 400MHz.
(3) All power supply pins are tied together. 0.1µF capacitor placed close to each power supply pin. Apply 50mVpp ripple and measure the spur level at the clock output

5.6 I2C Interface Specification

All timing requirements referred to V_{IH-min} and V_{IL-max}. Chip V_{DD} = I^2C V_{DD}.

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
V_{IL}	Input low voltage		–0.3	0.3 × V_{DD}	–0.3	0.3 × V_{DD}	V
V_{IH}	Input high voltage		0.7 × V_{DD}	V_{DD} + 0.3	0.7 × V_{DD}	V_{DD} + 0.3	V
V_{hys}	Hysteresis of Schmitt trigger input				0.05 × V_{DD}		V
V_{OL1}	Low level output voltage 1	At 3mA sink current. V_{DD} > 2V	0	0.4	0	0.4	V
V_{OL2}	Low level output voltage 2	At 2mA sink current. V_{DD} ≤ 2V			0	0.2 x V_{DD}	V
I_{OL}	Low level output current	V_{OL} = 0.4V	3		3		mA
		V_{OL} = 0.6V			6		mA

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All timing requirements referred to $V_{IH\text{-}min}$ and $V_{IL\text{-}max}$. Chip V_{DD} = I^2C V_{DD}.

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
t_{OF}	Output fall time from VIHmin to VILmax			250	20 × (V_{DD} / 5.5 V)	250	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter				0	50	ns
I_i	Input current each I/O pin	0.1 × V_{DD} < V_{IN} < 0.9 × V_{DDmax}	–10	10	–10	10	µA
C_i	Capacitance for each I/O pin			10		10	pF
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
$t_{HD\text{-}STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4		0.6		µs
tlow	Low period of the SCL clock		4.7		1.3		µs
thigh	High period of the SCL clock		4		0.6		µs
$t_{SU\text{-}STA}$	Set-up time for a repeated START condition		4.7		0.6		µs
$t_{HD\text{-}DAT}$	Data hold time	I^2C bus devices	0		0		µs
$t_{SU\text{-}DAT}$	Data set-up time		0.25		0.1		µs
t_R	Rise time of both SDA and SCL signals (1)			300	20	300	ns
t_F	Fall time of both SDA and SCL signals (1)			300	20 × (V_{DD} / 5.5 V)	300	ns
$t_{SU\text{-}STO}$	Set-up time for STOP condition		4		0.6		µs
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		µs
C_B	Capacitive load for each bus line			400		400	pF
$t_{VD\text{-}DAT}$	Data valid time			3.45		0.9	µs
$t_{VD\text{-}ACK}$	Data valid acknowledge time			3.45		0.9	µs
V_{NL}	Noise margin at the low level	For each connected device, including hysteresis	0.1 x V_{DD}		0.1 × V_{DD}		V
V_{NH}	Noise margin at the high level	For each connected device, including hysteresis	0.2 x V_{DD}		0.2 × V_{DD}		V

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6 Parameter Measurement Information

6.1 Output Format Configurations

This section describes the characterization test setup of the LVCMOS format option for the LMK3C0105.

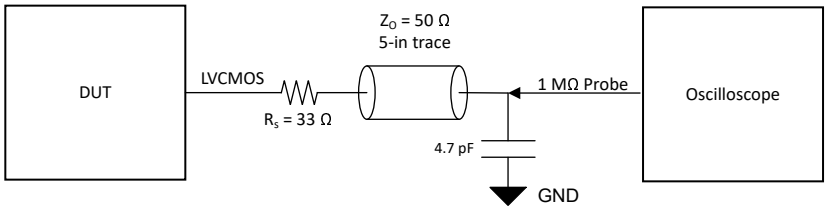

図 6-1. LVCMOS Output Configuration During Device Test

7 Detailed Description

7.1 Overview

The LMK3C0105 is a five-channel clock generator primarily used for LVCMOS clock generation, either with or without Spread Spectrum Clocking (SSC). The device has an integrated Bulk Acoustic Wave (BAW) resonator and does not require any external crystal or clock reference. The device has four selectable pages of memory, referred to as OTP pages. The collection of these pages in memory is referred to as the EFUSE.

The default output configuration is four 25MHz in-phase LVCMOS clocks plus one additional 25MHz LVCMOS clock, all enabled at startup. The LMK3C0105 supports programmable output frequencies up to 200MHz. The LMK3C0105V3 is the part number for the default configuration with a 3.3V supply voltage. The LMK3C0105V1 is the part number for the default configuration with a 1.8V supply voltage. Additional configuration part numbers are LMK3C0105Axxx, where xxx denotes the configuration number.

The LMK3C0105 supports two functional modes determined by the REF_CTRL pin at power-up: One-Time Programming (OTP) mode or I^2C mode.

1. In OTP mode, one out of four OTP pages is selected by pins OTP_SEL0 and OTP_SEL1. The default output frequency across all OTP pages is 25MHz.
2. In I^2C mode, the LMK3C0105 is configured by modifying the active registers. If a configuration other than the default operation is desired, the registers must be written every time at start-up.

Refer to *セクション 4* for the detailed descriptions of the device pins.

The LMK3C0105 has flexible SSC configurations, including:

1. SSC disabled on all outputs
2. SSC enabled on some outputs
3. SSC enabled on all outputs

Refer to *セクション 7.4.2.3* for SSC and jitter performance details.

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7.2 Functional Block Diagram

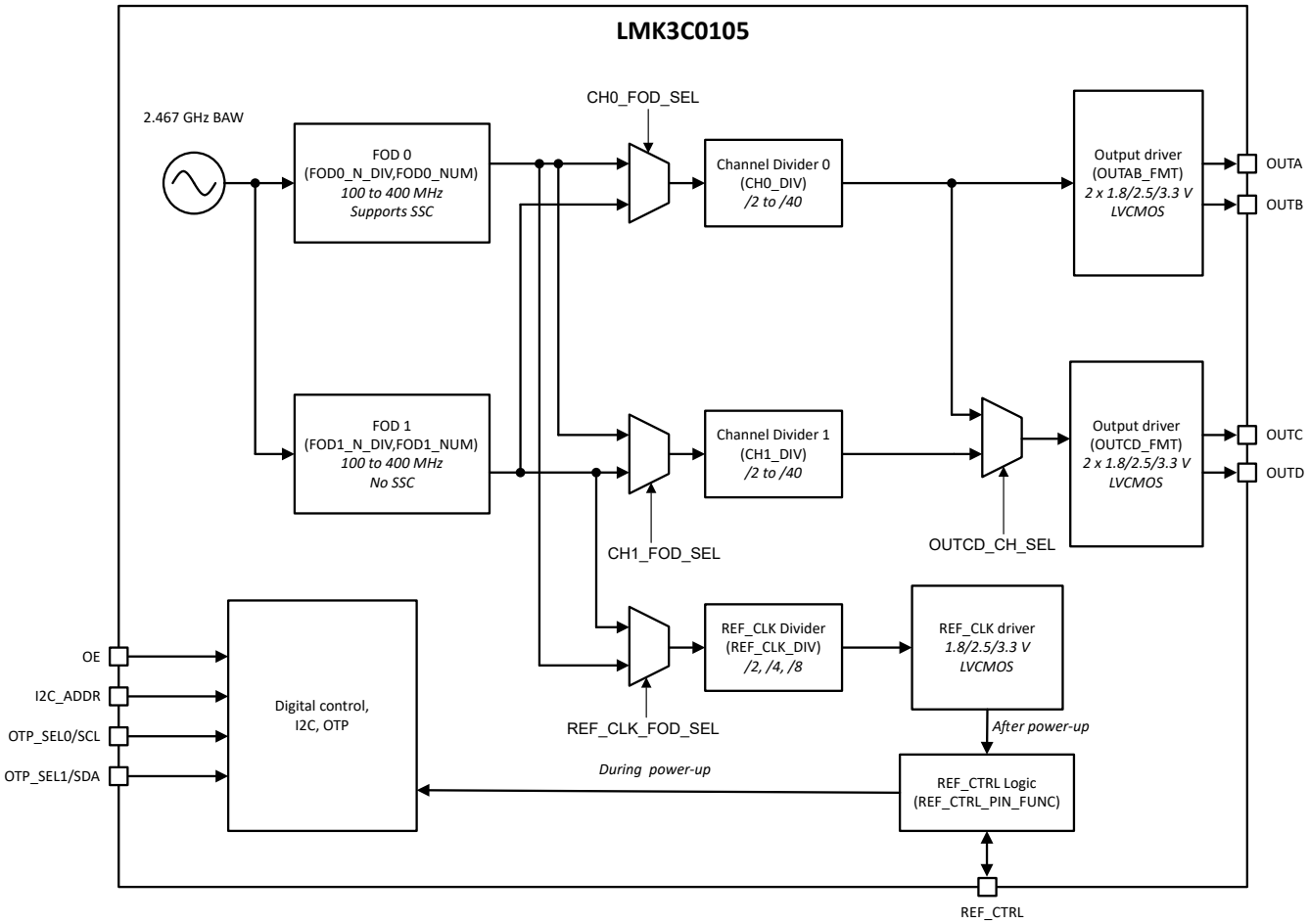

図 7-1. LMK3C0105 Functional Block Diagram

7.3 Feature Description

7.3.1 Device Block-Level Description

The LMK3C0105 is a reference-less clock generator with an integrated BAW oscillator. The BAW frequency, nominally 2467MHz, is divided down by two fractional output dividers (FODs), each of which is capable of generating frequencies between 100MHz and 400MHz. Each FOD can be routed to one of two channel dividers, which divides the FOD frequency down to generate frequencies from 2.5MHz to 200MHz. An additional LVCMOS clock, with a voltage corresponding with VDD, can be optionally generated on the REF_CTRL pin. By default, this pin is configured as an additional clock. OUTA and OUTB share an output driver and must be the same frequency. OUTC and OUTD share an output driver and must be the same frequency.

7.3.2 Device Configuration Control

図 7-2 shows the relationships between device states, the configuration pins, device initialization, and device operational modes. OTP mode is entered when the REF_CTRL pin is pulled high at start-up. I^2C mode is entered when the REF_CTRL pin is pulled low at start-up. In OTP mode, the state of the OTP_SEL0/SCL and OTP_SEL1/SDA pins determines the OTP page that is loaded into the active registers. The device is one-time programmable, meaning that the register settings stored into the internal EFUSE can not be changed. The device can be transitioned from OTP to I^2C mode, or reciprocally, by changing the state of the REF_CTRL pin, then triggering a device power cycle by pulling VDD low, then high again. In OTP mode, a change in the level of the OTP_SEL0 or OTP_SEL1 pins, followed by pulling the REF_CTRL pin high dynamically changes the active

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OTP page. The time between the first OTP_SEL pin change and pulling REF_CTRL high must be less than 350 us, otherwise the device enters I2C Mode.

In I^2C mode, the state of the I2C_ADDR pin can determine the I^2C address of the device, with the OTP_SEL0/SCL and OTP_SEL1/SDA pins re-purposed as I^2C clock and data pins, respectively. In I^2C mode, the host can update the active device registers. If using a configuration different than the programmed configuration, the registers must be written after each power cycle.

The device can be placed into a low power state by setting the PDN bit (R10[1]) to '1'. Clearing the PDN bit takes the device out of the low power state. If DEV_IDLE_STATE_SEL bit (R10[4]) is a '0' and the outputs are disabled, the device enters the low power state. Entering the low power state is required for changing the frequency of the FOD used by Channel 0, changing the SSC configuration, and changing the output format. TI recommends performing register writes within this low power state. Set the OTP_AUTOLOAD_DIS (R10[2]) bit to a '1' to prevent automatic loading of OTP Page 0 prior to setting PDN to '0'.

There are two fields that determine the state of the device when coming out of the low power state. PIN_RESAMPLE_DIS (R10[3]) controls whether or not the I2C_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and REF_CTRL pins are resampled when exiting the low power state. If the pins are resampled, the device can be transitioned into OTP mode if the REF_CTRL pin is pulled high. Set this bit to a '1' to disable this functionality. OTP_AUTOLOAD_DIS controls whether or not the contents of OTP Page 0 are loaded into the device registers when exiting the low power state. If OTP_AUTOLOAD_DIS bit is a '1' and PIN_RESAMPLE_DIS is a '1', then the register contents do not change. If OTP_AUTOLOAD_DIS bit is a '0' and PIN_RESAMPLE_DIS is a '1', then the contents of OTP Page 0 are loaded to the registers. If PIN_RESAMPLE_DIS is a '0' and REF_CTRL is pulled high, then the device enters OTP Mode. In this case, OTP_SEL0/SCL and OTP_SEL1/SDA control the OTP page loaded into the device registers.

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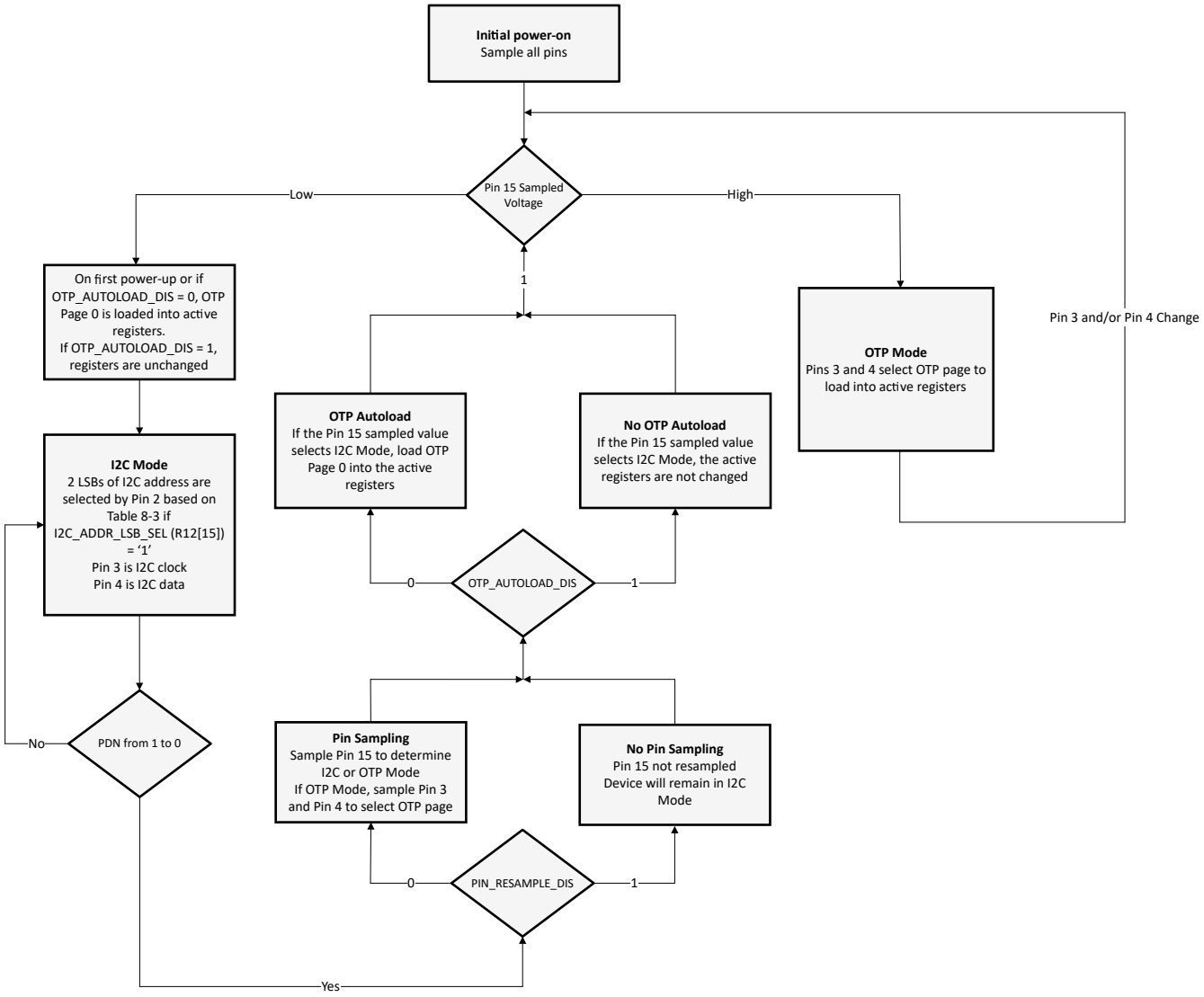

図 7-2. LMK3C0105 Device Mode Diagram

In I^2C Mode, the device registers are from the contents of OTP Page 0. In OTP mode, these values come from one of the four OTP pages, selectable based on the state of the OTP_SELx pins on start-up. 図 7-3 shows interface and control blocks within the LMK3C0105, with the arrows referring to read and write access from the different embedded memories.

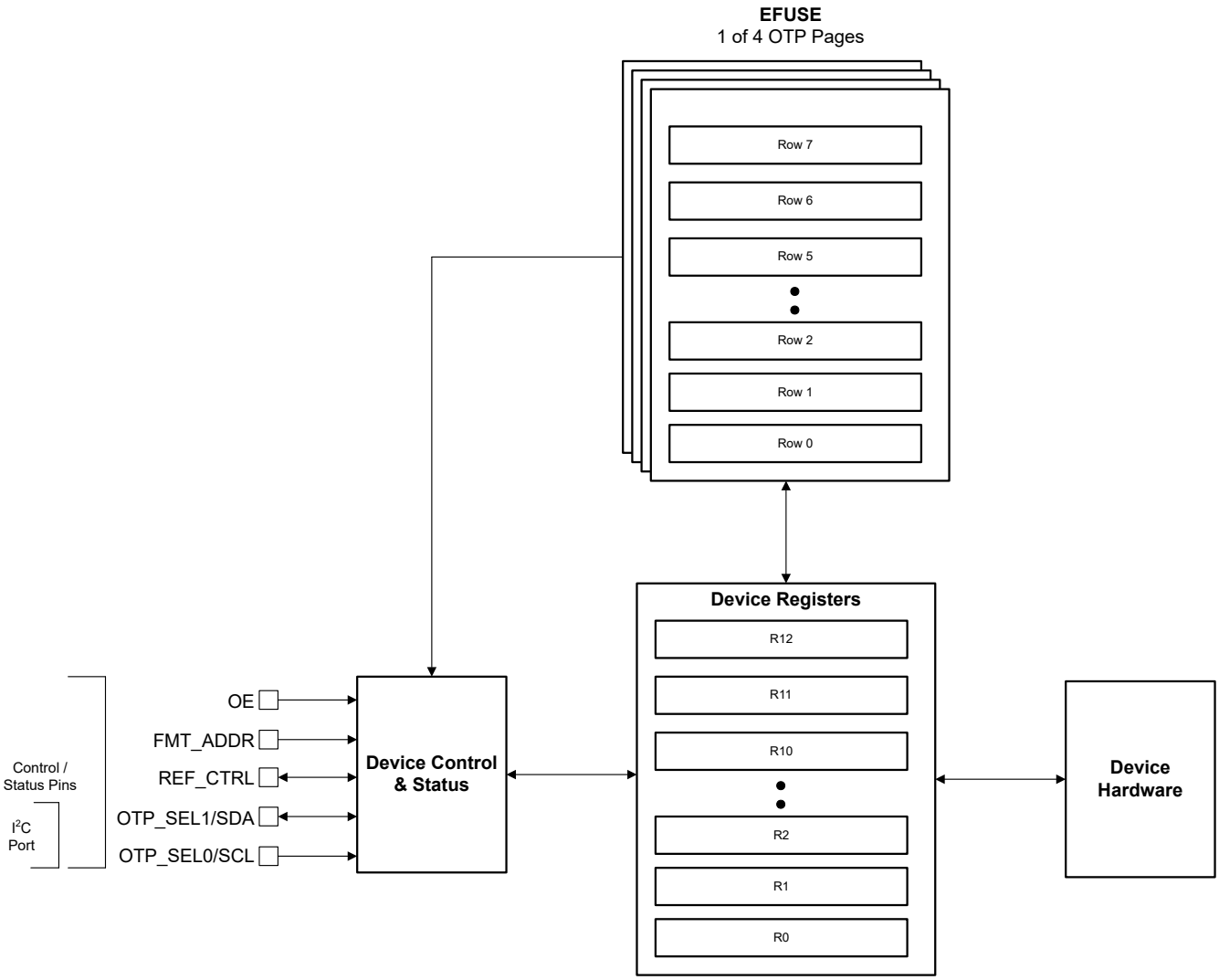

図 7-3. LMK3C0105 Interface and Control Blocks

7.3.3 OTP Mode

In this mode, the configuration pins allow for selection of one of four one-time programmable (OTP) pages, as well as output format selection. I^2C is not enabled in this mode, as the I^2C pins are repurposed for OTP page selection. 表 7-1 shows the OTP page selected based on the state of the OTP_SEL0 and OTP_SEL1 pins. In OTP mode, the I2C_ADDR pin is ignored.

表 7-1. OTP Page Selection in OTP Mode

OTP_SEL1 Pin	OTP_SEL0 Pin	OTP Page
Low	Low	0
Low	High	1
High	Low	2
High	High	3

The EFUSE of the devices is permanently programmed and has OTP_BURNT(R0[0]) = 1. If a new configuration is desired, the configuration must be loaded through I^2C on each start-up. Contact TI for creation of a custom OTP configuration.

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The following fields can be unique between the four OTP pages. All other register settings are shared between the OTP pages:

- SSC_EN: Enable or disable SSC.
- OUTAB_EN: Enable or disable OUTA and OUTB.
- OUTCD_EN: Enable or disable OUTC and OUTD.
- OUTAB_FMT: OUTA and OUTB output configuration, see *セクション 7.4.3.1*.
- OUTCD_FMT: OUTC and OUTD output configuration, see *セクション 7.4.3.1*.
- SSC_SETTING: SSC modulation type, see *Spread-Spectrum Clocking*.

When OTP_SEL1 or OTP_SEL0 pin state changes, the device automatically goes through a power cycle and reloads the new OTP page. The time elapsed from when pins 3 and 4 change to a stable state in the new OTP is no more than 1.5ms.

7.3.4 I²C Mode

In this mode, I²C is enabled and the SCA and SDL pins function as the I²C clock and I²C data pins, respectively. 表 7-2 shows the four default I²C addresses selectable by the I2C_ADDR pin. The 5 MSBs of the I²C address are set in the upper five bits of I2C_ADDR (R12[14:8]).

If I2C_ADDR_LSB_SEL (R12[15]) = 0, then the I2C_ADDR pin is ignored, and the I²C address is solely determined by I2C_ADDR.

表 7-2. I²C Address Selection

REF_CTRL PIN(1)	I2C_ADDR PIN	I²C ADDRESS(2)
High	X	N/A (I2C disabled)
Low	0	0x68 / 0xD0
Low	1	0x69 / 0xD2
Low	Tied to SDA	0x6A / 0xD4
Low	Tied to SCL	0x6B / 0xD8

(1) This is the state of the REF_CTRL pin at power-up, not the live pin state.
(2) The 0xD0, 0xD2, 0xD4, and 0xD8 addresses are with the R/W bit included set to '0'.

When changing the registers of the device, first set PDN to '1', write to the device registers, then set PDN to '0'. 図 7-4 shows this process.

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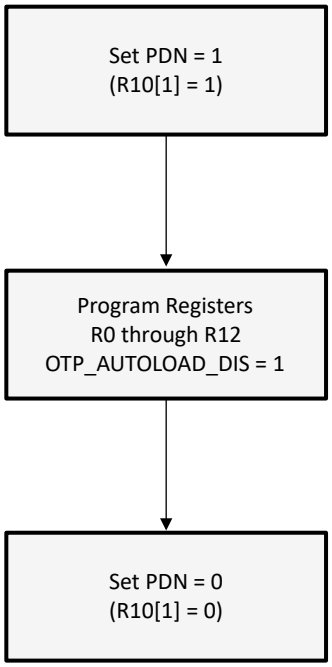

図 7-4. LMK3C0105 Programming Sequence

7.4 Device Functional Modes

7.4.1 Fail-Safe Inputs

The LMK3C0105 digital input pins are designed to support fail-safe input operation, with the exception of the REF_CTRL pin. This feature allows the user to drive the digital inputs before VDD is applied without damaging the device. Refer to *Absolute Maximum Ratings* for more information on the maximum input voltages supported by the device.

7.4.2 Fractional Output Dividers

The LMK3C0105 contains two fractional output dividers. If all outputs are able to be generated by a single FOD, TI recommends disabling FOD1 to conserve power and improve performance. If no output channels select FOD1, then FOD1 is disabled.

7.4.2.1 FOD Operation

The internal BAW resonator is divided down by one or two Fractional Output Dividers (FODs). FOD0 has an SSC generator and FOD1 does not have an SSC generator. If all outputs must be SSC clocks, the clocks must be sourced by FOD0. If SSC clocks and one non-SSC clocks are required at the same time, then FOD0 is enabled for the SSC clocks and FOD1 is enabled for the non-SSC clocks. If none of the output clocks require SSC, then either FOD can be used.

注

TI recommends that FOD0 be used as the default FOD if only one FOD is needed for an application. If both FODs are in use, TI recommends using FOD0 with OUTA/OUTB and FOD1 with OUTC/OUTD.

The maximum frequency that can be generated at the clock outputs by a single FOD is 200MHz. The two FODs can be configured independently so that OUTA/OUTB and OUTC/OUTD can have different frequencies. TI recommends sourcing from a single FOD whenever possible to make sure that OUTA/OUTB and OUTC/OUTD have a deterministic phase relationship and for minimizing power consumption.

The FODs in the LMK3C0105 can be configured to accommodate various output frequencies through I2C programming, or in the absence of programming, the one-time programmed (OTP) settings. The FODs can be

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configured by setting the integer (FODx_N_DIV) and fractional (FODx_NUM) divide values. 表 7-3 shows the register locations for these fields for each FOD.

表 7-3. FOD Integer and Numerator Divide Locations

Field	Register
FOD0_N_DIV	R0[9:3]
FOD0_NUM[23:16]	R1[15:8]
FOD0_NUM[15:0]	R2[15:0]
FOD1_N_DIV	R3[15:9]
FOD1_NUM[23:16]	R6[12:5]
FOD1_NUM[15:0]	R8[15:0]

An example of how to set the integer and numerator divide values is shown in 式 1 and 式 2.

$$FODx\_N\_DIV = floor(F_{BAW}/F_{FOD}) \quad (1)$$

where:

- FODx_N_DIV: Integer portion of the FOD divide value (7 bits, 6 to 24)
- F_{BAW}: BAW frequency, 2467MHz plus offset, described in further detail below
- F_{FOD}: Desired FOD frequency (100MHz to 400MHz)

$$FODx\_NUM = int(((F_{BAW}/F_{FOD}) - FODx\_N\_DIV) \times 2^{24}) \quad (2)$$

where FODx_NUM is the fractional portion of the FOD divide value (24 bits, that is 0 to 16777215).

The output frequency (F_{OUT}) is related to the FOD frequency as given in 式 3. OUTDIV can be 2, 4, 6, 8, 10, 20, or 40.

$$F_{OUT} = F_{FOD}/OUTDIV \quad (3)$$

Use 式 4 to calculate the actual value of the BAW frequency for a device. Users can find the value of BAWFREQ_OFFSET_FIXEDLUT by reading R238, which is a signed 16-bit value.

$$F_{BAW} = 2467MHz \times (1 + (BAWFREQ\_OFFSET\_FIXEDLUT \times 128E\text{-}9)) \quad (4)$$

7.4.2.2 Digital State Machine

The digital state machine of the LMK3C0105 has a clock that originates from one of the FODs. The FOD selected by CH0_FOD_SEL (R3[4]) drives the input to the state machine clock divider. The total divide value is the DIG_CLK_N_DIV (R0[9:3]) field plus two. Set DIG_CLK_N_DIV such that the FOD frequency divided by the total state machine clock divide value is between 40MHz and 50MHz. The divider value used to set this clock is equal to the value stored in . As an example, if the frequency of FOD0 is 200MHz, and CH0_FOD_SEL is a '0', then DIG_CLK_N_DIV must be set to '2', as 200MHz divided by 4 is 50MHz.

7.4.2.3 Spread-Spectrum Clocking

FOD0 supports spread-spectrum clocking (SSC). SSC can be used to reduce peak radiated emissions by modulating the output frequency. When SSC_EN (R4[0]) = '1', any outputs that are sourced from FOD0 have SSC. SSC_MOD_TYPE (R4[1]) selects between down-spread modulation (SSC_MOD_TYPE = 0) or center-spread modulation (SSC_MOD_TYPE = 1). The LMK3C0105 has four built-in down-spread SSC options, as well as a custom SSC option. SSC_CONFIG_SEL (R9[11:9]) selects between the custom or preconfigured options. The preconfigured options are optimized for a 200MHz output from FOD0. 表 7-4 details the register settings for the preconfigured SSC options.

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表 7-4. Predefined SSC Configurations

SSC_CONFIG_SEL	Down-spread SSC Depth
0x0	Custom, based on SSC_STEPS and SSC_STEP_SIZE
0x1	–0.10%
0x2	–0.25%
0x3	–0.30%
0x4	–0.50%
All other values	Reserved

If Custom SSC is selected, then SSC_STEPS (R4[14:2]) and SSC_STEP_SIZE (R5) must be configured to set the modulation depth. Use 式 5 or 式 6 to determine the SSC_STEPS (R4[14:2]) register settings, and use 式 7 or 式 8 to determine the SSC_STEP_SIZE (R5) settings. 式 7 is for down-spread SSC and 式 8 is for center-spread SSC.

$$\text{Down-spread: SSC\_STEPS} = \text{int}((F_{FOD0}/F_{MOD})/2) \quad (5)$$

$$\text{Center-spread: SSC\_STEPS} = \text{int}((F_{FOD0}/F_{MOD})/4) \quad (6)$$

where:

- F_{FOD0}: FOD0 Frequency
- F_{MOD}: Modulation frequency, typically 31.5kHz is used

$$SSC\_STEP\_SIZE = floor((F\_BAW/F\_FOD0 * (1/(1 - SSC\_DEPTH)) - 1))/(SSC\_STEPS) * DEN) \quad (7)$$

$$SSC\_STEP\_SIZE = floor((F\_BAW/F\_FOD0 * (1/(1 - SSC\_DEPTH)) - 1/(1 + SSC\_DEPTH)))/(2 * SSC\_STEPS) * DEN) \quad (8)$$

where:

- SSC_STEP_SIZE: Numerator increment value per step for SSC
- F_{BAW}: BAW frequency, 2467MHz. Note that the F_{BAW} value varies from device to device.
- SSC_DEPTH: Modulation depth, expressed as a positive value. If –0.5% depth is used, this value is 0.005
- SSC_STEPS: Result from 式 5 for down-spread or 式 6 for center-spread
- DEN: Fractional denominator, 2^{24}

If using a mix of SSC on one output and no SSC on a different output, there can be crosstalk between the two outputs. Contact TI to request measurement data for a specific configuration when configuring SSC on only a single output.

When modifying the SSC settings, do not set SSC_EN to a '1' until the other SSC settings have been configured. Perform the following steps for configuring the SSC:

1. Set PDN to a '1'.
2. Set OTP_AUTOLOAD_DIS to a '1'.
3. Modify SSC_MOD_TYPE, SSC_STEP_SIZE, and SSC_STEPS as necessary.
4. Set SSC_EN to a '1'.
5. Set PDN to a '0'.

7.4.2.4 Integer Boundary Spurs

When the decimal portion of the FOD divide value is near an integer boundary, integer boundary spurs can occur. In general, this "integer boundary" is when the decimal portion is between 0.9 and 1, or 0 and 0.1. For example, if the BAW frequency is 2467MHz, and an output of 61.44MHz, then the FOD can run at 122.88MHz. 2467MHz divided by 122.88MHz is approximately 20.076. The decimal portion of the divide value is 0.076, which falls between 0 and 0.1, and thus means that generating a 61.44MHz output can result in spurs in the 12kHz to 20MHz band on the output clock. In some cases, proper frequency planning can account for this by increasing

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the FOD frequency and the channel divider value. Using an FOD frequency of 368.64MHz and a channel divider of 6 also yields an output frequency of 61.44MHz. The FOD divide value here is approximately 6.692, which does not yield integer boundary spurs. For any concerns about integer boundary spurs for a specific frequency plan, contact TI.

7.4.3 Output Behavior

7.4.3.1 Output Format Selection

This device supports LVCMOS outputs only. For LVCMOS outputs,VDDO can be 1.8V, 2.5V or 3.3V if the VDD is 3.3V. Otherwise, the VDDO must be the same voltage as VDD.

表 7-5. Output Format via Registers

OUTAB_FMT / OUTCD_FMT	Description
0x0	Reserved
0x1	Reserved
0x2	Reserved
0x3	Reserved
0x4	LVCMOS enabled on OUTA/ OUTC LVCMOS disabled on OUTB/ OUTD
0x5	LVCMOS disabled on OUTA/ OUTC LVCMOS enabled on OUTB/ OUTD
0x6	LVCMOS enabled on OUTA/ OUTC LVCMOS enabled on OUTB/ OUTD OUTA/OUTC and OUTB/OUTD 180 degrees out of phase(1)
0x7	LVCMOS enabled on OUTA/ OUTC LVCMOS enabled on OUTB/ OUTD OUTA/OUTC and OUTB/OUTD in phase

(1) For best output performance, TI recommends using 180 degree out of phase LVCMOS if both OUTA and OUTB or both OUTC and OUTD clocks are required.

7.4.3.2 REF_CTRL Operation

At start-up, the REF_CTRL pin selects I^2C mode when low, and OTP mode when high. After start-up, REF_CTRL outputs an LVCMOS REF_CLK by default, which is derived from either FOD0 or FOD1 followed by an integer divider (/2, /4, /8). Alternatively, this pin can be disabled, or function as a "clock ready" signal. REF_CTRL_PIN_FUNC (R7[14:13]) controls the function of the REF_CTRL pin. 表 7-6 shows these options.

表 7-6. REF_CTRL Function after Startup

REF_CTRL_PIN_FUNC	REF_CTRL Function
0x0	Disabled, forced low
0x1	Disabled, tri-state
0x2 (default)	REF_CLK LVCMOS output

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表 7-6. REF_CTRL Function after Startup (続き)

REF_CTRL_PIN_FUNC	REF_CTRL Function
0x3	CLK_READY output

7.4.4 Output Enable

7.4.4.1 Output Enable Control

This device supports synchronous Output Enable (OE). Synchronous OE means there is no glitch on the outputs when OE signal is asserted or deasserted.

表 7-7 shows the enabling and disabling outputs through pin configuration and I^{2}C. Note that the OE pin must be low **and** OE bit must be "1" for the output to be active by default. The output enable bits are OUTAB_EN (R7[1]) and OUTCD_EN (R7[8]).

表 7-7. OE Functionality

OE Pin	OE Pin Polarity	Software Output Enable OUTx_EN	OUTx
High	Active low	0	Off
High	Active low	1	Off
Low	Active low	0	Off
Low	Active low	1	On
High	Active high	0	Off
High	Active high	1	On
Low	Active high	0	Off
Low	Active high	1	Off

7.4.4.2 Output Enable Polarity

OE pin polarity is programmable and is active low by default. When the OE pin is active low, the internal pulldown resistor is automatically enabled, and the internal pullup resistor is disabled. When the OE pin is active high, the internal pullup resistor is automatically enabled, and the internal pulldown resistor is disabled. By default, clock outputs are always enabled when the OE pin is floating. The OE pin polarity is set by OE_PIN_POLARITY (R7[0]) as '1' for active-low (default), or '0' for active-high.

7.4.4.3 Separate Output Enable

The I2C_ADDR pin can be reconfigured as a second output enable pin. Set SEPARATE_OE_EN (R11[14]) to enable this functionality. This bit is OTP programmable. When I2C_ADDR is used as an output enable pin, the OE pin controls OUTA and OUTB and the I2C_ADDR pin controls OUTC and OUTD. The OE_PIN_POLARITY (R7[0]) bit applies to the OE and I2C_ADDR pins in this case.

7.4.4.4 Output Disable Behavior

When the outputs are disabled, the outputs can be either forced low or tri-state, determined by OUTAB_DISABLE_STATE (R3[5]) for OUTA & OUTB and OUTCD_DISABLE_STATE (R3[6]) for OUTC & OUTD. The output is low for a '0', or tri-state for a '1'.

7.4.5 Device Default Settings

表 7-8 summarizes the default settings of the LMK3C0105V3 and LMK3C0105V1 at start-up for the four OTP pages. In I^{2}C mode, the Page 0 settings are loaded. For a full list of every default register setting, see *Device Registers*.

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表 7-8. LMK3C0105 Start-up Settings

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
VDD Supply Voltage	3.3V (LMK3C0105V33) 1.8V (LMK3C0105V18)			
OUTA/OUTB Frequency	25MHz	25MHz	25MHz	25MHz
OUTA/OUTB Output Format	LVCMOS, In-Phase	LVCMOS, In-Phase	LVCMOS, In-Phase	LVCMOS, In-Phase
OUTA/OUTB Enable	Enable	Enable	Enable	Enable
OUTA/OUTB Disable Behavior	GND	GND	GND	GND
OUTC/OUTD Frequency	25MHz	25MHz	25MHz	25MHz
OUTC/OUTD Output Format	LVCMOS, In-Phase	LVCMOS, In-Phase	LVCMOS, In-Phase	LVCMOS, In-Phase
OUTC/OUTD Enable	Enable	Enable	Enable	Enable
OUTC/OUTD Disable Behavior	GND	GND	GND	GND
REF_CTRL Behavior	REF_CLK, 25MHz	REF_CLK, 25MHz	REF_CLK, 25MHz	REF_CLK, 25MHz
FOD0 Frequency	200MHz	200MHz	200MHz	200MHz
FOD1 Frequency	200MHz	200MHz	200MHz	200MHz
SSC Enable	Disable	Enable	Enable	Enable
SSC Modulation Type	Down-spread	Down-spread	Down-spread	Down-spread
SSC Modulation Depth	0%	–0.1%	–0.3%	–0.5%
Pin 2 Function	I2C Address LSB Selection	I2C Address LSB Selection	I2C Address LSB Selection	I2C Address LSB Selection

7.5 Programming

The host (DSP, Microcontroller, FPGA, and so forth) configures and monitors the LMK3C0105 through the I^2C port. The host reads and writes to a collection of control bits called the register set. The device blocks can be controlled and monitored through a specific grouping of bits located within the register space. In the absence of the host, the LMK3C0105 can be configured to operate in OTP mode from one of four of the on-chip OTP pages, stored in the internal EFUSE, depending on the state of REF_CTRL and OTP_SELx pins. The EFUSE is one-time programmed by TI, and is not rewritable. This means that the values of the registers that are automatically loaded from the EFUSE at power-up cannot be customized. However, the values of the registers can be changed subsequently via the I^2C register interface. Within the device registers, there are certain bits that have read/write access. Other bits are read-only (an attempt to write to a read only bit does not change the state of the bit). Certain device registers and bits are reserved meaning that the fields must not be changed from the default reset state.

7.5.1 I^2C Serial Interface

The I^2C port on the LMK3C0105 works as a peripheral device and supports both the 100kHz standard mode and 400kHz fast-mode operations. Fast mode imposes a glitch tolerance requirement on the control signals. Therefore, the input receivers ignore pulses of less than 50ns duration. The I^2C timing requirements are provided in the *I2C Interface Specification*. 図 7-5 shows the timing diagram.

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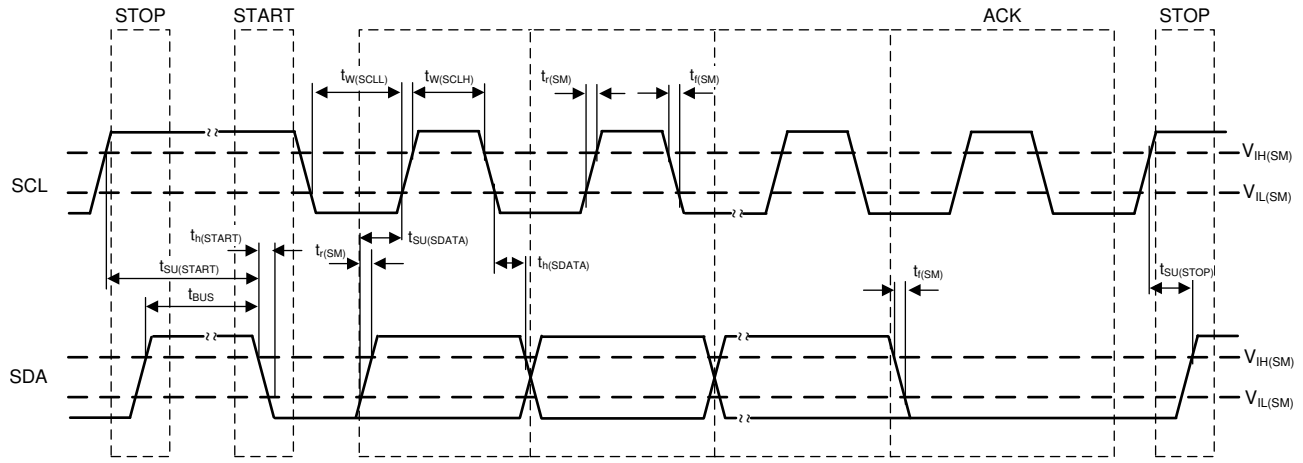

図 7-5. I²C Timing Diagram

The LMK3C0105 is accessed through a 7-bit peripheral address transmitted as part of an I²C packet. Only the device with a matching peripheral address responds to subsequent I²C commands. In I²C mode, the LMK3C0105 allows up to four unique peripheral devices to occupy the I2C bus based on the pin strapping of I2C_ADDR (tied to VDD, GND, SDA, or SCL). By default, the device peripheral address is 0b11010xx (the two LSBs are determined by the I2C_ADDR pin). The full address can be configured through I²C.

During the data transfer through the I²C interface, one clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. The start data transfer condition is characterized by a high-to-low transition on the SDA line while SCL is high. The stop data transfer condition is characterized by a low-to-high transition on the SDA line while SCL is high. The start and stop conditions are always initiated by the controller. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit and bytes are sent MSB first. The LMK3C0105 has an 8-bit register address, followed by a 16-bit data word.

The acknowledge bit (A) or non-acknowledge bit (A') is the 9th bit attached to any 8-bit data byte and is always generated by the receiver to inform the transmitter that the byte has been received (when A = 0) or not (when A' = 0). A = 0 is done by pulling the SDA line low during the 9th clock pulse and A' = 0 is done by leaving the SDA line high during the 9th clock pulse.

The I²C controller initiates the data transfer by asserting a start condition which initiates a response from all peripheral devices connected to the serial bus. Based on the 8-bit address byte sent by the controller over the SDA line (consisting of the 7-bit peripheral address (MSB first) and an R/W' bit), the device whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data transfer with the controller.

After the data transfer occurs, stop conditions are established. In write mode, the controller asserts a stop condition to end data transfer during the 10th clock pulse following the acknowledge bit for the last data byte from the peripheral. In read mode, the controller receives the last data byte from the peripheral but does not pull SDA low during the 9th clock pulse. This is known as a non-acknowledge bit. By receiving the non-acknowledge bit, the peripheral knows the data transfer is finished and enters the idle mode. The controller then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition. 図 7-6 and 図 7-7 show the sequence for block writes and block reads using the LMK3C0105, respectively.

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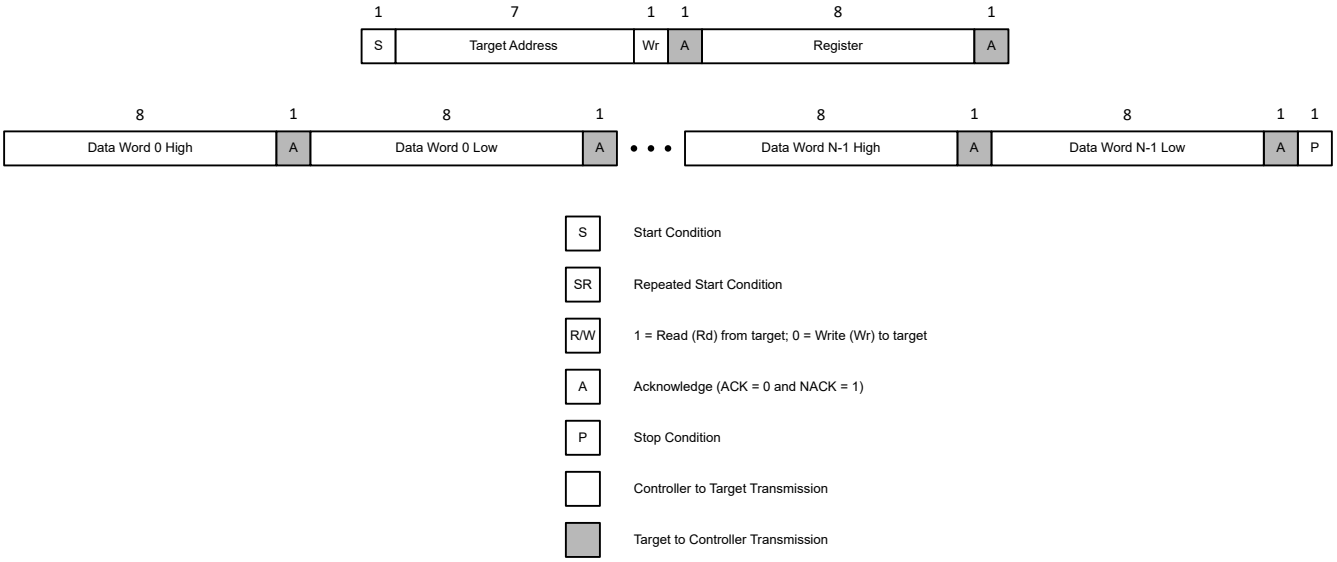

図 7-6. Generic Block Write Sequence

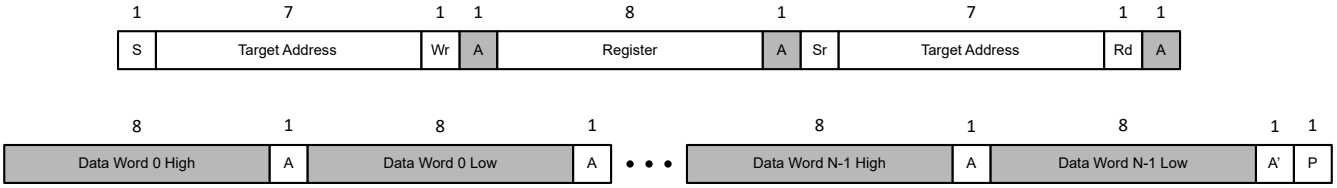

図 7-7. Generic Block Read Sequence

7.5.2 One-Time Programming Sequence

The upper register space includes all registers from R13 onward, as well as I2C_ADDR (R12[15:8]). Unlocking the upper register space is performed by writing 0x5B to UNLOCK_PROTECTED_REG (R12[7:0]), leaving I2C_ADDR unchanged.

There are six fields that can have different values depending on the EFUSE page loaded at device start-up.

- OUTA/OUTB Output Format
- OUTA/OUTB Enable
- OUTC/OUTD Output Format
- OUTC/OUTD Enable
- SSC Enable
- SSC Configuration (either preconfigured or custom)

All other fields retain the same value across all four EFUSE pages. For generating custom configurations, contact TI.

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8 Device Registers

8.1 Register Maps

表 8-1 lists the LMK3C0105 Device registers. All register offset address not listed in 表 8-1 can be considered as reserved locations. The register contents of reserved locations must not be modified.

表 8-1. LMK3C0105 Registers

Address	Acronym	Section
0x0	R0	R0
0x1	R1	R1
0x2	R2	R2
0x3	R3	R3
0x4	R4	R4
0x5	R5	R5
0x6	R6	R6
0x7	R7	R7
0x8	R8	R8
0x9	R9	R9
0xA	R10	R10
0xB	R11	R11
0xC	R12	R12
0xEE	R238	R238

Complex bit access types are encoded to fit into small table cells. 表 8-2 shows the codes that are used for access types in this section.

表 8-2. LMK3C0105 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WL	W L	Write Locked, requires UNLOCK_PROTECTED_REG (R12[7:0]) = 0x5B to unlock and write successfully

8.1.1 R0 Register (Address = 0x0) [reset = 0x0861/0x0863]

R0 is shown in 表 8-3.

Return to the Summary Table.

表 8-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	DIG_CLK_N_DIV	R/W	0x02	Digital State Machine clock rate. Derived from the FOD frequency sourced by the CH0_FOD_SEL multiplexer. The target for the frequency is 50MHz maximum. The actual divide value is the DIG_CLK_N_DIV value plus 2. This field is stored in the EFUSE.

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表 8-3. R0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
9:3	FOD0_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD0 frequency. This field is stored in the EFUSE.
2:1	SUP_LVL_SEL	R/W	0x0 (V33) 0x1 (V18)	Operating voltage for core supply LDO. This field is factory programmed, and **must not** be overwritten with a different value than the programmed value. Supply voltage on VDD and VDDO pins **must not** exceed the selected voltage value + 10%. 0: 3.3V 1: 1.8V 2: 2.5V
0	OTP_BURNT	R/WL	0x1	Indicates that the EFUSE has been programmed. If this field is '1', the EFUSE is programmed.

8.1.2 R1 Register (Address = 0x1) [reset = 0x5599]

R1 is shown in 表 8-4.

Return to the Summary Table.

表 8-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	FOD0_NUM[23:16]	R/W	0x55	High byte of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
7:0	Reserved	R/W	0x99	Reserved, only write 0x99 to this field.

8.1.3 R2 Register (Address = 0x2) [reset = 0xC28F]

R2 is shown in 表 8-5.

Return to the Summary Table.

表 8-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD0_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

8.1.4 R3 Register (Address = 0x3) [reset = 0x1804]

R3 is shown in 表 8-6.

Return to the Summary Table.

表 8-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	FOD1_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD1 frequency. This field is stored in the EFUSE.
8	CH1_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 1. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
7	Reserved	R/W	0x0	Reserved, only write '0' to this field.
6	OUTCD_DISABLE_STATE	R/W	0x0	When OUTC and OUTD are disabled, this bit selects whether the OUTC and OUTD pins are forced to GND or tri-state. This field is stored in the EFUSE. 0h: Forced to GND on disable. 1h: Tri-state on disable.

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表 8-6. R3 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5	OUTAB_DISABLE_STATE	R/W	0x0	When OUTA and OUTB are disabled, this bit selects whether the OUTA and OUTB pins are forced to GND or tri-state. This field is stored in the EFUSE. 0h: Forced to GND on disable. 1h: Tri-state on disable.
4	CH0_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 0. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
3	Reserved	R/W	0x0	Reserved, only write '0' to this tool.
2:0	CH0_DIV	R/W	0x4	Divider value for Channel Divider 0. This field is stored in the EFUSE. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40

8.1.5 R4 Register (Address = 0x4) [reset = 0x0000]

R4 is shown in 表 8-7.

Return to the Summary Table.

表 8-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	N/A	Reserved, do not write to this field.
14:2	SSC_STEPS	R/W	0x0000	Number of steps in each segment of the triangular profile for SSC. See セクション 7.4.2.3 for instructions to calculate this value. This field is stored in the EFUSE.
1	SSC_MOD_TYPE	R/W	0x0	Selects between down-spread or center-spread modulation for custom SSC configurations. This field is stored in the EFUSE. 0h: Down-spread modulation. 1h: Center-spread modulation.
0	SSC_EN	R/W	0x0	Enable SSC. This field is stored in the EFUSE. 0h: SSC Disabled. 1h: SSC Enabled.

8.1.6 R5 Register (Address = 0x5) [reset = 0x0000]

R5 is shown in 表 8-8.

Return to the Summary Table.

表 8-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SSC_STEP_SIZE	R/W	0x0000	Numerator increment value per step for SSC. See セクション 7.4.2.3 for instructions to calculate this value. This field is stored in the EFUSE.

8.1.7 R6 Register (Address = 0x6) [reset = 0x0AA7]

R6 is shown in 表 8-9.

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Return to the Summary Table.

表 8-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CH1_DIV	R/W	0x0	Divider value for Channel Divider 1. This field is stored in the EFUSE. 0h: Channel Divider disabled. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40
12:5	FOD1_NUM[23:16]	R/W	0x55	High byte of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
4:3	Reserved	R/W	0x0	Reserved, only write '0' to this field.
2:0	OUTAB_FMT	R/W	0x7	Selects the output format for OUTA/OUTB. This field is stored in the EFUSE. 0h: Reserved. 1h: Reserved. 2h: Reserved. 3h: Reserved. 4h: LVCMOS, OUTA enabled, OUTB disabled. 5h: LVCMOS, OUTA disabled, OUTB enabled. 6h: LVCMOS, OUTA enabled, OUTB enabled, 180 degrees out of phase. 7h: LVCMOS, OUTA enabled, OUTB enabled, OUTA and OUTB in phase.

8.1.8 R7 Register (Address = 0x7) [reset = 0x5D1F]

R7 is shown in 表 8-10.

Return to the Summary Table.

表 8-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	N/A	0x0	Reserved, do not write to this field.
14:13	REF_CTRL_PIN_FUNC	R/W	0x2	Sets the function of the REF_CTRL pin. This field is stored in the EFUSE. 0h: REF_CTRL pin disabled, pulled to GND. 1h: REF_CTRL pin disabled, tri-state. 2h: REF_CTRL pin functions as an additional LVCMOS REF_CLK output. 3h: REF_CTRL pin functions as "clock ready" signal.
12:11	REF_CLK_DIV	R/W	0x3	REF_CLK output divisor value when REF_CTRL is used as REF_CLK. This field is stored in the EFUSE. 0h: REF_CLK disabled. 1h: FOD / 2. 2h: FOD / 4. 3h: FOD / 8.
10	Reserved	R/W	0x1	Reserved. Do not write any value other than '1' to this field.
9	REF_CLK_FOD_SEL	R/W	0x0	Select the FOD used to generate the REF_CLK output. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.

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表 8-10. R7 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
8	OUTCD_EN	R/W	0x1	Output Enable bit for OUTC and OUTD. This field is stored in the EFUSE. 0h: OUTC and OUTD are disabled. 1h: OUTC and OUTD are enabled.
7	OUTCD_CH_SEL	R/W	0x0	Selects the source for OUTC/OUTD. This field is stored in the EFUSE. 0h: OUTC and OUTD are sourced from Channel Divider 0. 1h: OUTC and OUTD are sourced from Channel Divider 1.
6:5	Reserved	R/W	0x0	Reserved, only write '0' to this field.
4:2	OUTCD_FMT	R/W	0x7	Selects the output format for OUTC and OUTD. This field is stored in the EFUSE. 0h: Reserved. 1h: Reserved. 2h: Reserved. 3h: Reserved. 4h: LVCMOS, OUTC enabled, OUTD disabled. 5h: LVCMOS, OUTC disabled, OUTD enabled. 6h: LVCMOS, OUTC enabled, OUTD enabled, 180 degrees out of phase. 7h: LVCMOS, OUTC enabled, OUTD enabled, OUTC and OUTD in phase.
1	OUTAB_EN	R/W	0x1	Output Enable bit for OUTA and OUTB. This field is stored in the EFUSE. 0h: OUTA and OUTB are disabled. 1h: OUTA and OUTB are enabled.
0	OE_PIN_POLARITY	R/W	0x1	OE pin polarity selection. This bit does not affect the polarity of the OUTx_EN bits, only the OE pin. This field is stored in the EFUSE. 0h: OE is active high (OE tied to VDD enables outputs). 1h: OE is active low (OE tied to GND enables outputs).

8.1.9 R8 Register (Address = 0x8) [reset = 0xC28F]

R8 is shown in 表 8-11.

Return to the Summary Table.

表 8-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD1_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

8.1.10 R9 Register (Address = 0x9) [reset = 0x3000/0x1000]

R9 is shown in 表 8-12.

Return to the Summary Table.

表 8-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OTP_ID	R/W	0x3 (V33) 0x1 (V18)	Configurable field for identifying the OTP configuration. Can be used in I2C mode as a 4-bit spare field. This field is stored in the EFUSE.

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表 8-12. R9 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
11:9	SSC_CONFIG_SEL	R/W	0x0	SSC modulation configuration. If center-spread modulation is desired, then custom SSC configuration is required. Four preconfigured down-spread modulation depths are also available. Any other modulation depths require custom SSC configuration. This field is stored in the EFUSE. The preconfigured SSC options are specifically for 100MHz clock outputs. For other output frequencies, TI recommends creating a custom SSC configuration. 0h: Custom SSC Configuration - see セクション 7.4.2.3 for details on creating a custom configuration. 1h: –0.10% preconfigured down-spread. 2h: –0.25% preconfigured down-spread. 3h: –0.30% preconfigured down-spread. 4h: –0.50% preconfigured down-spread. All other values: Reserved
8:0	Reserved	R/W	0x000	Reserved, only write '0' to this field.

8.1.11 R10 Register (Address = 0xA) [reset = 0x0010]

R10 is shown in 表 8-13.

Return to the Summary Table.

表 8-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14:11	PROD_REVID	R	N/A	Product revision identifier.
10	CLK_READY	R	N/A	CLK_READY status. The REF_CTRL pin mirrors this status signal when the pin functions as a "clock ready" signal.
9	Reserved	R	N/A	Reserved, do not write to this field.
8	RB_PIN_15	R	N/A	Readback of the REF_CTRL pin.
7	RB_PIN_4	R	N/A	Readback of the OTP_SEL1/SDA pin.
6	RB_PIN_3	R	N/A	Readback of the OTP_SEL0/SCL pin.
5	RB_PIN_2	R	N/A	Readback of the I2C_ADDR pin.
4	DEV_IDLE_STATE_SEL	R/W	0x1	This bit controls the behavior of the device when both outputs are disabled. Placing the device into a low-power state is not recommended for PCIe applications, as the time to re-enable the clocks is extended. This field is stored in the EFUSE. 0h: When both outputs are disabled, the outputs are muted, and the device is placed into a low-power state. 1h: When both outputs are disabled, the outputs are muted. The device does not enter a low-power state.
3	PIN_RESAMPLE_DIS	R/W	0x0	This bit controls the resampling of the device pins when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: Pin resampling is enabled. When exiting the low power mode, the I2C_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and I2C_ADDR pins are resampled. If I2C_ADDR is high, the device enters OTP Mode. 1h: Pin resampling is disabled. When exiting the low power mode, the I2C_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and I2C_ADDR pins are not resampled. The device remains in I2C Mode.

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表 8-13. R10 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2	OTP_AUTOLOAD_DIS	R/W	0x0	This bit controls the behavior of the device when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: OTP autoload is enabled. When exiting the low power mode, the contents of OTP Page 0 are written to the device registers. 1h: OTP autoload is disabled. When exiting the low power mode, the contents of OTP Page 0 are not written to the device registers.
1	PDN	R/W	0x0	Writing a '1' to this bit puts the device into a low power state.
0	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.

8.1.12 R11 Register (Address = 0xB) [reset = 0x0000]

R11 is shown in 表 8-14.

Return to the Summary Table.

表 8-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14	SEPARATE_OE_EN	R/W	0x0	This bit enables the separate output enable functionality of the device. If this bit is a '1', then I2C_ADDR_LSB_SEL must be set to '0'. This field is stored in the EFUSE. 0h: Pin 1 is the output enable for OUTA, OUTB, OUTC, and OUTD. 1h: Pin 1 is the output enable for OUTA and OUTB, Pin 2 is the output enable for OUTC and OUTD.
13:0	Reserved	R/W	0x0000	Reserved, do not write to this field.

8.1.13 R12 Register (Address = 0xC) [reset = 0xE800]

R12 is shown in 表 8-15.

Return to the Summary Table.

表 8-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_ADDR_LSB_SEL	R/WL	0x1	I2C peripheral address source. If this bit is a '1', SEPARATE_OE_EN must be '0'. This field is stored in the EFUSE. 0h: I2C peripheral address comes entirely from the I2C_ADDR field. 1h: The two lowest bits of the I2C peripheral address come from the FMT_ADDR pin, all other bits come from R12[14:10].
14:8	I2C_ADDR	R/WL	0x68	I2C peripheral address. After writing to this field, the device responds to the new I2C address. This field is stored in the EFUSE.
7:0	UNLOCK_PROTECTED_REG	R/W	0x00	This field locks all registers from R13 onward, in addition to R12[15:8]. Registers R13 onward are largely device calibration registers, and must not have contents modified. These registers can be read from normally regardless of the unlock status. 5Bh: Unlocks register writes for R12[15:8] and above. Any other value: R12[15:8] and above ignore all writes.

8.1.14 R238 Register (Address = 0xEE) [reset = 0x0000]

R246 is shown in 表 8-16.

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表 8-16. R246 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BAWFREQ_OFFSET_FIXEDLUT	R/WL	0x0000	Offset value from 2467MHz for the BAW frequency. Signed 16-bit integer value. This field is stored in the EFUSE. Each bit of this fields corresponds to 128ppm of frequency deviation. **This field varies from part to part.** This field is for calculation purposes only, the device does not use this register for any internal calculation. Do **NOT** write to this field.

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9 Application and Implementation

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9.1 Application Information

The LMK3C0105 is a reference-less BAW-based clock generator that can be used to provide reference clocks for various applications, including PCIe reference clocking and 1Gb/10Gb Ethernet Switches.

9.2 Typical Applications

9.2.1 Application Block Diagram Examples

図 9-1 shows the use of the LMK3C0105 for replacement of crystals and crystal oscillators on a Gigabit Ethernet Switch application

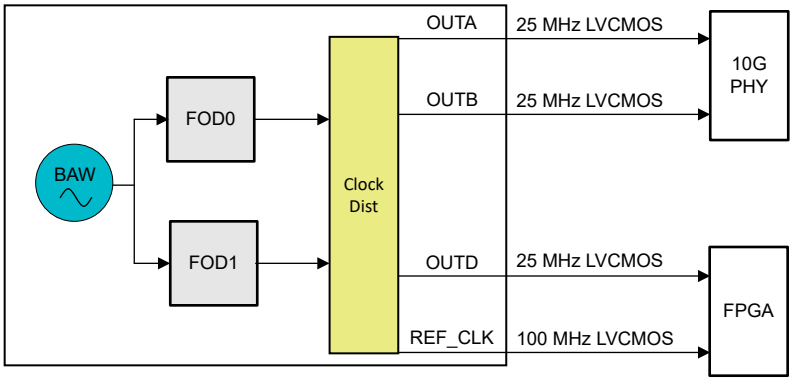

図 9-1. Crystal and Oscillator Replacement Example

9.2.2 Design Requirements

Consider a typical Gigabit Ethernet Switch application. In a system such as this, the clocks are expected to be available upon request without the need for any additional device-level programming. The default device configuration outputs five 25MHz LVCMOS clocks, all enabled by default. A typical output clock requirement in this application is two 25MHz LVCMOS clocks for the PHY, and both a 25MHz and 100MHz LVCMOS clock for the FPGA. The section below describes the detailed design procedure to generate the required output frequencies for the above scenario using the LMK3C0105.

9.2.3 Detailed Design Procedure

Design of all aspects of the LMK3C0105 is straightforward, and software support is available to assist in frequency planning and part programming. This design procedure gives a straightforward outline of the process.

1. Frequency Planning
   a. The first step of designing an LMK3C0105 configuration is to determine the FOD frequencies that are required to generate the required output frequencies. The process is as such:
      i. If both output frequencies are the same, and have the same SSC settings (that is, both use SSC or both do not use SSC), only one FOD is required.
      ii. If both output frequencies are different, but have the same SSC settings, the outputs can share an FOD to conserve current. If both frequencies can be generated from dividing a single valid FOD frequency by the channel divider options, then the second FOD can be disabled. Otherwise, both

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FODs must be used. If both outputs require SSC, then this frequency plan cannot be supported by the LMK3C0105 device.

iii. If one output requires SSC and the other does not, then the SSC output must use FOD0 and the non-SSC output must use FOD1.

b. If SSC is being used, determine whether or not a preconfigured down-spread modulation, a custom down-spread modulation, or a center-spread modulation is required for the application. If a custom configuration is required, follow the steps outlined in *セクション 7.4.2.3*.

c. Set the digital clock divider such that the digital clock frequency is as close to 50MHz as possible.

d. Determine the REF_CTRL pin functionality. If this is used as an additional LVCMOS reference clock, verify that the desired frequency can be generated based on the FOD0 and FOD1 frequencies, as the divider range for the REF_CLK output is /2, /4, or /8 only.

i. Keep in mind that if SSC is used on FOD0, and the REF_CLK source is FOD0, this output now has SSC as well.

2. Setting the Output Formats

a. The output formats that are required are based upon the number of clocks needed in the system. For crystal replacement, this is most often a collection of 24MHz, 25MHz, 27MHz, or 50MHz LVCMOS clocks.

b. OUTA and OUTB, or OUTC and OUTD, can be in phase, opposite, or individually enabled or disabled. OUTA and OUTC are always in phase. This allows for the generation of up to five LVCMOS clocks at a time, up to four of which can be in phase.

i. For LVCMOS outputs, the VDDO_x voltage MUST match the VDD voltage if VDD is 1.8V or 2.5V.

3. Output Enable Behavior

a. The output enable pin is active low by default, with an internal pulldown resistor to GND. If this functionality is not desired, then OE_PIN_POLARITY can be set to '0' to change the behavior of the OE pin to active-high. If this is done, the internal pulldown is disabled, and an internal pullup to VDD is used.

b. Determine whether or not both outputs being disabled means that the device enters low-power mode. While this is able to conserve current, low-power mode is not recommended for any applications where the clocks must turn back on quickly, such as PCIe clocking.

For the 10GB PHY, the following settings are required:

1. One FOD can be used to generate all outputs. As such, FOD0 can be set to have an output frequency of 200MHz, with Channel Divider 0 set to divide by 8. Often, if two clocks of the same frequency are required by a single device, these clocks need to be in phase. Both output drivers select Channel Divider 0. Output Driver 0 is set for LVCMOS in-phase, and Output Driver 1 is set for LVCMOS OUTD only. When configured for OUTD only, OUTD is in phase with OUTA.

a. DIG_CLK_N_DIV must be set to two to set the state machine clock properly. The state machine clock must be as close to 50MHz as possible without exceeding this frequency. In this case, DIG_CLK_N_DIV is set to 2 for a total divide of 4. 式 9 shows the relationship between the digital state machine frequency, the frequency selected by the CH0_FOD_SEL multiplexer, and the DIG_CLK_N_DIV field. Write the DIG_CLK_N_DIV field only while the device is in the low power state.

2. The REF_CTRL pin is used for generating the 100MHz LVCMOS clock. Set REF_CLK_FOD_SEL to 0 for selecting FOD0 as the REF_CTRL clock source. REF_CLK_DIV must be set to 1 for a divide by 2 from FOD0. Set REF_CTRL_PIN_FUNC to 2 for setting the REF_CTRL pin as an output clock.

$$F_{DIG} = \frac{F_{CH0\_FOD\_SEL}}{2 + \text{DIG\_CLK\_N\_DIV}} \quad (9)$$

where F_{DIG} is the digital state machine clock frequency and $F_{CH0\_FOD\_SEL}$ is the frequency selected by the CHO_FOD_SEL multiplexer

9.2.4 Example: Changing Output Frequency

If the user wants to change the output from 25MHz LVCMOS on OUTA, OUTB, and OUTD to 24MHz differential LVCMOS clocks on all outputs, the following example details this process. The value of the

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BAWFREQ_OFFSET_FIXEDLUT field for this example is 0x3701. The steps for changing the frequency are as follows:

1. Determine the BAW frequency of the device. This is critical for all following calculations. From 式 4, if BAWFREQ_OFFSET_FIXEDLUT is 0x3701, then the BAW frequency of this device is approximately 2471.446441856MHz.
2. Determine the channel divider settings and required FOD frequency. If the output frequency is 24MHz, and the range of the FODs is from 100MHz to 400MHz, then a channel divider value of at least 5 is required to generate the output. As there is not a divide by 5 option, and REF_CLK must also have a clock (see CH0_DIV, CH1_DIV, and REF_CLK_DIV), a divide by 8 is required. From here, 24MHz times 8 yields an FOD output frequency of 192MHz. If OUTC/OUTD were a different frequency, then using FOD1 can be required if both frequencies cannot be generated by dividing down from the same FOD frequency.
3. Set the FOD divide values. Use 式 1 to calculate the integer divide value FOD0_N_DIV = floor(2471.446441856/192) = 12. From 式 2, the numerator divide value FOD0_NUM = int(((2471.446441856/192) - 12) x 2^{24}) = 14631693
4. Write the desired settings to the device registers. This includes the divider settings listed above, as well as the output driver settings. Follow the procedure outlined in 図 7-4:
   a. Set PDN = 1.
   b. Set FOD0_N_DIV = 12 and FOD0_NUM = 14631693.
   c. Set CH0_DIV, and REF_CLK_DIV to divide by 8 (by default, OUTCD_CH_SEL is set to select Channel Divider 0).
   d. Set OUTAB_FMT and OUTCD_FMT to select in-phase LVCMOS as the output format.
   e. Set REF_CTRL_PIN_FUNC to output REF_CLK.
   f. Set OTP_AUTOLOAD_DIS to 1 (disable the OTP Page 0 autoload feature).
   g. Set DIG_CLK_N_DIV = 2 to set the digital state machine clock to 48MHz, based on 式 9
   h. Set PDN = 0

The time required for the frequency change to take affect is typically on the order of 1ms between issuing PDN = 0 and the output clocks starting at the desired frequency.

9.2.5 Crosstalk

Performance degradation can occur in the LMK3C0105 due to crosstalk in the device when the outputs are operating at different frequencies. 表 9-1 displays the performance of the LMK3C0105 outputs for common LVCMOS frequencies. Contact TI for measurement of additional combinations for impact of crosstalk on output performance.

表 9-1. LMK3C0105 LVCMOS Output Crosstalk

FOD0 Frequency (MHz)	FOD1 Frequency (MHz)	OUTA Frequency (MHz) (2)	OUTC Frequency (MHz)(2)	Typical OUTA RMS Jitter (fs) (1) (3)	Typical OUTC RMS Jitter (fs) (1) (3)
240	250	24	25	852	716
240	270	24	27	457	371
240	200	24	50	832	779
250	240	25	24	784	717
250	270	25	27	757	787
250	200	25	50	215	516
270	240	27	24	429	367
270	250	27	25	913	641
270	200	27	50	865	930
200	240	50	24	806	548
200	250	50	25	559	287
200	270	50	27	913	704

(1) Measured over 25°C to 105°C using differential LVCMOS output formats using VDD = VDDO_x = 3.3V, no SSC.
(2) OUTA and OUTC are generated using FOD0 and FOD1, respectively.

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(3) RMS Jitter measured over the 12kHz to 5MHz integration bandwidth.

9.3 Power Supply Recommendations

9.3.1 Power-Up Sequencing

The LMK3C0105 provides multiple power supply pins. Each power supply supports 1.8V, 2.5V, or 3.3V. Internal low-dropout regulators (LDO) source the internal blocks and allow each pin to be supplied with individual supply voltages. The VDD pin supplies the control pins, the serial interface, and the REF_CTRL pin. Therefore, any pullup resistors must be connected to the same domain as VDD.

If an output is not used, connect the corresponding VDDO_x rail to VDD. If the VDD and VDDO_x rails are the same voltage, TI recommends connecting these together directly. If VDD and the VDDO_x rails differ, VDD must ramp first, with VDDO_x no more than 5ms after.

9.3.2 Decoupling Power Supply Inputs

Do not tie VDD and VDDO pins to ground. Use a separate ferrite bead to isolate the VDD and the VDDO supplies. If OUTA/OUTB and OUTC/OUTD are different frequencies, a separate ferrite bead must be used for each VDDO supply. For each supply voltage pin, a 0.1µF or 1µF capacitor must be placed very close to the pin.

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9.4 Layout

9.4.1 Layout Guidelines

For this example, follow these guidelines:

- Isolate outputs using a GND shield. Route all outputs as differential pairs.
- Isolate outputs to adjacent outputs when generating multiple frequencies.
- Avoid impedance jumps in the fan-in and fan-out areas when possible.
- Use five vias to connect the thermal pad to a solid GND plane. Full-through vias are preferred.
- Place decoupling capacitors with small capacitance values very close to the supply pins. Place the decoupling capacitors on the same layer or on the bottom layer directly underneath the device. Larger values can be placed more far away. Ferrite beads are recommended to isolate the different output supplies and the VDD supply.
- Use multiple vias to connect wide supply traces to the respective power planes.

9.4.2 Layout Example

Below are printed circuit board (PCB) layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB.

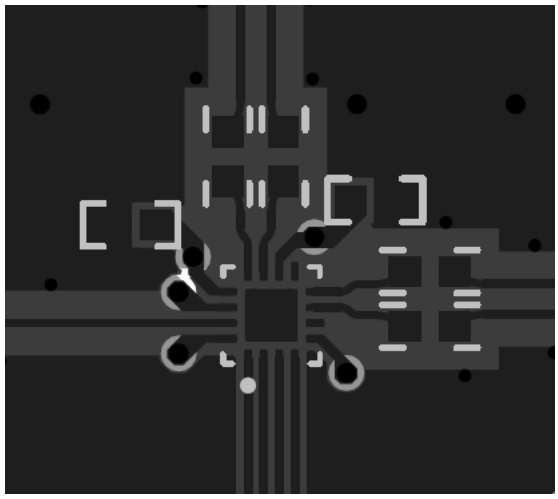

図 9-2. PCB Layout Example for LMK3C0105, Top Layer

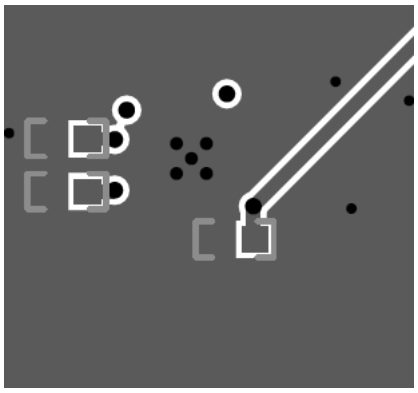

図 9-3. PCB Layout Example for LMK3C0105, Bottom Layer

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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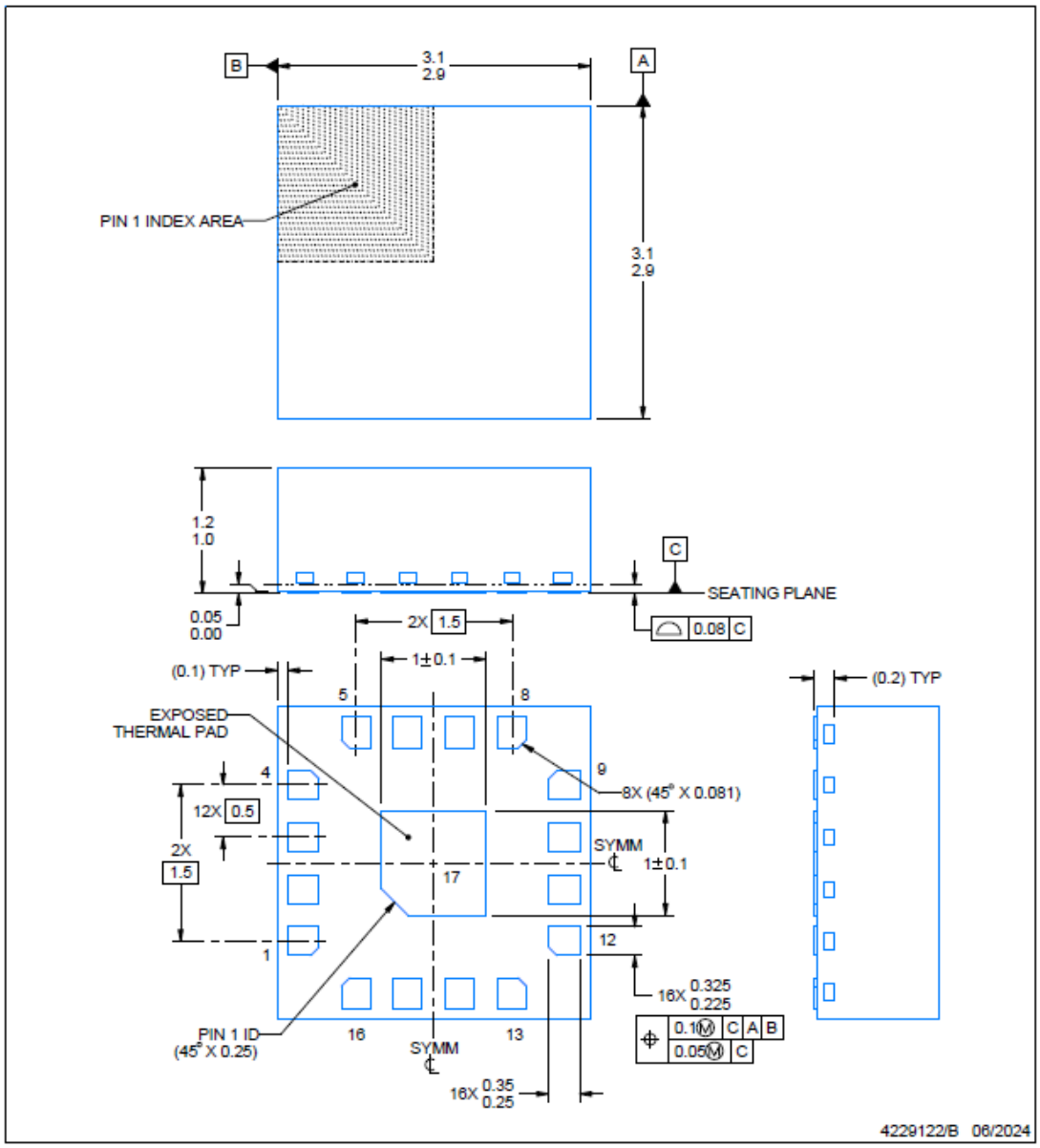
PACKAGE OUTLINE

RER0016A

TQFN - 1.2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

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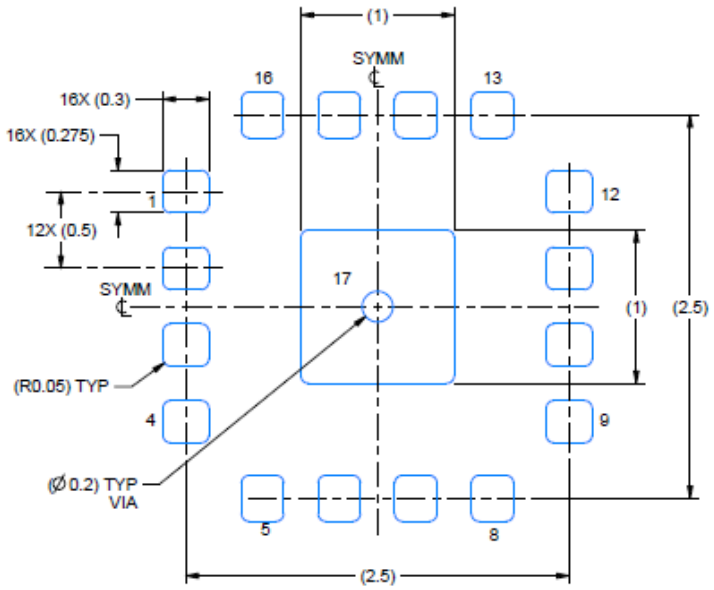
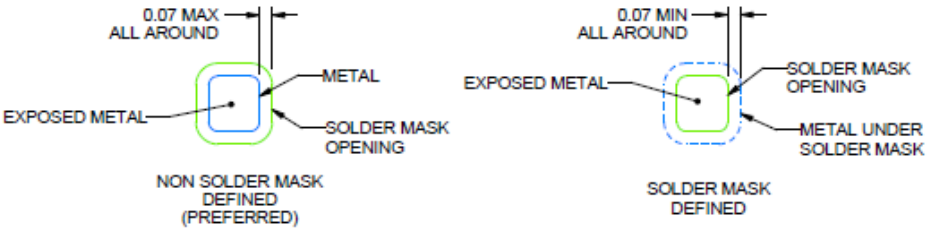
EXAMPLE BOARD LAYOUT

RER0016A — **TQFN - 1.2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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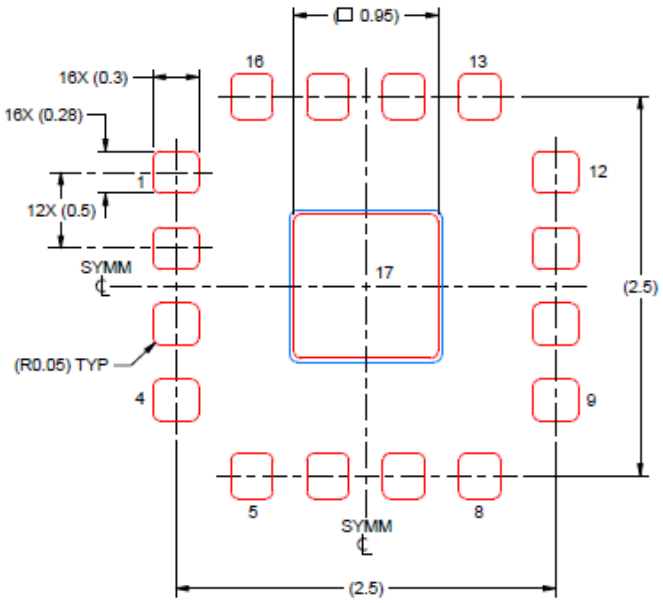
EXAMPLE STENCIL DESIGN

RER0016A — **TQFN - 1.2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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12.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
LMK3C0105V33RERR	ACTIVE	TQFN	RER	16	3000	RoHS & Green	NIPDAU	Level-2-260C-168 HR	-40 to 85	3CV1
LMK3C0105V18RERR	ACTIVE	TQFN	RER	16	3000	RoHS & Green	NIPDAU	Level-2-260C-168 HR	-40 to 85	3CV3

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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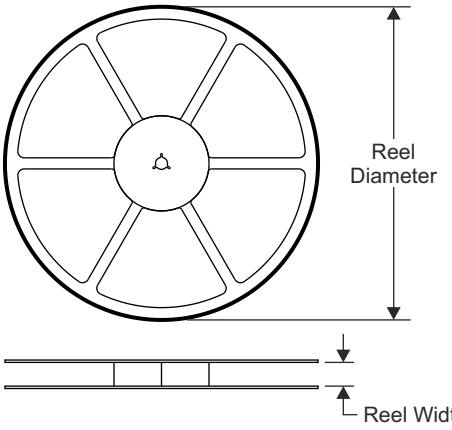
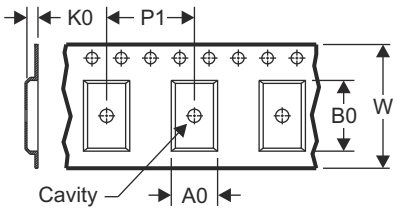
12.2 Tape and Reel Information

REEL DIMENSIONS

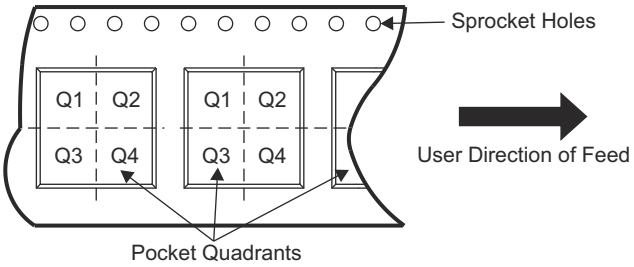


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK3C0105V33RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
LMK3C0105V18RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1

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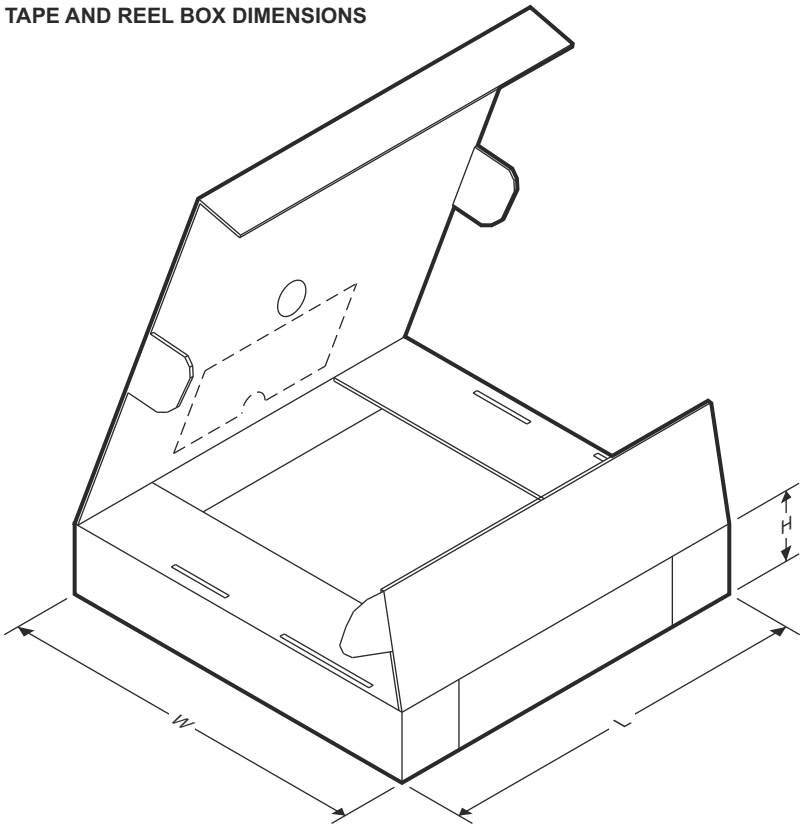
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK3C0105V33RERR	TQFN	RER0016A	16	3000	346	346	33
LMK3C0105V18RERR	TQFN	RER0016A	16	3000	346	346	33

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK3C0105V33RERR	ACTIVE	TQFN	RER	16	3000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	3CV33	Samples
LMK3C0105V33RERT	ACTIVE	TQFN	RER	16	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	3CV33	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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