LMK1D1208I I²C 構成可能な低付加ジッタ LVDS バッファ

1 特長

- 2 入力と 8 出力の高性能 LVDS クロック・バッファ・ファミリ
- 出力周波数:最大 2GHz
- 電源電圧:1.8V / 2.5V / 3.3V ±5%
- I²C プログラミングによるデバイス構成が可能
  - 入力および出力を個別にイネーブル / ディスエーブル可能
  - 出力の振幅を個別に選択可能 (標準またはブースト)
  - バンク入力マルチプレクサ
- IDX ピンを介してプログラム可能な 4 つの I²C アドレス
- 小さい付加ジッタ:156.25MHz 時、12kHz～20MHz の範囲で最大 60fs の RMS
  - 非常に小さい位相ノイズ・フロア:-164dBc/Hz (標準値)
- 非常に小さい伝搬遅延:575ps (最大値)
- 出力スキュー:20ps (最大値)
- ユニバーサル入力は LVDS、LVPECL、LVCMOS、HCSL、CML に対応
- フェイルセーフ入力
- LVDS リファレンス電圧 V_{AC_REF} を容量性結合入力に使用可能
- 産業用温度範囲:-40℃～105℃
- 利用可能なパッケージ:
  - 6mm × 6mm、40 ピン VQFN (RHA)

2 アプリケーション

- テレコミュニケーションおよびネットワーク機器
- 医療用画像処理
- 試験および計測機器
- ワイヤレス通信
- 業務用オーディオ / ビデオ

3 概要

LMK1D1208I は、I²C でプログラム可能な LVDS クロック・バッファです。このデバイスには 2 つの入力と 8 つの差動 LVDS クロック出力 (OUT0～OUT7) があり、クロック分配のスキューを最小限に抑えます。入力は LVDS、LVPECL、LVCMOS、HCSL、CML のいずれかに対応可能です。

LMK1D1208I は、50Ω 転送経路の駆動に特化して設計されています。シングルエンド・モードで入力を駆動する場合は、未使用の負入力ピンに適切なバイアス電圧を印加する必要があります (図 9-6 参照)。

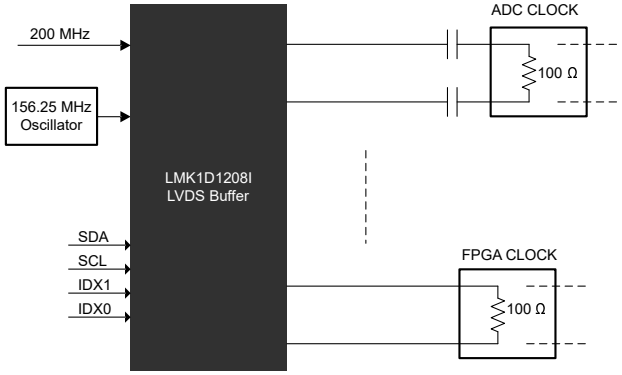
I²C プログラミングにより、このデバイスをシングル・バンク・バッファ (2 つの入力のうち 1 つを 8 つの出力ペアに分配)、またはデュアル・バンク・バッファ (各入力を 4 つの出力ペアに分配) として構成できます。各出力は、標準 (350mV) またはブースト (500mV) スイングのどちらかを持つよう構成できます。このデバイスは、I²C プログラミングによる各出力チャネルのイネーブルまたはディスエーブル機能も内蔵しています。LMK1D1208I にはフェイルセーフ入力があり、入力信号がない場合の出力の発振を防止し、VDD が供給される前に入力信号を受け入れます。

このデバイスは、1.8V、2.5V または 3.3V 電源で動作し、-40℃～105℃ (周囲温度) で動作が規定されています。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ (公称) (2)
LMK1D1208I	VQFN (40)	6.00mm × 6.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーションの例

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2022) to Revision A (June 2023)	Page
• 表のタイトルを「製品情報」から「パッケージ情報」に変更。	1
• Added the *Device Comparison* table for the LMK1Dxxxx buffer device family	3
• Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section	28

5 Device Comparison

DEVICE	DEVICE TYPE	FEATURES	OUTPUT SWING	PACKAGE	BODY SIZE
LMK1D2108	Dual 1:8	Global output enable and swing control through pin control	350 mV 500 mV	VQFN (48)	7.00 mm × 7.00 mm
LMK1D2106	Dual 1:6	Global output enable and swing control through pin control	350 mV 500 mV	VQFN (40)	6.00 mm × 6.00 mm
LMK1D2104	Dual 1:4	Global output enable and swing control through pin control	350 mV 500 mV	VQFN (28)	5.00 mm × 5.00 mm
LMK1D2102	Dual 1:2	Global output enable and swing control through pin control	350 mV 500 mV	VQFN (16)	3.00 mm × 3.00 mm
LMK1D1216	2:16	Global output enable control through pin control	350 mV 500 mV	VQFN (48)	7.00 mm × 7.00 mm
LMK1D1212	2:12	Global output enable control through pin control	350 mV 500 mV	VQFN (40)	6.00 mm × 6.00 mm
LMK1D1208P	2:8	Individual output enable control through pin control	350 mV 500 mV	VQGN (40)	6.00 mm × 6.00 mm
LMK1D1208I	2:8	Individual output enable control through I^2C	350 mV 500 mV	VQFN (40)	6.00 mm × 6.00 mm
LMK1D1208	2:8	Global output enable control through pin control	350 mV	VQFN (28)	5.00 mm × 5.00 mm
LMK1D1204P	2:4	Individual output enable control through pin control	350 mV	VQGN (28)	5.00 mm × 5.00 mm
LMK1D1204	2:4	Global output enable control through pin control	350 mV	VQFN (16)	3.00 mm × 3.00 mm

6 Pin Configuration and Functions

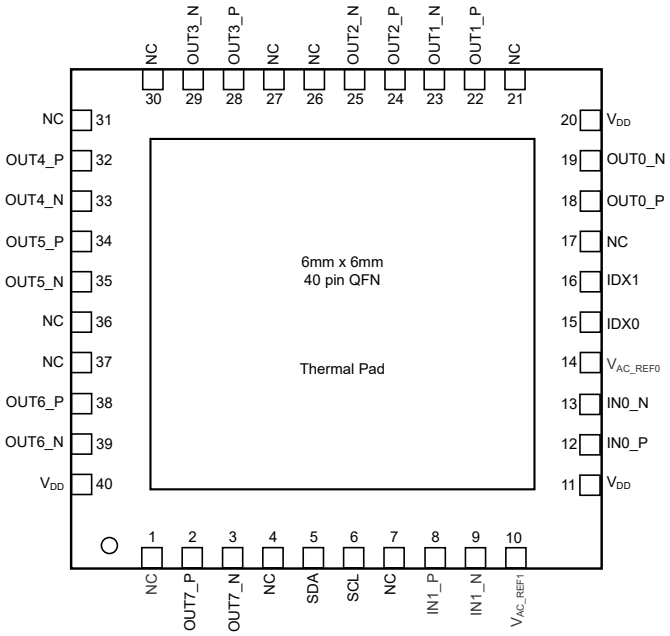


図 6-1. LMK1D1208I: RHA Package 40-Pin VQFN (Top View)

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	LMK1D1208I		
DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT			
IN0_P, IN0_N	12, 13	I	Primary: Differential input pair or single-ended input
IN1_P, IN1_N	8, 9	I	Secondary: Differential input pair or single-ended input.
I²C PROGRAMMING			
SDA	5	I/O	I²C data
SCL	6	I	I²C clock
IDX0	15	I,S,PU	I²C address bit[0]. This is a 2-level input that is decoded in conjunction with pin 15 to set the I²C address. It has internal 670-kΩ pullup.
IDX1	16	I,S, PU	I²C address bit[1]. This is a 2-level input that is decoded in conjunction with pin 16 to set the I²C address. It has internal 670-kΩ pullup.
BIAS VOLTAGE OUTPUT			
V_{AC_REF0}, V_{AC_REF1}	14, 10	O	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-µF capacitor to GND on this pin.
DIFFERENTIAL CLOCK OUTPUT			
OUT0_P, OUT0_N	18, 19	O	Differential LVDS output pair number 0
OUT1_P, OUT1_N	22, 23	O	Differential LVDS output pair number 1
OUT2_P, OUT2_N	24, 25	O	Differential LVDS output pair number 2
OUT3_P, OUT3_N	28, 29	O	Differential LVDS output pair number 3
OUT4_P, OUT4_N	32, 33	O	Differential LVDS output pair number 4
OUT5_P, OUT5_N	34, 35	O	Differential LVDS output pair number 5
OUT6_P, OUT6_N	38, 39	O	Differential LVDS output pair number 6
OUT7_P, OUT7_N	2, 3	O	Differential LVDS output pair number 7

表 6-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	LMK1D1208I		
SUPPLY VOLTAGE			
V_{DD}	11, 20, 40	P	Device power supply (1.8 V, 2.5 V, or 3.3 V)
GROUND			
DAP	DAP	G	Die Attach Pad. Connect to the printed circuit board (PCB) ground plane for heat dissipation.
NO CONNECT			
NC	1, 4, 7, 17, 21, 26, 27, 30, 31, 36, 37	—	No connection. Leave floating.

(1) The definitions below define the I/O type for each pin.

- I = Input
- O = Output
- I / O = Input / Output
- PU = Internal 670-kΩ Pullup
- S = Hardware Configuration Pin
- P = Power Supply
- G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	3.6	V
V_{IN}	Input voltage	–0.3	3.6	V
V_O	Output voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_J	Junction temperature		135	°C
T_{stg}	Storage temperature (2)	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Device unpowered

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
Supply Ramp	Supply voltage ramp	Requires monotonic ramp (10-90% of V_{DD})	0.1		20	ms
T_A	Operating free-air temperature		–40		105	°C
T_J	Operating junction temperature		–40		135	°C

7.4 Thermal Information

THERMAL METRIC(1)		LMK1D1208I VQFN 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

V_{DD} = 1.8 V ± 5 %, –40°C ≤ T_A ≤ 105°C. Typical values are at V_{DD} = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
IDD_{STAT}	LMK1D1208I	All-outputs enabled and unterminated, f = 0 Hz (AMP_SEL =1)		55		mA
IDD_{100M}	LMK1D1208I	All-outputs enabled, R_L = 100 Ω, f =100 MHz (AMP_SEL = 0, default)		75	95	mA
IDD_{100M}	LMK1D1208I	All-outputs enabled, RL = 100 Ω, f =100 MHz, AMP_SEL = 1			110	mA
IDX INPUT CHARACTERISTICS (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
V_{IH}	Input high voltage	Minimum input voltage for a logical "1" state	0.7 × V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input low voltage	Maximum input voltage for a logical "0" state	–0.3		0.3 × V_{CC}	V
I_{IH}	Input high current	V_{DD} can be 1.8V/2.5V/3.3V with V_{IH} = V_{DD}			30	µA
I_{IL}	Input low current	V_{DD} can be 1.8V/2.5V/3.3V with V_{IH} = V_{DD}	–30			µA
$R_{pull-up(IDX)}$	Input pullup resistor			670		kΩ
I^2C INTERFACE CHARACTERISTICS (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
V_{IH}	Input high voltage		0.7 × V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input low voltage		–0.3		0.3 × V_{CC}	V
I_{IH}	Input high current				30	µA
I_{IL}	Input low current		–30			µA
C_{IN_SE}	Input capacitance	at 25°C		2		pF
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.3	V
f_{SCL}	I^2C clock rate	Standard			100	kHz
		Fast mode			400	
		Ultra Fast mode			1000	
$t_{SU(START)}$	START condition setup time	SCL high before SDA low	0.6			us
t_H(START)	START condition hold time	SCL low after SDA low	0.6			us
$t_{W(SCLH)}$	SCL pulse width high		0.6			us
$t_{W(SCLL)}$	SCL pulse width low		1.3			us
$t_{SU(SDA)}$	SDA setup time		100			ns

V_{DD} = 1.8 V ± 5 %, –40°C ≤ T_A ≤ 105°C. Typical values are at V_{DD} = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{H(SDA)}$	SDA hold time	SDA valid after SCL low	0		0.9	us
$t_{R(IN)}$	SDA/SCL input rise time				300	ns
$t_{F(IN)}$	SDA/SCL input fall time				300	ns
$t_{F(OUT)}$	SDA output fall time	C_{BUS} <= 400 pF			300	ns
t_{SU}(STOP)	STOP condition setup time		0.6			us
t_{BUS}	Bus free time between STOP and START		1.3			us
SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f_{IN}	Input frequency	Clock input	DC		250	MHz
$V_{IN\_S\text{-}E}$	Single-ended Input Voltage Swing	Assumes a square wave input with two levels	0.4		3.465	V
dVIN/dt	Input Slew Rate (20% to 80% of the amplitude)		0.05			V/ns
I_{IH}	Input high current	V_{DD} = 3.465 V, V_{IH} = 3.465 V			50	µA
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{IL} = 0 V	–30			µA
C_{IN_SE}	Input capacitance	at 25°C		3.5		pF
DIFFERENTIAL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f_{IN}	Input frequency	Clock input			2	GHz
$V_{IN,DIFF(p\text{-}p)}$	Differential input voltage peak-to-peak {2*(V_{INP}-V_{INN})}	V_{ICM} = 1 V (V_{DD} = 1.8 V)	0.3		2.4	V_{PP}
		V_{ICM} = 1.25 V (V_{DD} = 2.5 V/3.3 V)	0.3		2.4	
V_{ICM}	Input common mode voltage	$V_{IN,DIFF(P\text{-}P)}$ > 0.4 V (V_{DD} = 1.8 V/2.5/3.3 V)	0.25		2.3	V
I_{IH}	Input high current	V_{DD} = 3.465 V, V_{INP} = 2.4 V, V_{INN} = 1.2 V			30	µA
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{INP} = 0 V, V_{INN} = 1.2 V	–30			µA
$C_{IN\_S\text{-}E}$	Input capacitance (Single-ended)	at 25°C		3.5		pF
LVDS DC OUTPUT CHARACTERISTICS						
|VOD|	Differential output voltage magnitude | V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 0	250	350	450	mV
|VOD|	Differential output voltage magnitude | V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	400	500	650	mV
ΔVOD	Change in differential output voltage magnitude. Per output, defined as the difference between VOD in logic hi/lo states.	$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 0	–15		15	mV
ΔVOD	Change in differential output voltage magnitude	$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	–20		20	mV
$V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 1.8 V)	1		1.2	V
		$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 2.5 V/3.3 V)	1.1		1.375	
$V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 1.8 V), AMP_SEL = 1	0.8		1	V
		$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 2.5 V/3.3 V), AMP_SEL = 1	0.9		1.1	
$\Delta_{VOC(SS)}$	Change in steady-state common mode output voltage. Per output, defined as the difference in VOC in logic hi/lo states.	$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 0	–15		15	mV
$\Delta_{VOC(SS)}$	Change in steady-state common mode output voltage	$V_{IN,DIFF(P\text{-}P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1	–20		20	mV
LVDS AC OUTPUT CHARACTERISTICS						

V_{DD} = 1.8 V ± 5 %, –40°C ≤ T_A ≤ 105°C. Typical values are at V_{DD} = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ring}	Output overshoot and undershoot	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, f_{OUT} = 491.52 MHz	–0.1		0.1	V_{OD}
V_{OS}	Output AC common mode	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω , AMP_SEL = 0		50	100	mV_{pp}
V_{OS}	Output AC common mode	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, AMP_SEL = 1		75	150	mV_{pp}
I_{OS}	Short-circuit output current (differential)	V_{OUTP} = V_{OUTN}	–12		12	mA
$I_{OS(cm)}$	Short-circuit output current (common-mode)	V_{OUTP} = V_{OUTN} = 0	–24		24	mA
t_{PD}	Propagation delay	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (2)	0.3		0.575	ns
$t_{SK, O}$	Output skew	Skew between outputs with the same load conditions (4 and 8 channel) (3)			20	ps
$t_{SK, PP}$	Part-to-part skew	Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading.			250	ps
$t_{SK, P}$	Pulse skew	50% duty cycle input, crossing point-to-crossing-point distortion (4)	–20		20	ps
$t_{RJIT(ADD)}$	Random additive Jitter (rms)	f_{IN} = 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns, Integration range = 12 kHz – 20 MHz, with output load R_{LOAD} = 100 Ω		50	60	fs, RMS
Phase noise	Phase Noise for a carrier frequency of 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns with output load R_{LOAD} = 100 Ω	PN_{1kHz}		–143		dBc/Hz
		PN_{10kHz}		–152		
		PN_{100kHz}		–157		
		PN_{1MHz}		–160		
		PN_{floor}		–164		
MUX_{ISO}	Mux Isolation	f_{IN} = 156.25 MHz. The difference in power level at f_{IN} when the selected clock is active and the unselected clock is static versus when the selected clock is inactive and the unselected clock is active.		80		dB
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t_R/t_F	Output rise and fall time	20% to 80% with R_{LOAD} = 100 Ω			300	ps
t_R/t_F	Output rise and fall time	20% to 80% with RLOAD = 100 Ω (AMP_SEL= 1)			300	ps
$t_{en/disable}$	Output Enable and Disable Time	Time taken for outputs to go from disable state to enable state and vice versa. (5) (6)			1	us
I_{leakZ}	Output leakage current in High Z	Outputs are held in high Z mode with OUTP = OUTN (max applied external voltage is the lesser of VDD or 1.89V and minimum applied external voltage is 0V			50	uA
V_{AC_REF}	Reference output voltage	VDD = 2.5 V, I_{LOAD} = 100 µA	0.9	1.25	1.375	V
POWER SUPPLY NOISE REJECTION (PSNR) V_{DD} = 2.5 V/ 3.3 V						

V_{DD} = 1.8 V ± 5 %, –40°C ≤ T_A ≤ 105°C. Typical values are at V_{DD} = 1.8 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSNR	Power Supply Noise Rejection ($f_{carrier}$ = 156.25 MHz)	10 kHz, 100 mVpp ripple injected on V_{DD}		–70		dBc
		1 MHz, 100 mVpp ripple injected on V_{DD}		–50		

(1) Measured between single-ended/differential input crossing point to the differential output crossing point.
(2) For the dual bank devices, the inputs are phase aligned and have 50% duty cycle.
(3) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.
(4) Applies to the dual bank family.
(5) Time starts after the acknowledge bit

7.6 Typical Characteristics

図 7-1 captures the variation of the LMK1D1208I current consumption with input frequency and supply voltage. 図 7-2 shows the variation of the differential output voltage (VOD) swept across frequency.

It is important to note that 図 7-1 and 図 7-2 serve as a guidance to the users on what to expect for the range of operating frequency supported by LMK1D1208I. These graphs were plotted for a limited number of frequencies and load conditions which may not represent the customer system.

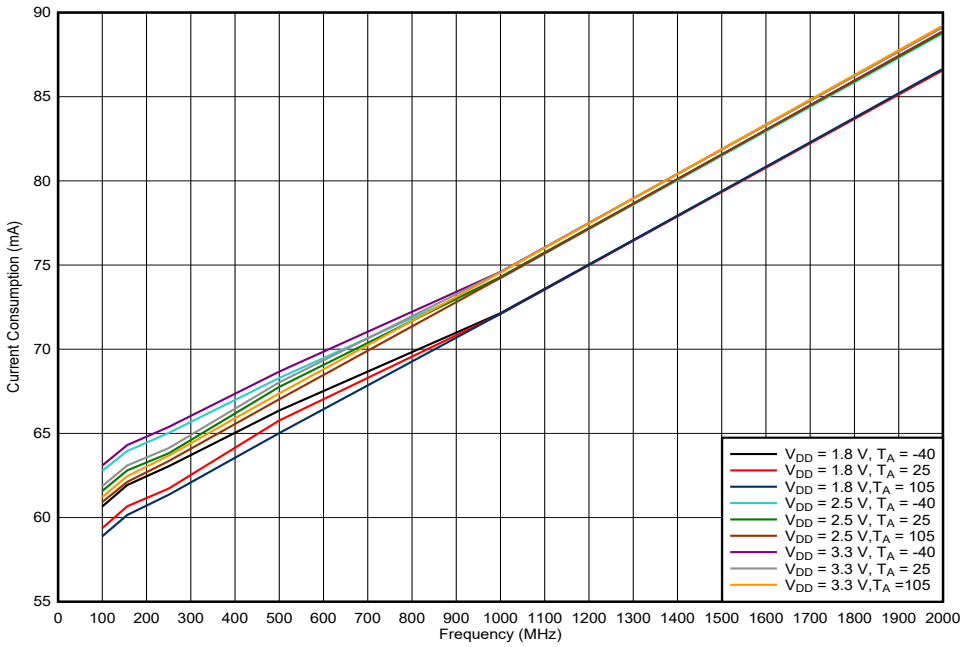


図 7-1. LMK1D1208I Current Consumption vs. Frequency

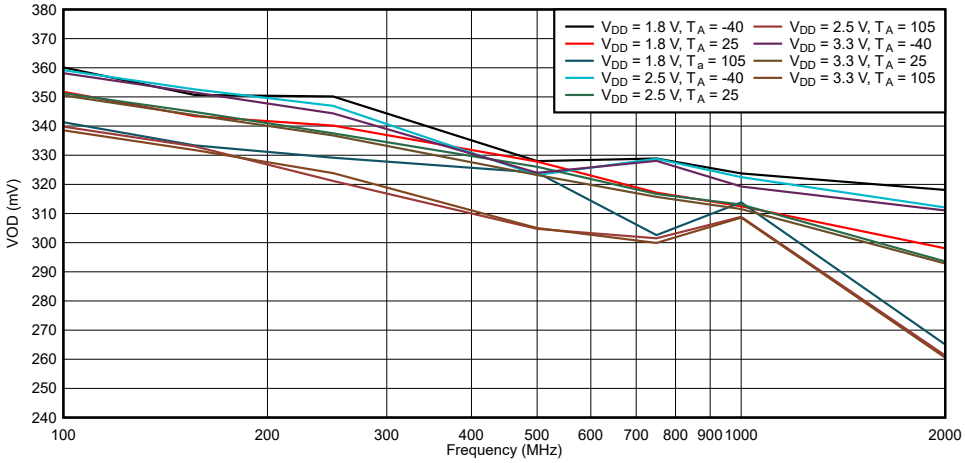


図 7-2. LMK1D1208I VOD vs. Frequency

8 Parameter Measurement Information

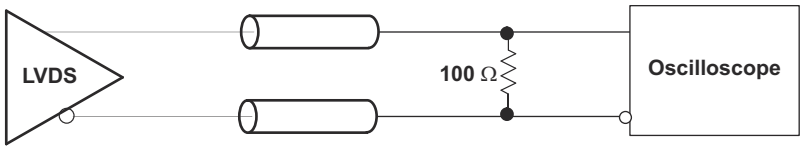


図 8-1. LVDS Output DC Configuration During Device Test

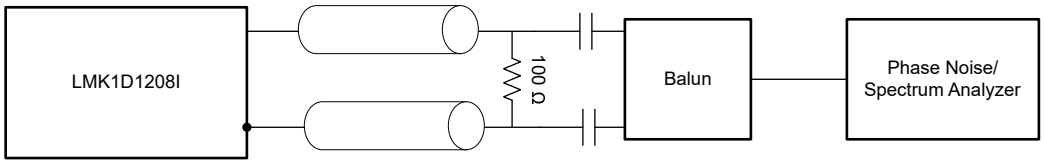


図 8-2. LVDS Output AC Configuration During Device Test

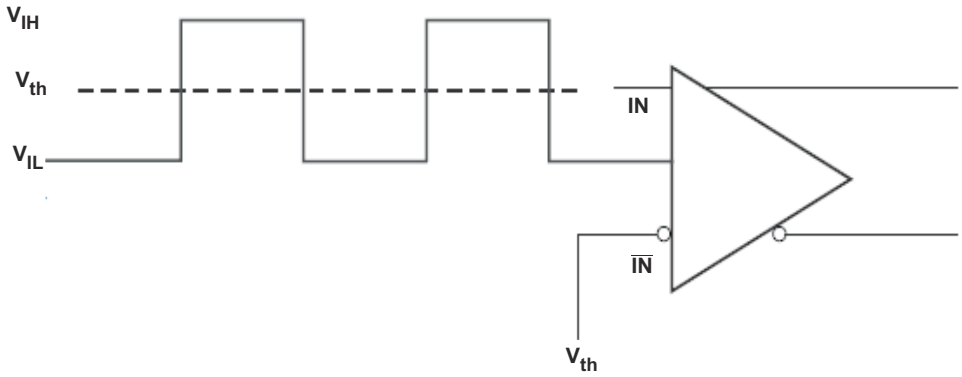


図 8-3. DC-Coupled LVCMOS Input During Device Test

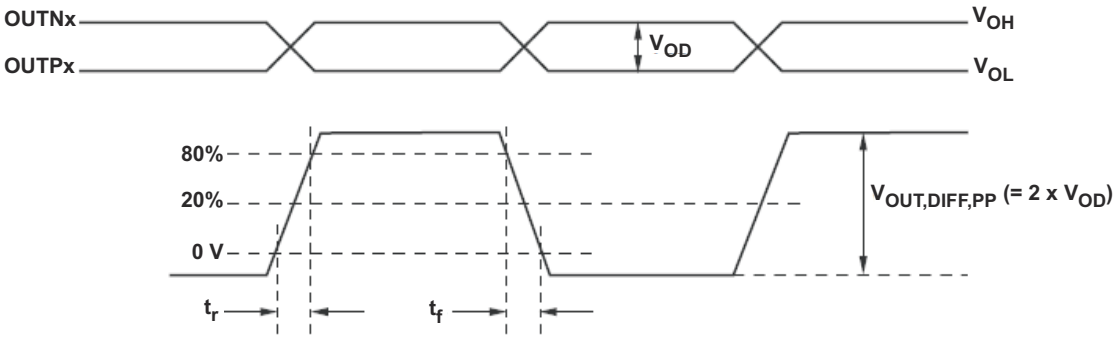
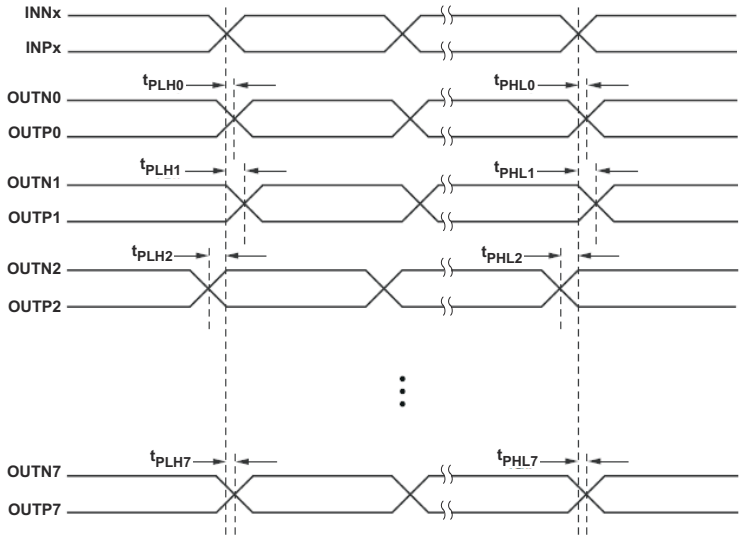


図 8-4. Output Voltage and Rise/Fall Time



A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, ..7)

B. Part-to-part skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, ..7)

図 8-5. Output Skew and Part-to-Part Skew

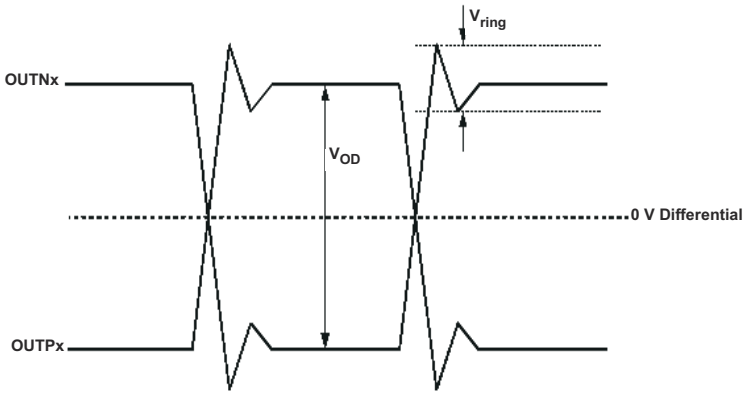


図 8-6. Output Overshoot and Undershoot

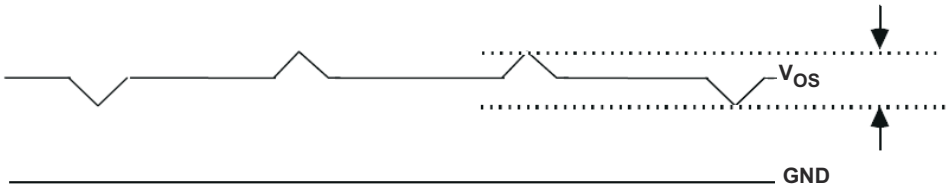


図 8-7. Output AC Common Mode

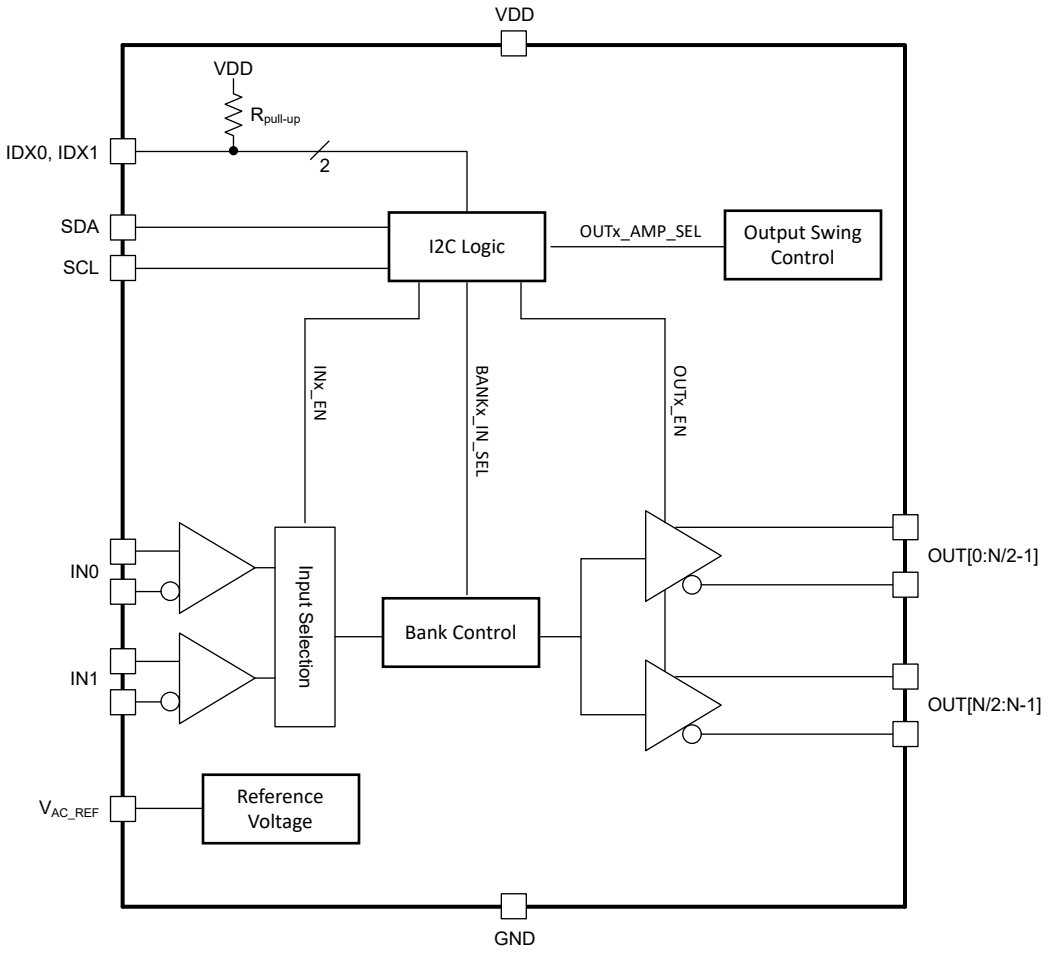
9 Detailed Description

9.1 Overview

The LMK1D1208I is a low-additive jitter, I²C-programmable, LVDS output clock buffer that uses CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity. The LMK1D1208I also includes status and control registers for configuring the different modes in the device.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D1208I, AC coupling must be used.If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

9.2 Functional Block Diagram



9.3 Feature Description

The LMK1D1208I is an I²C-programmable, low-additive jitter, LVDS fan-out buffer that can generate up to eight copies of two selectable LVPECL, LVDS, HCSL, CML, or LVCMOS inputs. This feature-rich device allows the user to have flexibility on the configuration based on their application use-case.

9.3.1 Fail-Safe Input

The LMK1D120x family of devices is designed to support fail-safe input operation. This feature allows the user to drive the device inputs before VDD is applied without damaging the device. Refer to *Specifications* for more information on the maximum input supported by the device. The device also incorporates an input hysteresis, which prevents random oscillation in absence of an input signal, allowing the input pins to be left open.

9.3.2 Input Stage Configurability

The LMK1D1208I has an input stage that accepts up to two clock inputs and can be configured as either a 2:1 mux or as a dual bank. When configured as a 2:1 mux, the LMK1D1208I device can select one of the two clock inputs and then distribute it to the eight LVDS output pairs. In the dual bank mode, the LMK1D1208I can assign each clock input to fan out four LVDS output pairs per bank. Refer to the *Device Functional Modes* for how to configure the two input stages.

Unused inputs can be left floating to reduce overall component cost. Both AC and DC coupling schemes can be used with the LMK1D1208I to provide greater system flexibility.

9.3.3 Dual Output Bank

LMK1D1208I has eight LVDS output pairs which are grouped into two banks, each with four LVDS output pairs. The 表 9-1 outlines this mapping.

表 9-1. Output Bank Map

BANK	CLOCK OUTPUTS
0	OUT0, OUT1, OUT2, OUT3
1	OUT4, OUT5, OUT6, OUT7

9.3.4 I²C

The I²C control is used to configure the different features in the LMK1D1208I. These features include individual input and output channel enable or disable, input mux select in each bank, bank muting (setting bank outputs to logic low), and individual output amplitude control. The I²C logic is also capable of fast mode where the frequency is 400 kHz.

9.3.4.1 I²C Address Assignment

The I²C address is assigned by the two pins, IDX0 and IDX1. Each IDX pin supports two levels allowing the LMK1D1208I to assume four different I²C addresses. See 表 9-2 for address pin assignment.

表 9-2. I²C Address Assignment

I²C ADDRESS	IDX1	IDX0
0x68	L	L
0x69	L	H
0x6A	H	L
0x6B	H	H

9.3.5 LVDS Output Termination

TI recommends that unused outputs are terminated differentially with a 100-Ω resistor for optimum performance. Unterminated outputs are also okay, but this will result in a slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

図 9-1 and 図 9-2 show how the LMK1D1208I can be connected to LVDS receiver inputs with DC and AC coupling, respectively.

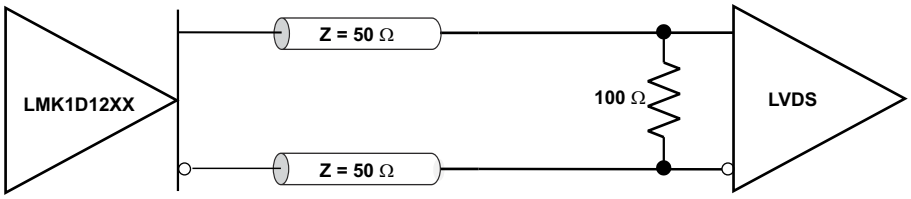


図 9-1. Output DC Termination

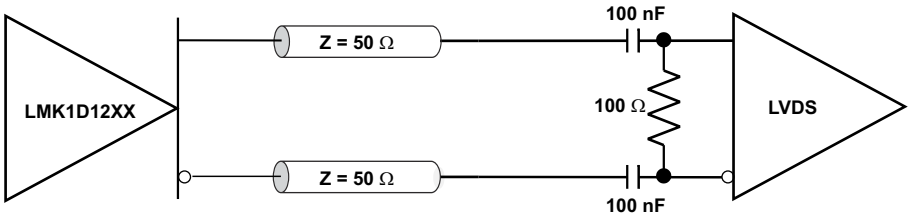


図 9-2. Output AC Termination (With the Receiver Internally Biased)

9.3.6 Input Termination

The LMK1D1208I inputs can be interfaced with LVDS, LVPECL, HCSL or LVCMOS drivers.

図 9-3 and 図 9-4 show how LVDS drivers can be connected to LMK1D1208I inputs with DC coupling and AC coupling, respectively.

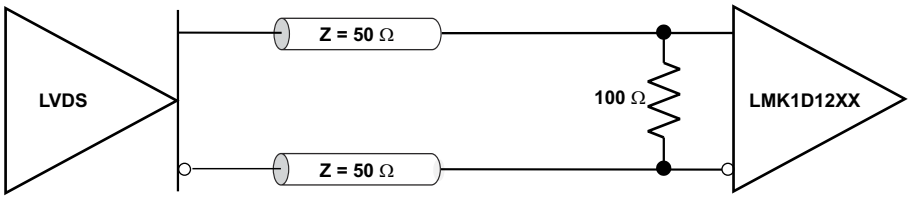


図 9-3. LVDS Clock Driver Connected to LMK1D1208I Input (DC-Coupled)

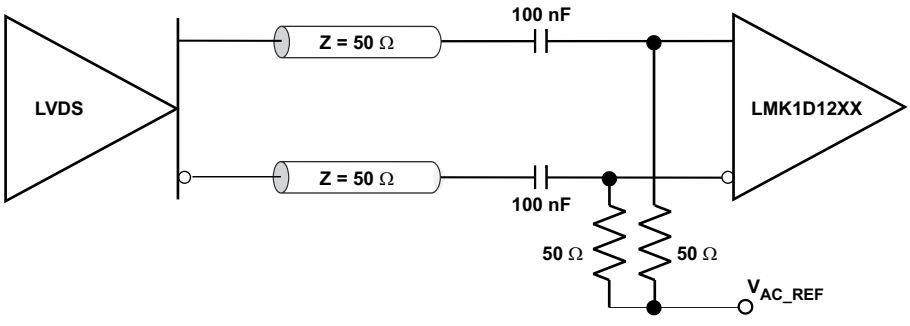


図 9-4. LVDS Clock Driver Connected to LMK1D1208I Input (AC-Coupled)

図 9-5 shows how to connect LVPECL inputs to the LMK1D1208I. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 V_{PP}.

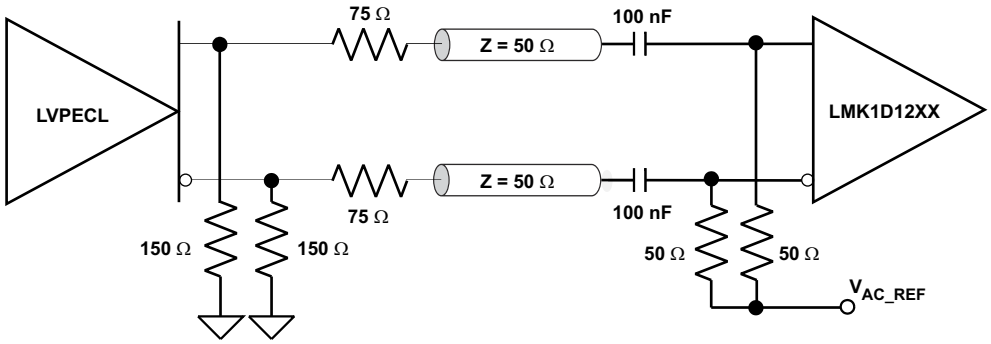


図 9-5. LVPECL Clock Driver Connected to LMK1D1208I Input

図 9-6 shows how to couple a LVCMOS clock input to the LMK1D1208I directly.

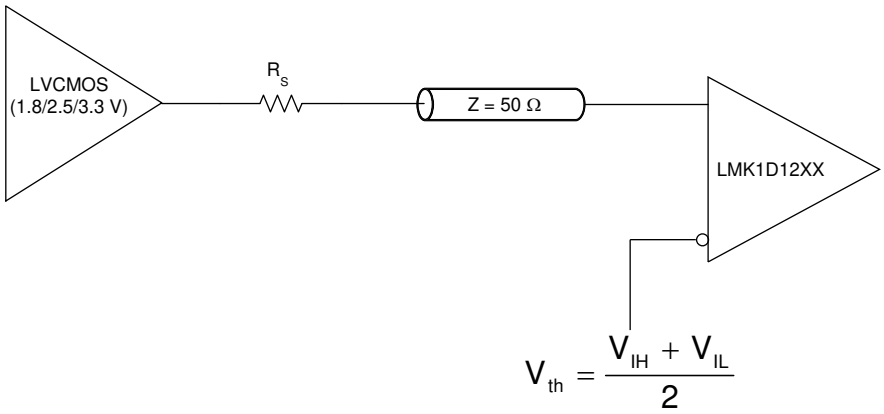


図 9-6. 1.8-V, 2.5-V, or 3.3-V LVCMOS Clock Driver Connected to LMK1D1208I Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

9.4 Device Functional Modes

The outputs of Bank 0 and Bank 1 can be one of three options: logic low, buffered IN0, or buffered IN1. These output types should only be attained by maintaining the register setting combination outlined in 表 9-3. The LMK1D1208I registers must be programmed within these possible logic states to ensure proper device functionality. Using the device outside the intended logic can result in degraded performance.

表 9-3. Register Control Logic Table

BANKx OUTPUTS	BANKx_IN_SEL	BANKx_MUTE	IN0_EN	IN1_EN
Logic low	X	1	X	X
IN0	1	0	1	X
IN1	0	0	X	1

9.4.1 Input Enable Control

The LMK1D1208I allows for individual input channel enable or disable through the INx_EN register field. The inputs should be disabled when not in use to reduce the power consumption.

表 9-4 describes the control of this function. INx_EN is set by register 0x02 (R2). See *R2 Register* for more information on this register.

表 9-4. Input Control

INx_EN	ACTIVE CLOCK INPUT
0	INx_P, INx_N disabled
1	INx_P, INx_N enabled

9.4.2 Bank Input Selection

Bank 0 and Bank 1 can choose between the two inputs to fanout four LVDS output pairs each. In the 2:1 input mux mode, each bank must select the same clock input to output eight identical clocks. With the dual bank mode, each bank can select a different clock input to distribute both inputs separately; this is analogous to having two 1:4 buffers. When operating in dual bank mode, TI recommends that Bank 0 not select IN1 and Bank 1 not select IN0 to avoid crosstalk and degraded performance.

The BANKx_IN_SEL register field configures this function described in 表 9-5. BANKx_IN_SEL is set by register 0x02 (R2). See *R2 Register* for more information on this register.

表 9-5. Bank Input Selection

BANKx_IN_SEL	BANK CLOCK INPUT
0	BANKx selects IN1_P, IN1_N
1	BANKx selects IN0_P, IN0_N

9.4.3 Bank Mute Control

Each bank, Bank 0 or Bank 1, can be individually muted such that the bank outputs are set to logic low (OUTx_P is low and OUTx_N is high).

表 9-6 describes the control of this function. The BANKx_MUTE register field is set by register 0x02 (R2). See *R2 Register* for more information on this register.

表 9-6. Bank Mute Control

BANKx_MUTE	BANK CLOCK OUTPUTS
0	BANKx outputs selected INx
1	BANKx outputs logic low

9.4.4 Output Enable Control

The outputs of the LMK1D1208I can be individually enabled or disabled through the OUTx_EN register field. The disabled state of the outputs is high impedance as this reduces the power consumption and also prevents back-biasing of the devices connected to these outputs. Unused outputs should be disabled to eliminate the need for a termination resistor. In the case of enabled unused outputs, TI recommends a 100-Ω termination for optimal performance.

表 9-7 describes the control of this function. OUTx_EN is set by register 0x00 (R0). See *R0 Register* for more information on this register.

表 9-7. Output Control

OUTx_EN	CLOCK OUTPUTS
0	OUTx_P, OUTx_N disabled in Hi-Z state
1	OUTx_P, OUTx_N enabled

9.4.5 Output Amplitude Selection

The amplitude of the LMK1D1208I outputs can be individually programmed through the OUTx_AMP_SEL register field. The boosted LVDS swing mode can be used in applications which require a higher output swing for better noise performance (higher slew rate) or for swing requirements in the receiver that the standard LVDS swing cannot meet.

表 9-8 describes the control of this function. OUTx_AMP_SEL is set by register 0x01 (R1). See *R1 Register* for more information on this register.

表 9-8. Output Amplitude Selection Table

OUTx_AMP_SEL	OUTPUT AMPLITUDE (VOD)
0	Standard LVDS swing (350 mV)
1	Boosted LVDS swing (500 mV)

9.5 Programming

The LMK1D1208I uses I²C to program the states of its eight output drivers. See *I²C* for more information on the I²C features and address assignment, and *Register Maps* for the list of programmable registers.

表 9-9. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Register address for *Byte* operations, or starting register address for *Block*, operations

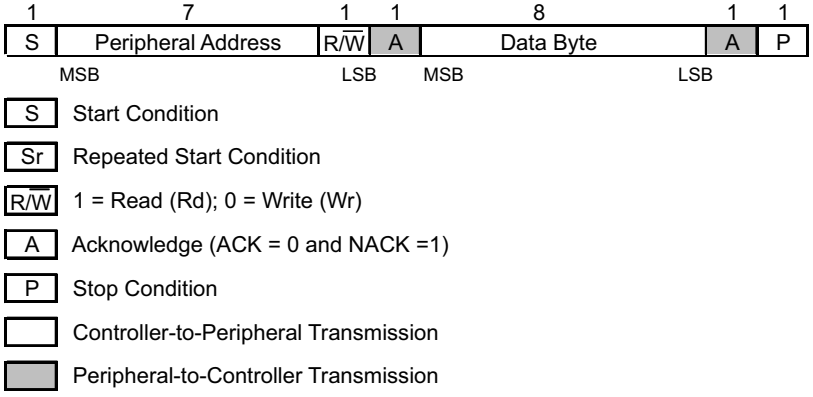


図 9-7. Generic Programming Sequence

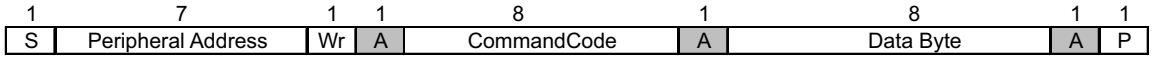


図 9-8. Byte Write Protocol

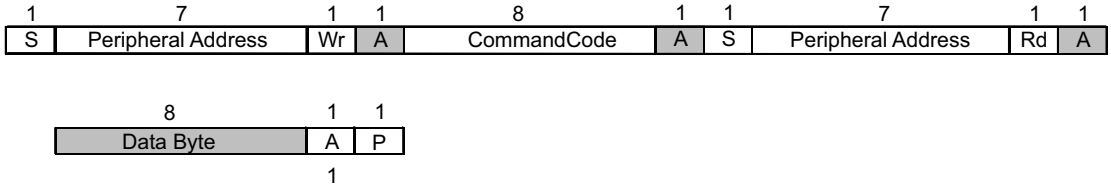


図 9-9. Byte Read Protocol

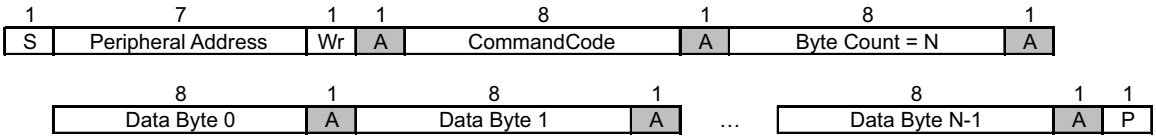


図 9-10. Block Write Protocol

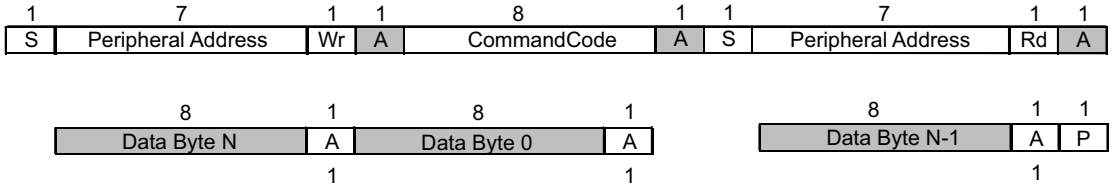


図 9-11. Block Read Protocol

9.6 Register Maps

9.6.1 LMK1D1208I Registers

表 9-10 lists the LMK1D1208I registers. All register locations not listed should be considered as reserved locations and the register contents should not be modified.

TI highly suggests that the user only operates within the logic states listed in 表 9-3 for optimum performance.

表 9-10. LMK1D1208I Registers

Address	Acronym	Register Fields	Section
0h	R0	Output Enable Control	Go
1h	R1	Output Amplitude Control	Go
2h	R2	Input Enable and Bank Setting Control	Go
5h	R5	Device/Revision Identification	Go
Eh	R14	I^2C Address Readback	Go

Complex bit access types are encoded to fit into small table cells. 表 9-11 shows the codes that are used for access types in this section.

表 9-11. LMK1D1208I Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Reset/default value in hexadecimal

9.6.1.1 R0 Register (Address = 0h) [reset = 0h]

R0 is shown in 表 9-12.

The R0 register contains bits that enable or disable individual output clock channels [7:0].

Return to the Summary Table.

表 9-12. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT7_EN	R/W	0h	This bit controls the output enable signal for output channel OUT7_P/OUT7_N. 0h = Output Disabled (Hi-Z) 1h = Output Enabled
6	OUT6_EN	R/W	0h	This bit controls the output enable signal for output channel OUT6_P/OUT6_N. 0h = Output Disabled (Hi-Z) 1h = Output Enabled
5	OUT5_EN	R/W	0h	This bit controls the output enable signal for output channel OUT5_P/OUT5_N. 0h = Output Disabled (Hi-Z) 1h = Output Enabled

表 9-12. R0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	OUT4_EN	R/W	0h	This bit controls the output enable signal for output channel OUT4_P/OUT4_N. 0h = Output Disabled (Hi-Z) 1h = Output Enabled
3	OUT3_EN	R/W	0h	This bit controls the output enable signal for output channel OUT3_P/OUT3_N. 0h = Output Disabled (Hi-Z) 1h = Output Enabled
2	OUT2_EN	R/W	0h	This bit controls the output enable signal for output channel OUT2_P/OUT2_N. 0h = Output Disabled (Hi-Z) 1h = Output Enabled
1	OUT1_EN	R/W	0h	This bit controls the output enable signal for output channel OUT1_P/OUT1_N. 0h = Output Disabled (Hi-Z) 1h = Output Enabled
0	OUT0_EN	R/W	0h	This bit controls the output enable signal for output channel OUT0_P/OUT0_N. 0h = Output Disabled (Hi-Z) 1h = Output Enabled

9.6.1.2 R1 Register (Address = 1h) [reset = 0h]

R1 is shown in 表 9-13.

The R1 register contains bits that set the output amplitude to a standard or boosted LVDS swing.

Return to the Summary Table.

表 9-13. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT7_AMP_SEL	R/W	0h	This bit sets the output amplitude for output channel OUT7_P/OUT7_N. 0h = Standard LVDS Swing (350 mV) 1h = Boosted LVDS Swing (500 mV)
6	OUT6_AMP_SEL	R/W	0h	This bit sets the output amplitude for output channel OUT6_P/OUT6_N. 0h = Standard LVDS Swing (350 mV) 1h = Boosted LVDS Swing (500 mV)
5	OUT5_AMP_SEL	R/W	0h	This bit sets the output amplitude for output channel OUT5_P/OUT5_N. 0h = Standard LVDS Swing (350 mV) 1h = Boosted LVDS Swing (500 mV)
4	OUT4_AMP_SEL	R/W	0h	This bit sets the output amplitude for output channel OUT4_P/OUT4_N. 0h = Standard LVDS Swing (350 mV) 1h = Boosted LVDS Swing (500 mV)
3	OUT3_AMP_SEL	R/W	0h	This bit sets the output amplitude for output channel OUT3_P/OUT3_N. 0h = Standard LVDS Swing (350 mV) 1h = Boosted LVDS Swing (500 mV)

表 9-13. R1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OUT2_AMP_SEL	R/W	0h	This bit sets the output amplitude for output channel OUT2_P/OUT2_N. 0h = Standard LVDS swing (350 mV) 1h = Boosted LVDS swing (500 mV)
1	OUT1_AMP_SEL	R/W	0h	This bit sets the output amplitude for output channel OUT1_P/OUT1_N. 0h = Standard LVDS Swing (350 mV) 1h = Boosted LVDS Swing (500 mV)
0	OUT0_AMP_SEL	R/W	0h	This bit sets the output amplitude for output channel OUT0_P/OUT0_N. 0h = Standard LVDS Swing (350 mV) 1h = Boosted LVDS Swing (500 mV)

9.6.1.3 R2 Register (Address = 2h) [reset = F1h]

R2 is shown in 表 9-14.

The R2 register contains bits that enable/disable the input channels and control the banks.

Return to the Summary Table.

表 9-14. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	1h	Register bit can be written to 1. Writing a different value than 1 will affect device functionality.
6	Reserved	R/W	1h	Register bit can be written to 1. Writing a different value than 1 will affect device functionality.
5	BANK1_IN_SEL	R/W	1h	This bit sets the input channel for Bank 1. 0h = IN1_P/IN1_N 1h = IN0_P/IN0_N
4	BANK0_IN_SEL	R/W	1h	This bit sets the input channel for Bank 0. 0h = IN1_P/IN1_N 1h = IN0_P/IN0_N
3	BANK1_MUTE	R/W	0h	This bit sets the outputs in Bank 1 to logic low level. 0h = INx_P/INx_N 1h = Logic low
2	BANK0_MUTE	R/W	0h	This bit sets the outputs in Bank 0 to logic low level. 0h = INx_P/INx_N 1h = Logic low
1	IN1_EN	R/W	0h	This bit controls the input enable signal for input channel IN1_P/IN1_N. 0h = Input Disabled (reduces power consumption) 1h = Input Enabled
0	IN0_EN	R/W	1h	This bit controls the input enable signal for input channel IN0_P/IN0_N. 0h = Input Disabled (reduces power consumption) 1h = Input Enabled

9.6.1.4 R5 Register (Address = 5h) [reset = 20h]

R5 is shown in 表 9-15.

The R5 register contains the silicon revision code and the device identification code.

Return to the Summary Table.

表 9-15. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	REV_ID	R	2h	These bits provide the silicon revision code.
3:0	DEV_ID	R	0h	These bits provide the device identification code.

9.6.1.5 R14 Register (Address = Eh) [reset = 0h]

R14 is shown in 表 9-16.

The R14 register contains the bits that report the current state of the I^2C address based on the IDX0 and IDX1 input pins.

Return to the Summary Table.

表 9-16. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IDX_RB	R	0h	These bits report the I^2C address state.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMK1D1208I is a low-additive jitter universal to LVDS fan-out buffer with two selectable inputs. The small package, low output skew, and low additive jitter make for a flexible device in demanding applications.

10.2 Typical Application

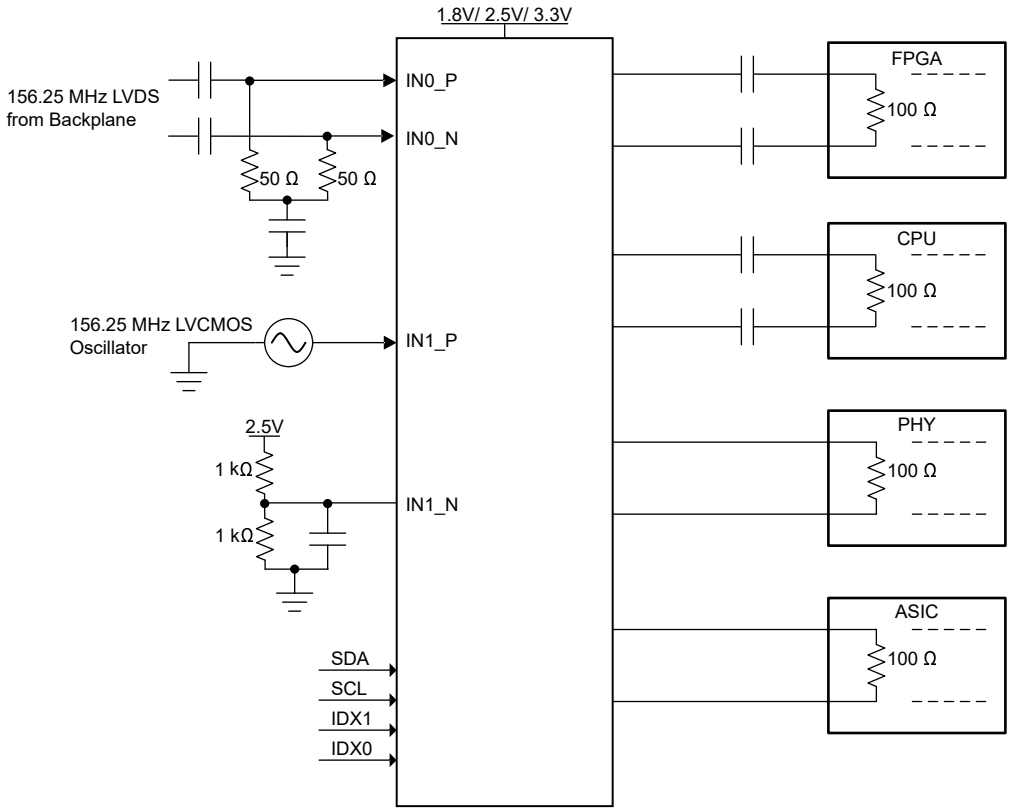


図 10-1. Fan-Out Buffer for Line Card Application

10.2.1 Design Requirements

The LMK1D1208I shown in 図 10-1 is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane at IN0, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator at IN1. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1-µF capacitors are used to reduce noise on both V_{AC_REF} and IN1_N. Either input signal can be then fanned out to desired devices via register control. The configuration example is driving four LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC coupling with an LVDS driver such as the LMK1D1208I. This PHY device features internal termination so no additional components are required for proper operation
- The ASIC LVDS receiver features internal termination and operates at the same common-mode voltage as the LMK1D1208I. Again, no additional components are required.
- The FPGA requires external AC coupling, but has internal termination. 0.1-µF capacitors are placed to provide AC coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.
- The unused outputs of the LMK1D1208I can be disabled by clearing the corresponding OUTx_EN register through I^2C. This results in a lower power consumption.

10.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

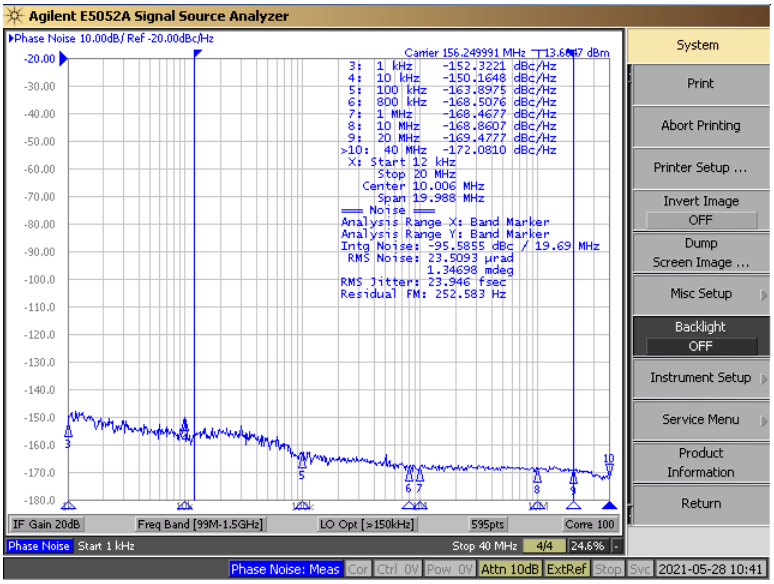
Unused outputs should be terminated differentially with a 100-Ω resistor or disabled through OUTx_EN register control (see 表 9-7) for optimum performance. Outputs may be left unterminated, but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

In this example, the PHY, ASIC, and FPGA or CPU require different schemes. Power-supply filtering and bypassing is critical for low-noise applications.

See *Power Supply Recommendations* for recommended filtering techniques. A reference layout is provided in *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* (SCAU043).

10.2.3 Application Curves

The following graphs show the low additive noise of the LMK1D1208I. The low noise 156.25-MHz source with 24-fs RMS jitter shown in 図 10-2 drives the LMK1D1208I, resulting in 46.4-fs RMS when integrated from 12 kHz to 20 MHz (図 10-3). The resultant additive jitter is a low 39.7-fs RMS for this configuration.



Reference signal is low-noise Rohde and Schwarz SMA100B

図 10-2. LMK1D1208I Reference Phase Noise, 156.25 MHz, 24-fs RMS (12 kHz to 20 MHz)

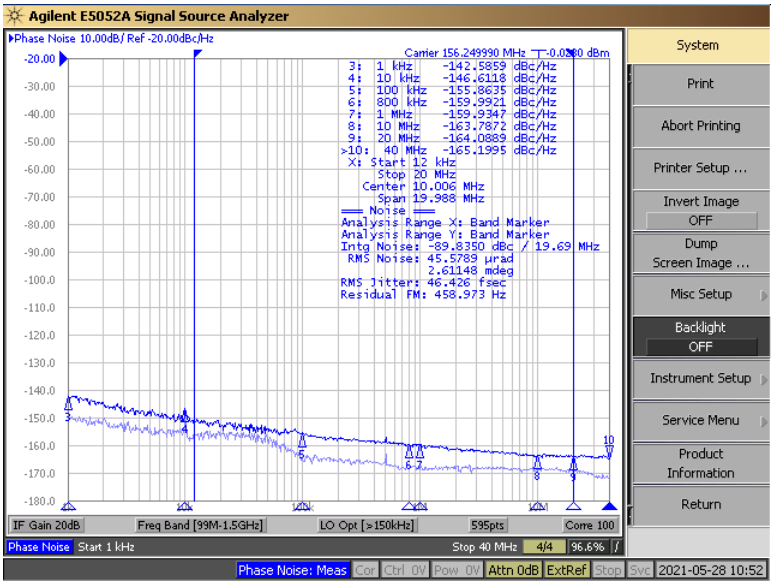


図 10-3. LMK1D1208I Output Phase Noise, 156.25 MHz, 46.4-fs RMS (12 kHz to 20 MHz)

図 10-4 shows the low close-in phase noise of the LMK1D1208I device. The LMK1D1208I has excellent flicker noise as a result of superior process technology and design. This enables their use for clock distribution in radar systems, medical imaging systems etc which require ultra-low close-in phase noise clocks.

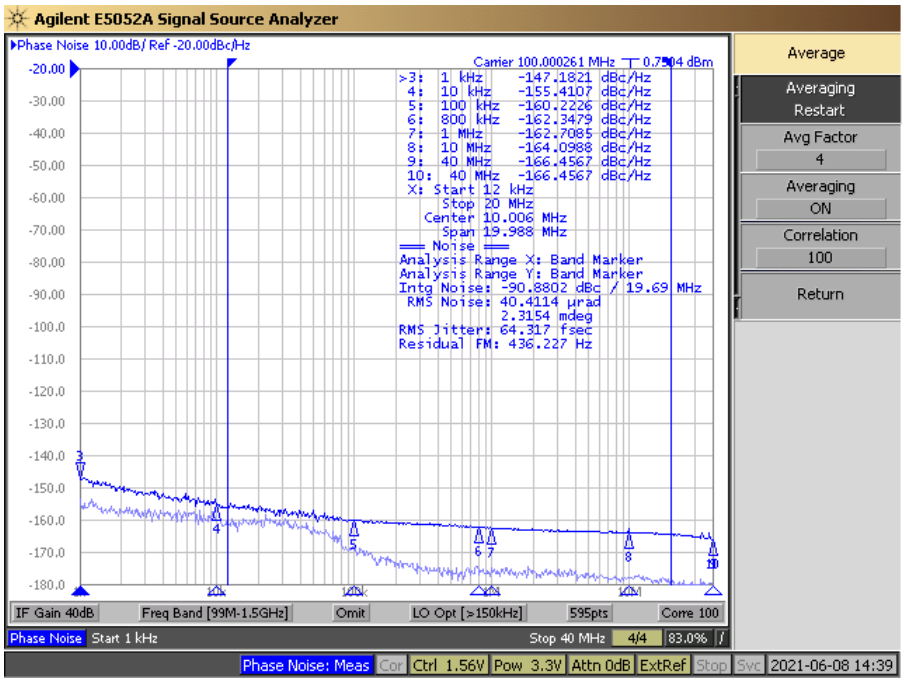


図 10-4. LMK1D1208I Output Phase Noise, 100 MHz, 1-kHz Offset: –147 dBc/Hz

10.3 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver. These beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC resistance, because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

図 10-5 shows this recommended power-supply decoupling method.

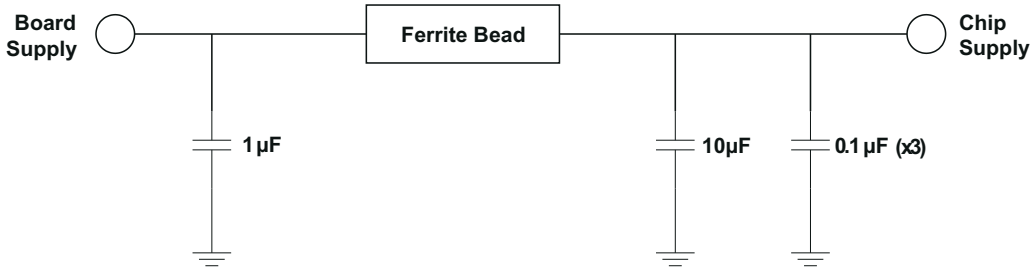


図 10-5. Power Supply Decoupling

10.4 Layout

10.4.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. 図 10-6 and 図 10-7 show the LMK1D1208I top and bottom PCB layer examples.

10.4.2 Layout Example

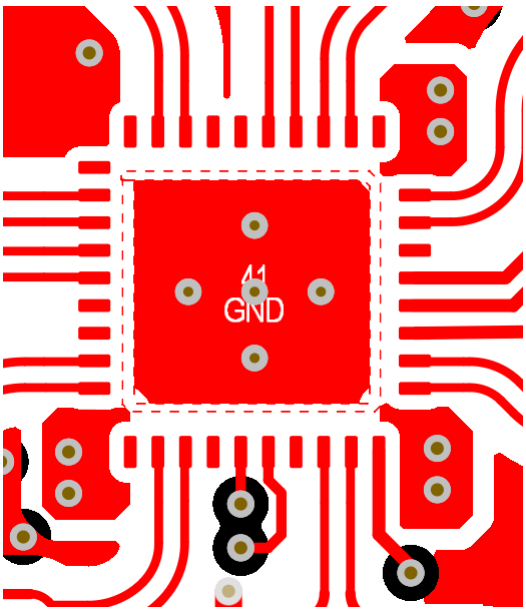


図 10-6. Recommended PCB Layout, Top Layer

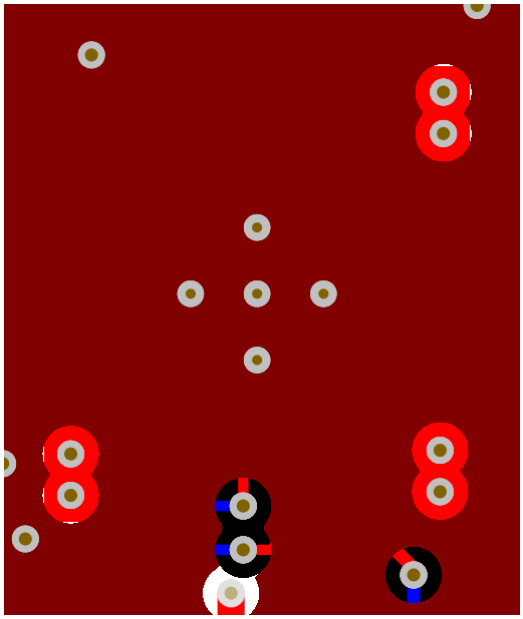


図 10-7. Recommended PCB Layout Bottom Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Power Consumption of LVPECL and LVDS* Analog Design Journal
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Using Thermal Calculation Tools for Analog Components* application note

11.2 ドキュメントの更新通知を受け取る方法

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
LMK1D1208IRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS& no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LMK1D1208I
LMK1D1208IRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS& no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LMK1D1208I

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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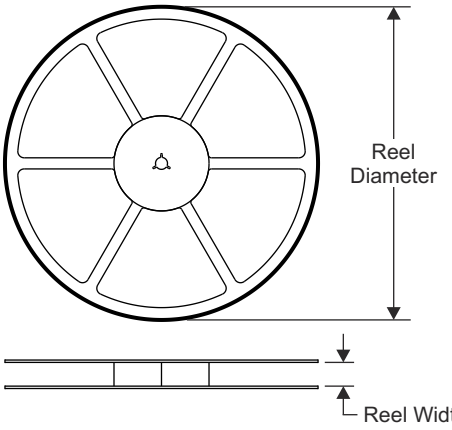
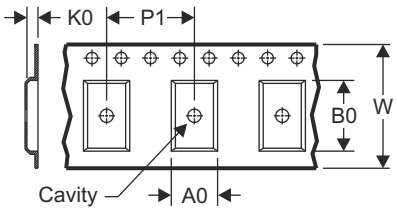
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

12.2 Tape and Reel Information

REEL DIMENSIONS

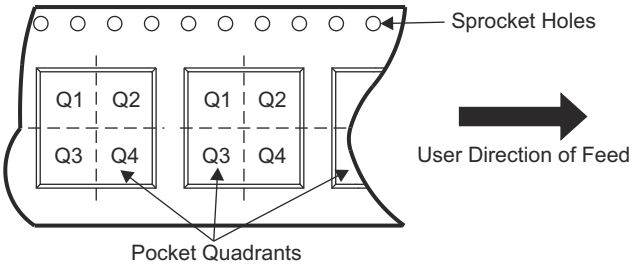


TAPE DIMENSIONS



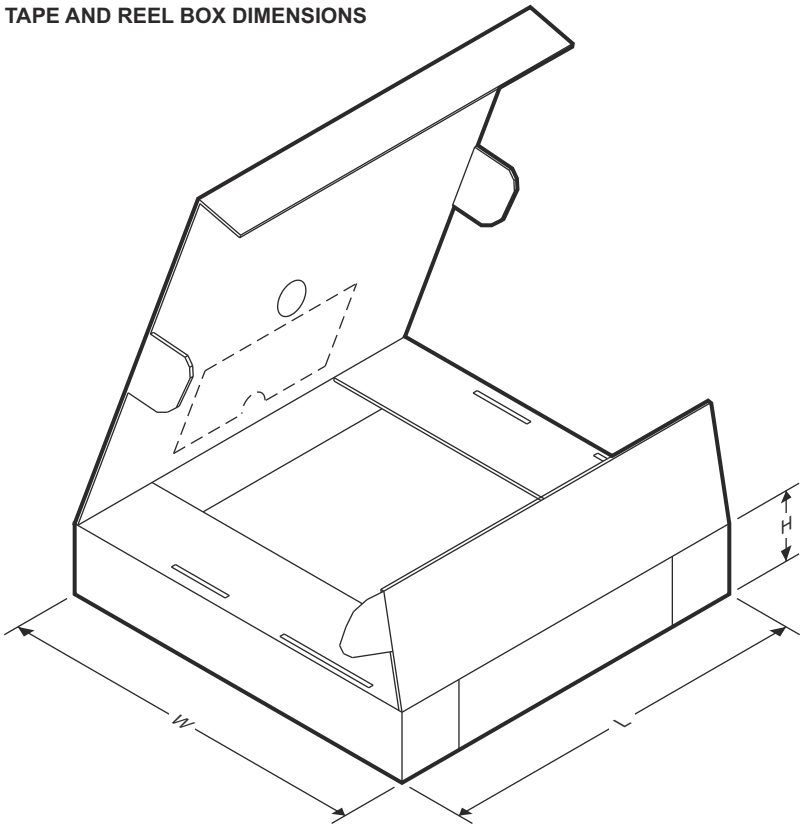
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1D1208IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	13.3	Q2
LMK1D1208IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	13.3	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1D1208IRHAR	VQFN	RHA	40	2500	367.0	367.0	35.0
LMK1D1208IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK1D1208IRHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208I	Samples
LMK1D1208IRHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LMK1D 1208I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

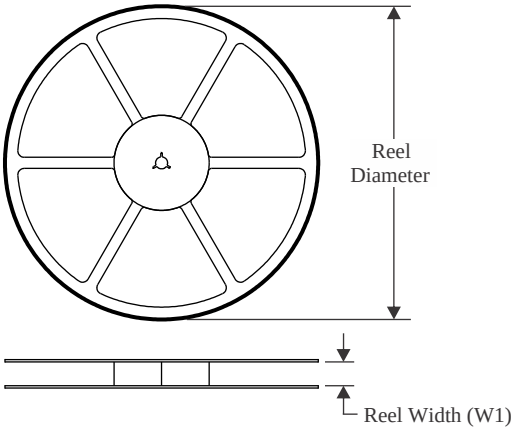
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

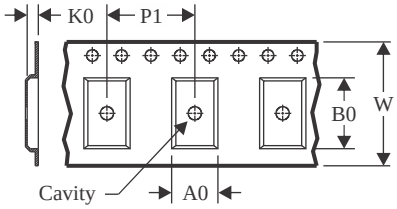
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

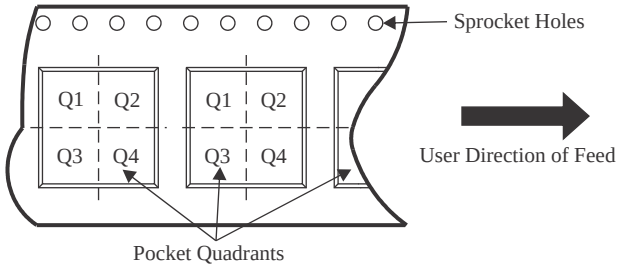


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

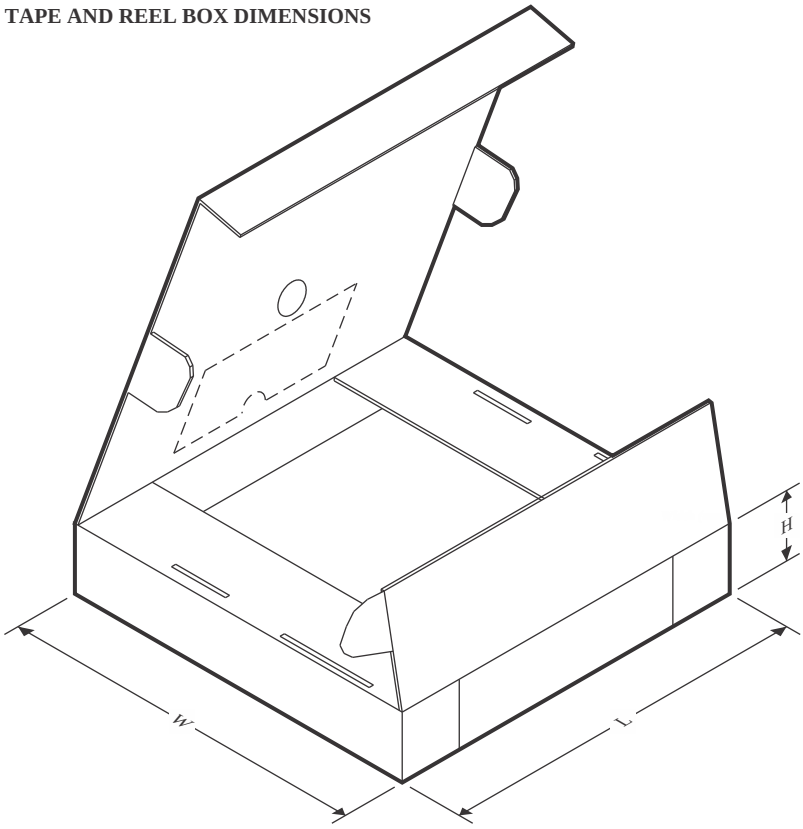
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1D1208IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
LMK1D1208IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1D1208IRHAR	VQFN	RHA	40	2500	367.0	367.0	35.0
LMK1D1208IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

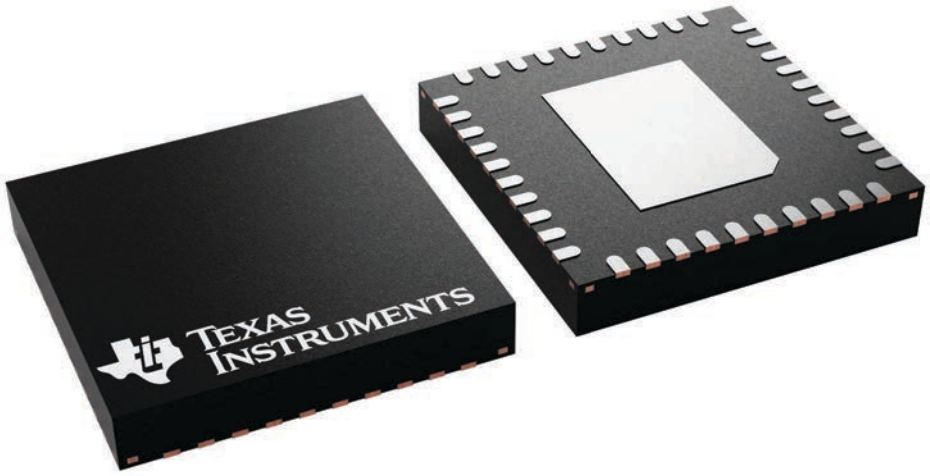
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



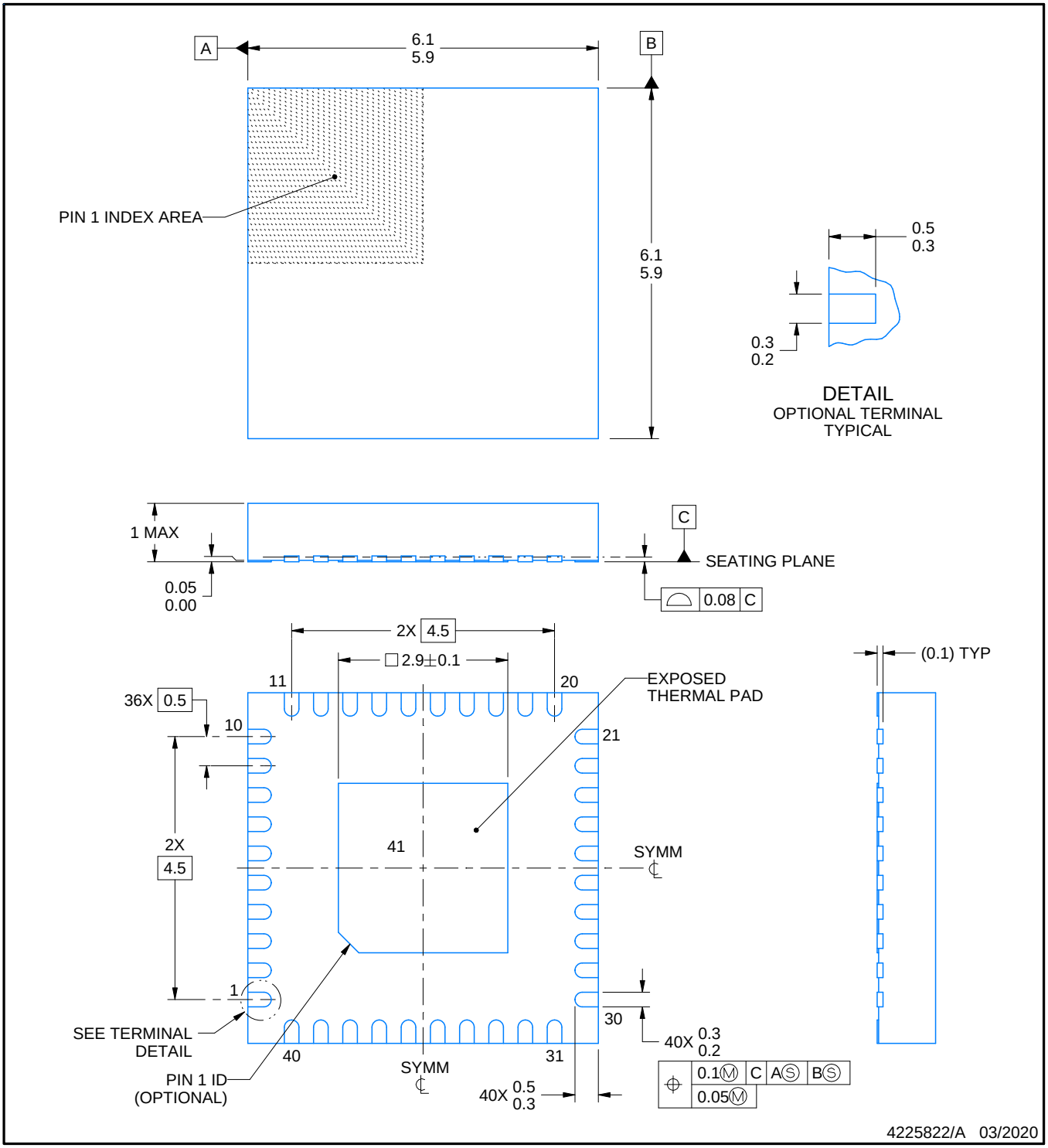
4225870/A

PACKAGE OUTLINE

RHA0040D

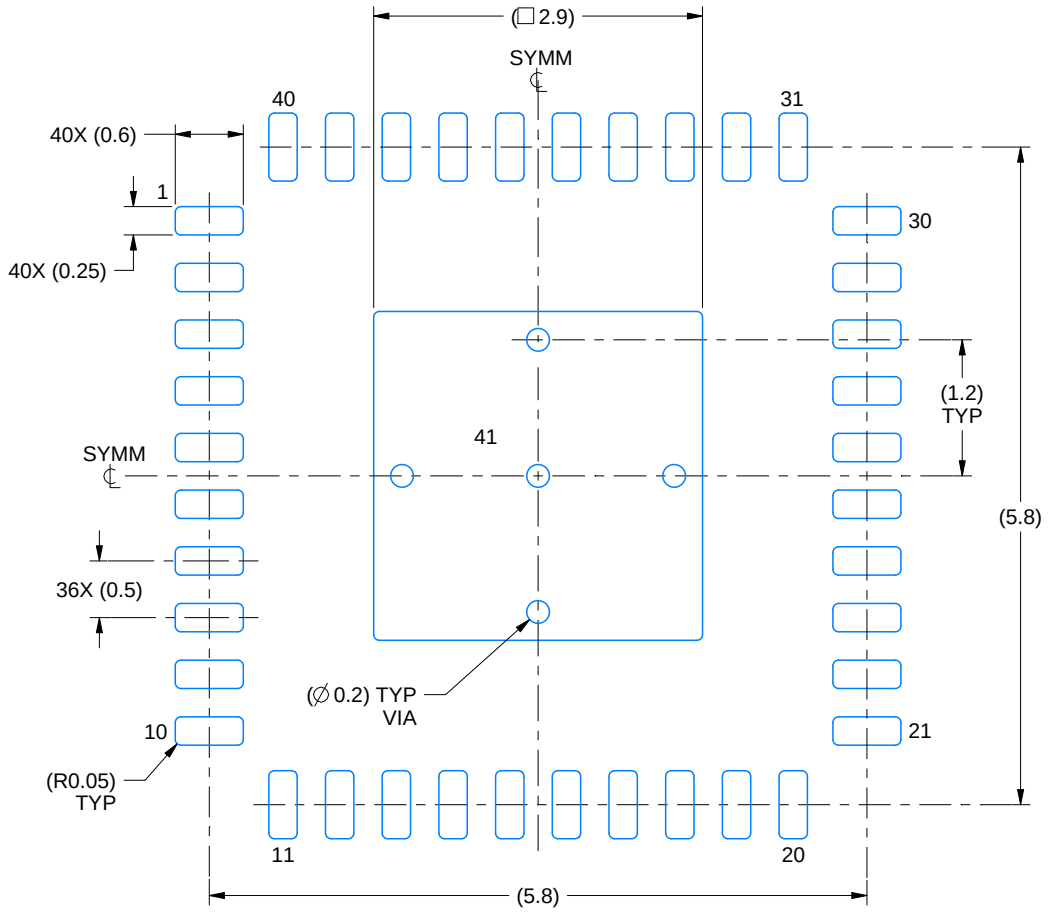
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

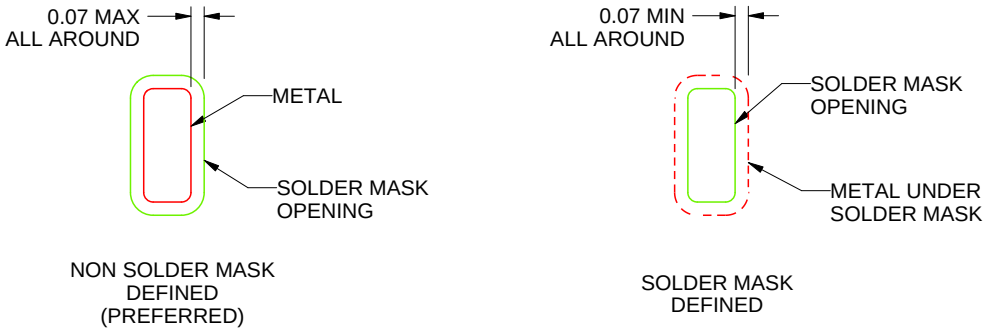


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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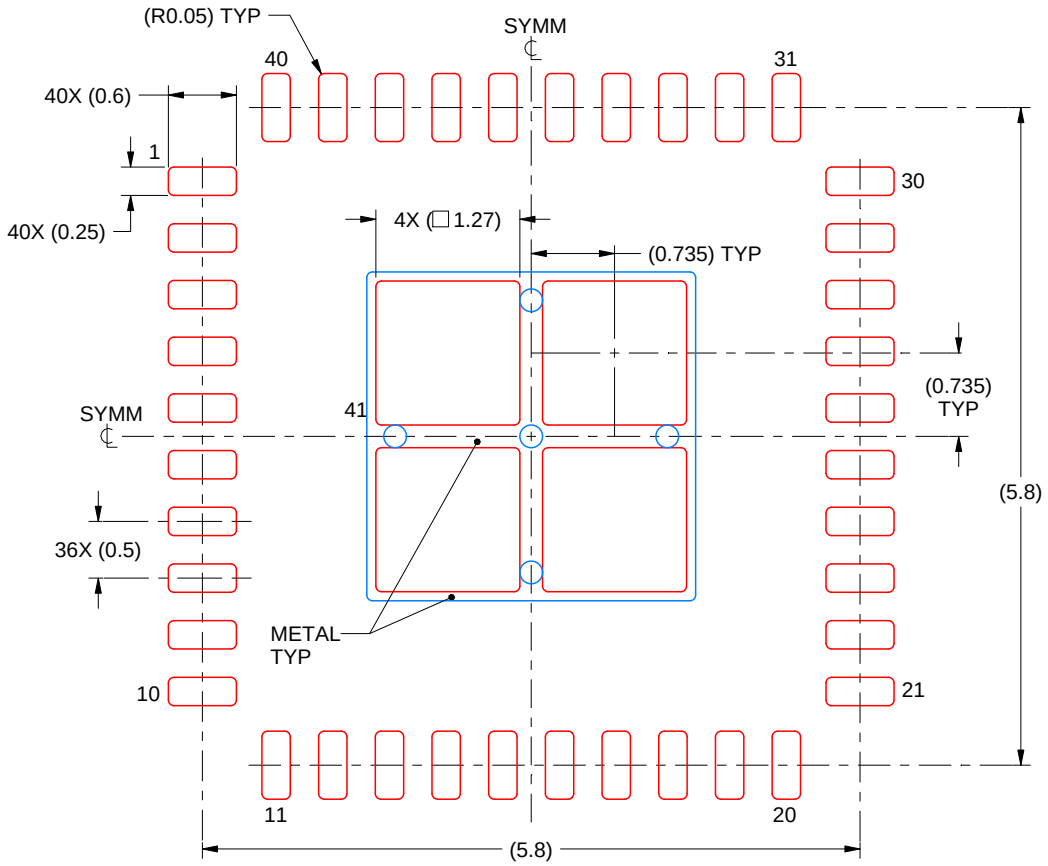
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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