LMH9226 シングルエンド、差動 2.3GHz～2.9GHz RF アンプ、バラン付き

1 特長

- シングル・チャネル、シングルエンド入力から差動出力への RF ゲイン・ブロック・アンプ
- 2.6GHz の中心周波数、400MHz の 1dB 帯域幅をサポート
- Z_{LOAD} = 50Ω に対して 1dB 帯域幅全体で 17dB (標準値) のゲイン
- 1dB 帯域幅で 3dB 未満のノイズ指数
- Z_{LOAD} = 50Ω に対して 2dBm の 2 トーン出力電力で 35dBm の OIP3
- Z_{LOAD} = 50Ω に対して 17.5dBm の出力 P1dB
- 3.3V 単一電源で 275mW の消費電力
- 最高 T_A = 105℃の動作温度

2 アプリケーション

- 5G m-MIMO 基地局
- アクティブ・アンテナ・システム (AAS) の mMIMO (マッシブ MIMO)
- スモール・セル基地局
- TDD/FDD セルラー基地局
- ワイヤレス・インフラ
- 低コスト無線
- シングルエンドから差動への変換
- バランの代替品
- RF ゲイン・ブロック
- GSPS ADC の差動ドライバ

3 概要

LMH9226 は、シングルエンド 50Ω 入力から差動 50Ω または 100Ω 出力への高性能シングル・チャネル RF ゲイン・ブロック・アンプであり、2.3GHz～2.9GHz の周波数帯に対応しています。このデバイスは、5G m-MIMO またはスモール・セル基地局アプリケーションの要件を満たすのに最適です。本デバイスは、パッシブ・バランを接続したシングルエンド入力差動出力 RF ゲイン・ブロック機能を統合しており、レシーバ信号チェーンの最終段でアナログ / デジタル・コンバータ (ADC) の差動入力のフルスケール電圧を駆動するために主に使用されます。

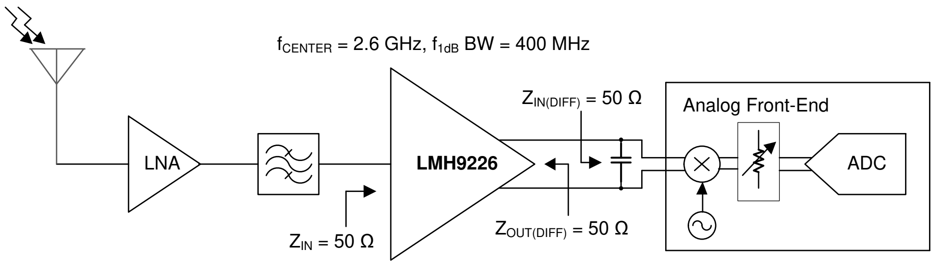
LMH9226 は、2.6GHz において 17dB (標準値) のゲインと 35dBm の出力 IP3 という優れた線形性能を備えており、400MHz の 1dB 帯域幅全体にわたって 3dB 未満のノイズ指数を維持します。このデバイスは、シングルエンド入力で 50Ω のインピーダンスと内部的に整合します。差動出力は、外部整合回路を使わずに 50Ω のインピーダンスと簡単に接続できます。100Ω のインピーダンスに整合させるには、2.6GHz で通常 0.3dB のゲイン損失をもたらす外部整合回路が必要です。

製品情報[1]

型番	パッケージ	本体サイズ(公称)
LMH9226	WQFN(12)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

LMH9226：2.3GHz～2.9GHz シングルエンド入力差動出力 RF ゲイン・ブロック・アンプ



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

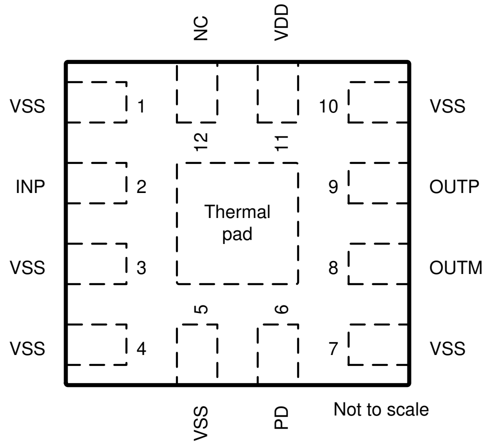
日付	リビジョン	注
2019年12月	*	初版

5 概要（続き）

このデバイスは、3.3V 単一電源で動作させた場合、スタンバイ電力が約 275mW に過ぎないため、高密度、5G、マッシブ・マルチ入力 / マルチ出力 (MIMO) アプリケーションに適しています。このデバイスは省スペースの 2mm × 2mm、12 ピンの WQFN パッケージで供給されます。このデバイスは最高 105℃の動作温度で定格が規定されているため、堅牢なシステム設計が可能です。1.8V JEDEC 準拠のパワーダウン・ピンを利用すると、時分割多重化 (TDD) システムに適した高速なデバイスの電源オン / オフが可能です。

6 Pin Configuration and Functions

RRL Package
12-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VSS	Power	Analog ground
2	INP	Input	RF single-ended input into amplifier
3	VSS	Power	Analog ground
4	VSS	Power	Analog ground
5	VSS	Power	Analog ground
6	PD	Input	Power-down connection. PD = 0 V, normal operation; PD = 1.8 V, power off mode.
7	VSS	Power	Analog ground
8	OUTM	Output	RF single-ended output negative
9	OUTP	Output	RF single-ended output positive
10	VSS	Power	Analog ground
11	VDD	Power	Positive supply voltage (3.3 V)
12	NC	—	Do not connect this pin
Thermal Pad		—	Connect the thermal pad to ground (VSS).

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	3.6	V
RF pins	INP, OUTP, OUTM	–0.3	VDD	V
Continuous wave (CW) input	f_{in} = 2.6 GHz at INP		25	dBm
Digital input pin	PD	–0.3	VDD	V
Junction temperature	T_J		150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±1000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	3.15	3.3	3.45	V
T_A	Ambient temperature	–40		105	°C
T_J	Junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		LMH9226 RRL PKG 12-PIN WQFN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

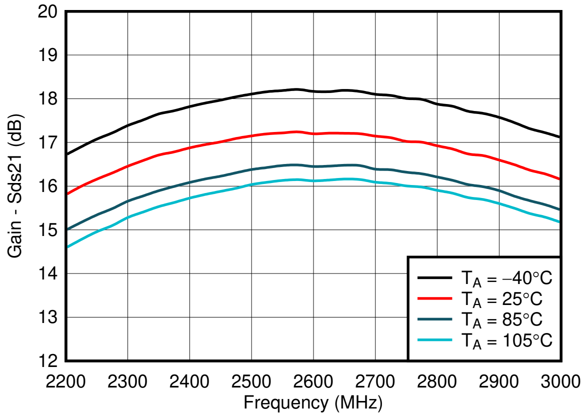
T_A = +25°C, VDD = 3.3 V, center frequency (f_{in}) = 2.6 GHz, single-ended input impedance (Z_{IN}) = 50 Ω, differential output impedance (Z_{LOAD}) = 50 Ω, $P_{OUT(TOTAL)}$ = 8 dBm into Z_{LOAD} = 50 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF PERFORMANCE						
f_{RF}	RF frequency range		2300		2900	MHz
BW_{1dB}	1-dB bandwidth	Center Frequency (f_{in}) = 2.6 GHz		400		MHz
S21	Gain	f_{in} = 2.6 GHz		17		dB
NF	Noise figure	f_{in} = 2.6 GHz, R_S = 50 Ω		3		dB
OIP1	Output P1dB	f_{in} = 2.6 GHz, R_{LOAD} = 50 Ω		17.5		dBm
OIP3	Output IP3	f_{in} = 2.6 GHz ± 10 MHz spacing, $P_{OUT/TONE}$ = 2 dBm		35		dBm
	Differential output gain imbalance (1)			0.5		dB
	Differential output phase imbalance (1)			4		degree
S11	Input return loss	f_{in} = 2.6 GHz, BW = 400 MHz		–11		dB
Z_{IN}	Single ended input reference impedance			50		Ω
S22	Differential output return loss	f_{in} = 2.6 GHz, BW = 400 MHz		–12		dB
Z_{LOAD}	Differential ouput reference impedance			50		Ω
S12	Reverse isolation	f_{in} = 2.6 GHz		–35		dB
CMRR	Common-mode rejection ratio (2)			27		dB
SWITCHING AND DIGITAL INPUT CHARACTERISTICS						
t_{ON}	Turn-on time	PD pin = 1.8 V to 0 V, f_{in} = 2.6 GHz		0.5		µs
t_{OFF}	Turn-off time	PD pin = 0 V to 1.8 V, f_{in} = 2.6 GHz		0.2		µs
V_{IH}	High-level input voltage (3)	At the PD pin	1.4			V
V_{IL}	Low-level input voltage (3)	At the PD pin			0.5	V
I_{IH}	High-level input current (3)	At the PD pin		28	60	µA
I_{IL}	Low-level input current (3)	At the PD pin		10	30	µA
DC CURRENT AND POWER CONSUMPTION						
I_{VDD_ON}	Supply current (3)	PD pin = 0 V		84	100	mA
I_{VDD_PD}	Power-down current (3)	PD pin = 1.8 V			10	mA
P_{dis}	Power dissipation	VDD = 3.3 V		275		mW

(1) Measured at f_{in} = 2.6GHz, over the BW_{1dB}
(2) CMRR is calculated using (S21-S31)/(S21+S31) for receive (1 is input port, 2 and 3 are differential output ports)
(3) 100% tested at T_A = 25℃

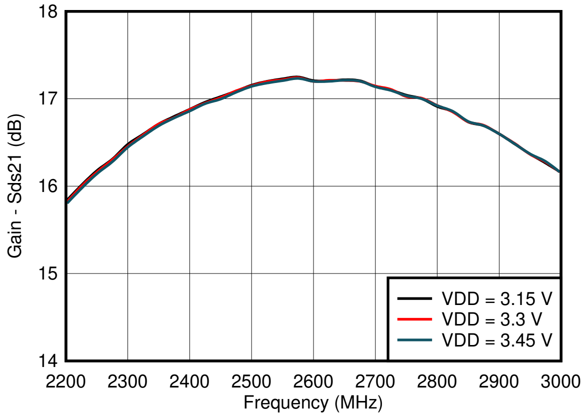
7.6 Typical Characteristics

at T_A = 25°C, VDD = 3.3 V, center frequency (f_{IN}) = 2.6 GHz, single-ended input impedance (Z_{IN}) = 50 Ω, differential output impedance (Z_{LOAD}) = 50 Ω, and $P_{OUT(TOTAL)}$ = 8 dBm into Z_{LOAD} = 50 Ω (unless otherwise noted)



P_{OUT} = 2 dBm

図 1. Gain vs Frequency and Temperature



P_{OUT} = 2 dBm

図 2. Gain vs Frequency and Supply Voltage

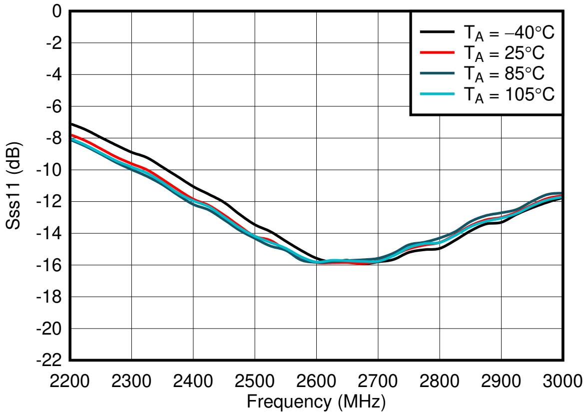


図 3. Input Return Loss vs Frequency

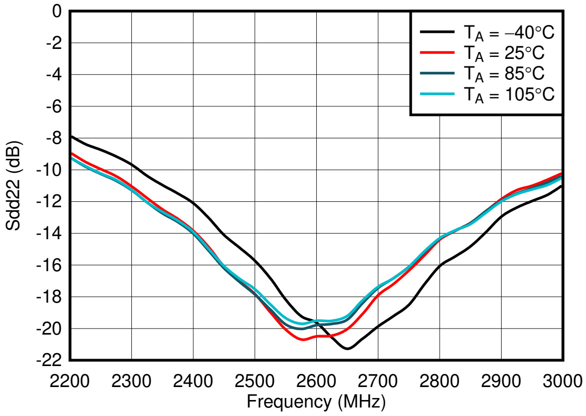


図 4. Output Return Loss vs Frequency

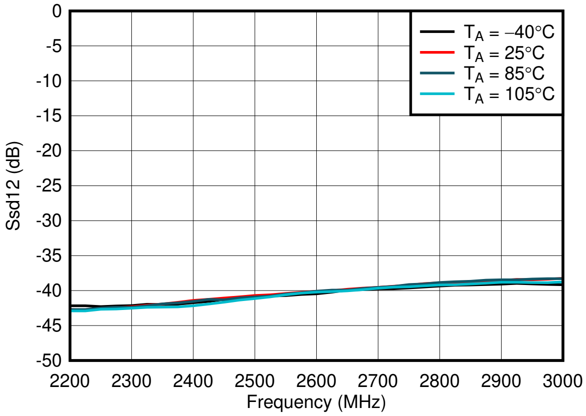
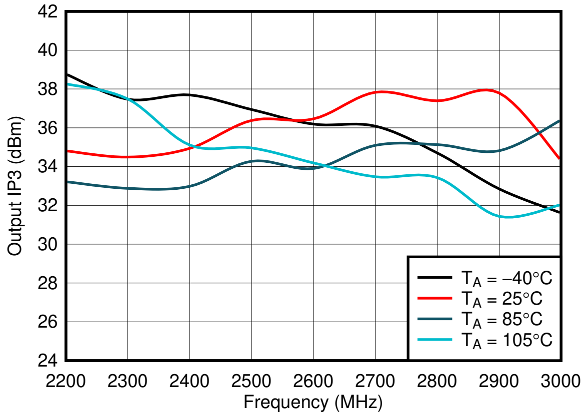


図 5. Reverse Isolation vs Frequency

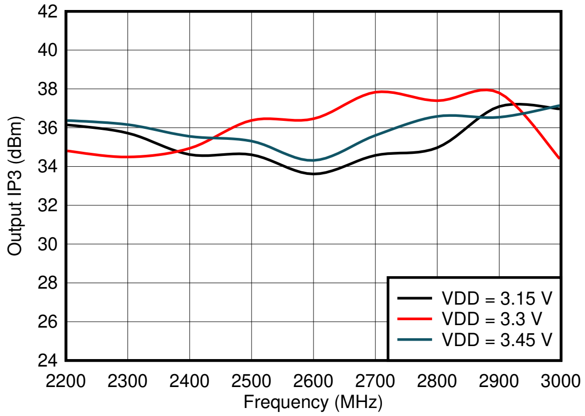


$P_{OUT/TONE}$ = 2 dBm, ±1-MHz tone spacing

図 6. Output IP3 vs Frequency and Temperature

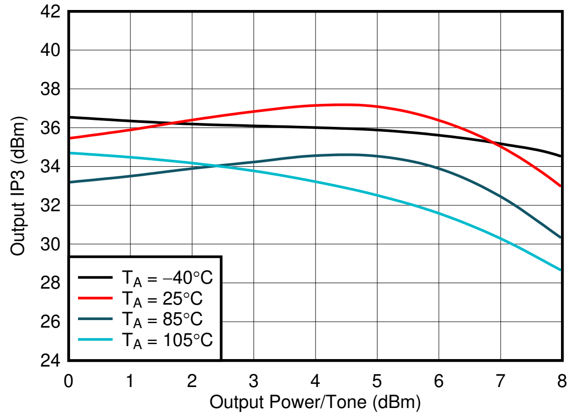
Typical Characteristics (continued)

at T_A = 25°C, VDD = 3.3 V, center frequency (f_{IN}) = 2.6 GHz, single-ended input impedance (Z_{IN}) = 50 Ω, differential output impedance (Z_{LOAD}) = 50 Ω, and $P_{OUT(TOTAL)}$ = 8 dBm into Z_{LOAD} = 50 Ω (unless otherwise noted)



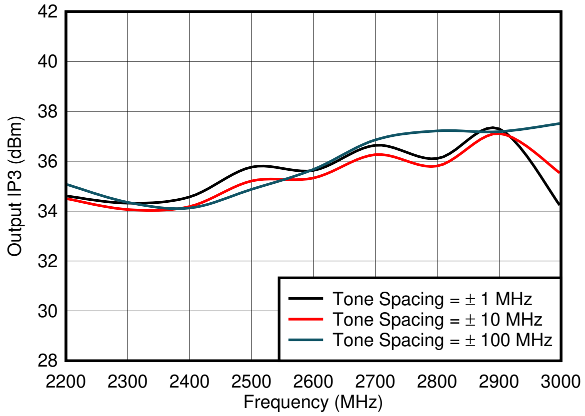
$P_{OUT/TONE}$ = 2 dBm, ±1-MHz tone spacing

図 7. Output IP3 vs Frequency and Supply Voltage



f = 2.6 GHz, ±1-MHz tone spacing

図 8. Output IP3 vs Output Power per Tone



$P_{OUT/TONE}$ = 2 dBm

図 9. Output IP3 vs Frequency and Tone Spacing

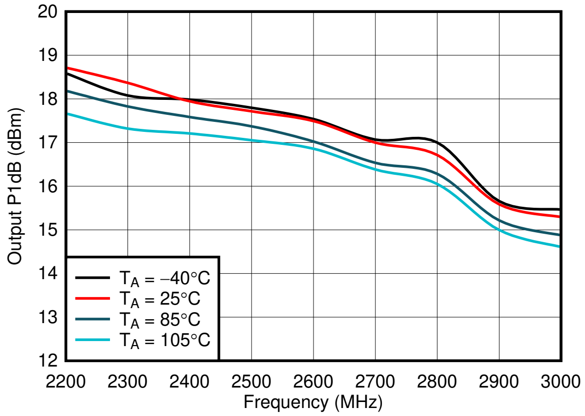


図 10. Output P1dB vs Frequency and Temperature

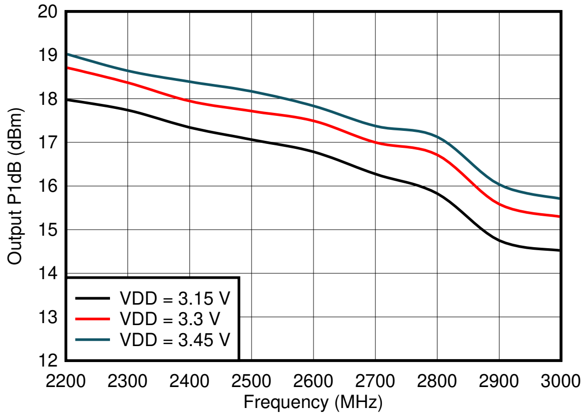
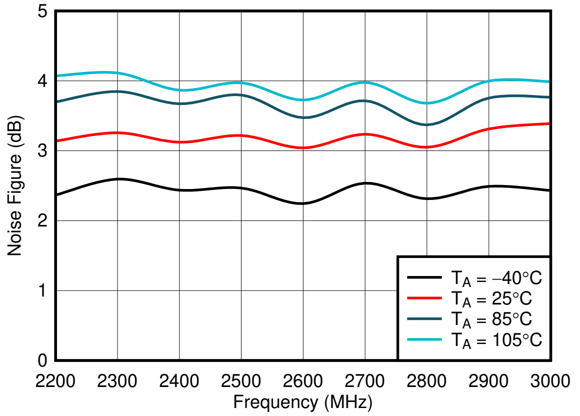


図 11. Output P1dB vs Frequency and Supply Voltage

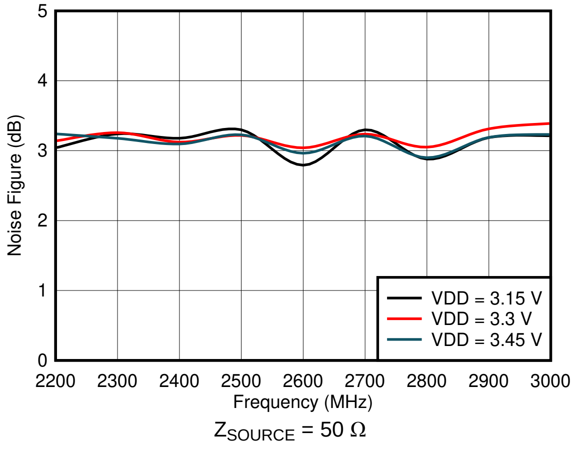


Z_{SOURCE} = 50 Ω

図 12. Noise Figure vs Frequency and Temperature

Typical Characteristics (continued)

at T_A = 25°C, VDD = 3.3 V, center frequency (f_{IN}) = 2.6 GHz, single-ended input impedance (Z_{IN}) = 50 Ω, differential output impedance (Z_{LOAD}) = 50 Ω, and $P_{OUT(TOTAL)}$ = 8 dBm into Z_{LOAD} = 50 Ω (unless otherwise noted)



Z_{SOURCE} = 50 Ω

図 13. Noise Figure vs Frequency and Supply Voltage

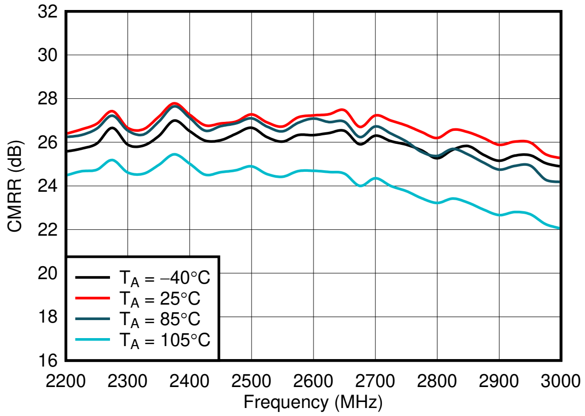


図 14. CMRR vs Frequency

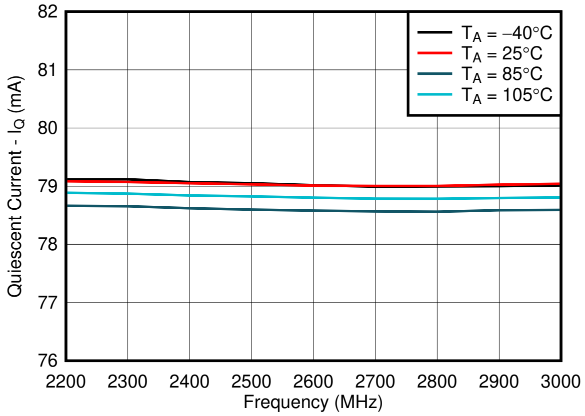


図 15. Quiescent Current vs Frequency and Temperature

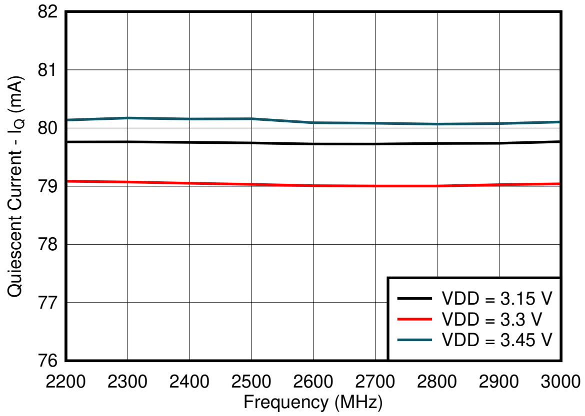


図 16. Quiescent Current vs Frequency and Supply Voltage

8 Detailed Description

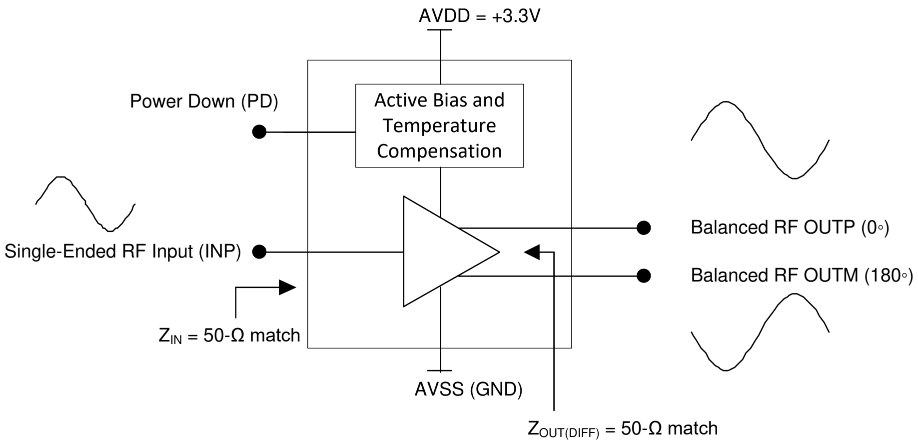
8.1 Overview

The LMH9226 is single-ended, 50-Ω input to differential 50-Ω or 100-Ω output RF gain block amplifier used in 2.3-GHz to 2.9-GHz, frequency-band, 5G, m-MIMO TDD receiver applications. The device provides a 17-dB fixed power gain with excellent linearity and noise performance across 400 MHz of the 1-dB bandwidth at the 2.6-GHz center frequency. The device is internally matched for a 50-Ω input impedance at 2.6 GHz. The device differential output can be matched to the 50-Ω impedance without external matching circuitry, or to the 100-Ω impedance with external matching circuitry (see the *Application and Implementation* section for details). The device is typically used in the final stage of a receive signal chain to drive the differential input of an analog-to-differential converter (ADC), while providing additional gain to a low-noise amplifier (LNA) to increase dynamic range and the required single-ended to differential conversion.

The LMH9226 has an on-chip active bias circuitry to maintain device performance over a wide temperature and supply voltage range. The included power-down function allows the amplifier to shut down and save power when the amplifier is not needed. Fast shut-down and start-up enable the amplifier to be used in a host of time division duplex (TDD) applications.

Operating on a single 3.3-V supply and consuming 84 mA of typical supply current, the device is available in a 2-mm × 2-mm, 12-pin WQFN package.

8.2 Functional Block Diagram



8.3 Feature Description

As shown in 図 17, the LMH9226 integrates the functionality of a single-ended RF amplifier and passive balun in a traditional receive application, achieving a small form factor with good linearity and noise performance. The active balun implementation, along with a higher operating temperature of 105°C, allows for a more robust receiver system implementation compared to a passive balun that is prone to reliability failures at high temperatures. The high-temperature operation is achieved by the on-chip, active bias circuitry that maintains device performance over a wide temperature and supply voltage range.

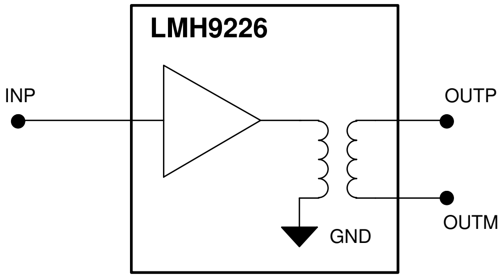


図 17. Single-Ended Input to Differential Output, Active Balun Implementation

8.4 Device Functional Modes

The LMH9226 features a PD pin that must be connected to GND for normal operation. For power-down mode, connect the PD pin to a logic high voltage of 1.8 V.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMH9226 is a single-ended, 50-Ω input to differential 50-Ω or 100-Ω output RF gain block amplifier, used in the receive path of a 2.6-GHz center frequency, 5G, TDD m-MIMO or small cell base station. The device replaces the traditional single-ended RF amplifier and passive balun offering a smaller footprint solution to the customer. TI recommends following good RF layout and grounding techniques to maximize the device performance.

9.2 Typical Application

The LMH9226 is typically used in a four transmit and four receive (4T/4R) array of active antenna system for 5G, TDD, wireless base station applications. Such a system is shown in 図 18, where the LMH9226 is used in the receive path as the final stage differential driver to an ADC input. TI typically recommends reducing the trace distance between the LMH9226 output and the ADC input to minimize amplitude and phase imbalance during the single-to-differential conversion.

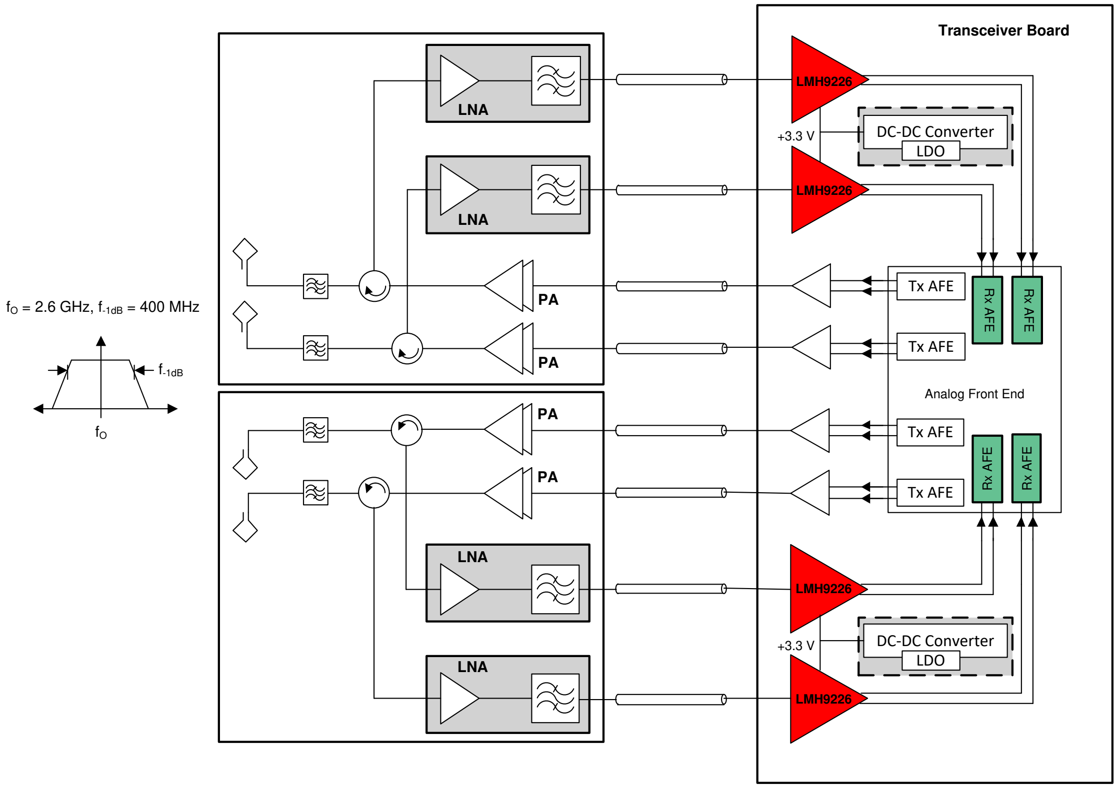


図 18. **LMH9226 in a 4T/4R 5G Active Antenna System**

Typical Application (continued)

The 4T/4R system is easily scaled to 16T/16R, 64T/64R, or higher antenna arrays that result in proportional scaling of the overall system power dissipation. As a result of the proportional scaling factor for multiple channels in a system, the individual device power consumption must be reduced to dissipate less overall heat in the system. Operating on a single 3.3-V supply, the LMH9226 consumes only 275 mW and therefore provides power saving to the customer. Multiple LMH9226 devices can be powered from a single DC/DC converter or a low-dropout regulator (LDO) operating on a 3.3-V supply. A DC/DC converter provides the most power efficient way of generating the 3.3-V supply. However, care must be taken when using the DC/DC converter to minimize the switching noise using inductor chokes and adequate isolation must be provided between the analog and digital supplies.

9.2.1 Design Requirements

表 1 shows example design requirements for an RF amplifier in a typical 5G, active antenna TDD system. The LMH9226 meets these requirements.

表 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Frequency range and 1-dB BW	2300 MHz to 2900 MHz with 400 MHz of 1-dB BW
Configuration	Single-ended 50-Ω input to differential 50-Ω output
Power gain	> 15 dB
Output IP3 at $P_{OUT/TONE}$ = 2 dBm	> 32 dBm
Noise figure at Zin = 50 Ω	< 4 dB
Output P1dB	< 17 dBm
Power consumption	< 350 mW
Turn-on time	< 1 µs
Package size	2 mm × 2 mm^2

9.2.2 Detailed Design Procedure

The LMH9226 is a single-to-differential RF gain block amplifier for a 2.6-GHz center frequency application with 400 MHz of the 1-dB bandwidth. 図 19 shows a single receive channel consisting of a low-noise amplifier (LNA) that sits close to the antenna and drives the signal into a single-ended, 50-Ω coaxial cable that then connects to a transceiver board. The LMH9226 that sits at the transceiver board input converts this single-ended signal received from the coax cable into a differential signal, thereby offering low noise and distortion performance while interfacing with the receiver analog front-end (AFE). The LMH9226 input impedance must be matched to 50 Ω to prevent any signal reflections resulting from the coax cable. The device differential output interfaces directly with the differential input of an AFE. The output matching is optimized for a 50-Ω output at the 2.6-GHz center frequency with 400 MHz of the 1-dB bandwidth. The AFE input impedance must be matched to 50 Ω at 2.6 GHz as well to prevent any ripple in the frequency response.

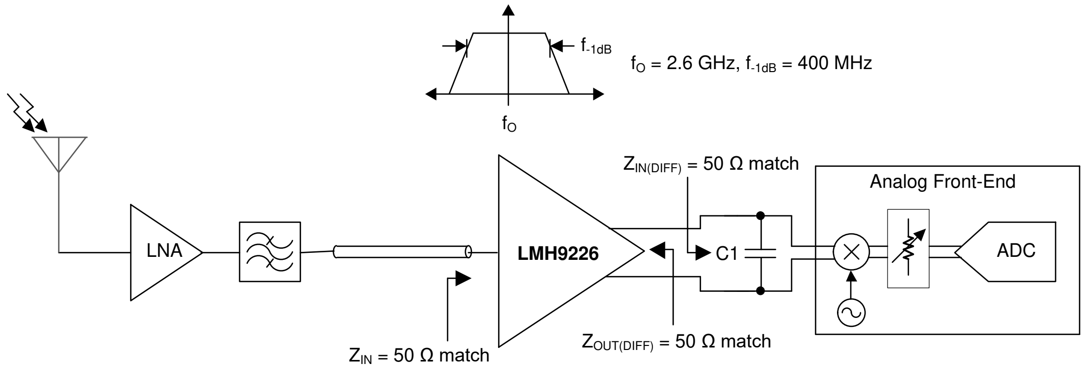


図 19. LMH9226 in a Receive Application Driving an AFE ($Z_{OUT(DIFF)}$ = 50 Ω)

For interfacing with a 100-Ω differential input AFE, as shown in 図 20, an external matching circuitry is needed close to the LMH9226 output. 表 2 lists example recommended component values when transforming the LMH9226 output impedance from 50 Ω to 100 Ω. The component values must be tweaked on the board, depending on the trace length between the matching circuitry and the AFE input to maintain 400 MHz of the 1-dB BW at the 2.6-GHz center frequency. LC component values must be selected with Q(min) > 30 that have a self resonant frequency (SRF) sufficiently higher than the desired frequency of operation. 図 21 and 図 22 provide a comparison of device performance when interfacing with a 50-Ω output matching as compared to a 100-Ω output matching. As depicted in 図 21, the forward path gain (S_{DS21}) is slightly lower for the 100-Ω differential output impedance because of the extra loss in the external matching circuitry.

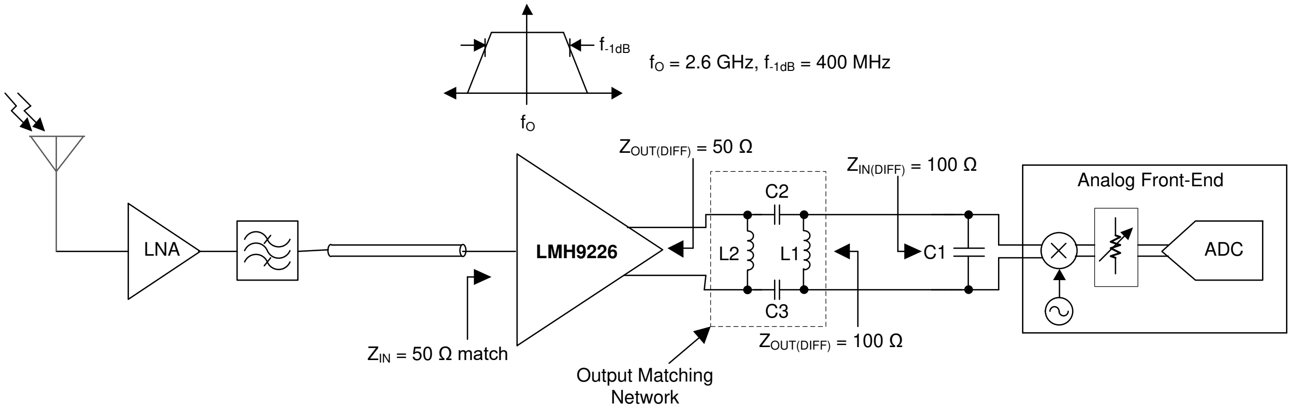


図 20. LMH9226 in a Receive Application Driving an AFE ($Z_{OUT(DIFF)}$ = 100 Ω)

表 2. Output Matching Network Component Values

COMPONENT	VALUE
C2, C3	2.2 pF
L1	6.2 nH
L2	Do not install (DNI)

Following the recommended RF layout with good quality RF components and local DC bypass capacitors ensures optimal performance is achieved. TI provides various support materials including S-parameter and ADS models to allow the design to be optimized to the application-specific performance needs.

9.2.3 Application Curves

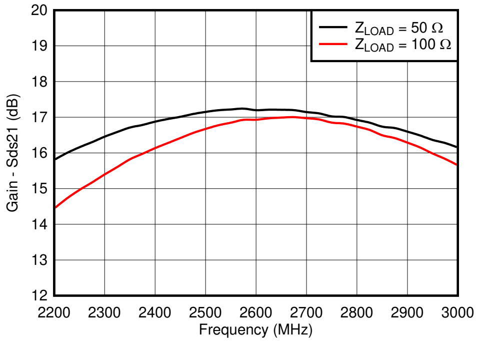


図 21. Power Gain vs Frequency and Z_{LOAD}

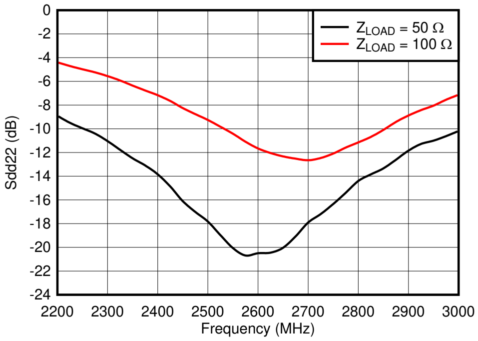


図 22. Output Return Loss vs Frequency and Z_{LOAD}

10 Power Supply Recommendations

The LMH9226 operates on a common nominal 3.3-V supply voltage. The supply voltage is recommended to be isolated through the decoupling capacitors placed close to the device. Select capacitors with a self-resonant frequency near the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device.

The LMH9226 can be powered from a DC/DC converter or an LDO operating on a 3.3-V supply. A DC/DC converter provides the most power efficient way of generating the 3.3-V supply. However, care must be taken when using the DC/DC converter to minimize the switching noise from inductor chokes and adequate isolation must be provided between the analog and digital supplies.

11 Layout

11.1 Layout Guidelines

When dealing with an RF amplifier with relatively high gain and a center frequency of 2.6 GHz, certain board layout precautions must be taken to ensure stability and optimum performance. TI recommends that the LMH9226 board be multi-layered to improve thermal performance, grounding, and power-supply decoupling. 図 23 shows a good layout example. In 図 23, only the top signal layer and its adjacent ground reference plane are shown.

- Excellent electrical connection from the thermal pad to the board ground is essential. Use the recommended footprint, solder the pad to the board, and do not include a solder mask under the pad.
- Connect the pad ground to the device terminal ground on the top board layer.
- Verify that the return DC and RF current path have a low impedance ground plane directly under the package and that the RF signal traces into and out of the amplifier.
- Ensure that ground planes on the top and any internal layers are well stitched with vias.
- Do not route RF signal lines over breaks in the reference ground plane.
- Avoid routing clocks and digital control lines near RF signal lines.
- Do not route RF or DC signal lines over noisy power planes. Ground is the best reference, although clean power planes can serve where necessary.
- Place supply decoupling close to the device.
- The differential output traces must be symmetrical in order to achieve the best linearity performance.

A board layout software package can simplify the trace thickness design to maintain impedances for controlled impedance signals. To isolate the affect of board parasitic on frequency response, TI recommends placing the external output matching resistors close to the amplifier output pins. See the *LMH9226 Evaluation Module* user guide for more details on board layout and design.

11.2 Layout Example

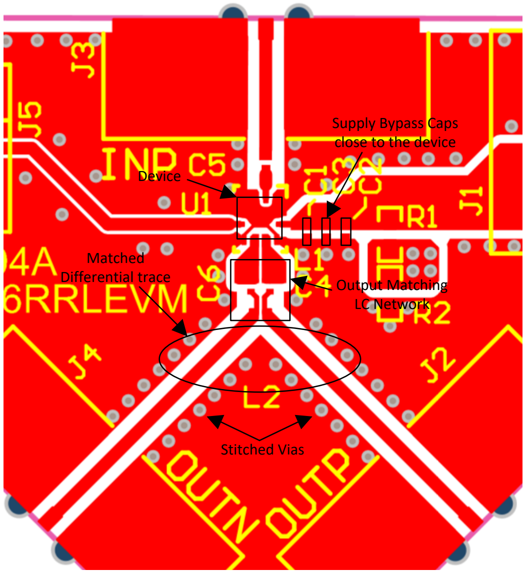


図 23. Supply Bypass and Output Matching

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

テキサス・インスツルメンツ『*LMH9226 Evaluation Module*』ユーザー・ガイド (英語)

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH9226IRRLR	ACTIVE	WQFN	RRL	12	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	22GO	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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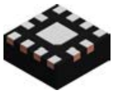
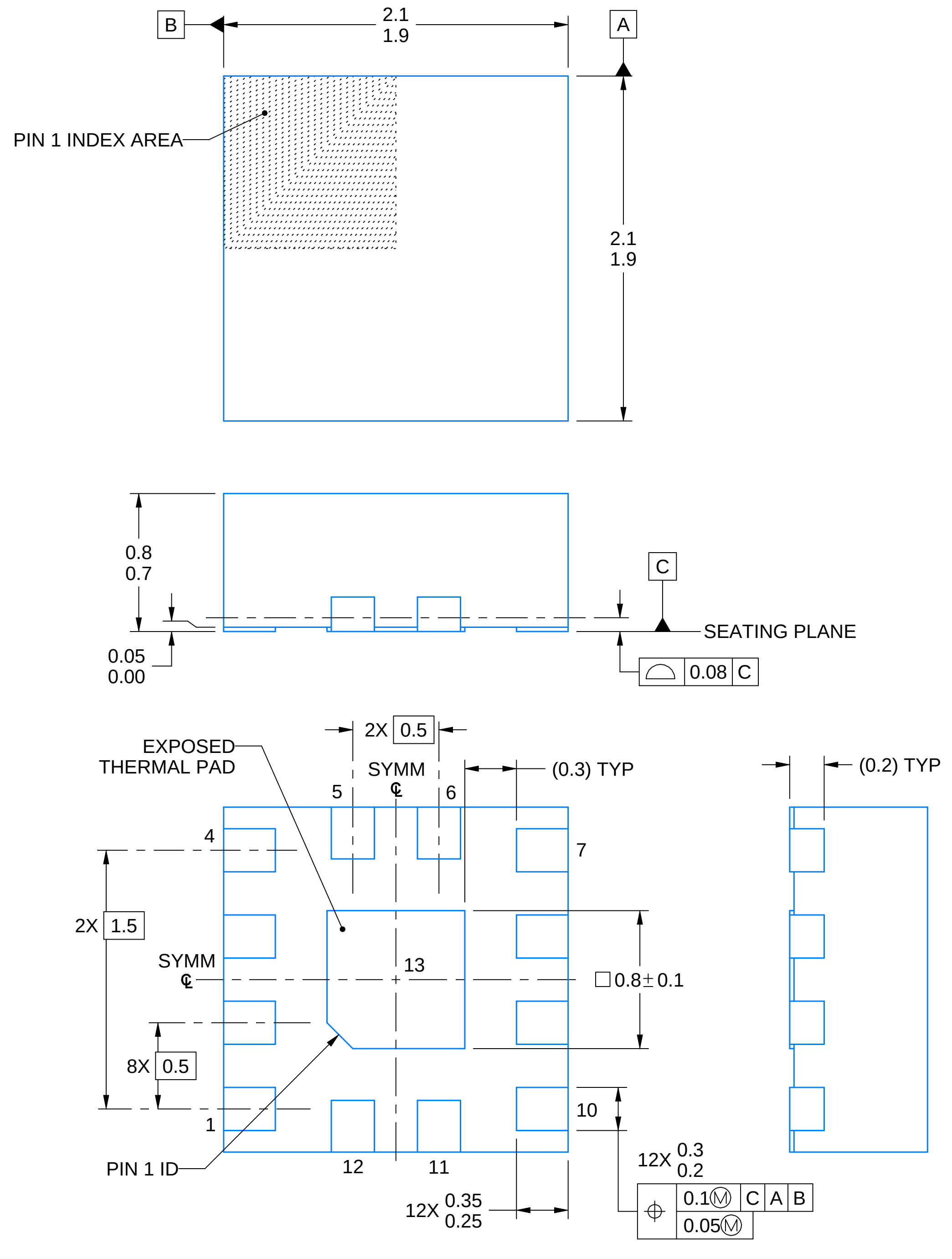
PACKAGE OUTLINE

RRL0012A



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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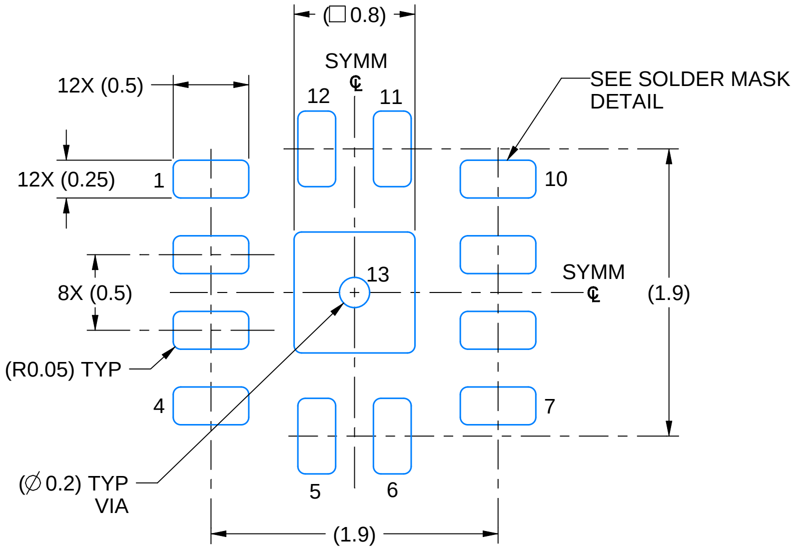
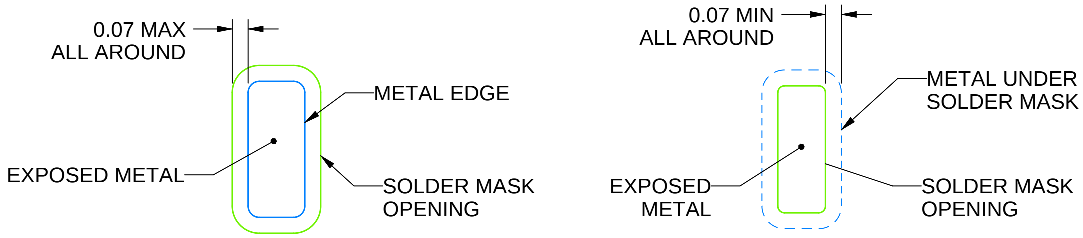
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



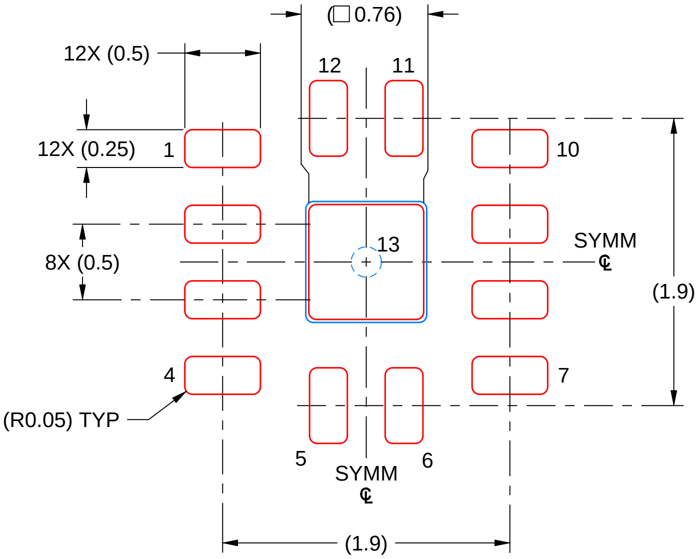
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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