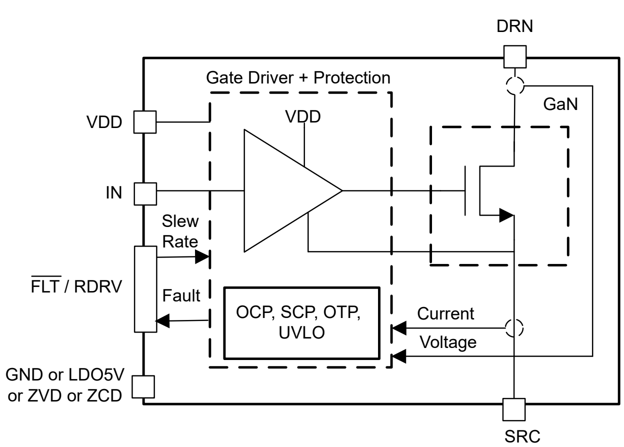
LMG365xR070 ドライバと保護機能を内蔵した 650V、70mΩ GaN FET

1 特長

- ゲートドライバ内蔵、650V、70mΩ の GaN 電力 FET
  - >200V/ns の FET ホールド オフ
  - 調整可能なスルーレートによるスイッチングパフォーマンスの最適化と EMI の軽減
    - 10V/ns から 100V/ns の有効化スルーレート
    - 10V/ns からフルスピードの有効化スルーレート
  - 電源ピンと入力ロジック ピンの 9V から 26V の電圧範囲で動作します
- 堅牢な保護
  - サイクル単位の過電流保護と応答時間 300ns 未満のラッチ付き短絡保護
  - ハード スイッチング中のサージ耐性：720V
  - 内部過熱および UVLO 監視機能による自己保護
- サーマル パッド付きの 9.8mm × 11.6mm TOLL パッケージ

2 アプリケーション

- 商用ネットワークとサーバーの電源
- 商用テレコム整流器
- ソーラー インバータと産業用モーター ドライブ
- 無停電電源



概略ブロック図

3 概要

ドライバと保護機能を内蔵した LMG365xR070 GaN FET は、スイッチ モード パワー コンバータを対象としています。このデバイスを使うと、設計者は比類ない電力密度と効率を実現できます。

調整可能なゲート ドライブ強度により、独立な有効化と最大限無効化スルーレートの制御が可能で、EMI のアクティブ制御とスイッチング性能の最適化に使用できます。有効化スルーレートは 100V/ns10 から V/ns まで変動する可能性がありますが、負荷電流の大きさに基づいて 10V/ns の範囲で無効化スルーレートの最大値に制限することができます。保護機能として、低電圧誤動作防止 (UVLO)、サイクル単位の電流制限、短絡保護、および過熱保護が搭載されています。LMG3651R070 は、外部デジタルアイソレータへの電力供給に使用できる LDO5V ピンで 5V LDO 出力を供給します。LMG3656R070 は、ゼロ電圧検出 (ZVD) 機能を備えており、ゼロ電圧スイッチングが発生したとき ZVD ピンからパルスを出力します。LMG3657R070 は、ドレイン-ソース間電流が負であり、ゼロクロスポイント検出時に Low に遷移すると ZCD ピンを High に設定するゼロ電流検出 (ZCD) 機能を備えています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LMG365xR070	KLA (TOLL, 9)	9.8 mm × 11.6mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。

製品情報

部品番号 (1)	ピン 7
LMG3650R070	GND
LMG3651R070	LDO5V
LMG3656R070	ZVD
LMG3657R070	ZCD

(1) 製品比較表を参照してください。

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4 Device Comparison

表 4-1. Device Comparison

DEVICE NAME	$R_{DS(on)}$	Pin 7
LMG3650R025	25mΩ	GND
LMG3651R025		LDO5V
LMG3656R025		ZVD
LMG3657R025		ZCD
LMG3650R035	35mΩ	GND
LMG3651R035		LDO5V
LMG3656R035		ZVD
LMG3657R035		ZCD
LMG3650R070	70mΩ	GND
LMG3651R070		LDO5V
LMG3656R070		ZVD
LMG3657R070		ZCD

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5 Pin Configuration and Functions

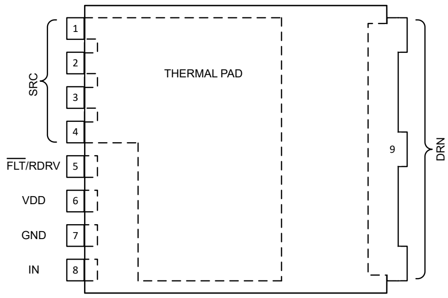

図 5-1. LMG3650R070, TOLL Package (Top View)

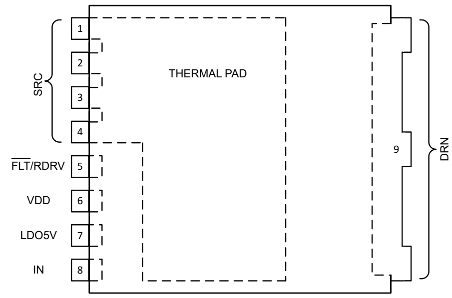

図 5-2. LMG3651R070, TOLL Package (Top View)

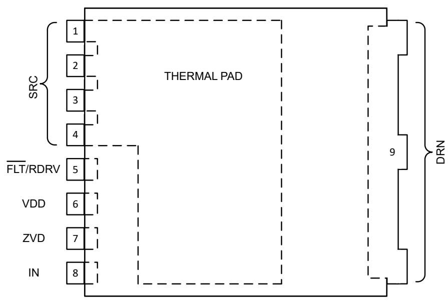

図 5-3. LMG3656R070, TOLL Package (Top View)

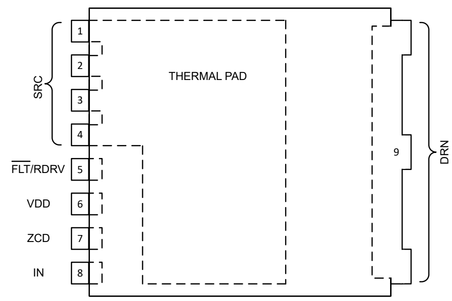

図 5-4. LMG3657R070, TOLL Package (Top View)

表 5-1. Pin Functions

PIN					TYPE (1)	DESCRIPTION
NAME	LMG3650R070	LMG3651R070	LMG3656R070	LMG3657R070		
SRC	1 - 4	1 - 4	1 - 4	1 - 4	P	GaN FET source.
$\overline{FLT}$/RDRV	5	5	5	5	O, I	Fault monitoring and drive strength selection pin. Connect a resistor from this pin to GND to set the turn-on drive strength. Connect a resistor in series with capacitor from this pin to GND to set the turn-off drive strength. Slew rates are set one time at the time of power up, then the pin is used for fault monitoring.
VDD	6	6	6	6	P	Device input supply
GND	7	—	—	—	G	Signal ground. Internally connected to SRC, and THERMAL PAD.
LDO5V	—	7	—	—	P	5V LDO output for external digital isolator.
ZVD	—	—	7	—	O	Push-pull digital output that provides zero-voltage detection signal to indicate if device achieves zero-voltage switching in current switching cycle.
ZCD	—	—	—	7	O	Push-pull digital output that sets ZCD pin high when the drain-to-source current is negative and transitions to low upon detecting the zero-crossing point.
IN	8	8	8	8	I	CMOS compatible non inverting input used to turn the FET on and off
DRN	9	9	9	9	P	GaN FET drain
THERMAL PAD	—	—	—	—	—	Thermal pad.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to GND/SRC[(1)]

			MIN	MAX	UNIT
V_{DS}	Drain-source voltage, FET off			650	V
$V_{DS(surge)}$	Drain-source voltage, surge condition, FET off			720	V
$V_{DS(tr)(surge)}$	Drain-source transient ringing peak voltage, surge condition, FET off			800	V
	Pin voltage	VDD	-0.5	28	V
		IN	-0.5	28	V
		$\overline{FLT}$/RDRV	-0.5	5.5	V
I_D	Peak drain current, FET on			TBD	A
$I_{D(pulse)}$	Pulse drain current, FET on, t_p < 10μs.		-34	Internally Limited	A
T_J	Operating junction temperature		–40	175	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 [(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to GND/SRC

			MIN	NOM	MAX	UNIT
	Supply voltage	VDD	9		26	V
	Input voltage	IN	0		26	V
I_D	Drain current, FET on				10	A
	Positive source current	LDO5V (LMG3651)			25	mA
R_1	Resistance from external turn-on slew rate control resistor between $\overline{FLT}$/RDRV to GND		29.4		open	kΩ
R2	Resistance and capacitance from external turn-off slew rate control series resistor and capacitor configuration between $\overline{FLT}$/RDRV to GND		2		open	kΩ
C2			0		680	pF

6.4 Thermal Information

THERMAL METRIC[(1)]		KLA (TOLL)	UNIT
		9 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.73	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/SRC; –40℃ ≤ T_J ≤ 150℃; VDD = 12V; $\overline{FLT}$/RDRV resistances R1 & R2 are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$R_{DS(on)}$	Drain-source on resistance	T_J = 25°C, I_L = 6A		70	111	mΩ
		T_J = 150°C, I_L = 6A		157		mΩ
V_{SD}	Source-drain third-quadrant voltage	T_J = 25°C, I_{SD} = 0.1A		1.8		V
		T_J = 150°C, I_{SD} = 0.1A		1.8		V
		T_J = 25°C, I_{SD} = 6A		2.9		V
		T_J = 150°C, I_{SD} = 6A		3		V
I_{DSS}	Drain leakage current	T_J = 25°C, V_{DS} = 650V		TBD		µA
		T_J = 150°C, V_{DS} = 650V		TBD		µA
Q_{OSS}	Output charge	V_{DS} = 400V		61		nC
C_{OSS}	Output capacitance	V_{DS} = 400V		84		pF
E_{OSS}	Output capacitance stored energy	V_{DS} = 400V		8		µJ
$C_{OSS(tr)}$	Time related effective output capacitance	V_{DS} = 400V		152		pF
$C_{OSS(er)}$	Energy related effective output capacitance	V_{DS} = 400V		97		pF
Q_{RR}	Reverse recovery charge			0		nC
OVERCURRENT AND SHORT-CIRCUIT PROTECTIONS						
$I_{T(OC)}$	Overcurrent fault - threshold current		16.4	18.2	20	A
$V_{T(Idsat)}$	Saturation current detection - threshold voltage		8.7	9	9.6	V
OVERTEMPERATURE PROTECTION						
T_{T+}	Temperature fault - positive-going threshold temperature			190		°C
$T_{T(hyst)}$	Temperature fault - threshold temperature hysterisis			20		°C
IN						
$V_{IN,IT+}$	Positive-going input threshold voltage		1.7	2	2.45	V
$V_{IN,IT-}$	Negative-going input threshold voltage		0.7	1	1.3	V
$V_{IN,IT(hyst)}$	Input threshold voltage hysteresis			1		V
R_{PDN}	Pull-down input resistance		115	150	185	kΩ
$\overline{FLT}$/RDRV						
V_{OL}	Low-level output voltage	Output sink 8mA		0.2	0.4	V
V_{OH}	High-level output voltage	Output source 8mA	4.6	4.8		V
VDD						
$I_{VDD(ON)}$	Quiescent current when FET is ON	IN=1		1	5.7	mA
$I_{VDD(OFF)}$	Quiescent current when FET is OFF	IN=0		0.7	1.1	mA
$I_{VDD(op)}$	Operating current at 140 kHz	f_{sw} = 140kHz, V_{bus} = 400V, Hard-switched, 50% duty cycle.		1.8	3.6	mA
$V_{VDD,\ T+\ (UVLO)}$	UVLO- positive-going threshold voltage		8.1	8.5	8.9	V
$V_{VDD,\ T-\ (UVLO)}$	UVLO- negative-going threshold voltage		7.6	8	8.4	V
$V_{VDD,\ T\ (hyst)}$	UVLO- threshold voltage hystresis			0.5		V

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6.6 Switching Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/SRC; –40℃ ≤ T_J ≤ 150℃; V_{DD} = 12V; $\overline{FLT}$/RDRV resistances R1 & R2 are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIMES						
$t_{d(on)}$	Turn-on delay time	From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 0A, 100V/ns		30	45	ns
	Turn-on current rise time + delay time	From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320V, V_{BUS} = 400V, L_{HB} current = 10A, 100V/ns		35	60	ns
$t_{vf(on)}$	Turn-on voltage falling time	From V_{DS} < 320V to V_{DS} < 80V, V_{BUS} = 400V, L_{HB} current = 10A, 100V/ns	1	2.3	6	ns
	Turn-on slew rate	dv/dt when V_{DS} = 200V, V_{BUS} = 400V, L_{HB} current = 10A, 100V/ns	76	115	150	V/ns
	Pulse width distortion	slew-rate setting at 100V/ns			20	ns
	Minimum input pulse changing the output L-H-L	slew-rate setting at 100V/ns such that SW crosses 200V			50	ns
$t_{d(off)}$	Turn-off delay time at full speed	From V_{IN} < 2.5V to V_{DS} >= 10V. V_{BUS} = 400V, I_L = 34A, fastest or full turn-off speed.	12	17	35	ns
$t_{vr(off)}$	Turn-off voltage rise time at full speed	From V_{DS} >= 20V to V_{DS} >= 380V. V_{BUS} = 400V, I_L = 34A, fastest or full turn-off speed.	3	4.5	10	ns
STARTUP TIMES						
T_{DRV_START}	Driver startup delay	From Driver supply crossing UVLO to switch turning on if IN is high.		35	65	µs
FAULT TIMES						
$t_{off(OC)}$	Overcurrent fault FET turn-off time, FET on before overcurrent	From I_D >= $I_{T(OC)}$ to V_{ds}> 10V, di/dt = 100A/µs, in the fastest turn-off speed		370	480	ns
$t_{off(OC\_ON)}$	Overcurrent total on time, turn-on into overcurrent.	From V_{ds} <= 10V to V_{ds} >= 10V, turning on at 110% of OC level, at 100 V/ns turn-on slew rate and fastest turn-off speed.		420	580	ns
$t_{off\_cur(SC\_ON)}$	SC on time measured through drain current	From LS I_{ds} > 50A to I_{ds} < 50A, at 100 V/ns turn-on slew rate in a half-bridge configuration.	100		500	ns
$t_{off\_cur(SC)}$	SC response time with source current measurement	From LS Vds>9V to LS Ids<50A, at 100 V/ns turn-on slew rate in a half-bridge configuration. .			300	ns
	Latched-Fault reset time	Time required to hold both gate driver input low to clear latched-fault	300	380	450	µs
ZCD/ZVD						
	ZCD delay	Current crossing zero (low to high) to ZCD output pulse di/dt = 0.03A/ns	12	25	50	ns
	ZVD delay	In rising to ZVD output pulse. 100V/ns turn-on speed.	13	20	50	ns
t_{WD_ZVD}	ZVD pulse width	V_{bus} = 10V, I_L = 5A, measure ZVD pulse width	90	120	170	ns

6.6 Switching Characteristics (続き)

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to GND/SRC; –40°C ≤ T_J ≤ 150°C; V_{DD} = 12V; $\overline{FLT}$/RDRV resistances R1 & R2 are open

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ZVD sensing time	Sensing time to fet turn on (100V/ns). IL=2A		11	25	ns

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7 Parameter Measurement Information

7.1 Switching Parameters

図 7-1 shows the circuit used to measure most switching parameters. The top device in this circuit is used to re-circulate the inductor current and functions in third-quadrant mode only. The bottom device is the active device that turns on to increase the inductor current to the desired test current. The bottom device is then turned off and on to create switching waveforms at a specific inductor current. Both the drain current (at the source) and the drain-source voltage is measured. 図 7-2 shows the specific timing measurement. TI recommends to use the half-bridge as a double pulse tester. Excessive third-quadrant operation can overheat the top device.

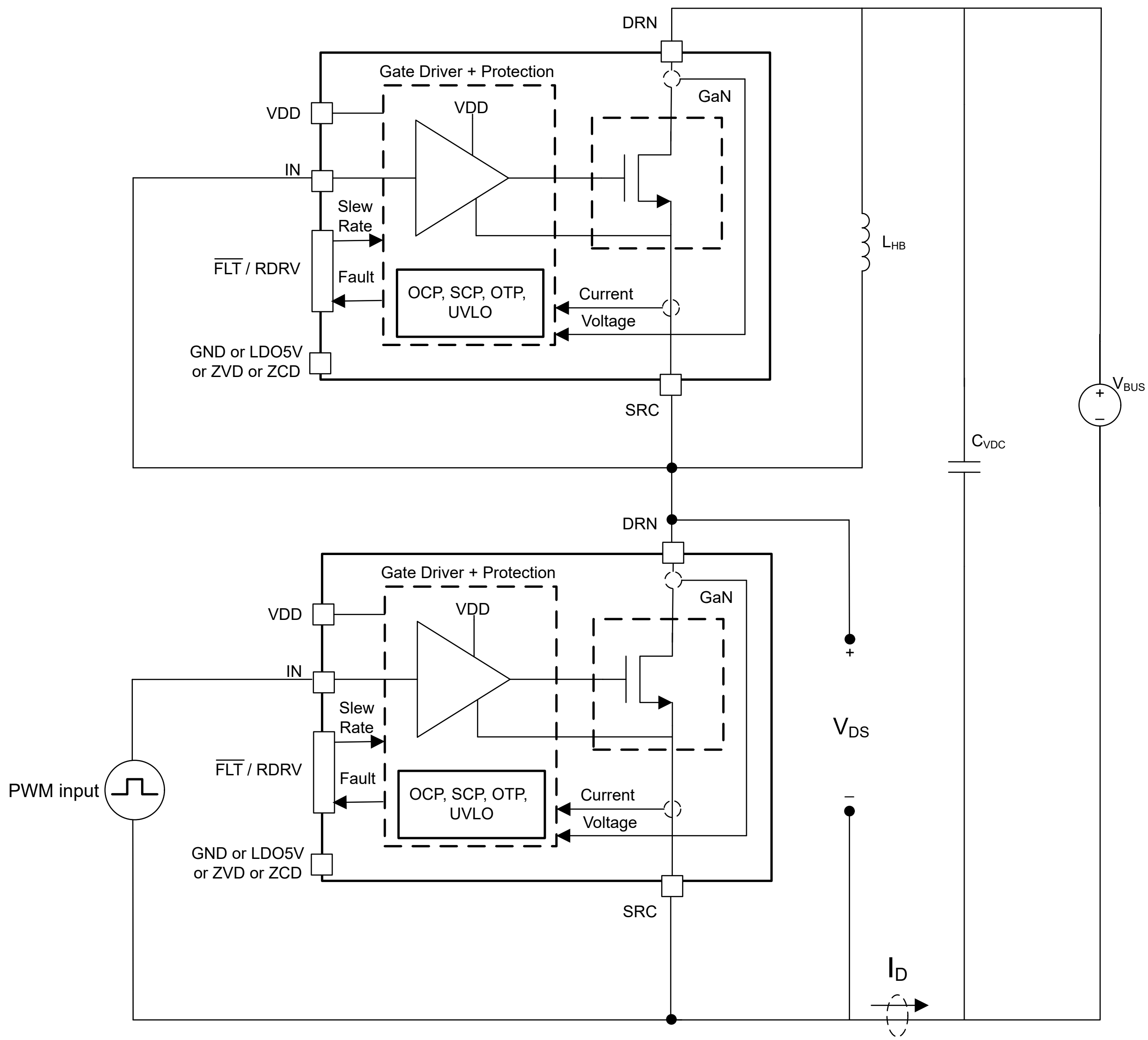

図 7-1. Circuit Used to Determine Switching Parameters

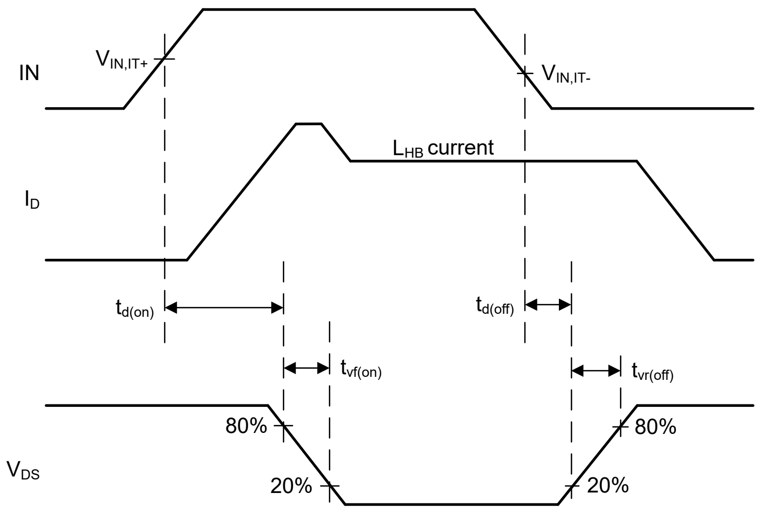

図 7-2. Measurement to Determine Propagation Delays and Slew Rates

7.1.1 Turn-On Times

The turn-on transition has two timing components: turn-on delay time, and turn-on voltage fall time. The turn-on delay time is from when IN goes high to when the drain-source voltage falls 20% below the bus voltage. The turn-on voltage fall time is from when drain-source voltage falls 20% below the bus voltage to when the drain-source voltage falls 80% below the bus voltage. Note that the turn-on timing components are a function of the turn-on drive strength resistance RDRV_on connected to the $\overline{\text{FLT}}$/RDRV pin.

7.1.2 Turn-Off Times

The turn-off transition has two timing components: turn-off delay time, and turn-off voltage rise time. The turn-off delay time is from when IN goes low to when the drain-source voltage rises to 20% of the bus voltage. The turn-off voltage rise time is from when the drain-source voltage rises from 20% of the bus voltage to when the drain-source voltage to 80% of the bus voltage. Note that the turn-off timing components are dependent on the L_{HB} load current, however LMG365xR070 also features the ability to limit turn-off drive strength. When the drain-to-source current is sufficiently high and the turn-off drive strength is limited, the timing components become dependent on the programming resistors RDRV_on, RDRV_off, and capacitance CDRV_off connected to the $\overline{\text{FLT}}$/RDRV pin.

7.1.3 Drain-Source Turn-On and Turn-off Slew Rate

The drain-source turn-on and turn-off slew rate is measured on V_{DS} around the midpoint of the bus voltage, with units in volts per nanosecond. The resistors RDRV_on, RDRV_off, and capacitance CDRV_off connected to the $\overline{\text{FLT}}$/RDRV pin is used to program the turn-on slew rate and limit the turn-off slew rate.

7.1.4 Zero-Voltage Detection Times (LMG3656R070 only)

図 7-3 defines the switching timings related to the zero-voltage detection (ZVD) block, and the device's drain-to-source voltage, IN pin signal, and ZVD output signals are demonstrated. When the device achieves zero-voltage switching (ZVS), the ZVD pin outputs a pulse-signal with width T_{WD_ZVD}, and the delay time in between IN pin's rising edge and ZVD pulse's rising edge is defined as T_{DL_ZVD}. A certain third quadrant conduction time is required to allow the device detecting a zero-voltage switching, and T_{3rd_ZVD} indicates this timing. See the セクション 8.3.8 section for more information about the ZVD timing parameters.

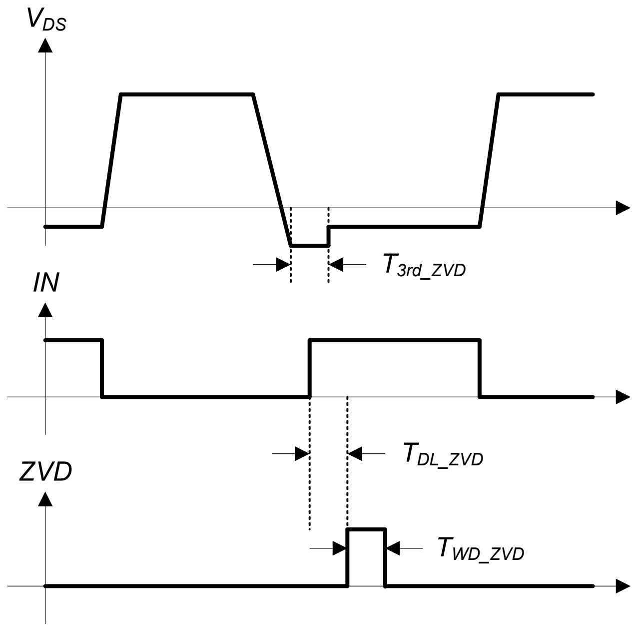

図 7-3. ZVD Timing Specifications

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8 Detailed Description

8.1 Overview

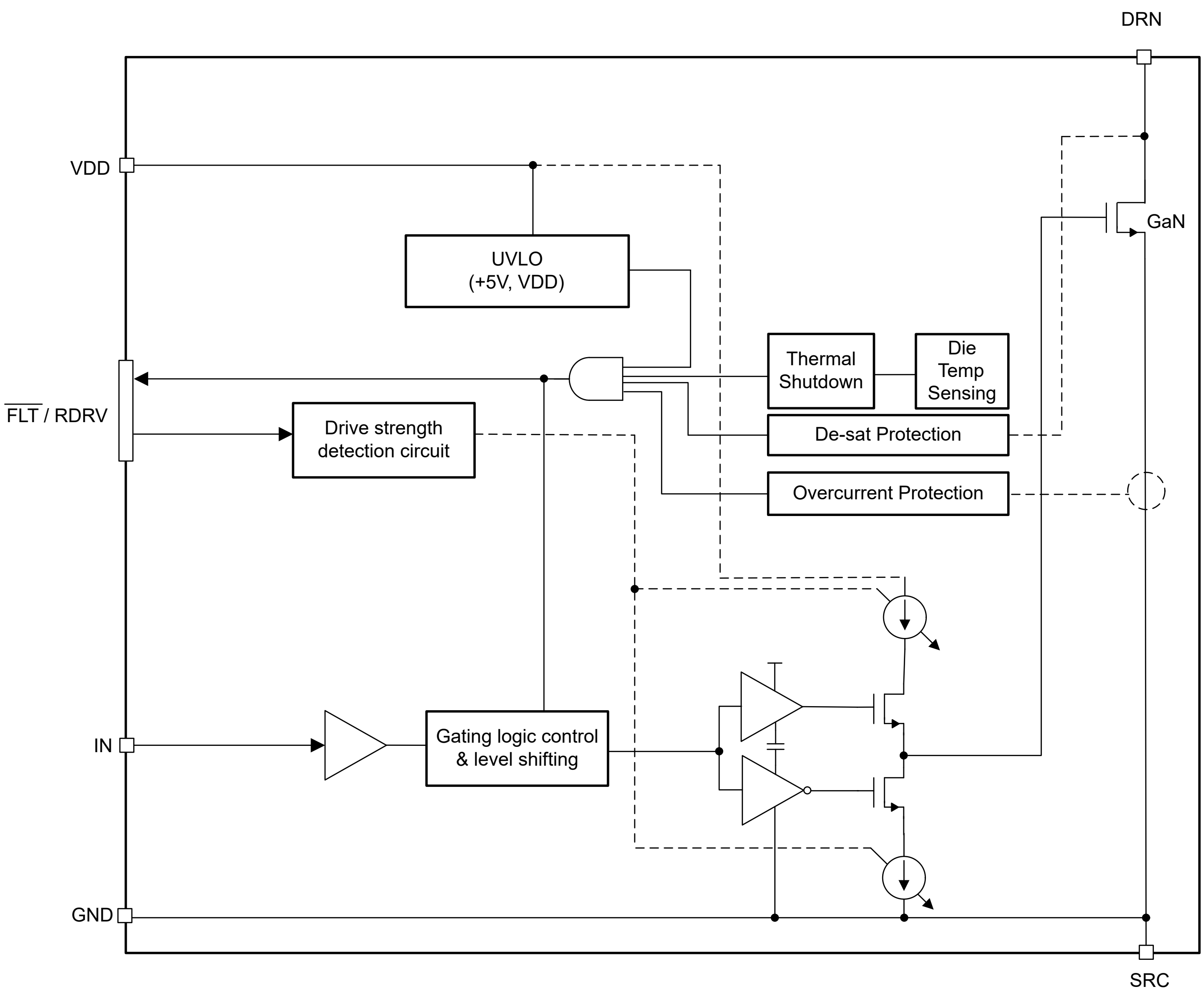
The LMG365xR070 is a high-performance power GaN device with integrated gate driver. The GaN device offers zero reverse recovery and ultra-low output capacitance, which enables high efficiency in bridge-based topologies.

The integrated driver ensures the device stays off for high drain slew rates. The integrated driver protects the GaN device from overcurrent, short-circuit, overtemperature, VDD undervoltage, and a high-impedance RDRV pin.

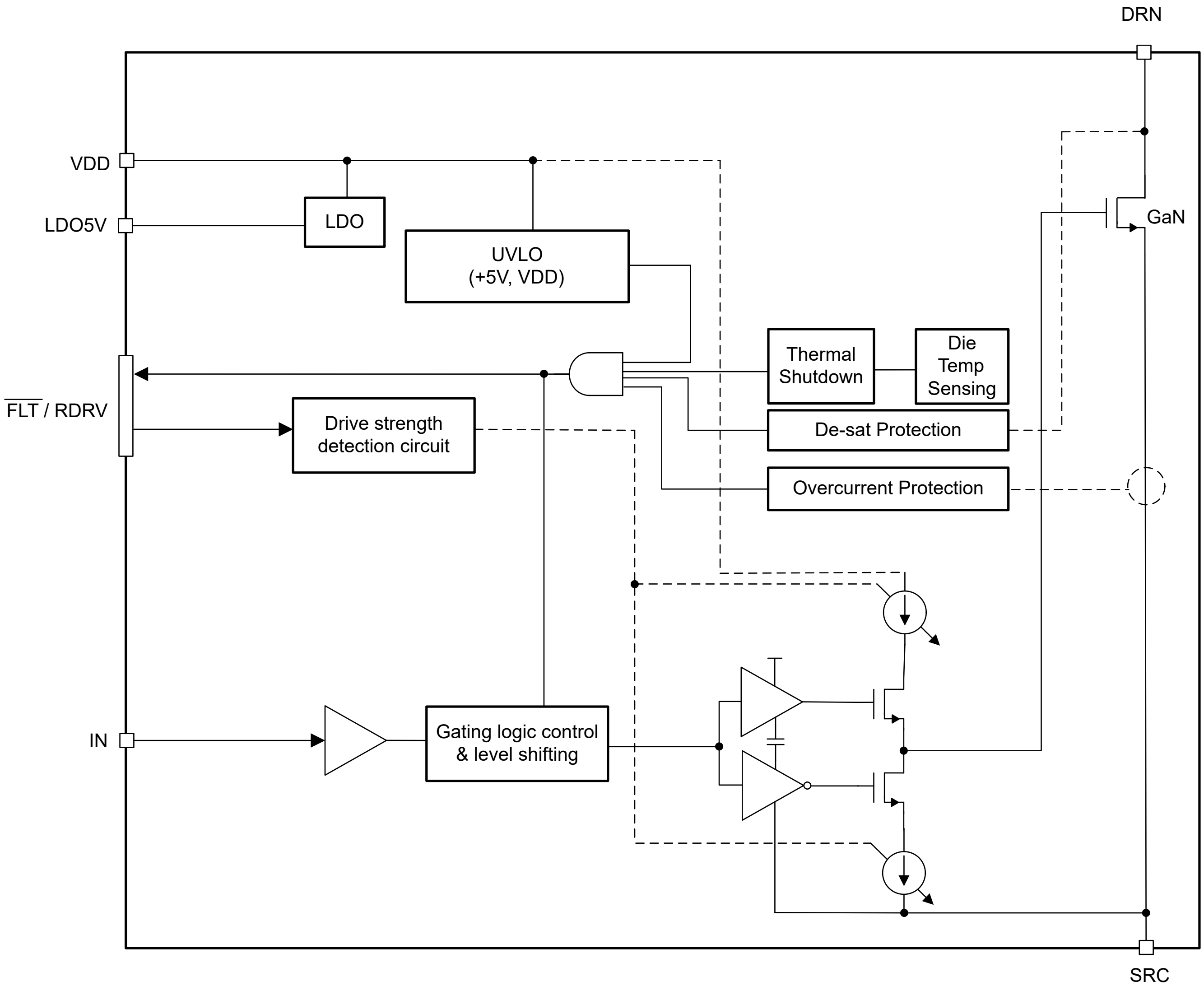
Unlike Si MOSFETs, GaN devices do not have a p-n junction from source to drain and thus have no reverse recovery charge. However, GaN devices still conduct from source to drain similar to a p-n junction body diode, but with higher voltage drop and higher conduction loss. Therefore, source-to-drain conduction time must be minimized while the LMG365xR070 GaN FET is turned off.

8.2 Functional Block Diagram

8.2.1 LMG3650R070 Functional Block Diagram



8.2.2 LMG3651R070 Functional Block Diagram



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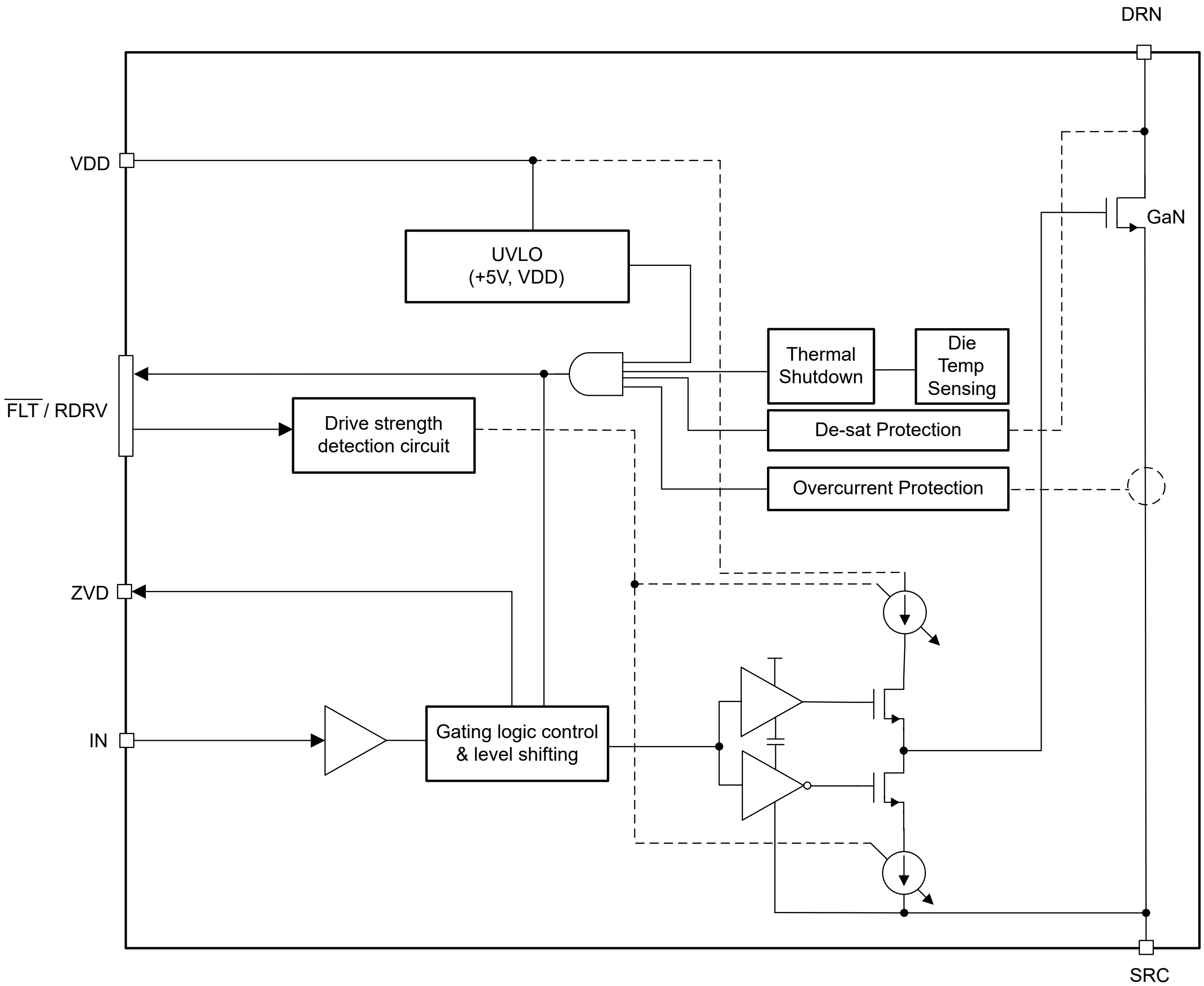
8.2.3 LMG3656R070 Functional Block Diagram



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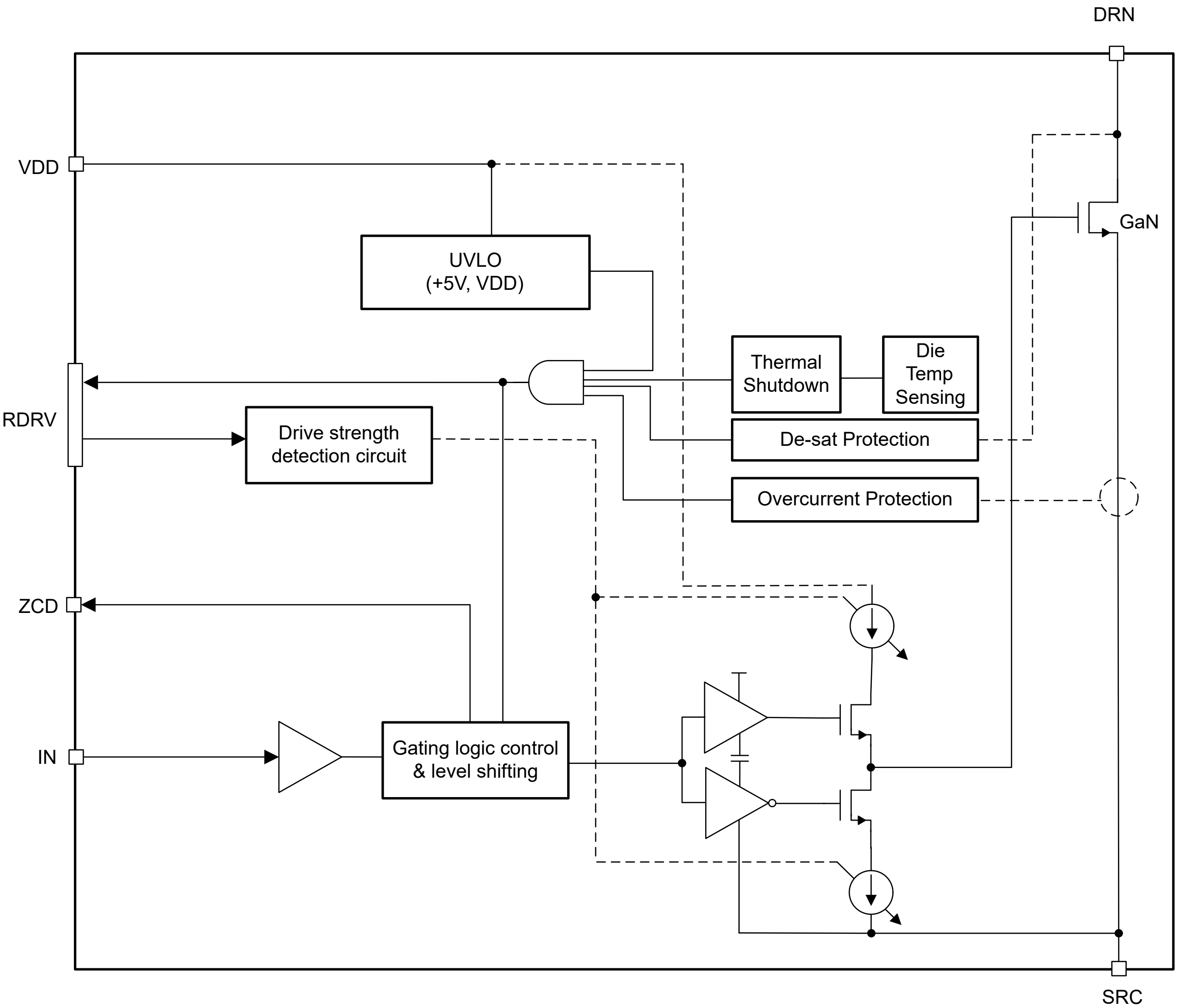
8.2.4 LMG3657R070 Functional Block Diagram



8.3 Feature Description

8.3.1 Drive Strength Adjustment

The LMG365xR070 allows users to adjust the drive strength of the device and obtain a desired slew rate, which provides flexibility when optimizing switching losses and minimizing EMI. The typical value of turn-on slew rate and the maximum value of turn-off slew rate can be independently controlled by connecting the resistors and capacitor as shown in the 図 8-1. The resistance and capacitance on $\overline{\text{FLT}}$/RDRV pin is sensed once at power-up. To do so, the device forces a step-function from 0V to 1.2V on the external R1-R2-C2 network and measures the resulting current waveform. The DC measurement determines the turn-on slew rate setting, which is programmed by the resistance R1. The AC measurement dependent on R1-R2-C2 determines the turn-off slew rate setting, which is dependent on the magnitude of the drain-to-source current charging the output capacitance but can be limited to a maximum value programmed by the resistance R2 and capacitance C2, connected in parallel to R1. 表 8-1 shows the recommended typical resistances and capacitance programming values at each slew rate setting.

The slew rate settings are determined one time at power up, then the $\overline{\text{FLT}}$/RDRV pin is used as a push-pull 5V digital output for fault monitoring, as described in *Fault Reporting*. If R2 and C2 are not used, the device turns-off at full-speed and the turn-off slew rate is strictly determined by the Coss and the load current. If R1 is not used, the device defaults to the 100V/ns slew rate setting. Using slower turn-on settings results in higher Eon losses, and slower turn-off settings results in higher Eoff losses.

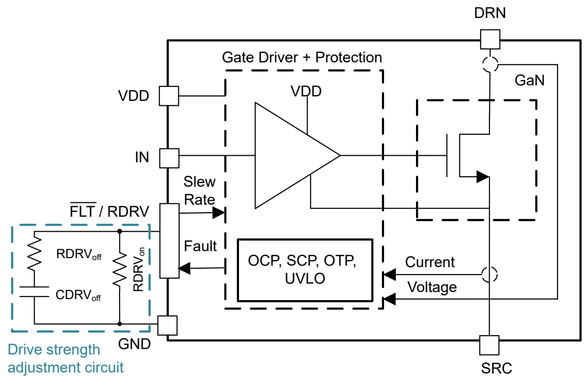


図 8-1. Drive Strength Adjustment Circuit

表 8-1. Recommended Typical Programming Resistance (kΩ) and Capacitance (pF) for Adjusting Slew Rates

TYPICAL TURN-ON SLEW RATE (V/ns)		MAXIMUM TURN-OFF SLEW RATE (V/ns)							
		10		20		40		No limit (1)	
	R1	R2	C2	R2	C2	R2	C2	R2	C2
10	29.4	2	680	4.87	270	9.09	150	high impedance (2)	
20	35.7	2	680	4.75	270	8.66	150		
40	43.2	2	680	4.64	270	8.25	150		
60	53.6	2	680	4.64	270	8.06	150		
80	69.8	2	680	4.53	270	7.68	150		
100	> 400 (2)	2	680	4.22	270	6.98	180		

(1) Fully dependent on the magnitude of the drain-to-source current charging the output capacitance
(2) Open-circuit connection for programming resistances is acceptable

For example, setting R1 = 53.6kΩ, R2 = 4.64kΩ and C2 = 270pF results in turn-on slew rate of 60V/ns and turn-off slew rate is limited to a maximum of 20V/ns.

8.3.2 VDD Supply

VDD is the input supply for the internal circuits. Wide voltage ranges from 9V to 26V are supported on VDD pin.

8.3.3 Overcurrent and Short-Circuit Protection

There are two types of current faults which can be detected by the driver: overcurrent fault and short-circuit fault.

The overcurrent protection (OCP) circuit monitors drain current and compares that current signal with an internally set limit $I_{T(OC)}$. Upon detection of the overcurrent, the LMG365xR070 performs cycle-by-cycle protection as shown in 図 8-2. In this mode, the GaN device is shut off when the drain current crosses the $I_{T(OC)}$ plus a delay $t_{off(OC)}$, but the overcurrent signal clears after the IN pin signal goes low. In the next cycle, the GaN device can turn on as normal. The cycle-by-cycle function can be used in cases where steady-state operation current is below the OCP level but transient response can still reach current limit, while the circuit operation cannot be paused. The cycle-by-cycle function also prevents the GaN device from overheating by overcurrent induced conduction losses.

The short-circuit protection is based on desaturation (de-sat) detection, which monitors the drain-source voltage V_{DS} and compares the voltage with an internally set limit $V_{T(Idsat)}$. If the OC occurs before the de-sat, the V_{DS} is below the threshold, then OC is triggered, else de-sat is triggered as shown in 図 8-3. Saturation can be damaging for the GaN to continue to operate in that condition. Therefore, if a de-sat is detected, the GaN device is turned off with an intentionally slowed driver so that a lower overshoot voltage and ringing can be achieved during the turn-off event. This fast response circuit helps protect the GaN device even under a hard short-circuit condition. In this protection, the GaN device is shut off and held off until the fault is reset by either holding the IN pin low for a period of time defined in the *Specifications* or removing power from VDD.

For safety considerations, OCP allows cycle-by-cycle operation while de-sat latches the device until reset. Both faults are reported on the $\overline{\text{FLT}}$/RDRV pin.

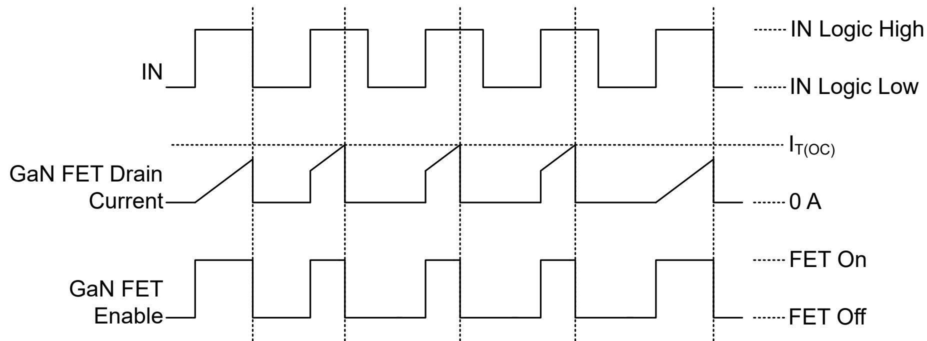


図 8-2. Cycle-by-Cycle Overcurrent Protection Operation

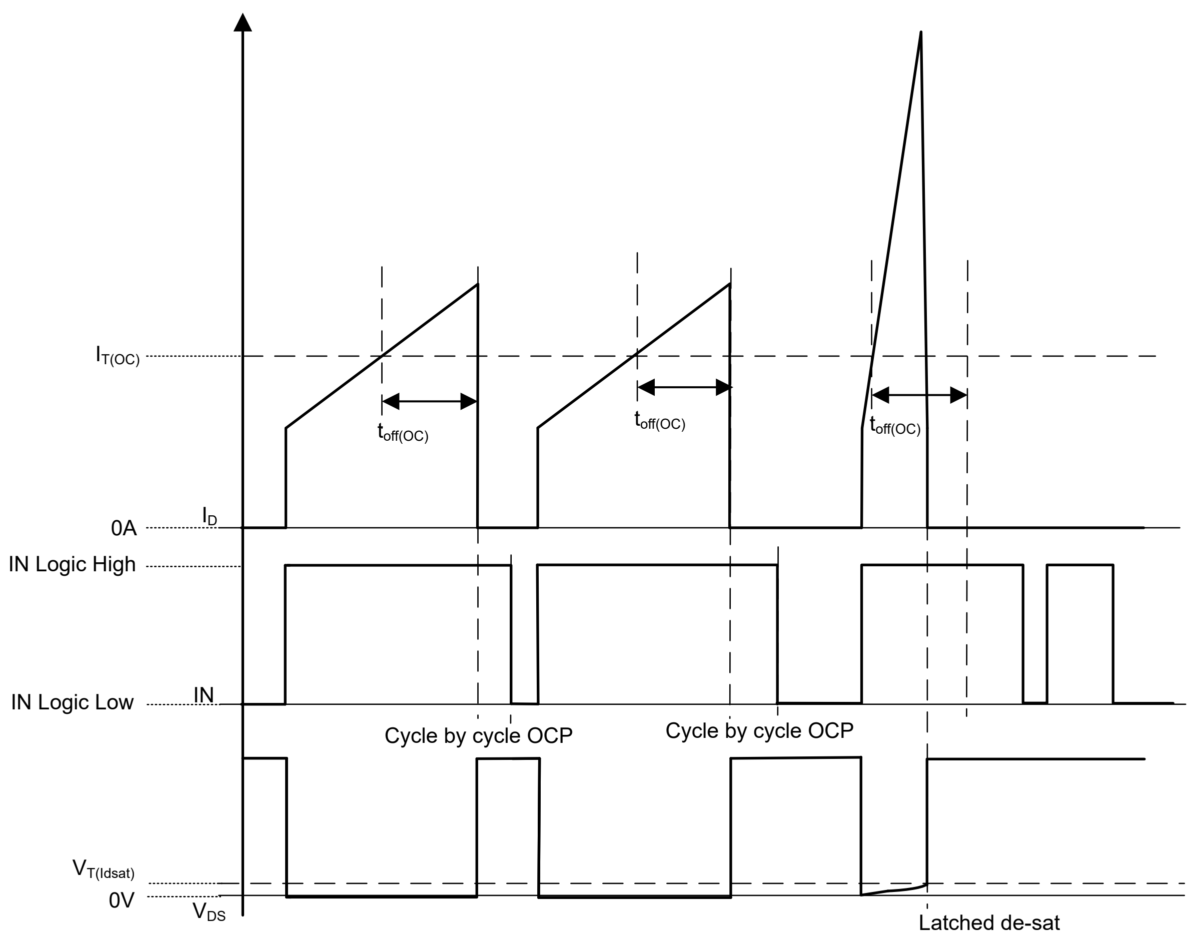


図 8-3. Overcurrent Detection vs Desaturation Detection

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8.3.4 Overtemperature Protection

The overtemperature protection holds off the GaN power FET if the LMG365xR070 temperature is above the overtemperature protection threshold. The overtemperature protection hysteresis avoids erratic thermal cycling. An overtemperature fault is reported on the $\overline{\text{FLT}}$/RDRV pin when the overtemperature protection is asserted. $\overline{\text{FLT}}$/RDRV de-asserts and the device automatically returns to normal operation after the device temperature fall below the negative-going trip point.

8.3.5 UVLO Protection

The LMG365xR070 supports a wide range of V_{DD} voltages. However, when the V_{DD} voltage is below V_{DD} UVLO threshold, the GaN device stops switching and is held off. The V_{DD} UVLO voltage hysteresis prevents on-off chatter near the UVLO voltage trip point. The $\overline{\text{FLT}}$/RDRV pin is pulled low as an indication of UVLO.

8.3.6 Fault Reporting

All faults are reported on the $\overline{\text{FLT}}$/RDRV pin, which serves as both an input and output pin.

The $\overline{\text{FLT}}$/RDRV is configured as an input only at the time of powerup to adjust the drive-strength, as described in *Drive Strength Adjustment*.

The $\overline{\text{FLT}}$/RDRV then used as an active low digital output, indicating the fault status thereafter. The pin is a push-pull 5V digital output which goes high when all faults have cleared, which means that there is additional quiescent current through R1 when the pin is forced high.

Depending on the input threshold levels for the external digital receiver connected to the fault pin, the 1.2V which is forced on this pin at power-up could be interpolated as either high or low. For this reason, it is recommended that the receiver has higher thresholds such as those common for CMOS-compatible inputs and not use TTL compatible inputs. If the input thresholds are lower, the 1.2V at power-up can be interpreted as a "high" and therefore showing that the device is not faulted when still powering up.

8.3.7 Auxiliary LDO (LMG3651R070 Only)

There is a 5V voltage regulator inside the part used to supply external loads, such as digital isolators for the high-side drive signal. The digital outputs of the part use this rail as their supply. No capacitor is required for stability, but transient response is poor if no external capacitor is provided. If the application uses this rail to supply external circuits, TI recommends to have a capacitor of at least 0.1µF for improved transient response. A larger capacitor can be used for further transient response improvement. The decoupling capacitor used here must be a low-ESR ceramic type. Capacitances above 0.47µF will slow down the start-up time of the LMG365xR070 due to the ramp-up time of the 5V rail.

8.3.8 Zero-Voltage Detection (ZVD) (LMG3656R070 Only)

The zero-voltage switching (ZVS) converters are widely used to improve the power converter's efficiency. However, in those soft-switching topologies like LLC and triangular current mode (TCM) totem pole PFC, the device can lose ZVS depending on the load condition, inductor, magnetic parameters and control techniques, which affects the system efficiency. To insure ZVS, certain design margins or additional circuits are needed which sacrifices the converter performance and adds components.

To simplify the system design for soft-switching converters,LMG3656R070 part integrates a zero-voltage detection (ZVD) circuit that provides a digital feedback signal to indicate if the device has achieved ZVS in the current switching cycle. The circuit diagram is shown in 図 8-4. When the IN pin signal goes high, the logic circuit checks if the device V_{DS} has reached below 0V to determine whether the device has achieved zero voltage switching in this switching cycle. Once a ZVS is identified, a pulse-output with a width of T_{WD_ZVD} will be sent out from the ZVD pin after a delay time of T_{DL_ZVD} as indicated in 図 7-3. Note a certain third quadrant conduction time is required to allow the device detecting a zero-voltage switching, and T_{3rd_ZVD} is a function of the gate driver strength.

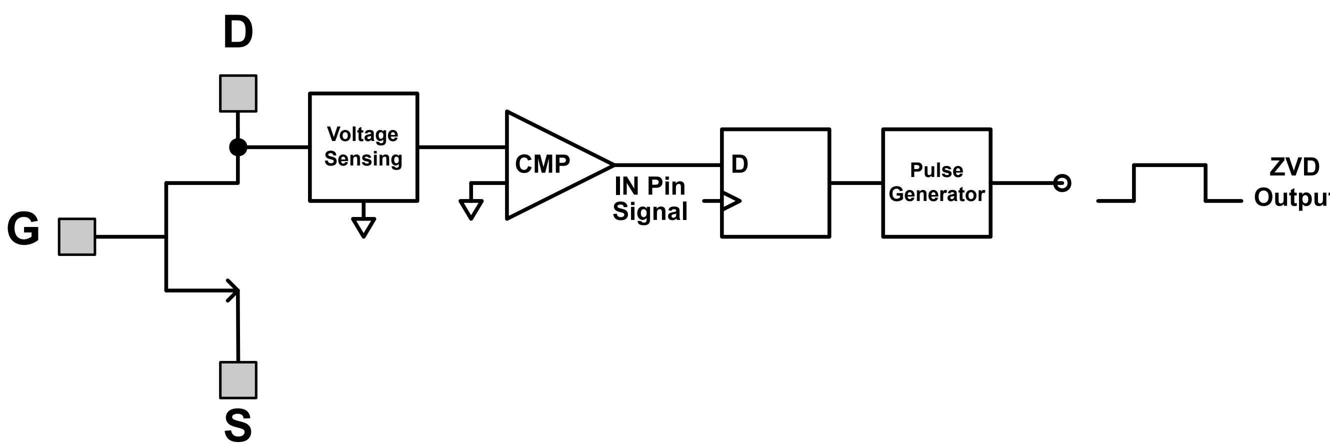

図 8-4. Circuit Diagram for Zero-Voltage Detection Circuit Block Diagram

The timings of the ZVD output corresponding to a continuous conduction mode Buck converter is shown in 図 8-5, and the purpose is to demonstrate how ZVD function works in both hard-switching and soft-switching conditions. The load current going out of the switch node is defined as positive. In CCM buck operation, the high-side the hard-switching device while the low-side device can achieve zero-voltage switching with a proper dead-time settings. In the first switching cycle when low-side GaN IN pin rises, the switch-node voltage V_{DS} has dropped below zero and stays in third quadrant conduction for a period of T_1. Since this third quadrant conduction time T_1 is larger than the detection time T_{3rd_ZVD} specified in electrical characteristic table, a zero-voltage switching is identified and the ZVD pin outputs a pulse signal to indicate that, and the pulse width of the ZVD pulse is also defined in the electrical characteristic table as T_{WD}. In the second switching cycle, the device is turned on earlier, and the third quadrant conduction time T_2 is less than T_{3rd_ZVD}. In this case, the ZVD signal stays low though the device has achieved ZVS. In the third switching cycle, the IN pin signal is advanced even earlier, and the device is in partial hard-switching. Accordingly, the ZVD output stays low in this case. Note the high side ZVD output stays low in this CCM buck operation as it always has hard-switching.

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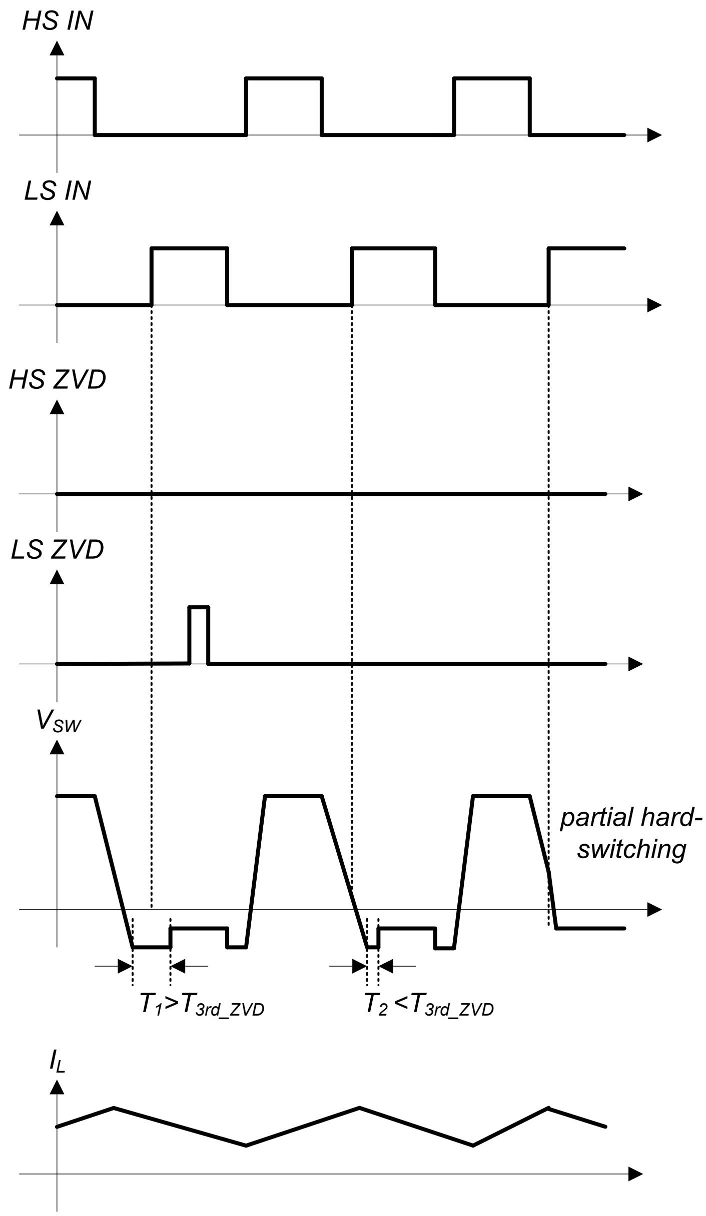

図 8-5. ZVD Function in a CCM Buck Converter

The ZVD function can facilitate the control in soft-switching topology, to illustrate it, the ZVD waveforms in a TCM totem pole PFC is shown in 図 8-6. In this diagram, the positive cycle is considered with V_{IN} > 0.5 V_{OUT}, and the load current going into the switch node is defined as positive. In the first switching cycle, the load current builds enough negative current, and the low-side device achieves ZVS with a clear third quadrant conduction time beyond T_{3rd_DET}. Therefore, the ZVD outputs a pulse signal and provide the ZVS information back. The ZVD pulses are missing in the next two switching cycles because the third quadrant conduction time becomes shorter in second cycle and the device actual loses ZVS in the third cycle.

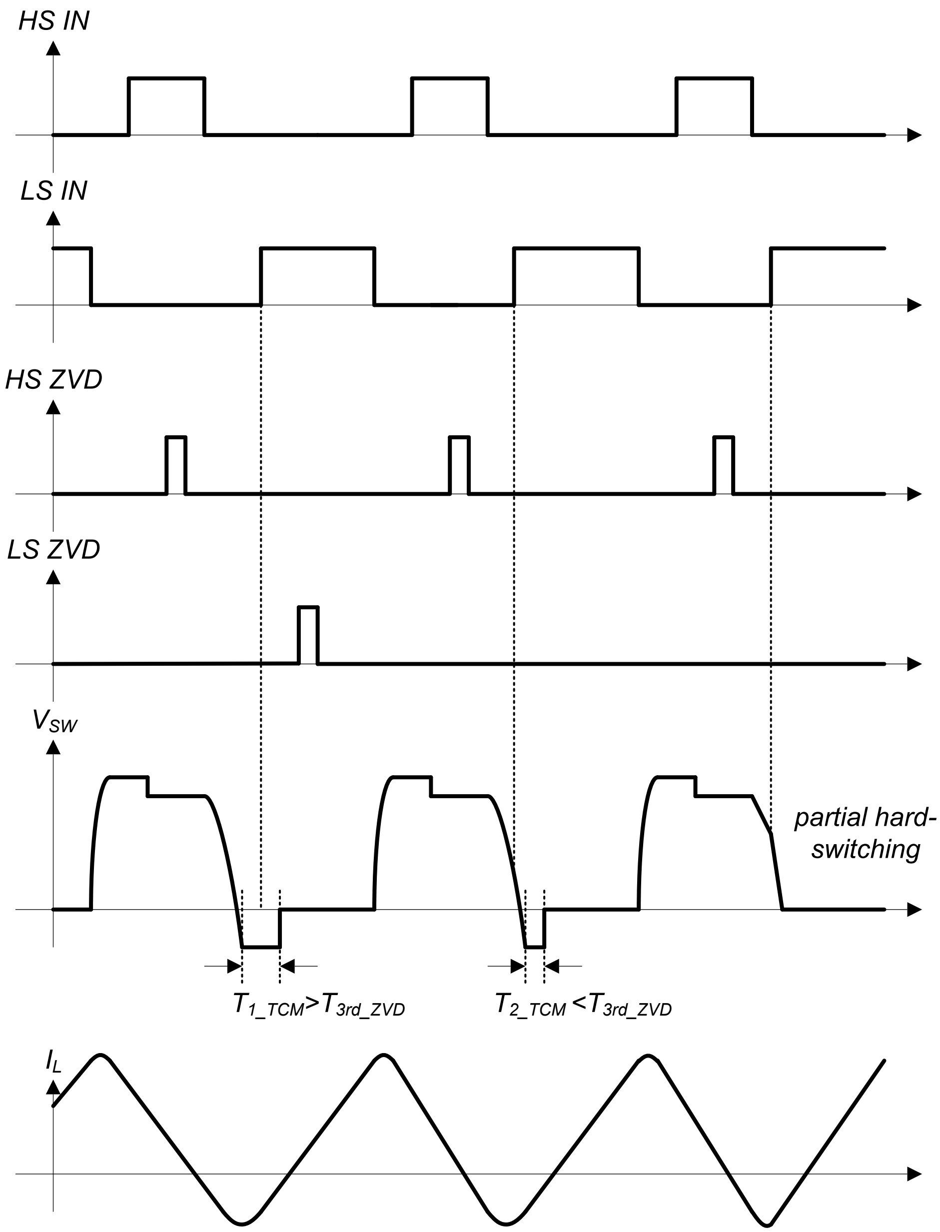

図 8-6. ZVD Function in a TCM TP PFC Converter

8.3.9 Zero-Current Detection (ZCD) (LMG3657R070 Only)

GaN FET is usually used for high frequency soft-switching and the detection of FET current zero-crossing is needed for system control. LMG3657R070 integrates a zero current detection (ZCD) circuit that provides a digital feedback signal to indicate the when the drain-to-source current is positive. When the IN pin signal goes high, the ZCD circuit includes a blanking time t_{ZCD_Blank}, to prevent nuisance ZCD triggering during the turn-on transient. Following the blanking period, the ZCD circuit monitors the drain-to-source current. If the current is negative, a pulse-output with a width of t_{WD_ZVD} is set on the ZCD pin after detecting the zero-crossing point, with a delay time of t_{zc_Det}. If the current is positive, the pulse output is set on the ZCD pin immediately, as indicated in the timing diagrams below.

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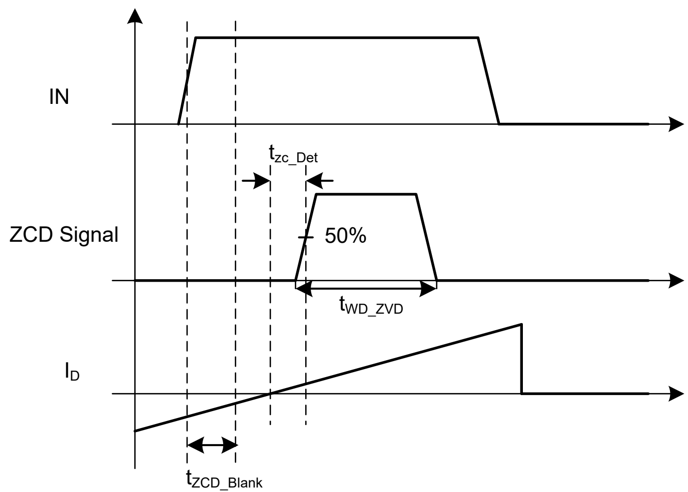

図 8-7. ZCD Timing Diagram When FET Turns ON Into Negative Current

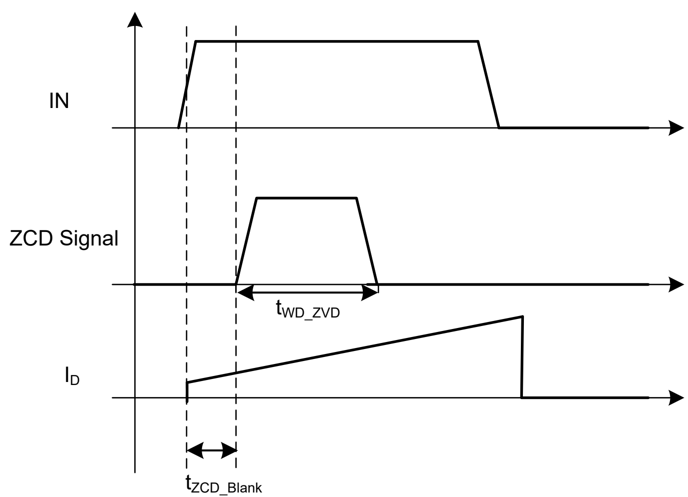

図 8-8. ZCD Timing Diagram When FET Turns ON Into Positive Current

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the Recommended Operating Conditions.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMG365xR070 is a power IC targeting hard-switching and soft-switching applications operating up to 480V bus voltages. GaN devices offer zero reverse-recovery charge enabling high-frequency, hard-switching in applications like the totem-pole PFC. Low Q_{OSS} of GaN devices also benefits soft-switching converters, such as the LLC and phase-shifted full-bridge configurations. As half-bridge configurations are the foundation of the two mentioned applications and many others, this section describes how to use the LMG365xR070 in a half-bridge configuration.

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9.2 Typical Application

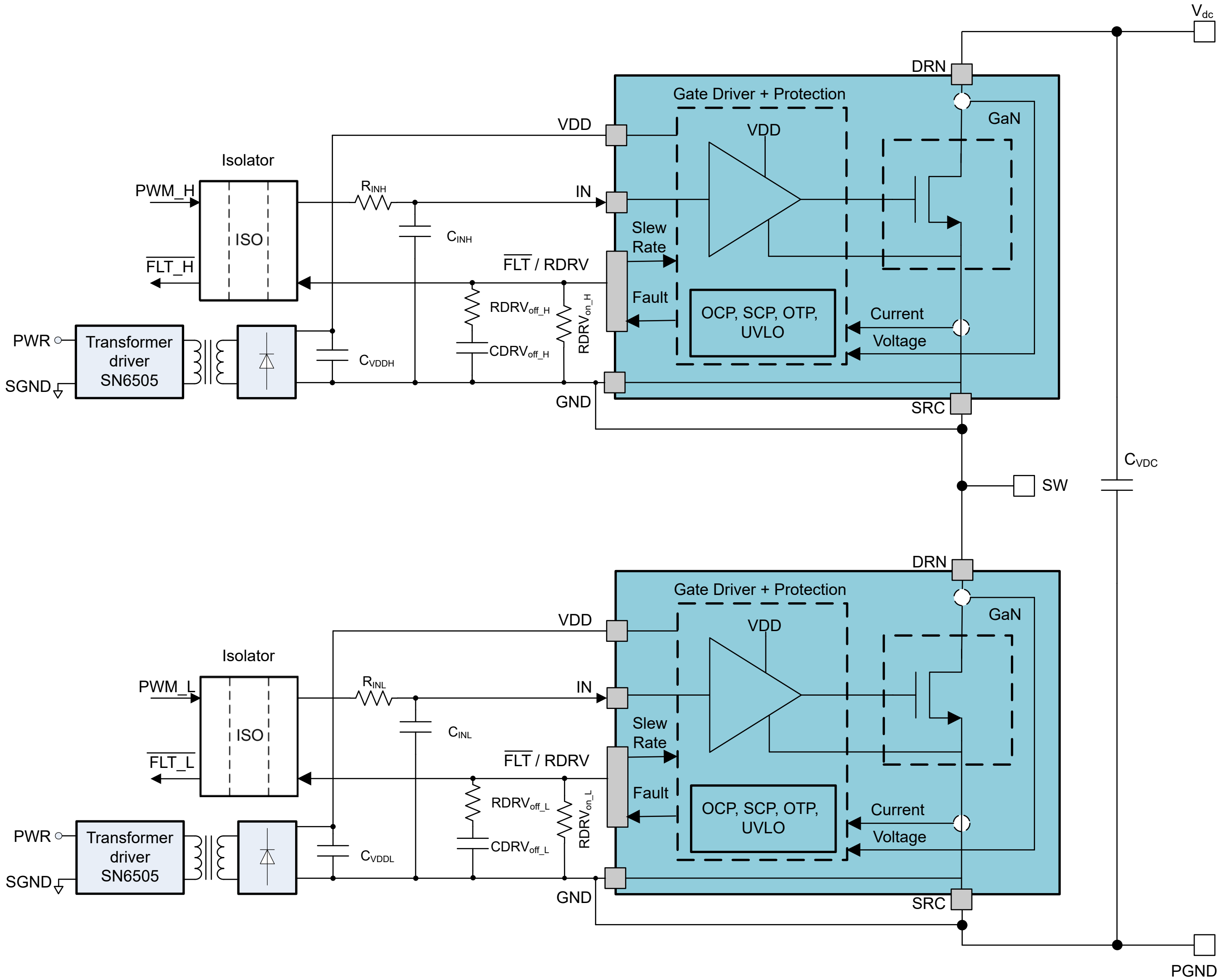

図 9-1. LMG3650R070 Typical Half-Bridge Application With Isolated Power Supply

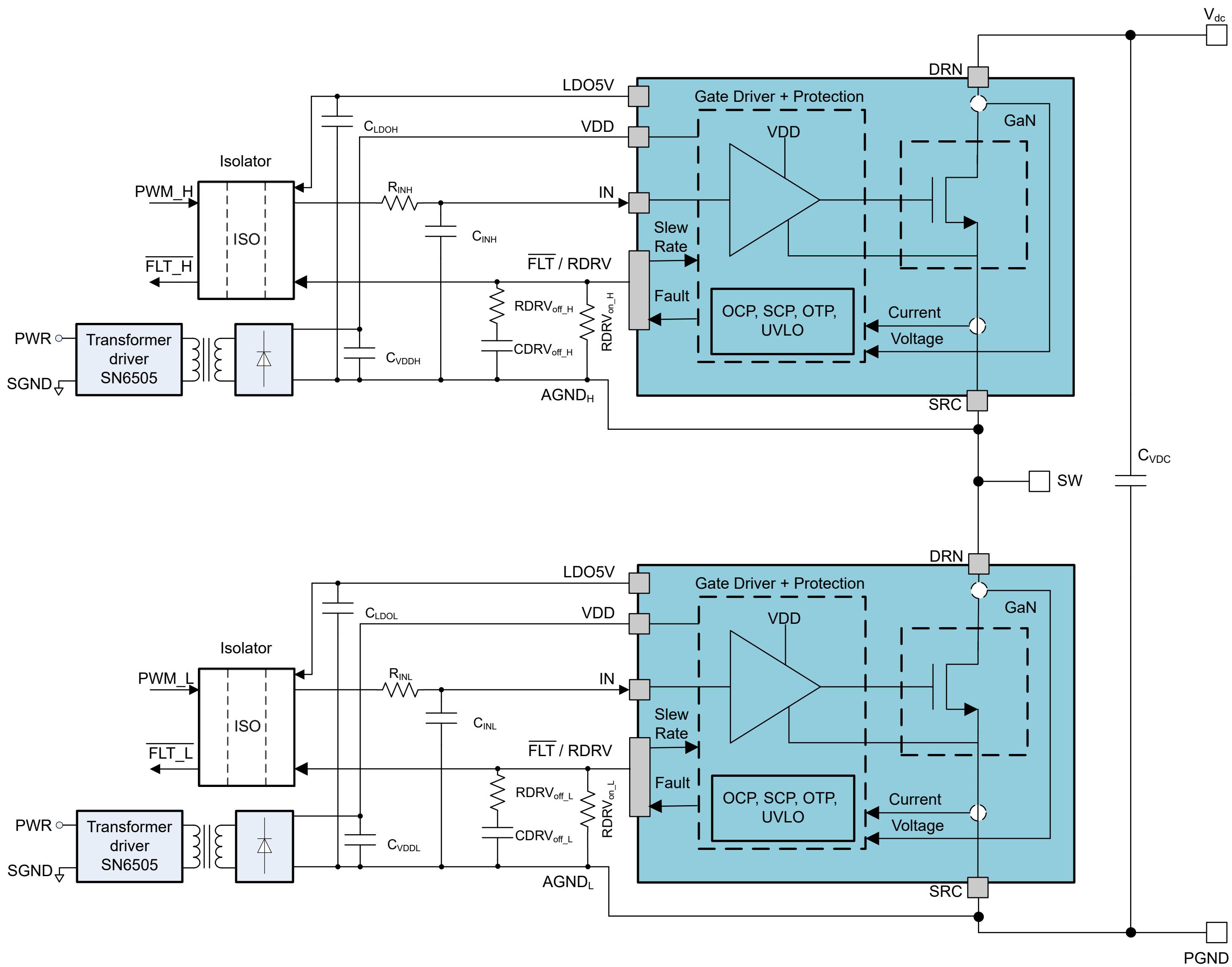

図 9-2. LMG3651R070 Typical Half-Bridge Application With Isolated Power Supply

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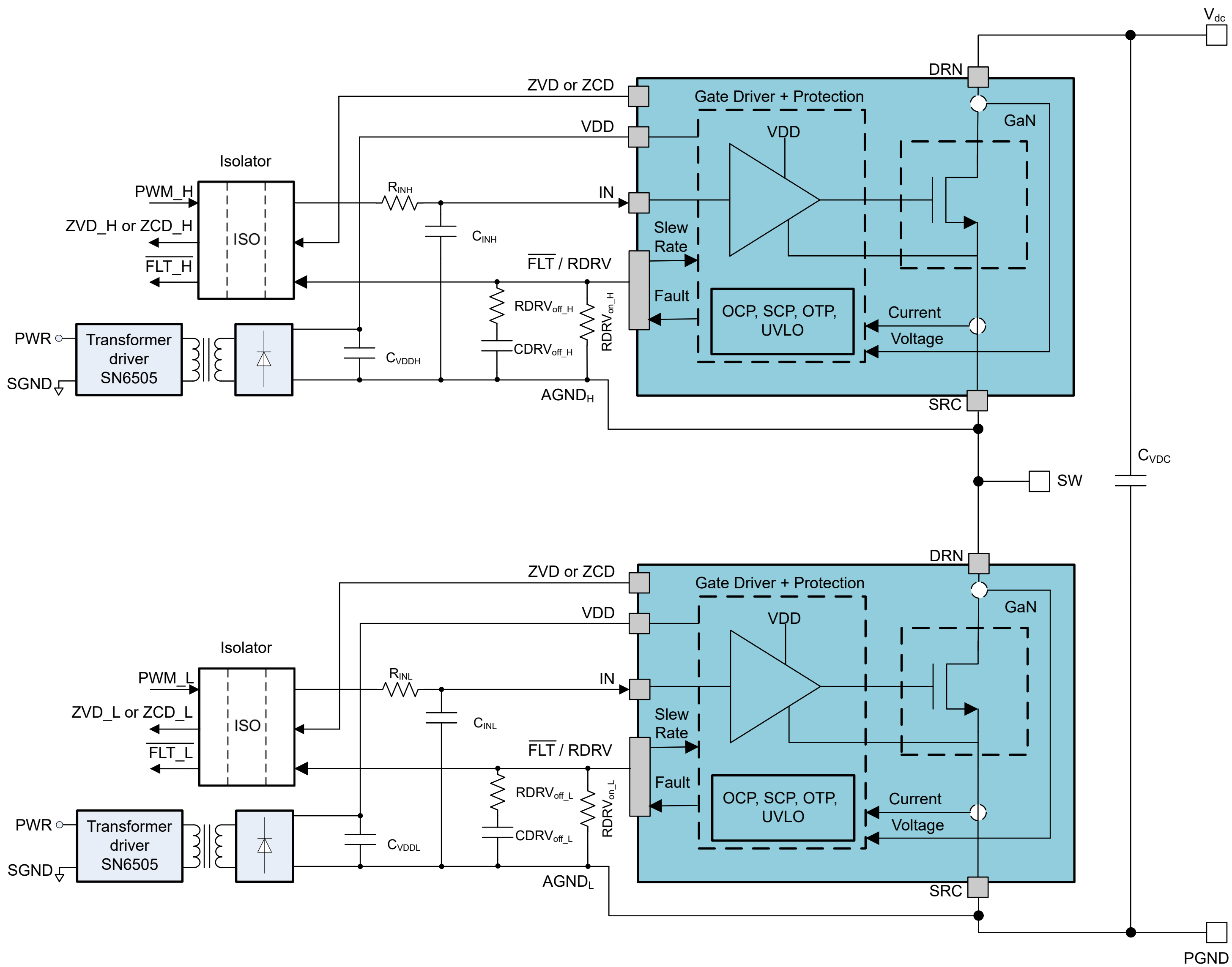

図 9-3. LMG3656R070 or LMG3657R070 Typical Half-Bridge Application With Isolated Power Supply

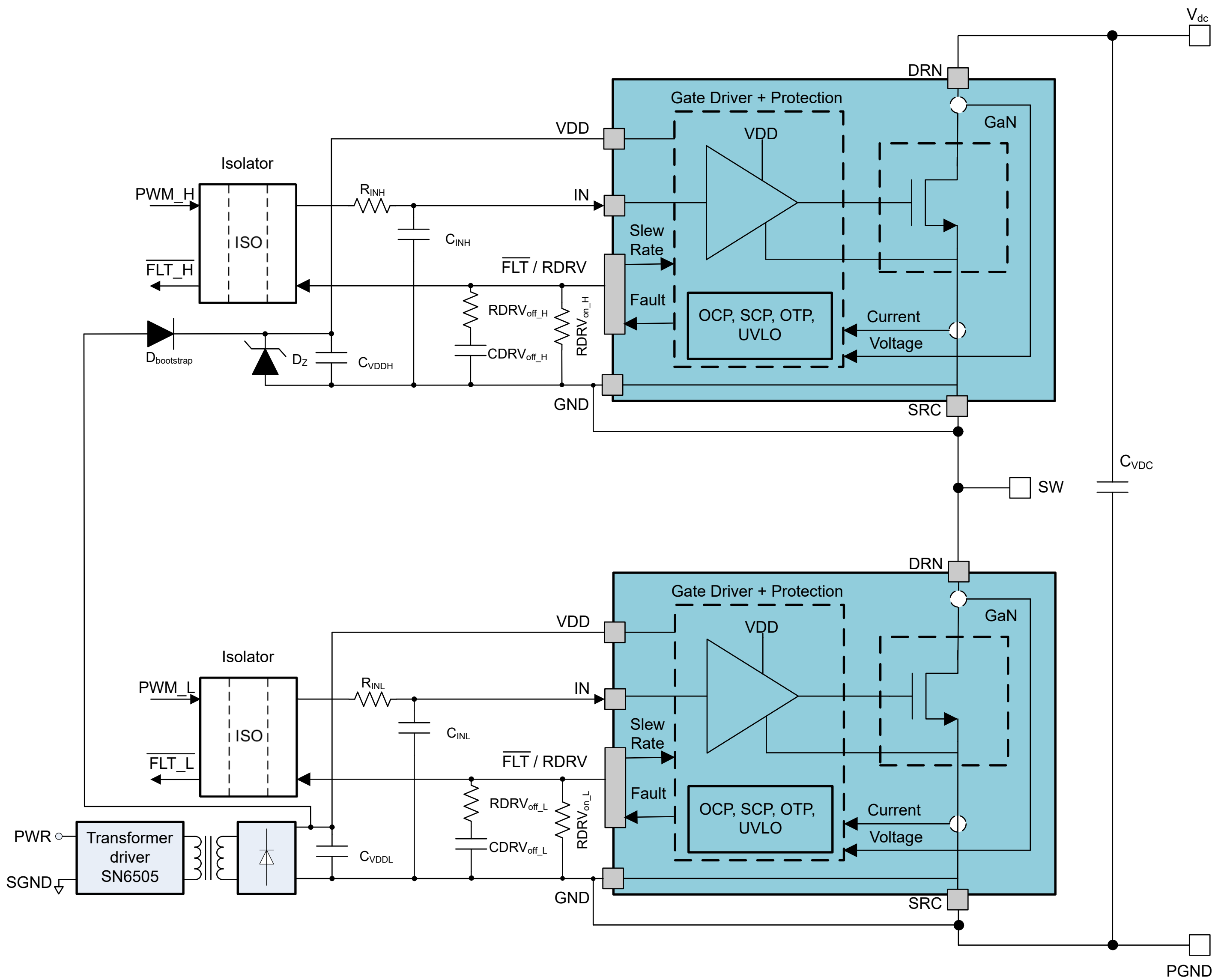

図 9-4. LMG3650R070 Typical Half-Bridge Application With Bootstrap

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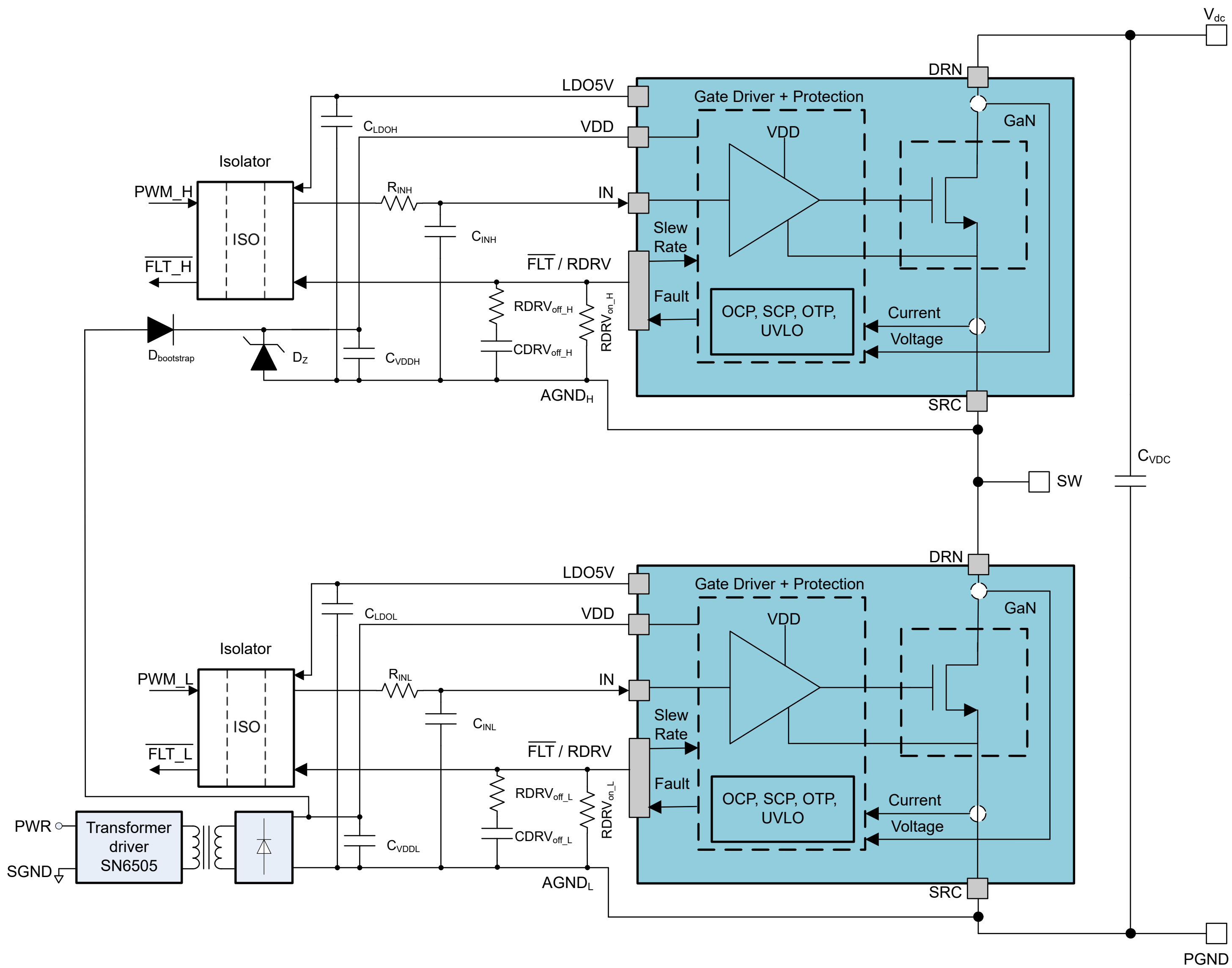

図 9-5. LMG3651R070 Typical Half-Bridge Application With Bootstrap

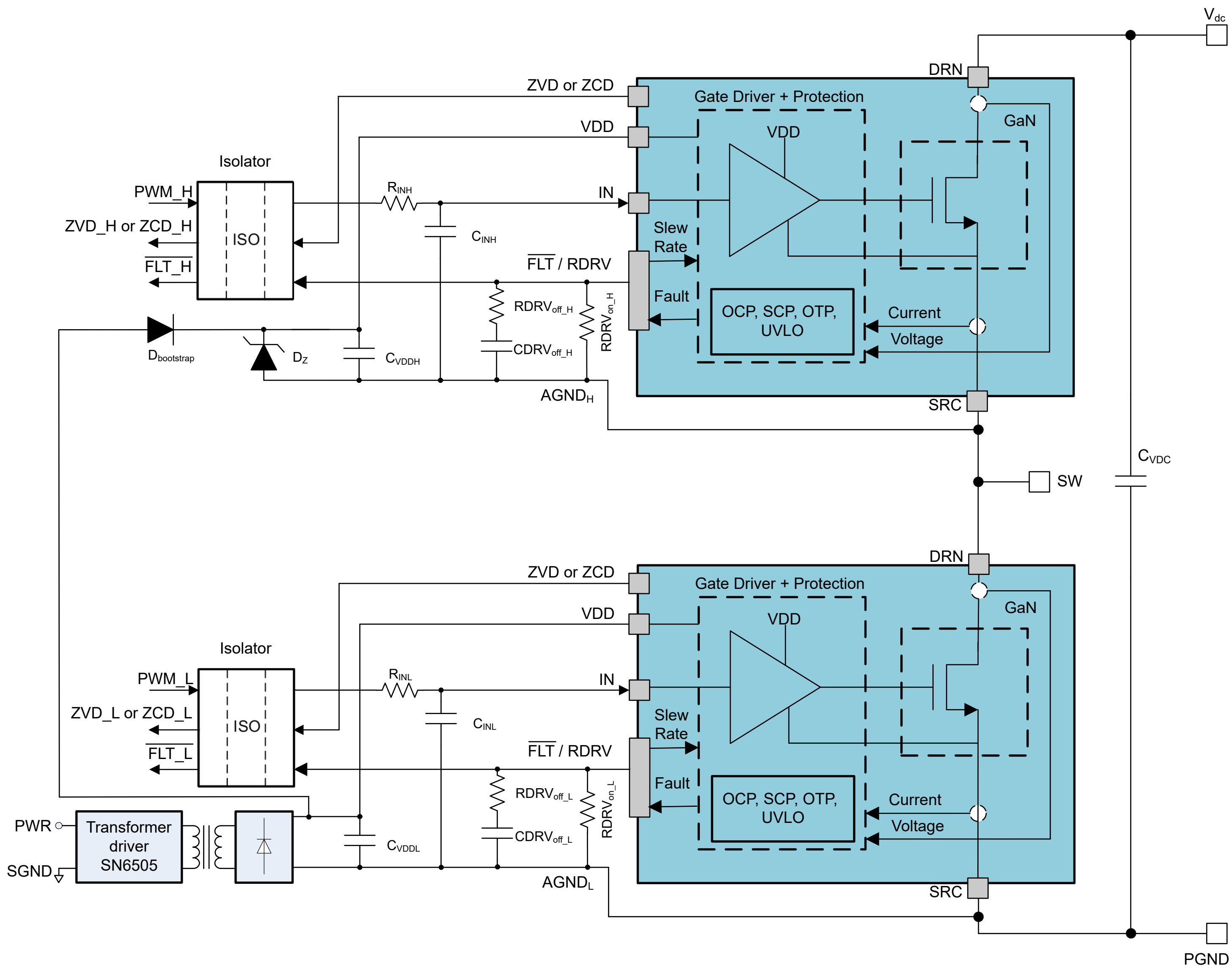

図 9-6. LMG3656R070 or LMG3657R070 Typical Half-Bridge Application With Bootstrap

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9.2.1 Design Requirements

This design example is for a hard-switched boost converter which is representative of PFC applications. Design Parameters shows the system parameters for this design.

表 9-1. Design Parameters

PARAMETER	VALUE
Input voltage	200VDC
Output voltage	400VDC
Input (inductor) current	20A
Switching frequency	100kHz

9.2.2 Detailed Design Procedure

In high-voltage power converters, circuit design and PCB layout are essential for high-performance power converters. As designing a power converter is out of the scope of this document, this data sheet describes how to build well-behaved half-bridge configurations with the LMG365xR070.

9.2.2.1 Slew Rate Selection

The slew rate of LMG365xR070 can be adjusted between approximately 10 V/ns and 100V/ns by connecting drive strength adjustment circuit. Refer to Drive Strength Adjustment for the details.

The slew rate affects GaN device performance in terms of:

- Switching loss
- Voltage overshoot
- Noise coupling
- EMI emission

Generally, high slew rates provide low switching loss, but high slew rates can also create higher voltage overshoot, noise coupling, and EMI emissions. Following the design recommendations in this data sheet helps mitigate the challenges caused by a high slew rate. The LMG365xR070 offers circuit designers the flexibility to select the proper slew rate for the best performance of their applications.

9.2.2.2 Signal Level-Shifting

In half-bridges, high-voltage level shifters or digital isolators must be used to provide isolation for signal paths between the high-side device and control circuit. Using an isolator is optional for the low-side device. However, using and isolator equalizes the propagation delays between the high-side and low-side signal paths, and provides the ability to use different grounds for the GaN device and the controller. If an isolator is not used on the low-side device, the control ground and the power ground must be connected at the device and nowhere else on the board. For more information, see *Layout Guidelines*. With fast-switching devices, common ground inductance can easily cause noise issues without the use of an isolator.

Choosing a digital isolator for level-shifting is important for improvement of noise immunity. As GaN device can easily create high dv/dt, > 50V/ns, in hard-switching applications, TI highly recommends to use isolators with high common-mode transient immunity (CMTI) and low barrier capacitance. Isolators with low CMTI can easily generate false signals, which could cause shoot-through. The barrier capacitance is part of the isolation capacitance between the signal ground and power ground, which is in direct proportion to the common mode current and EMI emission generated during the switching. Additionally, TI strongly encourages to select isolators which are not edge-triggered. In an edge-triggered isolator, a high dv/dt event can cause the isolator to flip states and cause circuit malfunction.

Generally, ON/OFF keyed isolators with default output low are preferred. Default low state ensures the system will not shoot-through when starting up or recovering from fault events. As a high CMTI event would only cause a very short (a few nanoseconds) false pulse, TI recommends a low pass filter, like 300Ω and 22pF R-C filter, to be placed at the driver input to filter out these false pulses.

9.3 Power Supply Recommendations

The LMG365xR070 only requires an unregulated VDD power supply from 9V to 26V. The low-side supply can be obtained from the local controller supply. The supply of the high-side device must come from an isolated supply or a bootstrap supply.

9.3.1 Using an Isolated Power Supply

Using an isolated power supply to power the high-side device has the advantage that it works regardless of continued power-stage switching or duty cycle. Using an isolated power supply can also power the high-side device before power-stage switching begins for a smooth start-up.

The isolated supply can be obtained with a push-pull converter, a flyback converter, a FlyBuck™ converter, or an isolated power module. When using an unregulated supply, the input of LMG365xR070 must not exceed the maximum supply voltage. A 26V TVS diode can be used to clamp the VDD voltage of LMG365xR070 for additional protection. Minimizing the inter-winding capacitance of the isolated power supply or transformer is necessary to reduce switching loss in hard-switched applications. Furthermore, capacitance across the isolated bias supply inject high currents into the signal-ground of the LMG365xR070 and can cause problematic ground-bounce transients. A common-mode choke can alleviate most of these issues.

9.3.2 Using a Bootstrap Diode

In half-bridge configuration, a floating supply is necessary for the high-side device. To obtain the best performance of LMG365xR070, TI highly recommends *Using an Isolated Power Supply*. A bootstrap supply can be used with the recommendations of this section.

9.3.2.1 Diode Selection

The LMG365xR070 offers no reverse-recovery charge and very limited output charge. Hard-switching circuits using the LMG365xR070 also exhibit high voltage slew rates. A compatible bootstrap diode must not introduce high output charge and reverse-recovery charge.

A silicon carbide diode, like the GB01SLT06-214, can be used to avoid reverse-recovery effects. The SiC diode has an output charge of 3nC. Although there is additional loss from its output charge, it does not dominate the losses of the switching stage.

9.3.2.2 Managing the Bootstrap Voltage

In a synchronous buck or other converter where the low-side switch occasionally operates in third-quadrant, the bootstrap supply charges through a path that includes the third-quadrant voltage drop of the low-side LMG365xR070 during the dead time as shown in Charging Path for Bootstrap Diode. This third-quadrant drop can be large, which can overcharge the bootstrap supply in certain conditions. The V_{DD} supply of LMG365xR070 must be kept below 28V.

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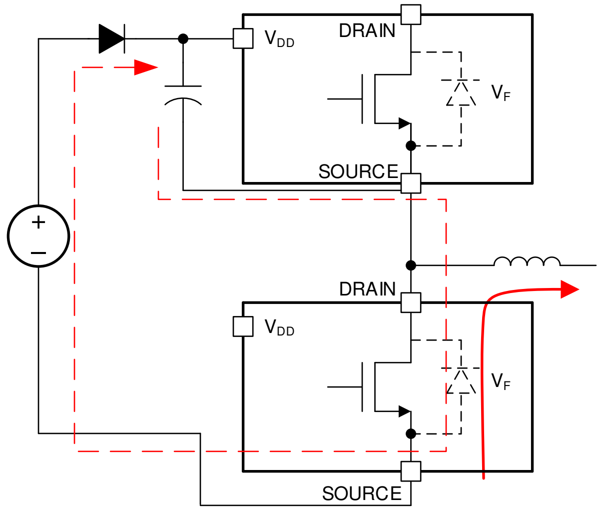

図 9-7. Charging Path for Bootstrap Diode

As shown in Suggested Bootstrap Regulation Circuit, the recommended bootstrap supply includes a bootstrap diode, a series resistor, and a 26V TVS or Zener diode in parallel with the V_{DD} bypass capacitor to prevent damaging the high-side LMG365xR070. The series resistor limits the charging current at start-up and when the low-side device is operating in third-quadrant mode. This resistor must be selected to allow sufficient current to power the LMG365xR070 at the desired operating frequency. At 100kHz operation, TI recommends a value of approximately 2Ω. At higher frequencies, this resistor value must be reduced or the resistor omitted entirely to ensure sufficient supply current.

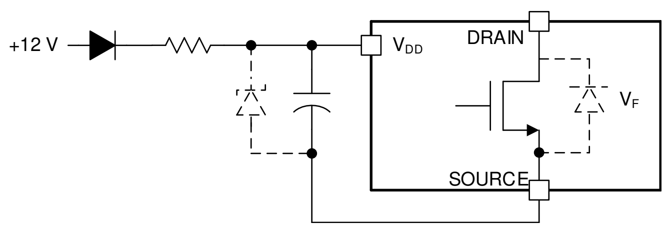

図 9-8. Suggested Bootstrap Regulation Circuit

9.4 Layout

9.4.1 Layout Guidelines

The layout of the LMG365xR070 is critical to its performance and functionality. Because the half-bridge configuration is typically used with these GaN devices, layout recommendations are considered with this configuration. A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance. Critical layout guidelines are summarized below, and more details are further elaborated in the following sections.

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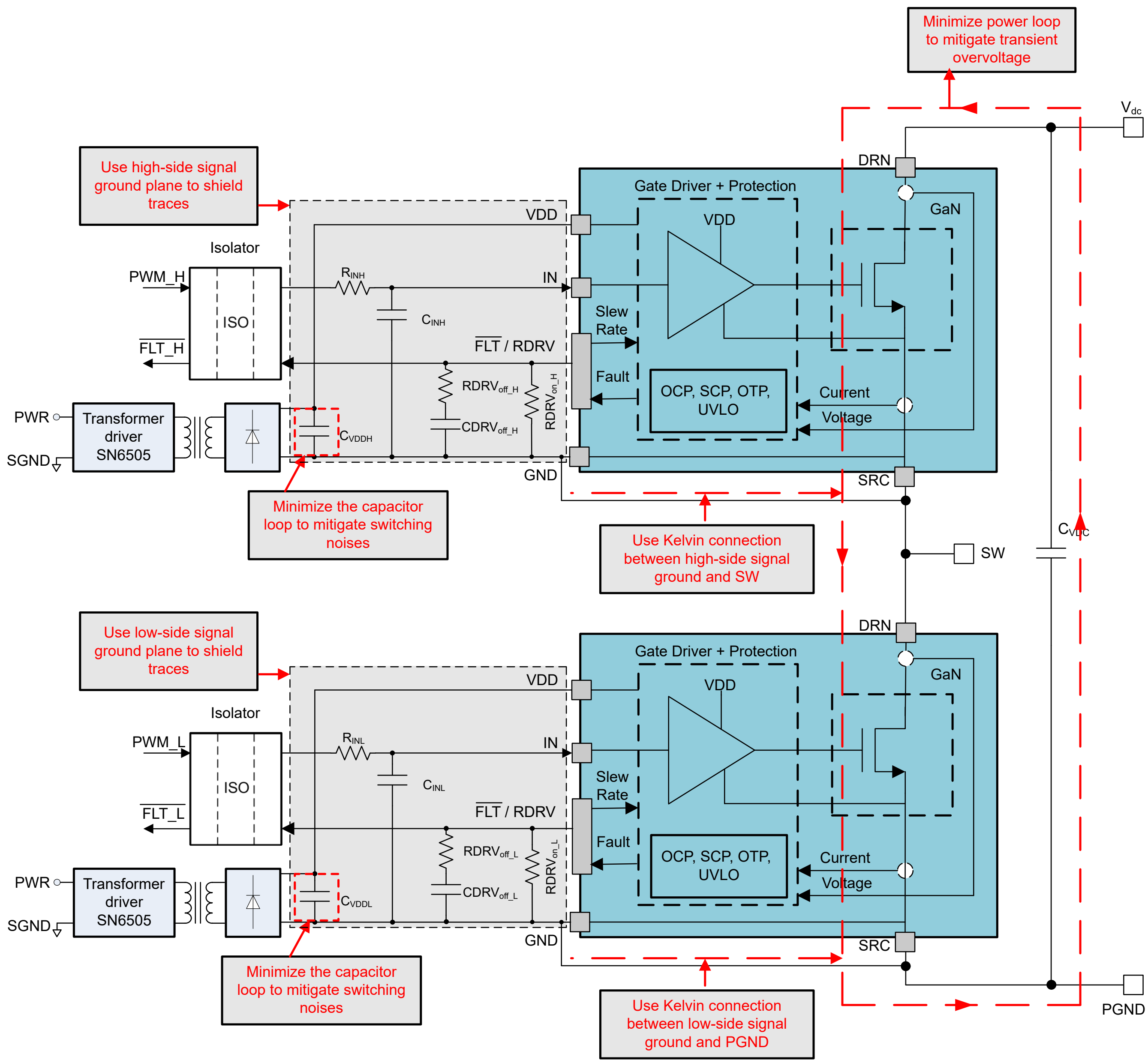

図 9-9. LMG3650R070 Typical Schematic With Layout Considerations

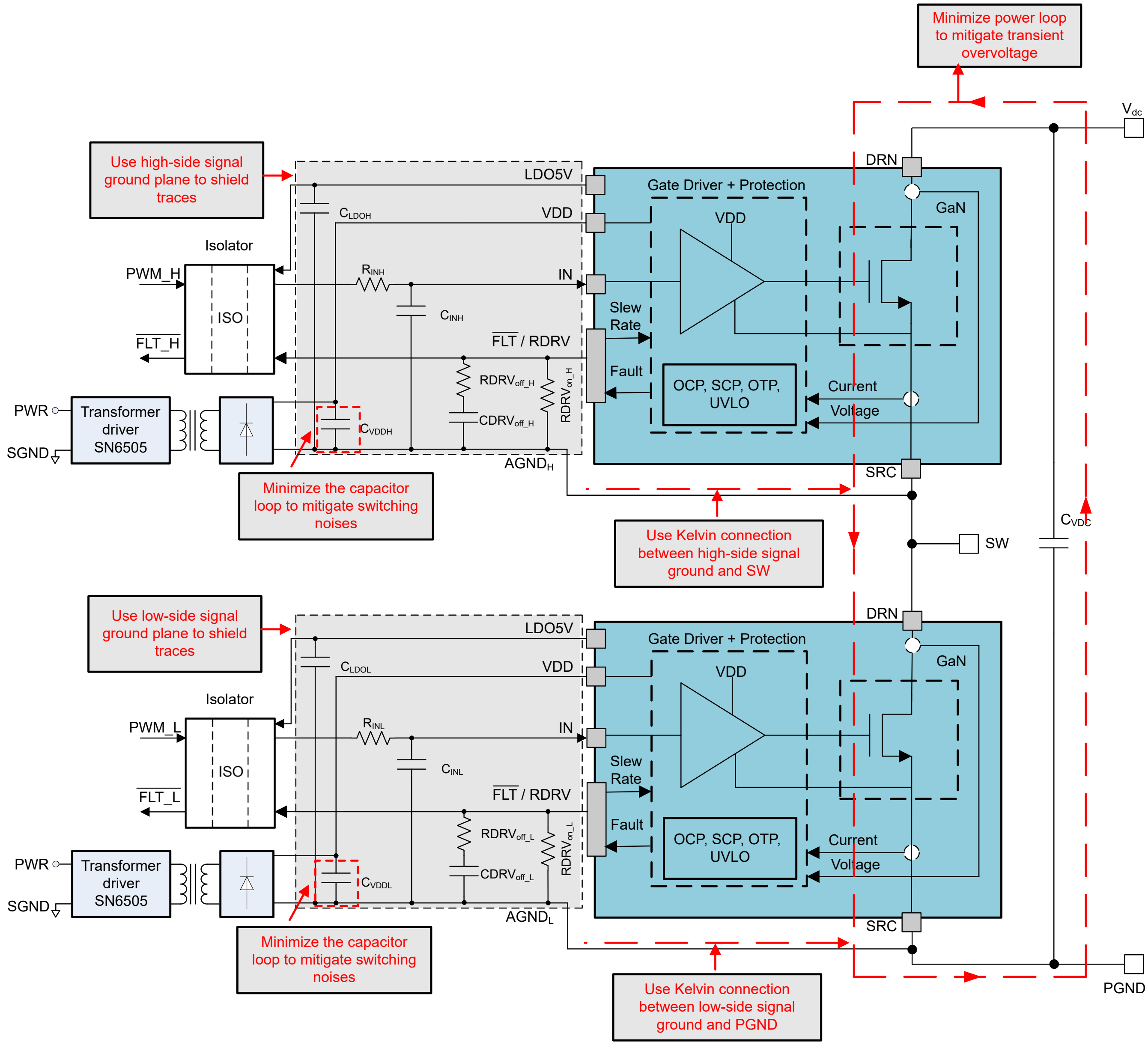

図 9-10. LMG3651R070 Typical Schematic With Layout Considerations

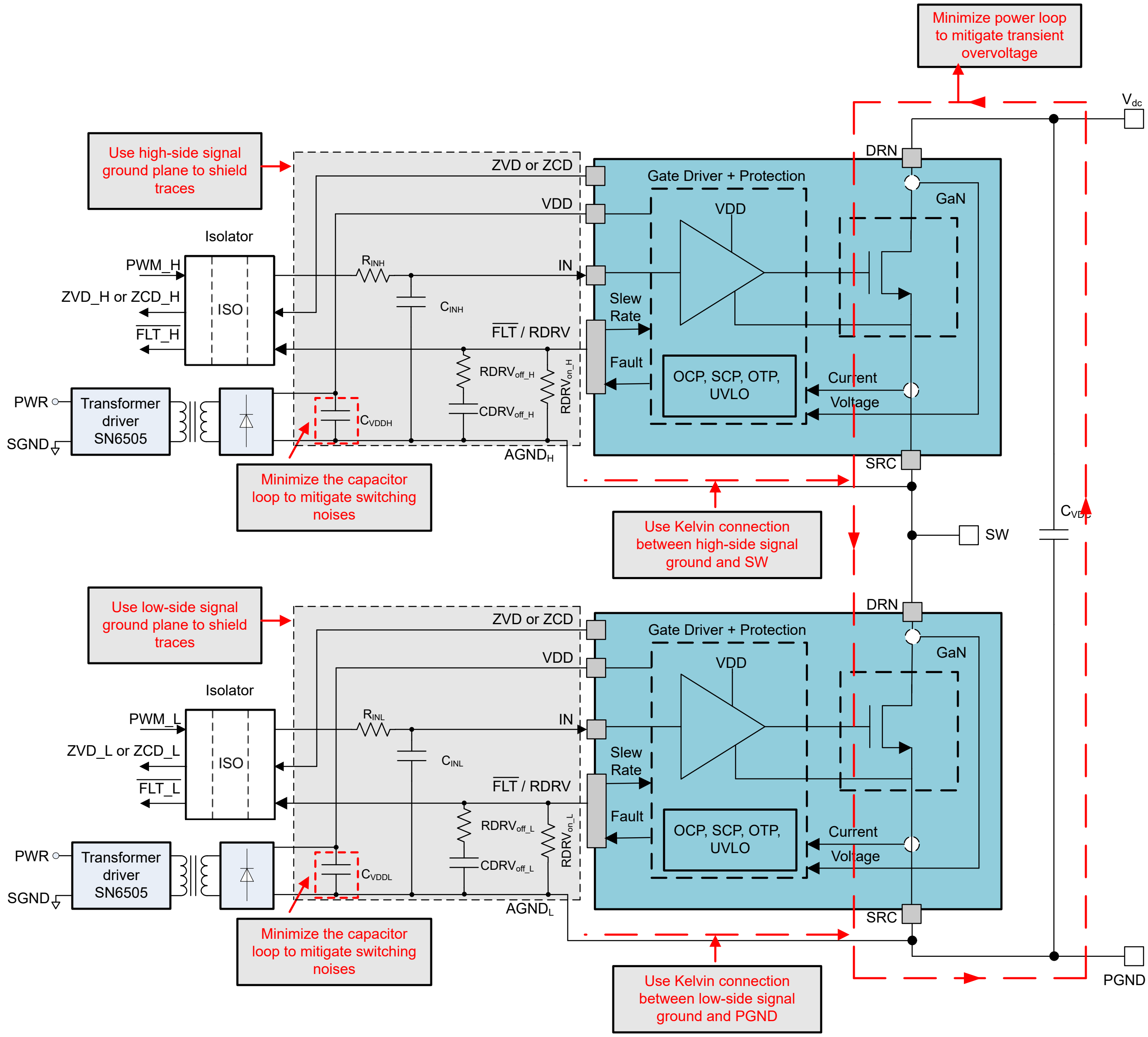

図 9-11. LMG3656R070 or LMG3657R070 Typical Schematic With Layout Considerations

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.3 Trademarks

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10.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

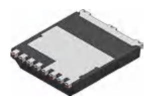
11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

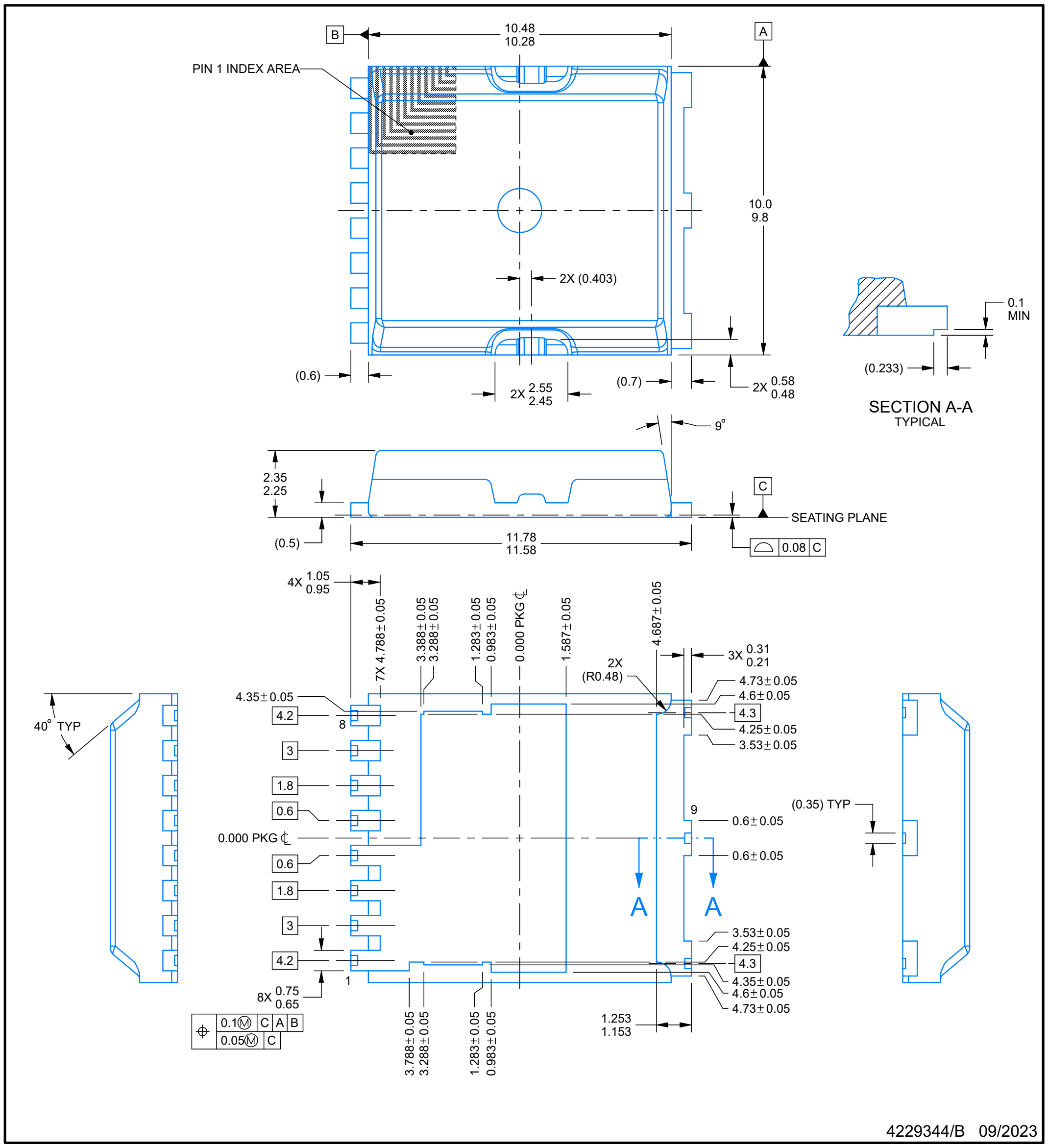


PACKAGE OUTLINE

KLA0009A

TOLL - 2.35 mm max height

TO LEADLESS



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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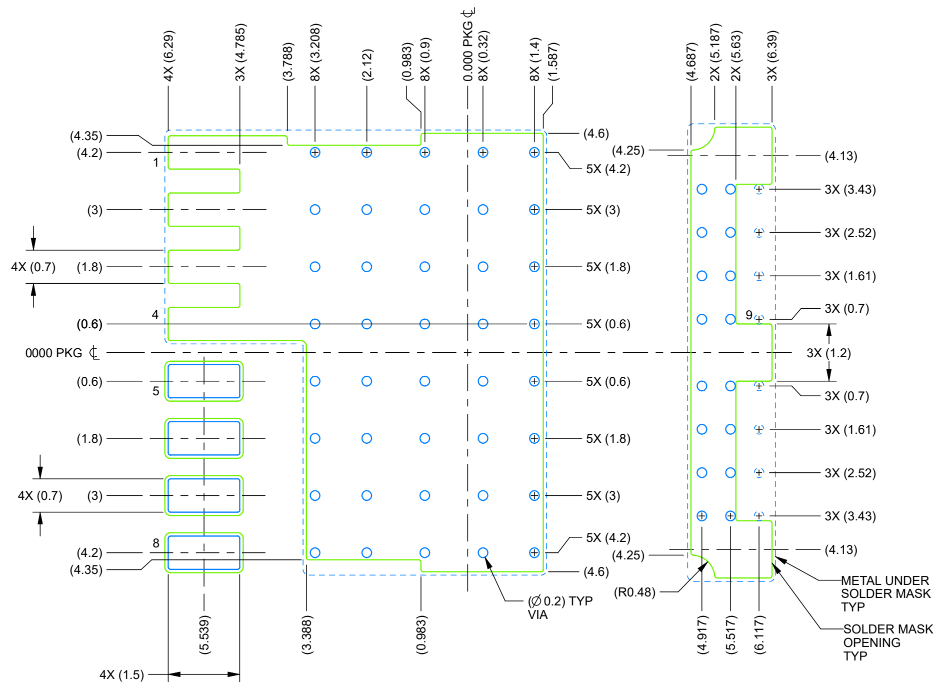
EXAMPLE BOARD LAYOUT

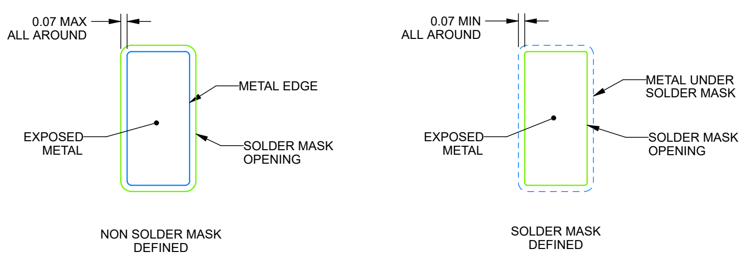
KLA0009A

TOLL - 2.35 mm max height

TO LEADLESS



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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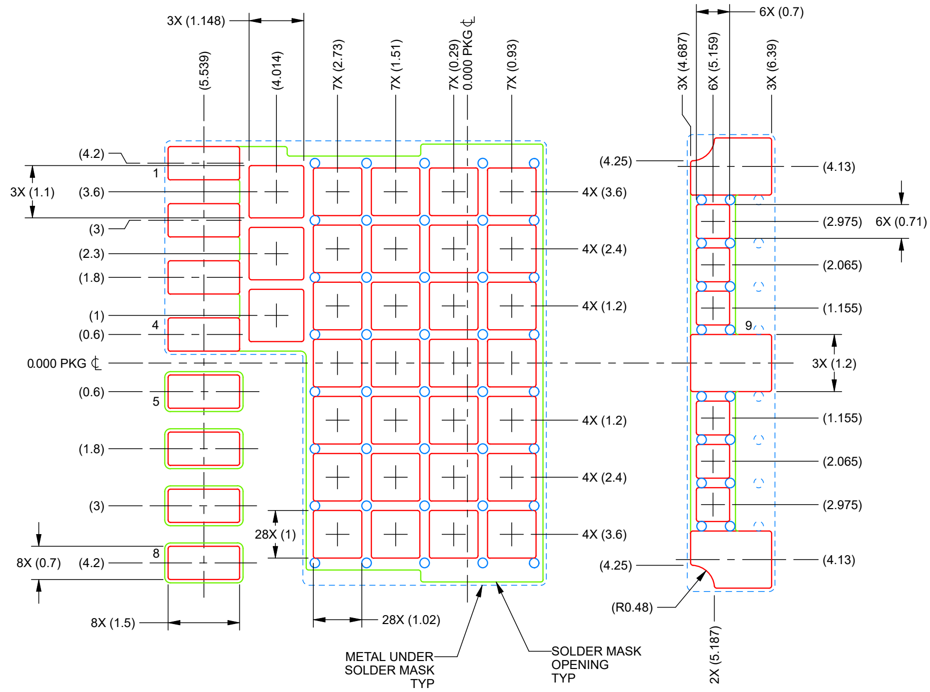
EXAMPLE STENCIL DESIGN

KLA0009A **TOLL - 2.35 mm max height**

TO LEADLESS



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD CONNECTED TO PINS 1 - 4: 67%
PAD 9: 87%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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ADVANCE INFORMATION

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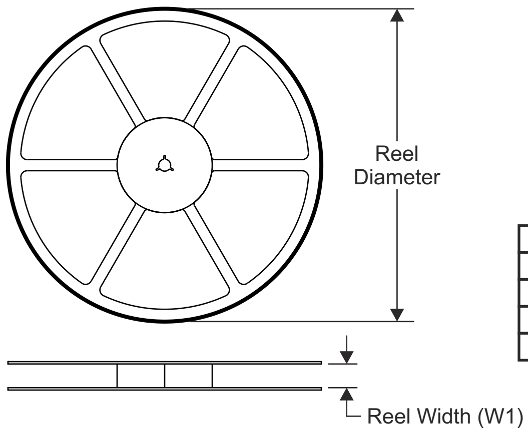
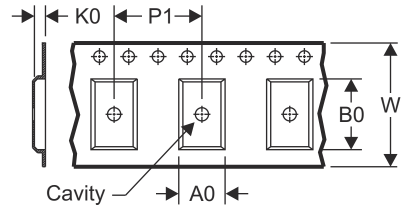
12.1 Tape and Reel Information

REEL DIMENSIONS

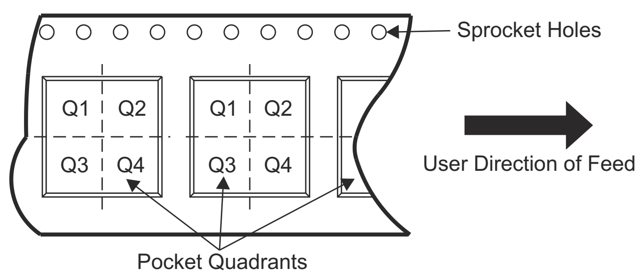


TAPE DIMENSIONS



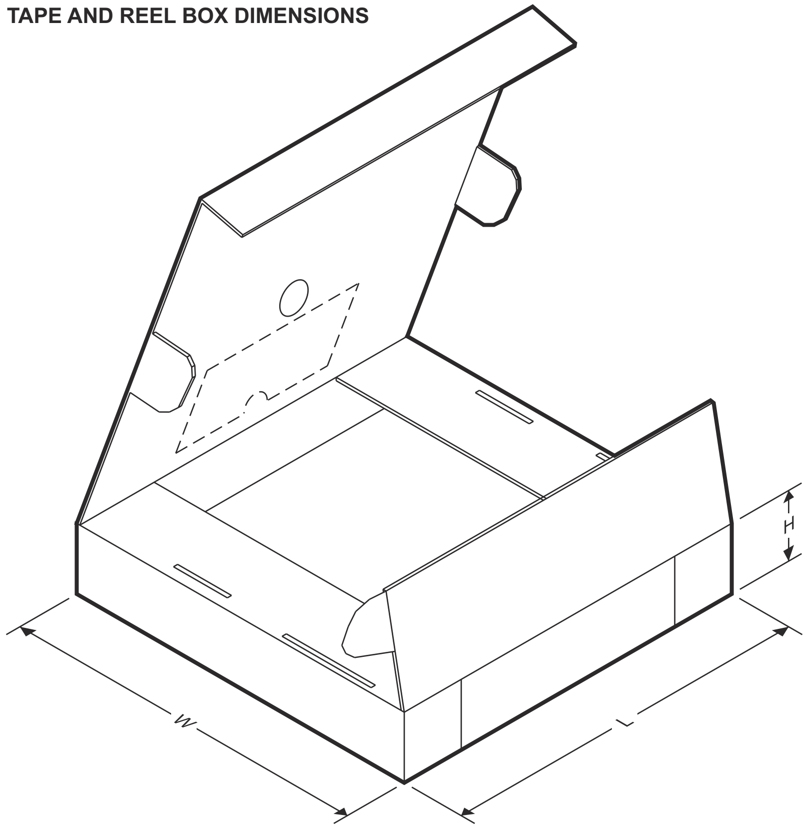
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XLMG3650R070KLAT	TO	KLA	9	2000	330.0	24.4	10.20	11.98	2.6	12.0	21.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XLMG3650R070KLAT	TO	KLA	9	2000	356.0	356.0	45.0

ADVANCE INFORMATION

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