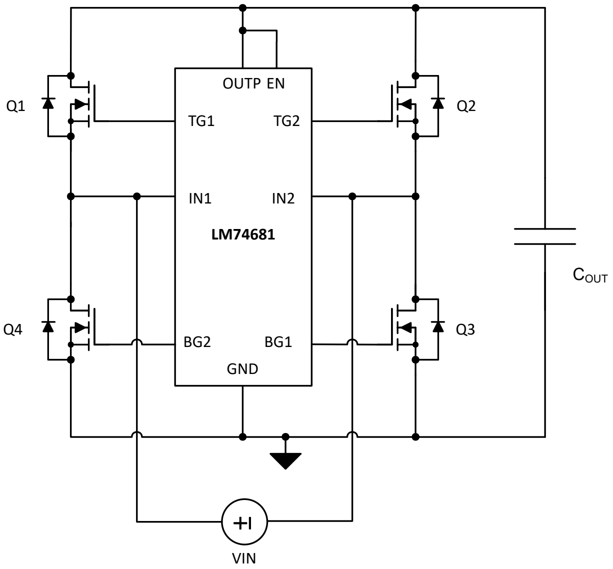
LM74681 100V 理想ダイオード ブリッジ コントローラ、PoE 受電アプリケーション向け

1 特長

- 動作入力電圧範囲：30V～90V
  - 絶対最大電圧 100V
- 4 つのゲート ドライブ制御を内蔵
- 165μA のゲート プルアップ強度
- 100mA のゲート プルダウン強度
- きわめて低い静止電流：0.27μA (検出および分類フェーズ時、$V_{IN1\text{-}IN2}$ < 23V)
- 電源 OR 接続アプリケーション向けのリニア ゲート レギュレーション制御
  - V_{TG_REG} = 11mV
- ユーザー制御によるデバイスのオン / オフ機能用イネーブル ピン
- 動作時の接合部温度範囲：–40℃～125℃
- 小さい占有面積：3mm×3mm WSON-12
  - IPC-9592 の間隔規定に適合

2 アプリケーション

- PoE 受電側機器 (48V)
- ビデオ監視：IP カメラ
- 極性のない電源入力



代表的なアプリケーション回路図

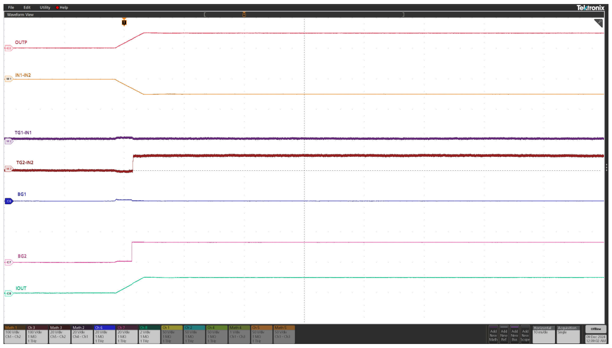
3 概要

LM74681 は、MOSFET ブリッジを駆動できる 100V 理想ダイオード ブリッジ コントローラであり、PoE (Power over Ethernet) アプリケーションにおいて、効率的な低損失ブリッジ整流器ソリューションを実現できます。これにより、Power over Ethernet (PoE) 受電側機器 (PD) が、RJ-45 データペア、予備ペア、またはこれら 2 つの任意の組み合わせから、電圧極性に関係なく電力を受け取ることができます。内蔵チャージ ポンプにより N チャネル MOSFET の使用が可能です。N チャネルは、同じ電力レベルの P チャネル MOSFET よりも小型で、コスト効率が優れています。LM74681 および N チャネル MOSFET ブリッジは、従来のダイオード ブリッジを置き換えることができ、2 ペアおよび 4 ペアの PoE PD システムの実装に便利です。電源障害や短絡が発生した場合、高速ターンオフ機能により逆電流スパイクを低減させます。また、このデバイスは静止電流が 0.27μA と非常に低いので、PoE PD の検出および分類フェーズ中にデータの破損が発生しないことが保証されます。このデバイスは、-40℃～+125℃の接合部温度範囲で動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LM74681	DRR (WSON、12)	3mm × 3mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



-48V DC 入力、Vin ランプでの起動

Table of Contents

4 Pin Configuration and Functions

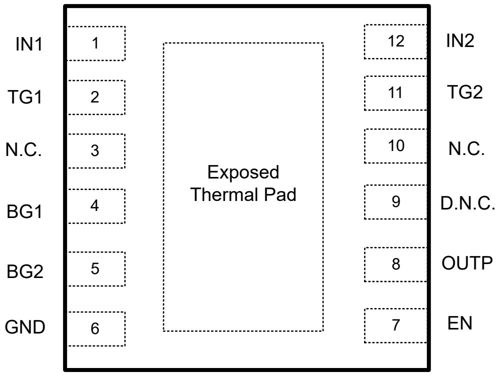


図 4-1. DRR Package, 12-Pin WSON (Top View)

表 4-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	IN1	I	Bridge rectifier input 1. Connect to top side MOSFET Q1 source and bottom side MOSFET Q4 drain.
2	TG1	O	Top side MOSFET gate drive 1.
3	N.C.	—	No connection.
4	BG1	O	Bottom side MOSFET gate drive 1.
5	BG2	O	Bottom side MOSFET gate drive 2.
6	GND	G	Device ground. Connect to bottom side MOSFETs Q3 and Q4 source and output ground.
7	EN	I	Enable pin. Can be connected to OUTP for always ON operation.
8	OUTP	I	Bridge rectifier output. Connect to top side MOSFETs Q1 and Q2 drain. Connect a minimum of 0.1µF between OUTP and GND close to the IC.
9	D.N.C.	—	No connection. Do not connect externally.
10	N.C.	—	No connection.
11	TG2	O	Top side MOSFET gate drive 2.
12	IN2	I	Bridge rectifier input 2. Connect to top side MOSFET Q2 source and bottom side MOSFET Q3 drain.

(1) I = Input, O = Output, G = GND

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	OUTP to GND	–0.3	100	V
	IN1, IN2 to GND	–2	OUTP+2	
	EN to GND	–0.3	OUTP	
	IN1-IN2	–100	100	
Output Pins	BG1, BG2 to GND	–0.3	15	V
	TG1 to IN1 and TG2 to IN2	–0.3	15	
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	OUTP to GND	30		90	V
	EN to GND	0		OUTP	
Input to Output pins	OUTP to INx	–90			V
External MOSFET max V_{GS} rating	GATE to SOURCE	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see セクション 5.5.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC(1)		LM7468x	UNIT
		DRR (WSON)	
		12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W

5.4 Thermal Information (続き)

THERMAL METRIC[1]		LM7468x	UNIT
		DRR (WSON)	
		12 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, OUTP = 48 V, $V_{(EN)}$ = OUTP, C_{OUT}: 1uF over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{OUTP}	OUTP voltage range		30		90	V
V_{OUT_UVLOR}			24.9	27.6	29.5	V
V_{OUT_UVLOF}			24	26.7	28.5	V
$V_{OUT\_UVLO\_Hyst}$				0.9		V
I_Q	Operating Quiescent Current	V_{EN} = 3.3V, V_{OUTP} = 48V, I_{GND}		270	450	µA
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0 V, V_{OUTP} = 48 V		12.8	15	µA
	UVLO shutdown current (detection phase)	2.7 V ≤ V_{OUTP} ≤ 10.1 V		0.27	3.8	µA
	UVLO shutdown current (classification phase)	10.2 V ≤ V_{OUTP} ≤ 23 V		0.27	3.8	µA
ENABLE INPUT						
V_{EN_IL}	Enable input low threshold		0.413	0.7	0.96	V
V_{EN_IH}	Enable input high threshold		0.631	0.9	1.15	
V_{EN_Hys}	Enable Hysteresis			0.2		V
I_{EN}	Enable pin leakage current	$V_{(EN)}$ = 48 V		87	241	nA
V_{IN} to V_{OUTP}						
V_{FWD}	Threshold for forward conduction		169	195	226	mV
V_{REV}	Threshold for reverse current blocking		-17	-11	-5	mV
V_{TG_REG}	Top side gate drive regulation voltage		7	11	16	mV
$V_{TG\_REG\_SINK}$	Top side regulation sink current		5	10	16	µA
V_{TG_FC}	Full conduction threshold			56		mV
GATE DRIVE						
$V_{TGx} – V_{INx}$	Top Gate Drive Voltage		8.7	10	11.1	V
$V_{BGx} – V_{GND}$	Bottom Gate Drive Voltage		11.96	13	13.85	V
I_{TGx}	Peak source current	$V_{INx} – V_{GND}$ = 100 mV, $V_{TGx} – V_{INx}$ = 5 V	124	165	210	µA
	Peak sink current	$V_{INx} – V_{GND}$ = –50 mV, $V_{TGx} – V_{INx}$ = 5 V		100		mA
I_{BGx}	Peak source current	$V_{BGx} – V_{GND}$ = 5 V	2.3	3.7	5	mA
	Peak sink current	$V_{BGx} – V_{GND}$ = 5 V		80		mA

5.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, OUTP = 48 V, $V_{(EN)}$ = OUTP, C_{OUT}: 1uF over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to TGx Turn On delay			170	265	µs
EN_{TDLY}	Enable (low to high) to BGx Turn On delay			6	9.5	µs
$t_{Reverse\ delay}$	Reverse voltage detection to TGx Turn Off delay	$V_{(IN)} – V_{(OUTP)}$ = 100 mV to –100 mV		2	3	µs
$t_{Forward\ recovery}$	Forward voltage detection to TGx Turn On delay	$V_{(IN)} – V_{(OUTP)}$ = –100 mV to 700 mV		5	9.1	µs

5.7 Typical Characteristics

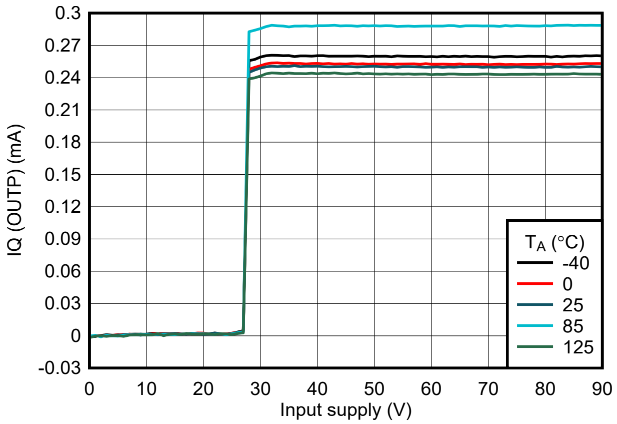


図 5-1. I_Q vs Supply Voltage

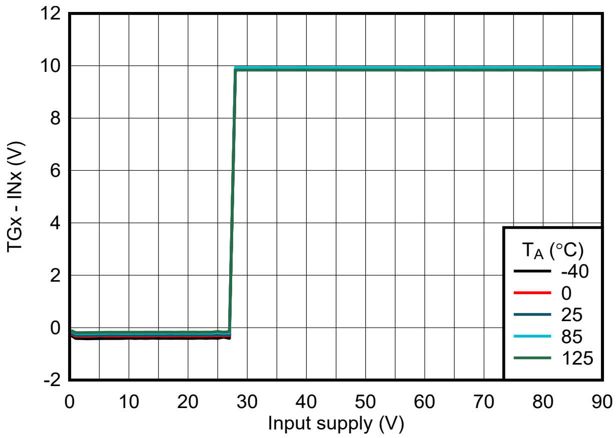


図 5-2. Top Side Gate Drive Voltage vs Supply Voltage

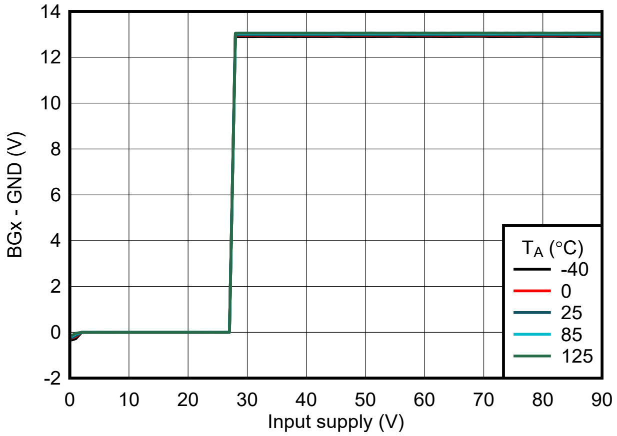


図 5-3. Bottom Side Gate Drive Voltage vs Supply Voltage

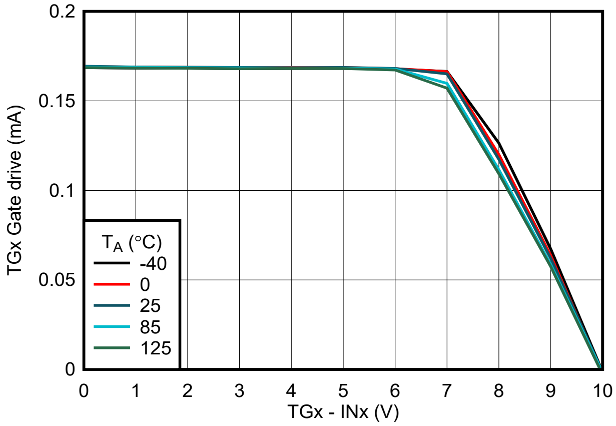


図 5-4. Top Side Gate Drive Source Current vs Gate Drive Voltage

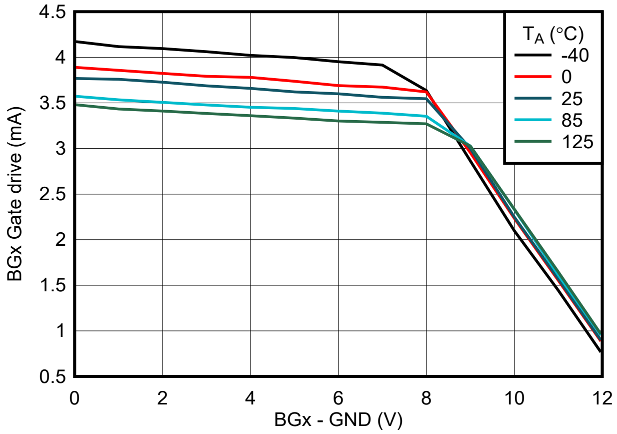


図 5-5. Bottom Side Gate Drive Source Current vs Gate Drive Voltage

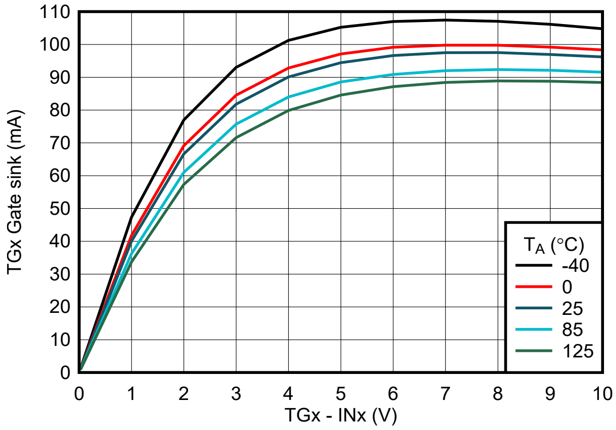


図 5-6. Top Side Gate Drive Sink Current vs Gate Drive Voltage

5.7 Typical Characteristics (continued)

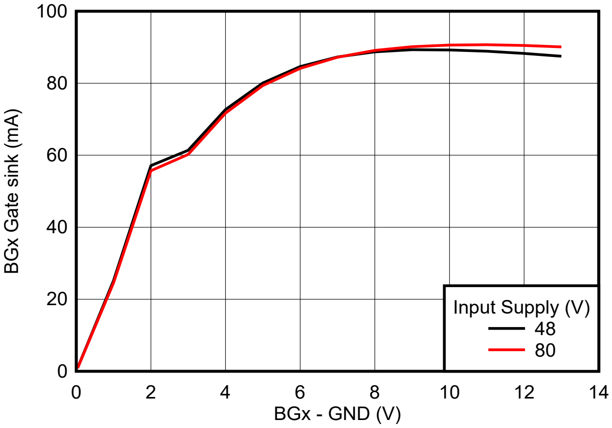


図 5-7. Bottom Side Gate Drive Sink Current vs Gate Drive Voltage

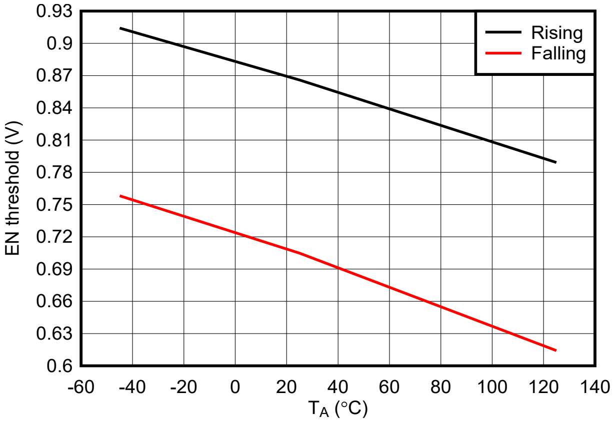


図 5-8. Enable Threshold vs Temperature

6 Parameter Measurement Information

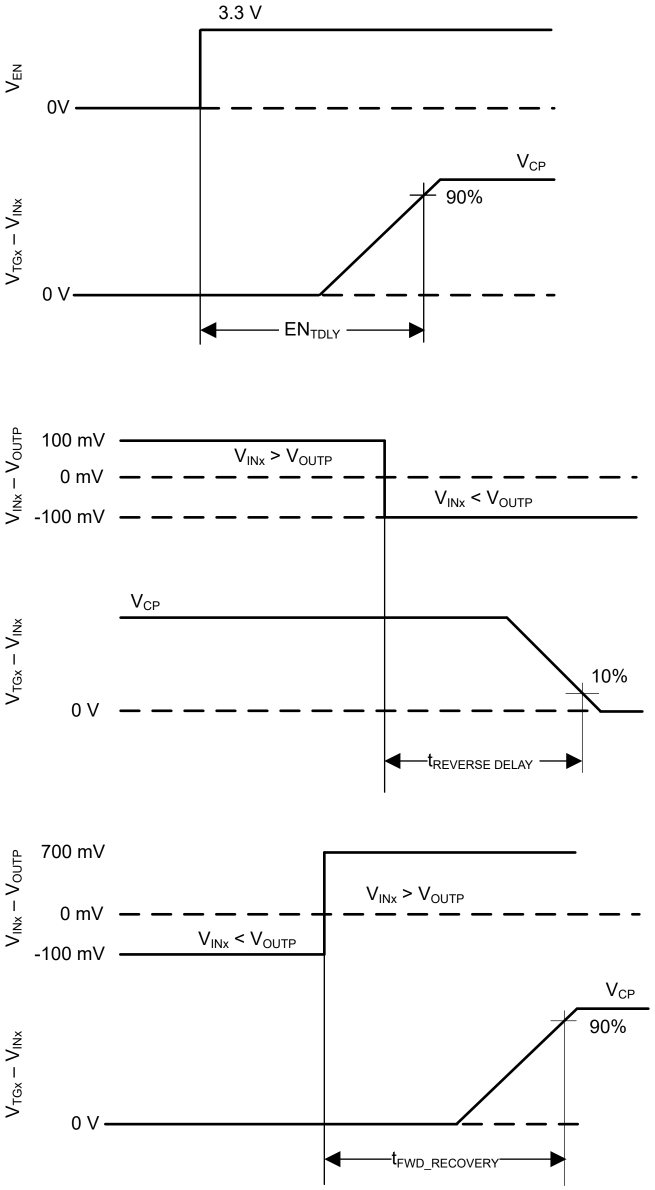


図 6-1. Timing Waveforms

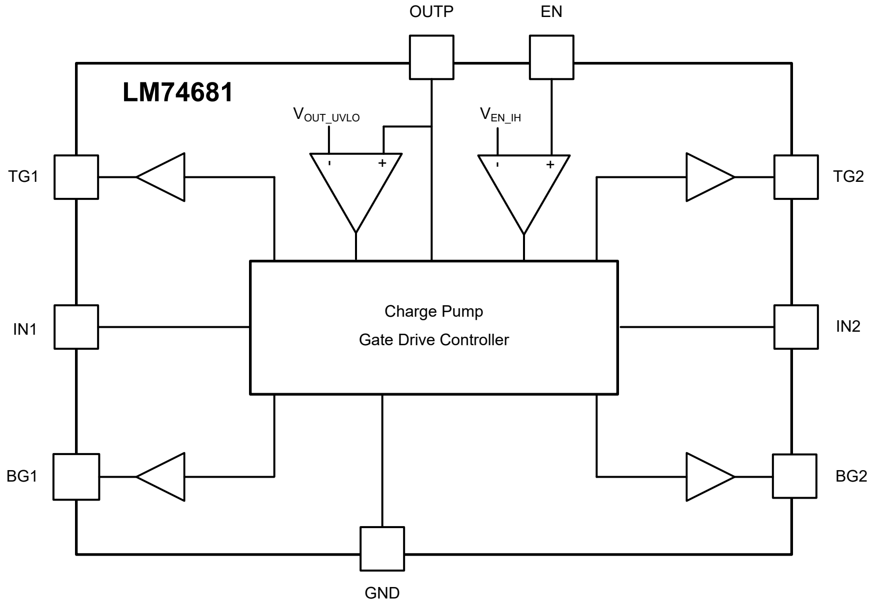
7 Detailed Description

7.1 Overview

The LM74681 is an ideal diode bridge controller designed to meet input rectifier requirements in PoE PD applications. A very common application is an IEEE 802.3 powered device, which is required to accept voltage in either polarity at its RJ-45 input (polarity agnostics input). Traditional diode bridges have lower efficiency due to the forward drop generated across two conducting diodes. Schottky diode based bridge rectifier offer lower forward drop compared to standard diode bridge however the schottky bridge may not be suitable for high temperature applications. Schottky diode bridges exhibit temperature induced leakage currents. These leakage currents have a voltage dependency that can invalidate the measured detection signature. In addition, these leakage currents can back-feed through the unpowered branch and the unused bridge, violating IEEE 802.3 specifications. Ideal diode bridge circuits are often implemented with discrete components such as a combination of P-channel and N-channel MOSFETs. These bridges usually exhibit poorer performance in terms of quiescent current, transient immunity against supply transients, and wider variation in leakage currents over temperature.

LM74681 offers integrated gate control for the external MOSFET bridge to realize low-loss rectifier solution for PoE PD applications. This device can handle transient voltages up to 100V, which makes it suitable to meet voltage transient requirements in 48V PoE powered applications. LM74681 features a linear ORing gate control mechanism that stops the powered device from allowing current to back-feed into the Ethernet cable. It also incorporates a built-in under-voltage lockout (UVLO) feature to ensure ultra-low quiescent current during both PoE PD detection (VIN < 10.5V) and classification phases (VIN < 20.5V).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input and Output Voltage

LM74681 supports power sources with wide input voltage range enabling polarity-agnostic power source to be connected to its IN1 and IN2 pins. LM74681 is designed to operate with IN1 and IN2 designed to vary from 90V to –90V. The LM74681 device includes an OUTP UVLO feature that enables it to consume extremely low quiescent current, around 0.27μA, when the OUTP voltage is below V_{OUTP_UVLO}. This capability guarantees that data corruption does not occur during the Power over Ethernet (PoE) Powered Device (PD) detection and classification stage.

The OUTP pin is used to power the internal circuitry of LM74681, typically drawing I_Q when enabled and I_{SHDN} when disabled. If the OUTP pin voltage is greater than the V_{OUTP_UVLO} rising threshold, then LM74681 operates in either shutdown mode or active mode in as per the EN pin voltage. LM74681 supports an OUTP voltage of up to 90V during normal operation and can withstand voltage transients up to 100V ensuring protection against surges.

7.3.2 Charge Pump

The internal charge pump supplies the voltage necessary to drive the gate of the external N-channel MOSFETs. The charge pump is activated once the EN pin voltage is above the specified input high threshold, V_{EN_IH}. If EN pin is pulled low, then the charge pump remains disabled. By enabling and disabling the charge pump, the operating quiescent current of the LM74681 can be optimized as per system requirements.

7.3.3 Gate Driver

The gate drivers are used to control the external N-Channel MOSFETs by setting the GATE to SOURCE voltage to the corresponding mode of operation. The FETs on the top side Q1 and Q2 are driven by gates TG1 and TG2 and the FETs on the bottom side Q3 and Q4 are driven by gates BG1 and BG2 respectively.

The internal charge pump powers the top side gate drivers and depending on the DRAIN to SOURCE voltage of each MOSFET, LM74681 has three defined modes of operation the gate driver operates under which are forward regulation, full conduction mode and reverse current protection. These modes are described in more detail in セクション 7.4.1.1, セクション 7.4.1.2, and セクション 7.4.2. 図 7-1 depicts how the modes of operation vary according to the DRAIN to SOURCE voltage. The threshold between forward regulation and conduction modes is when the DRAIN to SOURCE voltage is V_{TG_REG}. The threshold between forward regulation mode and reverse current protection mode is when the DRAIN to SOURCE voltage is V_{REV}.

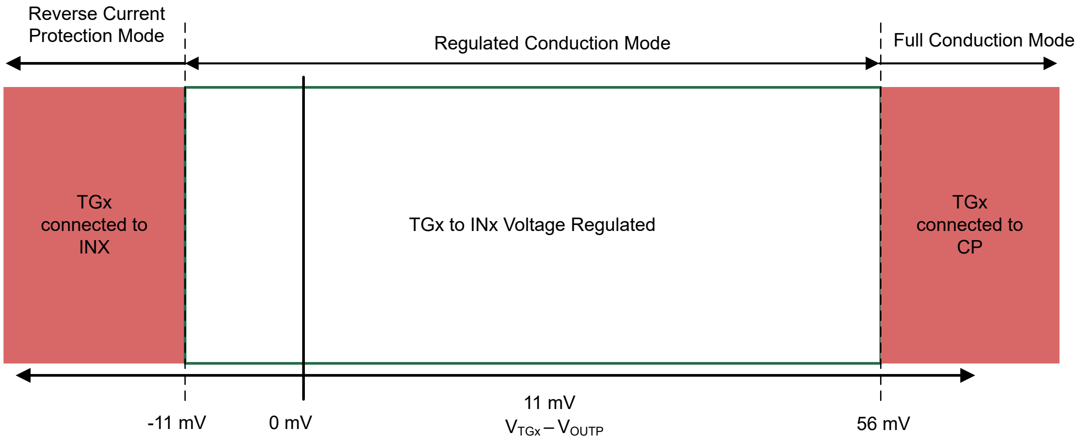


図 7-1. Gate Driver Mode Transitions

The bottom-side gate drivers of the LM74681 are powered directly from the IN1 or IN2 voltage and operate in two distinct modes which are forward full conduction and reverse current blocking. These gate drivers are controlled by below logic to ensure efficient power flow and protection against reverse current.

- BG1 is enabled and in full conduction when the voltage at IN1 is greater than that GND+2V and is disabled when IN1 falls below IN2 to block reverse current flow.
- Similarly, BG2 is enabled when IN2 exceeds GND+2V and is disabled when IN2 is lower than IN1.

7.3.4 Enable

The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate drivers and charge pump operates as described in セクション 7.3.3 and セクション 7.3.2. If the enable pin voltage is less than the input low threshold, the charge pump and gate drivers are disabled placing the LM74681 in shutdown mode. The EN pin to be connected directly to the OUTP pin if enable control is not needed.

7.4 Device Functional Modes

7.4.1 Conduction Mode

Conduction mode occurs when the top gate drivers are enabled and there are two regions of operating in this mode based on the source to drain voltage of the FETs driven by LM74681. The modes are described in セクション 7.4.1.1 and セクション 7.4.1.2.

7.4.1.1 Regulated Conduction Mode

For the LM74681 to operate its top gates TG1 and TG2 in regulated conduction mode, the gate driver must be enabled as described in セクション 7.3.3 and the current from source to drain of the external MOSFET must be within the range to result in an INx to OUTP voltage drop of V_{REV} to V_{TG_FC} . During forward regulation mode, the INx to OUTP voltage is regulated to V_{TG_REG} by adjusting the gate to source voltage. This closed loop regulation scheme enables graceful turn-off of the MOSFET at very light loads and ensures zero DC reverse current flow.

7.4.1.2 Full Conduction Mode

For the LM74681 to operate its top gates TG1 and TG2 in full conduction mode the gate driver must be enabled as described in セクション 7.3.3 and the current from source to drain of the external MOSFET must be large enough to result in an INx to OUTP voltage drop of greater than V_{TG_FC}. If these conditions are achieved the GATE pin is internally connected to the charge pump resulting in the INx to OUTP voltage being equal to $V_{TGx} – V_{INx}$. By connecting the internal charge pump to GATE the external MOSFET $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

7.4.2 Reverse Current Protection Mode

For the LM74681 to operate in reverse current protection mode, the gate driver must be enabled as described in セクション 7.3.3 and the current of the external MOSFET must be flowing from the drain to the source. When the INx to OUTP voltage is typically less than V_{REV}, reverse current protection mode is entered and the FET gates is internally connected to the source. This connection of the TGx to INx pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

8 Application and Implementation

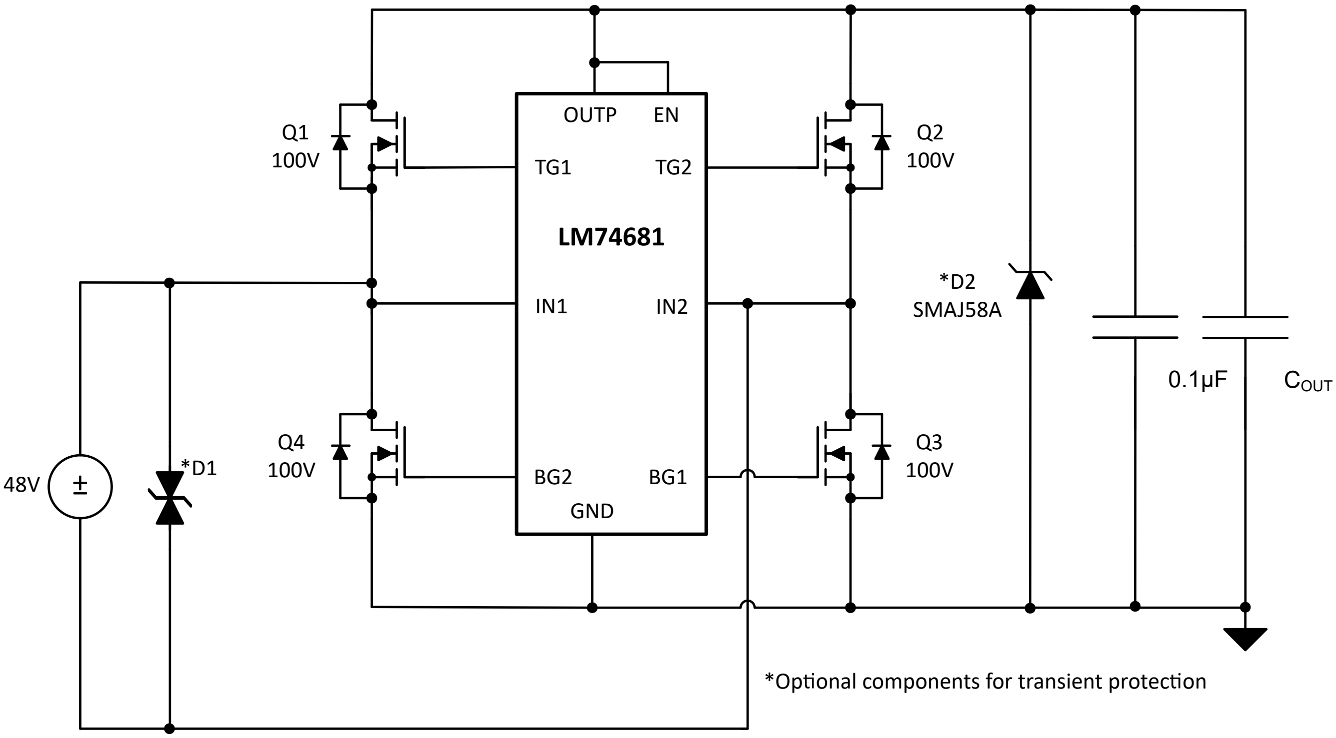
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM74681 drives four external N-channel MOSFETs in a diode bridge configuration, making it ideal for rectifying power supplies of any polarity. By replacing traditional diodes with MOSFETs, the device minimizes conduction losses, resulting in improved thermal performance and increased overall system efficiency. OUTP UVLO feature of LM74681 makes it suitable for Power over Ethernet (PoE) applications. The schematic for a 48V POE PD application is shown in 図 8-1 where the LM74681 is driving the high side MOSFETs Q1, Q2 and low side MOSFETs Q3, Q4 in diode bridge configuration.

8.2 Typical Application



*Optional components for transient protection

図 8-1. Typical Application Circuit

8.2.1 Design Requirements

A design example, with system design parameters listed in 表 8-1 is presented.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Application	PoE PD input IEEE 802.3at
Input voltage range	44V to 57V
Input Power	30W

8.2.2 Detailed Design Procedure

8.2.2.1 Design Considerations

- Input operating voltage range, including line transients
- Maximum load current
- Output Capacitance

8.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum gate-to-source voltage $V_{GS(MAX)}$, and the drain-to-source On resistance $R_{DS(ON)}$.

The $V_{DS(MAX)}$ rating of the MOSFET must be high enough to withstand the highest differential voltage seen in the application, including any anticipated transients during fault conditions. For a 48V PoE application, a MOSFET with a voltage rating of 100V is recommended. The LM74681 can drive a maximum gate-to-source voltage of 13.8V. A MOSFET with a minimum $V_{GS(MAX)}$ rating of 15V should be selected. For MOSFETs with lower V_{GS} ratings, a Zener diode can be used to clamp the voltage to a safe level.

The MOSFET I_D rating must exceed the maximum continuous load current to ensure reliable operation under full load conditions. Additionally, the MOSFET thermal resistance should be considered to ensure the junction temperature (T_J) remains within safe limits under the expected maximum power dissipation including the initial inrush phase when the output capacitors are charged through the MOSFETs body diode.

To reduce the MOSFET conduction losses, the lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not always be beneficial. Higher $R_{DS(ON)}$ will provide increased voltage information to the LM74681 reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with $R_{DS(ON)}$ that develops <30mV forward voltage drop at maximum current is a good starting point. Usually, $R_{DS(ON)}$ increases drastically below 4.5V V_{GS} and $R_{DS(ON)}$ is highest when V_{GS} is close to MOSFET V_{th}. For stable regulation at light load conditions, it is recommended to operate the MOSFET close to 4.5V V_{GS}, that is, much higher than the MOSFET gate threshold voltage. It is recommended to choose MOSFET gate threshold voltage V_{th} of 2.5V to 3.5V maximum. Choosing a lower V_{th} MOSFET also reduces the turn ON time.

PSMN040-100MSE N-channel MOSFET is selected to meet this 48V PoE PD bridge rectifier design and it is rated at:

- $V_{DS(MAX)}$: 100V
- $V_{GS(MAX)}$: ±20V
- $R_{DS(ON)}$: 29.4mΩ (typical) and 36.6mΩ (maximum) at 10V V_{GS}

8.2.2.3 Output capacitance

A minimum ceramic capacitor of 0.1µF is recommended to be placed across the OUTP and GND pins as close to the LM74681 as possible for decoupling. Additional output capacitance C_{OUT} may be required,

- Downstream DC-DC converter input capacitance requirement
- To ensure that the rectified output voltage remains stable during load transients
- To smooth the output voltage and reduce ripple to acceptable level

8.2.3 Application Curves

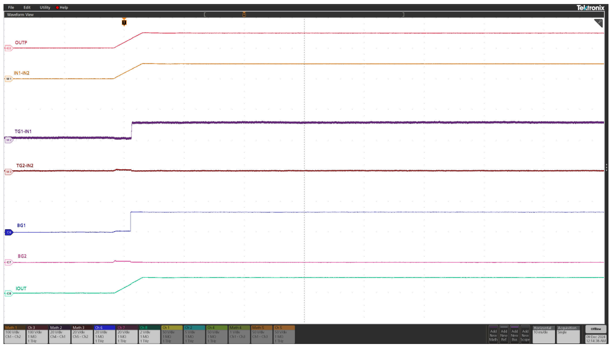


図 8-2. +48V DC Input, Startup with Vin Ramp

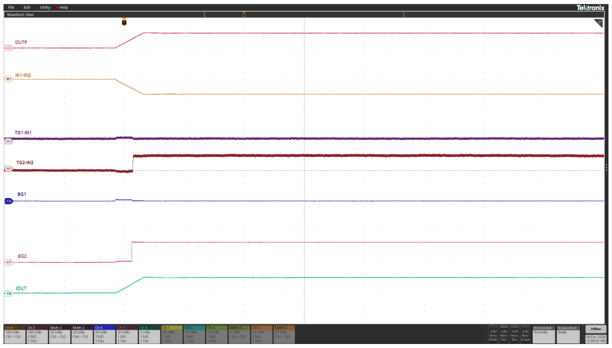


図 8-3. -48V DC Input, Startup with Vin Ramp

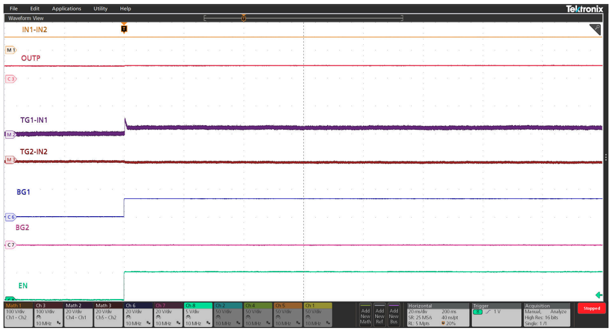


図 8-4. 48V DC Input, Startup with EN toggle High

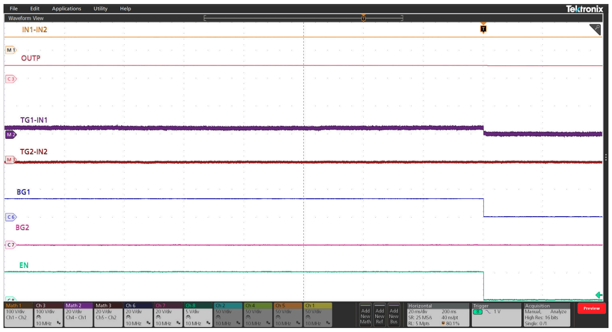


図 8-5. 48V DC Input, Shutdown with EN toggle Low

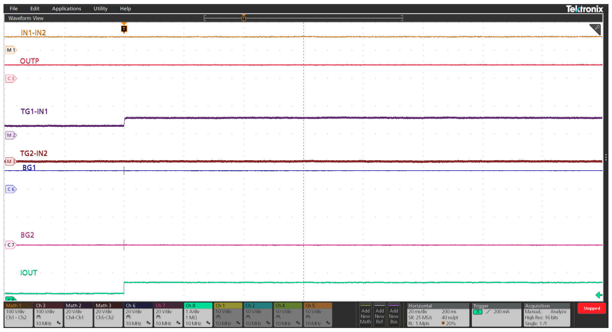


図 8-6. Load Step Increase from 10W to 30W

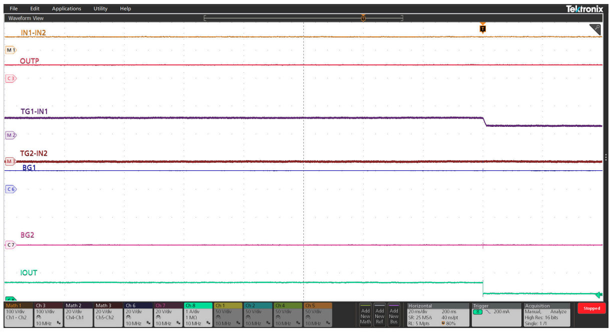


図 8-7. Load Step Decrease from 30W to 10W

8.3 Powered Device for IEEE 802.3bt Class 5-8 (45W-90W) Systems

In PoE PD applications requiring greater than 30W power, the IEEE 802.3bt standard recommends the use of a 4-pair cable for efficient power delivery. To support this, two LM74681 controllers can be used to drive two independent N-channel MOSFET based full-bridge rectifiers connected to a common output. Each LM74681 drives one full-bridge rectifier, enabling power rectification from the two separate 2-pair power paths provided by the 4-pair cable. This approach ensures compliance with the higher power delivery capabilities of the IEEE 802.3bt standard while maintaining high efficiency.

The linear ORing gate control mechanism of LM74681 actively drives the MOSFET gates, allowing forward conduction and reverse current blocking. This prevents backflow between the two power paths and avoids current flow back into the Ethernet cable. By replacing traditional diodes with low $R_{DS(ON)}$ MOSFETs, the LM74681 reduces conduction losses and heat generation, which is critical for high-power PoE systems. The rectified outputs of the two full bridges are combined at the PD input, providing seamless power delivery. This architecture enables efficient, reliable operation for PoE PD systems requiring high power levels in compliance with IEEE 802.3bt standards.

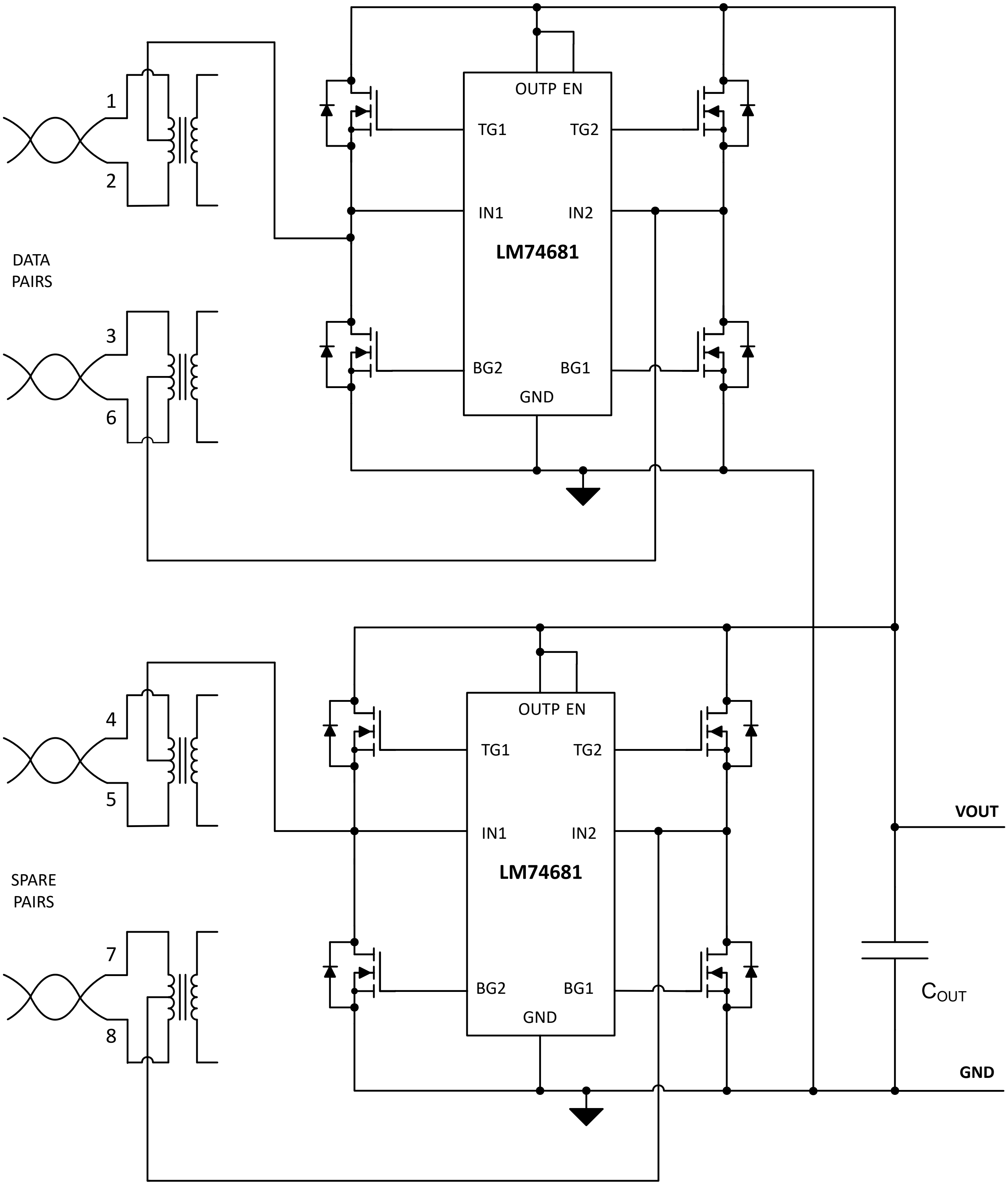


図 8-8. Typical PoE PD High Power Application

8.4 Power Supply Recommendations

8.4.1 Transient Protection

The TVS at input or output is not required for the LM74681 to operate, but it may be required to clamp the voltage transients caused by lightning, switching surges, or power disturbances that can exceed the voltage ratings of MOSFETs and the controller possibly causing damage. A TVS diode protects against such events by clamping the transient voltages to safe levels. For 48V PoE PD application, a unidirectional TVS like SMAJ58A with a standoff voltage above the maximum input DC voltage and a clamping voltage below the MOSFET's maximum rating is recommended. This TVS is recommended to be placed as close to the LM74681 as possible. In well-regulated applications with minimal transient risks, a TVS diode may not be necessary.

8.5 Layout

8.5.1 Layout Guidelines

- Place the decoupling capacitor close to the OUTP pin and IC GND.
- For the top side MOSFETs, connect the INx, TGx, and OUTP pins of LM74681 close to the MOSFET SOURCE, GATE, and DRAIN pins.
- The high current path is through the MOSFETs, therefore it is important to use thick and short traces for the source and drain of the MOSFET to minimize resistive losses.
- The TGx and BGx pins of the LM74681 must be connected to the respective MOSFET gate with a short trace.
- Place transient suppression components close to LM74681.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the セクション 8.5.2 is intended as a guideline and to produce good results.

8.5.2 Layout Example

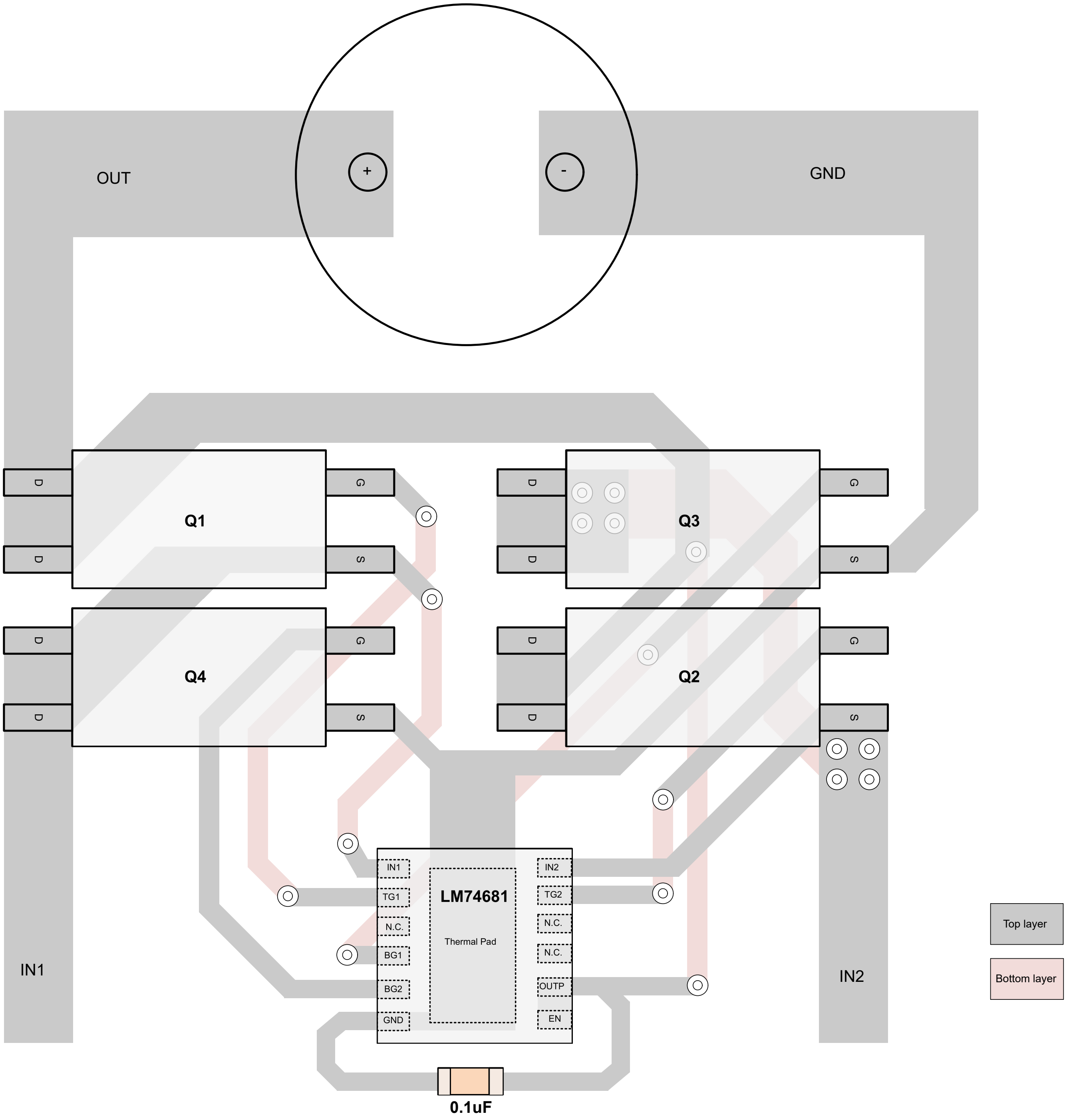


図 8-9. LM74681 Example Layout

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74681DRRR	ACTIVE	WSON	DRR	12	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L74681	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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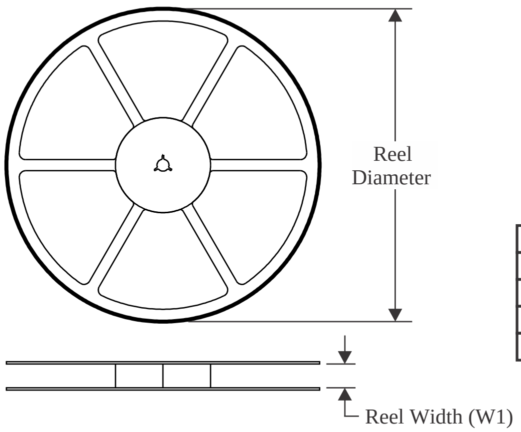
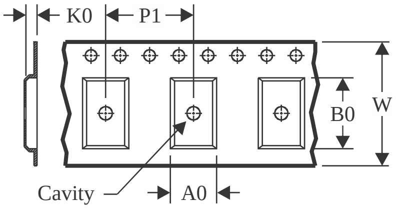
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

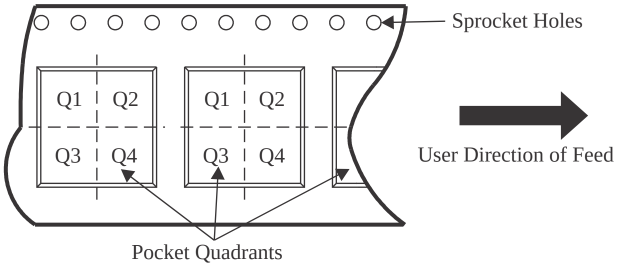


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

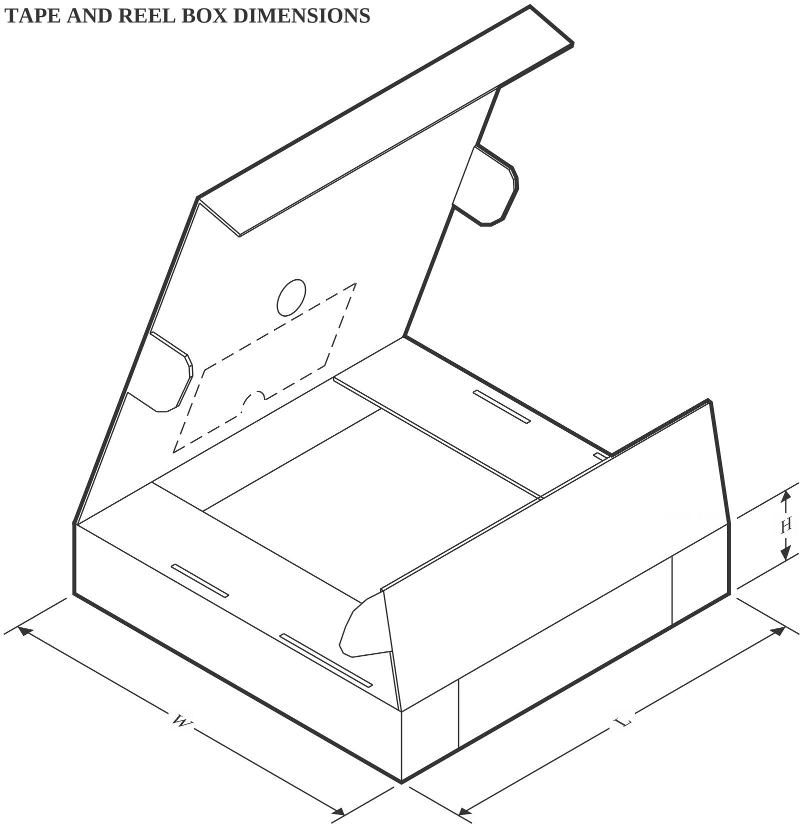
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74681DRRR	WSON	DRR	12	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74681DRRR	WSON	DRR	12	5000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

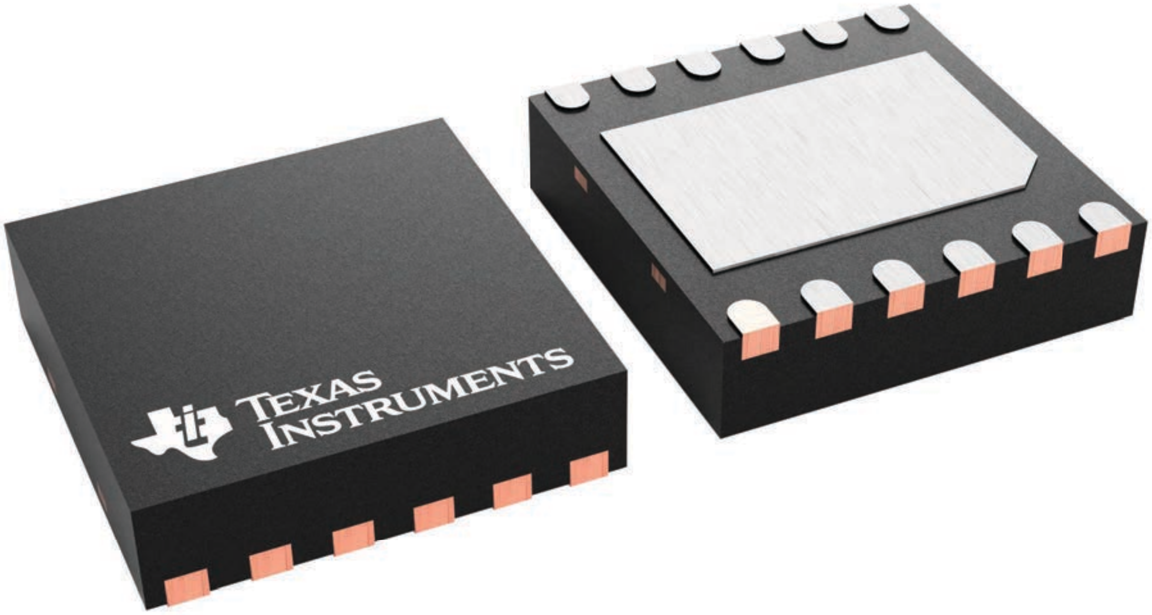
DRR 12

WSON - 0.8 mm max height

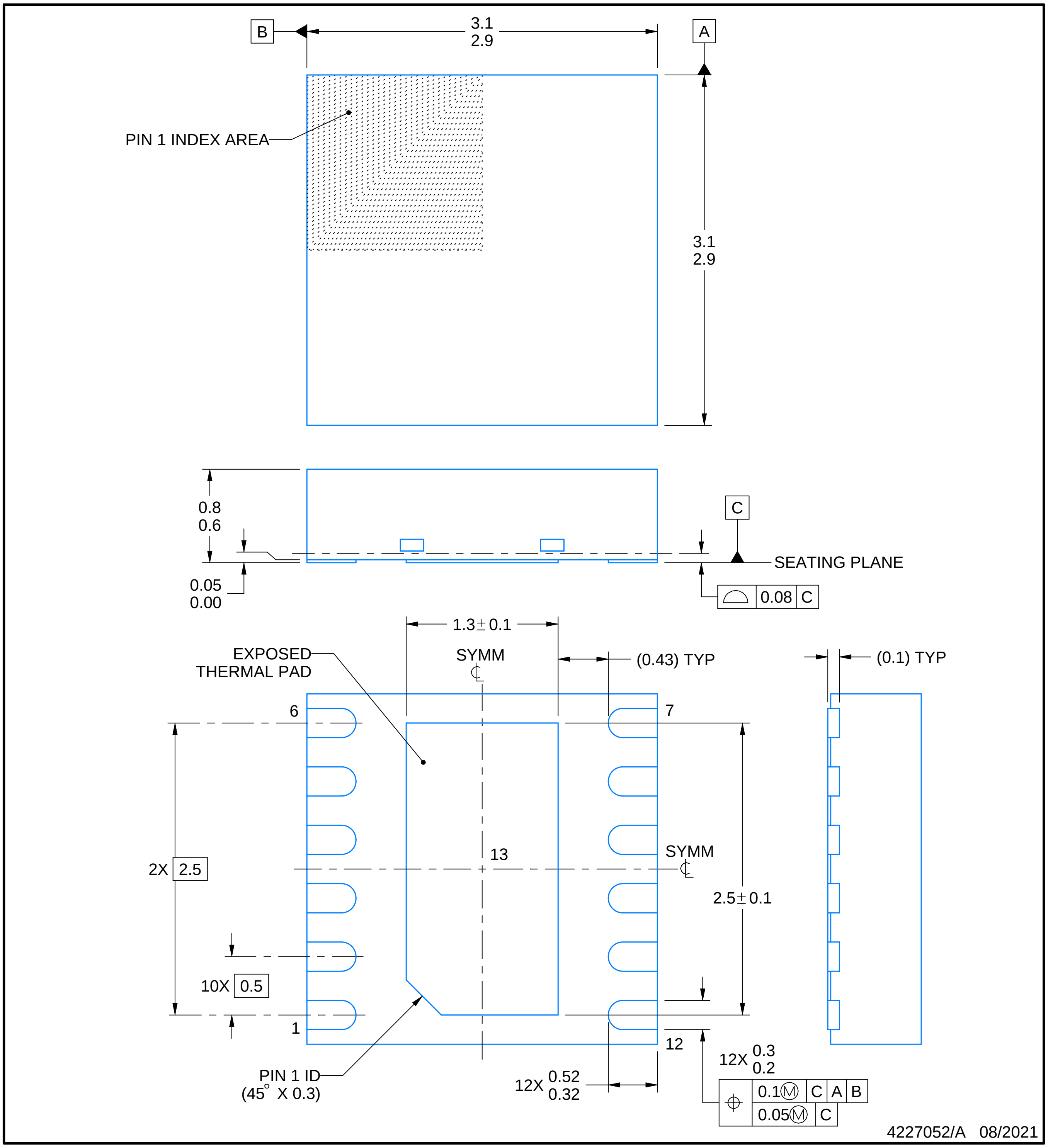
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

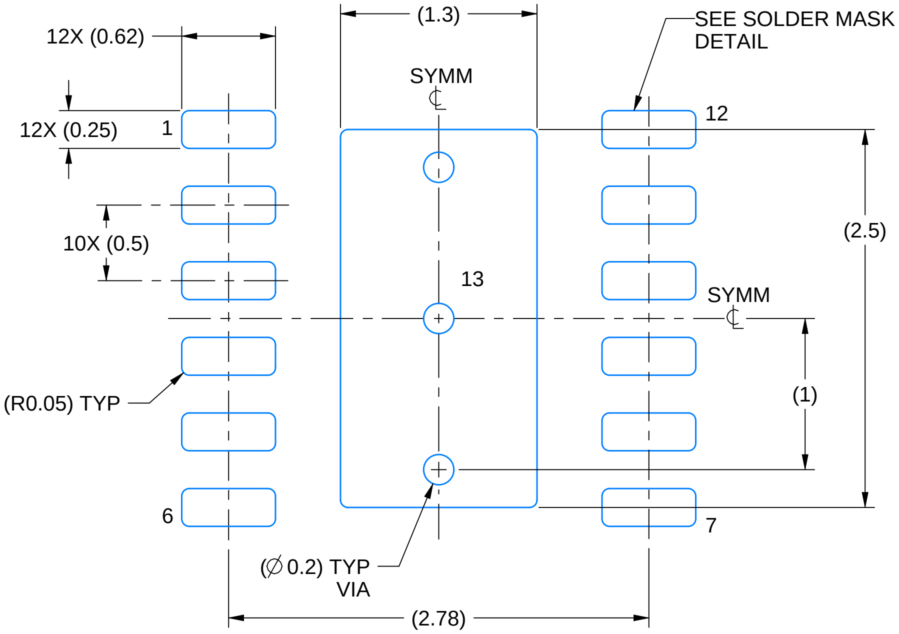


4223490/B

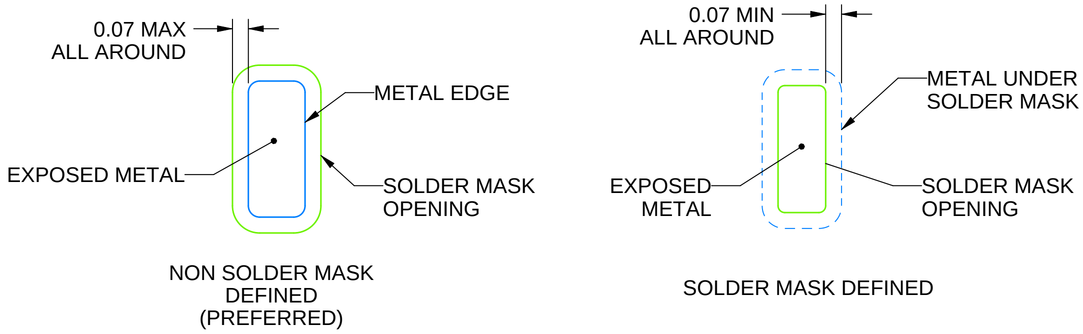


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

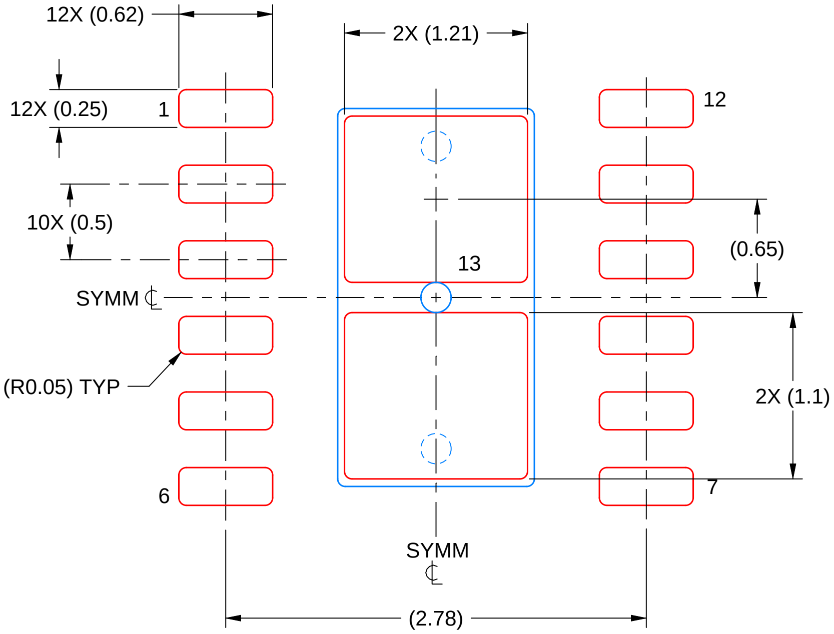


SOLDER MASK DETAILS

4227052/A 08/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 13
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227052/A 08/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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