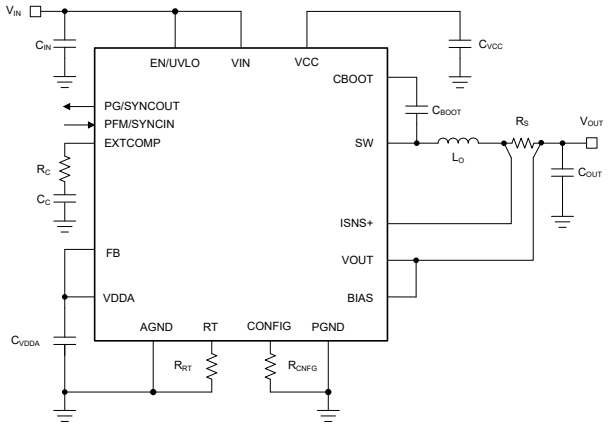
LM704A0-Q1 45V、10A、車載用、高電力密度向けに設計された高効率降圧コンバータ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 同期整流 DC/DC コンバータ、多用途降圧コントローラと堅牢なパワー MOSFET 付き
  - 幅広い入力電圧範囲:4.5V～45V
  - シャットダウン モード電流:2.3μA
  - 無負荷時 I_Q を 12V から 5V にレギュレート:15.5μA
  - 精度 1% の固定 3.3V、5V、12V 出力または可変出力 (0.8V～36V)
  - 最大 16A の出力電流をイネーブルにするデュアル フェーズ動作、単一出力
- 低 EMI 要件向けの設計
  - CISPR 25 Class 5 準拠
  - ピン選択可能な ±8% のデュアル ランダム スペクトラム拡散により、ピーク放射が低減されます
  - スイッチング周波数:200kHz～2.2MHz
  - ピンで構成可能な自動または FPWM 動作
- 堅牢な設計用の本質的な保護機能
  - ヒカップ モードによる過電流の内部保護
  - イネーブル、パワー グッド、サーマル シャットダウン
  - 内部または外部ループ補償
- 6mm × 6mm の熱最適化、RoHS 準拠、鉛フリー メッキの QFN-29 パッケージ
- WEBENCH® Power Designer により、LM704A0-Q1 を使用するカスタム設計を作成



代表的なアプリケーション回路

2 アプリケーション

- 車載用電子システム
- 先進運転支援システム (ADAS)
- インフォテインメントおよびクラスタ

3 概要

LM704A0-Q1 は、低 I_Q で V_{IN} の広い同期整流降圧のファミリで、4.5V～45V の入力電圧範囲用に設計され、3.3V、5V、12V の固定出力電圧または可変出力で最大 10A の出力電流を供給します。

LM704A0-Q1 はピーク電流モード制御アーキテクチャを採用しているため、ループ補償が簡単で、過渡応答が高速であり、負荷およびライン レギュレーションが非常に優れています。1 対の LM704A0-Q1 コンバータは、最大 20A の出力電流を必要とするアプリケーション向けに、高精度の電流共有が可能なインターリーブ モード (並列出力) に設定できます。

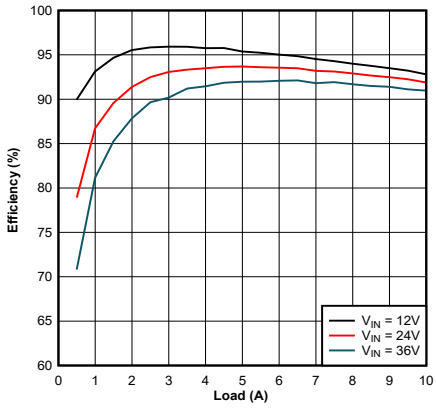
LM704A0-Q1 は独自のデュアル ランダム スペクトラム拡散 (DRSS) 機能を備えており、低周波数の三角波変調と高周波数のサイクル単位のランダム変調を組み合わせることで、広範囲の無線周波数帯域にわたって EMI 性能が向上します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LM704A0-Q1	RRX (VQFN、29)	6mm × 6mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。

(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的な効率、V_{OUT} = 5V、f_{SW} = 400kHz

LM704A0-Q1 の追加機能として、ユーザー選択可能なダイオード エミュレーションによる軽負荷時消費電流の低減、オープン ドレインのパワー グッド フラグによるフォルト報告と出力監視、高精度イネーブル入力、プリバイアスされた負荷への単調なスタートアップ、内蔵 VCC バイアス電源レギュレータ、内部 2.8ms ソフトスタート時間、自動回復機能付きサーマル シャットダウン保護があります。

LM704A0-Q1 コンバータは 6mm × 6mm 熱最適化 29 ピン QFN パッケージで供給されます。3 つのダイ接続パッド (VIN、SW、PGND) により、放熱性能と基板レベルの信頼性 (BLR) が向上しています。

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4 Pin Configuration and Functions

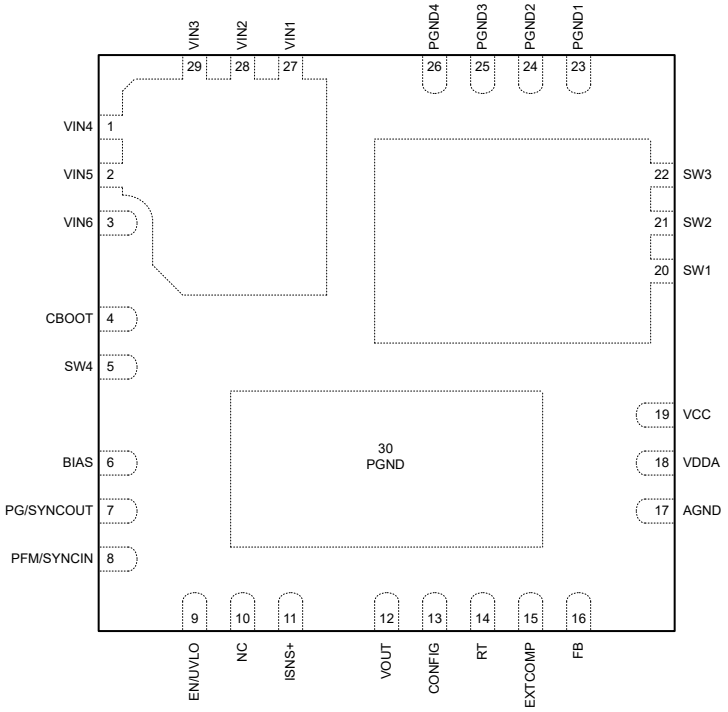


図 4-1. RRX Package, 29-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VIN4	P	Converter input pins to the drain of the high-side power MOSFET and the VCC regulator (VIN6). Connect to the input supply and the input filter capacitors. The path from the VIN pin to the input capacitors must be as short as possible.
2	VIN5	P	
3	VIN6	P	
4	CBOOT	P	High-side driver supply for the bootstrap gate drive. Connect a 47nF bootstrap capacitor between the CBOOT and SW4 pins. If VCC = 8V is selected, add a 1Ω resistor in series with the bootstrap capacitor.
5	SW4	P	Switch pin. Connect a 47nF bootstrap capacitor between the CBOOT and SW4 pins. This pin is internally connected to the switch pins SW1, SW2, and SW3. There is no need to route this pin to the other switch pins on a PCB.
6	BIAS	P	Optional input for an external bias supply. If configured for 3.3V fixed VOUT, connect the BIAS pin to an external bias supply from 5V to 30V. If configured for 5V fixed VOUT, connect the BIAS pin to the VOUT node or an external bias supply from 5V to 30V. If configured for 12V fixed or an adjustable VOUT, connect the BIAS pin to the VOUT node or an external bias supply from 10V to 30V. If the output voltage is above 30V and no external supply is used, tie the BIAS pin to GND.
7	PG / SYNCOUT	O	Power-Good / Sync Output pin. This pin is an open-collector output that goes low if VOUT is outside of the specified regulation window. PG / SYNCOUT can also be used as a synchronization output to synchronize the internal oscillator of the secondary device to the oscillator of the primary device.
8	PFM / SYNCIN	I	PFM / FPWM mode selection and synchronization input pin. Connect the PFM / SYNCIN pin to VDDA to enable diode emulation mode. Connect the PFM / SYNCIN pin to AGND to operate in Forced PWM (FPWM) mode with continuous conduction at light loads. The PFM / SYNCIN pin can also be used as a synchronization input to synchronize the internal oscillator to an external clock.
9	EN / UVLO	I	Enable / undervoltage lockout pin. Drive this pin high / low to enable / disable the device. If the enable function is not needed, tie this pin to VIN. Connect an external resistor divider network to set UVLO threshold.
10	NC	P	No connect pin. Leave floating or tie to GND.

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
11	ISNS+	I	Current sense amplifier input. Connect the ISNS+ pin to the inductor side of the external current sense resistor using a low-current Kelvin connection.
12	VOUT	I	Output voltage sense and the current sense amplifier input. Connect the VOUT pin to the output side of the respective current sense resistor.
13	CONFIG	I	Configuration pin. Connect a resistor to ground to set primary/secondary, spread spectrum enable/ disable, or interleaved operation.
14	RT	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 200kHz and 2.2MHz.
15	EXTCOMP	O	External compensation pin. This pin is the output of the transconductance amplifier. If used, connect the compensation network from the EXTCOMP pin to AGND. Connect a 100kΩ resistor between the EXTCOMP and VDDA pins to use the internal compensation.
16	FB	I	Feedback pin. Connect a resistor between FB and VDDA to set the output voltage to 3.3V, 5V or 12V. Connect a resistor divider network from VOUT to FB to set the output voltage level between 0.8V to 36V. The voltage reference setpoint is 0.8V.
17	AGND	G	Analog ground pin. Ground return for the internal voltage reference and analog circuits.
18	VDDA	P	Internal analog bias regulator output pin. Connect a 0.1µF ceramic decoupling capacitor from VDDA to AGND as close as possible to the pins.
19	VCC	P	VCC bias supply pin. Connect a 4.7µF ceramic capacitors between VCC and PGND as close as possible to the pins.
20	SW1	P	Switch pins. These pins form a switching node that is internally connected to the source terminal of the buck switch (high-side MOSFET) and the drain terminal of the synchronous rectifier (low-side MOSFET). Connect to the buck inductor.
21	SW2	P	
22	SW3	P	
23	PGND1	G	Power ground pins. These pins form a power ground node for the low-side MOSFET. Connect to the system ground on a PCB. Path to CIN must be as short as possible.
24	PGND2	G	
25	PGND3	G	
26	PGND4	G	
27	VIN1	P	Converter input pins to the drain of the high-side power MOSFET. Connect to the input supply and the input filter capacitors. The path from the VIN pin to the input capacitors must be as short as possible.
28	VIN2	P	
29	VIN3	P	
30	PGND	G	Controller power ground pin. Connect to the system ground using multiple vias.

(1) P = Power, G = Ground, I = Input, O = Output.

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN to PGND	–0.3	50	V
Pin voltage	SW to PGND	–0.3	50	V
Pin voltage	SW to PGND transient < 20ns	–5	55	V
Pin voltage	CBOOT to SW	–0.3	10	V
Pin voltage	CBOOT to SW, transient < 20ns	–2		V
Pin voltage	EN/UVLO to PGND	–0.3	50	V
Pin voltage	VDDA, PG/SYNCOUT, FB, CONFIG, PFM/SYNCIN, RT, EXTCOMP to AGND	–0.3	6.5	V
Pin voltage	VCC to AGND	–0.3	10	V
Pin voltage	BIAS to AGND	–0.3	32	V
Pin voltage	VOUT, ISNS+ to PGND	–0.3	40	V
Pin voltage	VOUT to ISNS+	–0.3	0.3	V
Pin voltage	PGND to AGND	–0.3	0.3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, 16, 17, 22, 23 and 29)	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		4.5		45	V
V_{OUT}	Output voltage range		0.8		36	V
	Pin voltage	VIN, EN/UVLO, SW to PGND	–0.3		45	V
	Pin voltage	CBOOT to SW	–0.3	8	8.5	V
	Pin voltage	FB, PFM/SYNCIN, PG/SYNCOUT to AGND	–0.3		5.25	V
	Pin voltage	VDDA to PGND	–0.3	5	5.25	V
	Pin voltage	VCC to PGND (Fixed 3.3V or 5V output)	–0.3	5	5.25	V
	Pin voltage	VCC to PGND	–0.3	8	8.5	V
	Pin voltage	BIAS to PGND	–0.3		30	V
	Pin voltage	VOUT, ISNS+ to PGND	–0.3		36	V
	PGND to AGND		–0.3		0.3	V
I_{OUT}	Output current range, LM704A0-Q1		0		10	A
R_S	Sense resistor, LM704A0-Q1		4			mΩ
T_J	Operating junction temperature		–40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		LM704x0-Q1		UNIT
		JESD 51-7	EVM	
		29 PINS	29 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.5[2]	18.6[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.6	[4]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.7	[4]	°C/W
ψ_{JT}	Junction-to-top characterization parameter ($T_{case-center}$)	11.5	7.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter ($T_{case-max}$)	–	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.6	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated with a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For thermal design information please see the *Maximum Ambient Temperature* section.
(3) Refer to the *EVM User's Guide* for board layout and additional information. For thermal design information please see the *Maximum Ambient Temperature* section.
(4) Not applicable to an EVM.

5.5 Electrical Characteristics

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN)						
I_{Q-SD}	V_{IN} shutdown current	Non-switching, V_{EN} = 0V, V_{FB} = V_{REF} + 50mV, T_J = 25°C		2.3	4	µA
		Non-switching, V_{EN} = 0V, V_{FB} = V_{REF} + 50mV, T_J = 125°C		2.3	8	µA
I_{Q-SBY}	V_{IN} standby current [1]	Non-switching, 0.5V ≤ V_{EN} ≤ 1V, External COMP, R_{CONFIG} = 29.4kΩ		350		µA
$I_{Q-SLEEP1-12V}$	V_{IN} sleep current, 3.3V fixed output, no load	V_{EN} = 5V, V_{IN} = 12V, V_{BIAS} = 0V, V_{VOUT} = 3.3V, no-load, non-switching, $V_{PFM/SYNCIN}$ = 5V, R_{FB} = 0Ω to VDDA		10.8		µA
$I_{Q-SLEEP2-12V}$	V_{IN} sleep current, 5V fixed output, no load	V_{EN} = 5V, V_{IN} = 12V, V_{BIAS} = 5V, V_{VOUT} = 5V, no-load, non-switching, $V_{PFM/SYNCIN}$ = 5V, R_{FB} = 24.9kΩ to VDDA		12.2	36	µA
ENABLE (EN / UVLO)						
V_{SBY-TH}	Shutdown-to-standby threshold voltage	$V_{EN/UVLO}$ rising		0.55		V
V_{EN-TH}	Enable voltage rising threshold	$V_{EN/UVLO}$ rising	0.95	1.0	1.05	V
V_{EN-HYS}	Enable voltage hysteresis			0.1		V
INTERNAL LDO (VCC)						
V_{VCC1}	VCC regulation voltage	I_{VCC} = 50mA, R_{FB} = 0Ω or 24.9kΩ	4.5	5	5.5	V
V_{VCC2}	VCC regulation voltage	I_{VCC} = 50mA	7	8	8.5	V
INTERNAL LDO (VDDA)						
V_{VDDA}	VDDA regulation voltage	I_{VDD} = 5mA	4.75	5	5.25	V
$I_{VDDA-CL}$	VDDA short-circuit current limit	V_{DDA} = 4.5V	10	15	20	mA
EXTERNAL BIAS (BIAS)						
$V_{BIAS-TH1}$	V_{IN} to V_{BIAS} switchover rising threshold, 12V fixed or adjustable output	R_{FB} = 49.9kΩ	8.8	9.1	9.3	V
$V_{BIAS-TH2}$	V_{IN} to V_{BIAS} switchover rising threshold, 3.3V or 5V fixed output	R_{FB} = 0Ω or 24.9kΩ	4.3	4.6	4.8	V
$V_{BIAS-HYS}$	V_{IN} to V_{BIAS} switchover hysteresis			550		mV
REFERENCE VOLTAGE (FB)						
V_{FB}	Regulated FB voltage		794	800	806	mV
OUTPUT VOLTAGE (VOUT)						
V_{OUT1}	3.3V output voltage setpoint	R_{FB} = 0Ω	3.267	3.3	3.333	V

5.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT2}	5V output voltage setpoint	R_{FB} = 24.9kΩ	4.95	5.0	5.05	V
V_{OUT3}	12V output voltage setpoint	R_{FB} = 49.9kΩ	11.88	12	12.12	V
ERROR AMPLIFIER (EXTCOMP)						
$g_{m\text{-}EXTERNAL}$	EA transconductance external compensation	FB to COMP	970	1200		µS
$g_{m\text{-}NTERNAL}$	EA transconductance internal compensation (1)	FB to COMP, EXTCOMP 100kΩ to VDDA		30		µS
I_{FB}	Error amplifier input bias current				75	nA
$V_{COMP\text{-}CLAMP}$	COMP clamp voltage	V_{FB} = 0V		2.1		V
$I_{COMP\text{-}SRC}$	EA source current	V_{COMP} = 1V, V_{FB} = 0.65V		170		µA
$I_{COMP\text{-}SINK}$	EA sink current	V_{COMP} = 1V, V_{FB} = 0.95V		170		µA
PULSE FREQUENCY MODULATION (PFM/SYNCIN)						
$V_{IL\text{-}SYNCIN}$	PFM/SYNCIN input threshold low		0.8			V
$V_{IH(SYNCIN)}$	PFM/SYNCIN input threshold high				1.17	V
f_{SYNC1}	Synchronization frequency range (220kHz)	R_{RT} = 100kΩ, ±20 % of the nominal oscillator frequency	176		264	kHz
f_{SYNC2}	Synchronization frequency range (2.2MHz)	R_{RT} = 10kΩ, ±20 % of the nominal oscillator frequency	1.76		2.64	MHz
$t_{SYNC\text{-}TON\text{-}MIN}$	Minimum positive pulse width of external synchronization signal	R_{RT} = 10kΩ			20	ns
$t_{SYNC\text{-}TOFF\text{-}MIN}$	Minimum negative pulse width of external synchronization signal	R_{RT} = 10kΩ			200	ns
$t_{SYNCIN\text{-}SW}$	Delay from PFM falling edge to SW rising edge (1)			35		ns
$t_{PFM\text{-}FILTER}$	SYNCIN to PFM mode		15		75	µs
DUAL RANDOM SPREAD SPECTRUM (DRSS)						
Δf_C	Distance from the switching frequency			8		%
f_m	Modulation frequency			10		kHz
SWITCHING FREQUENCY (SW)						
f_{SW1}	Switching frequency 1	R_{RT} = 100kΩ to AGND	200	220	240	kHz
f_{SW2}	Switching frequency 2	R_{RT} = 49.9kΩ to AGND	400	440	480	kHz
f_{SW3}	Switching frequency 3	R_{RT} = 22.1kΩ to AGND	0.85	0.95	1.05	MHz
f_{SW4}	Switching frequency 4	R_{RT} = 9.09kΩ to AGND	2	2.2	2.4	MHz
$t_{ON\text{-}MIN}$	Minimum on-time(1)			25		ns
$t_{OFF\text{-}MIN}$	Minimum off-time			88	126	ns
POWER GOOD (PG)						
$V_{PG\text{-}UV}$	Power-Good UV trip level	Falling with respect to the regulated voltage	90 %	92 %	94%	
$V_{PG\text{-}OV}$	Power-Good OV trip level	Rising with respect to the regulation voltage	108 %	110 %	112 %	
$V_{PG\text{-}UV\text{-}HYST}$	Power-Good UV hysteresis	Falling with respect to the regulated output		3.4 %		
$V_{PG\text{-}OV\text{-}HYST}$	Power-Good OV hysteresis	Raising with respect to the regulated output		3.4 %		
$t_{PG\text{-}DEGLITCH}$	Power-Good deglitch filter time	V_{OUT} falling or rising		25		µs
$V_{OL\text{-}PG}$	Power-Good voltage	Open collector, I_{PG} = 2mA			0.4	V
SYNCHRONIZATION OUTPUT (SYNCOUT)						
$V_{SYNCOUT\text{-}LTH}$	SYNCOUT low state voltage threshold	R_{CONFIG} = 54.9kΩ or 71.5kΩ, $I_{SYNCOUT}$ = 2mA			0.4	V
$V_{SYNCOUT\text{-}HTH}$	SYNCOUT high state voltage threshold	R_{CONFIG} = 54.9kΩ or 71.5kΩ, $I_{SYNCOUT}$ = −2mA	2.0			V
STARTUP (SOFT START)						
t_{SS}	Internal fixed soft-start time		1.9	2.8	4.4	ms
INTERNAL HICCUP MODE						

5.5 Electrical Characteristics (続き)

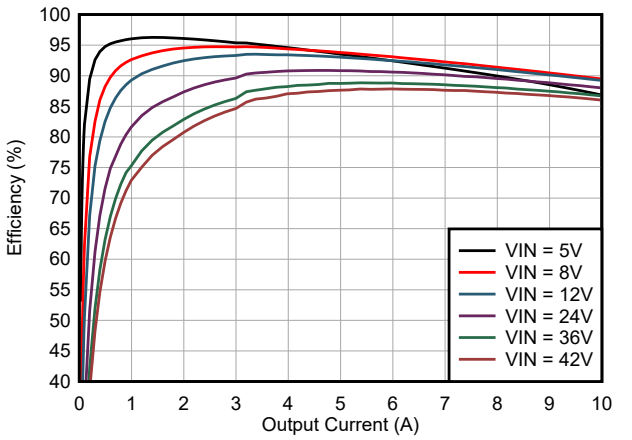
T_J = –40°C to +150°C. Typical values are at T_J = 25°C and V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HIC-DLY}$	HICCUP mode activation delay	$V_{ISNS+} - V_{VOUT}$ > 60mV		512		CYCLES
$t_{HIC-DURATION}$	HICCUP mode fault duration	$V_{ISNS+} - V_{VOUT}$ > 60mV		16384		CYCLES
OVERCURRENT PROTECTION (OCP)						
V_{CS-TH}	CS voltage threshold	Measured from ISNS+ to VOUT	50	56	62	mV
$t_{DELAY-CS}$	CS delay to output			75		ns
G_{CS}	CS amplifier gain (1)			10		V/V
$I_{BIAS-CS}$	CS amplifier input bias current (1)			0.35		µA
$V_{CS-TH-NEG}$	CS negative voltage threshold			30		mV
THERMAL SHUTDOWN (TSD)						
T_{J-SD}	Thermal shutdown threshold (1)	Temperature rising		175		°C
T_{J-HYS}	Thermal shutdown hysteresis (1)			15		°C

(1) Specified by design. Not production tested.

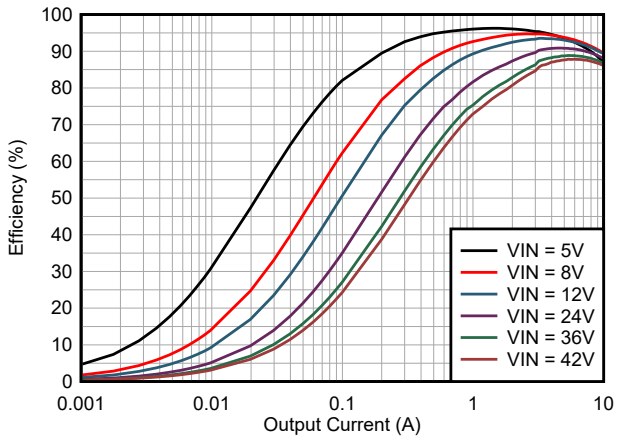
5.6 Typical Characteristics

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.



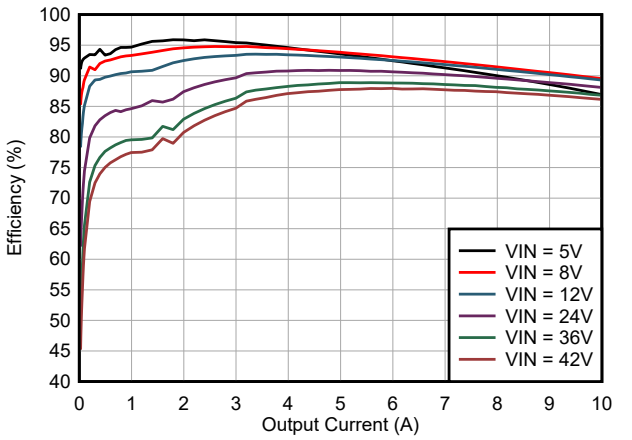
V_{OUT} = 3.3V F_{SW} = 400kHz FPWM

図 5-1. Efficiency vs I_{OUT}, Linear Scale



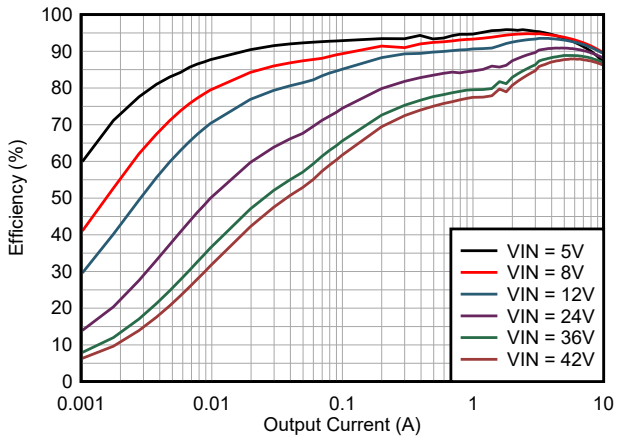
V_{OUT} = 3.3V F_{SW} = 400kHz FPWM

図 5-2. Efficiency vs I_{OUT}, Log Scale



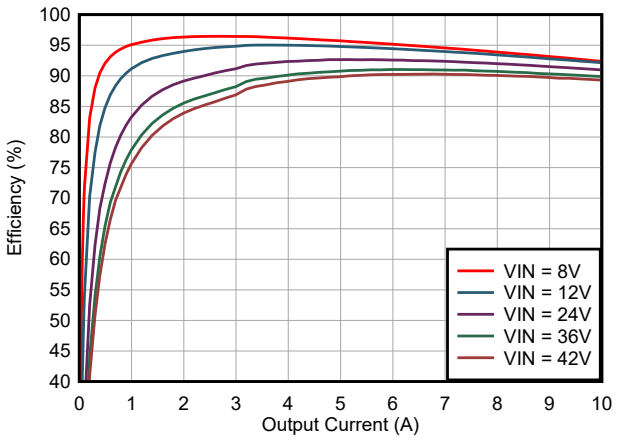
V_{OUT} = 3.3V F_{SW} = 400kHz PFM

図 5-3. Efficiency vs I_{OUT}, Linear Scale



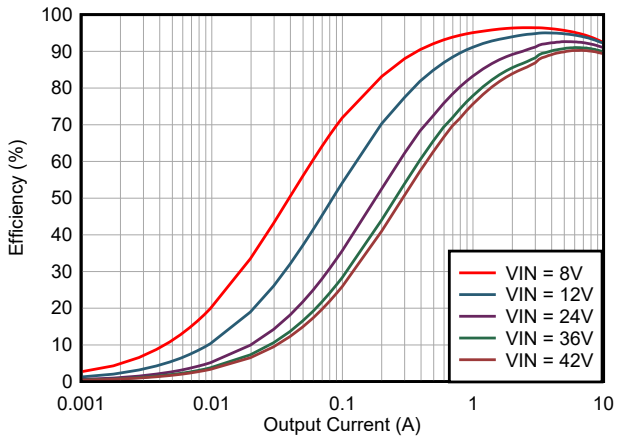
V_{OUT} = 3.3V F_{SW} = 400kHz PFM

図 5-4. Efficiency vs I_{OUT}, Log Scale



BIAS = V_{OUT} = 5V F_{SW} = 400kHz FPWM

図 5-5. Efficiency vs I_{OUT}, Linear Scale

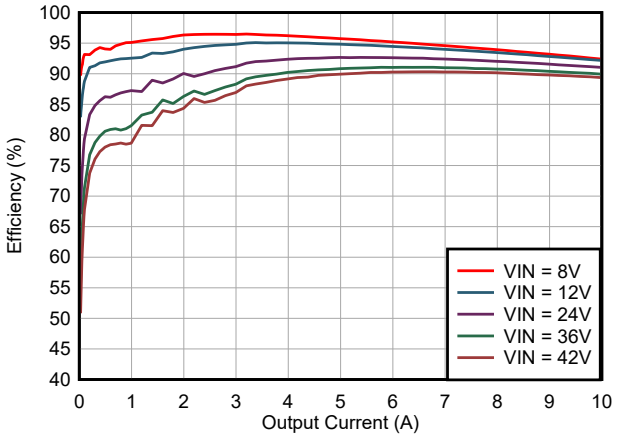


BIAS = V_{OUT} = 5V F_{SW} = 400kHz FPWM

図 5-6. Efficiency vs I_{OUT}, Log Scale

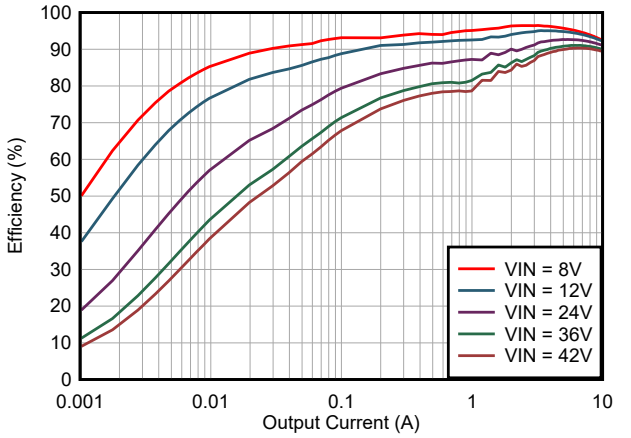
5.6 Typical Characteristics (continued)

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.



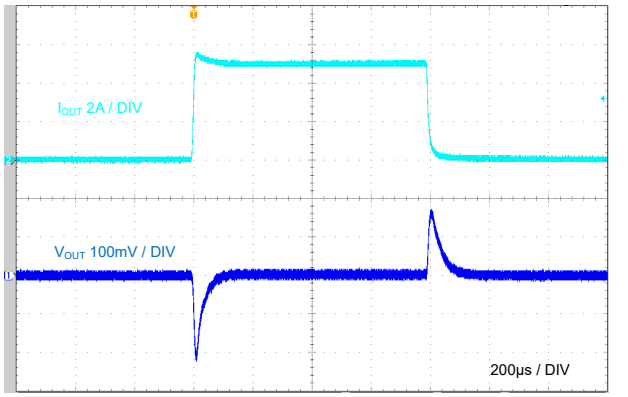
BIAS = V_{OUT} = 5V F_{SW} = 400kHz PFM

図 5-7. Efficiency vs I_{OUT}, Linear Scale



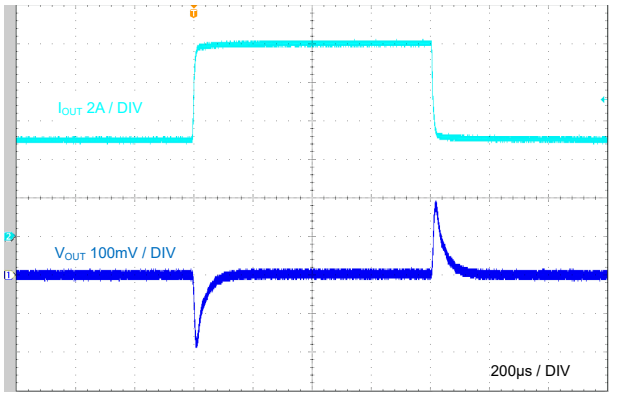
BIAS = V_{OUT} = 5V F_{SW} = 400kHz PFM

図 5-8. Efficiency vs I_{OUT}, Log Scale



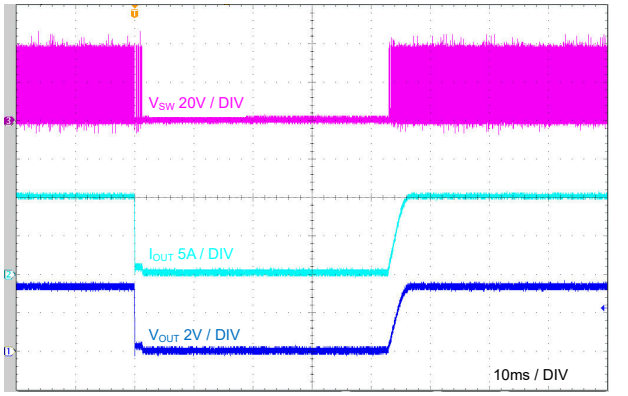
V_{IN} = 36V FPWM
V_{OUT} = 3.3V

図 5-9. Load Transient, 0A to 5A



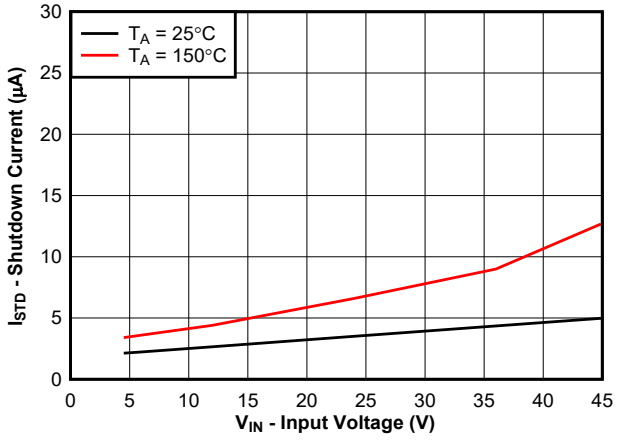
V_{IN} = 36V FPWM
V_{OUT} = 3.3V

図 5-10. Load Transient, 5A to 10A



V_{IN} = 36V I_{OUT} = 10A FPWM
V_{OUT} = 3.3V F_{SW} = 400kHz

図 5-11. Short-Circuit Recovery



V_{EN} = 0V

図 5-12. Shutdown Current vs Input Voltage

5.6 Typical Characteristics (continued)

V_{IN} = 12V, T_J = 25°C, unless otherwise stated.

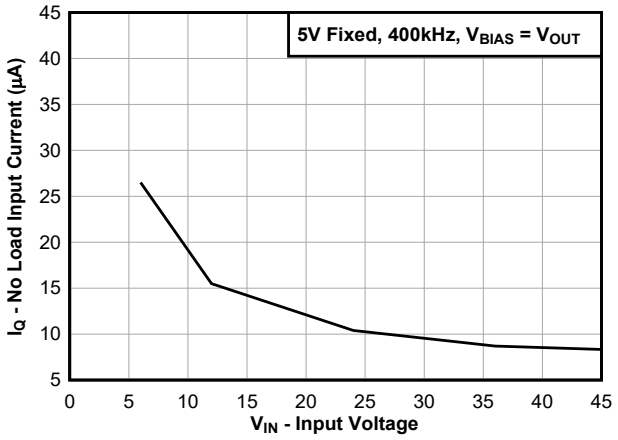


図 5-13. 5V Fixed Output No-Load Active Current vs Temperature

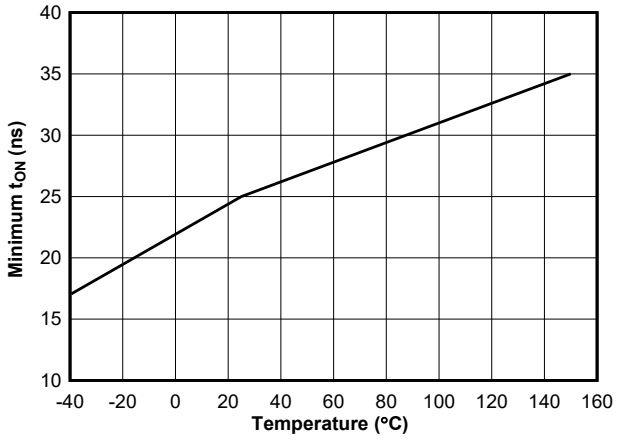


図 5-14. Minimum On-Time vs Temperature

6 Detailed Description

6.1 Overview

The LM704A0-Q1 is a multi-die, DC/DC converters that features high-side and low-side power MOSFETs and a versatile buck controller with all functions necessary to implement a high-efficiency synchronous buck regulator operating over a wide input voltage range from 4.5V to 45V. The LM704A0-Q1 is configured to provide a fixed 3.3V, 5V, or a 12V output, or an adjustable output between 0.8V and 36V.

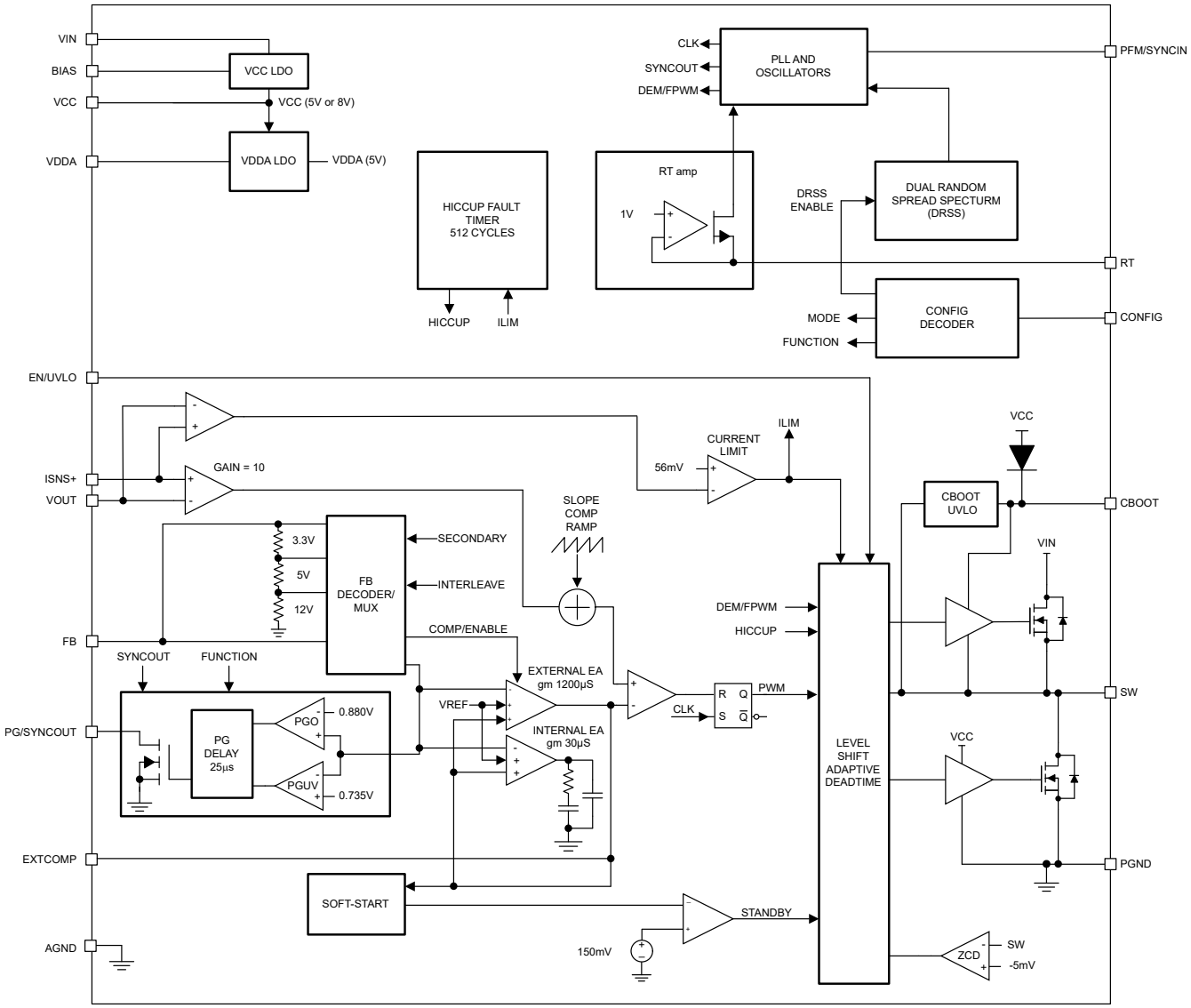
Current-mode control using a shunt resistor provides inherent line feedforward, cycle-by-cycle peak current limiting, and easy loop compensation. The device also supports a wide duty cycle range for high input voltage and low dropout applications as well as when a high-voltage conversion ratio (for example, 10-to-1) is required. The oscillator frequency is user-programmable between 200kHz to 2.2MHz. The LM704A0-Q1 can be synchronized to an external clock applied on the PFM / SYNC pin.

An external bias supply can be connected to the BIAS pin to maximize efficiency in high input voltage applications. A user-selectable diode emulation feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions. Fault protection features include current limiting, thermal shutdown, UVLO and remote shutdown capability.

The LM704A0-Q1 incorporates features to simplify the compliance with various EMI standards including CISPR 25 Class 5 that defines automotive EMI requirements. Dual Random Spread Spectrum (DRSS) technique reduces the peak harmonic EMI signature.

LM704A0-Q1 is provided in a 29-pin QFN package with the exposed VIN, SW, and PGND pads to maximize thermal dissipation.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Voltage Range (V_{IN})

The LM704A0-Q1 operational input voltage range is from 4.5V to 45V. The device is intended for step-down conversions from 12V automotive supply rails. The LM704A0-Q1 uses internal LDOs to provide an 8V or 5V VCC bias rail and a 5V VDDA rail for the gate drive and control circuits.

In high input voltage applications, make sure that the VIN and SW pins do not exceed the absolute maximum voltage rating of 50V during line or load transient events. Voltage excursions that exceed the absolute maximum ratings of these pins can damage the IC. Follow PCB board layout recommendations and use high-quality input bypass capacitors to minimize voltage overshoot and ringing.

As V_{IN} approaches V_{OUT}, the LM704A0-Q1 skips t_{OFF} cycles to allow the controller to extend the duty cycle up to approximately 99%. Refer to 図 6-1.

When in dropout, the output voltage tracks the input voltage and the peak current mode control is open loop. As a result, larger output voltage perturbations due to line and load transients are possible. Additional output capacitance and more aggressive external compensation can improve the output response.

Use 式 1 to calculate when the LM704A0-Q1 enters dropout mode.

$$V_{IN} = V_{OUT} \times \left(\frac{t_P}{t_P - t_{OFF}}\right) \quad (1)$$

- t_P is the oscillator period
- t_{OFF} is the minimum off time, typical 88ns

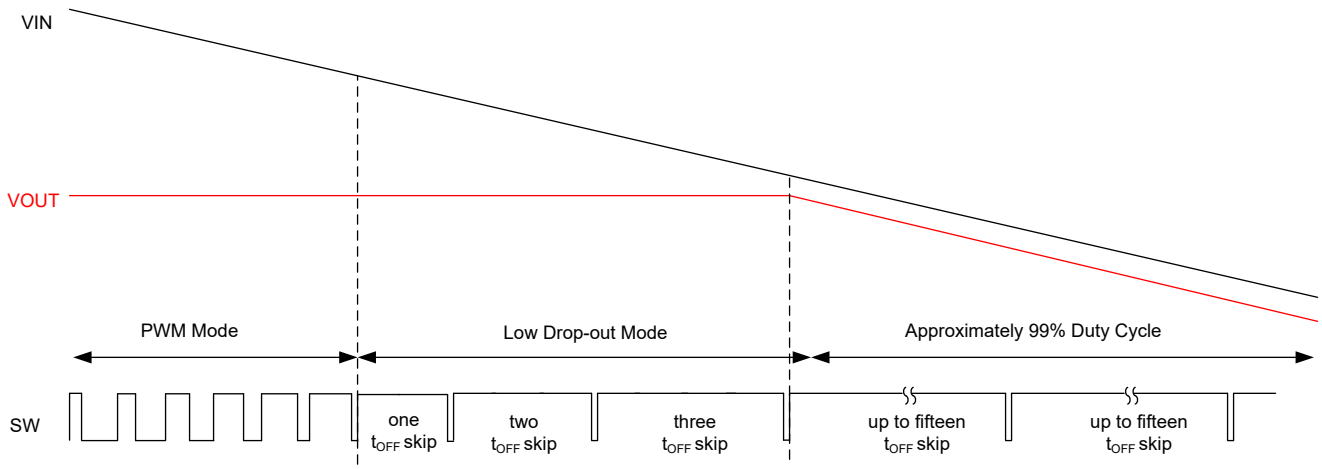


図 6-1. Dropout Mode Operation

6.3.2 High-Voltage Bias Supply Regulator (VCC, BIAS, VDDA)

The LM704A0-Q1 contains an internal high-voltage VCC bias regulator that provides the bias supply for the gate drivers for the power MOSFETs. The input voltage pin (VIN) can be connected directly to an input voltage source up to 45V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks VIN minus a small voltage drop.

If configured for a 3.3V fixed output, the VCC bias regulator output voltage is 5V to allow connecting the BIAS pin to an external supply from 5V to 30V. Similarly, if configured for a 5V fixed output, the VCC bias regulator output voltage is 5V to allow connecting the BIAS pin to the VOUT node or an external supply from 5V to 30V. For a 12V fixed output or an adjustable output, the VCC bias regulator output voltage is 8V to allow connecting the BIAS pin to the VOUT node or an external supply from 10V to 30V.

At power up, the VCC regulator sources current into the capacitor connected to the VCC pin (if EN pin is connected to a voltage greater than 2V). When the VCC voltage exceeds 4.3V, the output is enabled and the soft-start sequence begins. The output remains active unless the VCC voltage falls below the VCC falling UVLO threshold of 4V (typical) or the EN is driven below 900mV (typical). TI recommends that a 4.7µF capacitor is connected from the VCC pin to PGND and placed as close as possible to the device pins.

Internal power dissipation of the VCC regulator can be minimized by connecting the BIAS pin to VOUT or an external supply. If the BIAS voltage is above 9.1V (typical), the input to the VCC regulator switches over from VIN to BIAS. If configured for a 3.3V fixed or a 5V fixed output, the switchover happens at 4.6V (typical). Tie the BIAS pin to AGND if unused. Never connect the BIAS pin to a voltage greater than 32V. If an external supply is connected to the BIAS pin to power the LM704A0-Q1, V_{IN} must be greater than the external bias voltage under all conditions to avoid damage to the device.

An internal 5V linear regulator generates the VDDA bias supply from the VCC bias supply. Bypass VDDA with a 100nF ceramic capacitor to achieve a low-noise internal bias rail. Normally VDDA is 5V, however when configured for a fixed 3.3V or a fixed 5V VOUT, the VDDA regulator is disabled in sleep mode while the circuitry, normally powered by the VDDA, is switched over to VOUT as the power source.

6.3.3 Enable (EN)

The EN/UVLO pin can be connected to a voltage as high as 45V. The LM704A0-Q1 has a precision enable. When the EN pin is greater than 1V, the output is enabled. If the EN pin is pulled below 0.55V (typical), the LM704A0-Q1 is in shutdown with an I_Q of 2.3µA (typical) current draw from V_{IN}. When the enable voltage is between 0.55V (typical) and 1V (typical), the LM704A0-Q1 is in standby mode. When in standby mode, the VCC regulator is enabled, the device is not switching, and the I_Q current is 350µA (typical). Users can also enable the LM704A0-Q1 with standard CMOS logic drivers. A voltage greater than 2.0V enables the LM704A0-Q1, and a voltage less than 0.4V disables the LM704A0-Q1. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in 図 6-2 to establish a precision UVLO threshold. TI recommends setting the input voltage turn-on threshold at 4.5V or higher when the rise time of the input supply to the LM704A0-Q1 is significantly slower than the internal soft-start time. TI does not recommend leaving the EN pin floating.

Use 式 2 to calculate the UVLO resistors given the required input turn-on voltage. The EN voltage hysteresis, V_{EN-HYS}, is 100mV or 10% of the EN voltage rising threshold, V_{EN-TH}, therefore the input turn-off voltage is 90% of the input turn-on voltage.

$$R_{UV1} = \left(\frac{V_{IN(on)}}{V_{EN-TH}} - 1 \right) \times R_{UV2} \quad (2)$$

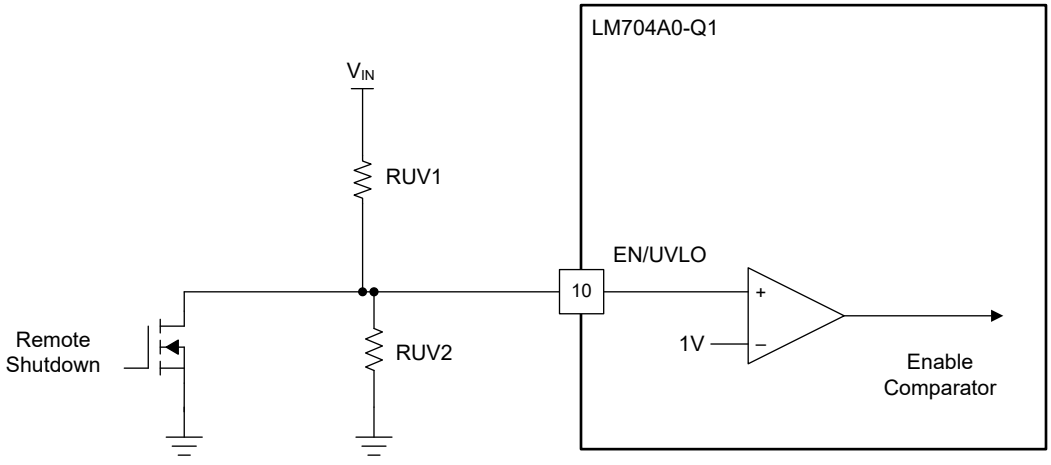


図 6-2. Programmable Input Voltage UVLO Turn-on and Turn-off

6.3.4 Power-Good Monitor (PG)

The LM704A0-Q1 includes an output voltage monitoring signal for V_{OUT} to simplify sequencing and supervision. The power-good function can be used to enable circuits that are supplied by the corresponding voltage rail or to turn on sequenced supplies. The power-good output (PG) switches to a high impedance open-drain state when the output voltage is in regulation. The PG output switches low when the corresponding output voltage drops below the lower power-good threshold (92% typical) or rises above the upper power-good threshold (110% typical). If the upper PG threshold is exceeded when operating in standalone configuration mode, the high-side switch is turned off immediately and the low-side switch is turn on to prevent overvoltage and discharge the output. A 25µs deglitch filter prevents false tripping of the power-good signal during transients. TI recommends a pull-up resistor of 100kΩ (typical) from PG to the relevant logic rail. PG is asserted low during soft-start and when the buck regulator is disabled via the EN input.

When the LM704A0-Q1 is configured as a primary device, the PG pin is converted to a synchronization clock output for the secondary device. The synchronization signal has logic levels and is 180° out of phase (lagging) with the internal high-side gate driver output of the primary device.

6.3.5 Switching Frequency (RT)

The LM704A0-Q1 oscillator is programmed by a resistor between RT and AGND to set an oscillator frequency between 200kHz and 2.2MHz. Calculate the RT resistance for a given switching frequency using 式 3.

$$R_{RT}[k\Omega] = \frac{\frac{10^6}{F_{SW}[kHz]} - 53}{45} \quad (3)$$

Under low V_{IN} conditions when the high-side MOSFET on-time exceeds the programmed oscillator period, the LM704A0-Q1 extends the switching period of that channel until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage. In such an event, the oscillators operate independently and asynchronously until the channel can maintain output regulation at the programmed frequency.

The approximate input voltage level where this occurs is given by 式 4, where t_{SW} is the switching period and $t_{OFF(min)}$ is the minimum off-time of 88ns.

$$V_{IN(min)} = V_{OUT} \times \left(\frac{t_{SW}}{t_{SW} - t_{OFF(min)}} \right) \quad (4)$$

6.3.6 Dual Random Spread Spectrum (DRSS)

The LM704A0-Q1 provides a Dual Random Spread Spectrum (DRSS) function which reduces the EMI of the power supply over a wide frequency range. The DRSS function combines a low-frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in the lower radio frequency bands, while the high frequency random modulation improves performance in the higher radio frequency bands.

Spread spectrum works by converting a narrowband signal into a wideband signal which spreads the energy over multiple frequencies. Industry standards require different spectrum analyzer resolution bandwidth (RBW) settings for different frequency bands. The RBW has an impact on the spread spectrum performance. For example, the CISPR-25 requires 9kHz RBW for the 150kHz to 30MHz frequency band. For frequencies greater than 30MHz, the required RBW is 120kHz. DRSS is able to simultaneously improve the EMI performance in the high and low RBWs with the low-frequency triangular modulation and high-frequency cycle-by-cycle random modulation as shown in 図 6-3. In the low-frequency band (150kHz -30MHz), the DRSS function can reduce the conducted emissions by as much as 15dBµV, and in the high-frequency band (30MHz - 108MHz) by as much as 5dBµV.

The DRSS function can be enabled by connecting either a 41.2kΩ or 71.5kΩ resistor from the CONFIG pin to AGND. The DRSS function is disabled when an external clock is applied to the PFM / SYNCIN pin.

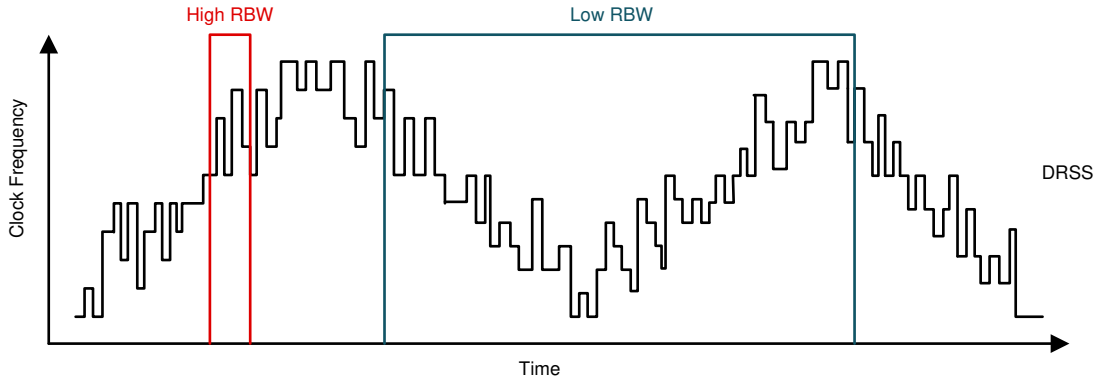


図 6-3. Dual Random Spread Spectrum Implementation

6.3.7 Soft Start

The LM704A0-Q1 has an internal 2.8ms soft-start timer (typical). The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

6.3.8 Output Voltage Setpoint (FB)

The LM704A0-Q1 outputs can be independently configured for one of the three fixed output voltages with no external feedback resistors, or adjusted to the desired voltage using an external resistor divider network. The output can be configured as a 3.3V output by connecting the FB pin to VDDA, a 5V output by connecting FB through a 24.9kΩ resistor to VDDA, or 12V by connecting the FB pin through a 49.9kΩ resistor to VDDA. With the output voltage selection, the VCC bias regulator output level is selected as well as shown in 表 6-1. The configuration settings are latched and cannot be changed until the input voltage to the LM704A0-Q1 is recycled.

表 6-1. Output Voltage and VCC Voltage Selection

FB Pin	Output Voltage	VCC Voltage
Short to VDDA	3.3V	5V
24.9kΩ to VDDA	5.0V	5V
49.9kΩ to VDDA	12V	8V
Resistor divider to VOUT	0.8V to 55V	8V

Alternatively, the output voltage can be set using external resistive dividers from the output to the FB pin. The output voltage adjustment range is between 0.8V and 36V. The voltage reference setpoint is 0.8V (V_{REF}). Use 式 5 to calculate the upper and lower feedback resistors, designated R_{FB1} and R_{FB2} respectively.

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_{FB2} \quad (5)$$

The recommended starting value for R_{FB2} is between 10kΩ and 20kΩ.

If a low I_Q mode is required, be careful when selecting the external resistors. The extra current drawn from the external divider is added to the LM704A0-Q1 $I_{Q\text{-}SLEEP}$ current. The divider current reflected to V_{IN} is divided down by the ratio of V_{OUT}/V_{IN}.

6.3.9 Minimum Controllable On-Time

There are two limitations to the minimum output voltage adjustment range: the LM704A0-Q1 voltage reference of 0.8V and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio V_{OUT}/V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy 式 6.

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \times F_{SW} \quad (6)$$

where

- $t_{ON(min)}$ is 25ns (typical).
- F_{SW} is the switching frequency.

If the desired voltage conversion ratio does not meet the above condition, the LM704A0-Q1 transitions from a fixed switching frequency operation mode to a pulse-skipping mode to maintain output voltage regulation.

For wide V_{IN} applications and low output voltages, an alternative is to reduce the LM704A0-Q1 switching frequency to meet the requirement of 式 6.

6.3.10 Error Amplifier and PWM Comparator (FB, EXTCOMP)

The LM704A0-Q1 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the feedback voltage and an internal precision reference (0.8V). The control loop compensation can be configured in two ways. The first is using the internal compensation amplifier, which has a gain of 30µS. To use the internal compensation network connect the EXTCOMP through a 100kΩ resistor to the VDDA pin. If a 100kΩ resistor is not detected, the LM704A0-Q1 defaults to the external loop compensation network. The external loop compensation network is latched and cannot be re-configured easily. When using the external compensation network, the gain of the transconductance amplifier is 1200µS. Typically if higher performance is required to meet a stringent transient response requirement, TI advises to use external compensation configuration. To re-configure the compensation (internal or external) power must be recycled and VCC must be allowed to drop below the VCC_{UVLO} threshold.

TI generally recommends a type-II compensation network for peak current-mode control. If no external compensation impedance is detected on power up, the fixed internal compensation network is used.

6.3.11 Slope Compensation

The LM704A0-Q1 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor downslope using 式 7.

$$L_{O(sc)} = \frac{V_{OUT}[V] \times R_S[m\Omega]}{24 \times F_{SW}[MHz]} \quad (7)$$

- A lower inductance value increases the peak-to-peak inductor current, which typically minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value decreases the peak-to-peak inductor current, which typically increases the full-load efficiency by reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

6.3.12 Shunt Current Sensing

図 6-4 illustrates inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For excellent current sense accuracy and overcurrent protection, use a low inductance ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM704A0-Q1 current sense amplifier.

If the peak differential current signal sensed from ISNS+ to VOUT exceeds the current limit threshold of 56mV, the current limit comparator immediately terminates the high-side gate driver output for cycle-by-cycle current limiting. Calculate the shunt resistance using 式 8.

$$R_S = \frac{V_{CS(TH)}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \quad (8)$$

where

- $V_{CS(TH)}$ is current sense threshold of 56mV.
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients.
- ΔI_L is the peak-to-peak inductor ripple current.

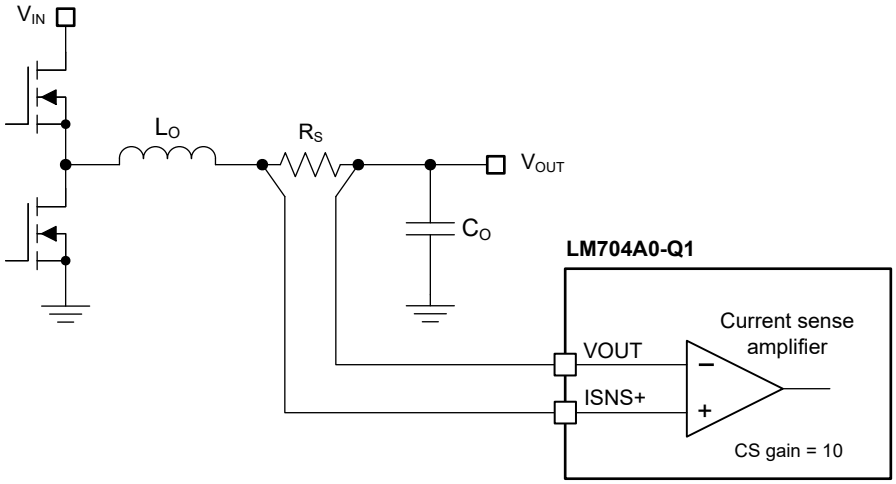


図 6-4. Shunt Current Sensing Implementation

The typical current sense delay ($t_{DELAY(CS)}$) is 75ns. Calculate the resultant inductor current overshoot above the overcurrent threshold using 式 9.

$$I_{L(overshoot)} = \frac{(V_{IN} - V_{OUT}) \times t_{DELAY(CS)}}{L_O} \quad (9)$$

The respective SS voltage is clamped 150mV above FB during an overcurrent condition. 16 overcurrent events must occur before the SS clamp is enabled. This requirement make sure that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

6.3.13 Hiccup Mode Current Limiting

The LM704A0-Q1 includes an internal hiccup mode protection function. When an overload condition occurs, a 512-cycle counter starts counting consecutive cycle-by-cycle current limit incidents after the internal soft-start sequence is completed. The 512-cycle counter is reset if four consecutive switching cycles occur without exceeding the current limit threshold. If V_{FB} > 400mV after 512-cycle counts are completed, the counter is restarted. When V_{FB} < 400mV and 512-cycle counts are completed, the internal soft-start output is pulled low and the internal high-side and low-side drivers are disabled. Then, a 16384 counter is enabled. After the counter reaches 16384, the internal soft-start circuit is enabled, and the output re-starts. Note: the Hiccup mode current limit is not enabled during the soft-start time and until the feedback voltage exceeds 0.4V.

6.3.14 Device Configuration (CONFIG)

The LM704A0-Q1 can be configured for operation in Standalone Mode (single device) or for operation in single output interleaved mode (two devices) for paralleling the outputs of two devices for high-current applications. When operating in interleaved mode, one of the two devices has to be configured as a primary device while the other device has to be configured as a secondary device. There is also the option to enable or disable the DRSS function as detailed in 表 6-2.

During device startup, the CONFIG pin is sampled and latched. The configuration cannot be changed "on the fly". The LM704A0-Q1 input voltage must be recycled or EN pin toggled before the device can be reconfigured. 図 6-5 shows the configuration timing diagram.

When the DRSS function is enabled, the LM704A0-Q1 cannot be synchronized to an external clock.

表 6-2. Configuration Modes

R_{CONFIG}	Mode	Function	DRSS
29.4kΩ	Standalone	N/A	Disabled
41.2kΩ	Standalone	N/A	Enabled
54.9kΩ	Interleaved	Primary	Disabled
71.5kΩ	Interleaved	Primary	Enabled
90.9kΩ	Interleaved	Secondary	N/A

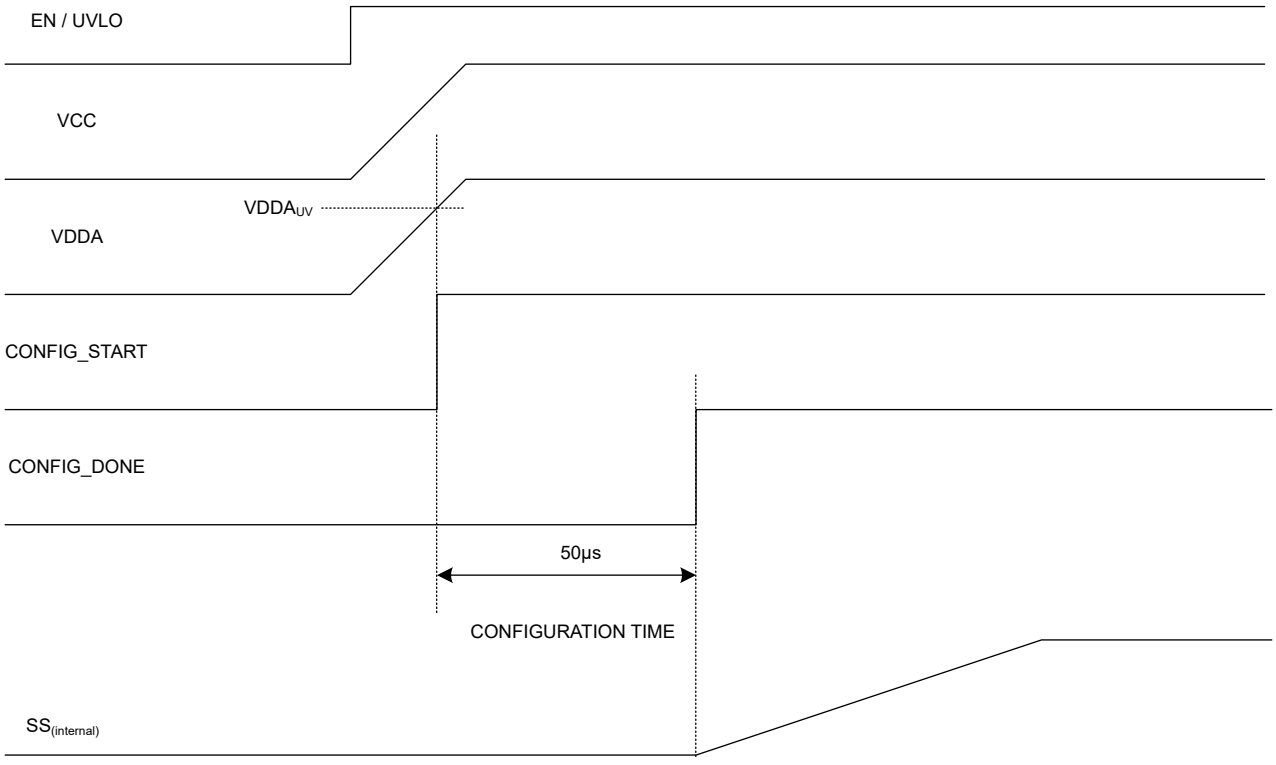


図 6-5. Configuration Timing

6.3.15 Single-Output Dual-Phase Operation

For single-output, dual-phase operation, two LM704A0-Q1 devices are required. Additional phases cannot be added. Configure the first device as a primary and the second device as a secondary per 表 6-2. This action disables the feedback error amplifier of the secondary device and places feedback error amplifier into a high-impedance state. Connect EXTCOMP pins of the primary and secondary devices together with minimal trace length. Add an external compensation network near the primary device. Internal compensation feature is not supported when operating in dual-phase configuration. The PG / SYNCOUT pin of the primary device must be connected to the PFM / SYNCIN pin of the secondary device. The SYNCOUT of the primary device is 180° out-of-phase and facilitates the interleaved operation. RT pin is not used for the oscillator when the LM704A0-Q1 is configured as a secondary device but instead is used for the slope compensation. RT resistance on the secondary device needs to be the same value as RT resistance on the primary device to make sure of correct operation. The oscillator frequency is derived from the primary device. When operating in Interleaved mode, both devices need to be enabled at the exact same time for start-up. After the regulator has started, pull the secondary EN pin low (< 0.8V) for phase shedding if needed at light load to increase the efficiency.

Configure PFM mode by connecting both the PFM/SYNC pin of the primary and the FB pin of the secondary to the VDDA pin as shown in 図 6-6.

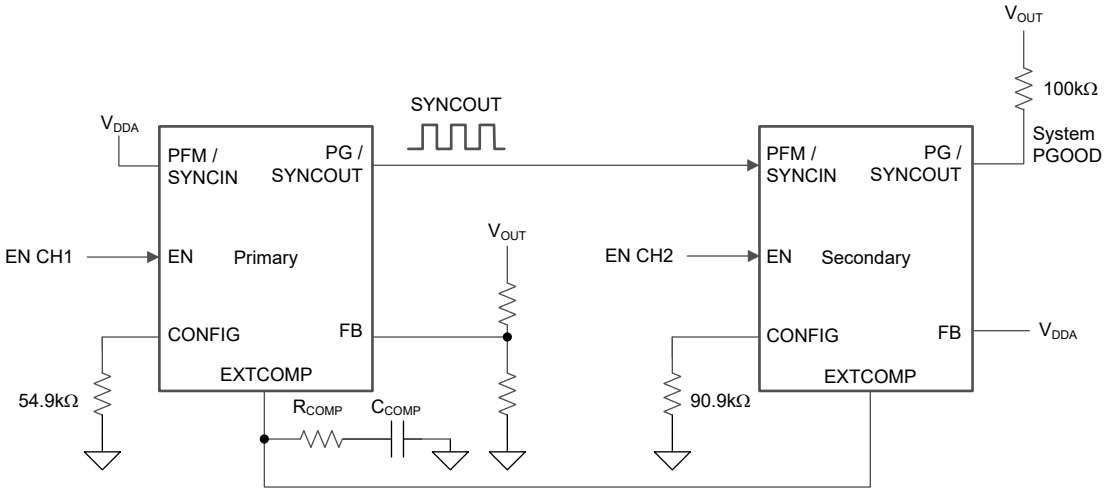


図 6-6. Simplified Schematic for Single-Output Dual-Phase Operation in PFM Mode

Configure FPWM mode by applying an external synchronization signal to the PFM/SYNCIN pin of the primary or connecting the pin to the AGND and connecting the FB pin of the secondary to the AGND pin as shown in 図 6-7.

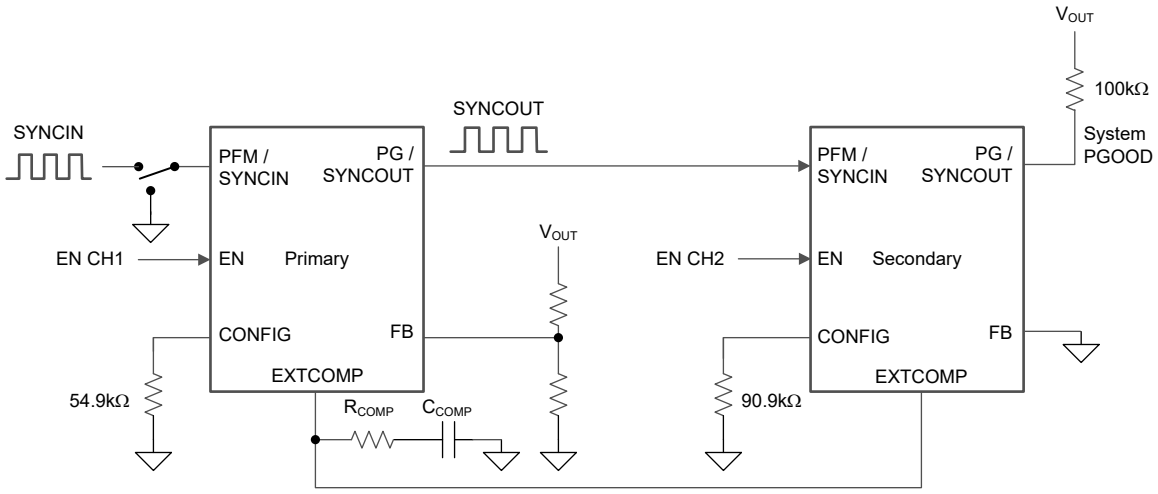


図 6-7. Simplified Schematic for Single-Output Dual-Phase Operation in FPWM Mode

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While in interleaved mode, if an external SYNCIN signal is applied after the start-up, there is a 2 clock cycle delay before the LM704A0-Q1 locks onto the external sync signal.

In PFM mode, while the primary device is pulse skipping to reduce the $I_{Q\text{-}SLEEP}$ current, the primary device disables the synchronization clock output, therefore the phase shedding is not supported. Phase shedding is only supported in FPWM.

When operating in PFM mode under light load conditions, either primary device or secondary device or both devices can switch.

In FPWM mode, the secondary device can be disabled to reduce the $I_{Q\text{-}SLEEP}$ current, and then the device can be enabled to support higher load currents when needed. When the secondary device enable is recycled the internal soft-start is pulled low, and then the LM704A0-Q1 goes through a normal soft-start turn-on. During the secondary soft-start time (2.8ms typical) there is a phase current imbalance until the soft-start is done. The phase current imbalance is also possible when in dropout as there is no control over the current. Matching the impedance of the outputs of the primary and secondary devices minimizes the phase current imbalance.

For more information, see *Benefits of a Multiphase Buck Converter* and *Multiphase Buck Design From Start to Finish.*

6.3.16 Pulse Frequency Modulation (PFM) / Synchronization

The LM704A0-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation (DEM), the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss during light load operation. Note: configuring the device for DEM has an effect of slower response to load transients during light load operation.

The diode emulation feature is configured with the PFM / SYNCIN pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect PFM / SYNCIN to VDDA. Note that diode emulation is automatically engaged to prevent reverse current flow during a prebias start-up in PFM. During start up, when the output voltage approaches the regulation set point a gradual change from DCM to CCM occurs, preventing the output voltage overshoot.

If forced pulse-width modulation (FPWM) or continuous conduction mode (CCM) operation is desired, tie PFM / SYNCIN to AGND. Note that the LM704A0-Q1 transitions from PFM to FPWM mode whenever LM704A0-Q1 is reset. The time to transition to FPWM operation is dependent on the output load current. In a typical application,

the transition from PFM to FPWM operation occurs in less than 1ms if the output current is greater than 100mA. Similarly, for the output currents of around 1mA, the transition generally occurs in tens of milliseconds.

To synchronize the LM704A0-Q1 to an external source, apply a logic-level clock (greater than 1.17V) to the PFM / SYNCIN pin. The LM704A0-Q1 can be synchronized to ±20% of the programmed frequency up to a maximum of 2.2MHz. If there is an RT resistor and a synchronization signal, the LM704A0-Q1 ignores the RT resistor and synchronizes to the external clock. Under low V_{IN} conditions when the minimum off-time is reached, the synchronization signal is ignored, allowing the switching frequency to be reduced to maintain output voltage regulation.

When in FPWM mode, the time for the LM704A0-Q1 to be synchronized to an external clock frequency is approximately 100µs. If an external clock is applied after startup while operating in PFM mode, the time to synchronize the switching frequency is dependent on the load. In a typical application, switch synchronization and FPWM operation occurs in less than 1ms if the output current exceeds 100mA. Similarly, for the output currents of around 1mA, the synchronization generally occurs in tens of milliseconds.

6.3.17 Thermal Shutdown (TSD)

The LM704A0-Q1 includes an internal junction temperature monitor that operates while the device is in active mode. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs.
2. Pulls SS and PG pins low.
3. Turns off the VCC regulator.
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical).

This protection is a non-latching protection, therefore, the device cycles into and out of thermal shutdown if the fault persists.

6.4 Device Functional Modes

6.4.1 Shutdown Mode

The EN / UVLO pin provides ON / OFF control for the LM704A0-Q1. When V_{EN} is below 0.55V (typical), the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 2.3µA (typical). The LM704A0-Q1 also includes undervoltage (UV) protection of the internal bias LDO. If the internal bias supply voltage is below the UV threshold level, the switching regulator remains off.

6.4.2 Standby Mode

The internal bias LDO has a lower enable threshold than the switching regulator. When V_{EN} is above 0.55V (typical) and below the precision enable threshold of 1V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on if the LDO output is above the bias rail UV threshold. The switching and output voltage regulation are disabled in standby mode.

6.4.3 Active Mode

The LM704A0-Q1 is in active mode when V_{EN} is above the precision enable threshold and the internal bias rail is above the UV threshold level. In active mode, the device operates in one of two modes depending on the load current, input voltage, output voltage, and PFM / SYNCIN pin configuration:

1. Forced pulse width modulation (FPWM) mode. This mode of operation is configured by tying the PFM / SYNCIN pin to GND or driving with an external clock source. The device operates in continuous conduction mode (CCM) with fixed switching frequency regardless of the load current.
2. Pulse frequency modulation (PFM) mode. This mode of operation is configured by tying the PFM / SYNCIN pin to VDDA. The device operates in discontinuous conduction mode (DCM) if the load current is less than half of the peak-to-peak inductor current, otherwise the device operates in continuous conduction mode (CCM). The transition between CCM and DCM is automatic.

6.4.4 Sleep Mode

The LM704A0-Q1 operates with peak current-mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the compensation voltage goes low and the switching is stopped. When the LM704A0-Q1 controller detects 16 missed switching cycles, the LM704A0-Q1 controller enters sleep mode and switches to a low $I_{Q\text{-}SLEEP}$ state to reduce the current drawn from the input. For the LM704A0-Q1 to go into sleep mode, the device must be programmed for PFM mode.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The following section discuss the output inductor, input and output capacitors, and EMI input filter.

7.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Choose the inductance using 式 10 based on a peak inductor current given by 式 11.

$$L_O = \frac{V_{OUT}}{\Delta I_L \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

$$I_{L(PK)} = I_{OUT} + \frac{\Delta I_L}{2} \quad (11)$$

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as the core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

7.1.1.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that given by 式 12.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times F_{SW} \sqrt{\Delta V_{OUT}^2 + \left(R_{ESR} \times \Delta I_L\right)^2}} \quad (12)$$

図 7-1 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

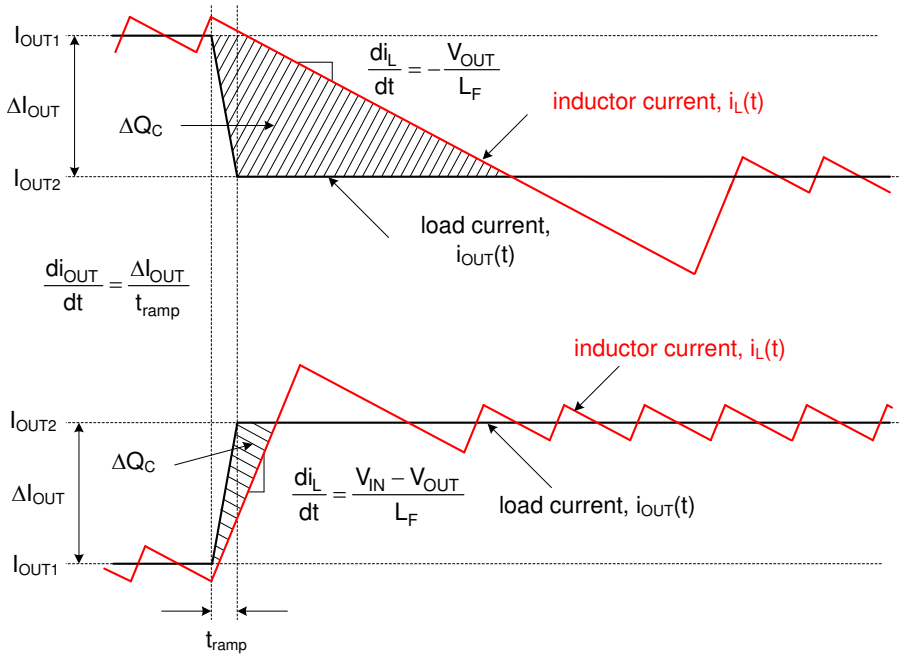


図 7-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12V input to low output voltage (for example, 3.3V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below the nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2} \quad (13)$$

The ESR of a capacitor is provided in the manufacturer data sheet either explicitly as a specification or implicitly in the impedance vs frequency curve. Depending on type, size and construction, electrolytic capacitors have significant ESR, 5mΩ and above, and relatively large ESL, 5nH to20 nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in 式 12 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Two to four 47µF, 10V, X7R capacitors in 1206 or 1210 footprint is a common choice for a 5V output. Use 式 13 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with the low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with the large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

7.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. The input capacitor RMS current for a single-channel buck regulator is given by 式 14.

$$I_{CIN(rms)} = \sqrt{D \times \left(I_{OUT}^2 \times (1 - D) + \frac{{\Delta I_L}^2}{12} \right)} \tag{14}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors must be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sinks I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by 式 15.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \tag{15}$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by 式 16.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} \tag{16}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and two 4.7µF X7R ceramic decoupling capacitors are usually sufficient for most applications. Select the input bulk capacitor based on the ripple current rating and operating temperature range.

Of course, a two-channel buck regulator with 180° out-of-phase interleaved switching provides input ripple current cancellation and reduced input capacitor current stress. The above equations represent valid calculations when one output is disabled and the other output is fully loaded.

7.1.1.4 EMI Filter

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^2}{P_{IN}} \right| \tag{17}$$

The EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- Input filter inductor L_{IN} is usually selected between 1µH and 10µH, but can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

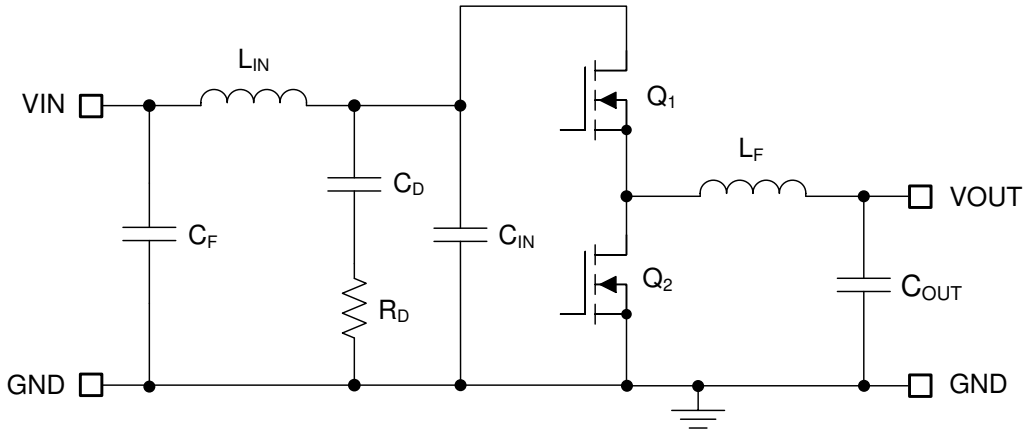


図 7-2. Buck Regulator With π-Stage EMI Filter

By calculating the first harmonic current from the fourier series of the input current waveform and multiplying the result by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by 式 18.

$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \times F_{SW} \times C_{IN}} \times \sin(\pi \times D_{MAX}) \times \frac{1}{1\mu V}\right) - V_{MAX} \tag{18}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification, for example CISPR 25 Class 5.
- C_{IN} is the existing input capacitance of the buck regulator.
- D_{MAX} is the maximum duty cycle.
- I_{PEAK} is the peak inductor current.

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from 式 19.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \times F_{SW}}\right)^2 \tag{19}$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. The resonant frequency of the filter is given by 式 20.

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_{IN} \times C_F}} \tag{20}$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by 式 21.

$$C_D \geq 4 \times C_{IN} \tag{21}$$

Select the damping resistor R_D using 式 22.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{22}$$

7.1.2 Error Amplifier and Compensation

A Type-II compensator using a transconductance error amplifier (EA) is shown in 図 7-3. The dominant pole of the EA open-loop gain is set by the EA output resistance, R_{OEA}, and effective bandwidth-limiting capacitance, C_{BW} as shown by 式 23.

$$G_{EA(openloop)}(s) = -\frac{g_m \cdot R_{O\text{-}EA}}{1 + s \cdot R_{O\text{-}EA} \cdot C_{BW}} \tag{23}$$

$$G_{EA(openloop)}(s) = -\frac{g_m \times R_{OEA}}{1 + s \times R_{OEA} \times C_{BW}} \tag{24}$$

The EA high-frequency pole is neglected in the above expression. The compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network, is calculated in 式 25.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \times \frac{g_m \times R_{OEA} \times \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \times \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{25}$$

where

- V_{REF} is the feedback voltage reference of 0.8V
- g_m is the EA gain transconductance of 1200µS
- $R_{O\text{-}EA}$ is the error amplifier output impedance of 64MΩ

$$\omega_{z1} = \frac{1}{R_{COMP} \times C_{COMP}} \tag{26}$$

$$\omega_{p1} = \frac{1}{R_{OEA} \times (C_{COMP} + C_{HF} + C_{BW})} \cong \frac{1}{R_{OEA} \times C_{COMP}} \tag{27}$$

$$\omega_{p2} = \frac{1}{R_{COMP} \times (C_{COMP} \,||\, (C_{HF} + C_{BW}))} \cong \frac{1}{R_{COMP} \times C_{HF}} \quad (28)$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, R_{COMP} << $R_{O\text{-}EA}$ and C_{COMP} >> C_{BW} and C_{HF}, so the approximations are valid. 図 7-3 circles the poles in red and the zero in blue.

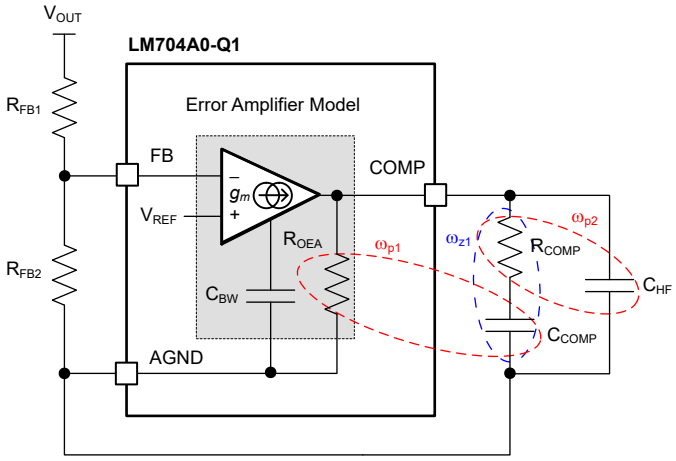


図 7-3. Error Amplifier and Compensation Network

7.1.3 Maximum Ambient Temperature

As with any power conversion device, the LM704A0-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient temperature. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$, of the device
- PCB layout

The maximum internal die temperature for the LM704A0-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 29 shows the relationships between the important parameters. Larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the LM704A0-Q1 Quickstart Calculator tool. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}} \quad (29)$$

where

- η = efficiency
- T_A = ambient temperature
- T_J = junction temperature
- $R_{\theta JA}$ = the effective thermal resistance of the IC junction to the air, mainly through the PCB

The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics* application report, the JESD 51-7 value of $R_{\theta JA}$ given in Thermal Information is not valid for design purposes and must not be used to estimate the thermal performance of the device in a real application. The JESD 51-7 values reported in Thermal Information were measured under a specific set of conditions that are rarely obtained in an actual application.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors. The following are the most critical parameters:

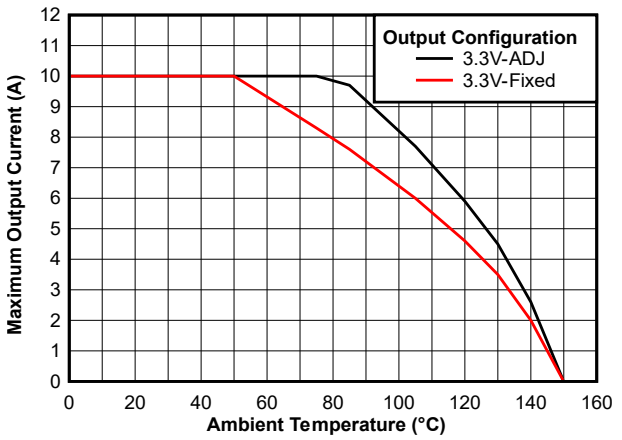
- Power dissipation
- Air temperature
- Airflow
- PCB area
- Copper heat-sink area
- Number of thermal vias under or near the package
- Adjacent component placement

Typical curves of maximum output current versus ambient temperature are shown in *Derating Curves* for a good thermal layout.

Use *Thermal Design Resources* as a guide for thermal PCB design and estimating $R_{\theta JA}$ for a given application environment.

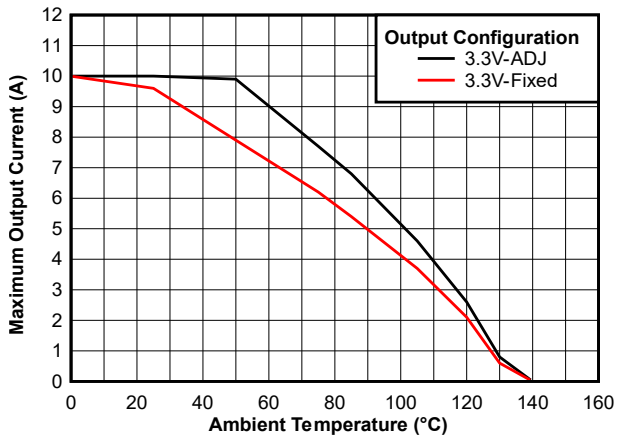
7.1.3.1 Derating Curves

The data in this section was taken on the LM706A0QEVM evaluation board with a device and PCB combination, giving an $R_{\theta JA}$ of about 19°C/W. Note that the data given in these graphs are for illustration purposes only and the actual performance in any given application depends on all of the previously mentioned factors.



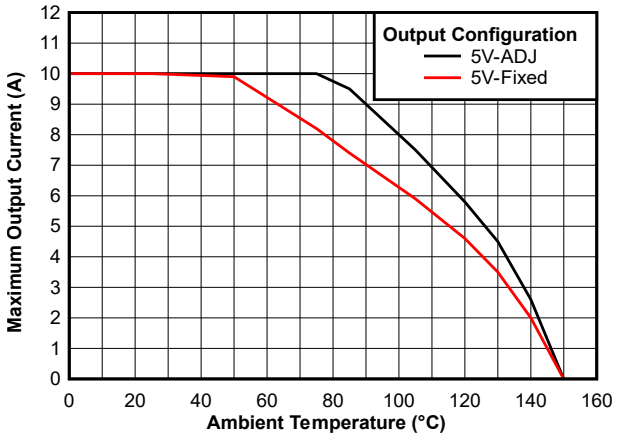
V_{IN} = 12V
V_{OUT} = 3.3V
F_{SW} = 400kHz
$R_{\theta JA}$ = 18.6°C/W

図 7-4. Maximum Output Current versus Ambient Temperature



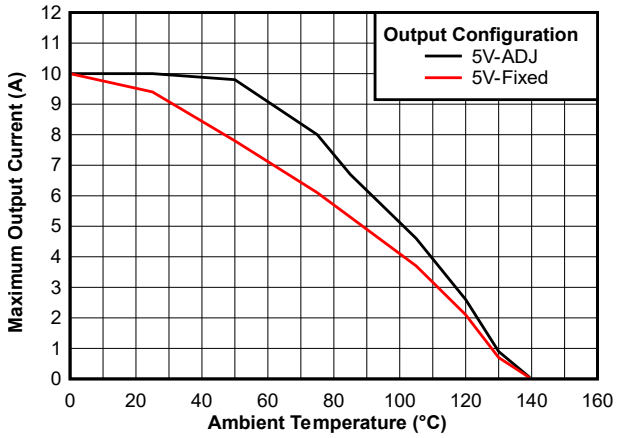
V_{IN} = 12V
V_{OUT} = 3.3V
F_{SW} = 2.1MHz
$R_{\theta JA}$ = 18.6°C/W

図 7-5. Maximum Output Current versus Ambient Temperature



V_{IN} = 12V
V_{OUT} = 5V
F_{SW} = 400kHz
$R_{\theta JA}$ = 18.6°C/W

図 7-6. Maximum Output Current versus Ambient Temperature



V_{IN} = 12V
V_{OUT} = 5V
F_{SW} = 2.1MHz
$R_{\theta JA}$ = 18.6°C/W

図 7-7. Maximum Output Current versus Ambient Temperature

7.2 Typical Applications

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LM704A0-Q1-powered implementation, see *TI Designs* reference design library.

7.2.1 Design 1 – High Efficiency, Wide Input, 400kHz Synchronous Buck Regulator

図 7-8 shows the schematic diagram of a single-output synchronous buck regulator with the output voltage of 5V and a rated load current of 8A. In this example, the target half-load and full-load efficiencies are 93.5% and 92.5%, respectively, based on a nominal input voltage of 24V that ranges from 8V to 45V. The switching frequency is set at 400kHz by resistor R_{RT}. An output voltage of 3.3V is also feasible simply by connecting FB to VDDA.

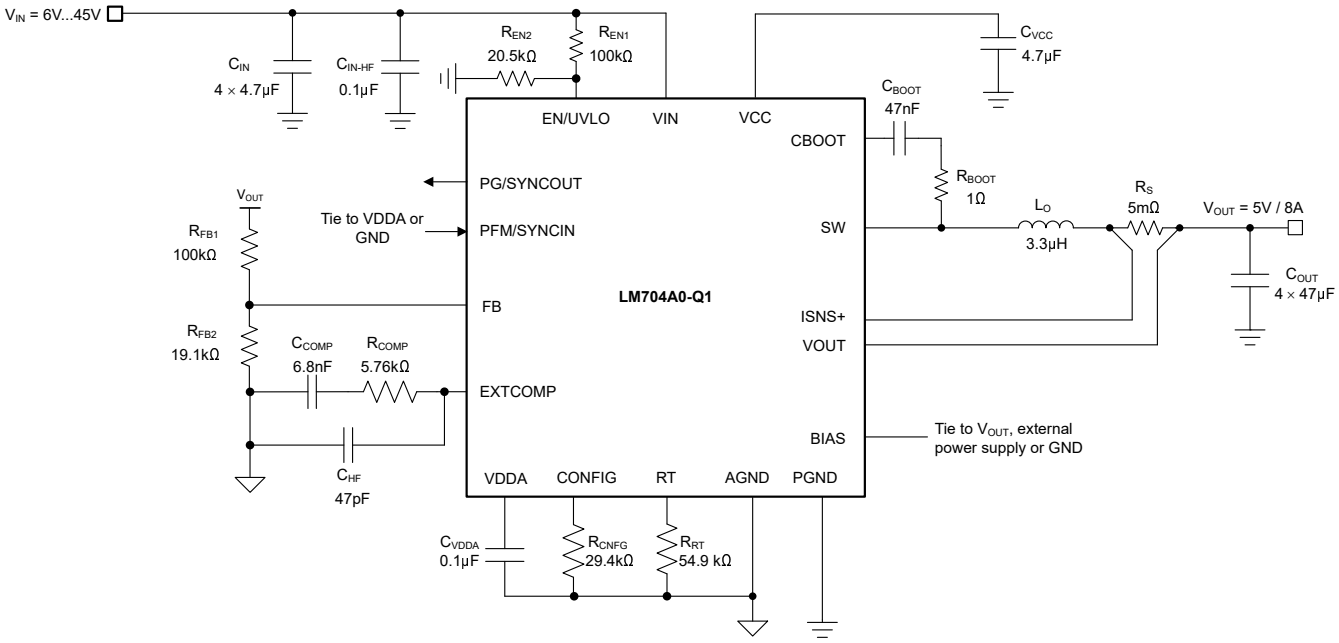


図 7-8. Application Circuit 1 With LM704A0-Q1 Buck Regulator at 400kHz

注

This and subsequent design examples are provided herein to showcase the LM704A0-Q1 converter in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to make sure of stability, particularly at low input voltage and high output current operating conditions. See Power Supply Recommendations for more detail.

7.2.1.1 Design Requirements

表 7-1 shows the intended input, output, and performance parameters for this automotive design example.

表 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	8V to 42V
Min transient input voltage (cold crank)	5.5V
Max transient input voltage (load dump)	45V
Output voltage	5V
Output current	8A
Switching frequency	400kHz
Output voltage regulation	±1%
Active current, no load	10µA
Shutdown current	2.2µA
Soft-start time	3ms

The switching frequency is set at 400kHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 30kHz with a phase margin greater than 50°.

The selected buck regulator powertrain components are cited in 表 7-2, and many of the components are available from multiple vendors. This design uses a low-DCR, metal-powder composite inductor, and ceramic output capacitor implementation.

表 7-2. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	4	4.7µF, 100V, X7S, 1210, ceramic	Murata	GCM32DC72A475KE02L
			TDK	CGA6M3X7S2A475K200
C_O	4	47µF, 6.3V, X7R, 1210, ceramic, AEC-Q200	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47µF, 10V, X7S, 1210, ceramic, AEC-Q200	TDK	CGA6P1X7S1A476M250AC
L_O	1	3.3µH, 5.9mΩ, 10.1A, 6.71 × 6.51 × 6.1mm, AEC-Q200	Coilcraft	XGL6060-332MEC
		3.3µH, 10.8mΩ, 15A, 6.45 × 6.65 × 5.8mm, AEC-Q200	Würth Electronik	74439346033
R_S	1	Shunt, 5mΩ, 0508, 1W, AEC-Q200	Susumu	KRL3216T4A-M-R005
U_1	1	LM704A0-Q1 45V, 10A synchronous DC/DC buck converter, AEC-Q100	Texas Instruments	LM704A0QRRXRQ1

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM704A0-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.1.2.2 Custom Design With Excel Quickstart Tool

Select components based on the regulator specifications using the LM704A0-Q1 Quickstart Calculator tool available for download from the LM704A0-Q1 product folder.

7.2.1.2.3 Buck Inductor

1. Use 式 30 to calculate the required buck inductance based on a 40% inductor ripple current at nominal input voltages.

$$L_O = \frac{V_{OUT}}{\Delta I_{LO} \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) = \frac{5V}{3.2A \times 400kHz} \times \left(1 - \frac{5V}{24V}\right) = 3.1\mu H \quad (30)$$

2. Select a standard inductor value of 3.3µH. Use 式 31 to calculate the peak inductor currents at maximum steady-state input voltage. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control. For design simplification, the LM704A0-Q1 has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation.

$$I_{LO(PK)} = I_{OUT} + \frac{\Delta I_{LO}}{2} = I_{OUT} + \frac{V_{OUT}}{2 \times L_O \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) = 8A + \frac{5V}{2 \times 3.3\mu H \times 400kHz} \times \left(1 - \frac{5V}{45V}\right) = 9.68A \quad (31)$$

3. Based on 式 7,use 式 32 to cross-check the inductance to set a slope compensation close to the ideal one times the inductor current downslope. The selected 3.3µH has less downslope and is adequate.

$$L_{O(sc)} = \frac{V_{OUT} \times R_S}{24 \times F_{SW}} = \frac{5V \times 5m\Omega}{24 \times 0.4MHz} = 2.6\mu H \quad (32)$$

7.2.1.2.4 Current-Sense Resistance

1. Calculate the current-sense resistance based on a maximum peak current capability of at least 25% higher than the peak inductor current at full load to provide sufficient margin during start-up and load-on transients. Calculate the current sense resistances using 式 33.

$$R_S = \frac{V_{CS(TH)}}{1.25 \times I_{LO(PK)}} = \frac{56mV}{1.25 \times 9.68} = 4.63m\Omega \quad (33)$$

where

- $V_{CS(TH)}$ is the 56mV current limit threshold.

2. Select a standard resistance value of 5mΩ for the shunt. A 0508 footprint component with wide aspect ratio termination design provides 1-W power rating, low parasitic series inductance, and compact PCB layout.

Carefully observe the *Layout Guidelines* to make sure that noise and DC errors do not corrupt the differential current-sense voltages measured at the ISNS+ and VOUT pins.

3. Place the shunt resistor close to the inductor.
4. Use Kelvin-sense connections, and route the sense lines differentially from the shunt to the LM704A0-Q1.
5. The ISNS-to-output propagation delay (related to the current limit comparator, internal logic and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay $t_{ISNS(delay)}$ of 40ns, use 式 34 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LOPK(SC)} = \frac{V_{CS(TH)}}{R_S} + \frac{V_{IN(max)} \times t_{ISNS(delay)}}{L_O} = \frac{56mV}{5m\Omega} + \frac{45V \times 45ns}{3.3\mu H} = 11.81A \quad (34)$$

6. Based on this result, select an inductor with saturation current greater than 12A across the full operating temperature range.

7.2.1.2.5 Output Capacitors

1. Use 式 35 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming a load transient deviation specification of 5% (250mV for a 5V output).

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2} = \frac{3.3\mu H \times (8A)^2}{(5V + 250mV)^2 - 5V^2} = 82\mu F \quad (35)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select four 47µF, 10V, X7S, 1210 ceramic output capacitors. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory.
3. Use 式 36 to estimate the peak-peak output voltage ripple at nominal input voltage.

$$\Delta V_{OUT} = \sqrt{\left(\frac{\Delta I_{LO}}{8 \times F_{SW} \times C_{OUT}}\right)^2 + (R_{ESR} \times \Delta I_{LO})^2} = \sqrt{\left(\frac{3.2A}{8 \times 400kHz \times 82\mu F}\right)^2 + (1m\Omega \times 3.2A)^2} = 12.6mV \quad (36)$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 82µF is the total effective (derated) ceramic output capacitance at 5V.

4. Use 式 37 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_{LO}}{\sqrt{12}} = \frac{3.2A}{\sqrt{12}} = 0.92A \quad (37)$$

7.2.1.2.6 Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. As mentioned earlier, dual-channel interleaved operation significantly reduces the input ripple amplitude. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Use 式 38 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{D \times (1 - D)} = 8A \times \sqrt{0.5 \times (1 - 0.5)} = 4A \quad (38)$$

3. Use 式 39 to find the required input capacitance.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} = \frac{0.5 \times (1 - 0.5) \times 8A}{400kHz \times (240mV - 2m\Omega \times 8A)} = 22.3\mu F \quad (39)$$

where

- ΔV_{IN} is the input peak-to-peak ripple voltage specification.
- R_{ESR} is the input capacitor ESR.

4. Recognizing the voltage coefficient of ceramic capacitors, select five 4.7µF, 100V, X7R, 1210 ceramic input capacitors. Place these capacitors adjacent to the VIN and PGND pins.
5. Use a 10nF, 100V, X7R, 0603 ceramic capacitor near the VIN and PGND pins to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower conducted and radiated EMI signature. Refer to *Layout Guidelines* for more detail.

7.2.1.2.7 Frequency Set Resistor

Calculate the RT resistance for a switching frequency of 400kHz using the following equation. Choose the nearest standard E96 value of 54.9kΩ.

$$R_{RT}[k\Omega] = \frac{\frac{10^6}{F_{SW}[kHz]} - 53}{45} = \frac{\frac{10^6}{400} - 53}{45} = 54.4k\Omega \quad (40)$$

7.2.1.2.8 Feedback Resistors

If an output voltage setpoint other than 3.3V or 5V is required (or to measure a bode plot when using either of the fixed output voltage options), determine the feedback resistances using 式 41.

$$R_{FB2} = \frac{R_{FB1}}{\left(\frac{V_{OUT}}{V_{REF}}\right) - 1} = \frac{100k\Omega}{\left(\frac{5V}{0.8V}\right) - 1} = 19.05k\Omega \quad (41)$$

7.2.1.2.9 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows.

1. Based on a specified loop gain crossover frequency, f_C, of 40kHz, use 式 42 to calculate R_{COMP}, assuming an effective output capacitance of 82µF. Choose a standard value for R_{COMP} of 5.36kΩ.

$$R_{COMP} = 2 \times \pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{R_S \times G_{CS}}{gm} \times C_{OUT} = 2 \times \pi \times 40kHz \times \frac{5V}{0.8V} \times \frac{5m\Omega \times 10}{1200\mu S} \times 82\mu F = 5.37k\Omega \quad (42)$$

2. To provide adequate phase boost at crossover while also allowing a fast settling time during a load or line transient, select C_{COMP} to place a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Choose a standard value for C_{COMP} of 6.8nF.

$$C_{COMP} = \frac{10}{2 \times \pi \times f_C \times R_{COMP}} = \frac{10}{2 \times \pi \times 40kHz \times 5.36k\Omega} = 7.42nF \quad (43)$$

Such a low capacitance value also helps to avoid output voltage overshoot when recovering from dropout (when the input voltage is less than the output voltage setpoint and V_{COMP} is railed high).

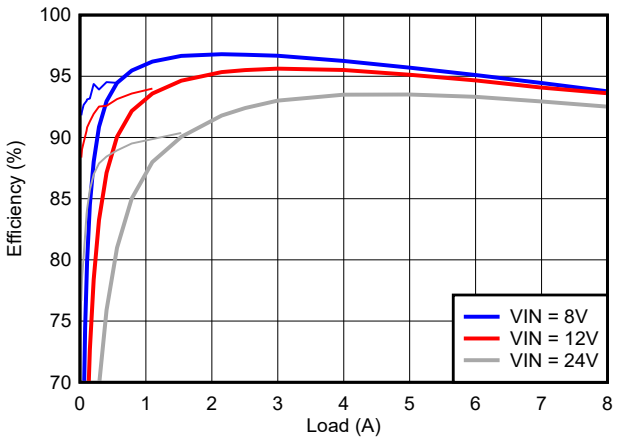
3. Calculate C_{HF} to create a pole at the ESR zero and to attenuate high-frequency noise at COMP. C_{BW} is the bandwidth-limiting capacitance of the error amplifier. Select a standard value for C_{HF} of 47pF.

$$C_{HF} = \frac{1}{2 \times \pi \times f_{ESR} \times R_{COMP}} - C_{BW} = \frac{1}{2 \times \pi \times 500kHz \times 5.36k\Omega} - 38pF = 21pF \quad (44)$$

注

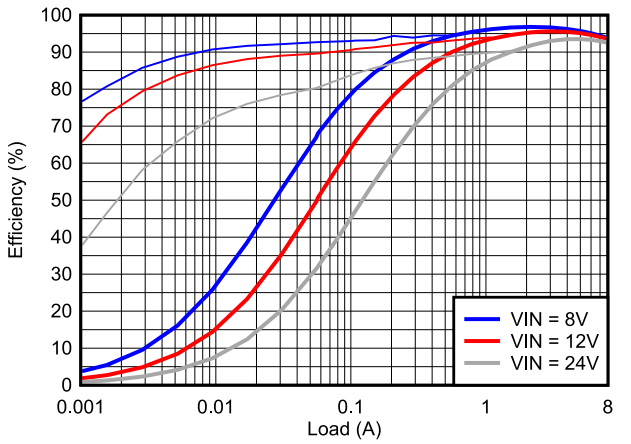
Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

7.2.1.3 Application Curves



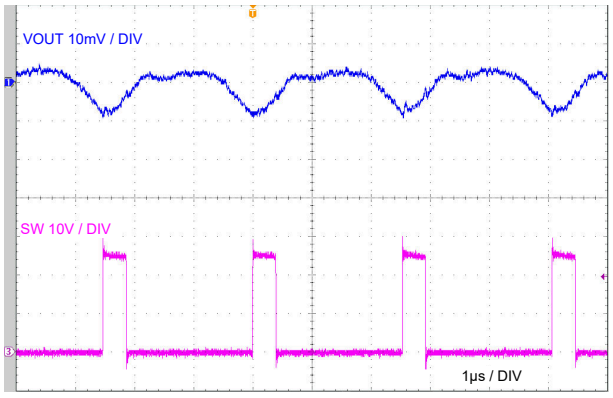
V_{OUT} = 5V F_{SW} = 400kHz PFM / FPWM

図 7-9. Efficiency versus I_{OUT}



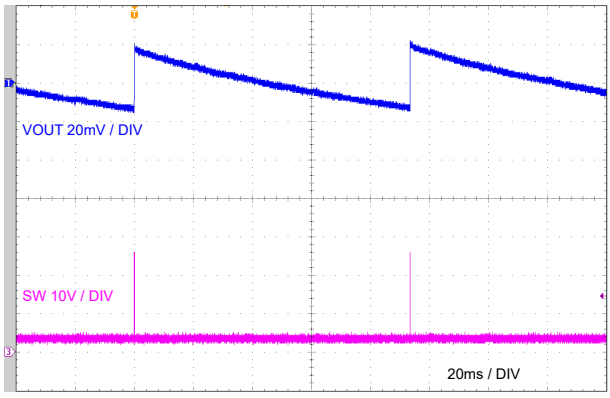
V_{OUT} = 5V F_{SW} = 400kHz PFM / FPWM

図 7-10. Efficiency versus I_{OUT}, Log Scale



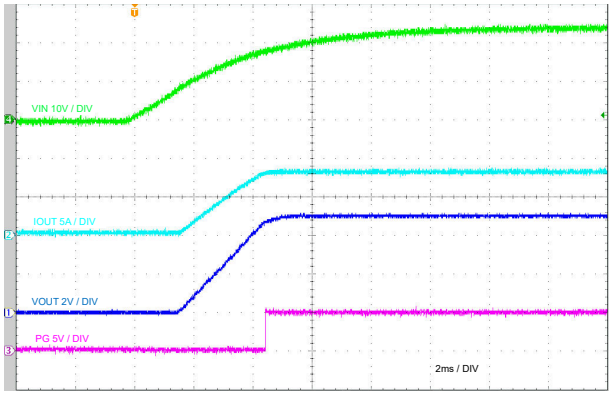
V_{IN} = 24V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = 5V F_{SW} = 400kHz

図 7-11. Full load Switching



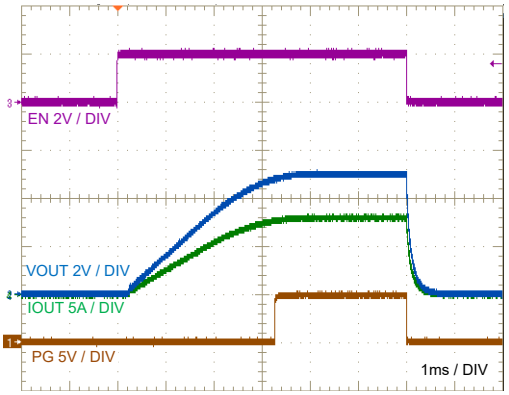
V_{IN} = 24V No load PFM
V_{OUT} = 5V

図 7-12. PFM Switching



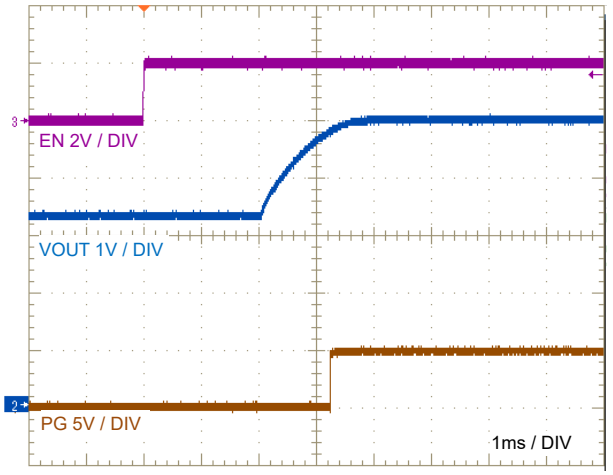
V_{IN} stepped to 24V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = 5V F_{SW} = 400kHz

図 7-13. V_{IN} Start-Up Characteristic



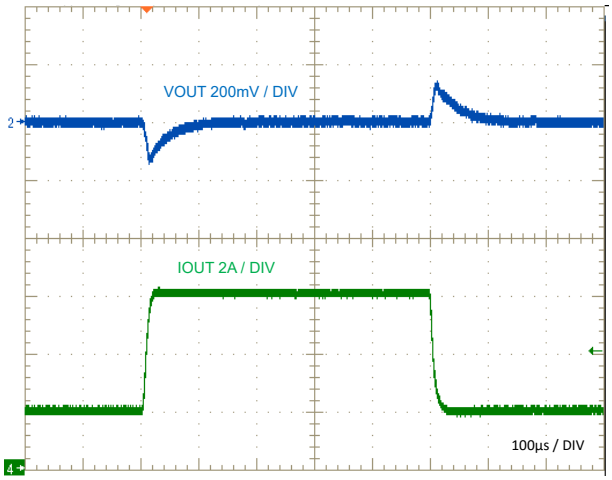
V_{IN}= 24V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = 5V F_{SW} = 400kHz

図 7-14. EN Start-Up Characteristic



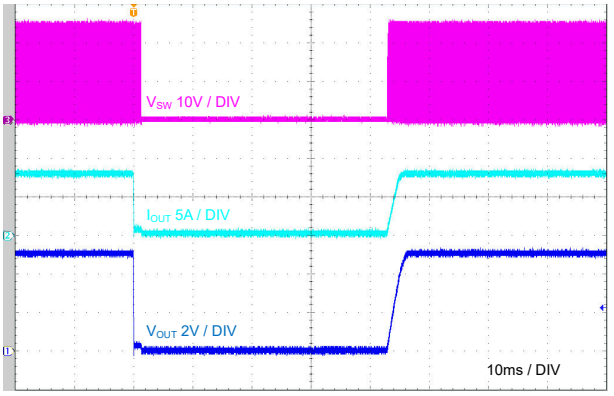
V_{IN} = 24V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = Prebiased to 5V F_{SW} = 400kHz

図 7-15. EN Start-Up Prebias Characteristic



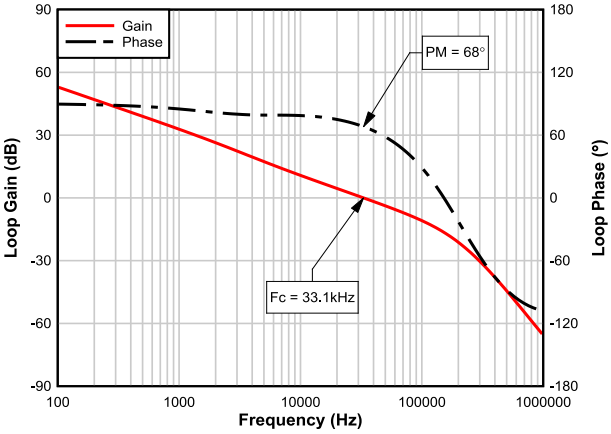
V_{IN} = 24V F_{SW} = 400kHz FPWM
V_{OUT} = 5V

図 7-16. Load Transient, 2A to 6A



V_{IN} = 24V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = 5V F_{SW} = 400kHz

図 7-17. Short-Circuit Recovery



F_c = crossover frequency, PM = phase margin.
V_{IN} = 24V I_{OUT} = 8A (resistive) FPWM
V_{OUT} = 5V F_{SW} = 400kHz L = 3.3µH

図 7-18. Bode Plot

7.2.2 Design 2 – High Efficiency 24V to 3.3V 400kHz Synchronous Buck Regulator

図 7-19 shows the schematic diagram of a single-output synchronous buck regulator with the output voltage of 3.3V and a rated load current of 10A. In this example, the target half-load and full-load efficiencies are 90.9% and 88.1%, respectively, based on a nominal input voltage of 24V that ranges from 12V to 42V. The switching frequency is set at 400kHz by resistor R_{RT}.

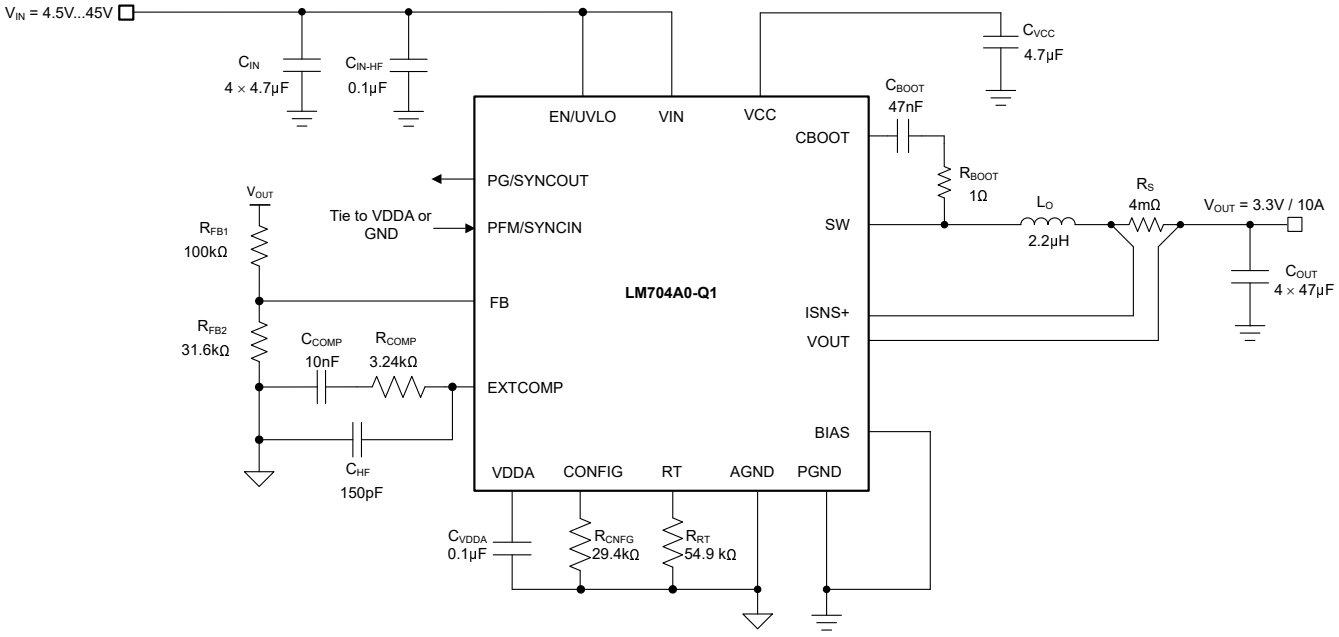


図 7-19. Application Circuit 2 With LM704A0-Q1 Buck Regulator at 400kHz

7.2.2.1 Design Requirements

表 7-3 shows the intended input, output, and performance parameters for this automotive design example.

表 7-3. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	12V to 42V
Min transient input voltage (cold crank)	5V
Max transient input voltage (load dump)	45V
Output voltage	3.3V
Output current	10A
Switching frequency	400kHz
Output voltage regulation	±1%
Active current, no load	12µA
Shutdown current	2.2µA
Soft-start time	3ms

The switching frequency is set at 400kHz by resistor R_{RT} The selected buck regulator powertrain components are cited in 表 7-4 and many of the components are available from multiple vendors. This design uses a low-DCR, metal-powder composite inductor and ceramic output capacitor implementation.

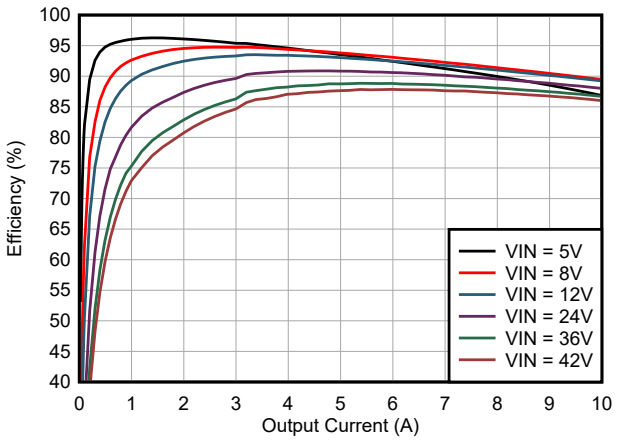
表 7-4. List of Materials for Application Circuit 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	4	4.7µF, 100V, X7S, 1210, ceramic	Murata	GCM32DC72A475KE02L
			TDK	CGA6M3X7S2A475K200
C_O	4	47µF, 10V, X7R, 1210, ceramic, AEC-Q200	Murata	GRM32ER71A476KE15L
		47µF, 10V, X7S, 1210, ceramic, AEC-Q200	TDK	CNA6P1X7S1A476M250AE
L_O	1	2.2µH, 3.8mΩ, 21.5A, 11.3 × 10 × 6mm, AEC-Q200	Coilcraft	XGL1060-222MEC
		2.2µH, 3.8mΩ, 26A, 11.2 × 10.3 × 6.5mm, AEC-Q200	Cyntec	VCHA106E-2R2MS6
		2.2µH, 4.1mΩ, 21.4A, 11.2 × 10.3 × 5.4mm, AEC-Q200	Cyntec	VCHA105D-2R2MS6
R_S	1	Shunt, 4mΩ, 0508, 1W, AEC-Q200	Susumu	KRL2012E-M-R004-F-T5
U_1	1	LM704A0-Q1 45V, 10A synchronous DC/DC buck converter, AEC-Q100	Texas Instruments	LM704A0QRRXRQ1

7.2.2.2 Detailed Design Procedure

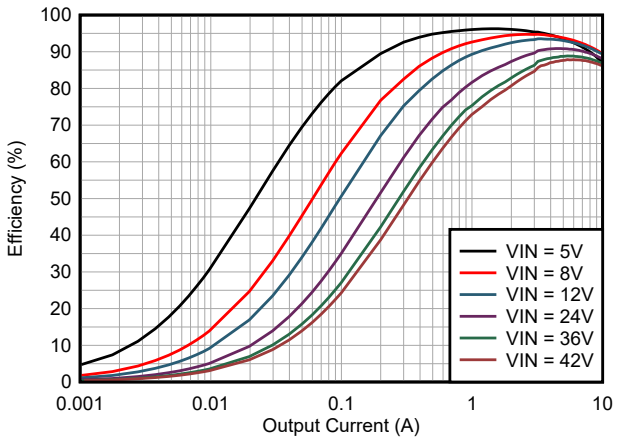
See Detailed Design Procedure.

7.2.2.3 Application Curves



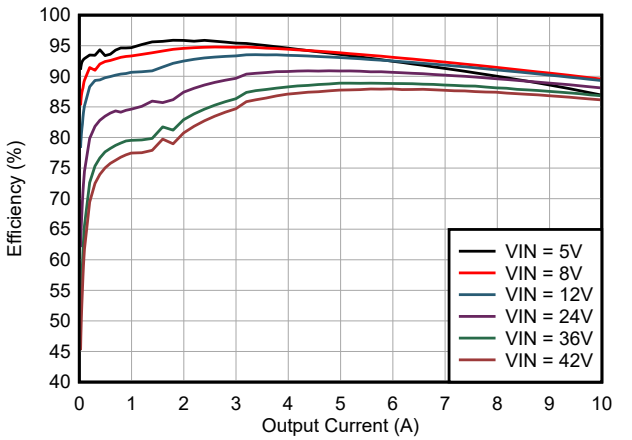
V_{OUT} = 3.3V F_{SW} = 400kHz FPWM

図 7-20. Efficiency versus I_{OUT}, Linear Scale



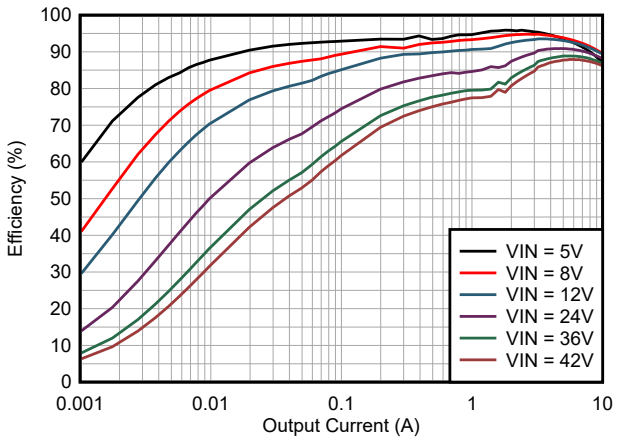
V_{OUT} = 3.3V F_{SW} = 400kHz FPWM

図 7-21. Efficiency versus I_{OUT}, Log Scale



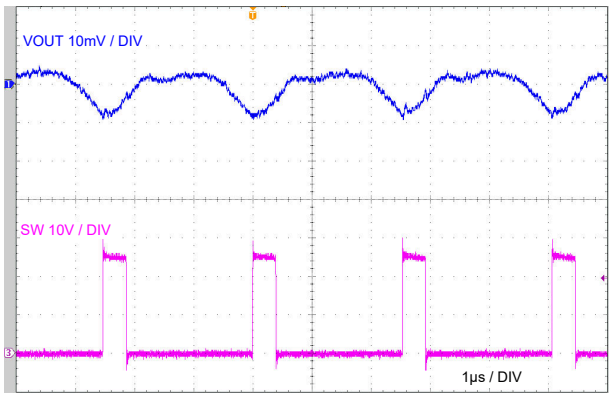
V_{OUT} = 3.3V F_{SW} = 400kHz PFM

図 7-22. Efficiency versus I_{OUT}, Linear Scale



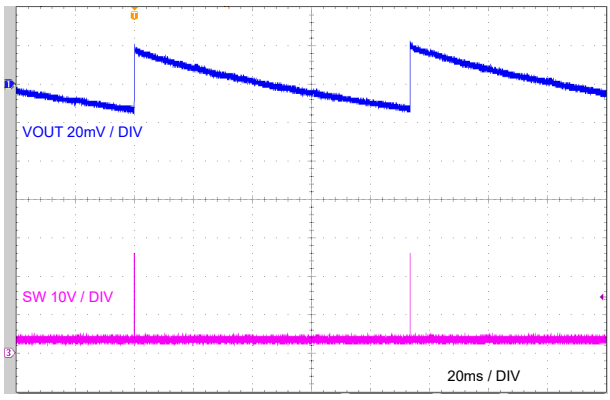
V_{OUT} = 3.3V F_{SW} = 400kHz PFM

図 7-23. Efficiency versus I_{OUT}, Log Scale



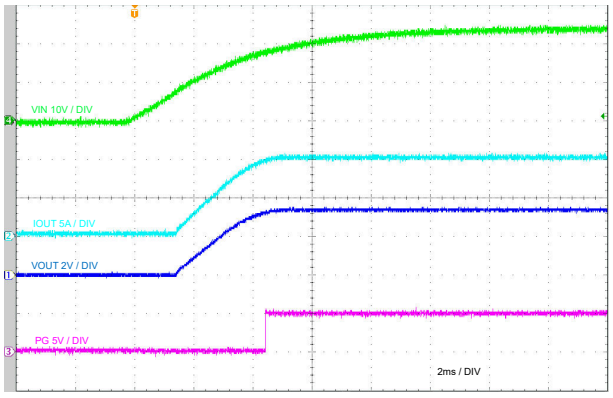
V_{IN} = 24V I_{OUT} = 10A FPWM
V_{OUT} = 3.3V F_{SW} = 400kHz

図 7-24. Full Load Switching



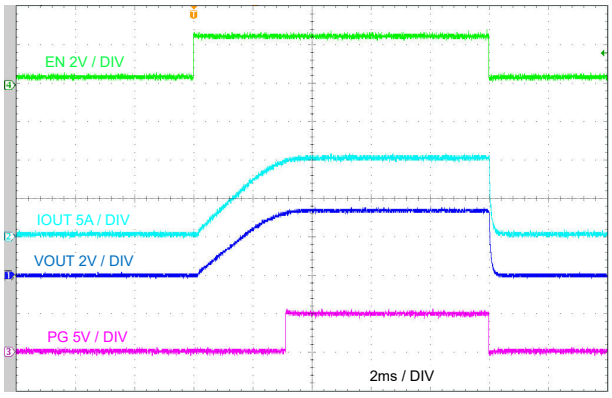
V_{IN} = 24V No load PFM
V_{OUT} = 3.3V

図 7-25. PFM Switching



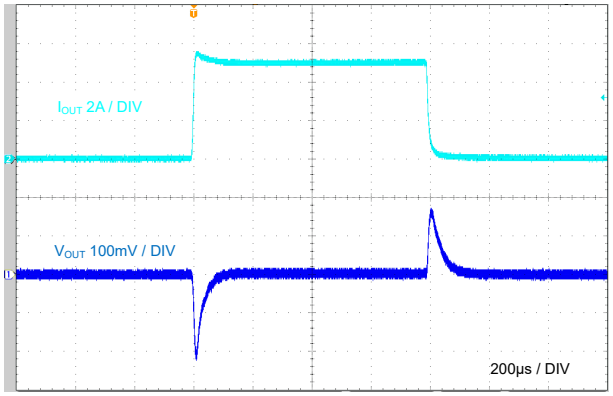
V_{IN} stepped to 24V I_{OUT} = 10A (resistive) FPWM
V_{OUT} = 3.3V F_{SW} = 400kHz

図 7-26. V_{IN} Start-Up Characteristic



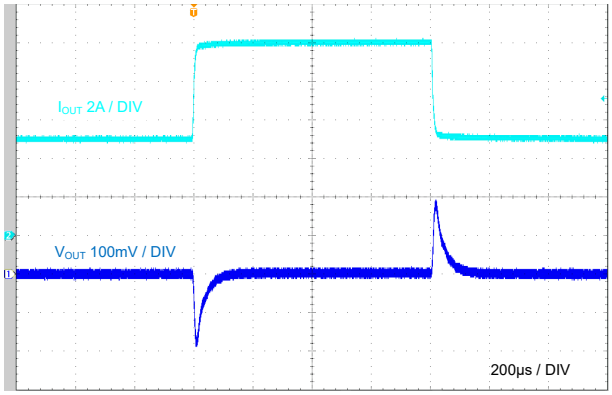
V_{IN} = 24V I_{OUT} = 10A (resistive) FPWM
V_{OUT} = 3.3V F_{SW} = 400kHz

図 7-27. EN Start-Up and Shutdown Characteristic



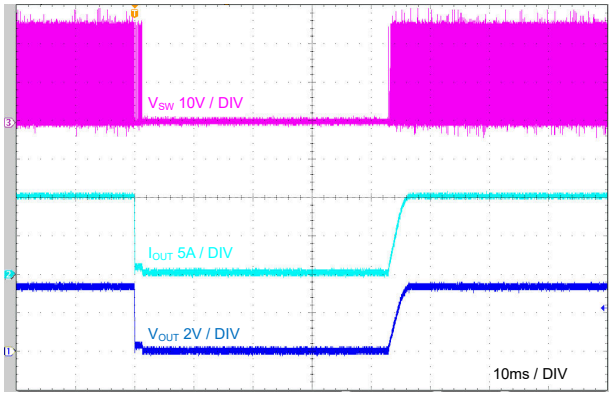
V_{IN} = 24V FPWM
V_{OUT} = 3.3V

図 7-28. Load Transient, 0A to 5A



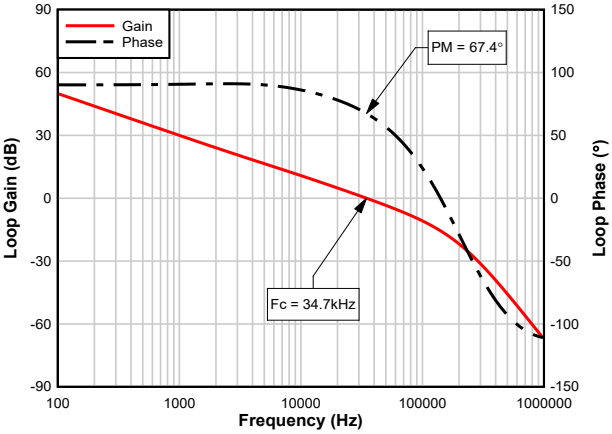
V_{IN} = 24V FPWM
V_{OUT} = 3.3V

図 7-29. Load Transient, 5A to 10A



V_{IN} = 24V I_{OUT} = 10A (resistive) FPWM
V_{OUT} = 3.3V F_{SW} = 400kHz

図 7-30. Short-Circuit Recovery



F_c = crossover frequency, PM = phase margin.
V_{IN} = 24V F_{SW} = 400kHz FPWM
V_{OUT} = 3.3V I_{OUT} = 10A (resistive) L = 2.2µH

図 7-31. Bode Plot

7.3 Power Supply Recommendations

The LM704A0-Q1 is designed to operate from a wide input voltage range of 4.5V to 45V. The input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with the following equation.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \times \eta} \quad (45)$$

where

- η is the efficiency

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10µF to 47µF is usually sufficient to provide parallel input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *Simple Success with Conducted EMI for DC-DC Converters* application report provides helpful suggestions when designing an input filter for any switching regulator.

7.4 Layout

7.4.1 Layout Guidelines

Proper PCB design and layout is important in high-current, fast-switching converter circuits (with high current and voltage slew rates) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the converter depends to a large extent on PCB layout.

The high-frequency power loop of a buck regulator power stage is denoted in red and the topological architecture of a buck regulator means that particularly high di/dt current flows in the components shown in 図 7-32. Reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory.

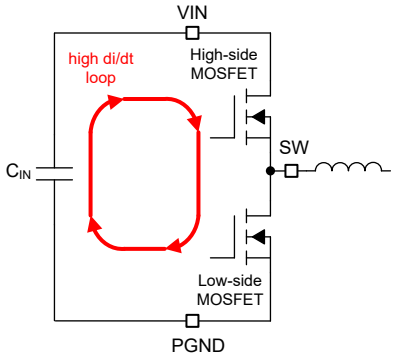


図 7-32. Input Current Loop

The following list summarizes the essential guidelines for PCB layout and component placement to optimize DC/DC converter performance, including thermals and EMI signature. 図 7-33 shows a recommended layout of the LM704A0-Q1 with optimized placement and routing of the power-stage and small-signal components.

- *Place the input capacitors as close as possible to the input power pins*: The VIN and PGND pins are close together (with a gap in between to increase clearance), thus simplifying input capacitor placement.

  - Use low-ESR ceramic capacitors with X7R or X7S dielectric from VIN to PGND. Place an 0402 capacitor close to VIN for high-frequency bypass as shown in 図 7-33. Use additional 1206 or 1210 capacitors for bulk capacitance.
  - Ground return paths for both the input and output capacitors must consist of localized top-side planes that connect to the PGND pins.
- *Use a solid ground plane on the PCB layer beneath the top layer with the IC*: This plane acts as a noise shield and a heat dissipation path. Using the PCB layer directly below the IC minimizes the magnetic field associated with the currents in the switching loops, thus reducing parasitic inductance and switch voltage overshoot and ringing. Use numerous thermal vias near PGND for heatsinking to the inner ground planes.
- *Make the VIN, VOUT, and GND bus connections as wide as possible*: These paths must be wide and direct as possible to reduce any voltage drops on the input or output paths of the converter, thus maximizing efficiency.
- *Locate the buck inductor close to the SW1, SW2, and SW3 pins*: Use a short, wide connection trace from the converter SW pins to the inductor. At the same time, minimize the length (and area) of this high-dv/dt surface to help reduce capacitive coupling and radiated EMI. Connect the dotted terminal of the inductor to the SW pins.
- *Place the VCC and BOOT capacitors close to the respective pins*: The VCC and BOOT capacitors represent the supplies for the internal low-side and high-side MOSFET gate drivers, respectively, and thus carry high-frequency currents. Locate C_{VCC} close to the VCC pin and place a GND via at the return terminal to connect to the GND plane and thus back to IC GND at the exposed pad. Connect C_{BOOT} close to the CBOOT and SW4 pins.
- *Place the feedback divider as close as possible to the FB pin*: Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the FB trace length and related noise coupling. The FB pin is the input to the voltage-loop error amplifier and represents a high-impedance node sensitive to noise. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the switch node) that can capacitively couple into the feedback path of the converter.
- *Provide enough PCB area for proper heatsinking*: Use sufficient copper area to achieve a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. Provide adequate heatsinking for the LM704A0-Q1 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad (GND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. Make the top and bottom PCB layers preferably with two-ounce copper thickness (and no less than one ounce).

7.4.1.1 Thermal Design and Layout

For a DC/DC converter to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM704A0-Q1 is available in a small 6mm × 6mm 29-pin QFN integrated circuit package to cover a range of application requirements. This section summarizes the thermal metrics of this package.

Numerous vias with a 0.3mm diameter connected from the thermal pads to the internal and solder-side plane or planes are vital to help dissipation. In a multi-layer PCB design, a solid GND plane is typically placed on the PCB layer below the power components. Not only does this action provide a plane for the power stage currents to flow but this action also represents a thermally conductive path away from the heat generating devices.

7.4.2 Layout Example

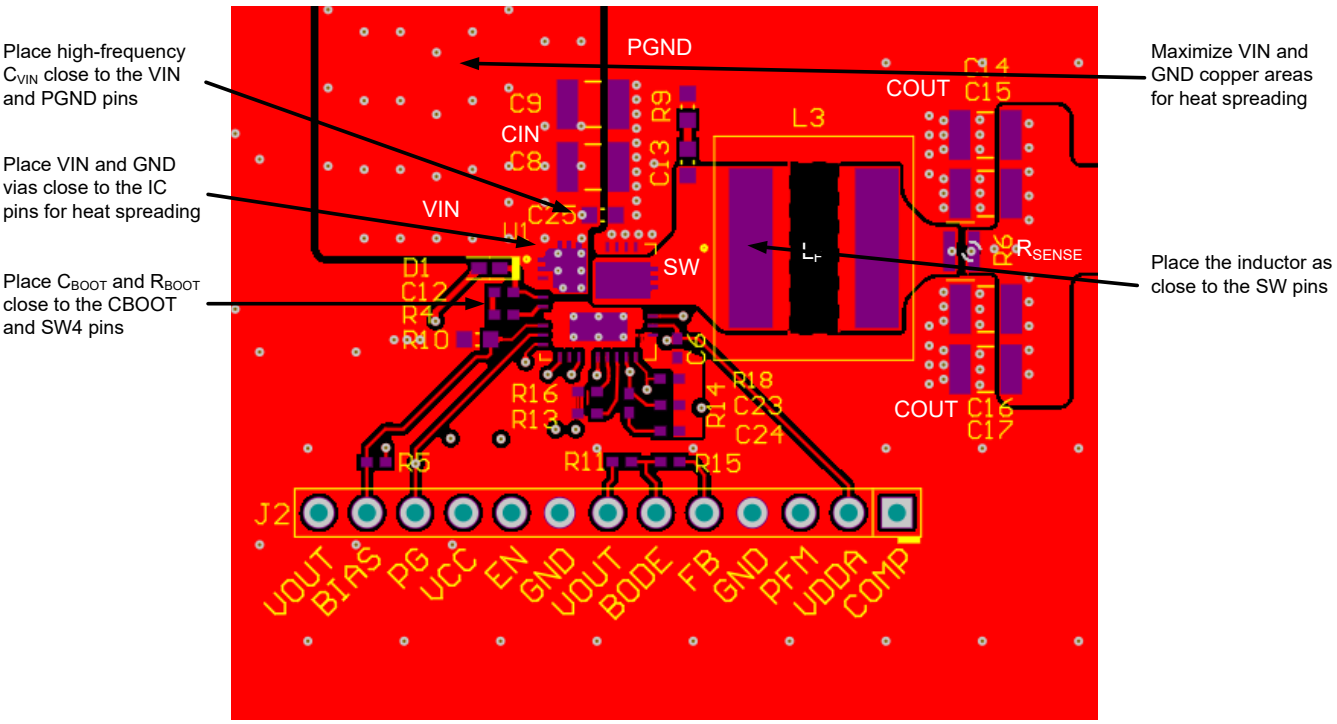


図 7-33. PCB Top Layer – High Density, Single-sided Design

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

For development support see the following:

- LM704A0-Q1 Quickstart Calculator tool
- LM704A0-Q1 Simulation Models
- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center
- TI Designs:
  - *ADAS 8-Channel Sensor Fusion Hub Reference Design with Two 4-Gbps Quad Deserializers*
  - *Automotive EMI and Thermally Optimized Synchronous Buck Converter Reference Design*
  - *Automotive High Current, Wide V_{IN} Synchronous Buck Controller Reference Design Featuring LM5141-Q1*
  - *25W Automotive Start-Stop Reference Design Operating at 2.2 MHz*
  - *Synchronous Buck Converter for Automotive Cluster Reference Design*
  - *137W Holdup Converter for Storage Server Reference Design*
  - *Automotive Synchronous Buck With 3.3V @ 12.0A Reference Design*
  - *Automotive Synchronous Buck Reference Design*
  - *Wide Input Synchronous Buck Converter Reference Design With Frequency Spread Spectrum*
  - *Automotive Wide V_{IN} Front-end Reference Design for Digital Cockpit Processing Units*
- Technical articles:
  - *High-Density PCB Layout of DC/DC Converters*
  - *Synchronous Buck Controller Solutions Support Wide V_{IN} Performance and Flexibility*
  - *How to Use Slew Rate for EMI Control*

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM704A0-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Application notes:
  - Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
  - Texas Instruments, *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
- Analog design journal:

  - Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*
- White papers:
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

8.2.1.1 PCB Layout Resources

- Application notes:
  - Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*
  - Texas Instruments, *AN-1229 Simple Switcher PCB Layout Guidelines*
  - Texas Instruments, *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Seminars:
  - Texas Instruments, *Constructing Your Power Supply – Layout Considerations*

8.2.1.2 Thermal Design Resources

- Application notes:
  - Texas Instruments, *AN-2020 Thermal Design by Insight, Not Hindsight*
  - *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - Texas Instruments, *Semiconductor and IC Package Thermal Metrics*
  - Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602*
  - Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
  - Texas Instruments, *PowerPAD Made Easy*
  - Texas Instruments, *Using New Thermal Metrics*

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

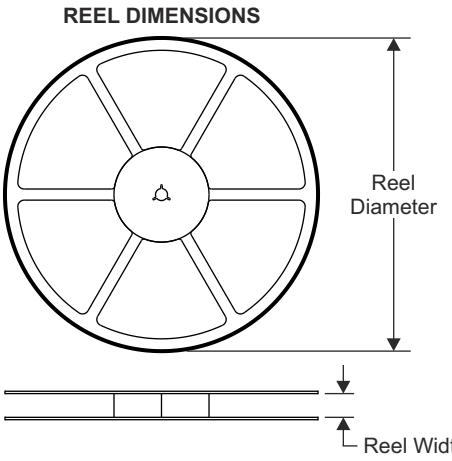
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

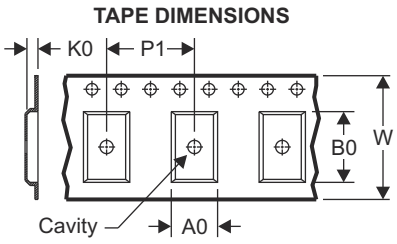
DATE	REVISION	NOTES
September 2024	*	Initial release

10 Mechanical, Packaging, and Orderable Information

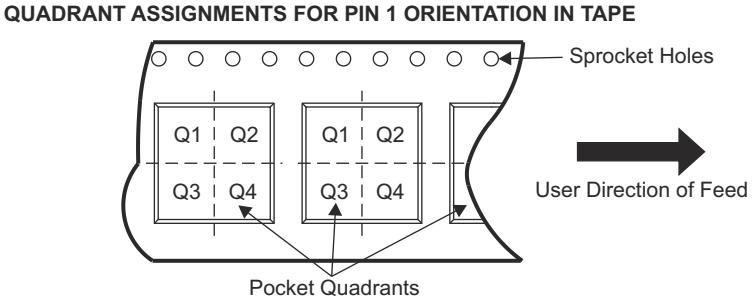
The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information



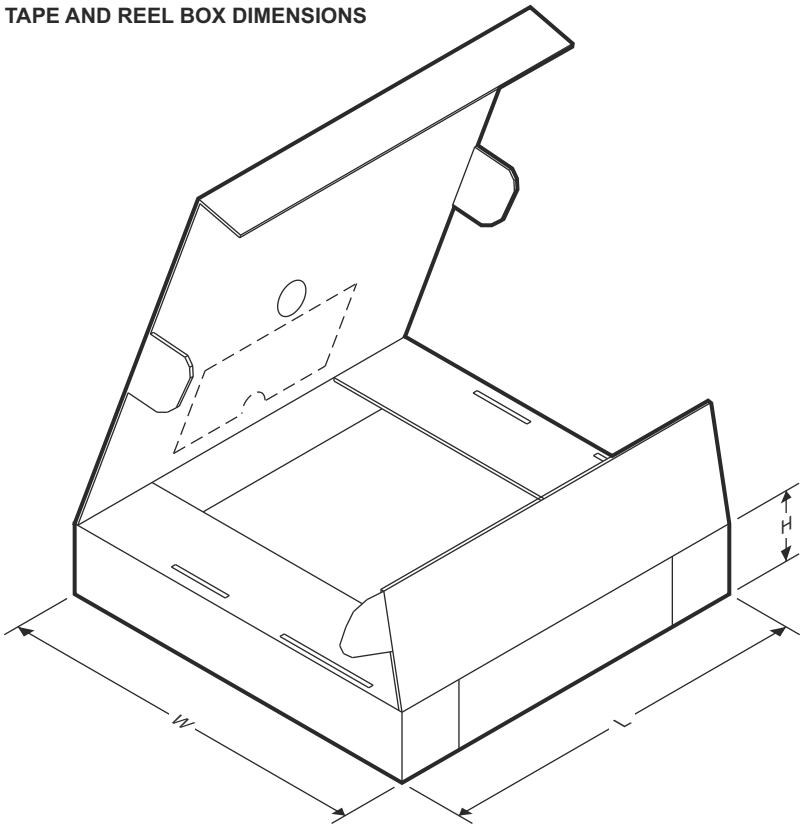


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM704A0QRRXRQ1	VQFN	RRX	29	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM704AQ0RRXRQ1	VQFN	RRX	29	3000	367.0	367.0	35.0

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM704A0QRRXRQ1	ACTIVE	VQFN	RRX	29	3000	RoHS-Exempt & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	704A0Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

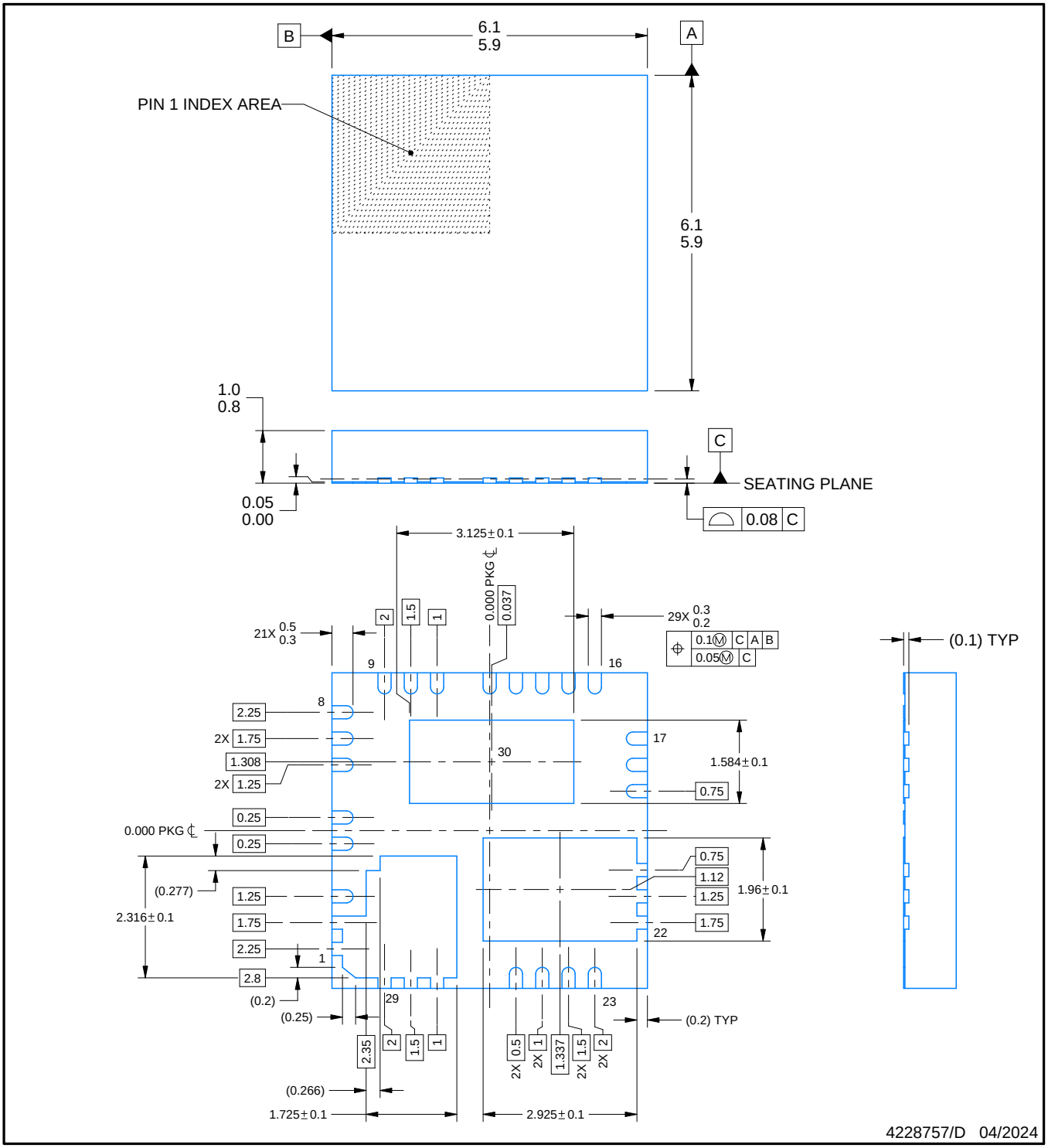
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RRX0029B

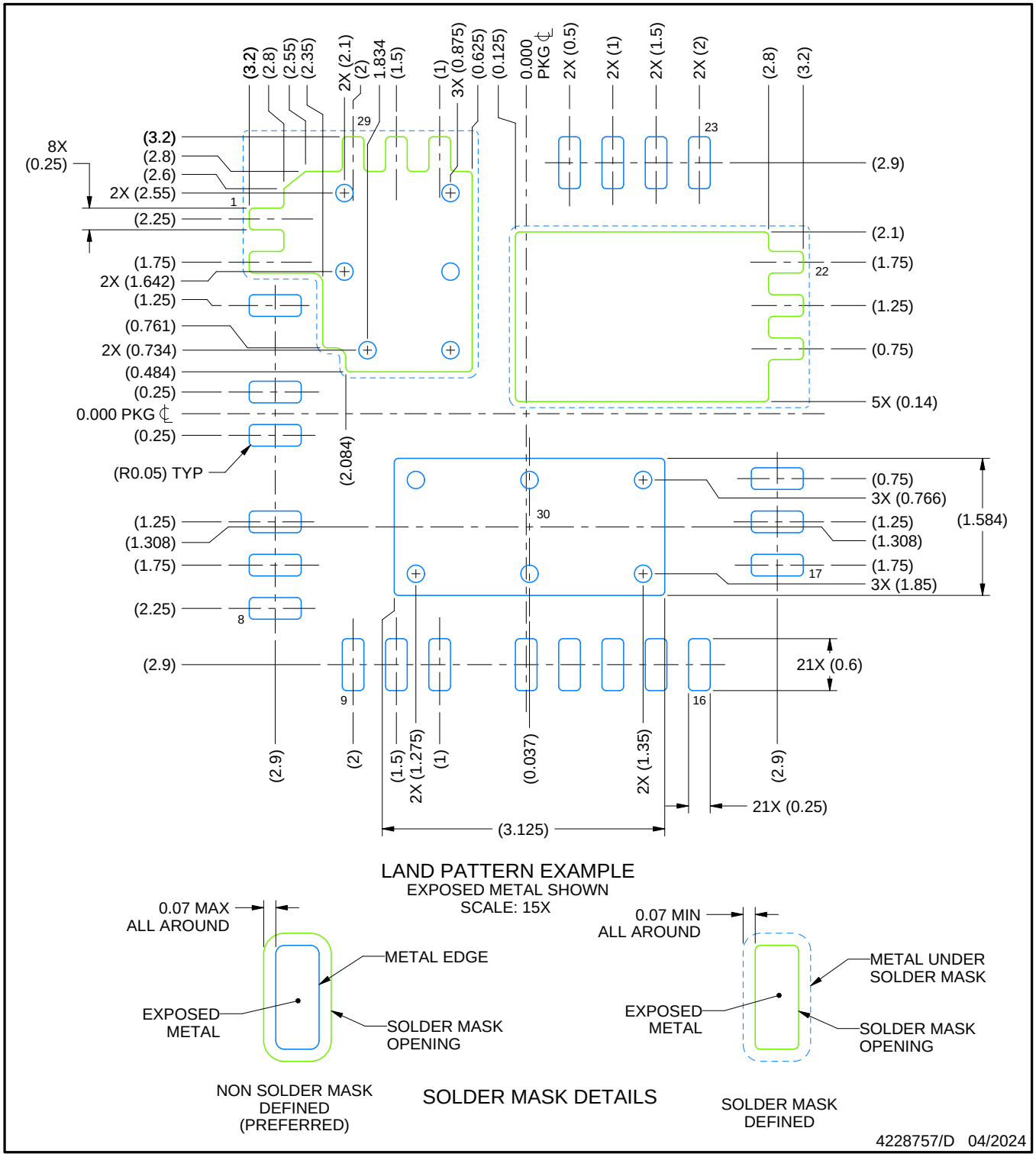
VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



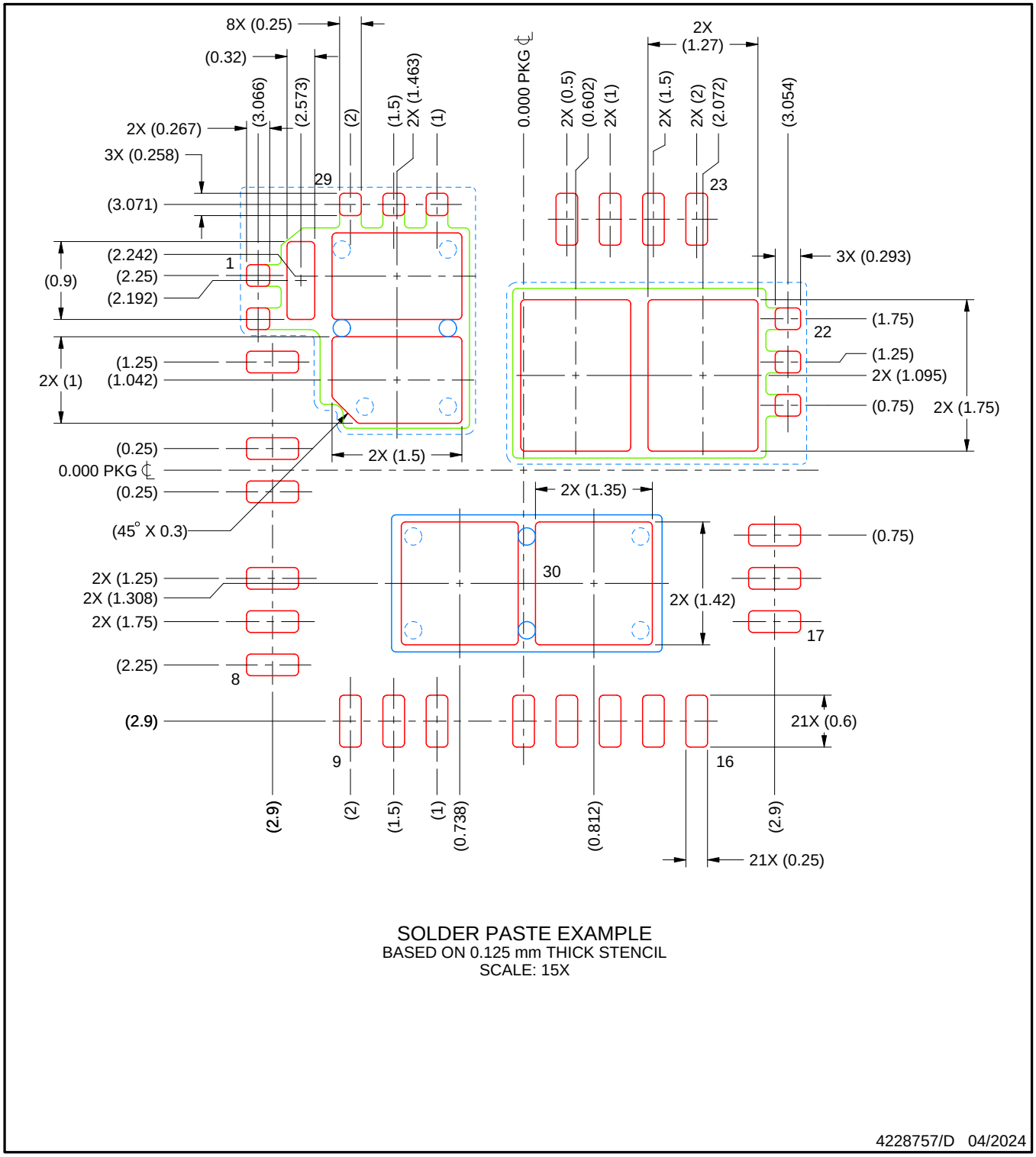
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

4228757/D 04/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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