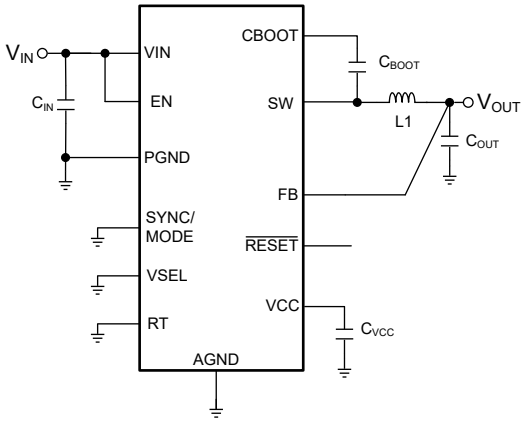
LM63635-Q1 3.5V～36V、3.25A、 の車載用降圧型電圧コンバータ

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 車載用システムの要件をサポート
  - 入力電圧範囲:3.5V～36V
  - 短い最小オン時間:50ns
  - 優れた電磁干渉 (EMI) 性能
  - 疑似ランダム拡散スペクトラム
  - CISPR 25 と互換
  - 低い動作時静止電流:23µA
  - 接合部温度範囲:-40°C～+150°C
- 多様な設計に対応する柔軟性
  - ピンで選択可能な V_{OUT}:3.3V、5V、可変 (1V～20V)
  - 出力電流:3.25A
  - ピンで選択可能な周波数:400kHz、2.1MHz、可変 (250kHz～2200kHz)
  - FPWM、自動、同期モードをピンで選択可能
  - 次の製品とピン互換:
    LM63610-Q1、LM63615-Q1、LM63625-Q1
  - TSSOP:高放熱パッケージ
- 小型デザイン サイズ
  - 最小 14mm × 14mm の WSON パッケージで 3.25A、2.2MHz
  - 高集積設計
  - 少ない部品点数



概略回路図

2 アプリケーション

- 車載用インフォテインメントおよびクラスタ
- 車載用ボディ・エレクトロニクス / ライティング
- 車載用 ADAS

3 概要

LM63635-Q1 レギュレータは、堅牢な車載アプリケーション向けに設計された、使いやすい同期整流降圧型 DC/DC コンバータです。LM63635-Q1 は、WSON パッケージでは最大 36V、HTSSOP パッケージでは 32V の入力から、最大 3.25A の負荷電流を駆動できます。このコンバータは、高い軽負荷時効率と出力精度を小さなデザイン サイズで実現しています。RESET フラグや高精度イネーブルなどの機能を使用すると、幅広いアプリケーションに対して柔軟で使いやすいソリューションを実現できます。軽負荷時には自動的に周波数フォールドバック モードになるため、負荷を厳密に制御しながら効率を上げることができます。高度な統合により、多くの外付け部品が不要で、PCB レイアウトが単純になるようにピン配置が設計されています。保護機能として、サーマル シャットダウン、入力低電圧誤動作防止、サイクル単位の電流制限、ヒカップ短絡保護機能が搭載されています。LM63635-Q1 は、PowerPAD™ 付き HTSSOP 16 ピン パワー パッケージと WSON 12 ピンのパワー パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LM63635-Q1	PWP (HTSSOP、16)	6.40mm × 5.00 mm
	DRR (WSON、12)	3.00mm × 3.00 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます

代表的な設計例：I_{OUT} = 3.25A、f_{SW} = 2200kHz

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4 Device Comparison Table

ORDER NUMBER (1)	PACKAGE	RATED CURRENT	F_{SW}	VOUT	Package size (NOM)
LM63635DQPWPRQ1	PWP0016D (HTSSOP)	3.25A	Adjustable with RT resistor RT = GND; F_{SW} = 2.1MHz RT = VCC; F_{SW} = 400kHz	V_{SEL} = VCC, VOUT = 5V V_{SEL} = GND, VOUT = 3.3V V_{SEL} = R_{SEL_ADJ}, VOUT = Adjustable via external FB resistors	6.40mm × 5.00mm
LM63635DQDRRRQ1	DRR0012 (WSON)				3.00mm × 3.00mm
LM63635CAQDRRRQ1			Fixed 2.1MHz	Adjustable VOUT via external FB resistors	

(1) For more information on device orderable part numbers, see *Device Nomenclature*.

5 Pin Configuration and Functions

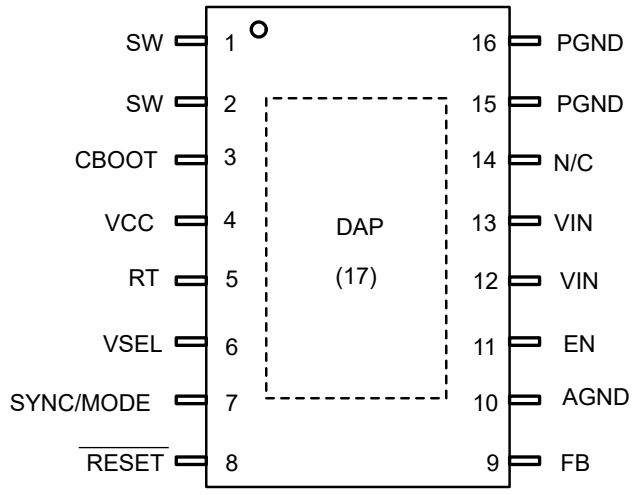


図 5-1. 16-Pin HTSSOP With PowerPAD™ Integrated Circuit Package, PWP — LM636x5D (Top View)

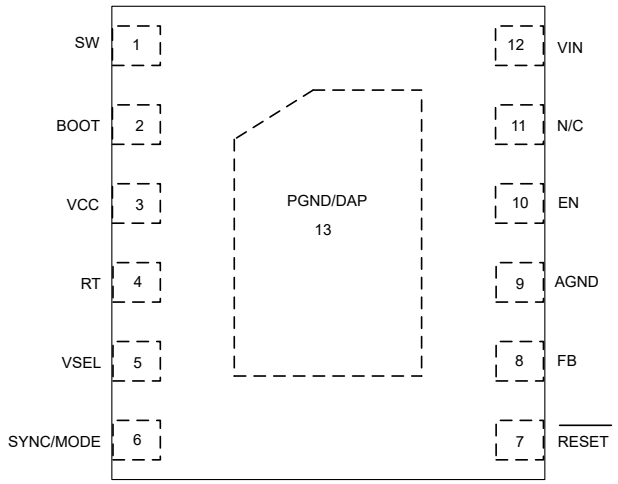


図 5-2. 12-Pin WSON With PowerPAD™ Integrated Circuit Package, DRR — LM63635D (Top View)

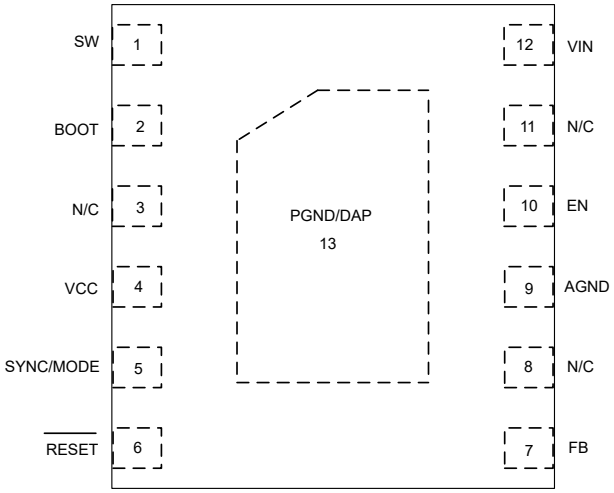


図 5-3. 12-Pin WSON With PowerPAD™ Integrated Circuit Package, DRR — LM63635C (Top View)

表 5-1. Pin Functions

PIN					DESCRIPTION
TSSOP LM63635D	WSON LM63635D	WSON LM63635C	NAME	TYPE	
1, 2	1	1	SW	P	Regulator switch node. Connect to power inductor.
3	2	2	CBOOT	P	Bootstrap supply voltage for internal high-side driver. Connect a high-quality, 220nF capacitor from this pin to the SW pin.
4	3	4	VCC	A	Internal 5V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for regulator functions. Connect a high-quality, 1µF capacitor from this pin to PGND.
5	4	-	RT	A	Frequency programming input. Tie to VCC for 400kHz or to AGND for 2.1MHz or connect to an R_T timing resistor. See セクション 7.3.3 for details. Do not float.

表 5-1. Pin Functions (続き)

PIN					DESCRIPTION
TSSOP LM63635D	WSON LM63635D	WSON LM63635C	NAME	TYPE	
6	5	-	VSEL	A	Output voltage select input. Tie to VCC for 5V output or to AGND for 3.3V output; connect to a 10kΩ for an adjustable output. See セクション 7.3.2 for details. Do not float.
7	6	5	SYNC/ MODE	A	Mode selection and synchronization input. Tie to VCC for FPWM mode, AGND for AUTO mode, or supply an external synchronizing clock to this input.
8	7	6	$\overline{\text{RESET}}$	A	Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be open when not used.
9	8	7	FB	A	Feedback input to regulator. Connect to output capacitor for 5V or 3.3V fixed option or tap point of the feedback voltage divider for ADJ option. Do not float; do not ground.
10	9	9	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB.
11	10	10	EN	A	Enable input to regulator. High = ON, Low = OFF. Can be connected directly to VIN. Do not float.
12, 13	12	12	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitors directly to this pin and PGND.
14	11	3, 8, 11	NC	—	No internal connection to device
15, 16	13	13	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
17	13	13	DAP	G	Electrical ground and heat sink connection. Solder directly to system ground plane.
A = Analog, P = Power, G = Ground					

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended junction temperature range (1)

PARAMETER		MIN	MAX	UNIT
	VIN to PGND (HTSSOP package)	–0.3	38	V
	VIN to PGND (WSON package)	–0.3	42	V
	EN to AGND (HTSSOP package)	–0.3	38	V
	EN to AGND (WSON package)	–0.3	42	V
	SYNC/MODE to AGND	–0.3	6	V
	VOUT_SEL and RT to AGND	–0.3	5.5	V
	$\overline{\text{RESET}}$ to AGND	–0.3	16	V
	FB to AGND (Fixed VOUT mode)	–0.3	16	V
	FB to AGND (Adjustable VOUT mode)	–0.3	5.5	V
	AGND to PGND	–0.3	0.3	V
	SW to PGND for transients of less than 10ns (HTSSOP package)	–6	38	V
	SW to PGND for transients of less than 10ns (WSON package)	–6	42	V
	BOOT to SW	–0.3	5.5	V
	VCC to AGND	–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1) HBM ESD Clasification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD clasiffication Level C5	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended junction temperature range of –40°C to 150°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
	VIN to PGND (WSON package)	3.5	36	V
	VIN to PGND (HTSSOP package)	3.5	32	V
	EN (WSON package)	0	36	V
	EN (HTSSOP package)	0	32	V
	SYNC/MODE, VOUT_SEL and RT to AGND	0	5	V
	$\overline{\text{RESET}}$	0	5	V
	V_{OUT} (2)	1	20	V
	V_{CC}	2.7	5.25	V
	I_{OUT}, LM63635	0	3.25	A

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional. For ensured specifications, see the *Electrical Characteristics Table*.
(2) Under no conditions should the output voltage be allowed to fall below zero volts.

6.4 Thermal Information

THERMAL METRIC (1)		LM63635 DRR0012 (WSON) 12 PINS	LM63635 HTSSOP (PWP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	47.4	43.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.6	35.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	18.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	18.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.3	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information please see the ***Maximum Ambient Temperature*** section.

6.5 Electrical Characteristics

Limits apply over the junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	Minimum operating input voltage				3.5	V
I_Q	Non-switching input current; measured at VIN pin (2)	V_{EN} = 3.3V, V_{FB} = 1.2x regulation point		23	40	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0V		5.3	10	µA
V_{UVLO_R}	Minimum operating voltage threshold	Rising V_{IN}, I_{VCC} = 0A			3.5	V
V_{UVLO_F}	Minimum operating voltage threshold	Falling V_{IN}, I_{VCC} = 0A	2.6		3	V
I_{POR}	Pull down current on SW when OVP is triggered	V_{EN} = 0V V_{SW} = 5V	0.5	1.5	2.5	mA
ENABLE (EN PIN)						
V_{EN-VCC}	VCC enable voltage	V_{EN} rising		0.85		V
V_{EN-H}	Precision enable high level for VOUT	V_{EN} rising	1.425	1.5	1.575	V
V_{EN-L}	Precision enable low level for VOUT	V_{EN} falling	0.9	0.94		V
I_{LKG-EN}	Enable input leakage current	V_{EN} = 13.5V, WSON package	–100	0.2	300	nA
I_{LKG-EN}	Enable input leakage current	V_{EN} = 13.5V, HTSSOP package	–100	0.2	150	nA
OUTPUT VOLTAGE SELECTION (VSEL PIN)						
$R_{SEL-ADJ}$	Resistor range for valid adjustable output voltage selection at startup		8		50	kΩ
INTERNAL LDO						
V_{CC}	Internal VCC voltage	6V ≤ V_{IN} ≤ Max Operating V_{IN}	4.75	5	5.25	V
V_{CCM}	VCC Clamp Voltage	1mA sourced into VCC	5.25	5.55	5.8	V
VOLTAGE REFERENCE (FB PIN)						
V_{FB_ADJ}	Feedback voltage	V_{IN} = 3.5V - Max Operating V_{IN}	0.985	1	1.015	V
V_{FB_5V}	Feedback voltage	V_{IN} = 5.5V - Max Operating V_{IN}	4.925	5	5.075	V
V_{FB_3p3V}	Feedback voltage	V_{IN} = 3.8V - Max Operating V_{IN}	3.25	3.3	3.35	V
I_{FB_ADJ}	Input leakage current at FB PIN	FB = 1.0V		0.2	100	nA
I_{FB_5V}	Input leakage current at FB PIN	FB = 5.0V		2.89	3.4	µA
I_{FB_3p3V}	Input leakage current at FB PIN	FB = 3.3V		1.67	2	µA
CURRENT LIMITS						
I_{SC}	Short circuit high side current Limit	3.25A Version	3.9	4.4	5.4	A
$I_{LS-LIMIT}$	Low side current limit		3.2	3.7	4.4	A
$I_{PEAK-MIN}$	Minimum Peak Inductor Current			0.62	1.25	A
I_{L-NEG}	Negative current limit		–3.1	–2.2	–1.9	A
V_{HICCUP}	Hiccup threshold on FB pin		37	42	47	%

6.5 Electrical Characteristics (続き)

Limits apply over the junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD ($\overline{\text{RESET}}$ PIN)						
$V_{\overline{\text{RESET}}-HIGH}$	$\overline{\text{RESET}}$ upper threshold - Rising	% of FB voltage	110	112	115	%
$V_{\overline{\text{RESET}}-LOW}$	$\overline{\text{RESET}}$ lower threshold - Falling	% of FB voltage	91	93	95	%
$V_{\overline{\text{RESET}}-HYS}$	$\overline{\text{RESET}}$ hysteresis	% of FB voltage	1.1	1.8	2.5	%
$V_{\overline{\text{RESET}}\_VALID}$	Minimum input voltage for proper PG function	Measured when $V_{\overline{\text{RESET}}}$ < 0.4V with 10kΩ pullup to external 5V	0.7	1.04	1.25	V
$R_{\overline{\text{RESET}}}$	$\overline{\text{RESET}}$ ON resistance	V_{EN} = 5.0V, 1mA pull-up current		60	150	Ω
$R_{\overline{\text{RESET}}}$	$\overline{\text{RESET}}$ ON resistance	V_{EN} = 0V, 1mA pull-up current		40	125	Ω
OSCILLATOR (SYNC/MODE PIN)						
$V_{SYNC-HIGH}$	Sync input and mode high level threshold			1.5	1.8	V
$V_{SYNC-HYS}$	Sync input hysteresis			0.355		V
$V_{SYNC-LOW}$	Sync input and mode low level threshold		0.8	1.15		V
R_{SYNC}	Pulldown on MODE pin			100		kΩ
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET on-resistance	Load = 1A		93		mΩ
$R_{DS-ON-LS}$	Low-side MOSFET on-resistance	Load = 1A		61		mΩ
$V_{CBOOT-UVLO}$	C_{BOOT} - SW UVLO threshold (3)			2.13		V

(1) MIN and MAX limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turn to recharge the boot capacitor

6.6 Timing Characteristics

Limits apply over the junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMITS AND HICCUP						
N_{OC}	Number of switching current limit continuous events before hiccup is tripped			128		Cycles
t_{OC}	Overcurrent hiccup retry delay time		70	104	140	ms
t_{OC_active}	Time after soft start done timer before hiccup current protection is enabled		11	16	22	ms
SOFT START						
t_{SS}	Internal soft-start time		1	1.6	2.2	ms
t_{SS_DONE}	Soft-start done timer		5	8	11	ms
POWER GOOD ($\overline{\text{RESET}}$ PIN) and OVERVOLTAGE PROTECTION						
t_{dg}	$\overline{\text{RESET}}$ edge deglitch delay		10	17	30	µs
$t_{RISE-DELAY}$	$\overline{\text{RESET}}$ active time	Time FB must be valid before $\overline{\text{RESET}}$ is released.	2	3	5	ms
OSCILLATOR (SYNC/MODE PIN)						
$t_{ON\_OFF-SYNC}$	Sync input ON and OFF-time		100			ns

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are verified through correlation usingStatistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

6.7 Switching Characteristics

Limits apply over the junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following s apply: V_{IN} = 13.5V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LIMITS (SW PINS)						
t_{ON-MIN}	Minimum switch on-time	V_{IN} = 12V, I_{SW} = 1A		50	75	ns
$t_{OFF-MIN}$	Minimum switch off-time	V_{IN} = 5V		50	100	ns
t_{ON-MAX}	Maximum switch on-time	HS timeout in dropout	5.4	7	10	µs
OSCILLATOR (RT and SYNC PINS)						
f_{OSC}	Internal oscillator frequency	RT = GND	1.85	2.1	2.35	MHz
f_{OSC}	Internal oscillator frequency	RT = VCC	360	400	440	kHz
f_{ADJ1}		RT = 66.5kΩ, 1%		240		kHz
f_{ADJ2}		RT = 7.15kΩ, 1%		2200		kHz
f_{SYNC}	Synchronization Frequency Range		250		2200	kHz
SPREAD SPECTRUM						
f_{PSS} (2)	Spread spectrum pseudo random pattern frequency	f_{OSC} = 2.1MHz		0.98		Hz
f_{SPREAD}	Spread of internal oscillator with Spread Spectrum Enabled	LM63635 (HTSSOP package)	–3.6		3.6	%
f_{SPREAD}	Spread of internal oscillator with Spread Spectrum Enabled	LM63635 (WSON package)	–5		5	%

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are verified through correlation usingStatistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

6.8 System Characteristics

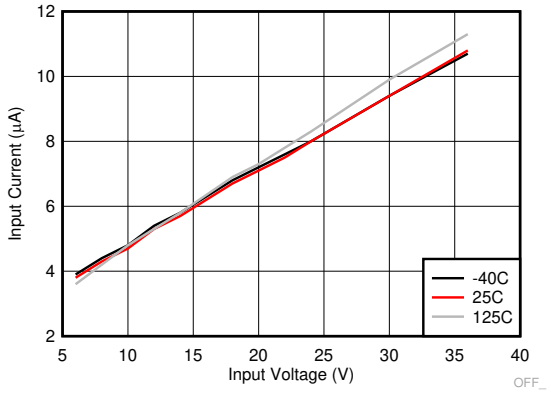
The following specifications apply only to the typical applications circuit with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A, R_{FBT} = 1MΩ		23		µA
V_{DROP}	Dropout voltage; (V_{IN} – V_{OUT})	V_{OUT} = 5V, I_{OUT} = 1A, F_{SW} = 1850kHz		0.95		V
V_{DROP}	Dropout voltage; (V_{IN} – V_{OUT})	V_{OUT} = 5V, I_{OUT} = 1A, V_{OUT} – 1% of regulation, F_{SW} = 140kHz		150		mV
D_{MAX}	Maximum switch duty cycle (2)	V_{IN} = V_{OUT} = 12V, I_{OUT} = 1A		98		%
VOLTAGE REFERENCE (FB PIN)						
V_{OUT} (1)	V_{OUT} = 5V	V_{IN} = 7V to 30V, I_{OUT} = 1A to full load, CCM	–1.5		1.5	%
	V_{OUT} = 5V	V_{IN} = 7V to 30V, I_{OUT} = 0A to full load, AUTO mode	–1.5		2.5	%
V_{OUT} (1)	V_{OUT} = 3.3V	V_{IN} = 3.8V to 30V, I_{OUT} = 1A to full load, CCM	–1.5		1.5	%
	V_{OUT} = 3.3V	V_{IN} = 3.8V to 30V, I_{OUT} = 0A to full load, AUTO mode	–1.5		2.5	%
t_{SYNC-L}	Delay from sync clock staying low to PFM entry			100		ns
t_{SYNC-H}	Delay from sync clock staying high to default frequency			100		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	Shutdown temperature	155	163	175	°C
T_{SDR}	Thermal shutdown temperature	Recovery temperature		150		°C

(1) Deviation is with respect to V_{IN} =13.5V, I_{OUT} = 1A.
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / (t_{ON-MAX} + $T_{OFF-MIN}$). D_{MAX} = t_{ON-MAX} /(t_{ON-MAX} + $t_{OFF-MIN}$).

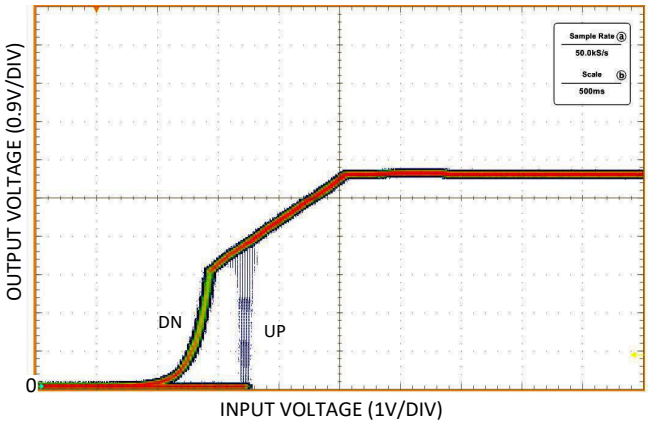
6.9 Typical Characteristics

Unless otherwise specified the following conditions apply: T_A = 25°C, V_{IN} = 13.5 V



EN = 0 V

図 6-1. Input Supply Current in Shutdown Mode



I_{OUT} = 1 mA

See 図 8-26

図 6-2. UVLO Thresholds

7 Detailed Description

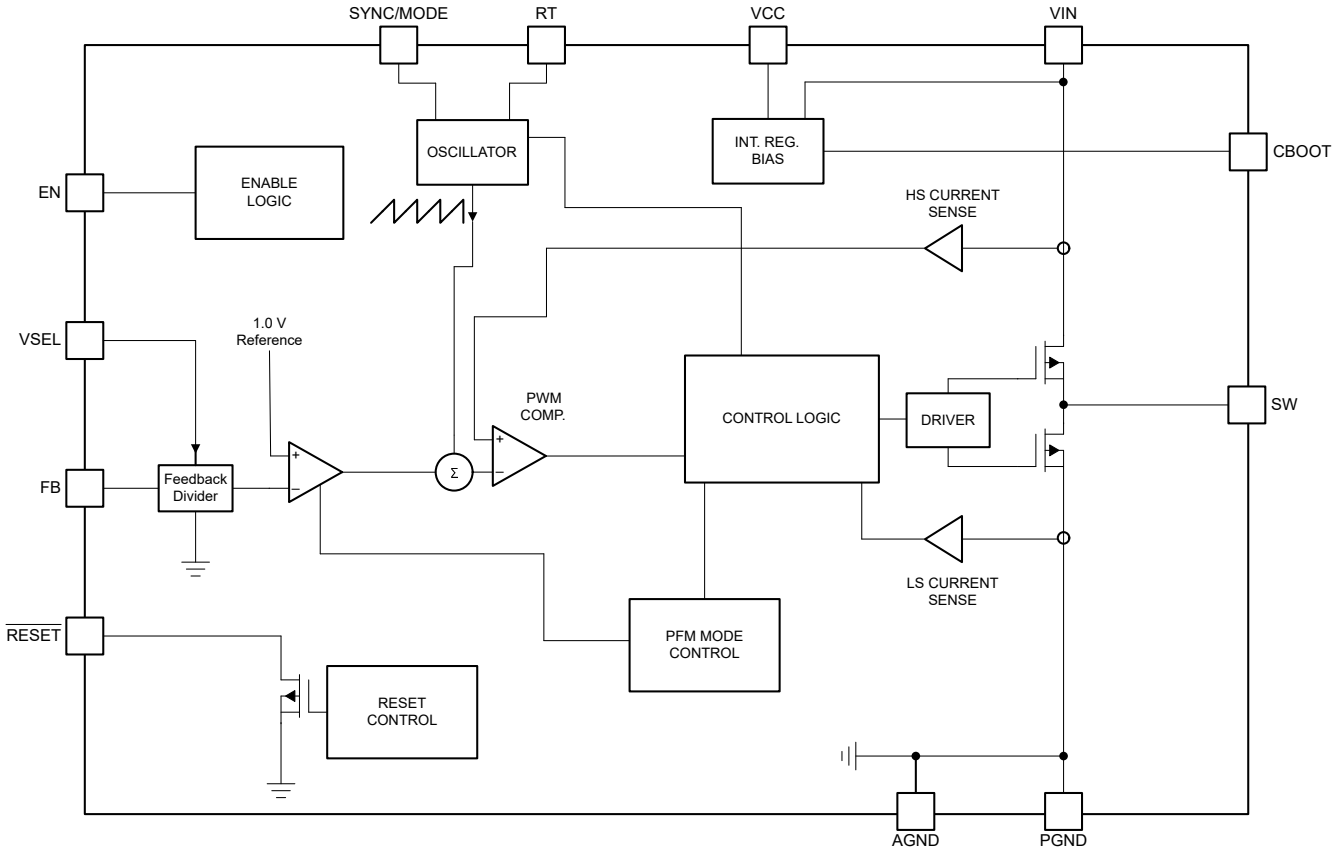
7.1 Overview

The LM63635-Q1 device is a synchronous peak-current-mode buck regulator designed for a wide variety of automotive applications. The regulator automatically switches modes between PFM and PWM, depending on load. At heavy loads, the device operates in PWM at a constant switching frequency. At light loads, the mode changes to PFM with diode emulation, allowing DCM. This reduces the input supply current and keeps efficiency high. The device features the following:

- Adjustable switching frequency
- Forced PWM mode (FPWM)
- Frequency synchronization
- Selectable output voltage

The $\overline{\text{RESET}}$ output allows easy system sequencing. In addition, internal compensation reduces design time and requires fewer external components than externally compensated regulators.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Sync/Mode Selection

The LM63635-Q1 features selectable operating modes through the SYNC/MODE input. 表 7-1 shows the selection programming. Mode changes can be made *on the fly* anytime after the device is powered up. TI does not recommend that this input be allowed to float, however, an internal 100 kΩ pulls the input to ground if left floating. The value of this internal resistor and the logic thresholds for this input can be found in the *Electrical Characteristics*. See セクション 7.4 for details of the operating modes.

表 7-1. Mode Selection Settings

SYNC/MODE INPUT	MODE
VCC	FPWM
AGND	AUTO
Synchronizing clock	FPWM; synchronized to external clock
Float (not recommended)	AUTO

7.3.2 Output Voltage Selection

The output voltage of the LM63635D-Q1 is set by the condition of the VSEL input. The condition of this input is tested when the device is first enabled. After the converter is running, the voltage selection is fixed and cannot be changed until the next power-on cycle. 表 7-2 shows the selection programming. The LM63635D-Q1 contains an integrated voltage divider connected to the FB input. The converter regulates the voltage on the FB input to 5-V, 3.3-V, or 1-V, as selected. In ADJ mode, the voltage on the FB input is regulated to 1-V and the internal divider is disabled. In this case, an external voltage divider is used to set the desired output voltage anywhere within the recommended operating range. ADJ mode is programmed by connecting 10 kΩ from the VSEL input to ground. Although not recommenced, if this input is left floating, the device enters ADJ mode. See セクション 8.2.2.2 for details of selecting the FB divider resistors.

For the LM63635C-Q1 variant, the output voltage is set by external feedback resistors and does not have the VSEL pin. See セクション 6 for ensured specifications regarding the accuracy of the FB voltage and input current to the FB pin.

Providing internal voltage dividers for the 5-V and 3.3-V modes saves external components, reducing both board space and component cost. The relatively large values of the internal dividers reduce the load on the output, helping to improve the light load efficiency of the converter. In addition, because the divider is inside the device, it is less likely to pick up externally generated noise.

表 7-2. Output Voltage Settings

VSEL INPUT	OUTPUT VOLTAGE
VCC	5 V
AGND	3.3 V
10 kΩ to AGND	ADJ
Float (not recommended)	ADJ

7.3.3 Switching Frequency Selection

The switching frequency is set by the condition of the RT input. The condition of this input is tested when the device is first enabled. After the converter is running, the switching frequency selection is fixed and cannot be changed until the next power-on cycle. 表 7-3 shows the selection programming. In the adjustable frequency mode, the switching frequency can be set between 250 kHz and 2200 kHz by proper selection of the value of R_T. The curve in 図 7-1 indicates the required resistor value for R_T to set a desired switching frequency. TI does not recommend that this input be allowed to float; the switching action ceases with no generated output voltage under this condition.

$$R_T = \frac{15770}{f_{SW}} \quad (1)$$

where

- RT = value of RT timing resistor in kΩ
- f_{SW} = switching frequency in kHz

表 7-3. Switching Frequency Settings

RT INPUT	SWITCHING FREQUENCY
VCC	400 kHz
AGND	2100 kHz
R_T to AGND	Adjustable according to R_T value
Float (not recommended)	No switching

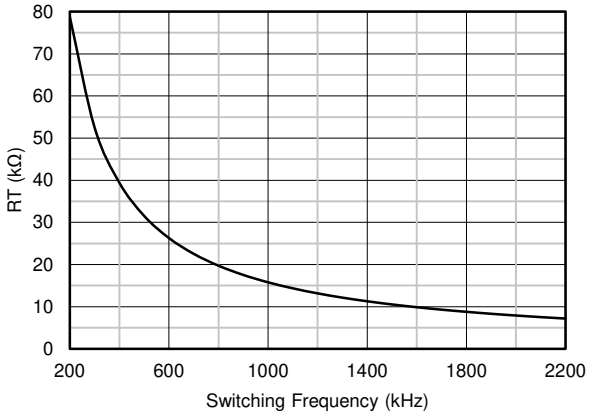


図 7-1. Switching Frequency versus R_T

7.3.3.1 Spread Spectrum Option

The LM63635-Q1 is available with a spread spectrum clock dithering feature. This feature uses a pseudo-random pattern to dither the internal clock frequency. The pattern repeats at a 0.98-Hz rate while the depth of modulation is ±3%.

The purpose of the spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. In most systems containing the LM63635-Q1 device, low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The LM63635-Q1 device use a ±3% spread of frequencies which spreads energy smoothly across the FM band but is small enough to limit subharmonic emissions below the switching frequency.

7.3.4 Enable and Start-Up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see セクション 8.2.2.8). Applying a voltage greater than V_{EN-VCC} causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to V_{EN-H} fully enables the device, allowing it to enter start-up mode and begin the soft-start period. When the EN input is brought below V_{EN-L}, the regulator stops running and enters standby mode. Further decrease in the EN voltage to below V_{EN-VCC} completely shuts down the device. 図 7-2 shows this behavior. The EN input can be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in セクション 6.

The LM63635-Q1 uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. 図 7-3 shows a typical start-up waveform along with typical timings. After EN goes high, there is a delay of about 1 ms before the soft-start period begins. The output voltage begins to rise and reaches the final value in about 1.5 ms (t_{ss}). After a delay of about 3 ms ($t_{rise-delay}$), the $\overline{\text{RESET}}$ flag goes high. During start-up, the device is not allowed to enter FPWM mode until the $t_{ss-done}$ time has elapsed. This time is measured from the rising edge of EN.

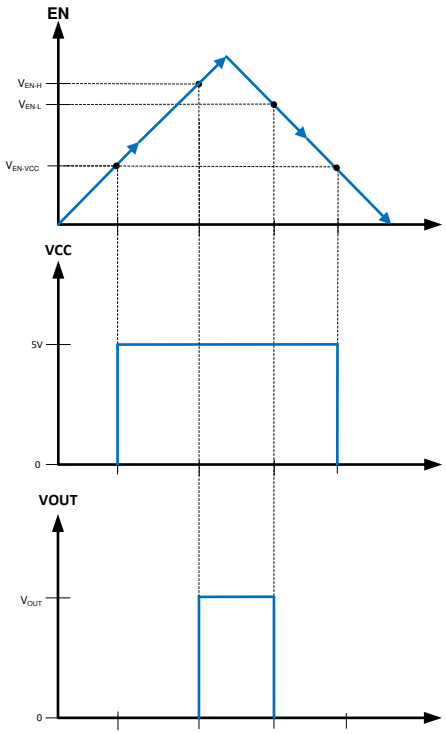


図 7-2. Precision Enable Behavior

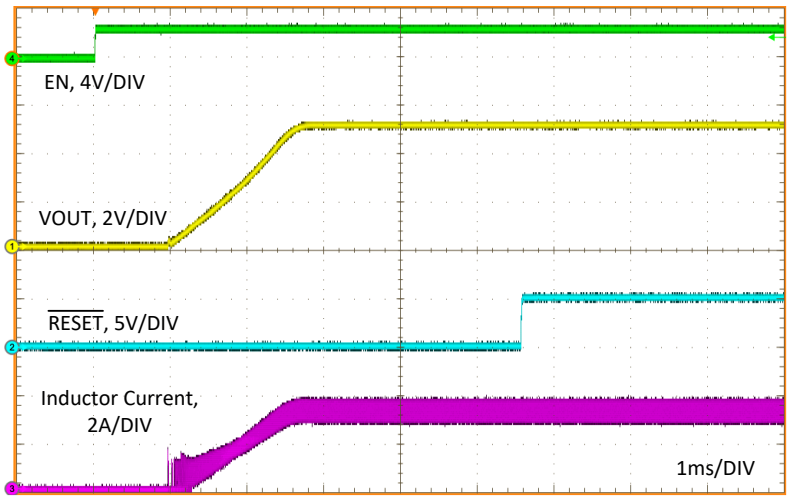


図 7-3. Typical Start-up Behavior V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3.25 A

7.3.5 $\overline{\text{RESET}}$ Flag Output

The $\overline{\text{RESET}}$ flag function ($\overline{\text{RESET}}$ output pin) of the LM63635-Q1 device can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{dg} do not trip the $\overline{\text{RESET}}$ flag. After the FB voltage has returned to the regulation value and after a delay of $t_{rise\text{-}delay}$, the $\overline{\text{RESET}}$ flag goes high. $\overline{\text{RESET}}$ operation can best be understood by reference to 図 7-4 and 図 7-5.

The $\overline{\text{RESET}}$ output consists of an open-drain NMOS, requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either VCC or V_{OUT} through an appropriate resistor, as desired. Pullup resistor values in the range of 10 kΩ to 100 kΩ are reasonable. If this function is not needed, the $\overline{\text{RESET}}$ pin can be left floating. When EN is pulled low, the flag output is also forced low. With EN low, $\overline{\text{RESET}}$ remains valid as long as the input voltage is ≥ 1.2 V (typical). Limit the current into the $\overline{\text{RESET}}$ flag pin to approximately 5 mA D.C. The maximum current is internally limited to approximately 50 mA when the device is enabled and approximately 65 mA when the device is disabled. The internal current limit protects the device from any transient currents that can occur when discharging a filter capacitor connected to this output.

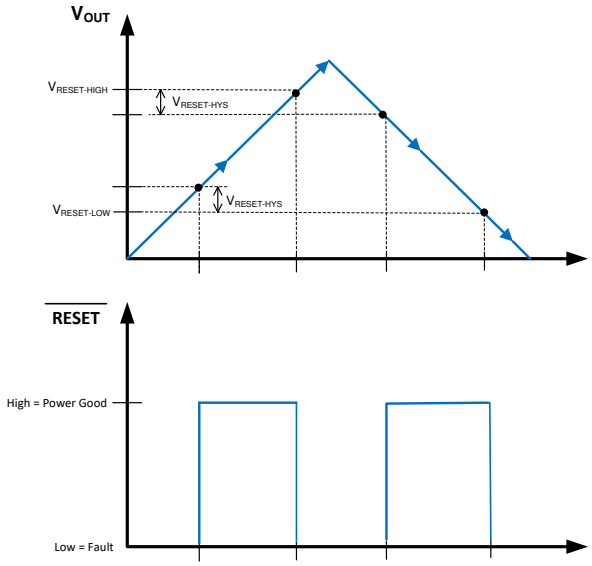


図 7-4. Static $\overline{\text{RESET}}$ Operation

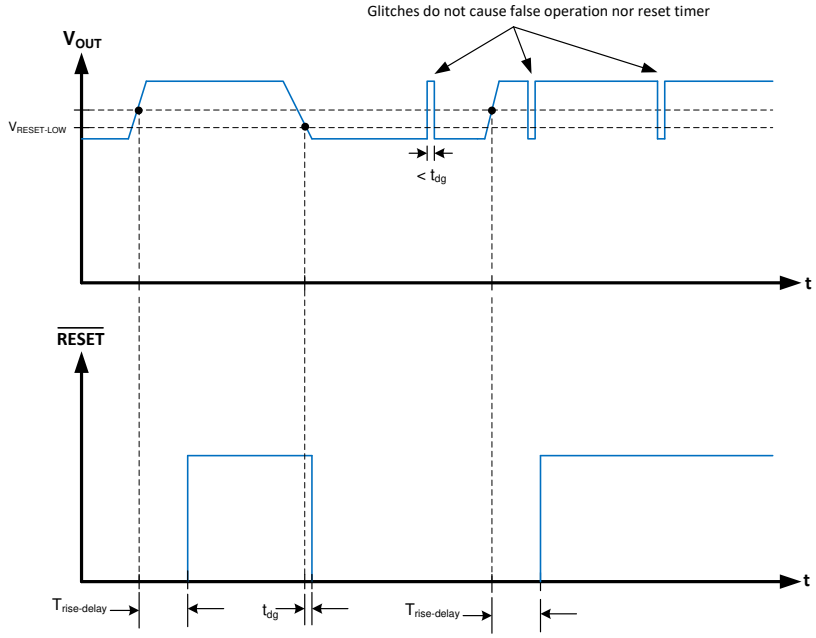


図 7-5. $\overline{\text{RESET}}$ Timing Behavior

7.3.6 Undervoltage Lockout and Thermal Shutdown and Output Discharge

The LM63635-Q1 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When V_{IN} reaches approximately V_{POR-R}, the device is ready to receive an EN signal and start up. When V_{IN} falls below V_{POR-F}, the device shuts down, regardless of EN status. Because the LDO is in dropout during these transitions, the above values roughly represent the VCC voltage levels during the transitions. An extended input voltage UVLO can also be accomplished as shown in セクション 8.2.2.8.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 163°C, the device shuts down; re-start occurs when the temperature falls to about 150°C.

The LM63635-Q1 features an output voltage discharge FET connected from the SW pin to ground. This FET is activated when the EN input is below V_{EN-L}, or when the output voltage exceeds $V_{RESET-HIGH}$. This way, the output capacitors are discharged through the power inductor. At output voltages above about 5 V, the discharge current is approximately constant at I_{POR} or about 1.4 mA. Below this voltage, the FET characteristic looks approximately resistive at a value of 2.5 kΩ.

7.4 Device Functional Modes

7.4.1 Overview

In typical usage, the device is put in AUTO mode (SYNC/MODE pin = ground). In AUTO mode, the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM where the switching frequency is varied to regulate the output voltage. At higher loads, the mode changes to PWM with the switching frequency set by the condition of the RT pin (see セクション 7.3.3).

In PWM mode, the regulator operates as a current mode, constant frequency converter using PWM to regulate the output voltage. While operating in this mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM mode, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK-MIN}$. The periodicity of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see the *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. See セクション 8.2.4 for output voltage variation with load in PFM mode. 図 7-6 and 図 7-7 show the typical switching waveforms in PFM and PWM.

There are four cases where the switching frequency does not conform to the condition set by the RT pin:

- Light load operation (AUTO mode)
- Dropout
- Minimum on-time operation
- Current limit

Under all of these cases, the switching frequency *folds back*, meaning it is less than that programmed by the RT control pin. During these conditions, by definition, the output voltage remains in regulation, except for current limit operation.

When the device is placed in forced PWM mode (FPWM), the switching frequency remains constant as programmed by the RT pin for all load conditions. This mode essentially turns off the light-load PFM frequency foldback mode detailed in セクション 7.4.2. See セクション 7.3.1 and セクション 7.4.2.1 for details.

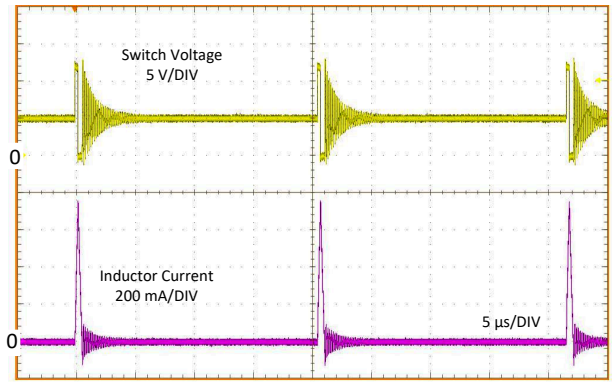


図 7-6. Typical PFM Switching Waveforms V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 10 mA

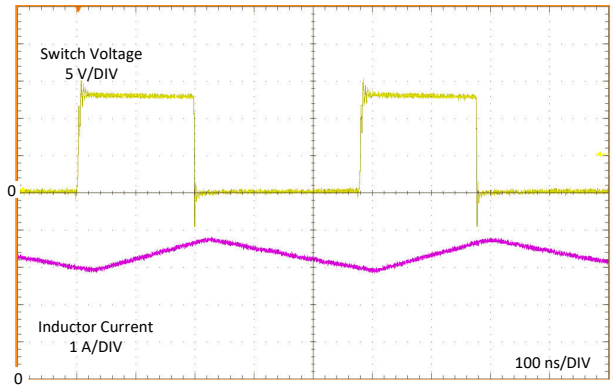


図 7-7. Typical PWM Switching Waveforms Without Spread Spectrum V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3.25 A, f_{SW} = 2100 kHz

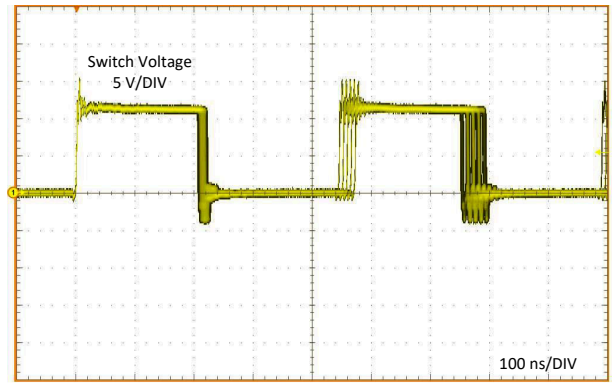


図 7-8. Typical PWM Switching Waveforms With Spread Spectrum V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 2.5 A, f_{SW} = 2100 kHz

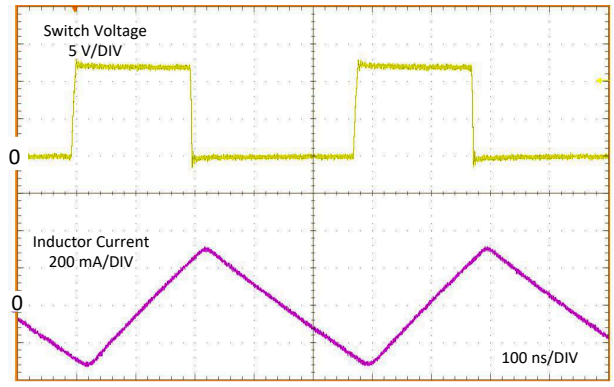


図 7-9. Typical PWM Switching Waveforms FPWM V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 0 A, f_{SW} = 2100 kHz

7.4.2 Light Load Operation

During light load operation, the device is in PFM mode with DEM. This provides high efficiency at the lower load currents. The actual switching frequency and output voltage ripple depend on the input voltage, output voltage, and load. The output current at which the device moves in and out of PFM can be found in セクション 8.2.4. The output current for mode change depends on the input voltage, inductor value, and the programmed switching frequency. The curves apply for the BOM shown in 表 8-3. At higher programmed switching frequencies, the load at which the mode change occurs is greater. For applications where the switching frequency must be known for a given condition, the transition between PFM and PWM must be carefully tested before the design is finalized. Alternatively, the mode can be set to FPWM.

7.4.2.1 Sync/FPWM Operation

The forced PWM mode (FPWM) can be used to turn off AUTO mode and force the device to switch at the frequency programmed by the RT pin, even for small loads. This has the disadvantage of lower efficiency at light loads.

When a valid clock signal is present on the SYNC/MODE input, the switching frequency is locked to the external clock. The device mode is also FPWM. The mode can be changed dynamically by the system. See 図 7-10 for typical examples of SYNC/MODE function changes.

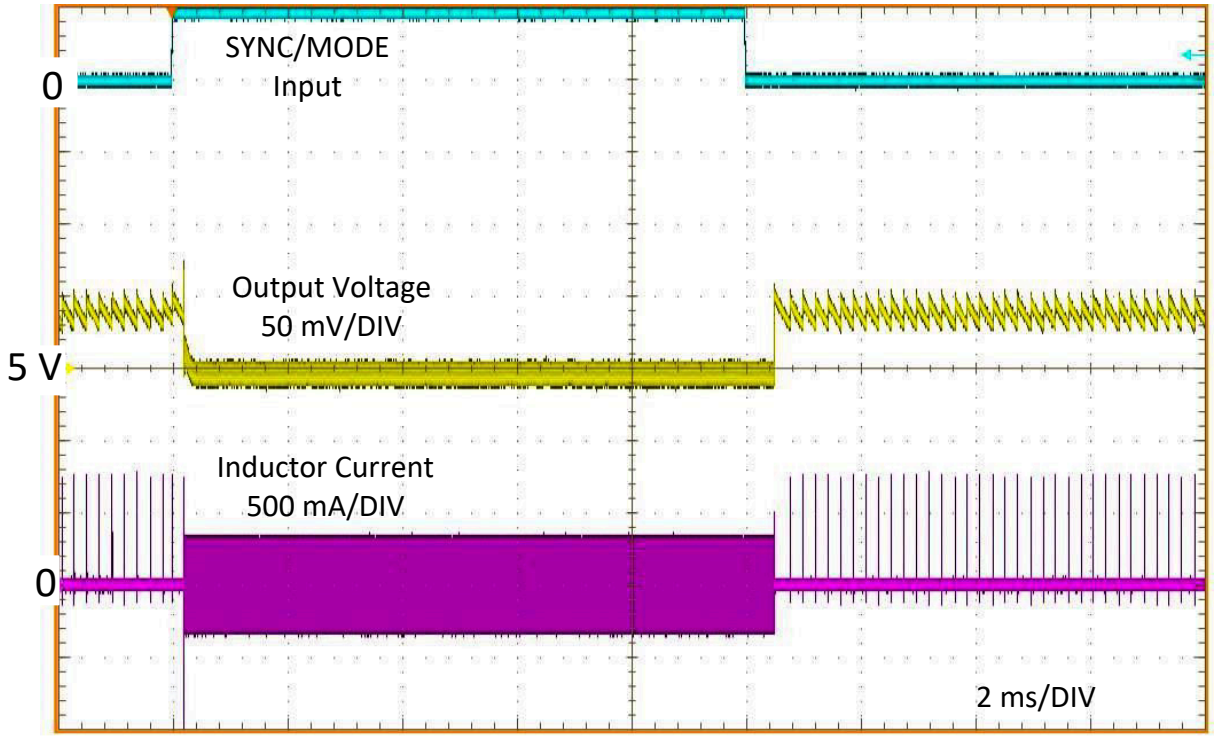


図 7-10. Typical Transition from FPWM to AUTO Mode V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 1 mA

7.4.3 Dropout Operation

The dropout performance of any buck regulator is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off-time of the high-side MOSFET starts to approach the minimum value (see セクション 6). Beyond this point, the switching can become erratic and the output voltage can fall out of regulation. To avoid this problem, the LM63635-Q1 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. There are two definitions of *dropout* voltage used in this data sheet. For both definitions, the dropout voltage is the difference between the input and output voltage under a specific condition. For the first definition, the difference is taken when the switching frequency has dropped to 1850 kHz (obviously this applies to cases where the nominal switching frequency is >1850 kHz). For this condition, the output voltage is within regulation. For the second definition, the difference is taken when the output voltage has fallen by 1% of the nominal regulation value. In this condition, the switching frequency has reached the lower limit of about 130 kHz. See セクション 8.2.4 for details on these characteristics. Typical overall dropout characteristics can be found in 図 7-11.

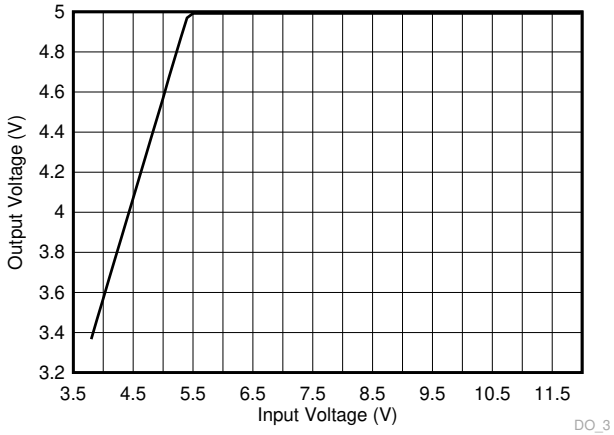


図 7-11. Overall Dropout Characteristic V_{OUT} = 5 V, I_{OUT} = 3.25 A

7.4.4 Minimum On-time Operation

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LM63635-Q1 automatically reduces the switching frequency when the minimum on-time limit is reached. This way, the converter can regulate the lowest programmable output voltage at the maximum input voltage. Use 式 2 to find an estimate for the approximate input voltage for a given output voltage before frequency foldback occurs. The values of t_{ON} and f_{SW} can be found in セクション 6. As the input voltage is increased, the switch on-time (duty-cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops while the on-time remains fixed. This relationship is highlighted in f_{SW} *versus* V_{IN} curves in セクション 8.2.4.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \times f_{SW}} \tag{2}$$

7.4.5 Current Limit and Short-Circuit Operation

The LM63635-Q1 incorporates both peak and valley inductor current limits to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current run-away during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. A "hiccup" type mode is also incorporated for sustained short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see the *Glossary*). The nominal value of this limit is about 0 A.

As the device is overloaded, a point is reached where the valley of the inductor current cannot reach below $I_{LS\text{-}LIMIT}$ before the next clock cycle. When this event occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, but the output voltage remains in regulation. As the overload is increased, both the inductor current ripple and peak current increase until the high-side current limit, I_{SC}, is reached. When this limit is activated, the switch duty cycle is reduced and the output voltage falls out of regulation. This represents the maximum output current from the converter and is given approximately by 式 3. The output voltage and switching frequency continue to drop as the device moves deeper into overload while the output current remains at approximately I_{OMAX}. If the inductor ripple current is large, the high-side current limit can be tripped before the low-side limit is reached. In this case, 式 4 gives the approximate maximum output current.

$$I_{OMAX} \approx \frac{I_{SC} + I_{LS-LIMIT}}{2} \tag{3}$$

$$I_{OMAX} \approx I_{SC} - \frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \quad (4)$$

If a severe overload or short circuit causes the FB voltage to fall below V_{HICCUP}, the convert enters "hiccup" mode. V_{HICCUP} represents about 40% of the nominal programmed output voltage. In this mode, the device stops switching for t_{OC}, or about 100 ms, and then goes through a normal restart with soft start. If the short-circuit condition remains, the device runs in current limit for a little longer than t_{OC_active}, or about 23 ms, and then shuts down again. This cycle repeats (as shown in 図 7-12) as long as the short-circuit condition persists. This mode of operation reduces the temperature rise of the device during a sustained short on the output. The output current in this mode is approximately 20% of I_{OMAX}. After the output short is removed and the t_{OC} delay is passed, the output voltage recovers normally as shown in 図 7-13 .

See 図 7-14 for the overall output voltage versus output current characteristic.

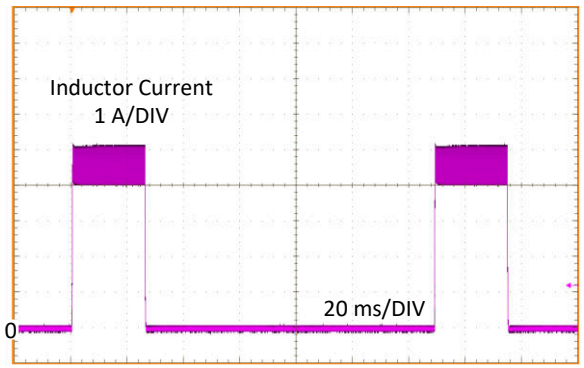


図 7-12. Inductor Current Burst in Short-Circuit Mode

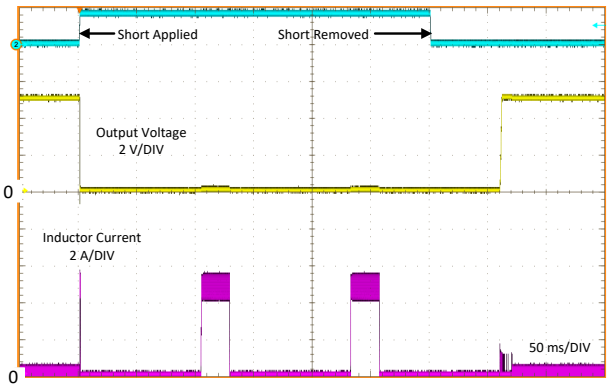


図 7-13. Short-Circuit Transient and Recovery

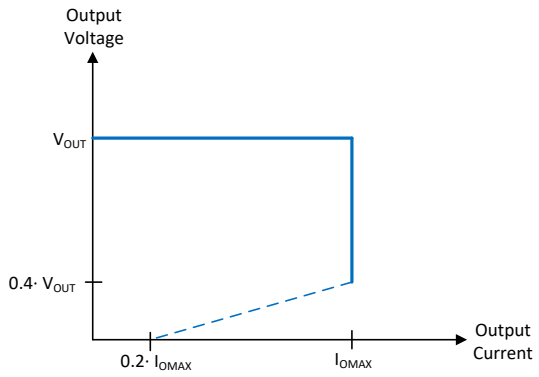


図 7-14. Output Voltage versus Output Current in Current Limit

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LM63635-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3.25 A. The following design procedure can be used to select components for the LM63635D-Q1.

注

In this data sheet, the *effective* value of capacitance is defined as the actual capacitance under D.C. bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

8.2 Typical Application

図 8-1 shows a typical application circuit for the LM63635D-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, see 表 8-1 for typical component values.

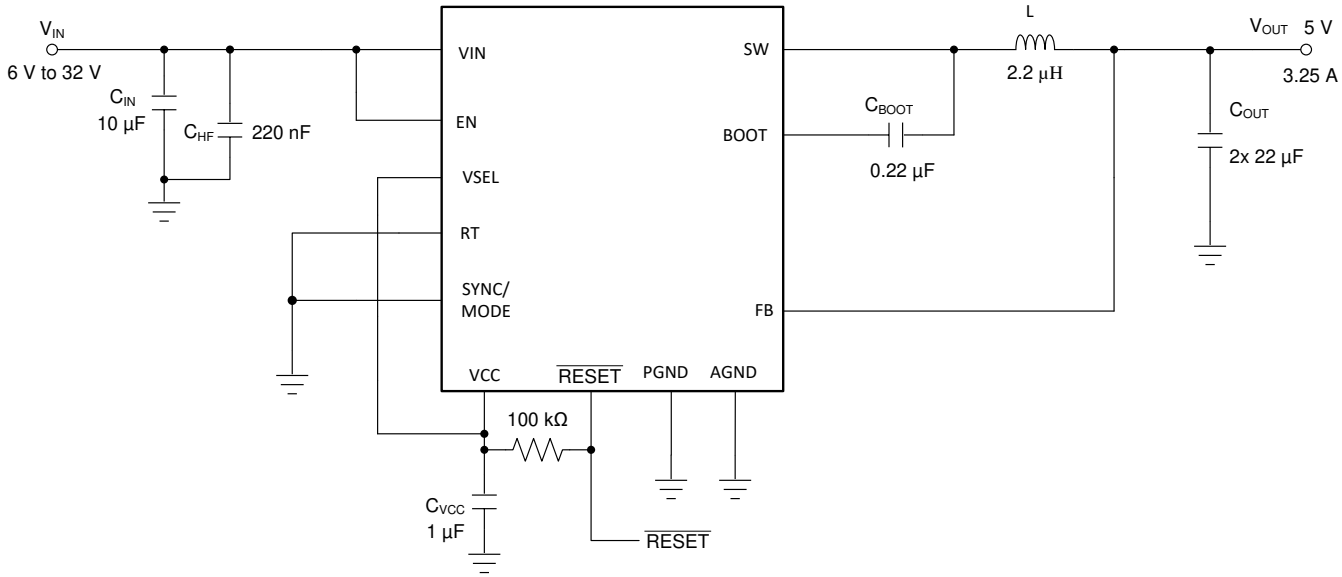


図 8-1. Example Application Circuit V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3.25 A, f_{SW} = 2.1 MHz

表 8-1. Typical External Component Values for 3.25-A Output Current

f_{SW} (kHz)	V_{OUT}	L (µH)(1)	TYPICAL(2) C_{OUT}	MINIMUM(2) C_{OUT}	VSEL	RT	C_{IN}	C_{BOOT}	C_{VCC}
400	3.3	10	3 × 22 µF	2 × 22 µF	AGND	VCC	10 µF + 220 nF	220 nF	1 µF
2100	3.3	2.2	2 × 22 µF	1 × 22 µF + 1 x 10 µF	AGND	AGND	10 µF + 220 nF	220 nF	1 µF
400	5	10	3 × 22 µF	2 × 22 µF	VCC	VCC	10 µF + 220 nF	220 nF	1 µF
2100	5	2.2	2 × 22 µF	1 × 22 µF + 1 x 10 µF	VCC	AGND	10 µF + 220 nF	220 nF	1 µF

(1) See the セクション 8.2.2.3.
(2) See the セクション 8.2.2.4.

8.2.1 Design Requirements

表 8-2 provides the parameters for the detailed design procedure:

表 8-2. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V (6 V to 32 V)
Output voltage	5-V
Maximum output current	0 A to 3.25 A
Switching frequency	2.1 MHz

8.2.2 Detailed Design Procedure

The following design procedure applies to 図 8-1 and 表 8-2.

8.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence, a more compact design. There are several options to set the switching frequency of the LM63635-Q1. For the LM63635D-Q1, either the RT or the SYNC pin can be used to set the switching frequency. For the LM63635C-Q1, the internal (default) frequency is set at 2.1 MHz or can be set externally via the SYNC pin. When the SYNC pin is being used, avoid asserting or de-asserting the SYNC signal during operation to prevent disturbances in the output voltage. For the application example, the switching frequency (F_{sw}) was chosen to be 2100 kHz.

8.2.2.2 Setting the Output Voltage

The output voltage of the LM63635D-Q1 is set by the condition of the VSEL input. This example requires a 5-V output, so the VSEL input is connected to VCC and the FB input is connected directly to the output capacitor.

For cases where the desired output voltage is other than 5-V or 3.3-V or using the LM63635C-Q1 variant, an external feedback divider is required. As shown in 図 8-2, the divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. In this case, a 10-kΩ resistor is connected from the VSEL input to ground. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, 1-V. The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity, but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ with a maximum value of 1 MΩ. If 1 MΩ is selected for R_{FBT}, then a feedforward capacitor must be used across this resistor to provide adequate loop phase margin (see セクション 8.2.2.2.1). After R_{FBT} is selected, 式 5 is used to select R_{FBB}. V_{REF} is nominally 1 V.

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \quad (5)$$

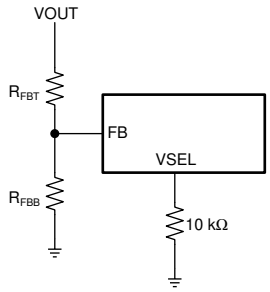


図 8-2. Feedback Divider for Adjustable Output Voltage Setting

8.2.2.2.1 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT} in combination with the parasitic capacitance at the FB pin can create a small signal pole that interferes with the loop stability. A C_{FF} helps mitigate this effect. 式 6 can be used to estimate the value of C_{FF}. The value found with 式 6 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

$$C_{FF} < \frac{V_{OUT} \times C_{OUT}}{120 \times R_{FBT} \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{6}$$

8.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Larger values of ripple current can restrict the maximum output current, before current limit is reached. This trade-off can be examined with the help of 式 3 and the ensured current limits found in セクション 6. Smaller values of ripple current reduce the SNR of the current mode controller and can lead to increased jitter in the duty cycle. Both the inductor and switching frequency tolerance have an impact on the selection of ripple current, and, therefore, inductor value. Use the maximum device current when calculating the ripple current for applications with much smaller maximum load than the maximum available from the device. The ratio of inductor ripple current over maximum output current is designated as K in the following equations. 式 7 can be used to determine the value of inductance. K = 0.2 was chosen for this example and L = 2.1 µH inductance was found. A standard value of 2.2 µH was selected. This gives a new K = 0.19.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUTmax}} \times \frac{V_{OUT}}{V_{IN}} \tag{7}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{SC} (see セクション 6). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

To avoid subharmonic oscillation, the inductance value must not be less than that given in 式 8. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L_{MIN} \geq M \times \frac{V_{OUT}}{f_{SW}} \tag{8}$$

where

- M = 0.37 for 3.25 A device

8.2.2.4 Output Capacitor Selection

The value of the output capacitor and the ESR determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements rather than the output voltage ripple. Use 式 9 to estimate a lower bound on the total output capacitance, and an upper bound on the ESR, which are required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT} \times K} \times \left[(1-D) \times (1+K) + \frac{K^2}{12} \times (2-D)\right] \tag{9}$$

$$ESR \leq \frac{(2+K) \times \Delta V_{OUT}}{2 \times \Delta I_{OUT} \times \left[1 + K + \frac{K^2}{12} \times \left(1 + \frac{1}{(1-D)}\right)\right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = ripple factor from セクション 8.2.2.3

After the output capacitor and ESR have been calculated, use 式 10 to check the peak-to-peak output voltage ripple, V_r.

$$V_r \cong \Delta I_L \times \sqrt{ESR^2 + \frac{1}{(8 \times f_{SW} \times C_{OUT})^2}} \tag{10}$$

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

This example requires a ΔV_{OUT} of ≤ 200 mV for an output current step of ΔI_{OUT} = 3.25 A. 式 9 gives a minimum value of 28 µF and a maximum ESR of 0.056 Ω. Assuming a 20% tolerance and a 10% bias de-rating, the user arrives at a minimum capacitance of 39 µF. This can be achieved with a bank of 2 × 22-µF, 16-V, ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel with the ceramics to build up the required value of capacitance. When using a mixture of aluminum and ceramic capacitors, use the minimum recommended value of ceramics and add aluminum electrolytic capacitors as needed.

In general, use a capacitor rating of at least 10 V for output voltages of 3.3 V or less, and use a capacitor of 16 V or more for output voltages of 5 V and above.

The recommendations given in 表 8-1 provide typical and minimum values of output capacitance for the given conditions. These values are the rated or nameplate figures. If the minimum values are to be used, the design must be tested over all of the expected application conditions, including input voltage, output current, and ambient temperature. This testing must include both bode plot and load transient assessments. The maximum

value of total output capacitance must be limited to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can help reduce spikes on the output caused by inductor and board parasitics.

8.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 4.7 µF of ceramic capacitance is required on the input of the LM63635-Q1, connected directly between VIN and PGND. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. More input capacitance is required for larger output currents. In addition, a small case size, 220-nF ceramic capacitor must be used at the input as close a possible to the regulator, typically within 1 mm of the VIN and PGND pins. This provides a high frequency bypass for the control circuits internal to the device. For this example, a 10-µF, 50-V, X7R (or better) ceramic capacitor is chosen. Two 4.7-µF capacitors can also be used. The 220 nF must also be rated at 50 V with an X7R dielectric and preferably a small case size, such as an 0603.

Many times, it is desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. Use 式 11 to calculate the approximate RMS current. This value must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{11}$$

8.2.2.6 C_{BOOT}

The LM63635-Q1 requires a bootstrap capacitor to be connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 220 nF and at least 16 V is required.

8.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to PGND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the $\overline{\text{RESET}}$ function and as a logic supply for the various control inputs of the device. A value of 100 kΩ is a good choice for the $\overline{\text{RESET}}$ flag pullup resistor. The nominal output voltage on VCC is 5 V.

8.2.2.8 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This need can be accomplished by using the circuit shown in 図 8-3. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ. Then, 式 12 is used to calculate R_{ENT} and V_{OFF}.

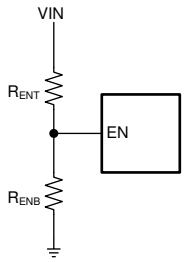


図 8-3. Setup for External UVLO Application

$$R_{ENT} = R_{ENB} \times \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \quad (12)$$
$$V_{OFF} = V_{En-l} \times \left(\frac{V_{ON}}{V_{EN-H}} \right)$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

8.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the LM63635-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device, and PCB combination. The maximum internal die temperature for the LM63635-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 13 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. Note that these curves include the power loss in the inductor. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. The data given for $R_{\theta JC(bott)}$ and Ψ_{JT} can be useful when determining thermal performance. See the *Semiconductor and IC Package Thermal Metrics Application Report* for more information and the resources given at the end of this section.

$$I_{OUTmax} = \frac{\left(T_J - T_A\right)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}} \quad (13)$$

where

- η = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The HTSSOP and the DRR0012 package use a die attach paddle, or "thermal pad" (DAP), to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Typical examples of $R_{\theta JA}$ versus copper board area can be found in 図 8-4 and 図 8-5 . The copper area given in the graph is for each layer. The top and bottom layers are 2-oz. copper each, while the inner layers are 1 oz. 図 8-6 shows a typical curve of maximum output current versus ambient temperature. This data was taken with a device and PCB combination, giving an $R_{\theta JA}$ of approximately 22°C/W. Remember that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

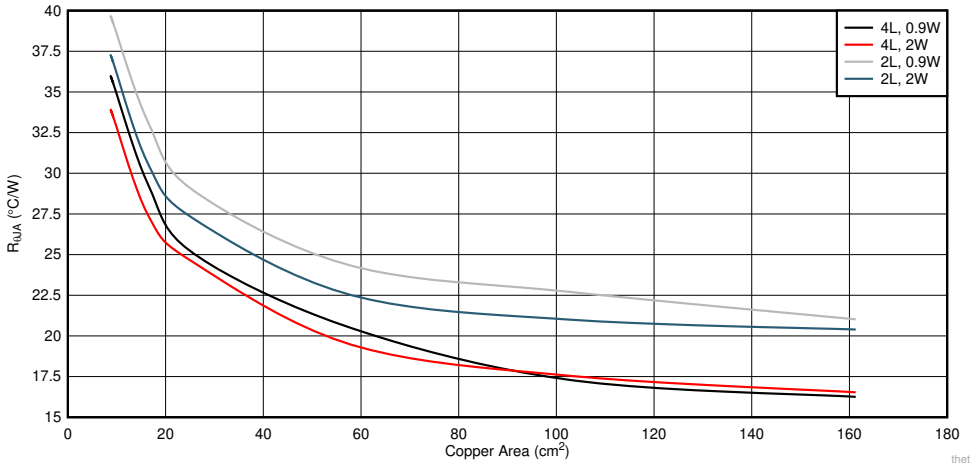


図 8-4. Typical $R_{\theta JA}$ versus Copper Area for the HTSSOP Package

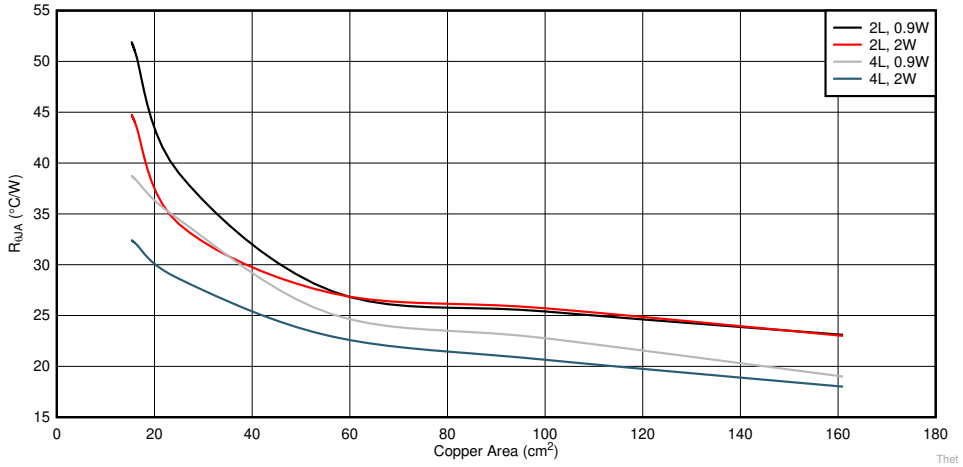


図 8-5. Typical $R_{\theta JA}$ vs Copper Area for the WSON Package

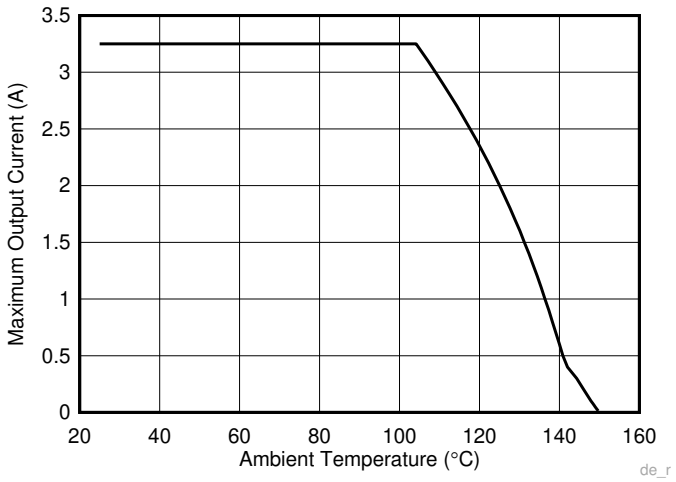


図 8-6. Maximum Output Current versus Ambient Temperature V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 400 kHz, $R_{\theta JA}$ = 22°C/W

The following resources can be used as a guide to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *AN-2020 Thermal Design By Insight, Not Hindsight Application Report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *Using New Thermal Metrics Application Report*

8.2.3 Full Feature Design Example

The schematic in 図 8-7 shows a typical application using all of the features of the LM63635D-Q1. This example provides a 12-V output at 3.25 A from an input of 24 V. Components are calculated using the equations and procedures found in セクション 8.2.2.

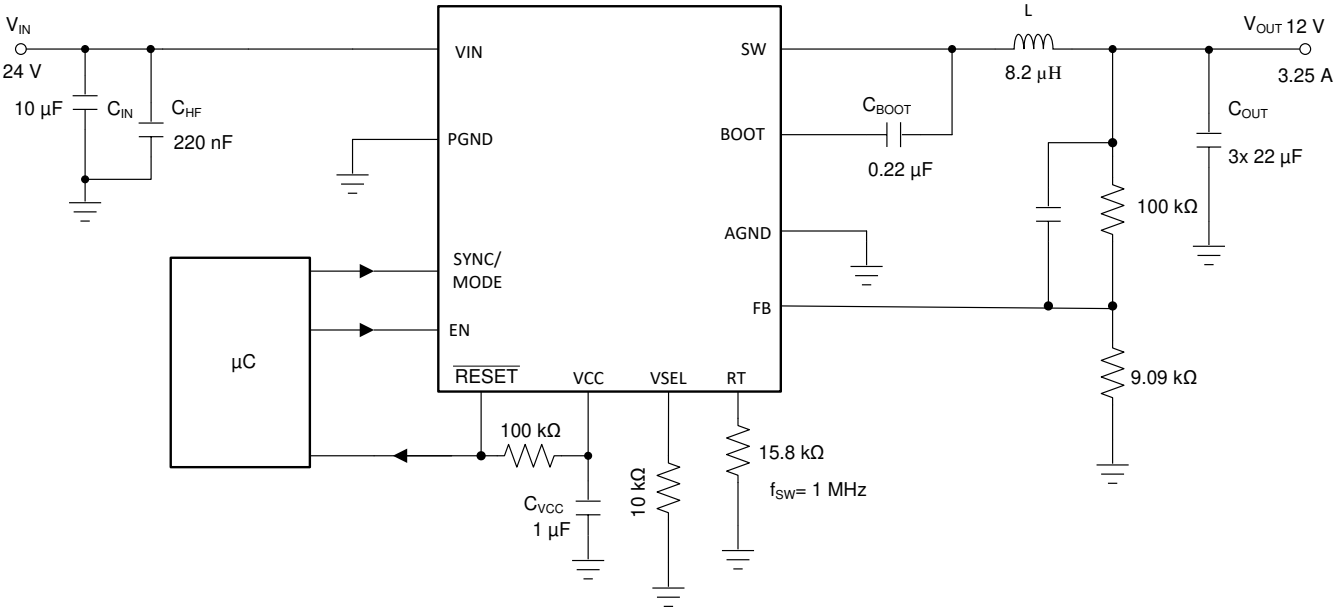
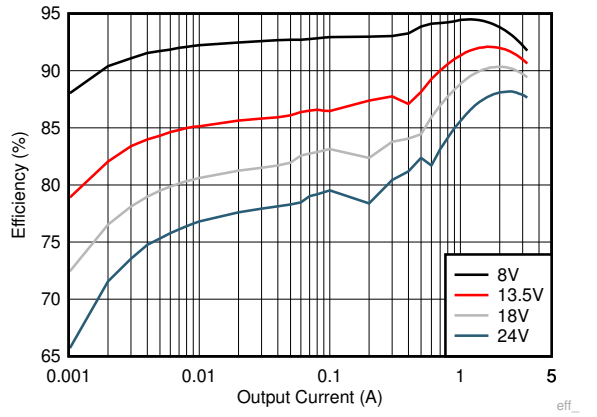


図 8-7. Full-Featured Design Example V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 3.25 A, f_{SW} = 1 MHz

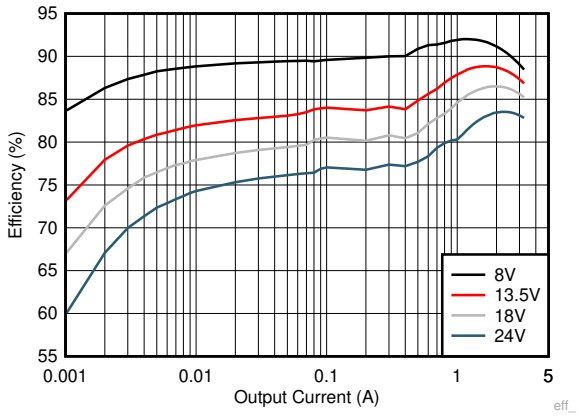
8.2.4 Application Curves

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. 表 8-3 shows the circuit with the appropriate BOM from 図 8-26.



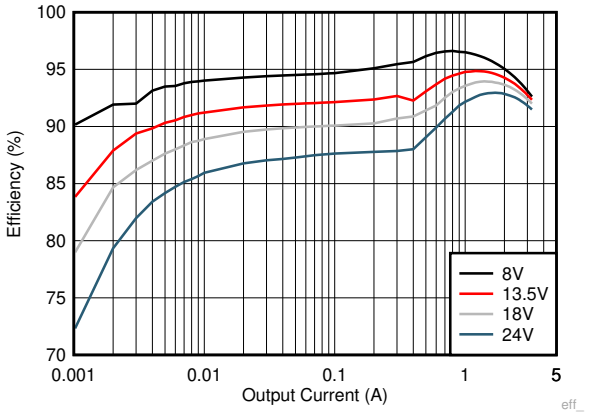
V_{OUT} = 5 V f_{SW} = 2100 kHz (AUTO)

図 8-8. Efficiency



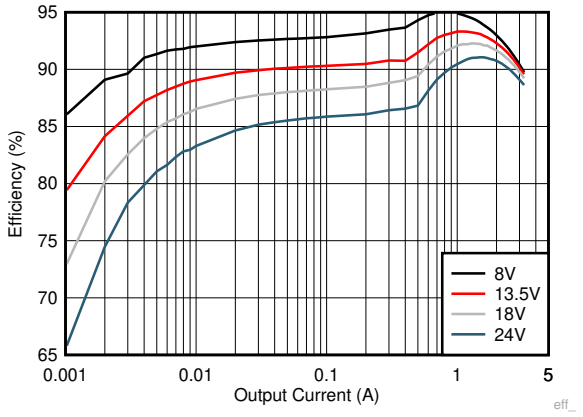
V_{OUT} = 3.3 V f_{SW} = 2100 kHz (AUTO)

図 8-9. Efficiency



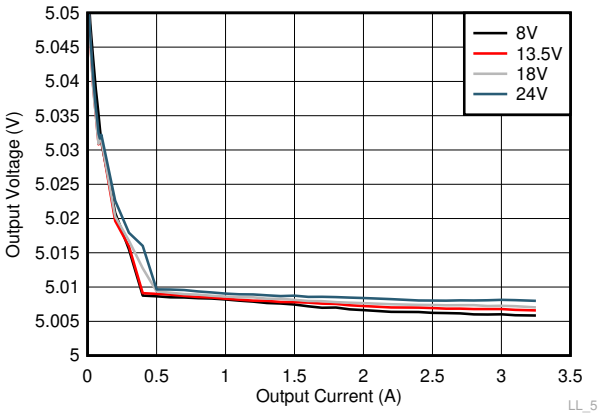
V_{OUT} = 5 V f_{SW} = 400 kHz (AUTO)

図 8-10. Efficiency



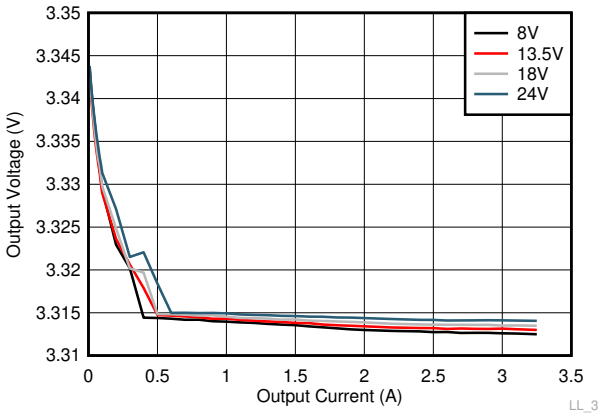
V_{OUT} = 3.3 V f_{SW} = 400 kHz (AUTO)

図 8-11. Efficiency



V_{OUT} = 5 V f_{SW} = 2100 kHz (AUTO)

図 8-12. Line and Load Regulation

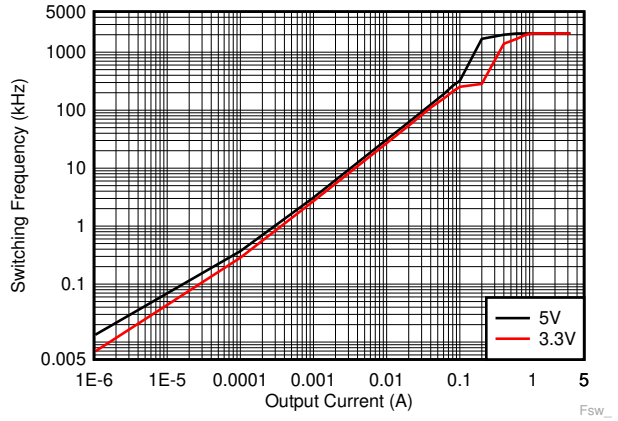


V_{OUT} = 3.3 V f_{SW} = 2100 kHz (AUTO)

図 8-13. Line and Load Regulation

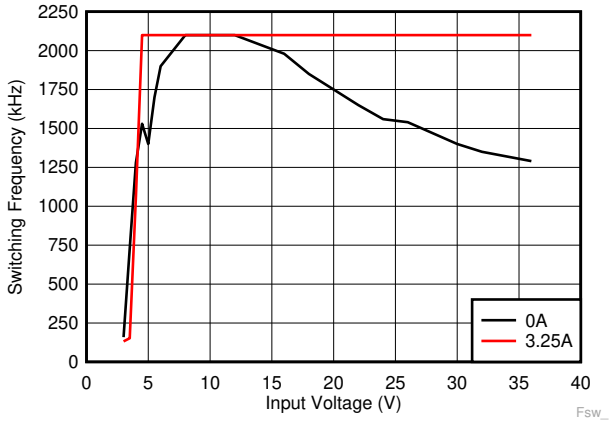
8.2.4 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. 表 8-3 shows the circuit with the appropriate BOM from 図 8-26.



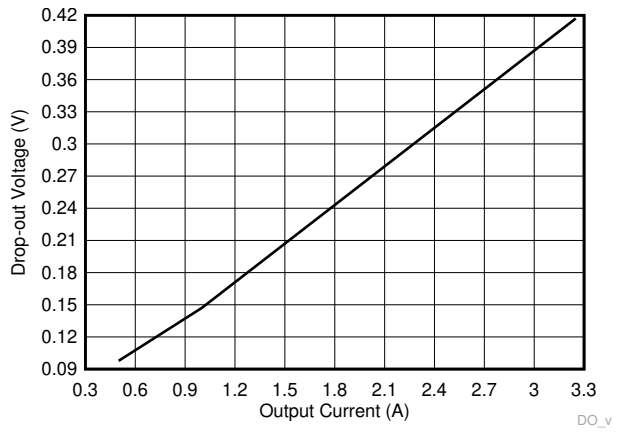
V_{IN} = 13.5 V f_{SW} = 2100 kHz (AUTO)

図 8-14. Switching Frequency versus Output Current



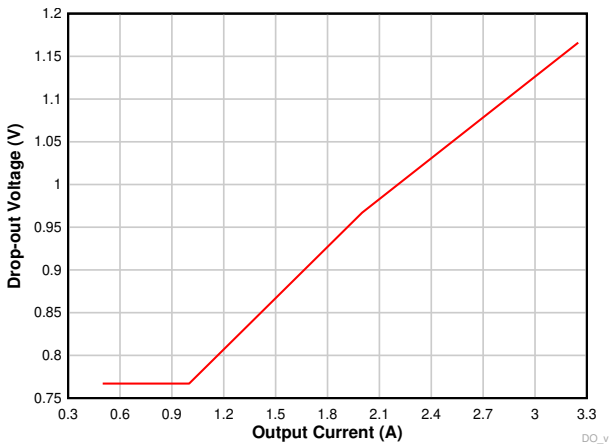
V_{OUT} = 3.3 V f_{SW} = 2100 kHz (FPWM)

図 8-15. Switching Frequency vs Input Voltage



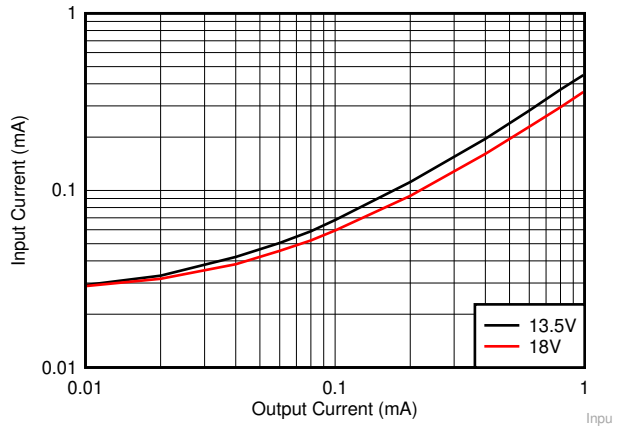
V_{OUT} = 5 V

図 8-16. Dropout Voltage versus Output Current for -1% Drop



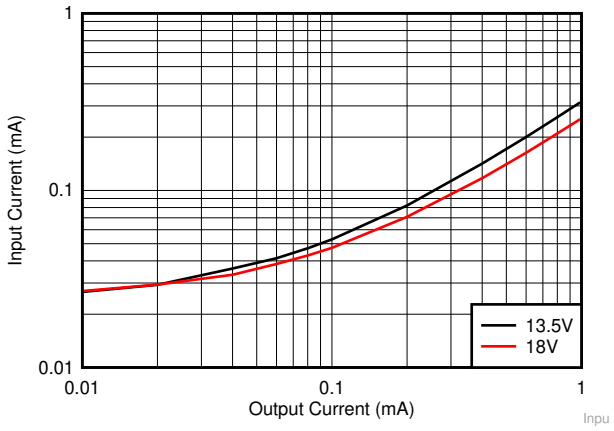
V_{OUT} = 5 V

図 8-17. Dropout Voltage versus Output Current to 1.85 MHz



V_{OUT} = 5 V

図 8-18. Input Supply Current versus Output Current

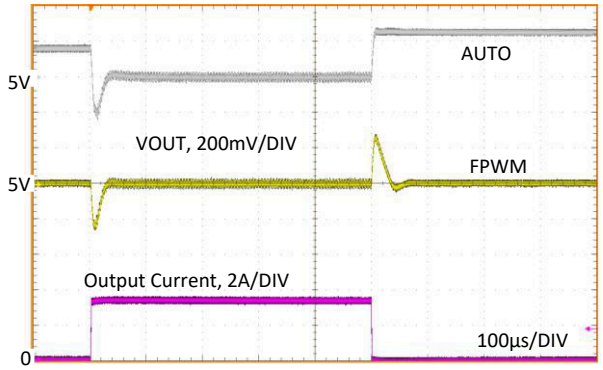


V_{OUT} = 3.3 V

図 8-19. Input Supply Current versus Output Current

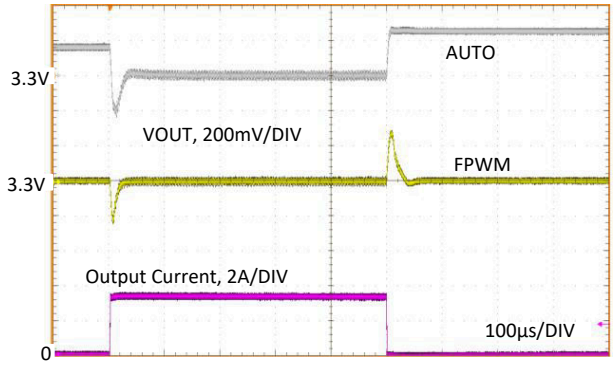
8.2.4 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. 表 8-3 shows the circuit with the appropriate BOM from 図 8-26.



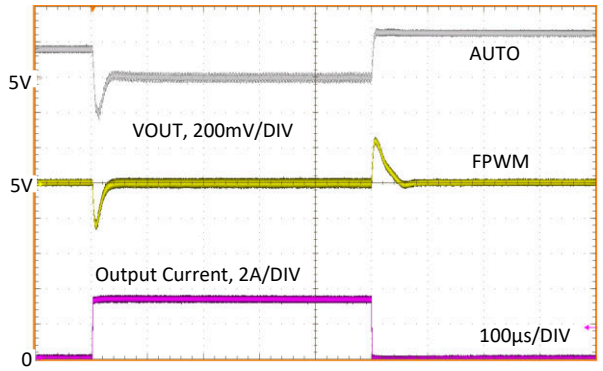
0 A to 3.25 A, 2 µs V_{OUT} = 5 V f_{SW} = 400 kHz

図 8-20. Load Transient



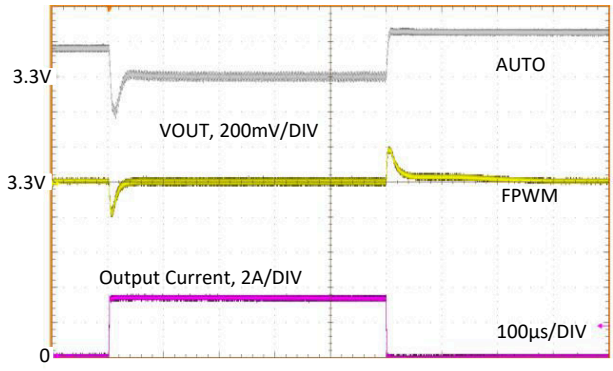
0 A to 3.25 A, 2 µs V_{OUT} = 3.3 V f_{SW} = 400 kHz

図 8-21. Load Transient



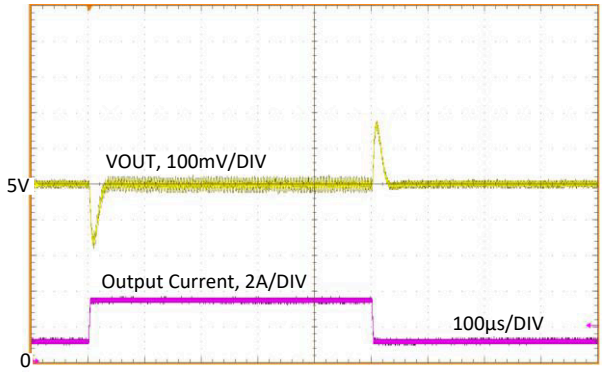
0 A to 3.25 A, 2 µs V_{OUT} = 5 V f_{SW} = 2100 kHz

図 8-22. Load Transient



0 A to 3.25 A, 2 µs V_{OUT} = 3.3 V f_{SW} = 2100 kHz

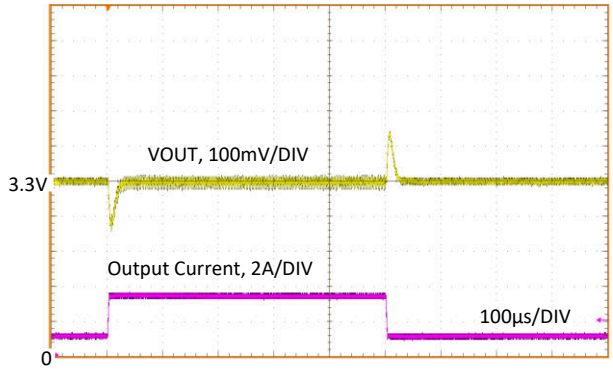
図 8-23. Load Transient



V_{OUT} = 5 V
AUTO

f_{SW} = 400 kHz
1 A to 3.25 A, 2 µs

図 8-24. Load Transient



V_{OUT} = 3.3 V
AUTO

f_{SW} = 400 kHz
1 A to 3.25 A, 2 µs

図 8-25. Load Transient

8.2.4 Application Curves (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 13.5 V, T_A = 25°C. 表 8-3 shows the circuit with the appropriate BOM from 図 8-26.

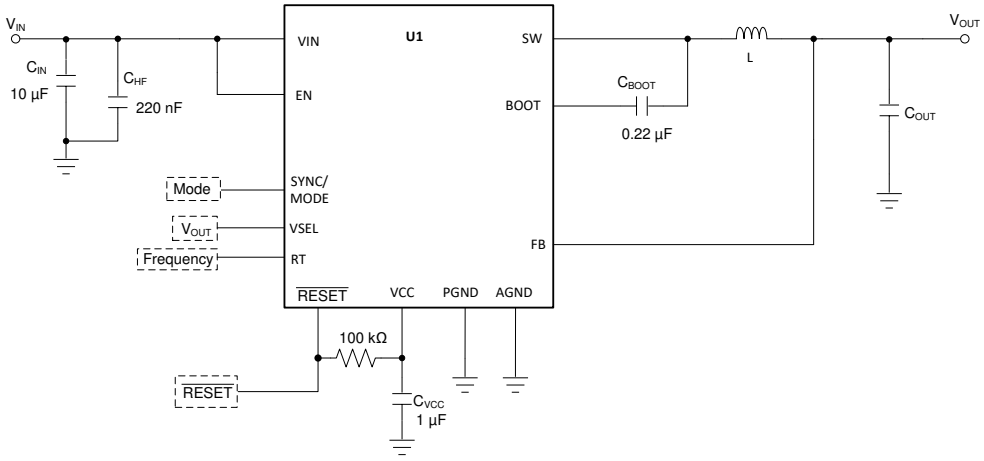


図 8-26. Circuit for Typical Application Curves

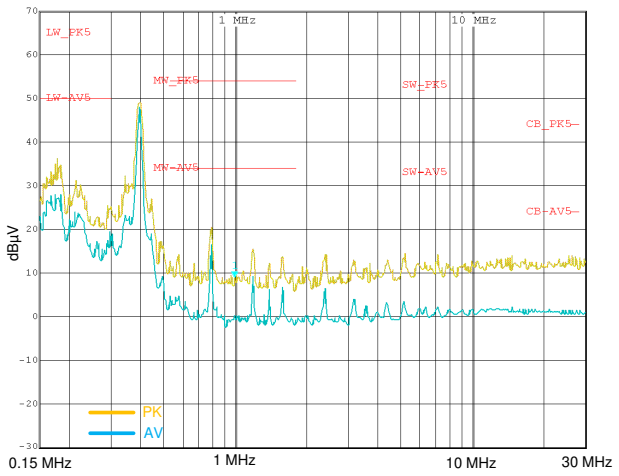
表 8-3. BOM for Typical Application Curves

V_{OUT} (1)	FREQUENCY	OUTPUT CURRENT	C_{OUT}	L	U1
3.3 V	400 kHz	3.25 A	3 × 22 µF	6.8 µH, 22 mΩ	LM63635D
3.3 V	2100 kHz	3.25 A	3 × 22 µF	1.5 µH, 10 mΩ	LM63635D
5 V	400 kHz	3.25 A	3 × 22 µF	6.8 µH, 22 mΩ	LM63635D
5 V	2100 kHz	3.25 A	3 × 22 µF	1.5 µH, 10 mΩ	LM63635D

(1) The values in this table were selected to enhance certain performance criteria and may not represent typical values.

8.2.5 EMI Performance Curves

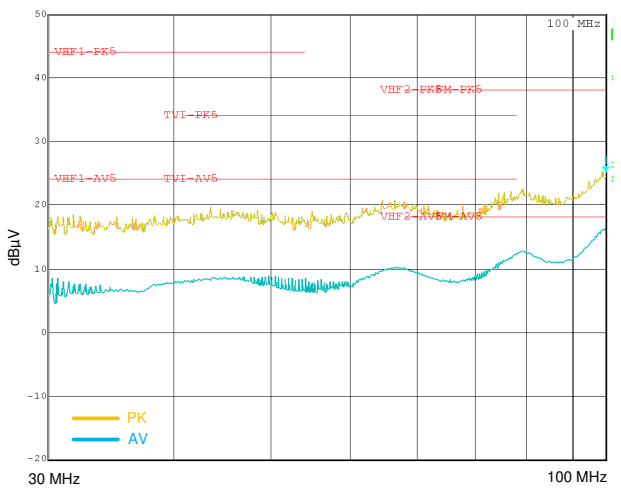
EMI results critically depend on PCB layout and test setup. The results given here are typical and given for information purposes only. 図 8-29 shows the used EMI filter. The limit lines shown refer to CISPR25 class 5.



V_{OUT} = 5 V
Dither

f_{SW} = 400 kHz
I_{OUT} = 3.25 A

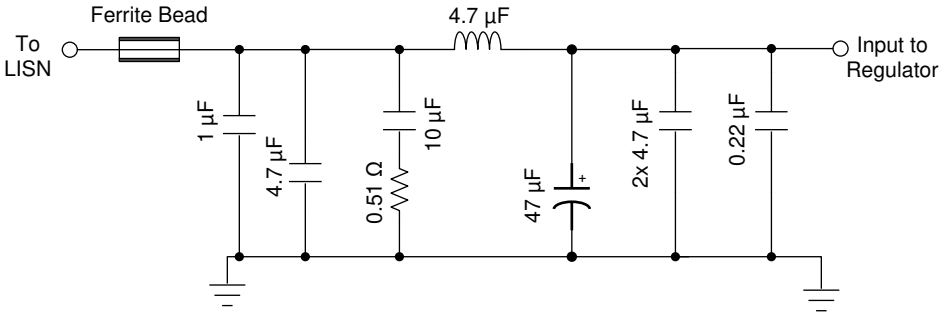
図 8-27. Typical Conducted EMI 0.15 MHz to 30 MHz



V_{OUT} = 5 V
Dither

f_{SW} = 400 kHz
I_{OUT} = 3.25 A

図 8-28. Typical Conducted EMI 30 MHz to 108 MHz



A. Input filter used only for EMI measurements shown in *セクション 8.2.5*.

図 8-29. Typical Input EMI Filter

8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Do not use the value of $R_{\theta JA}$ given in the *Thermal Information* table to design your application. See セクション 8.2.2.9.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.
- Use a 220-nF capacitor connected directly to the VIN and PGND pins of the device. See セクション 8.2.2.5 for details.

8.4 Power Supply Recommendations

The characteristics of the input supply must be compatible with the limits found in セクション 6 of this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 14.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{14}$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

TI recommends that the input supply must not be allowed to fall below the output voltage by more than 0.3 V. Under such conditions, the output capacitors discharges through the body diode of the high-side power MOSFET. The resulting current can cause unpredictable behavior, and in extreme cases, possible device damage. If the application allows for this possibility, then use a Schottky diode from VIN to VOUT to provide a path around the regulator for this current.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharges through the device, as mentioned above.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability as well as some of the effects mentioned above, unless it is designed carefully. The *AN-2162 Simple Success with Conducted EMI from DCDC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching regulator.

8.5 Layout

8.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitors and power ground, as shown in 図 8-30. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 図 8-31 and 図 8-32 show recommended layouts for the critical components of the LM63635-Q1 .

1. **Place the input capacitors as close as possible to the VIN and PGND terminals.** VIN and PGND pins are adjacent, simplifying the input capacitor placement. Thermal reliefs in this area are not recommended.

2. **Place a bypass capacitor for VCC close to the VCC pin.** This capacitor must be placed close to the device and routed with short, wide traces to the VCC and PGND pins. Thermal reliefs in this area are not recommended.
3. **Use wide traces for the C_{BOOT} capacitor.** Place C_{BOOT} close to the device with short and wide traces to the BOOT and SW pins. Thermal reliefs in this area are not recommended.
4. **Place the feedback divider as close as possible to the FB pin of the device.** If an external feedback divider is used with the ADJ option, place R_{FBB}, R_{FBT}, and C_{FF} close to the device. The connections to FB and AGND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. **Use at least one ground plane in one of the middle layers.** This plane acts as a noise shield and also act as a heat dissipation path.
6. **Connect the thermal pad to the ground plane.** The thermal pad (DAP) connection must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection and an electrical ground connection for the regulator. The integrity of this solder connection has a direct bearing on the total effective $R_{\theta JA}$ of the application. Thermal reliefs in this area are not recommended.
7. **Provide wide paths for VIN, VOUT, SW, and PGND.** Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency. Thermal reliefs in this area are not recommended.
8. **Provide enough PCB area for proper heat-sinking.** As stated in *セクション 8.2.2.9*, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two-ounce copper and no less than one ounce. Use an array of heat-sinking vias to connect the thermal pad (DAP) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
9. **Keep switch area small.** Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies Application Report*
- *Simple Switcher PCB Layout Guidelines Application Report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

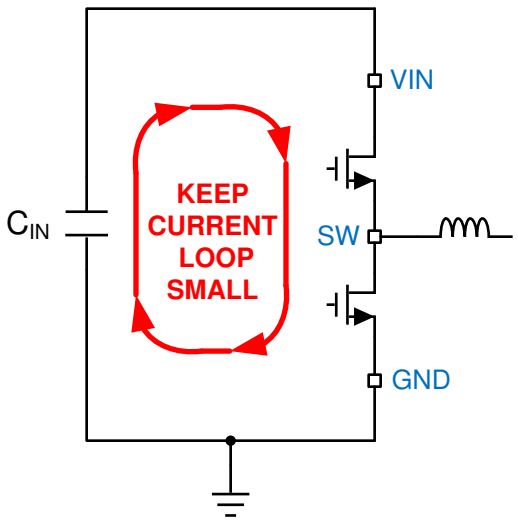


図 8-30. Current Loops With Fast Edges

8.5.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. Connect the AGND and PGND pins to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET switch and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by using the thermal pad (DAP) of the device as the primary thermal path. Use a minimum 4 × 3 array of 10 mil thermal vias to connect the DAP to the system ground plane heat sink. The vias must be evenly distributed under the DAP. Use as much copper as possible for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness and proper layout provides low current conduction impedance, proper shielding, and lower thermal resistance.

8.5.2 Layout Example

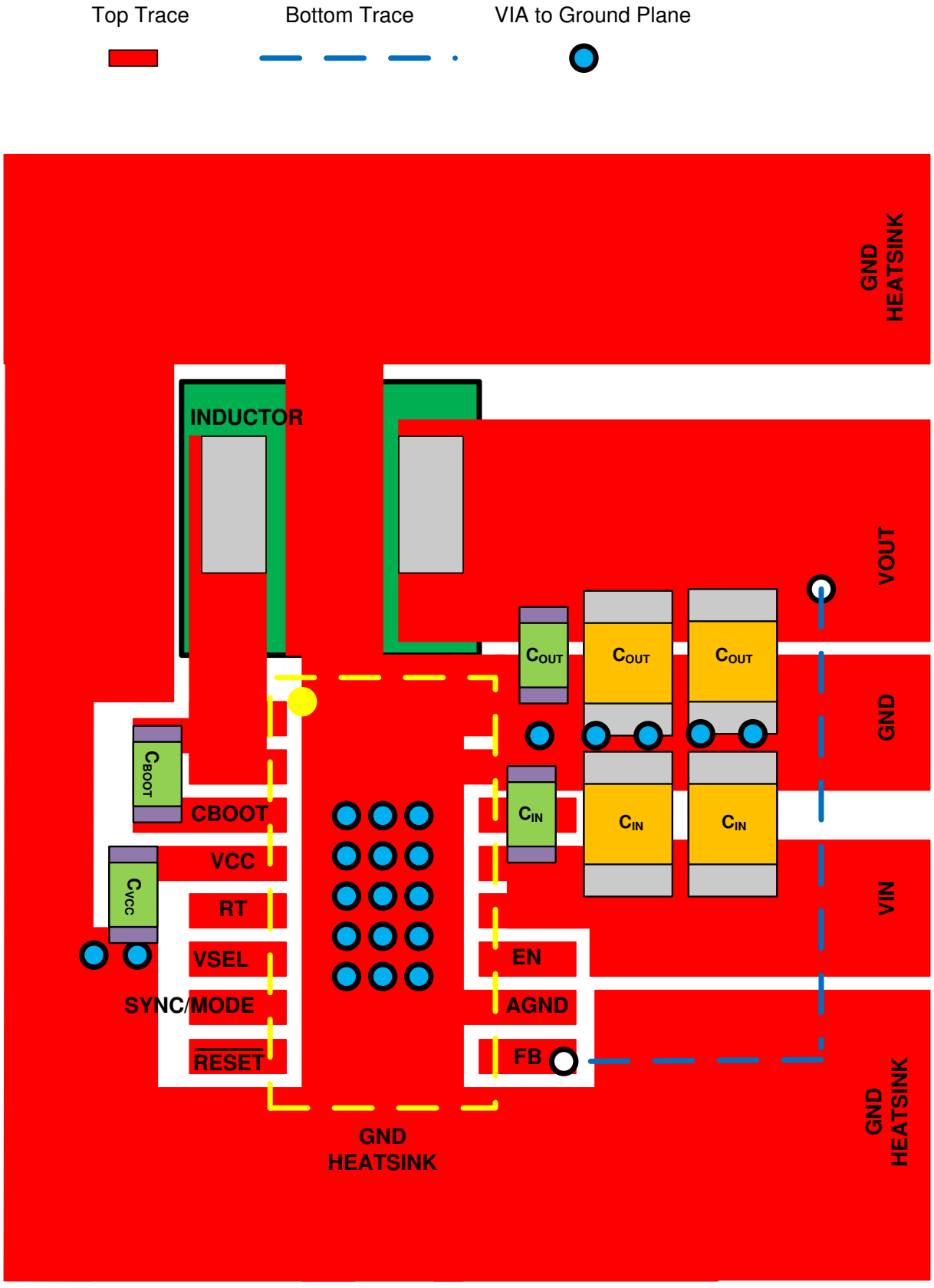


図 8-31. Example Layout for HTSSOP Package

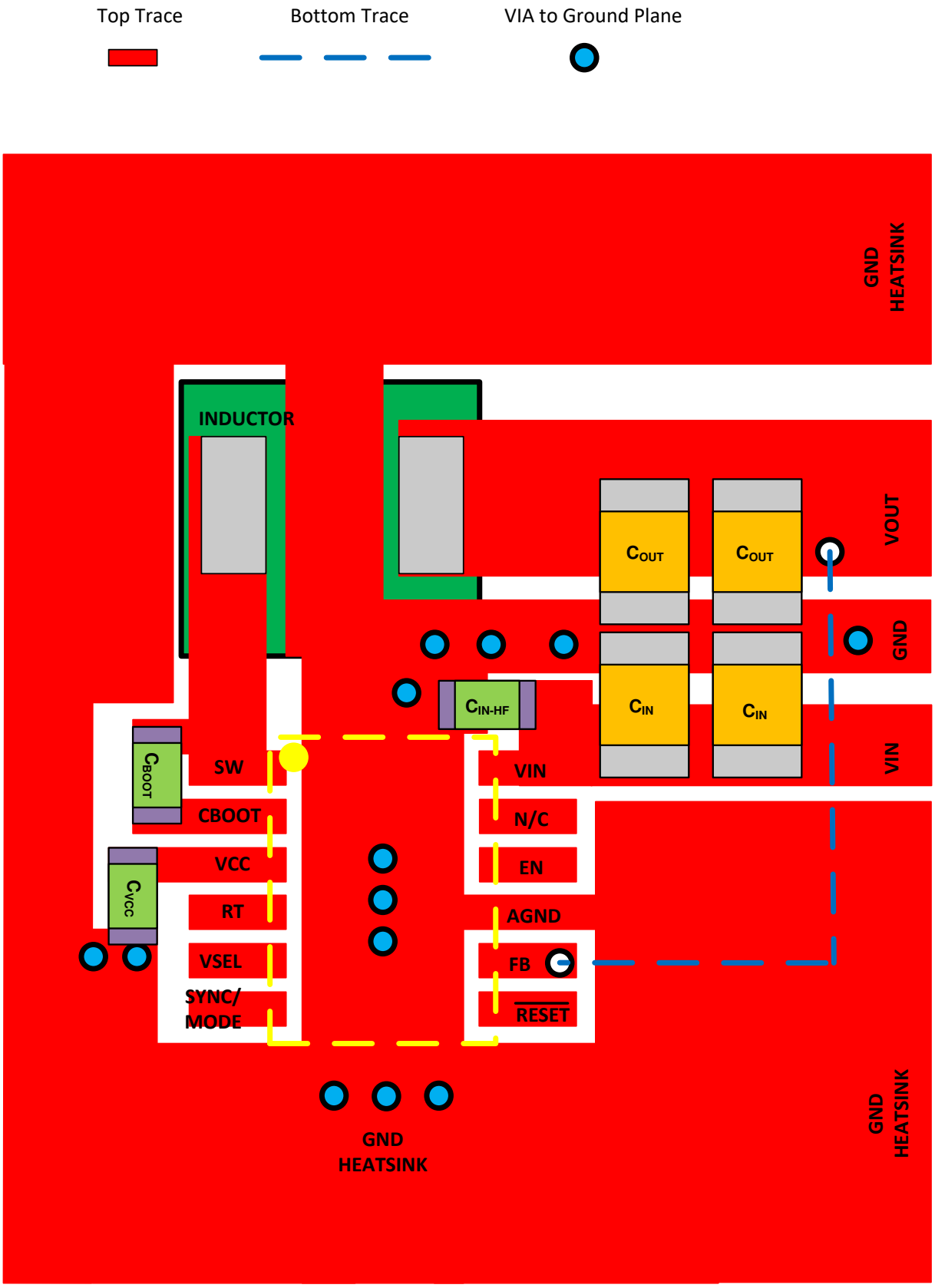


図 8-32. Example Layout for WSON Package

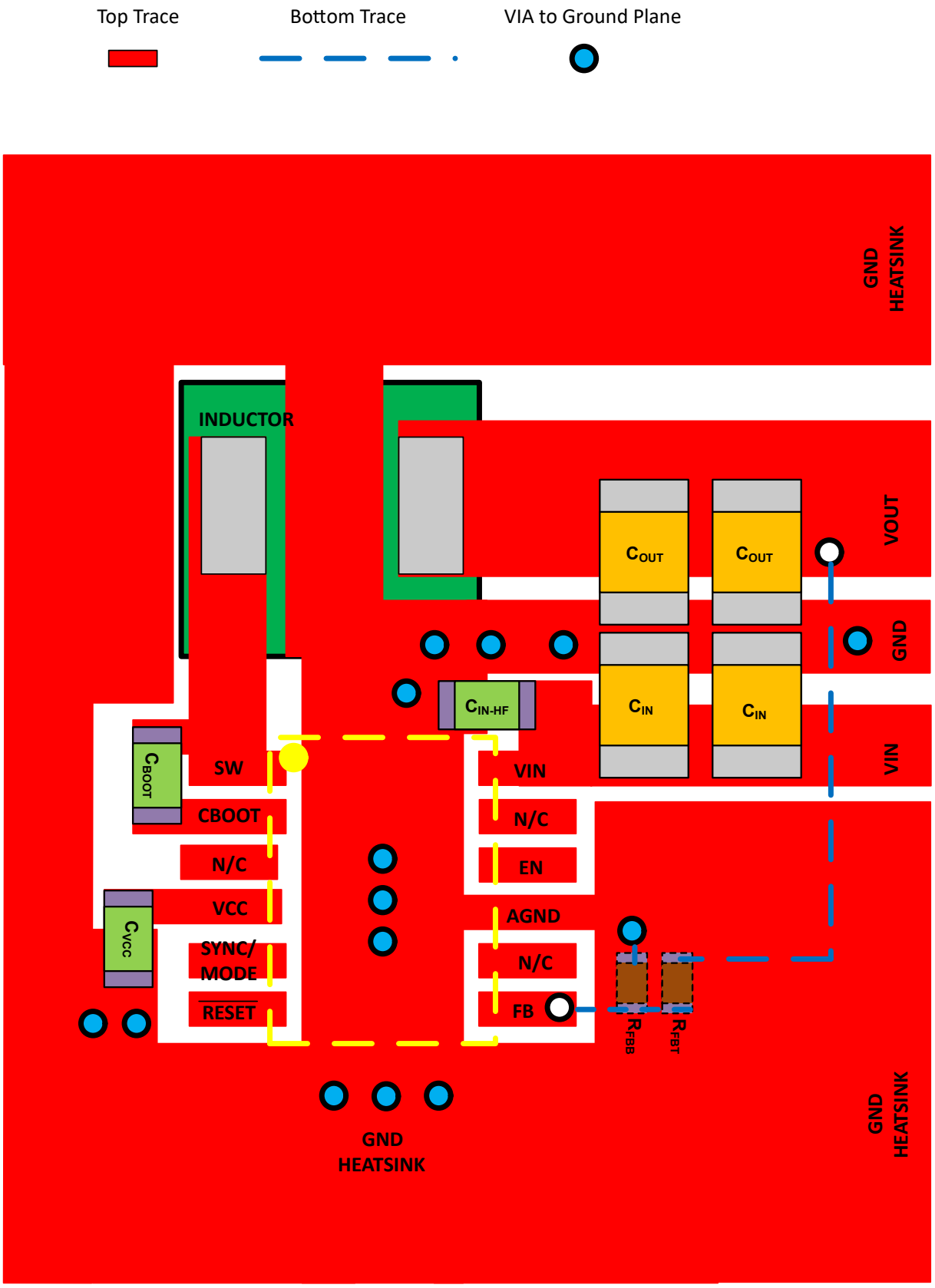


図 8-33. Example Layout for WSON Package 2nd pinout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

図 9-1 shows the device naming nomenclature of the LM63635-Q1. See セクション 4 for the availability of each variant. Contact TI sales representatives or on TI's E2E support forum for detail and availability of other options; minimum order quantities apply.

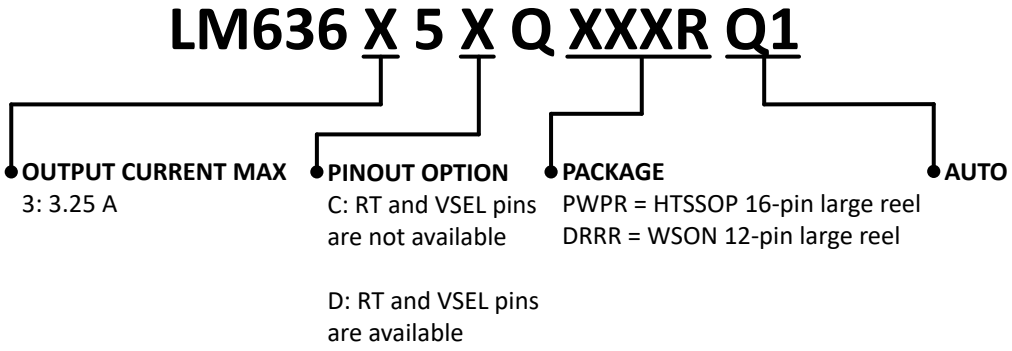


図 9-1. Device Naming Nomenclature

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight Application Report*
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies Application Report*
- Texas Instruments, *Simple Switcher PCB Layout Guidelines Application Report*
- Texas Instruments, *Constructing Your Power Supply-layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (September 2024) to Revision G (November 2024)	Page
• 以前の改訂履歴のページ番号を更新	1

Changes from Revision E (July 2024) to Revision F (September 2024)	Page
• 概略回路図を、より高い解像度の画像に更新	1
• Updated number and unit formatting to comply with TI standard	4
• Added I_{LKG-EN} for the HTSSOP package in the *Electrical Characteristics* table	8
• Changed /RESET to $\overline{\text{RESET}}$ in the *Timing Characteristics* table	10
• Added f_{ADJ} and f_{SPREAD} to the *Switching Characteristics* table	11
• Updated the *Functional Block Diagram* to a higher resolution image	14

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM63635CAQDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	L635CA	Samples
LM63635DQDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	L63635	Samples
LM63635DQPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	63635DQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

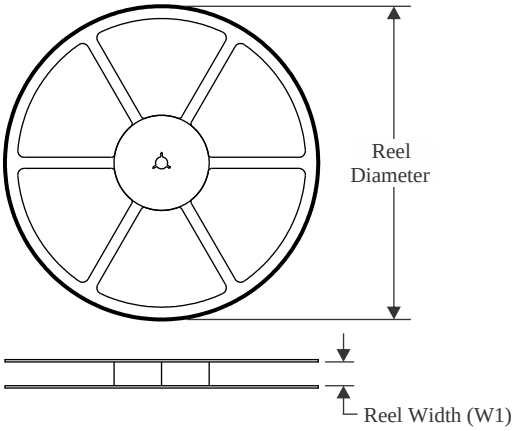
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

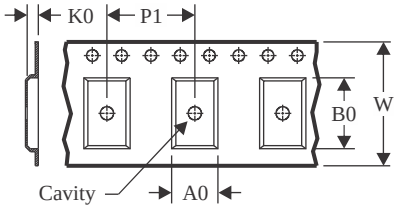
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

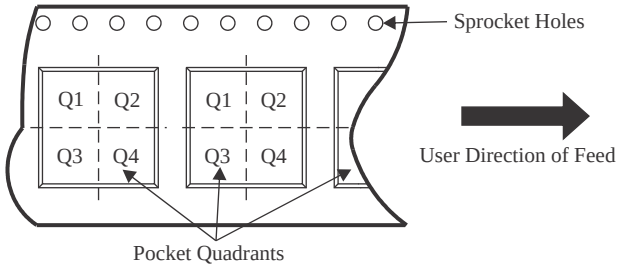


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

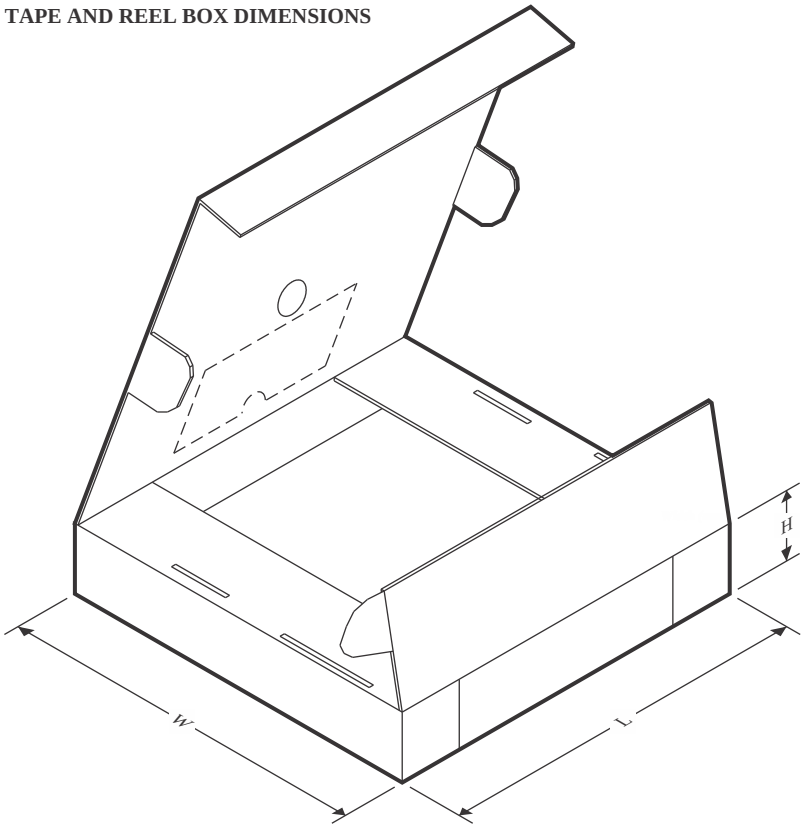
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM63635CAQDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM63635DQDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM63635DQPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

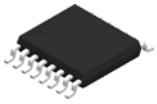


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM63635CAQDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0
LM63635DQDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0
LM63635DQPWPRQ1	HTSSOP	PWP	16	2000	356.0	356.0	35.0

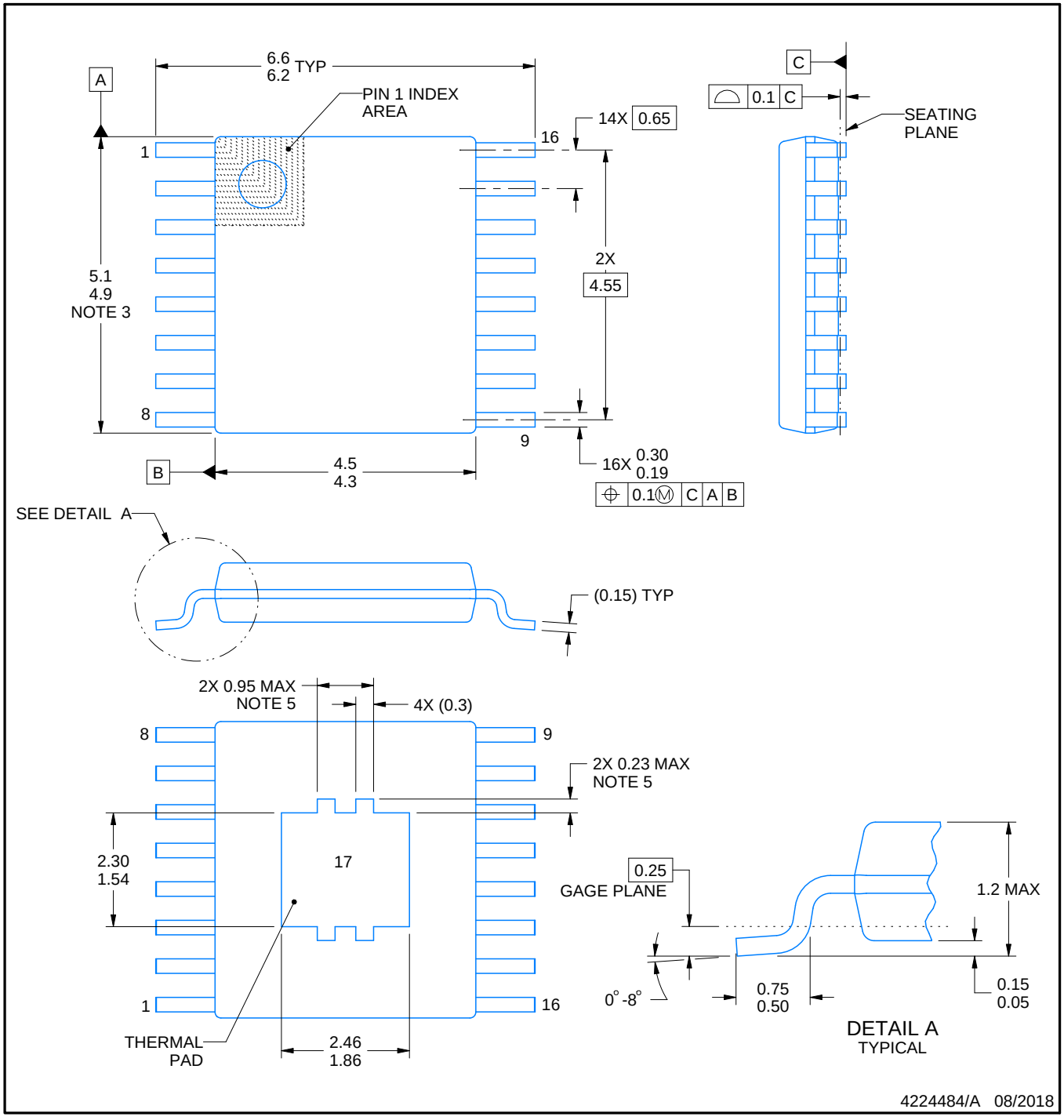
PACKAGE OUTLINE

PWP0016K



PowerPAD™ TSSOP - 1.2 mm max height

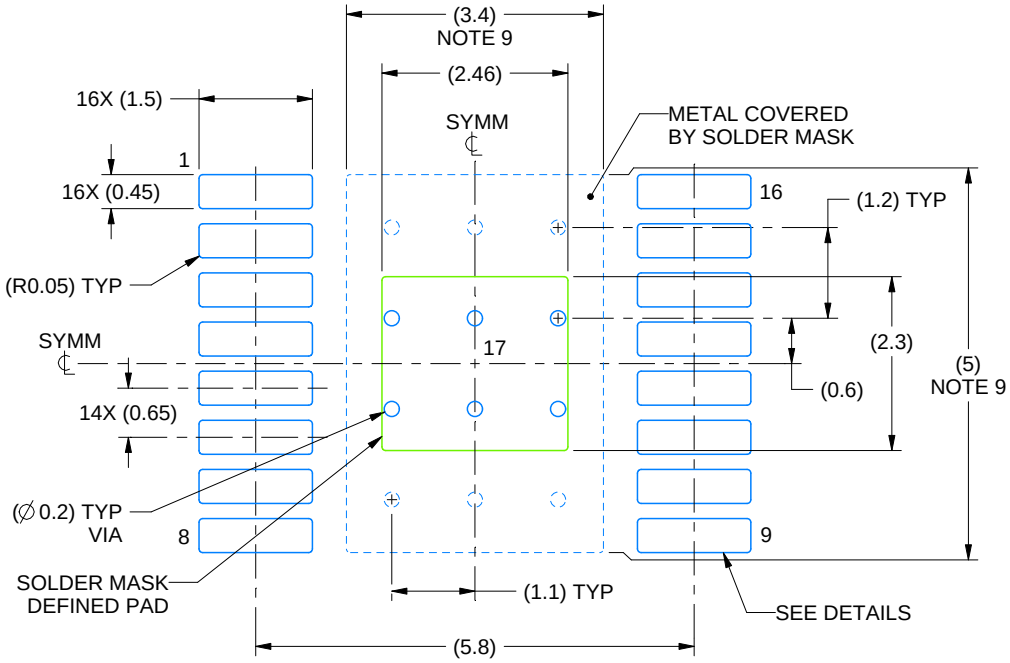
SMALL OUTLINE PACKAGE



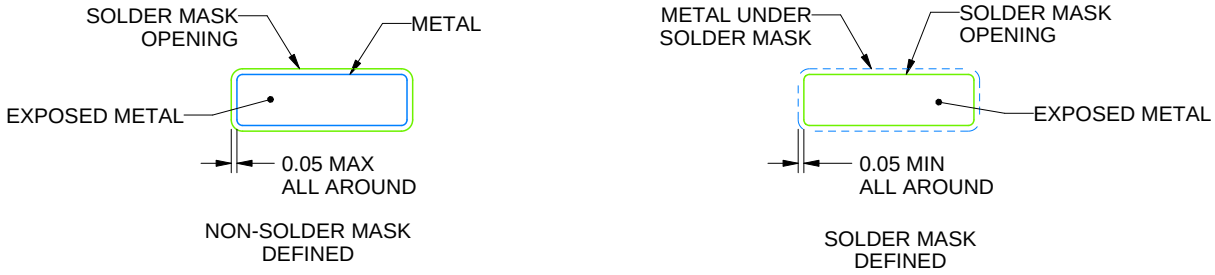
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

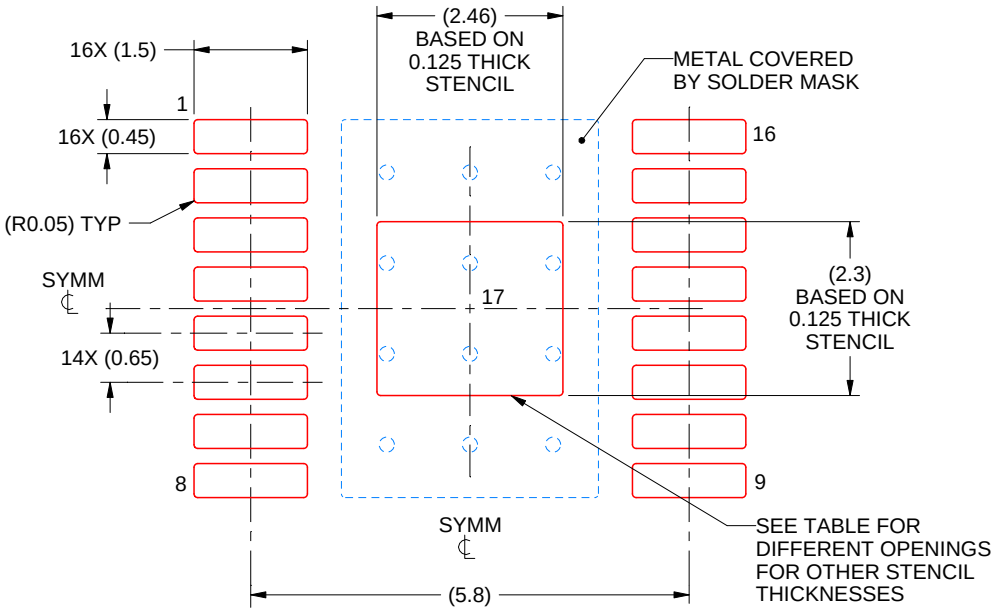


SOLDER MASK DETAILS

4224484/A 08/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.57
0.125	2.46 X 2.30 (SHOWN)
0.15	2.25 X 2.10
0.175	2.08 X 1.94

4224484/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

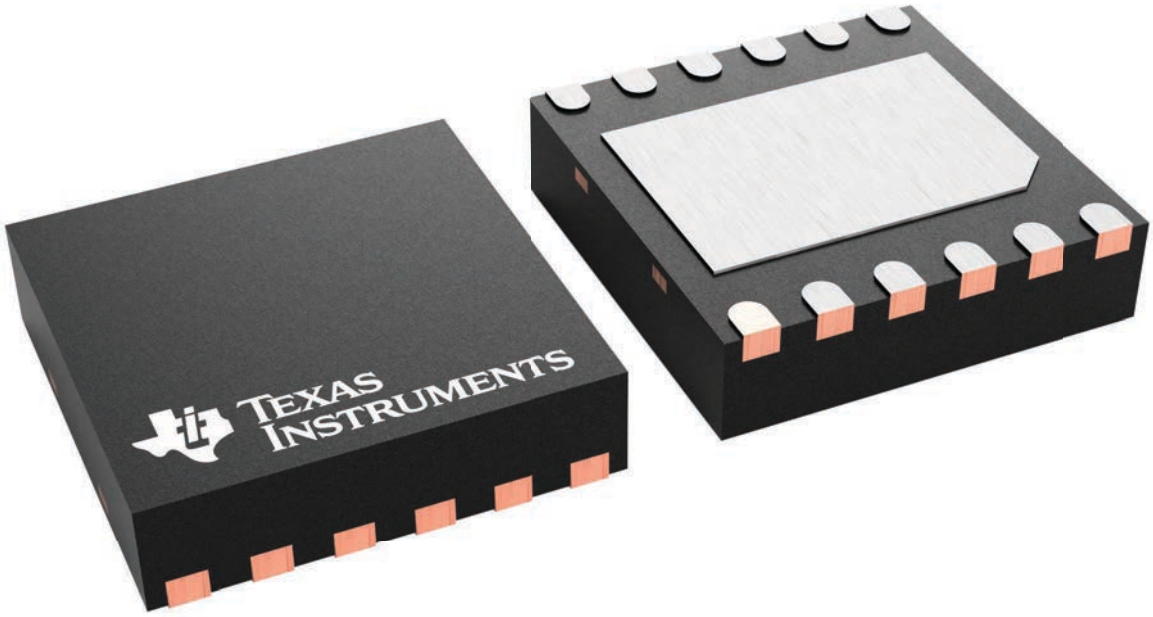
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



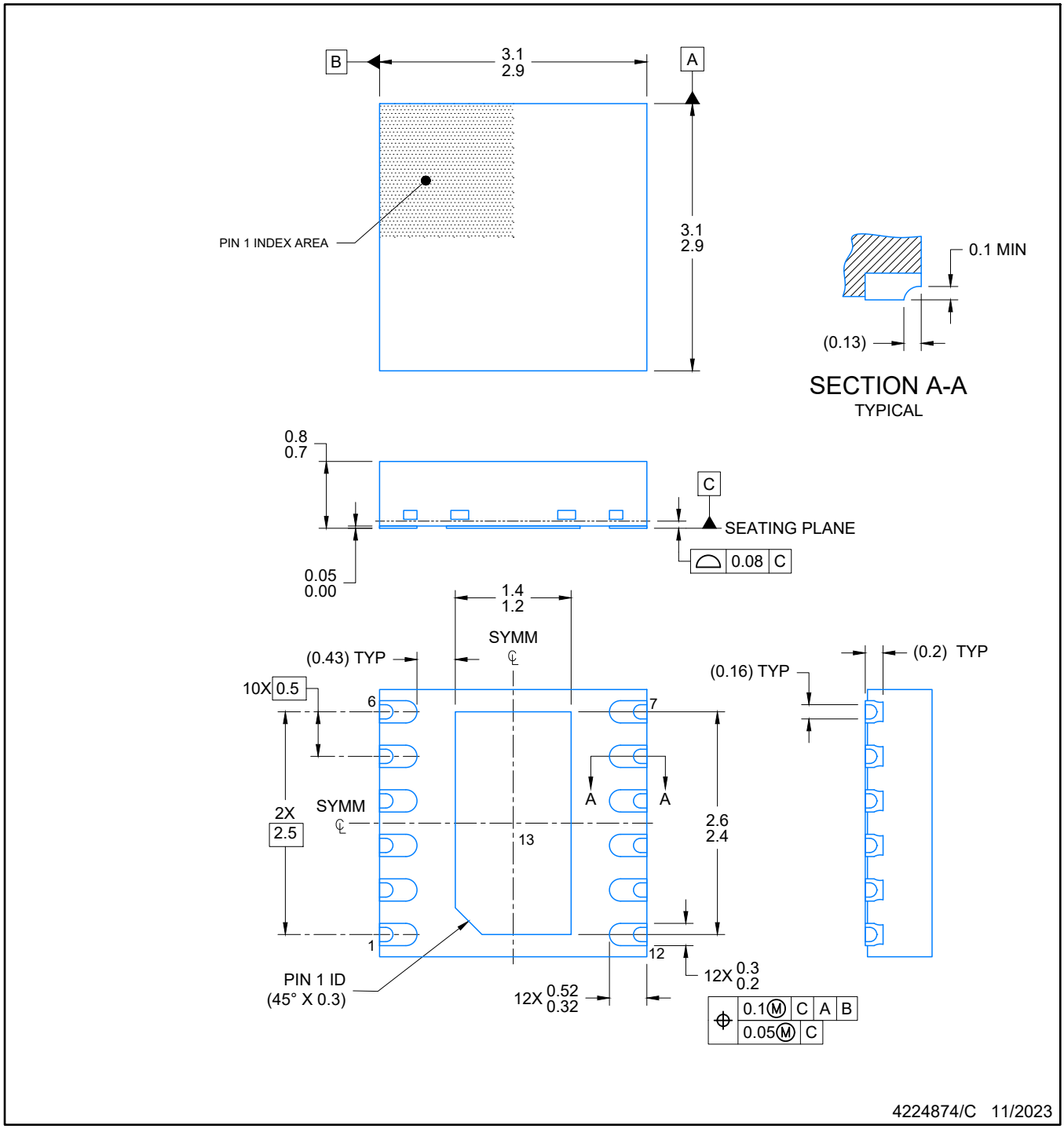
4223490/B

PACKAGE OUTLINE

DRR0012E

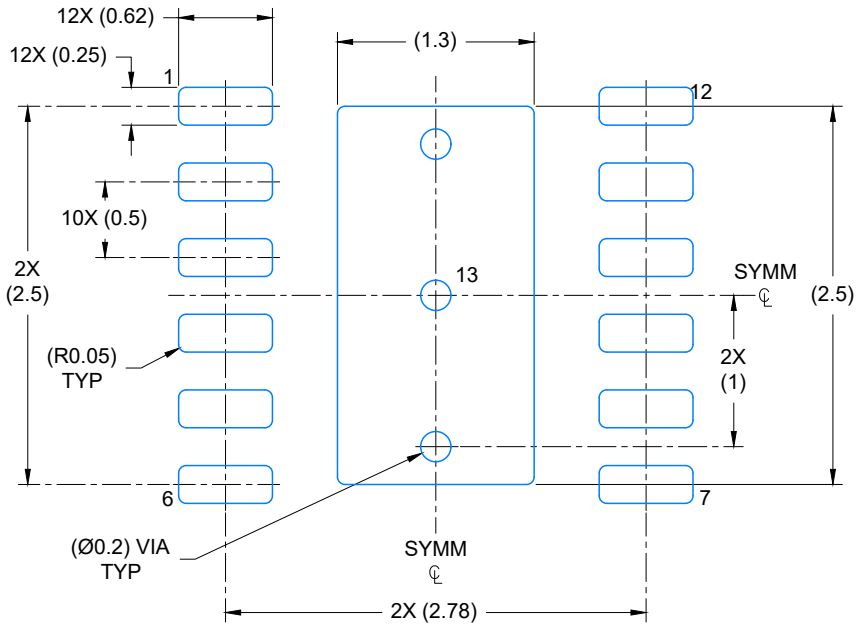
WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

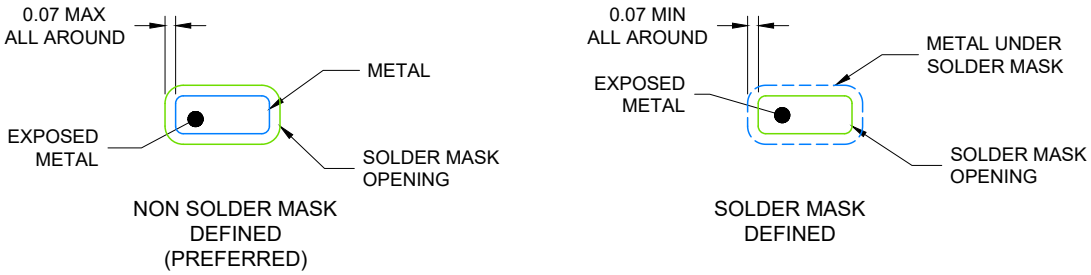


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

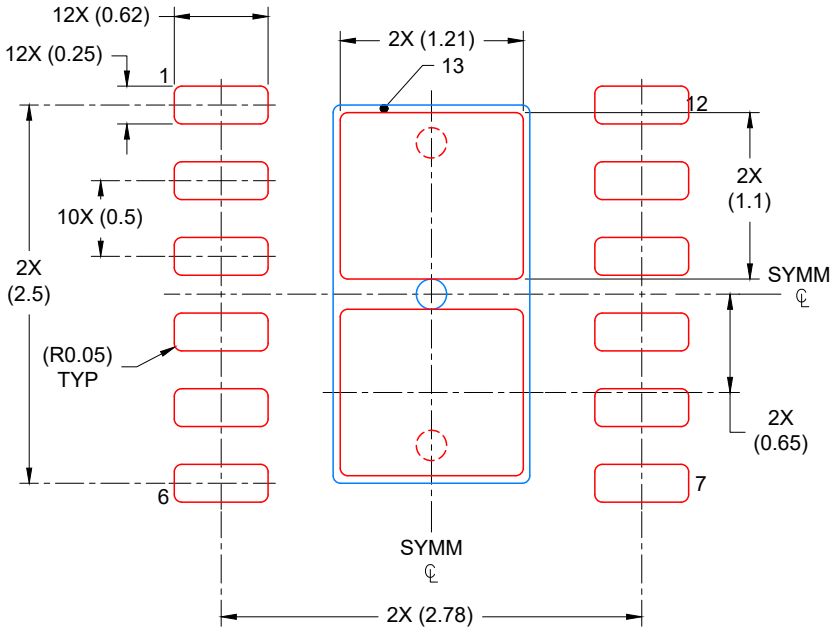


SOLDER MASK DETAILS

4224874/C 11/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

4224874/C 11/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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