# LM6172 デュアル、高速、低消費電力、低歪み、電圧帰還型アンプ

## 1 特長

- 特に記述のない限り標準値
- 使いやすい電圧帰還トポロジ
- 高いスルーレート:3000V/μs
- 広いユニティ ゲイン帯域幅:100 MHz
- 低い消費電流:2.3mA/ チャネル
- 大出力電流:50mA/ チャネル
- 規定動作:±15V および ±5V

## 2 アプリケーション

- スキャナの I/V (電流 / 電圧) コンバータ
- ADSL/HDSL ドライバ
- マルチメディア放送システム
- ビデオ アンプ
- NTSC、PAL、SECAM システム
- ADC/DAC バッファ
- パルス アンプおよびピーク検出器

## 3 概要

LM6172 は、デュアル高速電圧帰還型アンプです。このデバイスはユニティゲイン安定で、優れた DC および AC 性能を備えています。LM6172 は、100MHz のユニティゲイン帯域幅、3000V/μs のスルーレート、チャネルあたりの出力電流 50mA で、デュアル アンプで高性能を実現し、さらに、チャネルあたりの消費電流はわずか 2.3mA です。

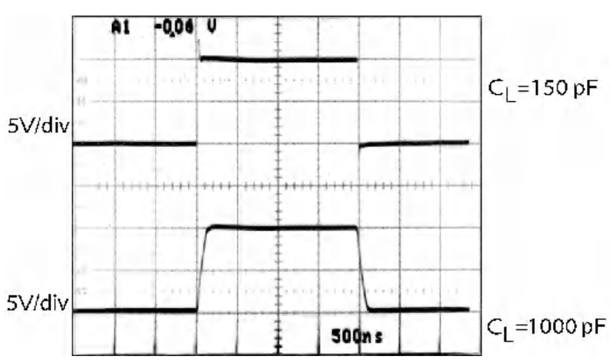
LM6172 は、ADSL、スキャナ、超音波機器など、大きい電圧振幅を必要とするシステム向けに ±15V の電源で動作します。このデバイスは、携帯型ビデオ システムなどの低電圧アプリケーション向けの ±5V 電源についても仕様が規定されています。

LM6172 は、テキサス・インスツルメンツの先進的な相補型バイポーラ プロセスで製造されます。これらと同じ特長を持つシングル アンプについては、LM6171 データシートを参照してください。

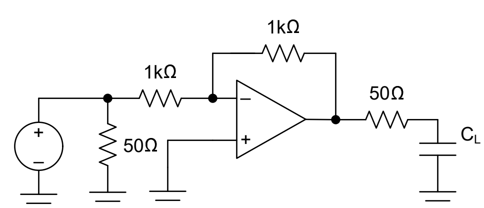
**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ(2) |
|---|---|---|
| LM6172 | D (SOIC、8) | 4.9mm × 6mm |
| | P (PDIP、8) | 9.81mm × 9.43mm |

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。




LM6172 による容量性負荷の駆動




LM6172 による容量性負荷の駆動

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# 4 Pin Configuration and Functions

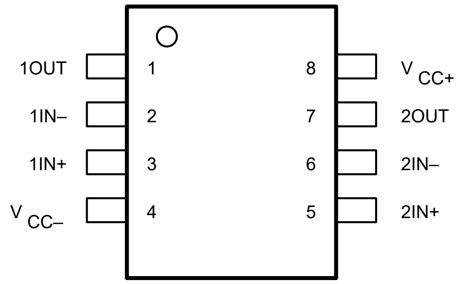



**図 4-1. D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)**

**表 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1IN– | 2 | Input | Channel 1 inverting input |
| 1IN+ | 3 | Input | Channel 1 noninverting input |
| 1OUT | 1 | Output | Channel 1 output |
| 2IN– | 6 | Input | Channel 2 inverting input |
| 2IN+ | 5 | Input | Channel 2 noninverting input |
| 2OUT | 7 | Output | Channel 2 output |
| $V_{CC-}$ | 4 | — | Negative power supply |
| $V_{CC+}$ | 8 | — | Positive power supply |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage ($V_{CC+} – V_{CC–}$) | | 36 | V |
| $V_I$ | Differential input voltage | | ±10 | V |
| $V_{CM}$ | Common-mode voltage | $V_{CC–}$ – 0.3 | $V_{CC+}$ + 0.3 | V |
| $I_{IN}$ | Input current | | ±10 | mA |
| $I_{SC}$ | Output current short to ground[(3)] | | Continuous | A |
| $T_J$ | Junction temperature[(4)] | | 150 | ℃ |
| $T_{stg}$ | Storage temperature | –65 | 150 | ℃ |
| $T_{SOLDER}$ | Infrared or convection reflow (20 seconds) | | 235 | ℃ |
| | Wave soldering lead temp (10 seconds) | | 260 | |

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(2) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | ±3000 | V |
| | | Machine model[(2)] | ±300 | V |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) Machine model, 200Ω in series with 100pF.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Supply voltage | 5.5 | | 36 | |
| $T_A$ | Ambient temperature | −40 | | 85 | °C |

## 5.4 Thermal Information

| THERMAL METRIC[(1)] | | LM6172 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | P (PDIP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 172 | 108 | ℃/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 62.4 | 52.4 | ℃/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 55.7 | 51.9 | ℃/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 16.5 | 6.8 | ℃/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 55.1 | 51.1 | ℃/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | ℃/W |

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics ±15V

at $T_J$ = 25°C, $V_{CC+}$ = 15V, $V_{CC-}$ = −15V, $V_{CM}$ = 0V, and $R_L$ = 1kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN[2] | TYP[1] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | | | | 0.4 | 3 | mV |
| | | $T_A$ = –40°C to +85°C | | | | 4 | |
| $TCV_{OS}$ | Input offset voltage average drift | | | | 6 | | µV/°C |
| $I_B$ | Input bias current | | | | 1.2 | 3 | µA |
| | | $T_A$ = –40°C to +85°C | | | | 4 | |
| $I_{OS}$ | Input offset current | | | | 0.02 | 2 | µA |
| | | $T_A$ = –40°C to +85°C | | | | 3 | |
| $R_{IN}$ | Input resistance | Common-mode | | | 40 | | MΩ |
| | | Differential-mode | | | 4.9 | | |
| $R_O$ | Open-loop output resistance | | | | 14 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{CM}$ = ±10V | | 70 | 110 | | dB |
| | | | $T_A$ = –40°C to +85°C | 65 | | | |
| PSRR | Power supply rejection ratio | $V_S$ = ±15V to ±5V | | 75 | 95 | | dB |
| | | | $T_A$ = –40°C to +85°C | 70 | | | |
| $V_{CM}$ | Input common-mode voltage | CMRR > 60dB | | | ±13.5 | | V |
| $A_V$ | Large-signal voltage gain[3] | $R_L$ = 1kΩ, $V_{OUT}$ = ±5V | | 80 | 86 | | dB |
| | | | $T_A$ = –40°C to +85°C | 75 | | | |
| | | $R_L$ = 100Ω, $V_{OUT}$ = ±5V | | 65 | 78 | | |
| | | | $T_A$ = –40°C to +85°C | 60 | | | |
| $V_O$ | Output swing | $R_L$ = 1kΩ, sourcing | | 12.5 | 13.2 | | V |
| | | | $T_A$ = –40°C to +85°C | 12 | | | |
| | | $R_L$ = 1kΩ, sinking | | | −13.1 | −12.5 | |
| | | | $T_A$ = –40°C to +85°C | | | −12 | |
| | | $R_L$ = 100Ω, sourcing | | 6 | 9 | | |
| | | | $T_A$ = –40°C to +85°C | 5 | | | |
| | | $R_L$ = 100Ω, sinking | | | −8.5 | −6 | |
| | | | $T_A$ = –40°C to +85°C | | | −5 | |
| | Continuous output current (open loop)[4] | Sourcing, $R_L$ = 100Ω | | 60 | 90 | | mA |
| | | | $T_A$ = –40°C to +85°C | 50 | | | |
| | | Sinking, $R_L$ = 100Ω | | | −85 | −60 | |
| | | | $T_A$ = –40°C to +85°C | | | −50 | |
| $I_{SC}$ | Output short-circuit current | D package | Sourcing | | 173 | | mA |
| | | | Sinking | | −183 | | |
| | | P package | Sourcing | | 107 | | |
| | | | Sinking | | −105 | | |
| $I_S$ | Supply current | | | | 4.6 | 8 | mA |
| | | $T_A$ = –40°C to +85°C | | | | 9 | |
| SR | Slew rate[5] | $A_V$ = +2, $V_{IN}$ = $13V_{PP}$ | | | 3000 | | V/µs |
| | | $A_V$ = +2, $V_{IN}$ = $10V_{PP}$ | | | 2500 | | |
| | Unity-gain bandwidth | D package | | | 80 | | MHz |
| | | P package | | | 100 | | |
| | −3dB frequency | $A_V$ = +1 | | | 160 | | MHz |
| | | $A_V$ = +2 | | | 62 | | MHz |

## 5.5 Electrical Characteristics ±15V (続き)

at $T_J$ = 25°C, $V_{CC+}$ = 15V, $V_{CC-}$ = −15V, $V_{CM}$ = 0V, and $R_L$ = 1kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN[2] | TYP[1] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|---|
| $φ_m$ | Phase margin | | | | 40 | | Deg |
| | Bandwidth matching between channels | | | | 2 | | MHz |
| $t_s$ | Settling time (0.1%) | $A_V$ = −1, $V_{OUT}$ = ±5V, $R_L$ = 500Ω | | | 65 | | ns |
| $A_D$ | Differential gain[6] | | | | 0.28 | | % |
| $φ_D$ | Differential phase[6] | | | | 0.6 | | ° |
| $e_n$ | Input-referred voltage noise | f = 10kHz | | | 12 | | nV/√Hz |
| $i_n$ | Input-referred current noise | f = 10kHz | | | 1 | | pA/√Hz |
| HD2 | Second harmonic distortion | D package | $f_{IN}$ = 10kHz | | −88 | | dBc |
| | | | $f_{IN}$ = 5MHz | | −50 | | |
| | | P package | $f_{IN}$ = 10kHz | | −110 | | |
| | | | $f_{IN}$ = 5MHz | | −50 | | |
| HD3 | Third harmonic distortion | D package | $f_{IN}$ = 10kHz | | −93 | | dBc |
| | | | $f_{IN}$ = 5MHz | | −41 | | |
| | | P package | $f_{IN}$ = 10kHz | | −105 | | |
| | | | $f_{IN}$ = 5MHz | | −50 | | |

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Large-signal voltage gain is the total output swing divided by the input signal required to produce that swing. For $V_S$ = ±15V, $V_{OUT}$ = ±5V. For $V_S$ = 5V, $V_{OUT}$ = ±1V.
(4) The open-loop output current is the output swing with the 100Ω load resistor divided by that resistor.
(5) Slew rate is the average of the rising and falling slew rates.
(6) Differential gain and phase are measured with $A_V$ = +2, $V_{IN}$ = 1$V_{PP}$ at 3.58MHz and both input and output 75Ω terminated.

## 5.6 Electrical Characteristics ±5V

at $T_J$ = 25°C, $V_{CC+}$ = 5V, $V_{CC-}$ = −5V, $V_{CM}$ = 0V, and $R_L$ = 1kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN[2] | TYP[1] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage | | | | 0.1 | 3 | mV |
| | | $T_A$ = –40°C to +85°C | | | | 4 | |
| $TCV_{OS}$ | Input offset voltage average drift | | | | 4 | | μV/°C |
| $I_B$ | Input bias current | | | | 1.4 | 2.5 | μA |
| | | $T_A$ = –40°C to +85°C | | | | 3.5 | |
| $I_{OS}$ | Input offset current | | | | 0.02 | 1.5 | μA |
| | | $T_A$ = –40°C to +85°C | | | | 2.2 | |
| $R_{IN}$ | Input resistance | Common-mode | | | 40 | | MΩ |
| | | Differential-mode | | | 4.9 | | |
| $R_O$ | Open loop output resistance | | | | 14 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{CM}$ = ±2.5V | | 70 | 105 | | dB |
| | | | $T_A$ = –40°C to +85°C | 65 | | | |
| PSRR | Power supply rejection ratio | $V_S$ = ±15V to ±5V | | 75 | 95 | | dB |
| | | | $T_A$ = –40°C to +85°C | 70 | | | |
| $V_{CM}$ | Input common-mode voltage | CMRR > 60dB | | | ±3.7 | | V |
| $A_V$ | Large-signal voltage gain[3] | $R_L$ = 1 kΩ, $V_{OUT}$ = ±1V | | 70 | 82 | | dB |
| | | | $T_A$ = –40°C to +85°C | 65 | | | |
| | | $R_L$ = 100Ω, $V_{OUT}$ = ±1V | | 65 | 78 | | |
| | | | $T_A$ = –40°C to +85°C | 60 | | | |
| $V_O$ | Output swing | $R_L$ = 1kΩ, sourcing | | 3.1 | 3.4 | | V |
| | | | $T_A$ = –40°C to +85°C | 3 | | | |
| | | $R_L$ = 1kΩ, sinking | | | −3.3 | −3.1 | |
| | | | $T_A$ = –40°C to +85°C | | | −3 | |
| | | $R_L$ = 100Ω, sourcing | | 2.5 | 2.9 | | |
| | | | $T_A$ = –40°C to +85°C | 2.4 | | | |
| | | $R_L$ = 100Ω, sinking | | | −2.7 | −2.4 | |
| | | | $T_A$ = –40°C to +85°C | | | −2.3 | |
| | Continuous output current (open loop)[4] | Sourcing, $R_L$ = 100Ω | | 25 | 29 | | mA |
| | | | $T_A$ = –40°C to +85°C | 24 | | | |
| | | Sinking, $R_L$ = 100Ω | | | −27 | −24 | |
| | | | $T_A$ = –40°C to +85°C | | | −23 | |
| $I_{SC}$ | Output short-circuit current | D package | Sourcing | | 155 | | mA |
| | | | Sinking | | −158 | | |
| | | P package | Sourcing | | 93 | | |
| | | | Sinking | | −72 | | |
| $I_S$ | Supply current | | | | 4.4 | 6 | mA |
| | | TA = –40°C to +85°C | | | | 7 | |
| SR | Slew rate[5] | $A_V$ = +2, $V_{IN}$ = 3.5$V_{PP}$ | | | 750 | | V/μs |
| | Unity-gain bandwidth | | | | 70 | | MHz |
| | −3dB frequency | $A_V$ = +1 | | | 130 | | MHz |
| | | $A_V$ = +2 | D package | | 75 | | |
| | | | P package | | 45 | | |

## 5.6 Electrical Characteristics ±5V (続き)

at $T_J$ = 25°C, $V_{CC+}$ = 5V, $V_{CC-}$ = −5V, $V_{CM}$ = 0V, and $R_L$ = 1kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN[(2)] | TYP[(1)] | MAX[(2)] | UNIT |
|---|---|---|---|---|---|---|---|
| $\varphi_m$ | Phase margin | D Package | | | 41 | | Deg |
| | | P package | | | 57 | | |
| $t_s$ | Settling time (0.1%) | $A_V$ = −1, $V_{OUT}$ = ±1V, $R_L$ = 500Ω | | | 72 | | ns |
| $A_D$ | Differential gain[(6)] | | | | 0.4 | | % |
| $\varphi_D$ | Differential phase[(6)] | | | | 0.7 | | ° |
| $e_n$ | Input-referred voltage noise | f = 10kHz | | | 11 | | nV/√Hz |
| $i_n$ | Input-referred current noise | f = 10kHz | | | 1 | | pA/√Hz |
| HD2 | Second harmonic distortion | D package | $f_{IN}$ = 10kHz | | −89 | | dBc |
| | | | $f_{IN}$ = 5MHz | | −48 | | |
| | | P package | $f_{IN}$ = 10kHz | | −110 | | |
| | | | $f_{IN}$ = 5MHz | | −48 | | |
| HD3 | Third harmonic distortion | D package | $f_{IN}$ = 10kHz | | −93 | | dBc |
| | | | $f_{IN}$ = 5MHz | | −42 | | |
| | | P package | $f_{IN}$ = 10kHz | | −105 | | |
| | | | $f_{IN}$ = 5MHz | | −50 | | |

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Large-signal voltage gain is the total output swing divided by the input signal required to produce that swing. For $V_S$ = ±15V, $V_{OUT}$ = ±5V. For $V_S$ = 5V, $V_{OUT}$ = ±1V.
(4) The open-loop output current is the output swing with the 100Ω load resistor divided by that resistor.
(5) Slew rate is the average of the rising and falling slew rates.
(6) Differential gain and phase are measured with $A_V$ = +2, $V_{IN}$ = $1V_{PP}$ at 3.58MHz and both input and output 75Ω terminated.

## 5.7 Typical Characteristics: D (SOIC, 8) Package

at $T_A$ = 25°C (unless otherwise noted)

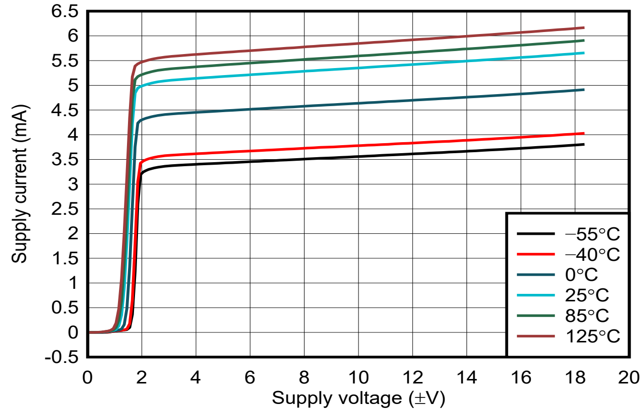



図 5-1. Supply Voltage vs Supply Current

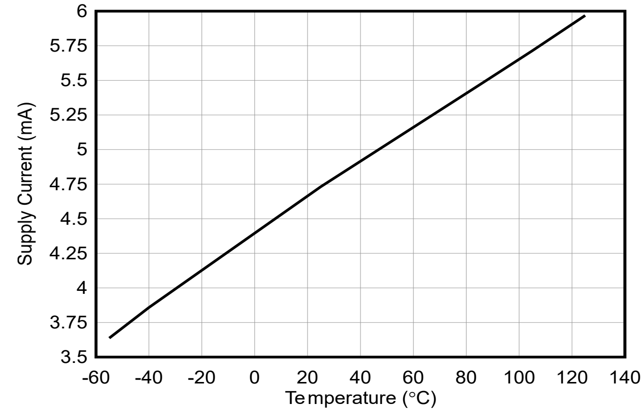



図 5-2. Supply Current vs Temperature

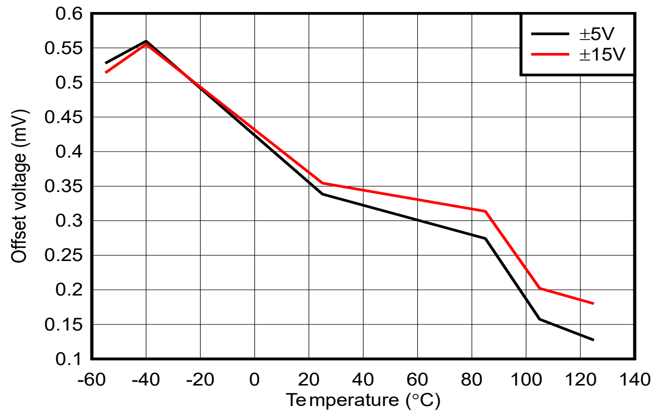



図 5-3. Input Offset Voltage vs Temperature

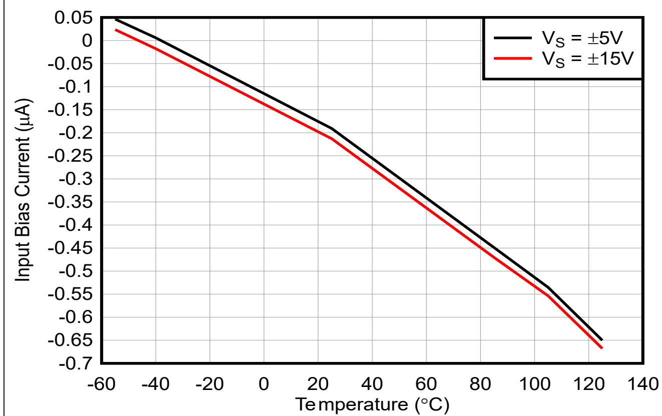



図 5-4. Input Bias Current vs Temperature

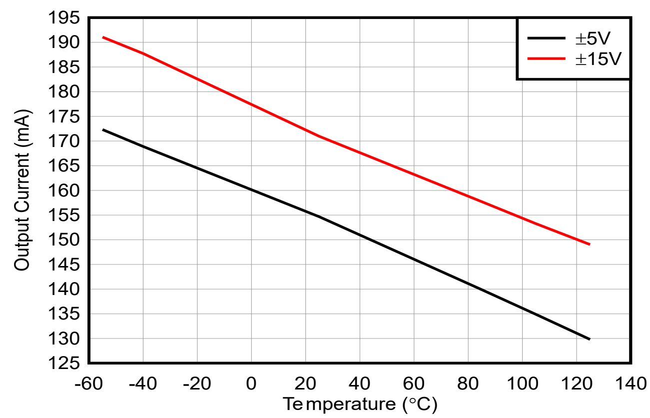



図 5-5. Short Circuit Current vs Temperature (Sourcing)

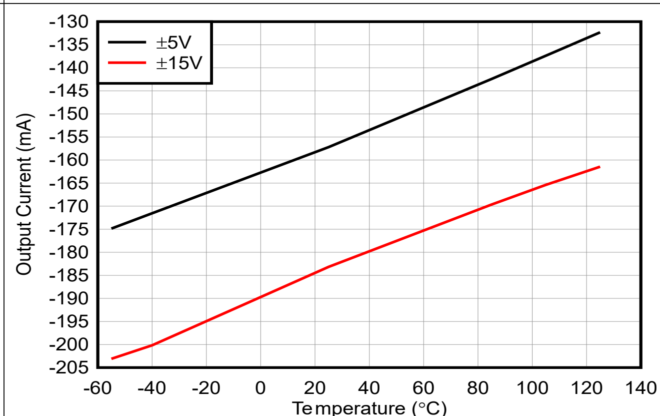



図 5-6. Short Circuit Current vs Temperature (Sinking)

## 5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)

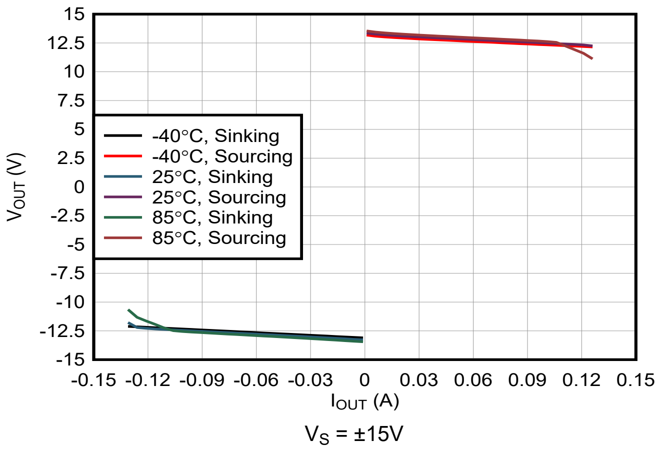



図 5-7. Output Voltage vs Output Current

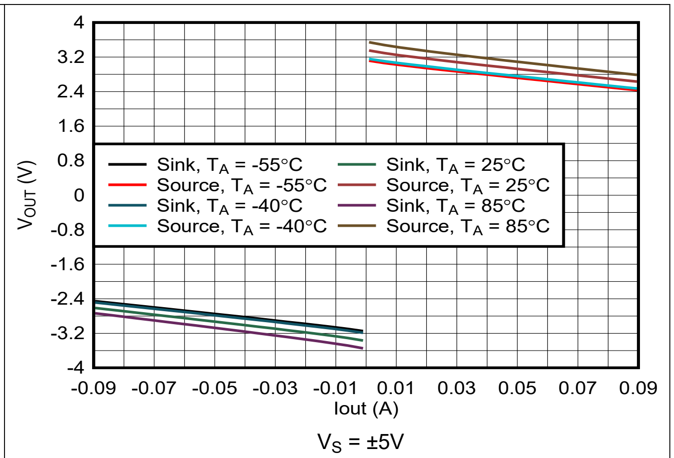



図 5-8. Output Voltage vs Output Current

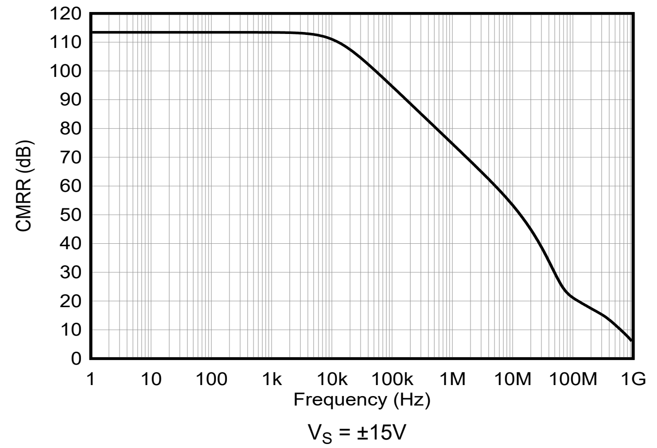



図 5-9. Common-Mode Rejection Ratio vs Frequency

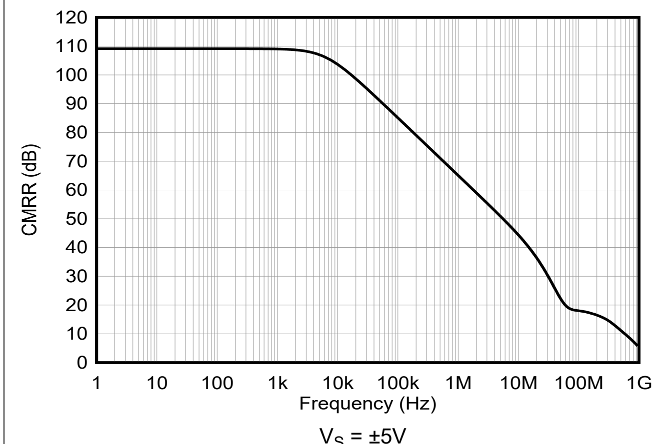



図 5-10. Common-Mode Rejection Ratio vs Frequency

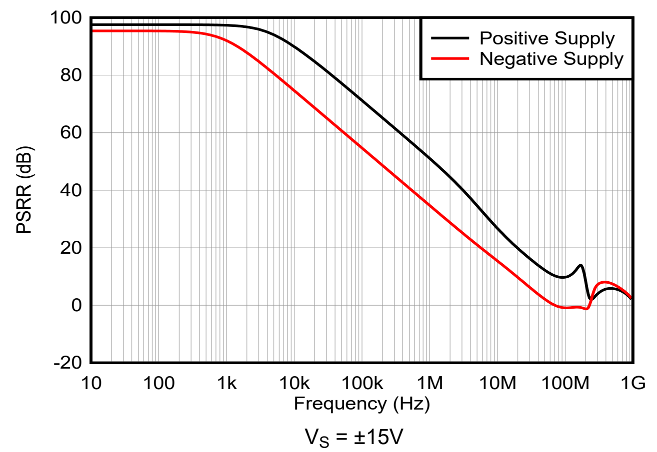



図 5-11. Power-Supply Rejection Ratio vs Frequency

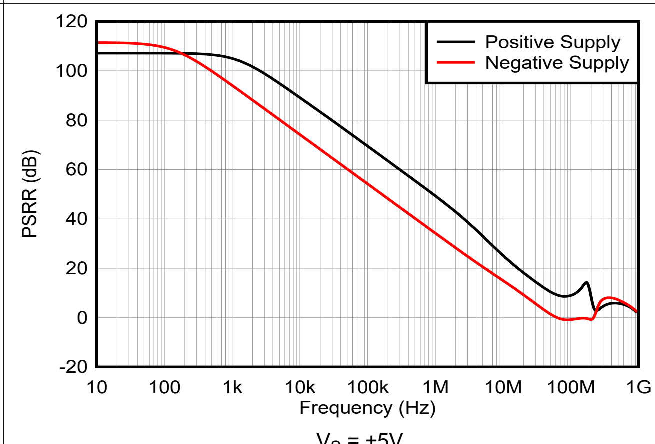



図 5-12. Power-Supply Rejection Ratio vs Frequency

## 5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)

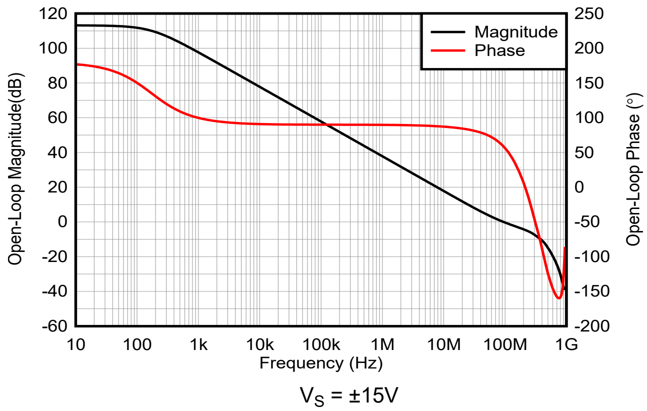



図 5-13. Open-Loop Frequency Response

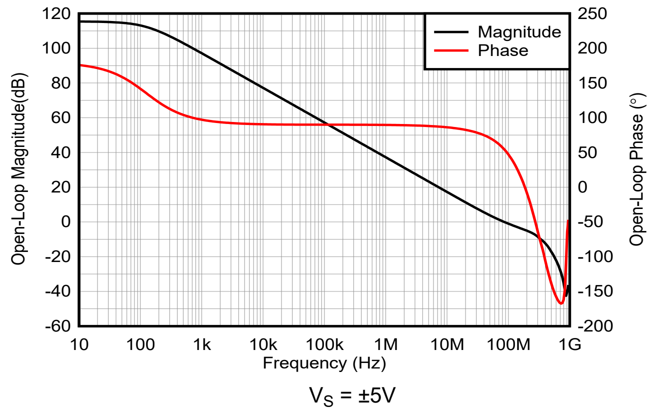



図 5-14. Open-Loop Frequency Response

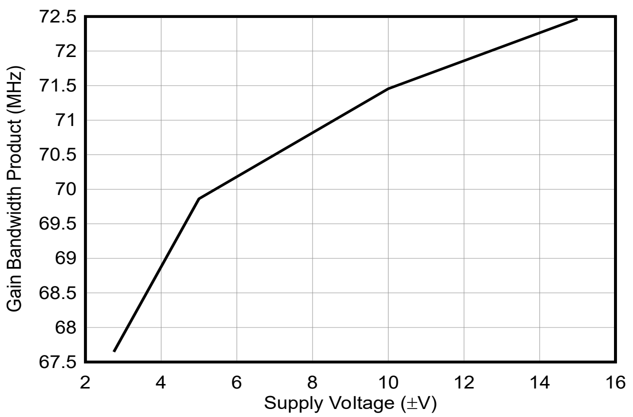



図 5-15. Gain-Bandwidth Product vs Supply Voltage at Different Temperature

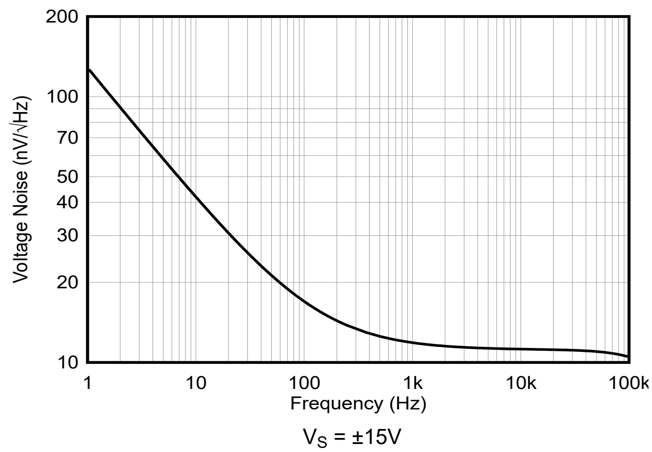



図 5-16. Input Voltage Noise vs Frequency

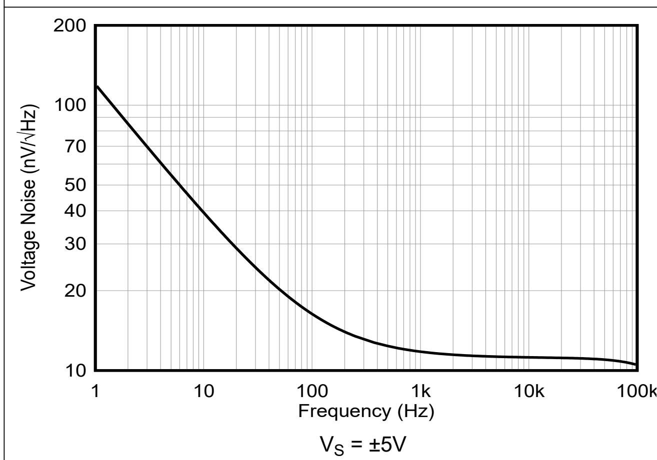



図 5-17. Input Voltage Noise vs Frequency

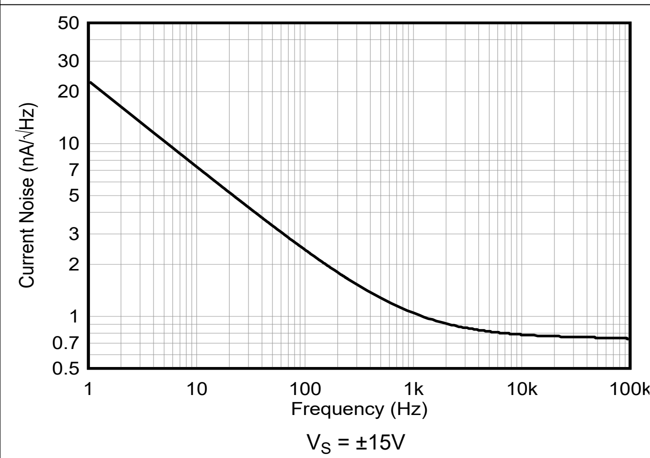
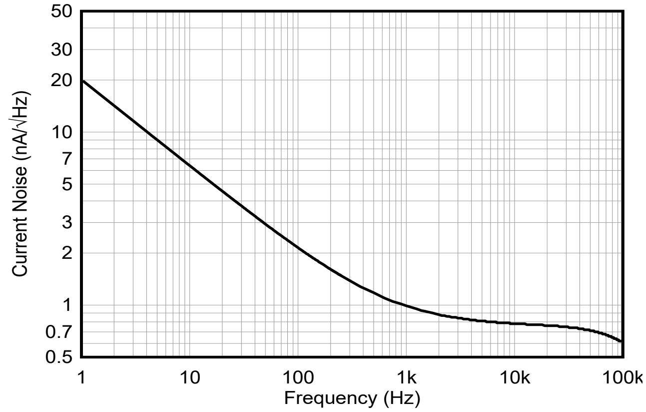



図 5-18. Input Current Noise vs Frequency

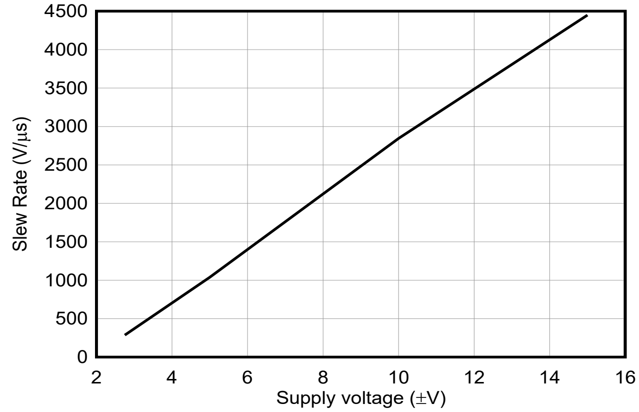
## 5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)



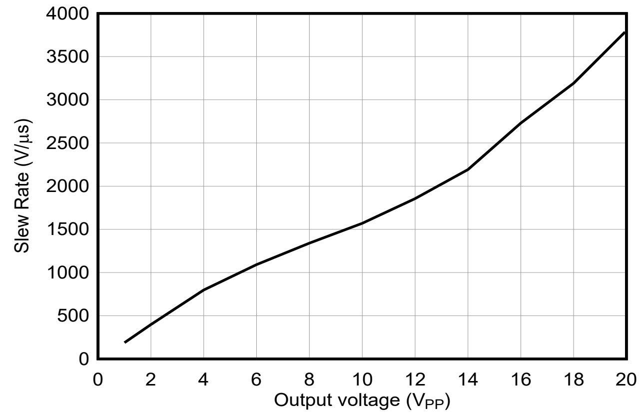

$V_S$ = ±5V

**図 5-19. Input Current Noise vs Frequency**



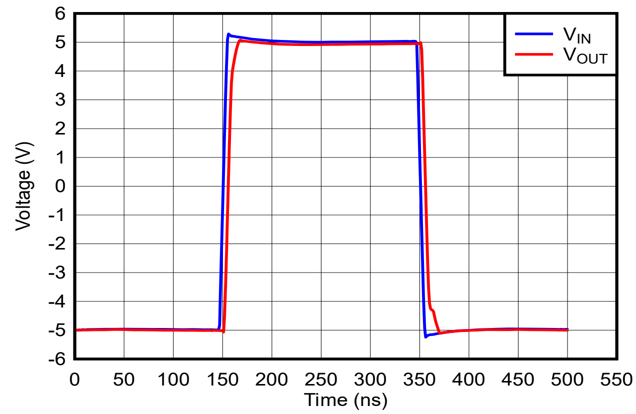

$A_V$ = +2

**図 5-20. Slew Rate vs Supply Voltage**



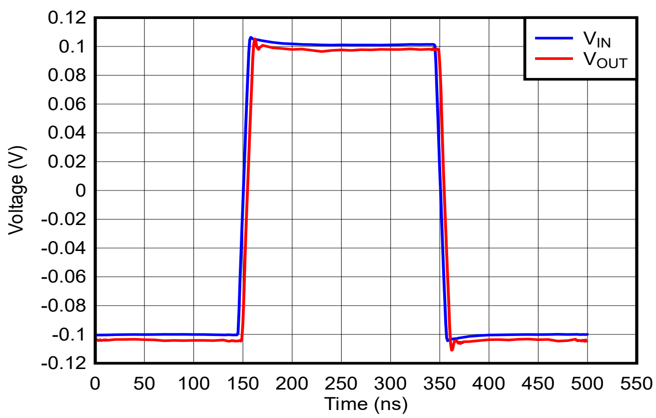

$A_V$ = +2

**図 5-21. Slew Rate vs Output Voltage**



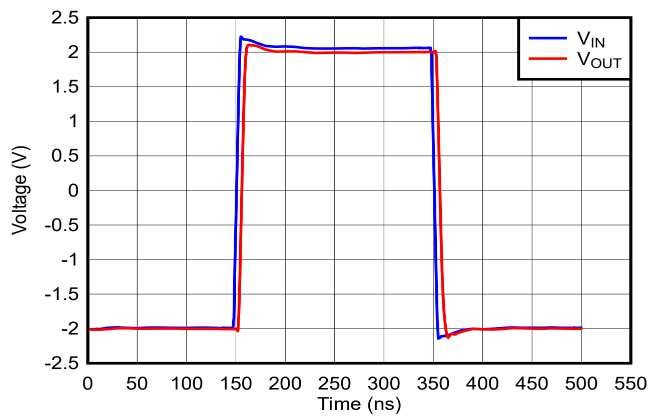

$A_V$ = +1, $V_S$ = ±15V

**図 5-22. Large-Signal Pulse Response**




$A_V$ = +1, $V_S$ = ±15V

**図 5-23. Small-Signal Pulse Response**

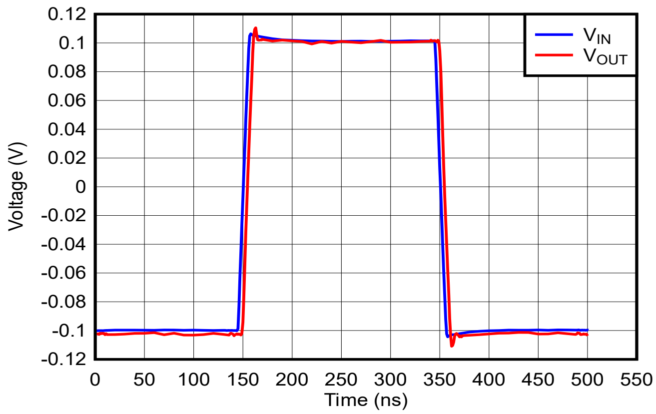



$A_V$ = +1, $V_S$ = ±5V

**図 5-24. Large-Signal Pulse Response**

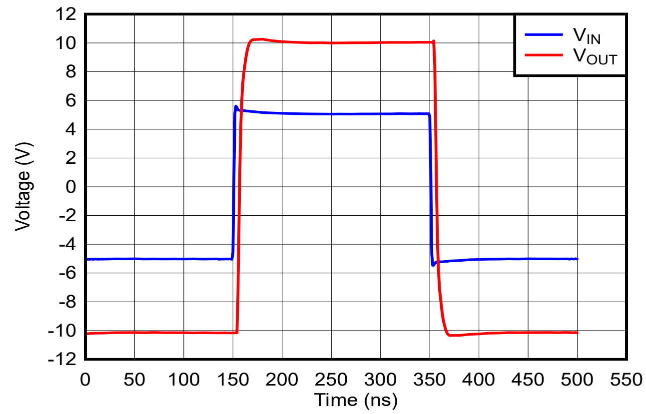
## 5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)



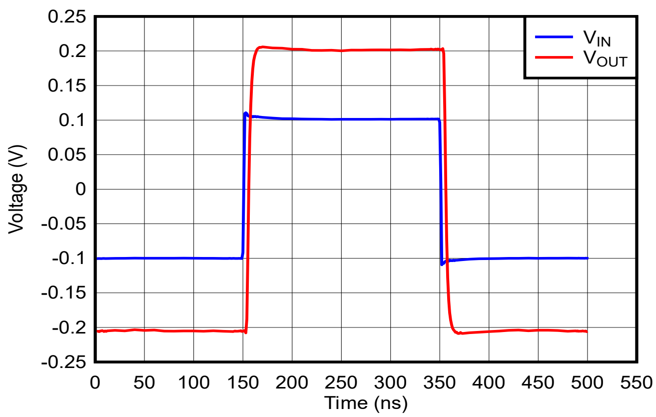

$A_V$ = +1, $V_S$ = ±5V

**図 5-25. Small-Signal Pulse Response**



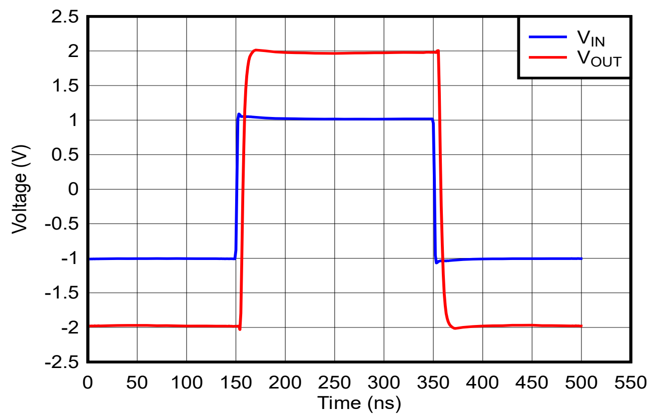

$A_V$ = +2, $V_S$ = ±15V

**図 5-26. Large-Signal Pulse Response**



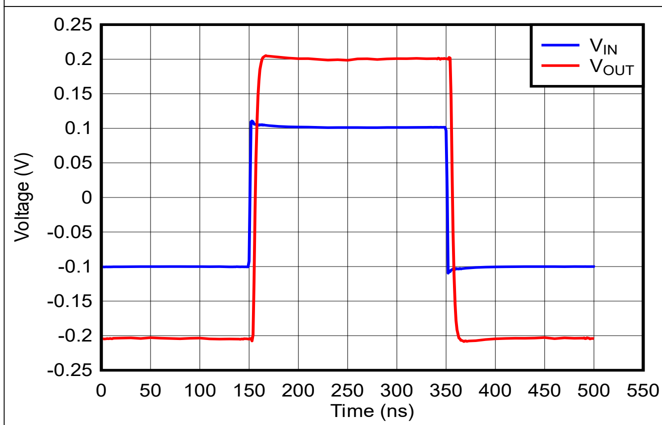

$A_V$ = +2, $V_S$ = ±15V

**図 5-27. Small-Signal Pulse Response**



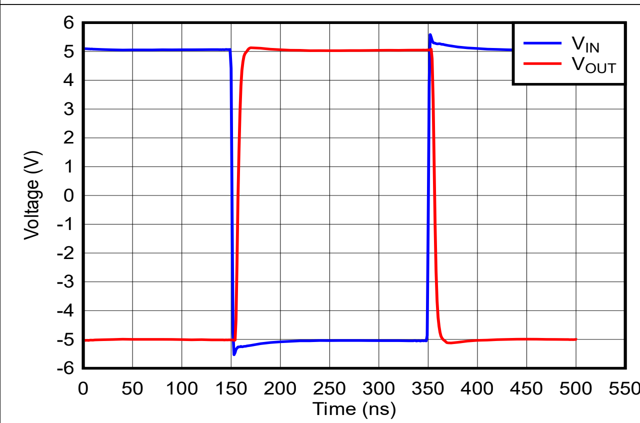

$A_V$ = +2, $V_S$ = ±5V

**図 5-28. Large-Signal Pulse Response**




$A_V$ = +2, $V_S$ = ±5V

**図 5-29. Small-Signal Pulse Response**

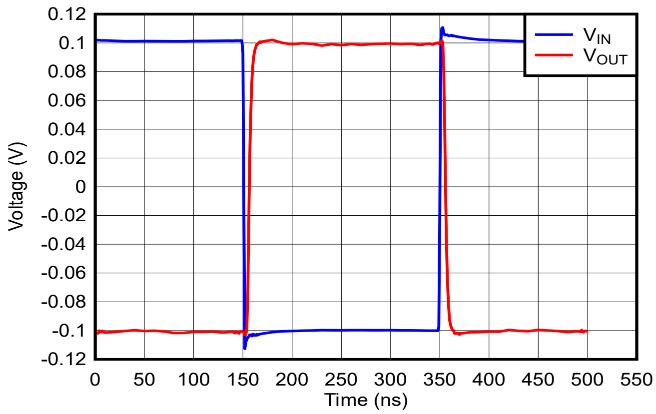



$A_V$ = −1, $V_S$ = ±15V

**図 5-30. Large-Signal Pulse Response**

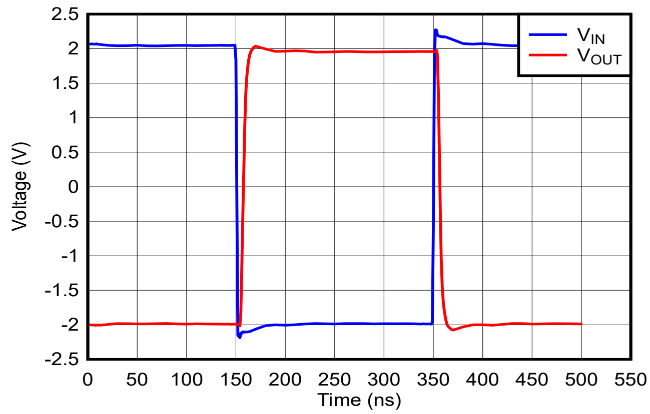
## 5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)



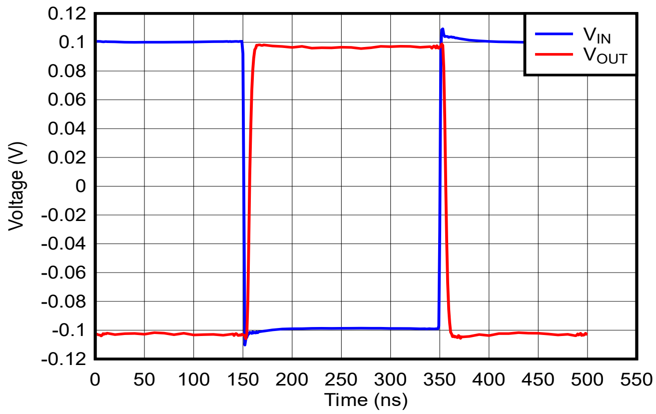

$A_V$ = −1, $V_S$ = ±15V

**図 5-31. Small-Signal Pulse Response**



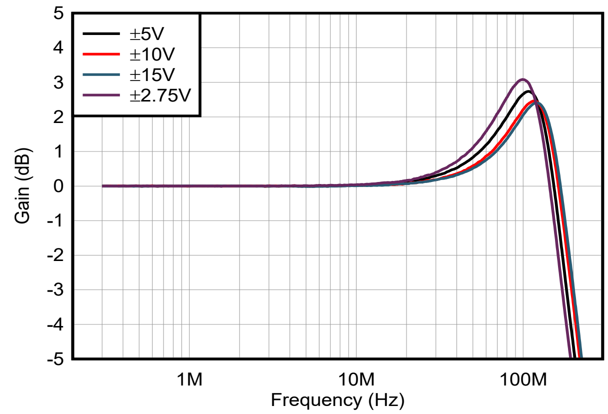

$A_V$ = −1, $V_S$ = ±5V

**図 5-32. Large-Signal Pulse Response**



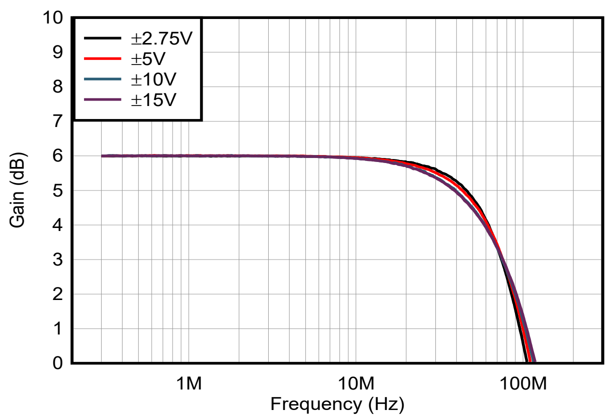

$A_V$ = −1, $V_S$ = ±5V

**図 5-33. Small-Signal Pulse Response**



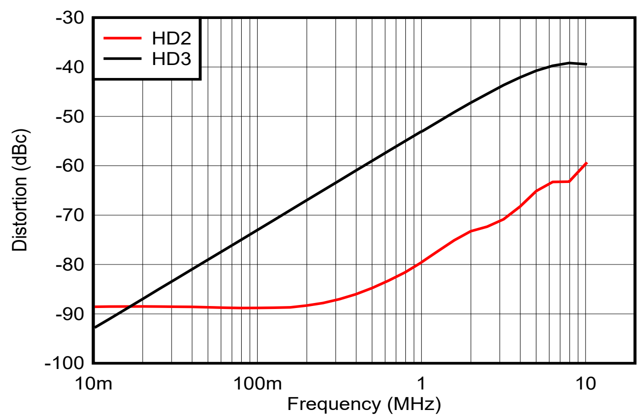

$A_V$ = +1

**図 5-34. Closed-Loop Frequency Response vs Supply Voltage**




$A_V$ = +2

**図 5-35. Closed-Loop Frequency Response vs Supply Voltage**

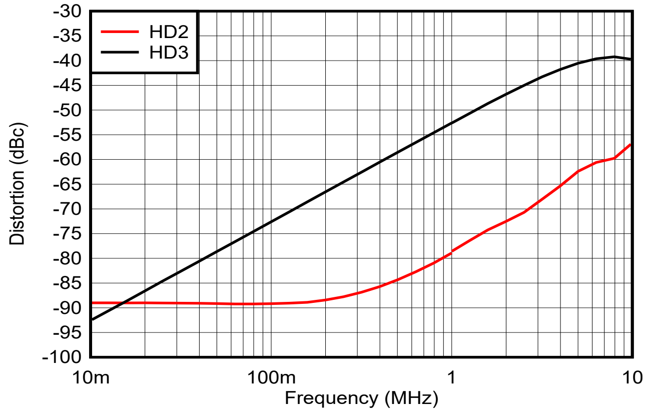



$V_S$ = ±15V

**図 5-36. Harmonic Distortion vs Frequency**

## 5.7 Typical Characteristics: D (SOIC, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)




$V_S$ = ±5V

図 5-37. Harmonic Distortion vs Frequency

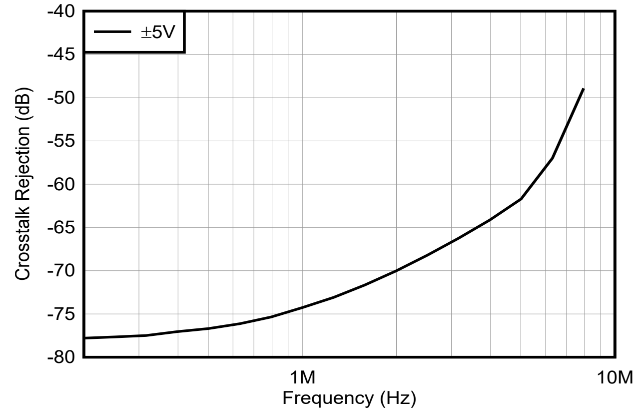



図 5-38. Crosstalk Rejection vs Frequency

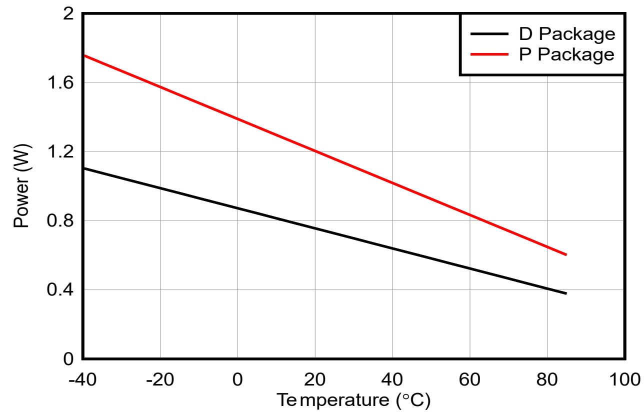



図 5-39. Maximum Power Dissipation vs Ambient Temperature

## 5.8 Typical Characteristics: P (PDIP, 8) Package

at $T_A$ = 25°C (unless otherwise noted)

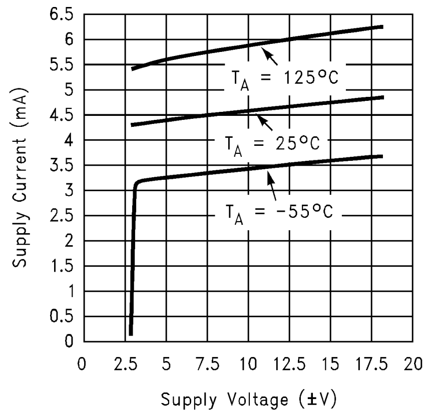



図 5-40. Supply Voltage vs. Supply Current

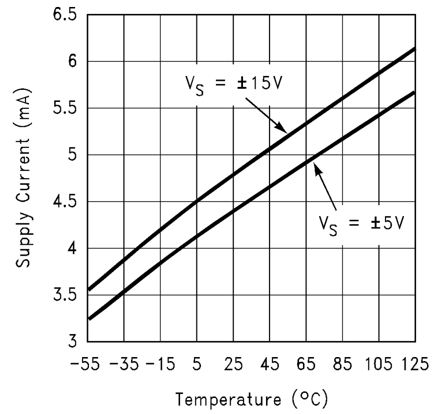



図 5-41. Supply Current vs Temperature

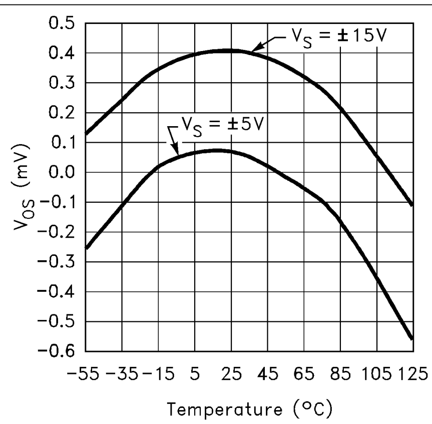



図 5-42. Input Offset Voltage vs Temperature

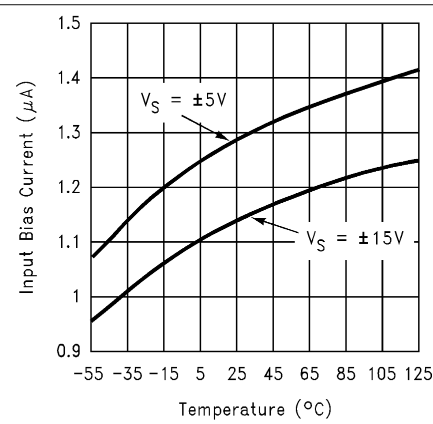



図 5-43. Input Bias Current vs Temperature

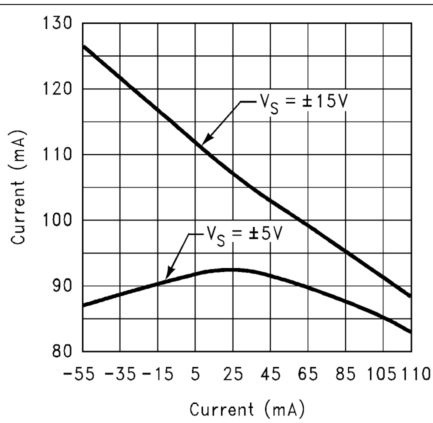



図 5-44. Short Circuit Current vs Temperature (Sourcing)

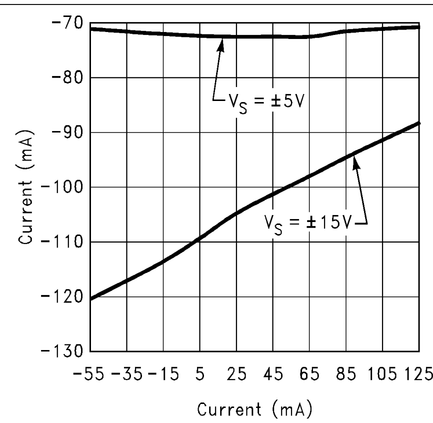



図 5-45. Short Circuit Current vs Temperature (Sinking)

## 5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)

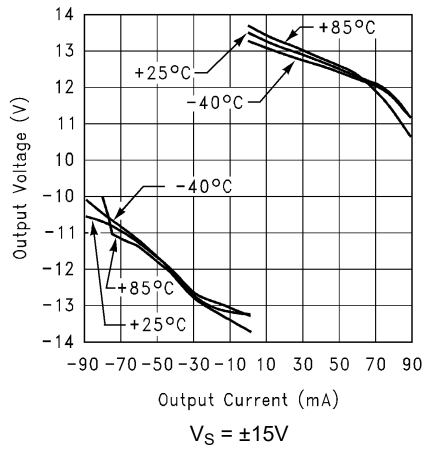



図 5-46. Output Voltage vs Output Current

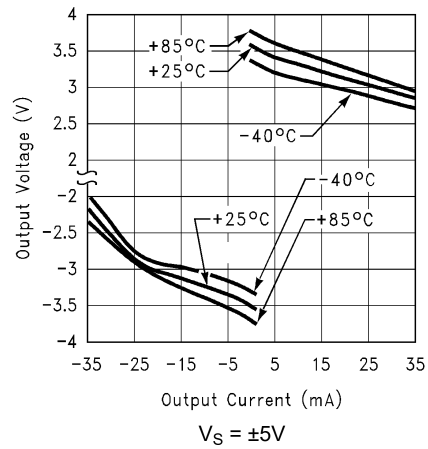



図 5-47. Output Voltage vs Output Current

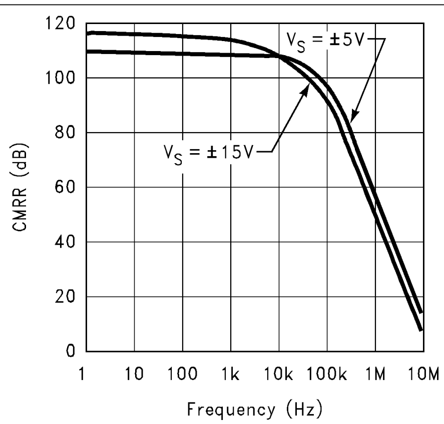



図 5-48. Common-Mode Rejection Ratio vs Frequency

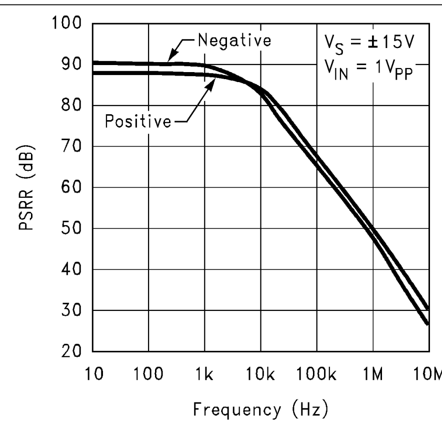



図 5-49. PSRR vs Frequency

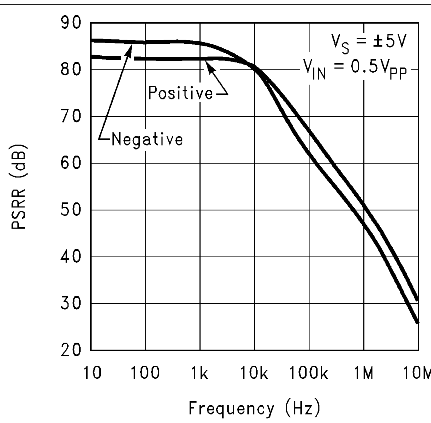



図 5-50. PSRR vs Frequency

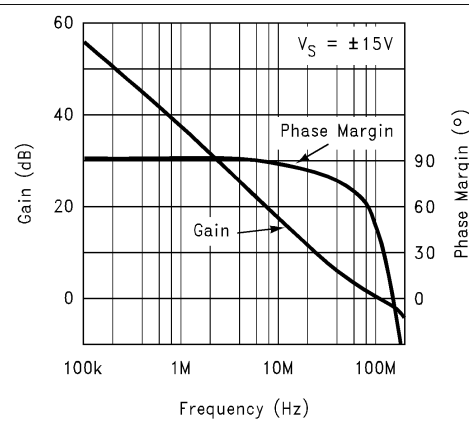



図 5-51. Open-Loop Frequency Response

## 5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)

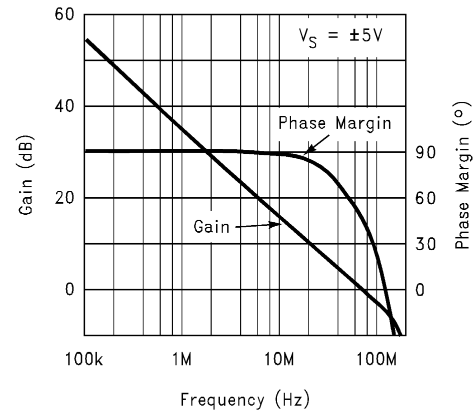



図 5-52. Open-Loop Frequency Response

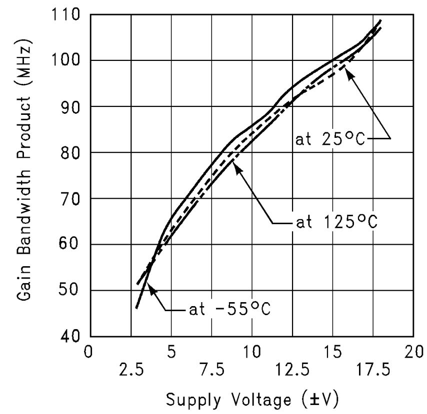



図 5-53. Gain-Bandwidth Product vs Supply Voltage at Different Temperature

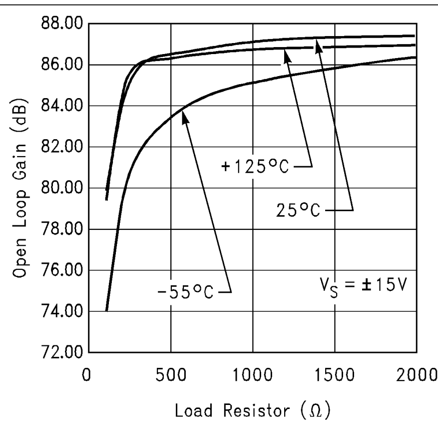



図 5-54. Large-Signal Voltage Gain vs Load

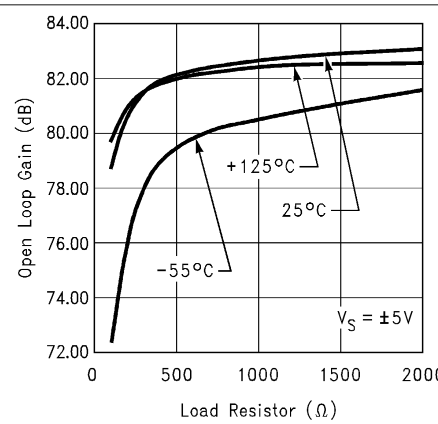



図 5-55. Large-Signal Voltage Gain vs Load

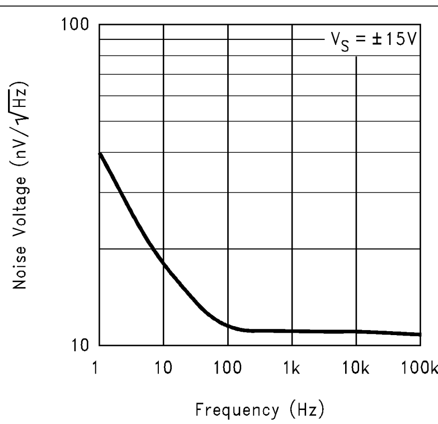



図 5-56. Input Voltage Noise vs Frequency

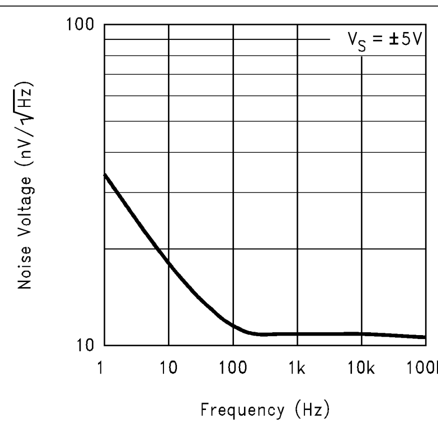



図 5-57. Input Voltage Noise vs Frequency

## 5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)

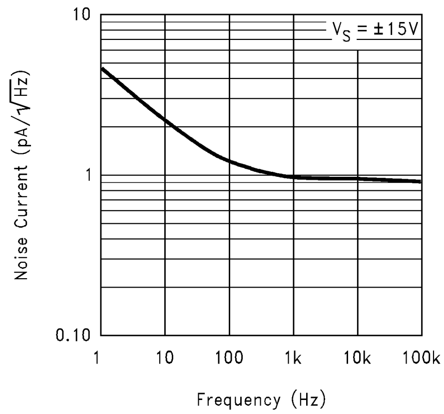



**図 5-58. Input Current Noise vs Frequency**

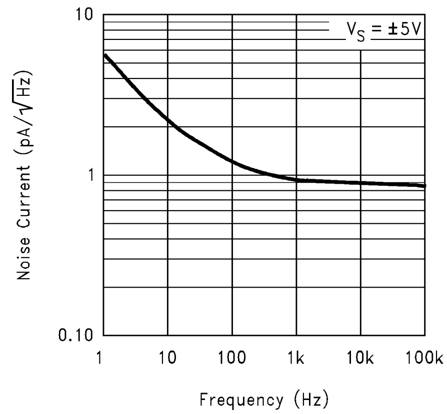



**図 5-59. Input Current Noise vs Frequency**

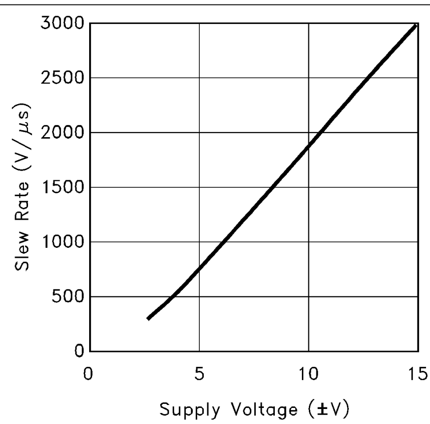



**図 5-60. Slew Rate vs Supply Voltage**

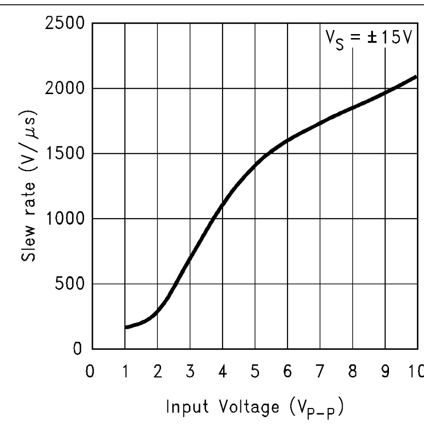
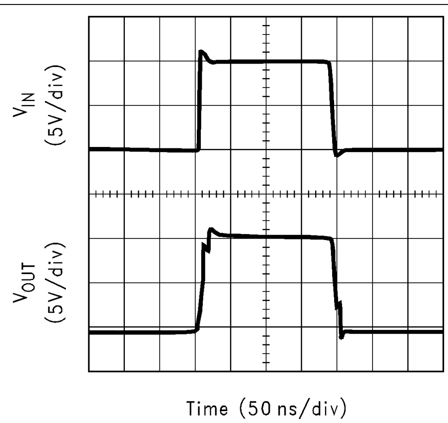
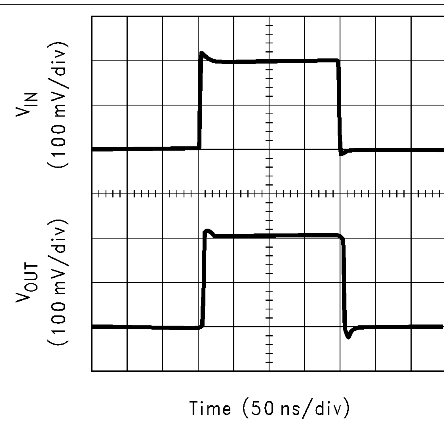



**図 5-61. Slew Rate vs Input Voltage**




$A_V$ = +1, $V_S$ = ±15V

**図 5-62. Large-Signal Pulse Response**

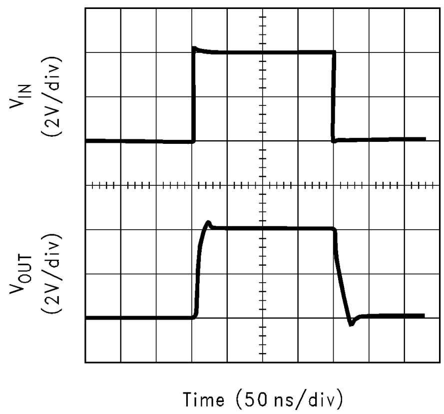



$A_V$ = +1, $V_S$ = ±15V

**図 5-63. Small-Signal Pulse Response**

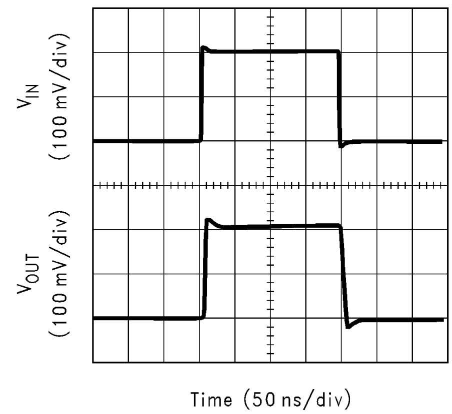
## 5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)



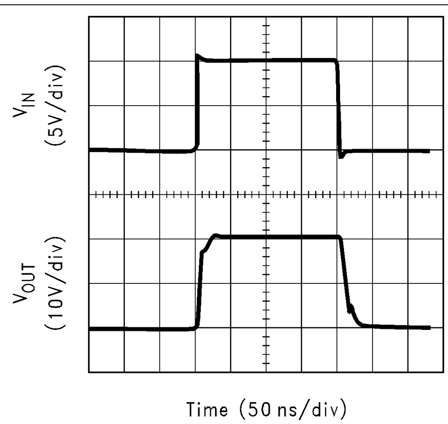

$A_V$ = +1, $V_S$ = ±5V

**図 5-64. Large-Signal Pulse Response**



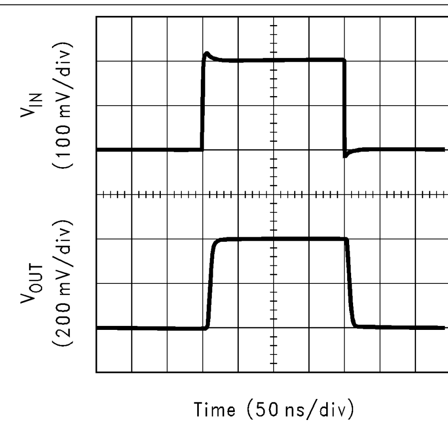

$A_V$ = +1, $V_S$ = ±5V

**図 5-65. Small-Signal Pulse Response**



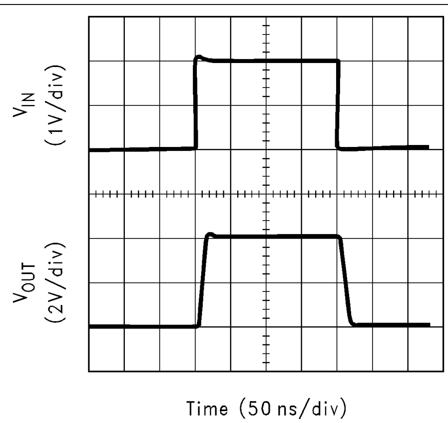

$A_V$ = +2, $V_S$ = ±15V

**図 5-66. Large-Signal Pulse Response**



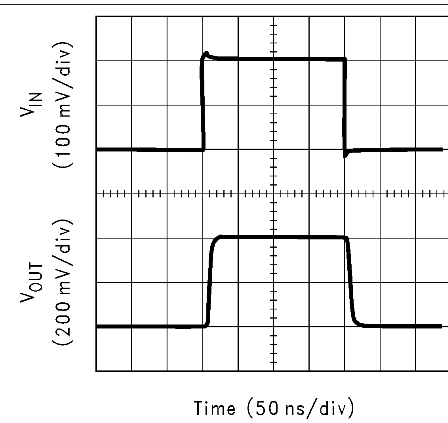

$A_V$ = +2, $V_S$ = ±15V

**図 5-67. Small-Signal Pulse Response**




$A_V$ = +2, $V_S$ = ±5V

**図 5-68. Large-Signal Pulse Response**

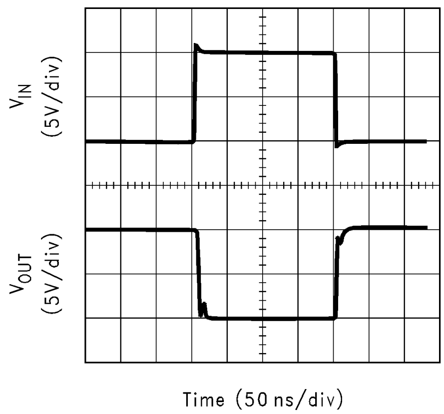



$A_V$ = +2, $V_S$ = ±5V

**図 5-69. Small-Signal Pulse Response**

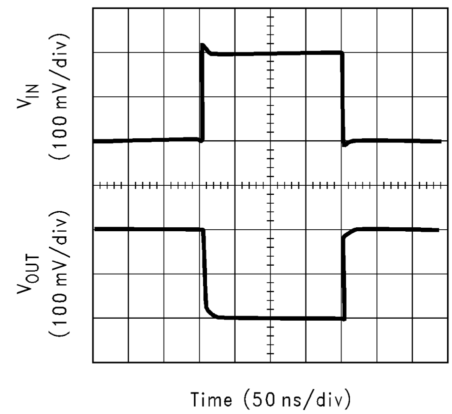
## 5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)



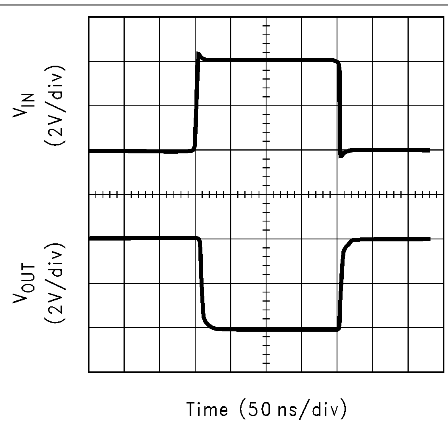

$A_V$ = −1, $V_S$ = ±15V

**図 5-70. Large-Signal Pulse Response**



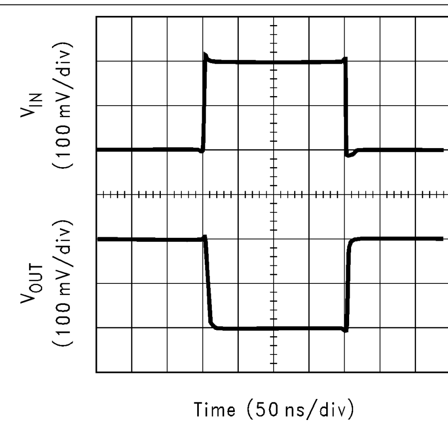

$A_V$ = −1, $V_S$ = ±15V

**図 5-71. Small-Signal Pulse Response**



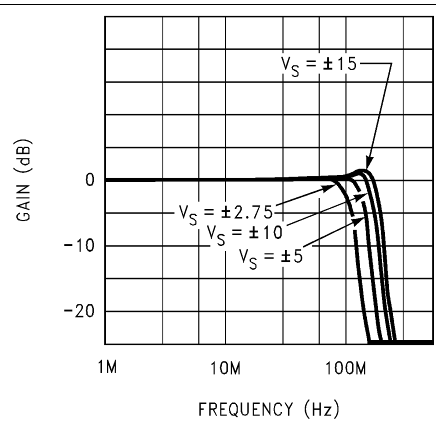

$A_V$ = −1, $V_S$ = ±5V

**図 5-72. Large-Signal Pulse Response**



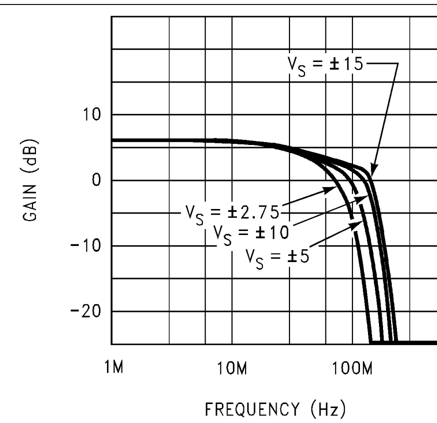

$A_V$ = −1, $V_S$ = ±5V

**図 5-73. Small-Signal Pulse Response**




$A_V$ = +1

**図 5-74. Closed-Loop Frequency Response vs Supply Voltage**

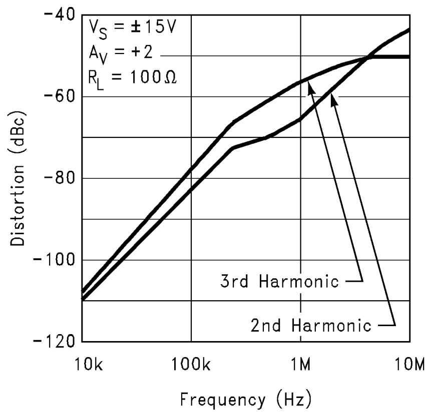



$A_V$ = +2

**図 5-75. Closed-Loop Frequency Response vs Supply Voltage**

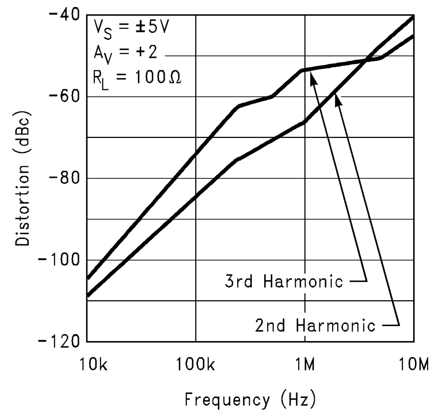
## 5.8 Typical Characteristics: P (PDIP, 8) Package (continued)

at $T_A$ = 25°C (unless otherwise noted)




$V_S$ = ±15V

**図 5-76. Harmonic Distortion vs Frequency**




$V_S$ = ±5V

**図 5-77. Harmonic Distortion vs Frequency**

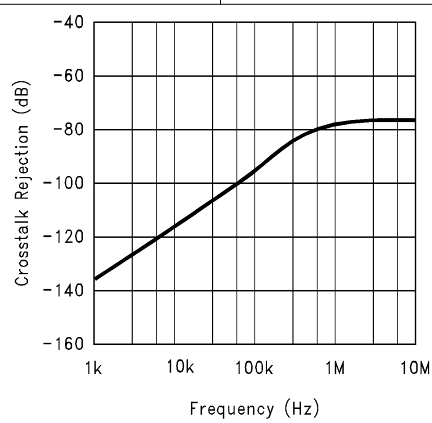


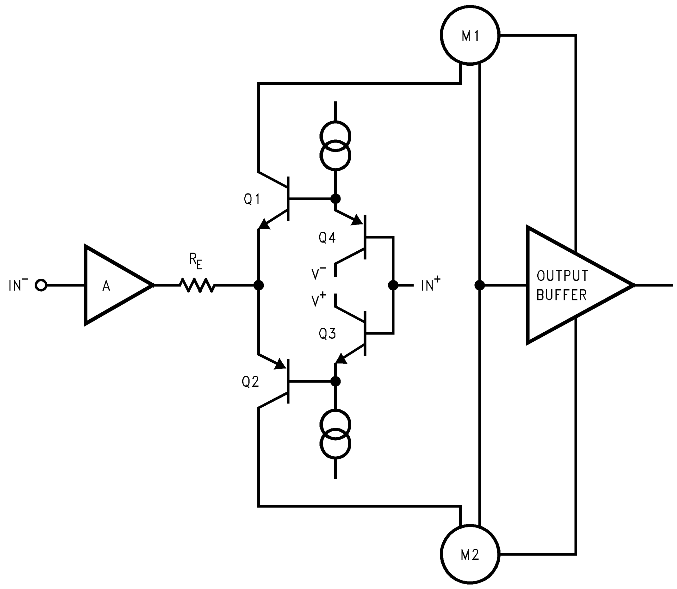

**図 5-78. Crosstalk Rejection vs Frequency**

# 6 Detailed Description

## 6.1 Overview

The LM6172 is a dual, high-speed, low-power, voltage-feedback amplifier. The device is unity-gain stable and offers outstanding performance with only 2.3mA of supply current per channel. The combination of 100MHz unity-gain bandwidth, 3000V/µs slew rate, 50mA per channel output current, and other attractive features makes the LM6172 easy to implement in various applications. The quiescent power of the LM6172 is 138mW operating at a ±15V supply and 46mW at a ±5V supply.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### *6.3.1 Slew Rate*

The slew rate of LM6172 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor $R_E$. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast, large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor (such as 1kΩ) to the input of LM6172, the slew rate is reduced to help lower the overshoot, which reduces settling time.

# 7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 7.1 Application Information

### *7.1.1 Circuit Operation*

The class AB input stage in LM6172 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the functional block diagram of セクション 6.2, Q1 through Q4 form the equivalent of the current feedback input buffer, $R_E$ the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

### *7.1.2 Reduce Settling Time*

The LM6172 has a very fast slew rate that causes overshoot and undershoot. To reduce settling time on LM6172, a 1kΩ resistor can be placed in series with the input signal to decrease slew rate. A feedback capacitor can also be used to reduce overshoot and undershoot. This feedback capacitor serves as a zero to increase the stability of the amplifier circuit. A 2pF feedback capacitor is recommended for initial evaluation. When the LM6172 is configured as a buffer, a feedback resistor of 1kΩ must be added in parallel to the feedback capacitor.

Another possible source of overshoot and undershoot comes from capacitive load at the output. See also セクション 7.1.3.

### *7.1.3 Drive Capacitive Loads*

Amplifiers that drive capacitive loads can oscillate or ring at the output. To eliminate oscillation or reduce ringing, place an isolation resistor as shown in 図 7-1. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped (slow) the pulse response becomes. For the LM6172, a 50Ω isolation resistor is recommended for initial evaluation.

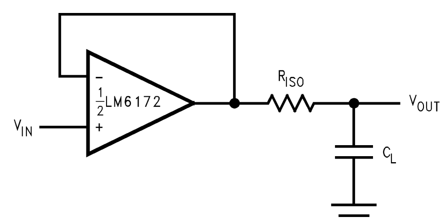



**図 7-1. Isolation Resistor Used to Drive Capacitive Load**

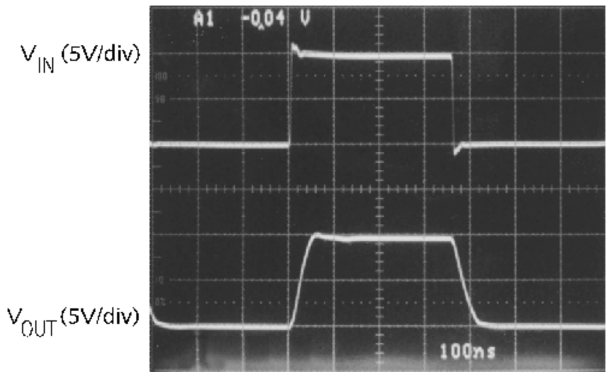



**図 7-2. The LM6172 Driving a 510pF Load With a 30Ω Isolation Resistor**

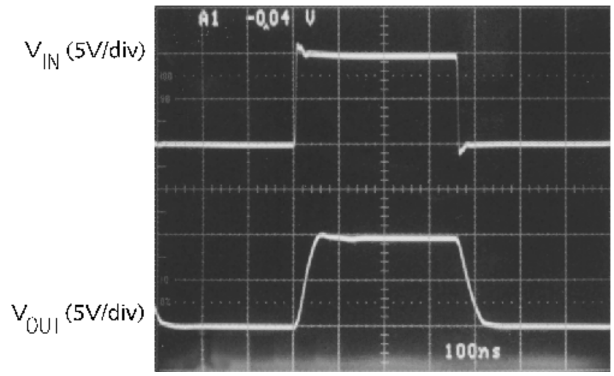



**図 7-3. The LM6172 Driving a 220pF Load With a 50Ω Isolation Resistor**

### *7.1.4 Compensation for Input Capacitance*

The combination of an amplifier input capacitance with gain-setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with the following value can be used to cancel that pole:

$$C_F > (R_G \times C_{IN}) / R_F \tag{1}$$

For the LM6172, a feedback capacitor of 2pF is recommended. 図 7-4 illustrates the compensation circuit.

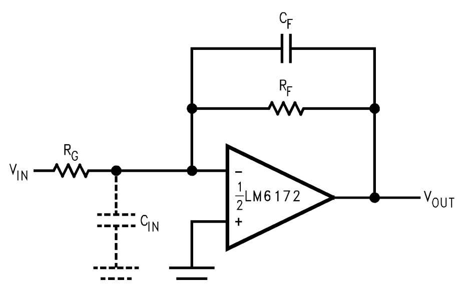



**図 7-4. Compensating for Input Capacitance**

### *7.1.5 Termination*

In high-frequency applications, reflections occur if signals are not properly terminated. 図 7-5 shows a properly terminated signal while 図 7-6 shows an improperly terminated signal.

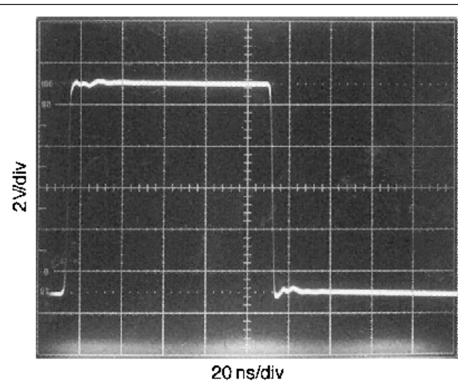



**図 7-5. Properly Terminated Signal**

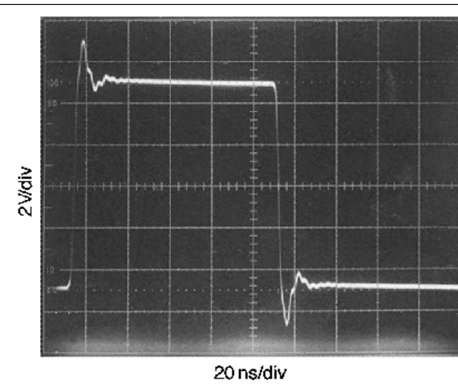



**図 7-6. Improperly Terminated Signal**

To minimize reflection, use coaxial cable with matching characteristic impedance to the signal source. Terminate the other end of the cable with the same value terminator or resistor. For commonly used cables, RG59 has a 75Ω characteristic impedance, and RG58 has a 50Ω characteristic impedance.

## 7.2 Typical Application

### *7.2.1 Application Circuits*

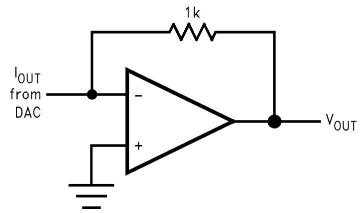



**図 7-7. I-to-V Converters**

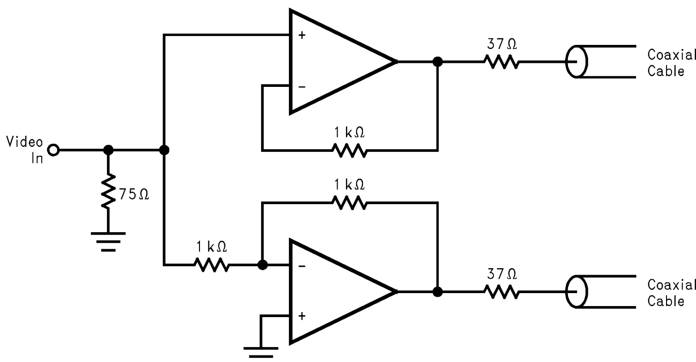



**図 7-8. Differential Line Driver**

## 7.3 Power Supply Recommendations

### 7.3.1 Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Bypass both positive and negative power supplies individually by placing 0.01µF ceramic capacitors directly to the power supply pins and 2.2µF tantalum capacitors close to the power-supply pins.

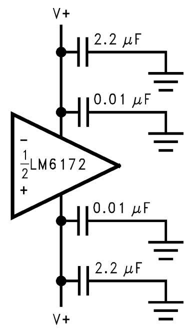



**図 7-9. Power Supply Bypassing**

### 7.3.2 Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A) / \theta_{JA} \quad (2)$$

where

- $P_D$ is the power dissipation in a device
- $T_{J(max)}$ is the maximum junction temperature
- $T_A$ is the ambient temperature
- $\theta_{JA}$ is the thermal resistance of a particular package

For example, for the LM6172 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 726mW.

Thermal resistance, $\theta_{JA}$, depends on parameters such as die size, package size, and package material. The smaller the die size and package, the higher the $\theta_{JA}$. The 8-pin PDIP package has lower thermal resistance (108°C/W) than that of the 8-pin SOIC (172°C/W). Therefore, for higher dissipation capability, use an 8-pin PDIP.

The total power dissipated in a device can also be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

where

- $P_Q$ is quiescent power dissipated in a device with no load connected at the output.
- $P_L$ is power dissipated in the device with a load connected at the output, not power dissipated by the load.

Furthermore,

- $P_Q$ = supply current × total supply voltage with no load
- $P_L$ = output current × (voltage difference between supply voltage and output voltage of the same supply)

For example, use 式 3 to solve the total power dissipated by the LM6172 with $V_S$ = ±15V and both channels swinging output voltage of 10V into 1kΩ:

- = 2[(2.3mA)(30V)] + 2[(10mA)(15V − 10V)]
- = 138mW + 100mW
- = 238mW

## 7.4 Layout

### *7.4.1 Layout Guidelines*

#### 7.4.1.1 Printed Circuit Boards and High-Speed Op Amps

There are many things to consider when designing printed circuit boards (PCBs) for high-speed op amps. Without proper caution, excessive ringing, oscillation and other degraded ac performance in high-speed circuits can occur. As a rule, use short and wide the signal traces to provide low inductance and low impedance paths. Ground any unused board space to reduce stray signal pickup. Also ground critical components at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. Best practice is to solder the amplifier directly into the PCB without using a socket.

#### 7.4.1.2 Using Probes

Active (FET) probes are an excellent choice for taking high-frequency measurements because these probes have wide bandwidth, high input impedance, and low input capacitance. However, the probe ground leads provide a long ground loop that produces errors in measurement. Instead, ground the probes directly by removing the ground leads and probe jackets and using scope probe jacks.

#### 7.4.1.3 Components Selection and Feedback Resistor

In high-speed applications, keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface-mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high-speed amplifiers. For the LM6172, a feedback resistor less than 1kΩ gives optimized performance.

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 8.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

## 8.3 Trademarks

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## 8.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision D (March 2013) to Revision E (December 2024)** **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「パッケージ情報」表、「ピン構成および機能」、「仕様」、「ESD 定格」、「推奨動作条件」、「熱に関する情報」、「詳細説明」、「概要」、「機能ブロック図」、「機能説明」、「デバイスの機能モード」、「アプリケーションと実装」、「代表的なアプリケーション」、「電源に関する推奨事項」、「レイアウト」、「レイアウトのガイドライン」、「レイアウト例」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- Changed pin names and updated pinout diagram to reflect new naming convention ... 3
- Updated *Thermal Information* for the D (SOIC-8) and P (PDIP-8) packages ... 4
- Moved *DC and AC Electrical Characteristics* into one table for both ±15V and ±5V specifications ... 5
- Changed output short-circuit current for D package ... 5
- Updated unity-gain bandwidth from 100MHz to 80MHz for D package ... 5
- Updated second harmonic distortion for D package ... 5
- Updated third harmonic distortion for D package ... 5
- Changed output short-circuit current for D package ... 7
- Updated –3dB frequency for D package ... 7
- Updated phase margin for D package ... 7
- Updated second harmonic distortion for D package ... 7

**Changes from Revision C (March 2013) to Revision D (March 2013)** **Page**



## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM6172IM/NOPB | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 85 | LM61 72IM | |
| LM6172IMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | LM61 72IM | Samples |
| LM6172IN/NOPB | ACTIVE | PDIP | P | 8 | 40 | RoHS & Green | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | LM6172IN | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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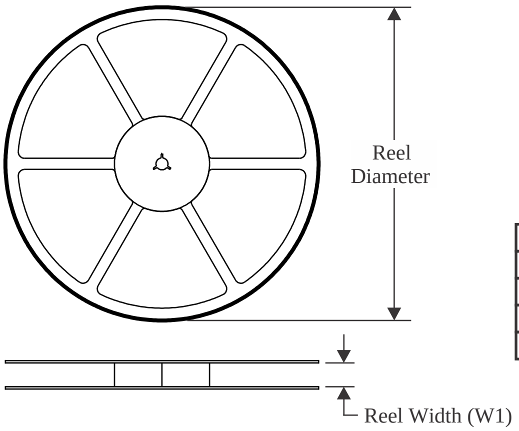
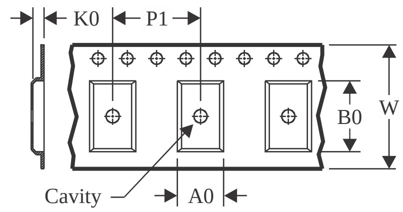
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

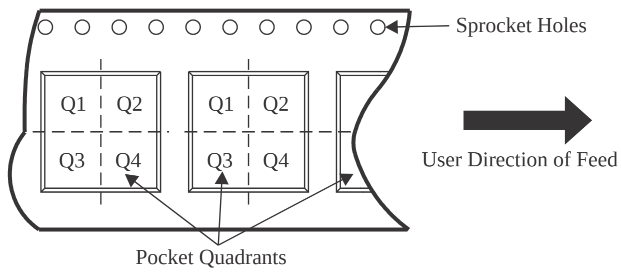



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

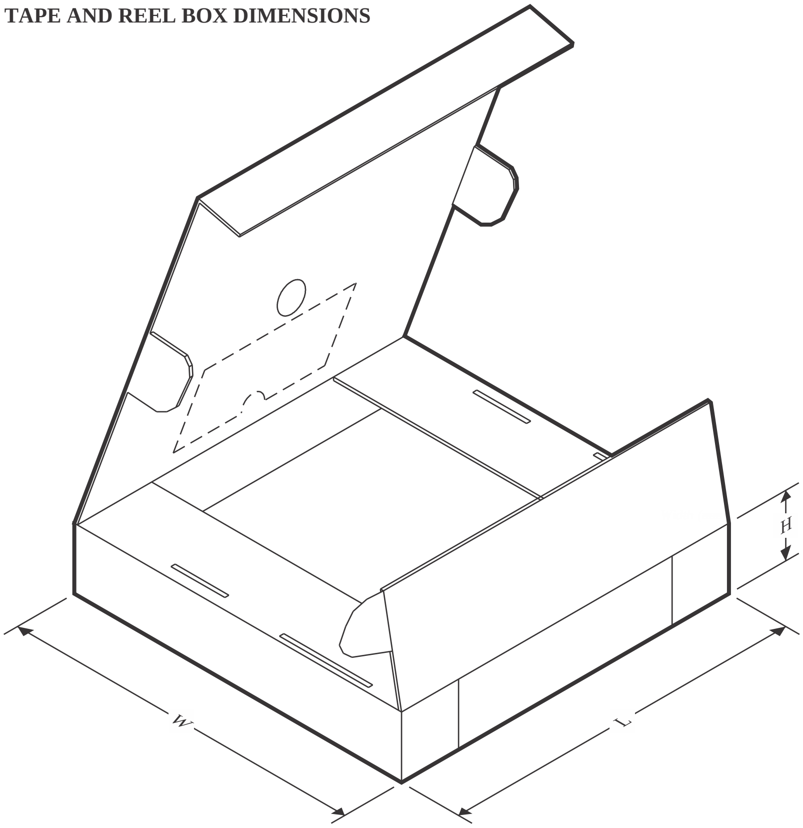
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM6172IMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

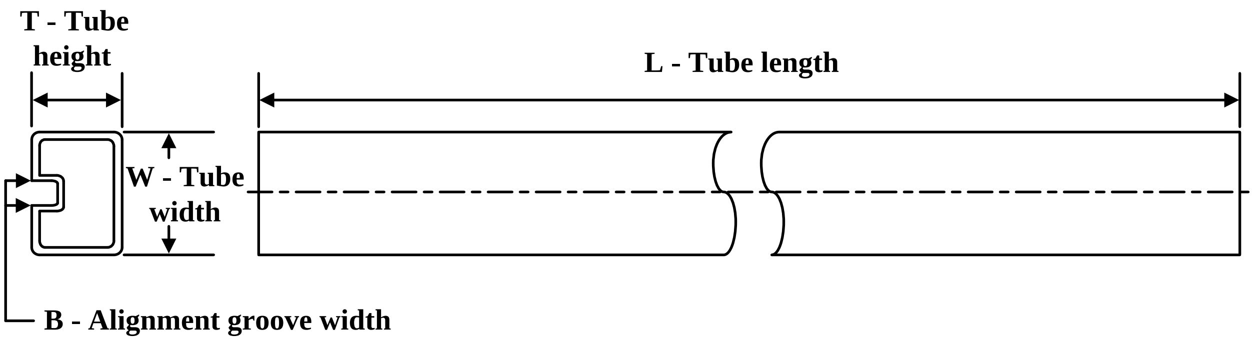
## TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

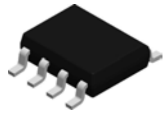
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM6172IMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

## TUBE




*All dimensions are nominal

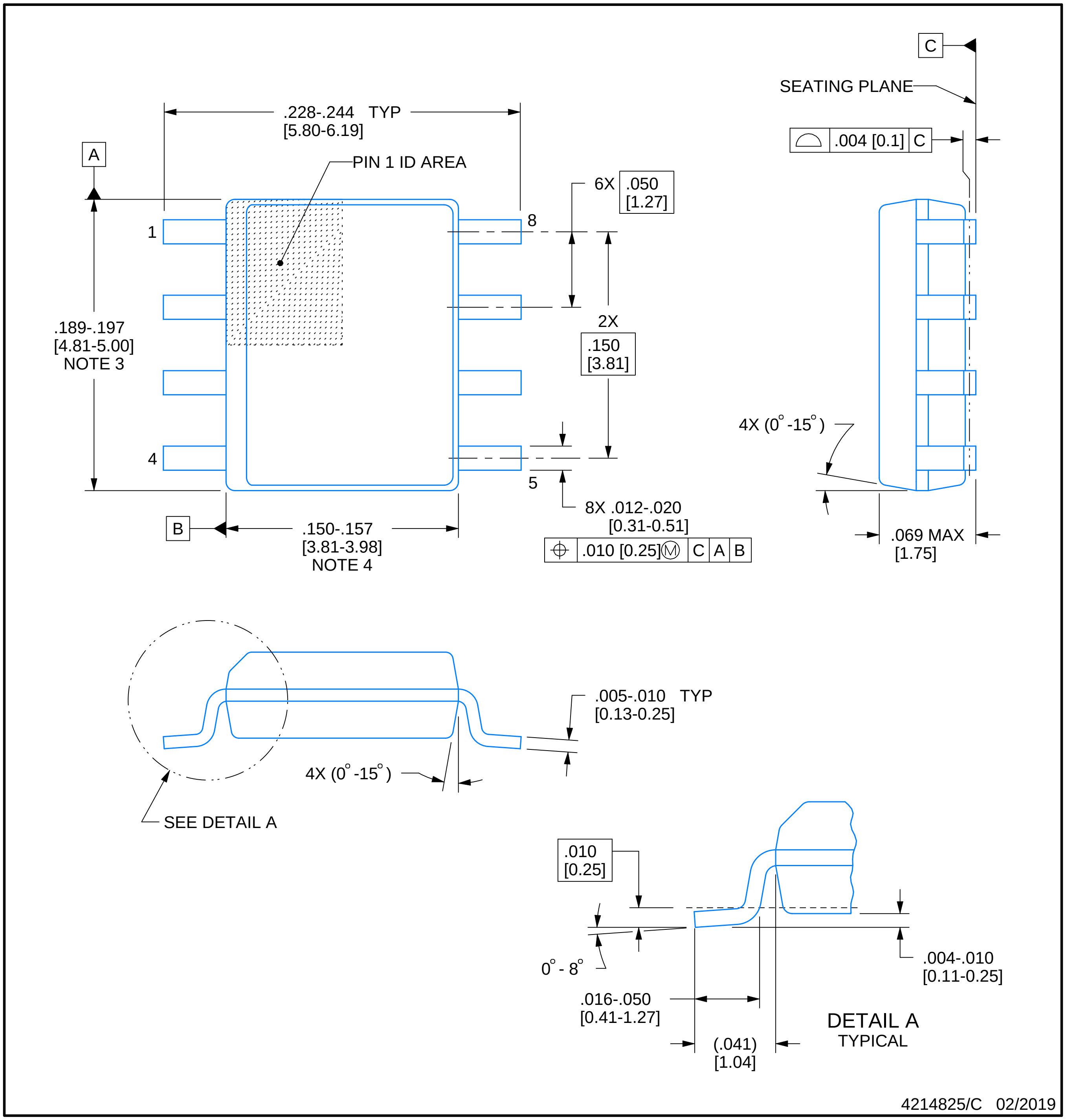
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM6172IN/NOPB | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |



# PACKAGE OUTLINE

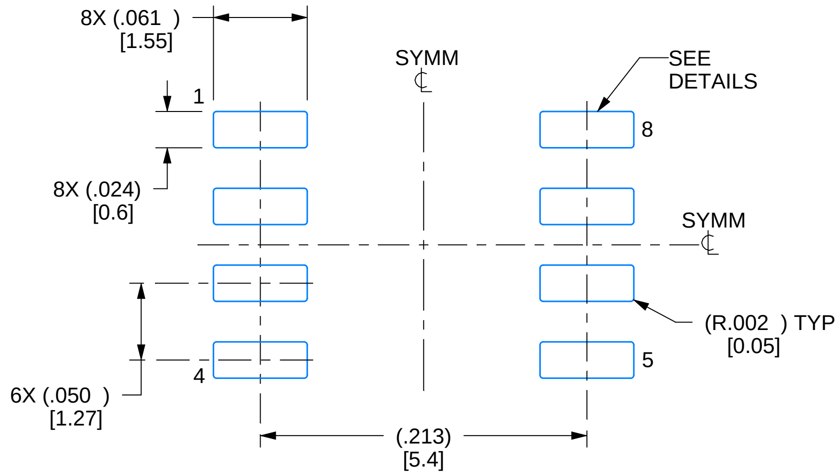
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

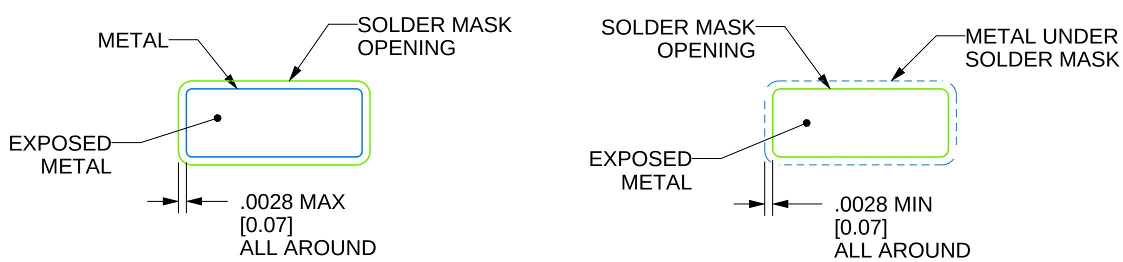



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




NON SOLDER MASK
DEFINED

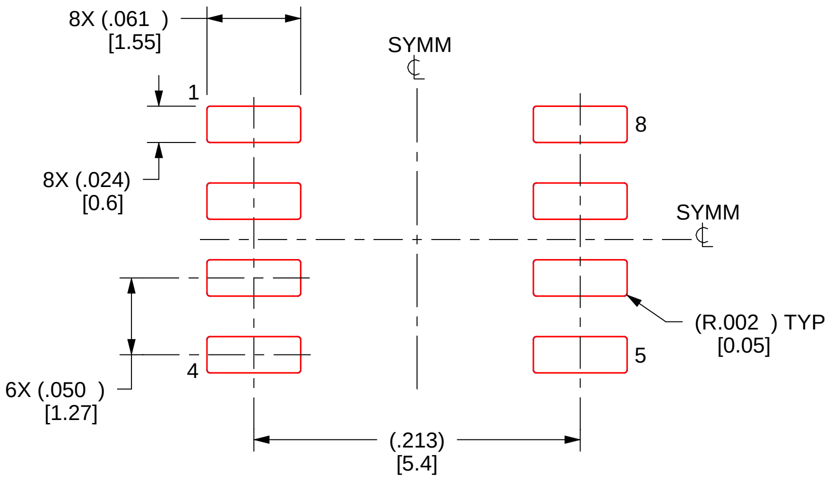
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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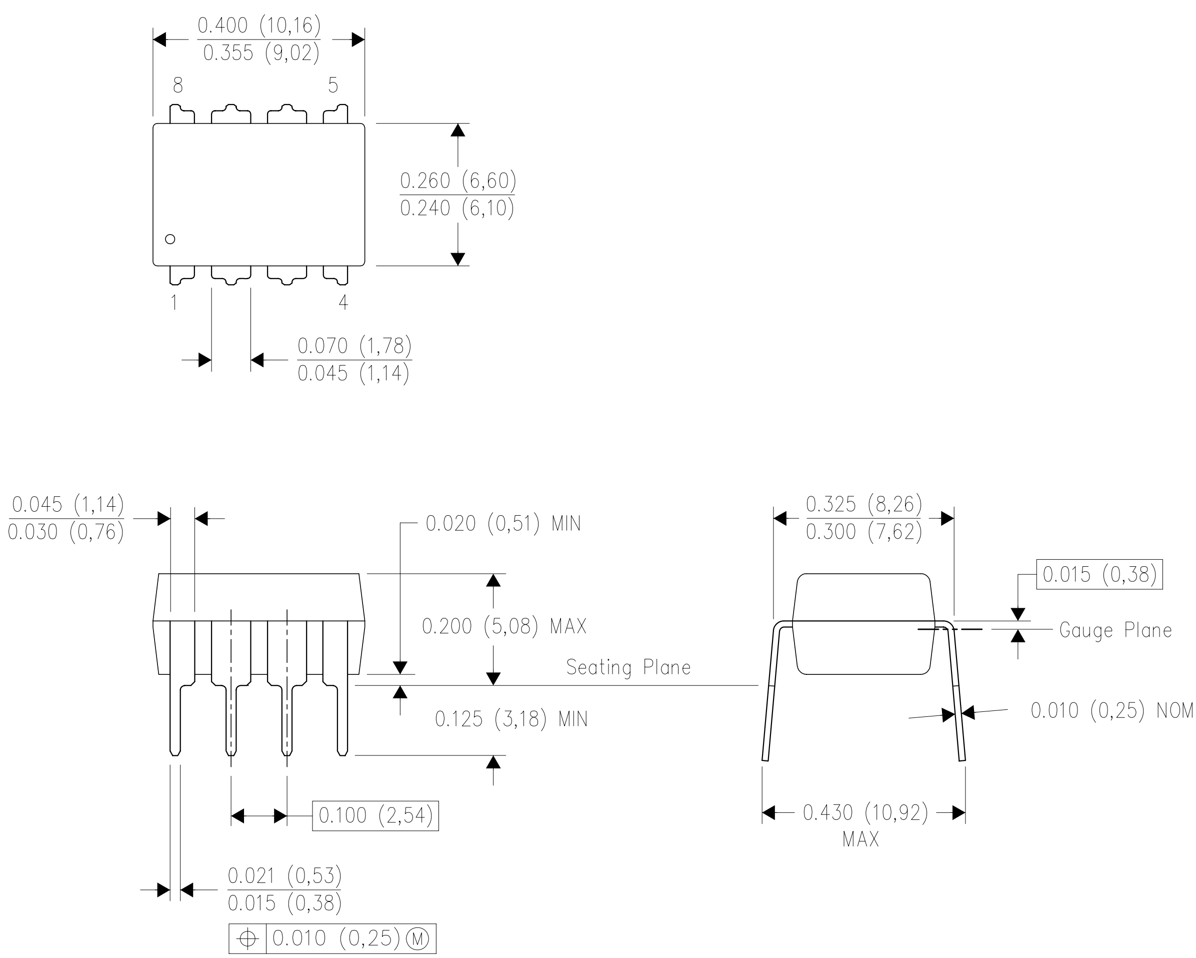
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE




4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

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